Micro SMD
Qualification Package

LM358, LMC6035, LM431, LM78L05, and LMC555

National's Micro SMD – The Obvious Answer For Portable Applications

Micro SMD Package
- 0.5mm Bump Pitch
- 0.9mm Max Package Height
- Eutectic Bump Reflow For Self-Alignment
- Coplanarity Guaranteed by Process
- The Die is the Package
- Epoxy Backcoating Provides Conventional Black Marking Surface

Ease of Manufacturing
- Uses Standard Surface Mount Equipment and Flow
- No Underfill Required
- Pick and Place Accuracy - 0.5mm Bump Pitch
- Available in Standard 8mm Tape and Reel
- Simplified PC Board Layout

Reliability
- Passes All Standard Product Reliability Tests:
  - OPL, THBT, Temp Cycle, Autoclave, and ESD
- Passes All Board Level Reliability Tests:
  - Drop, Vibration, and 3-Point Bend

For More Information on Micro SMD:
Visit Our Website at:
http://microsmd.national.com

Standard Surface Mount Packages vs. Micro SMD

Part #	Description
LM358BP	Low Power Dual **Op Amp**
LM431AIBP	Adjustable Precision Shunt **Regulator**
LMC555CBP	General Purpose CMOS **Timer**
LMC6035IBP	2.7V Dual CMOS **Op Amp**
LM78L05IBP	3-Terminal Positive **Regulator**

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MICRO SMD QUALIFICATION PACKAGE

April 2000

Table of Contents

1.0 LM358BP

1.1 Introduction

1.1.1 General Product Description 1-1-1
1.1.2 Technical Product Description 1-1-1
1.1.3 Reliability/Qualification Overview 1-1-1
1.1.4 Technical Assistance 1-1-1

1.2 Device Information

1.2.1 Datasheet 1-2-1
1.2.2 Die Photo 1-2-24

1.3 Process Information

1.3.1 Process Details 1-3-1
1.3.2 Process Masks Steps 1-3-1
1.3.3 Process Flow 1-3-1
1.3.4 Micro SMD Assembly Flow 1-3-2

1.4 Reliability Data

1.4.1 Reliability Report 1-4-1

2.0 LMC6035IBP

2.1 Introduction

2.1.1 General Product Description 2-1-1
2.1.2 Technical Product Description 2-1-1
2.1.3 Reliability/Qualification Overview 2-1-1
2.1.4 Technical Assistance 2-1-1

2.2 Device Information

2.2.1 Datasheet 2-2-1
2.2.2 Die Photo 2-2-21

2.3 Process Information

2.3.1 Process Outline 2-3-1
2.3.2 Process Detail & Masks 2-3-1
2.3.3 Assembly Flow 2-3-1

2.4 Reliability Data

2.4.1 Reliability Report 2-4-1

3.0 LM431AIBP

3.1 Introduction

3.1.1 General Product Description 3-1-1
3.1.2 Technical Product Description 3-1-1
3.1.3 Reliability/Qualification Overview 3-1-1
3.1.4 Technical Assistance 3-1-1

3.2 Device Information

3.2.1 Datasheet 3-2-1
3.2.2 Die Photo 3-2-14

3.3 Process Information

3.3.1 Process Details 3-3-1
3.3.2 Process Mask Steps 3-3-1
3.3.3 Process Flow 3-3-1
3.3.4 Micro SMD Assembly Flow 3-3-2

3.4 Reliability Data

3.4.1 Reliability Report 3-4-1

4.0 LM78L05IBP

4.1 Introduction

4.1.1 General Product Description 4-1-1
4.1.2 Technical Product Description 4-1-1
4.1.3 Reliability/Qualification Overview 4-1-1
4.1.4 Technical Assistance 4-1-1

4.2 Device Information

4.2.1 Datasheet 4-2-1
4.2.2 Die Photo 4-2-13

4.3 Process Information

4.3.1 Process Details 4-3-1
4.3.2 Masking Sequence 4-3-1
4.3.3 Process Flow 4-3-1
4.3.4 Micro SMD Assembly Flow 4-3-2

4.4 Reliability Data

4.4.1 Reliability Report 4-4-1

5.0 LMC555CBP

5.1 Introduction

5.1.1 General Product Description 5-1-1
5.1.2 Technical Product Description 5-1-1
5.1.3 Reliability/Qualification Overview 5-1-1
5.1.4 Technical Assistance 5-1-1

5.2 Device Information

5.2.1 Datasheet 5-2-1
5.2.2 Die Photo 5-2-13

5.3 Process Information

5.3.1 Process Details 5-3-1
5.3.2 Process Mask Steps 5-3-1
5.3.3 Process Flow 5-3-1
5.3.4 Micro SMD Assembly Flow 5-3-2

5.4 Reliability Data

5.4.1 Reliability Report 5-4-1

6.0 Packaging Information

6.1 Package Material

6.2 Package Dimensions

6.2.1 Reference Table 6-2-1
6.2.2 4-Bump Micro SMD Drawing 6-2-2
6.2.3 8-Bump Micro SMD Drawing 6-2-4

6.3 Tape & Reel Dimensions

6.3.1 Reference Table 6-3-1
6.3.2 Tape & Reel Drawing 6-3-2

7.0 Application Information

7.1 Application Note AN-1112 7-1-1

1.1 LM358BP INTRODUCTION

1.1.1 General Product Description

The LM358BP is a low power dual operational amplifier in the micro SMD (surface mount device) package. Although designed to operate from a single power supply over a wide range of voltages, operation from split power supplies is also possible.

Since the die is the package, the micro SMD is the smallest package possible, making it ideal for applications that can take advantage of a surface mount package that is smaller than SOT-23 and SC-70. The LM358 is also available in standard SOIC-8, DIP-8, and TO-5 packages. Please refer to the datasheet included in this booklet or visit National Semiconductor's website (http://www.national.com) for more information on those packages.

1.1.2 Technical Product Description

As with previous versions of the LM358, the LM358BP is manufactured using National's single-layer metal bipolar process.

National's name for the wafer-level chip-scale package used for the LM358 is micro SMD. Since assembly of the die is done at wafer level, there are additional wafer processing steps that are used instead of the usual assembly of a molded plastic surface mount package. These additional steps are covered under the Packaging Information section of this booklet.

The micro SMD version of the LM358 is assembled with 8 eutectic solder bumps (functioning as pins) on the active side of the die. The non-active side of the die is coated with epoxy and laser marked with a part number identification code, a die lot/date code, and a bump one identifier. The LM358 in micro SMD is shipped in standard 250 and 3,000 unit tape and reel. The devices are mounted on printed circuit boards bump side down using the same methods as other small surface mount packages.

For more information concerning application and use of the micro SMD package, please refer to Application Note AN-1112 included in this booklet.

1.1.3 Reliability/Qualification Overview

The LM358 is re-laid out (die rev E) so as to provide necessary spacing between the bond pads that enables proper surface mounting of this die. To qualify this new die, one lot of the micro SMD device was fabricated and mounted on conversion boards to be tested through OPL. Additional units was also ESD tested.

1.1.4 Technical Assistance

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Tel: 1-800-272-9959
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Email: support@nsc.com

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Fax: 81-3-5639-7507

Asia Pacific
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Email: sea.support@nsc.com
Tel: 65-2544466
(IDD telephone charge to be paid by caller)

See us on the Worldwide Web @ http://www.national.com

1.2 DEVICE INFORMATION

1.2.1 Datasheet

National Semiconductor

January 2000

LM158/LM258/LM358/LM2904
Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

The LM358 is also available in a chip sized package (8-Bump micro SMD) using National's micro SMD package technology.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

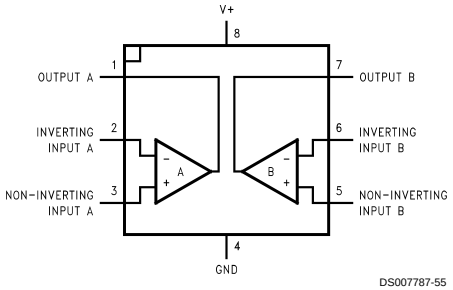
- Two internally compensated op amps
- Eliminates need for dual supplies
- Allows direct sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual op amp

Features

- Available in 8-Bump micro SMD chip sized package, (See AN-1112)
- Internally frequency compensated for unity gain
- Large dc voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature compensated)
- Wide power supply range:
  — Single supply: 3V to 32V
  — or dual supplies: ±1.5V to ±16V
- Very low supply current drain (500 µA) — essentially independent of supply voltage
- Low input offset voltage: 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing: 0V to V^+ − 1.5V

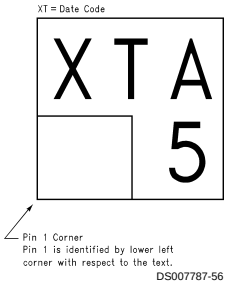
Connection Diagrams

8-Bump micro SMD



Top View
(Bump Side Down)

micro SMD Marking Orientation

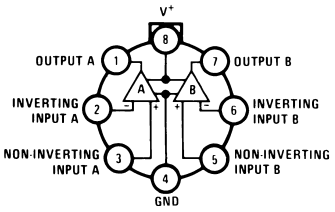


Bumps are numbered counter-clockwise.

Top View

Connection Diagrams (Continued)

Metal Can Package



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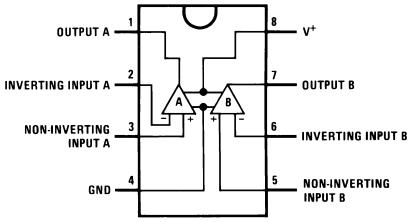
Top View

DIP/SO Package



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Top View

Ordering Information

Package	Temperature Range				NSC Drawing
	−55˚C to 125˚C	−25˚C to 85˚C	0˚C to 70˚C	−40˚C to 85˚C	
SO-8			LM358AM LM358M	LM2904M	M08A
8-Pin Molded DIP			LM358AN LM358N	LM2904N	N08E
8-Pin Ceramic DIP	LM158AJ/883(Note 1) LM158J/883(Note 1) LM158J LM158AJLQML(Note 2) LM158AJQMLV(Note 2)				J08A
TO-5, 8-Pin Metal Can	LM158AH/883(Note 1) LM158H/883(Note 1) LM158AH LM158H LM158AHLQML(Note 2) LM158AHLQMLV(Note 2)	LM258H	LM358H		H08C
8-Bump micro SMD			LM358BP LM358BPX		BPA08AAA

Note 1: LM158 is available per SMD #5962-8771001

LM158A is available per SMD #5962-8771002

Note 2: See STD Mil DWG 5962L87710 for Radiation Tolerant Devices

Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 3)		
Molded DIP	830 mW	830 mW
Metal Can	550 mW	
Small Outline Package (M)	530 mW	530 mW
micro SMD	435mW	
Output Short-Circuit to GND		
(One Amplifier) (Note 4)		
$V^+ \leq 15V$ and $T_A = 25^\circ C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3V$) (Note 5)	50 mA	50 mA
Operating Temperature Range		
LM358	0˚C to +70˚C	−40˚C to +85˚C
LM258	−25˚C to +85˚C	
LM158	−55˚C to +125˚C	
Storage Temperature Range	−65˚C to +150˚C	−65˚C to +150˚C
Lead Temperature, DIP		
(Soldering, 10 seconds)	260˚C	260˚C
Lead Temperature, Metal Can		
(Soldering, 10 seconds)	300˚C	300˚C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260˚C	260˚C
Small Outline Package		
Vapor Phase (60 seconds)	215˚C	215˚C
Infrared (15 seconds)	220˚C	220˚C
See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.		
ESD Tolerance (Note 12)	250V	250V

Electrical Characteristics

$V^+ = +5.0V$, unless otherwise stated

Parameter	Conditions	LM158A			LM358A			LM158/LM258			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 7), $T_A = 25^\circ C$		1	2		2	3		2	5	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25^\circ C$, $V_{CM} = 0V$, (Note 8)		20	50		45	100		45	150	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25^\circ C$		2	10		5	30		3	30	nA
Input Common-Mode Voltage Range	$V^+ = 30V$, (Note 9) (LM2904, $V^+ = 26V$), $T_A = 25^\circ C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range										
	$R_L = \infty$ on All Op Amps										
	$V^+ = 30V$ (LM2904 $V^+ = 26V$)		1	2		1	2		1	2	mA
	$V^+ = 5V$		0.5	1.2		0.5	1.2		0.5	1.2	mA

Electrical Characteristics

V^+ = +5.0V, unless otherwise stated

Parameter	Conditions	LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 7) , T_A = 25˚C		2	7		2	7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, T_A = 25˚C, V_{CM} = 0V, (Note 8)		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V, T_A = 25˚C		5	50		5	50	nA
Input Common-Mode Voltage Range	V^+ = 30V, (Note 9) (LM2904, V^+ = 26V), T_A = 25˚C	0		V^+−1.5	0		V^+−1.5	V
Supply Current	Over Full Temperature Range R_L = ∞ on All Op Amps							
	V^+ = 30V (LM2904 V^+ = 26V)		1	2		1	2	mA
	V^+ = 5V		0.5	1.2		0.5	1.2	mA

Electrical Characteristics

V^+ = +5.0V, (Note 6), unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = 15V, T_A = 25˚C, $R_L \geq 2$ kΩ, (For V_O = 1V to 11V)	50	100		25	100		50	100		V/mV
Common-Mode Rejection Ratio		T_A = 25˚C, V_{CM} = 0V to V^+−1.5V	70	85		65	85		70	85		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2904, V^+ = 5V to 26V), T_A = 25˚C	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, T_A = 25˚C (Input Referred), (Note 10)		−120			−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25˚C	20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V V^+ = 15V, T_A = 25˚C, V_O = 2V	10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V T_A = 25˚C, V_O = 200 mV, V^+ = 15V	12	50		12	50		12	50		µA
Short Circuit to Ground		T_A = 25˚C, (Note 4), V^+ = 15V		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 7)			4			5			7	mV
Input Offset Voltage Drift		R_S = 0Ω		7	15		7	20		7		µV/˚C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100	nA
Input Offset Current Drift		R_S = 0Ω		10	200		10	300		10		pA/˚C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	200		40	300	nA
Input Common-Mode Voltage Range		V^+ = 30 V, (Note 9) (LM2904, V^+ = 26V)	0		V^+−2	0		V^+−2	0		V^+−2	V

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 6), unless otherwise stated

Parameter		Conditions		LM158A			LM358A			LM158/LM258			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = +15V (V_O = 1V to 11V) $R_L \geq 2\ k\Omega$		25			15			25			V/mV
Output Voltage Swing	V_{OH}	V^+ = +30V	R_L = 2 kΩ	26			26			26			V
		(LM2904, V^+ = 26V)	R_L = 10 kΩ	27	28		27	28		27	28		V
	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V		10	20		10	20		10	20		mA
	Sink	V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V		10	15		5	8		5	8		mA

Electrical Characteristics

V^+ = +5.0V, (Note 6), unless otherwise stated

Parameter		Conditions	LM358			LM2904			Units
			Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = 15V, T_A = 25˚C, $R_L \geq 2\ k\Omega$, (For V_O = 1V to 11V)	25	100		25	100		V/mV
Common-Mode Rejection Ratio		T_A = 25˚C, V_{CM} = 0V to V^+−1.5V	65	85		50	70		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2904, V^+ = 5V to 26V), T_A = 25˚C	65	100		50	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, T_A = 25˚C (Input Referred), (Note 10)		−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25˚C	20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V V^+ = 15V, T_A = 25˚C, V_O = 2V	10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V T_A = 25˚C, V_O = 200 mV, V^+ = 15V	12	50		12	50		µA
Short Circuit to Ground		T_A = 25˚C, (Note 4), V^+ = 15V		40	60		40	60	mA
Input Offset Voltage		(Note 7)			9			10	mV
Input Offset Voltage Drift		R_S = 0Ω		7			7		µV/˚C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			150		45	200	nA
Input Offset Current Drift		R_S = 0Ω		10			10		pA/˚C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	500		40	500	nA
Input Common-Mode Voltage Range		V^+ = 30 V, (Note 9) (LM2904, V^+ = 26V)	0		V^+−2	0		V^+ −2	V

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 6), unless otherwise stated

Parameter		Conditions		LM358			LM2904			Units
				Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = +15V (V_O = 1V to 11V) $R_L \geq 2\ k\Omega$		15			15			V/mV
Output Voltage	V_{OH}	V^+ = +30V	R_L = 2 kΩ	26			22			V
		(LM2904, V^+ = 26V)	R_L = 10 kΩ	27	28		23	24		V
Swing	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	100	mV
Output Current	Source	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V		10	20		10	20		mA
	Sink	V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V		5	8		5	8		mA

Note 3: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125˚C maximum junction temperature and a thermal resistance of 120˚C/W for MDIP, 182˚C/W for Metal Can, 189˚C/W for Small Outline package, and 230˚C/W for micro SMD, which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150˚C maximum junction temperature. The dissipation is the total of both amplifiers — use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 4: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 5: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25˚C).

Note 6: These specifications are limited to −55˚C ≤ T_A ≤ +125˚C for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to −25˚C ≤ T_A ≤ +85˚C, the LM358/LM358A temperature specifications are limited to 0˚C ≤ T_A ≤ +70˚C, and the LM2904 specifications are limited to −40˚C ≤ T_A ≤ +85˚C.

Note 7: $V_O \cong$ 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ −1.5V) at 25˚C. For LM2904, V^+ from 5V to 26V.

Note 8: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 9: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25˚C). The upper end of the common-mode voltage range is V^+ −1.5V (at 25˚C), but either or both inputs can go to +32V without damage (+26V for LM2904), independent of the magnitude of V^+.

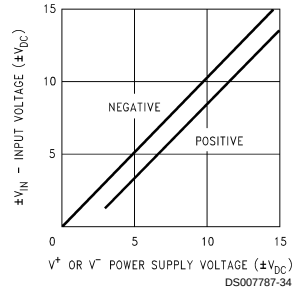
Note 10: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 11: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

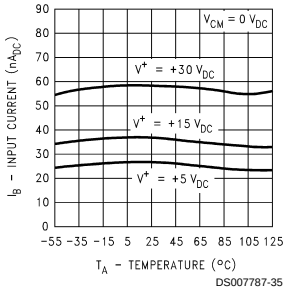
Note 12: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

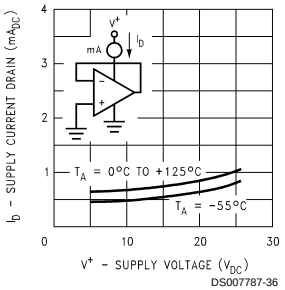
Input Voltage Range



Input Current

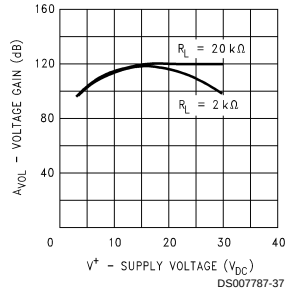


Supply Current



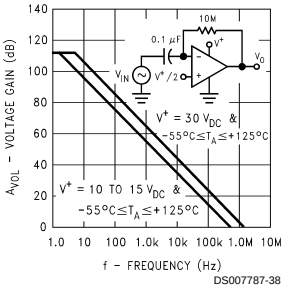
Typical Performance Characteristics (Continued)

Voltage Gain



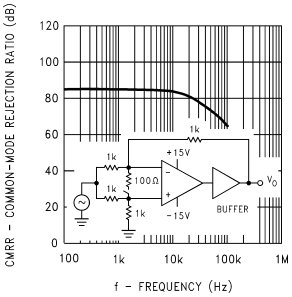
DS007787-37

Open Loop Frequency Response



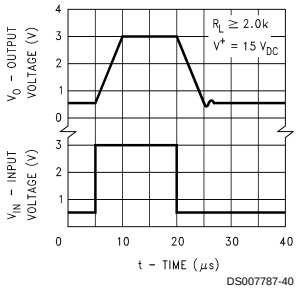
DS007787-38

Common-Mode Rejection Ratio



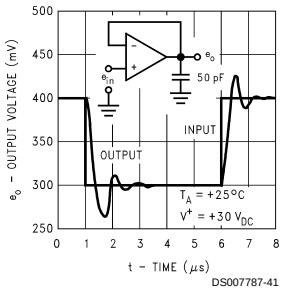
DS007787-39

Voltage Follower Pulse Response



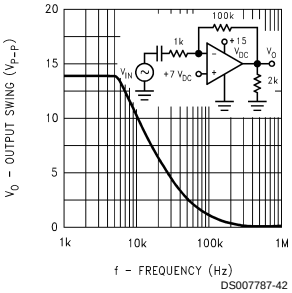
DS007787-40

Voltage Follower Pulse Response (Small Signal)



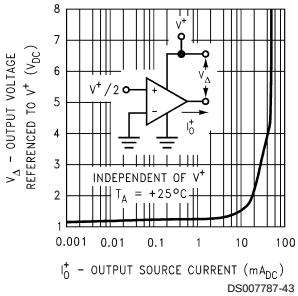
DS007787-41

Large Signal Frequency Response



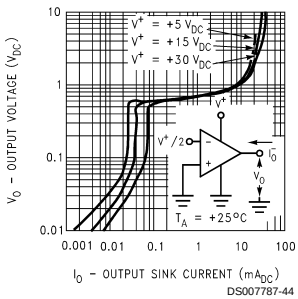
DS007787-42

Output Characteristics Current Sourcing



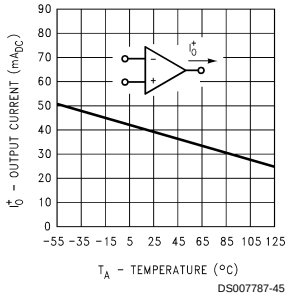
DS007787-43

Output Characteristics Current Sinking



DS007787-44

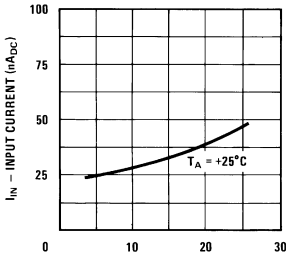
Current Limiting



DS007787-45

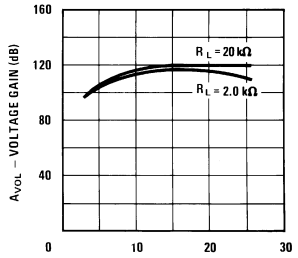
Typical Performance Characteristics (Continued)

Input Current (LM2902 only)



DS007787-46

Voltage Gain (LM2902 only)



DS007787-47

Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

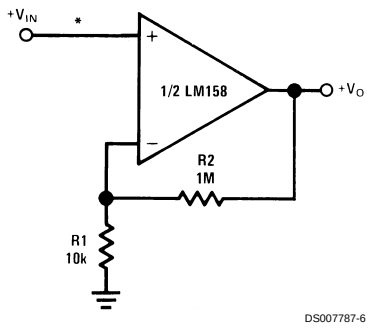
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

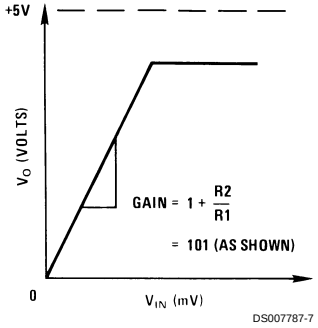
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications (V^+ = 5.0 V_{DC})

Non-Inverting DC Gain (0V Output)



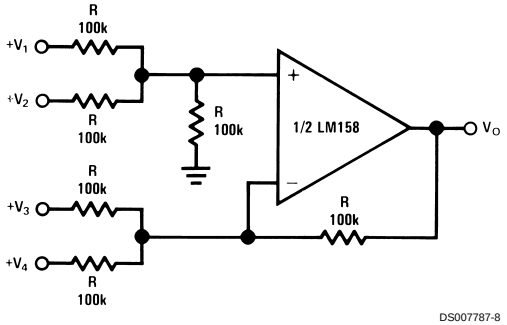
DS007787-6



DS007787-7

*R not needed due to temperature independent I_{IN}

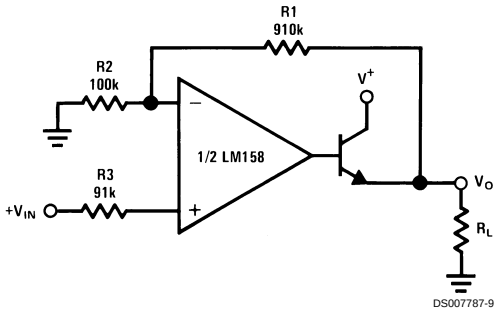
DC Summing Amplifier
(V_{IN}'S ≥ 0 V_{DC} and V_O ≥ 0 V_{DC})



DS007787-8

Where: $V_O = V_1 + V_2 + V_3 + V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0$ V_{DC}

Power Amplifier

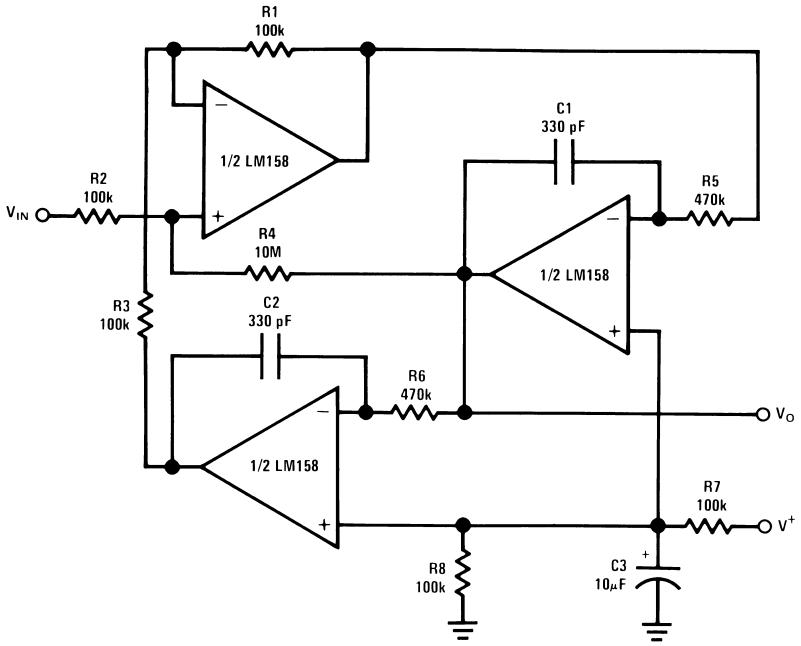


DS007787-9

V_O = 0 V_{DC} for V_{IN} = 0 V_{DC}
A_V = 10

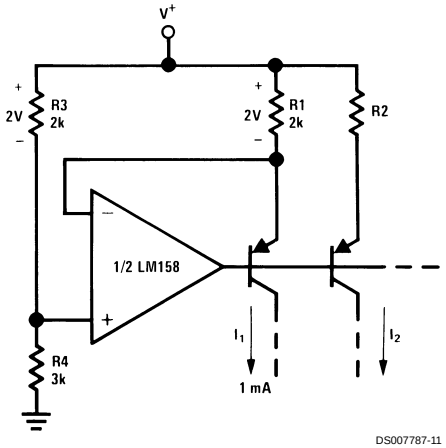
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

"BI-QUAD" RC Active Bandpass Filter



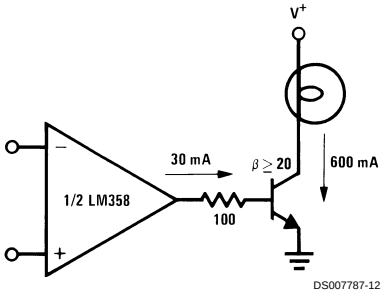
f_o = 1 kHz
Q = 50
A_V = 100 (40 dB)

Fixed Current Sources



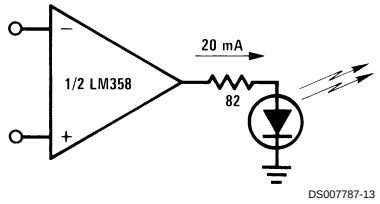
$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Lamp Driver



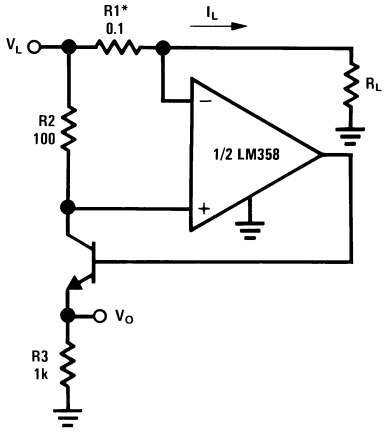
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

LED Driver



DS007787-13

Current Monitor

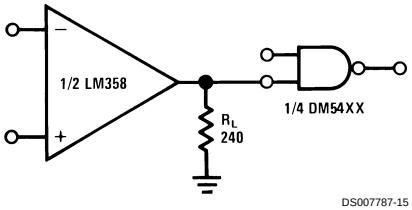


DS007787-14

$$V_O = \frac{1V\ (I_L)}{1A}$$

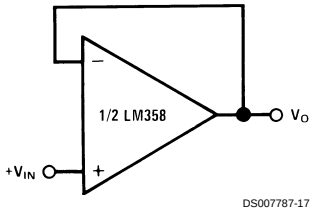
*(Increase R1 for I_L small)
$V_L \leq V^+ - 2V$

Driving TTL



DS007787-15

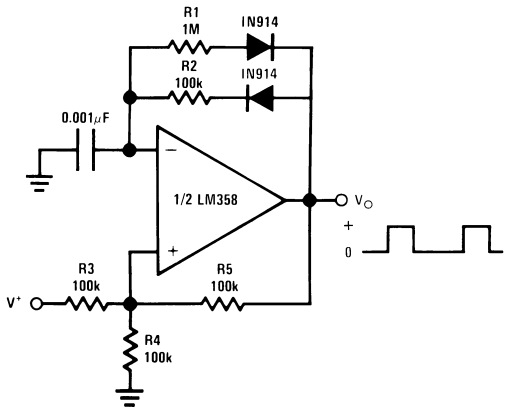
Voltage Follower



DS007787-17

$V_O = V_{IN}$

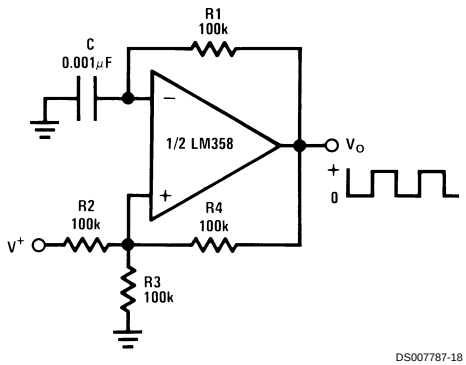
Pulse Generator



DS007787-16

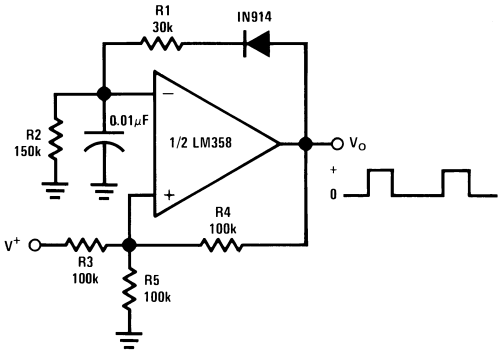
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Squarewave Oscillator



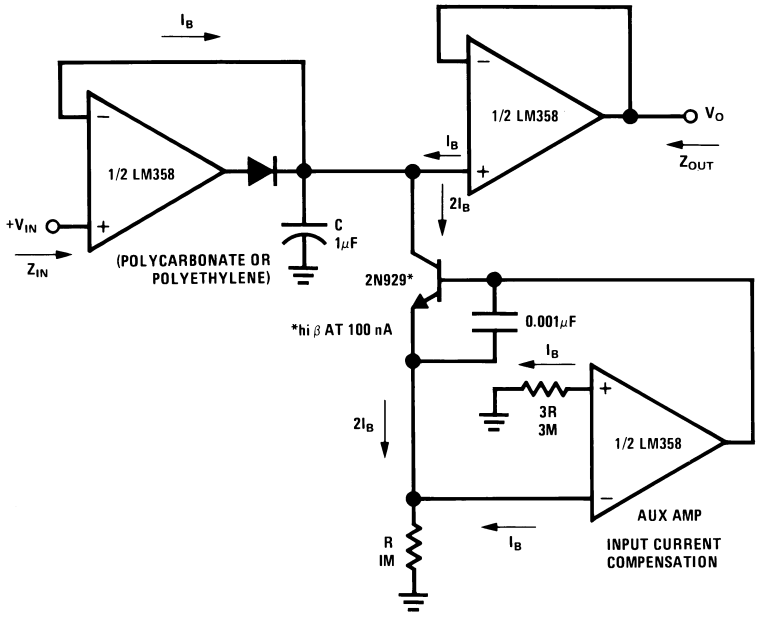
DS007787-18

Pulse Generator



DS007787-19

Low Drift Peak Detector

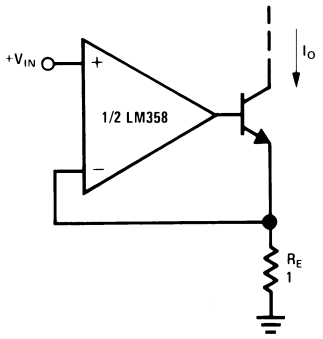


DS007787-20

HIGH Z_{IN}
LOW Z_{OUT}

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

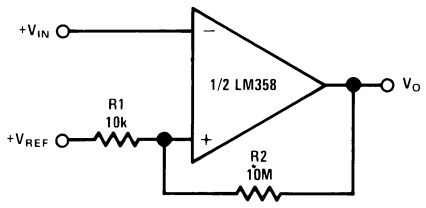
High Compliance Current Sink



DS007787-21

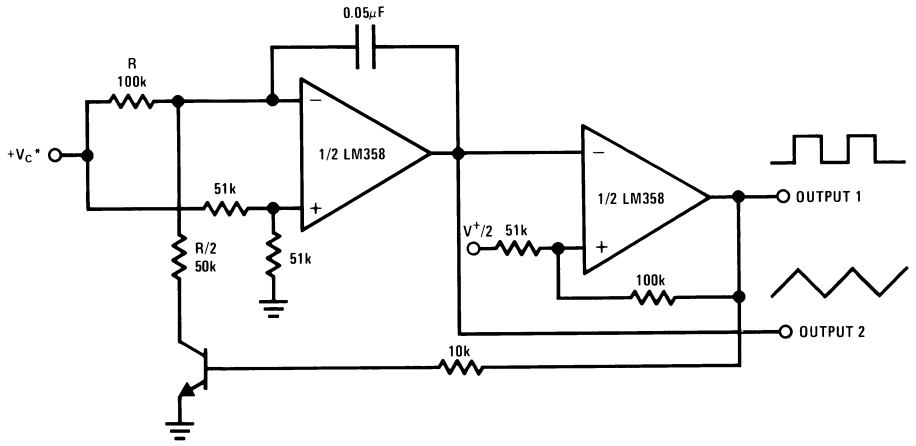
I_O = 1 amp/volt V_{IN}
(Increase R_E for I_O small)

Comparator with Hysteresis



DS007787-22

Voltage Controlled Oscillator (VCO)

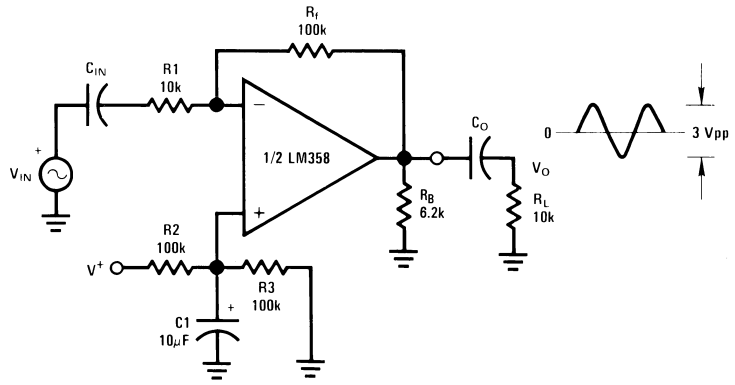


DS007787-23

*WIDE CONTROL VOLTAGE RANGE: 0 $V_{DC} \le V_C \le 2$ ($V^+ - 1.5V_{DC}$)

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

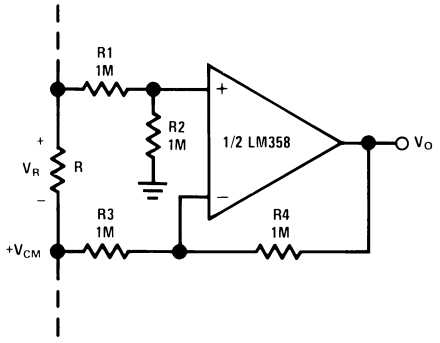
AC Coupled Inverting Amplifier



DS007787-24

$A_V = \frac{R_f}{R1}$ (As shown, A_V = 10)

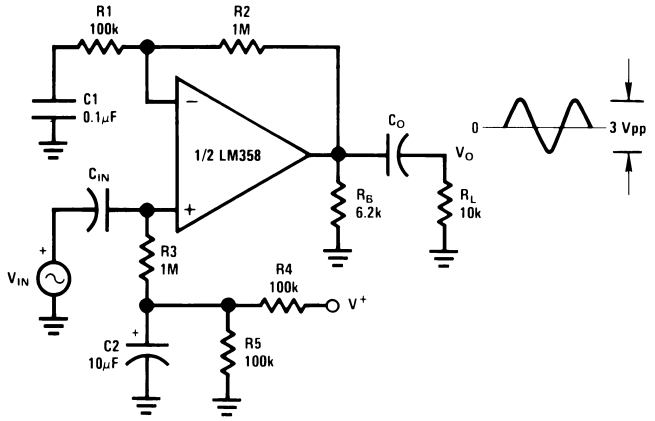
Ground Referencing a Differential Input Signal



DS007787-25

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

AC Coupled Non-Inverting Amplifier

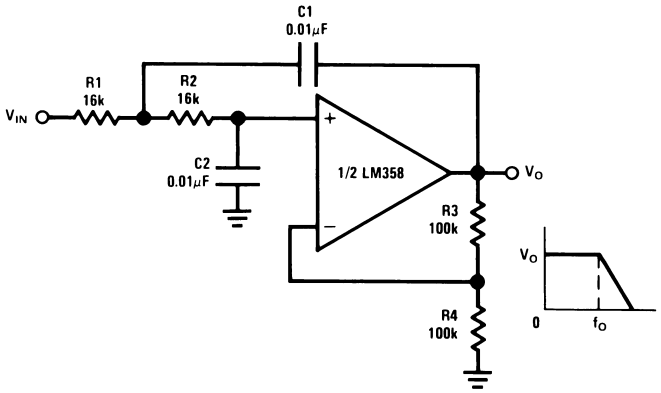


DS007787-26

$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (As Shown)

DC Coupled Low-Pass RC Active Filter

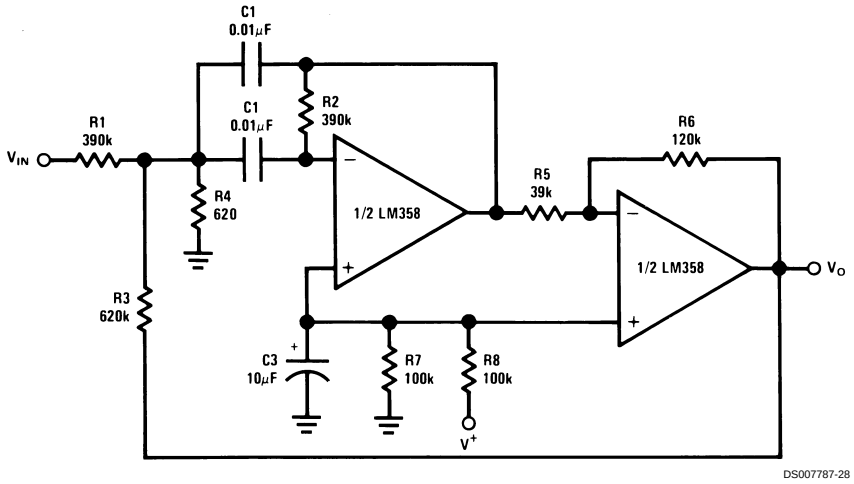


DS007787-27

f_o = 1 kHz
Q = 1
A_V = 2

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

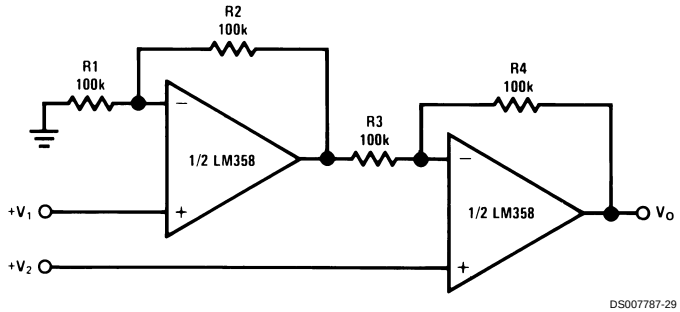
Bandpass Active Filter



DS007787-28

f_o = 1 kHz
Q = 25

High Input Z, DC Differential Amplifier



DS007787-29

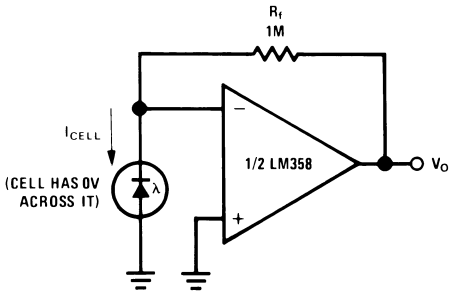
For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3} (V_2 - V_1)$

As Shown: $V_O = 2 (V_2 - V_1)$

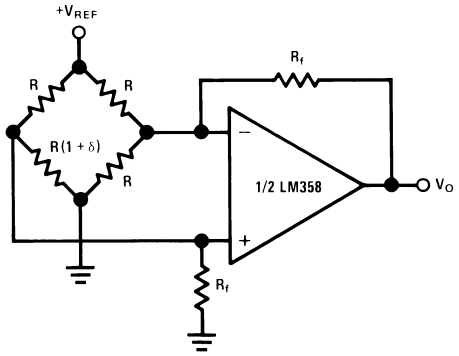
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Photo Voltaic-Cell Amplifier



DS007787-30

Bridge Current Amplifier

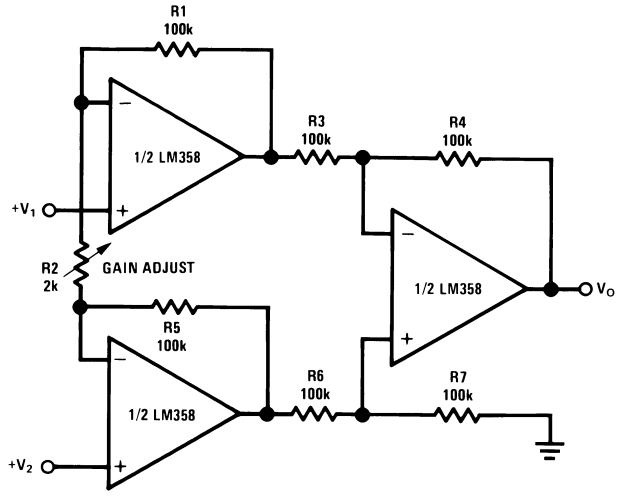


DS007787-33

For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

High Input Z Adjustable-Gain DC Instrumentation Amplifier



DS007787-31

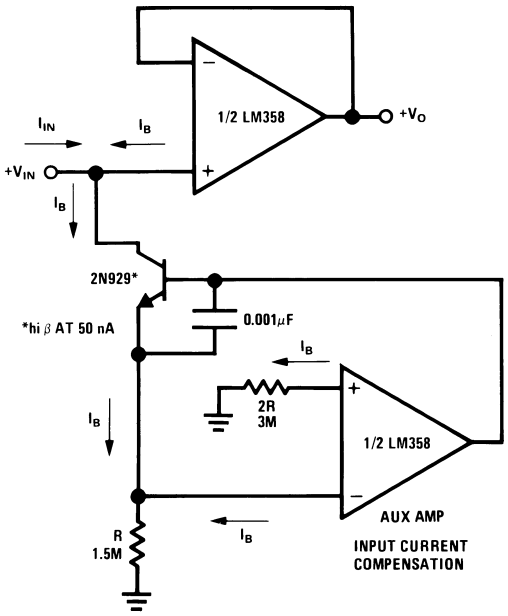
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101\,(V_2 - V_1)$

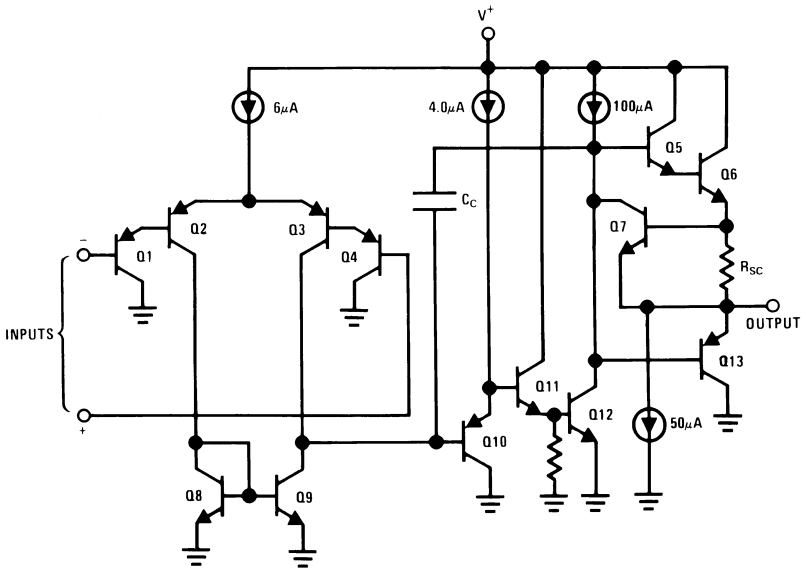
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



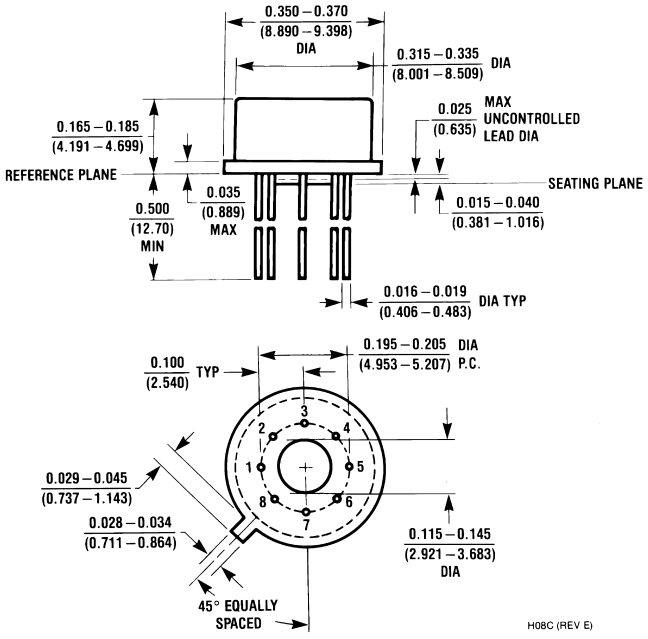
DS007787-32

Schematic Diagram (Each Amplifier)

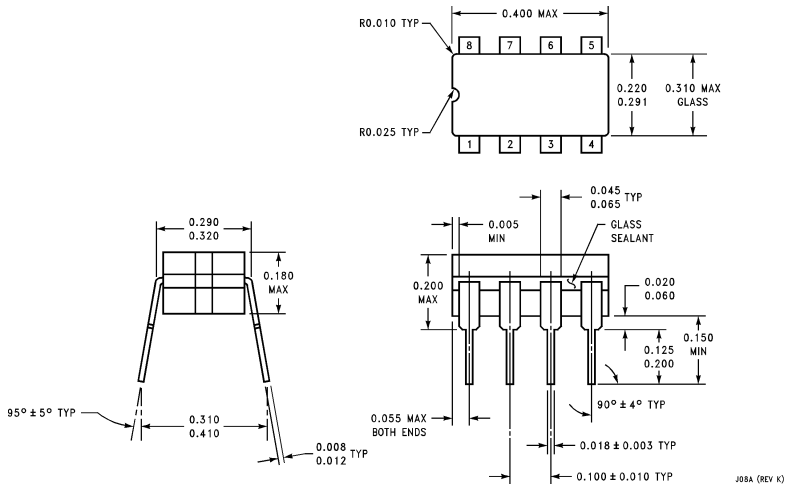


DS007787-3

Physical Dimensions inches (millimeters) unless otherwise noted

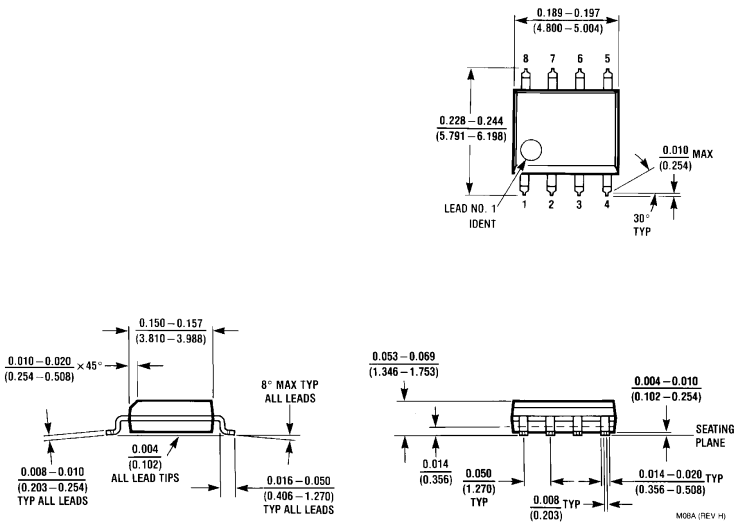


Metal Can Package (H)
Order Number LM158AH, LM158AH/883, LM158H, LM158H/883, LM258H or LM358H
NS Package Number H08C



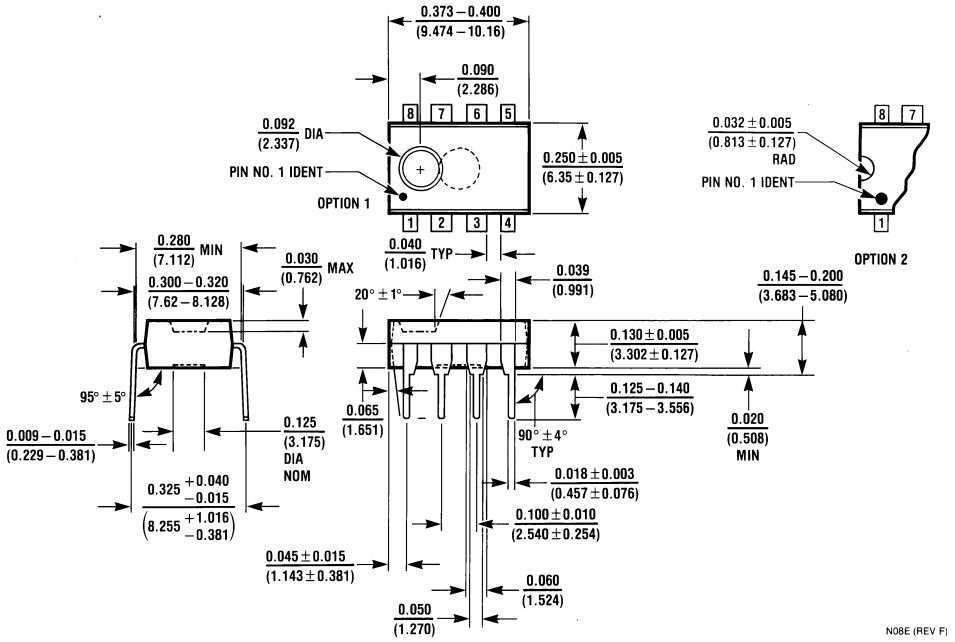
Cerdip Package (J)
Order Number LM158J, LM158J/883, LM158AJ or LM158AJ/883
NS Package Number J08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



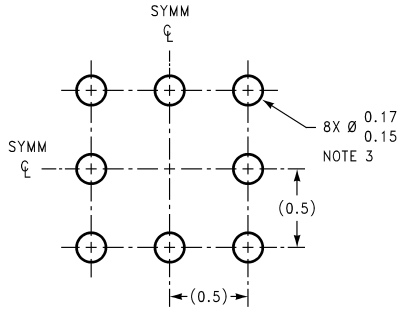
S.O. Package (M)
Order Number LM358M, LM358AM or LM2904M
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

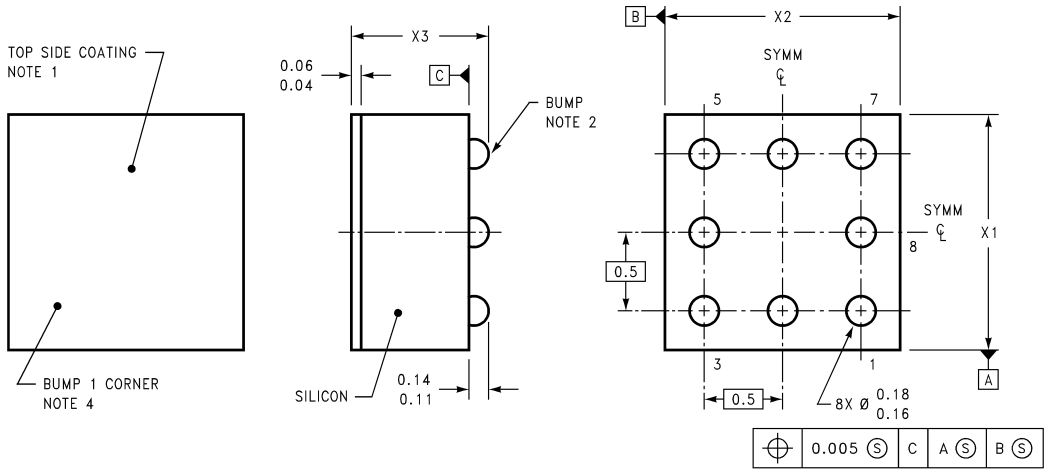


Molded Dip Package (N)
Order Number LM358AN, LM358N or LM2904N
NS Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS BPA08XXX (REV A)

NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION REMAINING PINS ARE NUMBERED COUNTERCLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X_1 IS PACKAGE WIDTH, X_2 IS PACKAGE LENGTH AND X_3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

8-Bump micro SMD
NS Package Number BPA08AAA
X_1 = 1.285 X_2 = 1.285 X_3 = 0.700

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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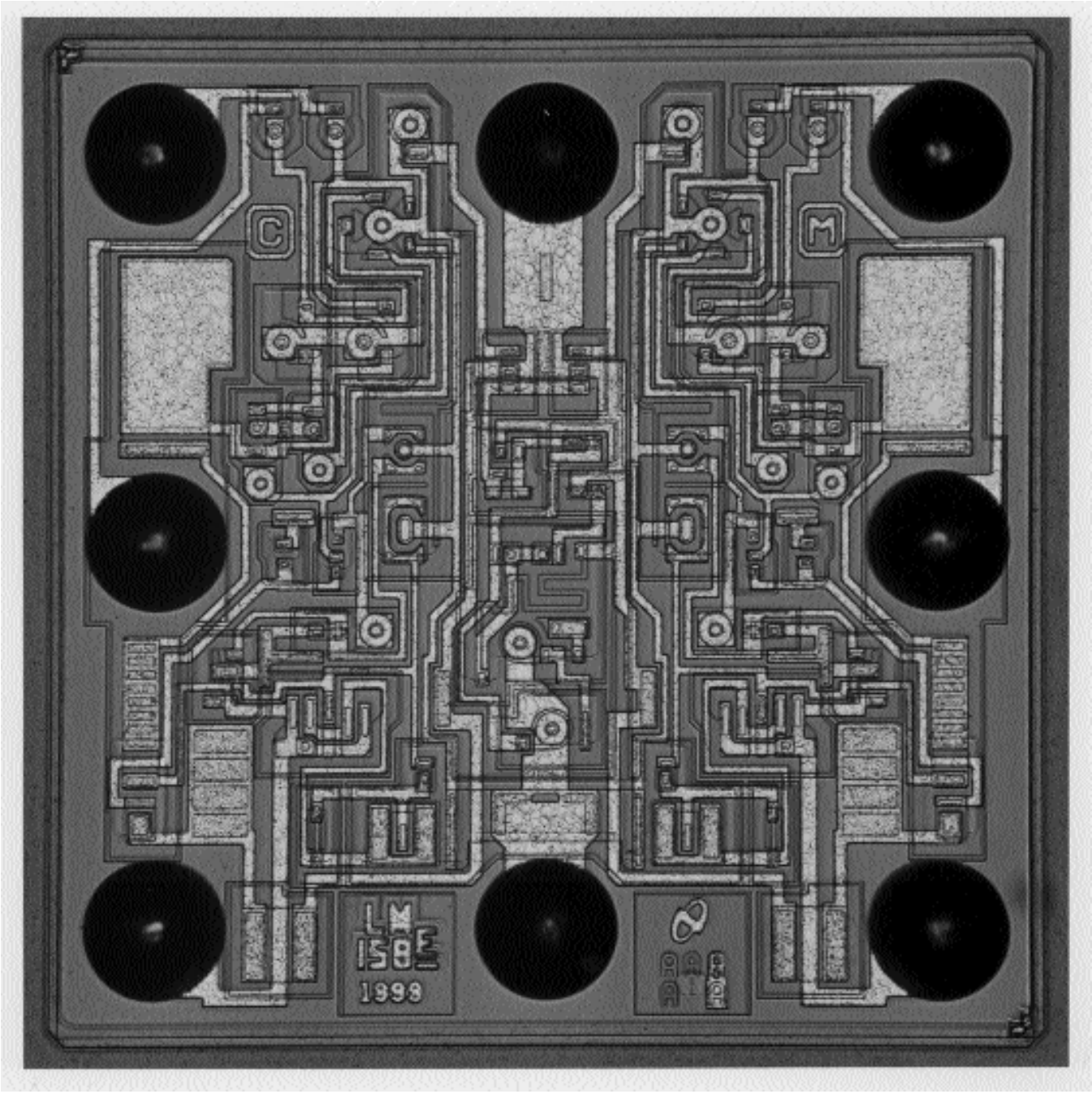
Fax: 81-3-5639-7507

1.2.2 Die Photo



1.3 PROCESS INFORMATION

1.3.1 Process Details

Fabrication site	Greenock, Scotland
Process Technology	Bipolar SLM
Wafer Diameter	4 inches
Number of Masks	9
Starting Material Substrate	P-type <111>
Metalization	0.5% CuAl
Passivation	10KA VOM
	10KA Plasma Nitride

1.3.2 Process Mask Steps

Mask #	**Name**
10	Collector
20	Isolation
30	Base
40	Emitter
41	Resistor Implant
42	Capacitor
50	Contact
60	Metal
70	Pad

1.3.3 Process Flow

1. Initial Oxidation
2. Mask 10
3. SB implant
4. SB drive
5. Epitaxial growth
6. Epitaxial re-oxidation
7. Mask 20
8. Iso Predeposition
9. Iso drive
10. FTA implant
11. Mask 30
12. Pre base oxidation
13. Base implant
14. Base diffusion
15. Mask 40
16. Emitter diffusion
17. Mask 41
18. Ion implant
19. VOE
20. Getter
21. Mask 42
22. Mosox
23. Mask 50
24. 0.5% CuAl sputter
25. Mask 60
26. VOM
27. Plasma Nitride
28. Mask 70
29. EOL Anneal
30. Wafer test

1.3.4 Micro SMD Assembly Flow

1: Receive into Bump Assembly Processing	[wafer level]
2: 2nd Passivation	[wafer level]
3: Passivation Mask	[wafer level]
4: Passivation Etch	[wafer level]
5: UBM (under bump metal) Application	[wafer level]
6: UBM Etch	[wafer level]
7: Solder Bump Application	[wafer level]
8: Solder Bump Reflow	[wafer level]
9: Epoxy Back Side	[wafer level]
10: Laser Mark Back Side	[wafer level]
11: Electric Test	[wafer level]
12: Saw Scribe Singulation	[wafer level]
13: Pack in Tape/Reel	[individual part level]

1.4 RELIABILITY DATA

1.4.1 Reliability Report

National Semiconductor

Reliability Test Report

File Number:
FSC19990318
Originator:
Alex Ruiz
Date: September 9, 1999

Purpose

Qualification of the redesigned LM358 in the 8-bump micro SMD package.

Approvals

Reliability Engineer	Date
Reliability Engineering Manager	Date
Product Line Engineer	Date
Product Line Engineering Manager	Date
Product Line General Manger	Date
Product Line V.P.	Date
Corporate Reliability Director	Date
QA&R V.P.	Date

Reference File Numbers

RSC199902251
Q19990216

FSC19980255
Q19980548

Distribution List

Standard Analog Product Group:
Doug Simin, Frank Smoot, Sharon Ignaut

QA&R:
MN Bhatt, Richard Rosales, Gil Alcaraz, Violetta Luis, Alex Ruiz

Abstract

The Micro Surface Mount Device (micro SMD) is a version of a wafer level chip scale package where the package-size is the same as that of the die. Electrical connection to the outside world is made through solder bump construction on the Aluminum bond pad, where the die is flipped to solder on to the printed circuit board. The passivation and the BCB, along with the solder bumps form a protective barrier for the active area of the die from outside world contaminants. An Epoxy back coat done to the backside of the die is used for marking.

The LM358 is re-laid out (die rev E) so as to provide necessary spacing between the bond pads that enables proper surface mounting of this die. To qualify this new die, one lot of the micro SMD device was fabricated and mounted on conversion boards to be tested through OPL. Additional units was also ESD tested.

1.5 RELIABILITY DATA

The 8-bump micro SMD package was qualified by extension to the successful LMC6035 8-bump qualification (Q19980548, FSC19980255).

1) The LM358 has passed 500 hours OPL with no failure.
2) After completion of all ESD testing, it was found that the device only has 400V HBM ESD rating. This data shows that the ESD rating is better than the control unit 300V HBM ESD rating. Based on the HBM ESD comparison, the redesigned die has no impact on HBM ESD capability.
3) The datasheet for the LM358 states 250V HBM ESD rating – a rating lower than the current ESD data.
4) There has been no PQA in the last year for ESD related failure for the LM358 device.

In summary, the LM358 is being released to production with a waiver for HBM ESD performance with no corrective action required.

Description

Test Request	Device Name	Sbgp	Wafer Die Run	Fab Loc	Tech Code	Pkg Code	# Leads	Assy Loc	Date Cd	Mold Cmpnd
RSC199902251	LM358IBP	A	micro SMD	UK	LF	C\SSWA	8	SC	9912	N/A
RSC199902251	LM358IBP	B	Control	UK	LF	C\SSWA	8	SC	9912	N/A
RSC199902251	LM358N	A	micro SMD	UK	LF	N\MDIP	8	SC	9912	B8
RSC199902251	LM358N	B	Control	UK	LF	N\MDIP	8	SC	9912	B8

Tests Performed

```
Test: Operating Life Test (Static) (SOPL)
   Test Request    Device            Sbgrp  High Temp
   RSC199902251 LM358IBP            A      125
   RSC199902251 LM358IBP            B      125
                Board Circuit: 01589RE     Voltage: Vcc=+/-15V    Current: Icc=1mA

   Timepoints:     Test Request      TP     Duration
                   RSC199902251      1      168
                   RSC199902251      2      500

Test: Electrostatic Discharge - Human Body Model (ESDH)
   Test Request    Device            Method
   RSC199902251 LM358N               ATE
   (Tst# 1)        Sublot            Voltage
                   1                 150
                   2                 200
                   3                 250
                   4                 300
                   5                 400
                   6                 500

Test: Electrostatic Discharge - Machine Model (ESDM)
   Test Request    Device            Method
   RSC199902251 LM358N               ATE
   (Tst# 2)        Sublot            Voltage
                   1                 50
                   2                 100
                   3                 150
                   4                 200
                   5                 250
```

Results/Discussion

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199902251	LM358IBP	A	1	168	100	0
RSC199902251	LM358IBP	A	2	500	100	0
RSC199902251	LM358IBP	B	1	168	25	0
RSC199902251	LM358IBP	B	2	500	25	0

Test: Electrostatic Discharge - Human Body Model (ESDH)

Test Request	Device	Sbgrp	Sublot	Voltage	SS	#Failures	#ETRejects
RSC199902251	LM358N	A	1	150	5	0	0
RSC199902251	LM358N	A	2	200	5	0	0
RSC199902251	LM358N	A	3	250	5	0	0
RSC199902251	LM358N	A	4	300	5	0	0
RSC199902251	LM358N	A	5	400	5	0	0
RSC199902251	LM358N	A	6	500	5	2	2
RSC199902251	LM358N	B	1	150	5	0	0
RSC199902251	LM358N	B	2	200	5	0	0
RSC199902251	LM358N	B	3	250	5	0	0
RSC199902251	LM358N	B	4	300	5	2	2
RSC199902251	LM358N	B	5	400	5	5	5
RSC199902251	LM358N	B	6	500	5	5	5

Test: Electrostatic Discharge - Machine Model (ESDM)

Test Request	Device	Sbgrp	Sublot	Voltage	SS	#Failures	#ETRejects
RSC199902251	LM358N	A	1	50	5	0	0
RSC199902251	LM358N	A	2	100	5	0	0
RSC199902251	LM358N	A	3	150	5	0	0
RSC199902251	LM358N	A	4	200	5	0	0
RSC199902251	LM358N	A	5	250	5	0	2
RSC199902251	LM358N	B	1	50	5	0	0
RSC199902251	LM358N	B	2	100	5	0	0
RSC199902251	LM358N	B	3	150	5	0	0
RSC199902251	LM358N	B	4	200	5	0	0
RSC199902251	LM358N	B	5	250	5	0	1

Conclusion

The LM358IBP micro SMD qualification has successfully satisfied all reliability requirements as per qualification plan Q19990216 with the exception of Human Body Model (HBM) ESD testing. The LM358IBP device is being released to production with a waiver for HBM ESD performance with no requirement for corrective action.

The LM358IBP device, fabbed on the NSUK BIP Linear process and packaged in the 8-bump micro SMD package, is now fully qualified and approved for production release.

2.1 LMC6035IBP INTRODUCTION

2.1.1 General Product Description

This qualification booklet covers a general purpose dual op amp assembled in the micro SMD package, a wafer-level chip-scale package. It is available in 3000 piece or 250 piece tape and reel carriers.

LMC6035IBPX (3000 piece tape and reel)
LMC6035IBP (250 piece tape and reel)

It features low voltage single supply operation with guaranteed performance at 2.7V, 3V, and 15V. Using a package with lateral dimensions the same size as the die, it is ideal in applications that can take advantage of a surface mount package smaller than SOT23 or SC70.

The LMC6035 has previously been offered only in larger size packages (8-Pin Small Outline – LMC6035IMX/LMC6035IM, and 8-Pin Mini Small Outline – LMC6035IMMX/LMC6035IMM).

2.1.2 Technical Product Description

As with previous versions of LMC6035, the LMC6035IBPX and LMC6035IBP is manufactured using National's double silicon poly gate CMOS process with 4-micron minimum channel length and single-layer metal. Internal name for this process is P2CMOS, which uses 6-inch wafers.

National's name for the wafer-level chip-scale package used for LMC6035 is micro SMD (Surface Mount Device). Since assembly of the die is done at wafer level, there are additional wafer processing steps that are used instead of the usual assembly of a molded plastic surface mount package. These additional steps are covered under Packaging Information section of this qualification booklet.

The micro SMD version of LMC6035 is assembled with 8 eutectic solder bumps (functioning as pins) on active side of die. Non-active side of die is coated with epoxy and laser marked with a pin1 orientation symbol, part number identification code, and a die lot/date code. Customer mounts part on application printed circuit board bump side down using same methods as other small surface mount packages.

2.1.3 Reliability/Qualification Overview

Reliability testing was done for 3 different qualification aspects – device level, mechanical joint integrity, and board level.

Device level testing was done on LMC6035 and included Operational Life, High Temperature Bias Test, and Temperature Cycle.

Mechanical joint integrity of 2 interfaces – bump to die and bump to printed circuit board, was done using a daisy chain test die.

Board level reliability also used the daisy chain test die mounted on boards and involved drop, bend, and vibration tests.

2.1.4 Technical Assistance

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Email: support@nsc.com

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Email: europe.support@nsc.com
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Japan
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Fax: 81-3-5639-7507

Asia Pacific
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Email: sea.support@nsc.com
Tel: 65-2544466
(IDD telephone charge to be paid by caller)

See us on the Worldwide Web @ http://www.national.com

2.2 DEVICE INFORMATION

2.2.1 Datasheet

National Semiconductor

January 2000

LMC6035/LMC6036
Low Power 2.7V Single Supply CMOS Operational Amplifiers

General Description

The LMC6035/6 is an economical, low voltage op amp capable of rail-to-rail output swing into loads of 600Ω. LMC6035 is available in a chip sized package (8-Bump micro SMD) using National's micro SMD package technology. Both allow for single supply operation and are guaranteed for 2.7V, 3V, 5V and 15V supply voltage. The 2.7 supply voltage corresponds to the End-of-Life voltage (0.9V/cell) for three NiCd or NiMH batteries in series, making the LMC6035/6 well suited for portable and rechargeable systems. It also features a well behaved decrease in its specifications at supply voltages below its guaranteed 2.7V operation. This provides a "comfort zone" for adequate operation at voltages significantly below 2.7V. Its ultra low input currents (I_{IN}) makes it well suited for low power active filter application, because it allows the use of higher resistor values and lower capacitor values. In addition, the drive capability of the LMC6035/6 gives these op amps a broad range of applications for low voltage systems.

Features

(Typical Unless Otherwise Noted)

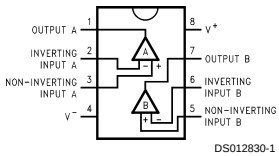
- LMC6035 in micro SMD Package
- Guaranteed 2.7V, 3V, 5V and 15V Performance
- Specified for 2 kΩ and 600Ω Loads
- Wide Operating Range: 2.0V to 15.5V
- Ultra Low Input Current: 20 fA
- Rail-to-Rail Output Swing
  @ 600Ω: 200 mV from either rail at 2.7V
  @ 100 kΩ: 5 mV from either rail at 2.7V
- High Voltage Gain: 126dB
- Wide Input Common-Mode Voltage Range
  -0.1V to 2.3V at Vs = 2.7V
- Low Distortion: 0.01% at 10 kHz

Applications

- Filters
- High Impedance Buffer or Preamplifier
- Battery Powered Electronics
- Medical Instrumentation

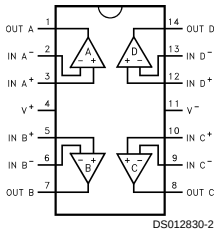
Connection Diagrams

8-Pin SO/MSOP



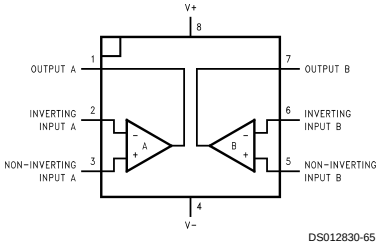
Top View

14-Pin SO/TSSOP



Top View

8-Bump micro SMD



Top View
(Bump Side Down)

Ordering Information

Package	Temperature Range	Transport Media	NSC Drawing
	Industrial −40˚C to +85˚C		
8-pin Small Outline (SO)	LMC6035IM	Rails	M08A
	LMC6035IMX	2.5k Units Tape and Reel	
8-pin Mini Small Outline (MSOP)	LMC6035IMM	1k Units Tape and Reel	MUA08A
	LMC6035IMMX	3.5k Units Tape and Reel	
14-pin Small Outline (SO)	LMC6036IM	Rails	M14A
	LMC6036IMX	2.5k Units Tape and Reel	
14-pin Thin Shrink Small Outline (TSSOP)	LMC6036IMT	Rails	MTC14
	LMC6036IMTX	2.5k Units Tape and Reel	
8-Bump micro SMD	LMC6035IBP	250 Units Tape and Reel	BPA08FFB
	LMC6035IBPX	3k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	3000V
Machine Model	300V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 8)
Output Short Circuit to V^-	(Note 3)
Lead Temperature (soldering, 10 sec.)	260˚C
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 4)	150˚C

Operating Ratings (Note 1)

Supply Voltage	2.0V to 15.5V
Temperature Range	
LMC6035I and LMC6036I	$-40^\circ C \le T_J \le +85^\circ C$
Thermal Resistance (θ_{JA})	
MSOP, 8-pin Mini Surface Mount	230˚C/W
M Package, 8-pin Surface Mount	175˚C/W
M Package, 14-pin Surface Mount	127˚C/W
MTC Package, 14-pin TSSOP	137˚C/W
BP, 8-Bump micro SMD Package	220˚C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = 1.0V$, $V_O = 1.35V$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6035I LMC6036I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.5	5	mV
				6	max
TCV_{OS}	Input Offset Voltage Average Drift		2.3		µV/˚C
I_{IN}	Input Current	(Note 11)	0.02		pA
				90	max
I_{OS}	Input Offset Current	(Note 11)	0.01		pA
				45	max
R_{IN}	Input Resistance		> 10		Tera Ω
CMRR	Common Mode Rejection Ratio	$0.7V \le V_{CM} \le 12.7V$, $V^+ = 15V$	96	63	dB
				60	min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V_O = 2.5V$	93	63	dB
				60	min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$, $V_O = 2.5V$, $V^+ = 5V$	97	74	dB
				70	min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 2.7V$, For CMRR ≥ 40 dB	−0.1	0.3	V
				0.5	max
			2.3	2.0	V
				1.7	min
		$V^+ = 3V$, For CMRR ≥ 40 dB	−0.3	0.1	V
				0.3	max
			2.6	2.3	V
				2.0	min
		$V^+ = 5V$, For CMRR ≥ 50 dB	−0.5	−0.2	V
				0.0	max
			4.5	4.2	V
				3.9	min
		$V^+ = 15V$, For CMRR ≥ 50 dB	−0.5	−0.2	V
				0.0	max
			14.4	14.0	V
				13.7	min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6035I LMC6036I Limit (Note 6)	Units
A_V	Large Signal Voltage Gain (Note 7)	R_L = 600Ω	Sourcing	1000	100	V/mV
					75	min
			Sinking	250	25	V/mV
					20	min
		R_L =2 kΩ	Sourcing	2000		V/mV
			Sinking	500		V/mV
V_O	Output Swing	V^+ = 2.7V R_L = 600Ω to 1.35V		2.5	2.0	V
					1.8	min
				0.2	0.5	V
					0.7	max
		V^+ = 2.7V R_L = 2 kΩ to 1.35V		2.62	2.4	V
					2.2	min
				0.07	0.2	V
					0.4	max
		V^+ = 15V R_L = 600Ω to 7.5V		14.5	13.5	V
					13.0	min
				0.36	1.25	V
					1.50	max
		V^+ = 15V R_L = 2 kΩ to 7.5V		14.8	14.2	V
					13.5	min
				0.12	0.4	V
					0.5	max
I_O	Output Current	V_O = 0V	Sourcing	8	4	mA
					3	min
		V_O = 2.7V	Sinking	5	3	mA
					2	min
I_S	Supply Current	LMC6035 for Both Amplifiers V_O = 1.35V		0.65	1.6	mA
					1.9	max
		LMC6036 for All Four Amplifiers V_O = 1.35V		1.3	2.7	mA
					3.0	max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 9)	1.5	V/µs
GBW	Gain Bandwidth Product	V^+ = 15V	1.4	MHz
θ_m	Phase Margin		48	°
G_m	Gain Margin		17	dB
	Amp-to-Amp Isolation	(Note 10)	130	dB
e_n	Input-Referred Voltage Noise	f = 1 kHz V_{CM} = 1V	27	$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise	f = 1 kHz	0.2	$fA/\sqrt{Hz}$
THD	Total Harmonic Distortion	f = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} V^+ = 10V	0.01	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of 30 mA over long term may adversely affect reliabilty.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board with no air flow.

Note 5: Typical Values represent the most likely parametric norm or one sigma value.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 3.5V ≤ V_O ≤ 7.5V.

Note 8: Do not short circuit output to V^+ when V^+ is greater than 13V or reliability will be adversely affected.

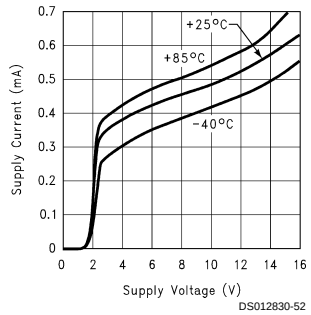
Note 9: V^+ = 15V. Connected as voltage follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 10: Input referred, V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

Note 11: Guaranteed by design.

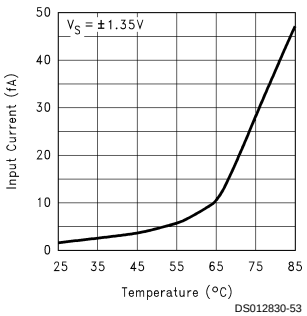
Typical Performance Characteristics Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25˚C

Supply Current vs Supply Voltage (Per Amplifier)



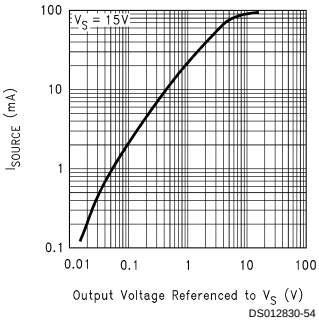
DS012830-52

Input Current vs Temperature



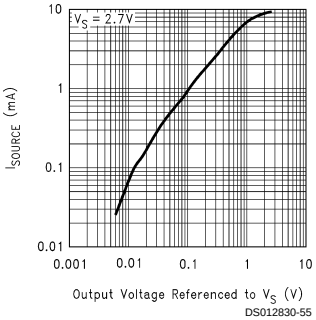
DS012830-53

Sourcing Current vs Output Voltage



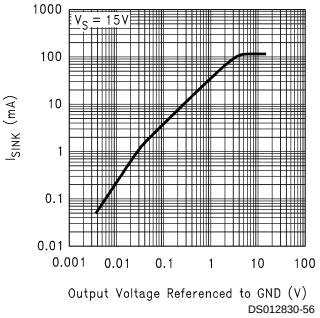
DS012830-54

Sourcing Current vs Output Voltage



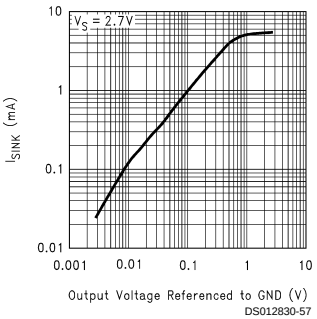
DS012830-55

Sinking Current vs Output Voltage



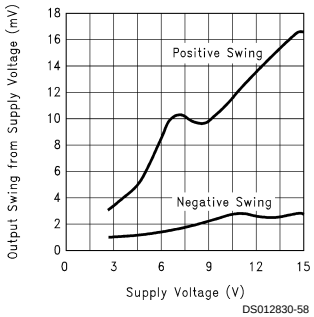
DS012830-56

Sinking Current vs Output Voltage



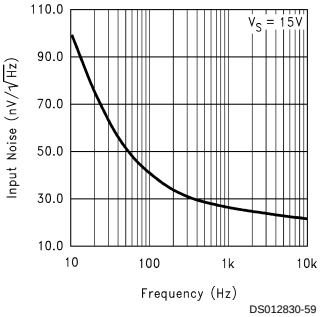
DS012830-57

Output Voltage Swing vs Supply Voltage



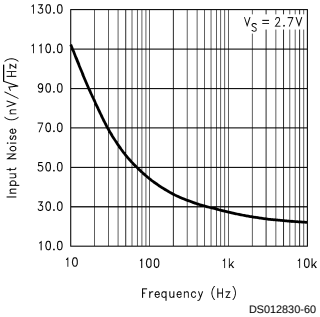
DS012830-58

Input Noise vs Frequency



DS012830-59

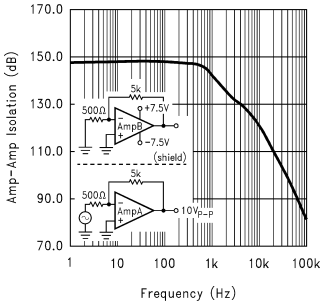
Input Noise vs Frequency



DS012830-60

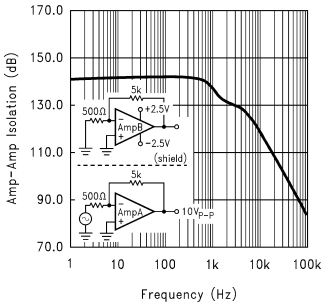
Typical Performance Characteristics Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25˚C (Continued)

Amp to Amp Isolation vs Frequency



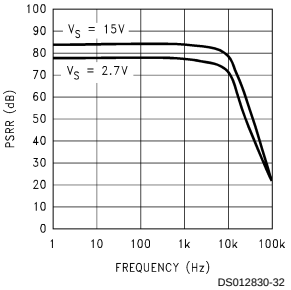
DS012830-61

Amp to Amp Isolation vs Frequency



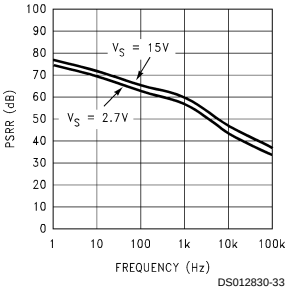
DS012830-62

+PSRR vs Frequency



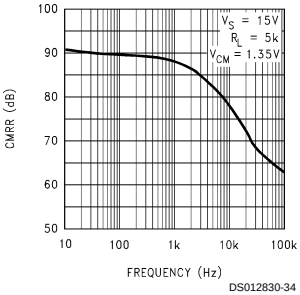
DS012830-32

−PSRR vs Frequency



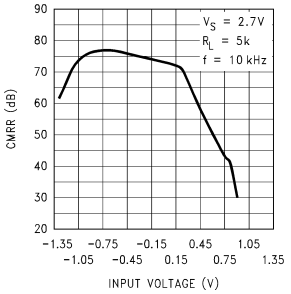
DS012830-33

CMRR vs Frequency



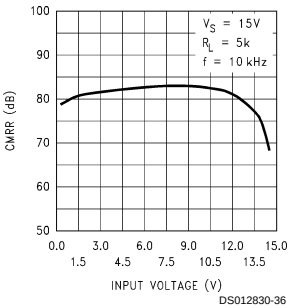
DS012830-34

CMRR vs Input Voltage



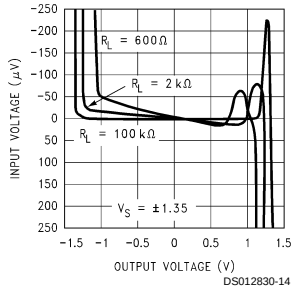
DS012830-35

CMRR vs Input Voltage



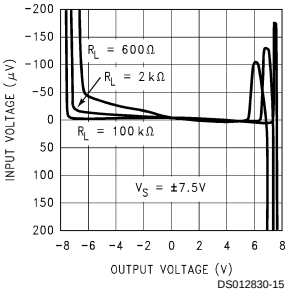
DS012830-36

Input Voltage vs Output Voltage



DS012830-14

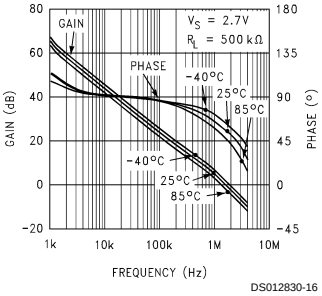
Input Voltage vs Output Voltage



DS012830-15

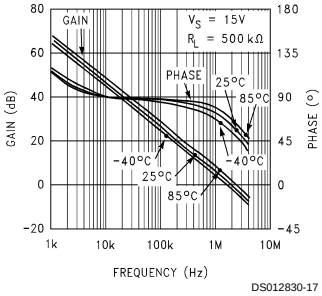
Typical Performance Characteristics Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25˚C (Continued)

Frequency Response vs Temperature



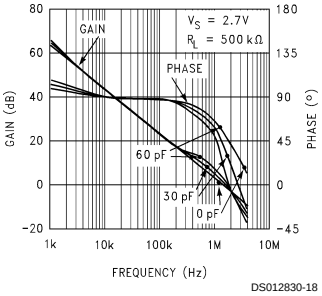
DS012830-16

Frequency Response vs Temperature



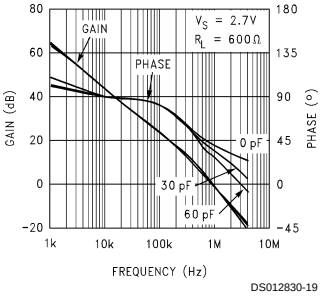
DS012830-17

Gain and Phase vs Capacitive Load



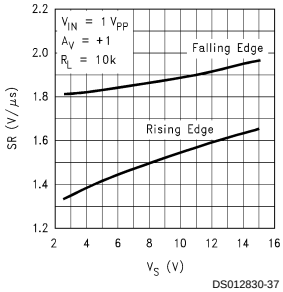
DS012830-18

Gain and Phase vs Capacitive Load



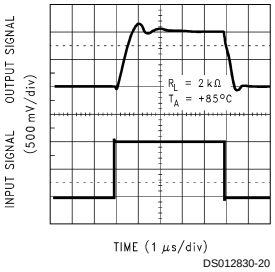
DS012830-19

Slew Rate vs Supply Voltage



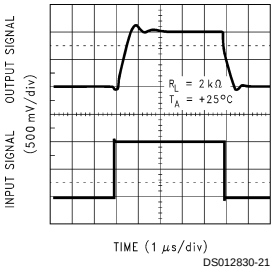
DS012830-37

Non-Inverting Large Signal Response



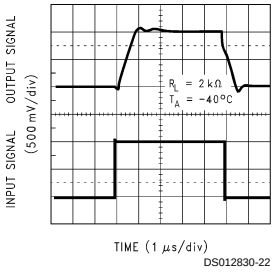
DS012830-20

Non-Inverting Large Signal Response



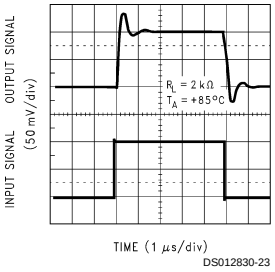
DS012830-21

Non-Inverting Large Signal Response



DS012830-22

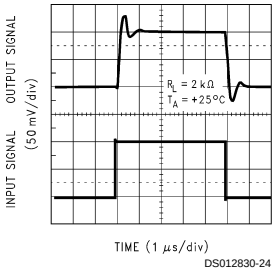
Non-Inverting Small Signal Response



DS012830-23

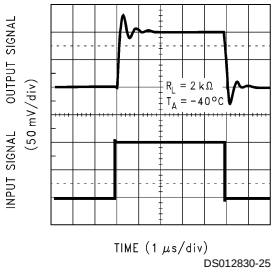
Typical Performance Characteristics Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25˚C (Continued)

Non-Inverting Small Signal Response



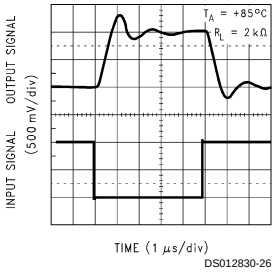
DS012830-24

Non-Inverting Large Signal Response



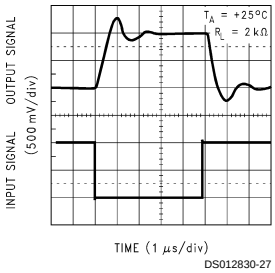
DS012830-25

Inverting Large Signal Response



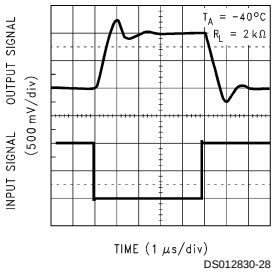
DS012830-26

Inverting Large Signal Response



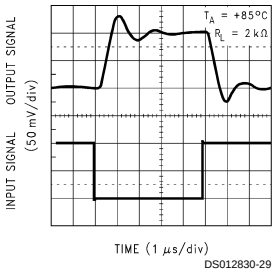
DS012830-27

Inverting Large Signal Response



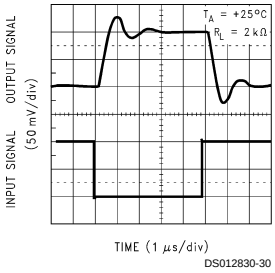
DS012830-28

Inverting Small Signal Response



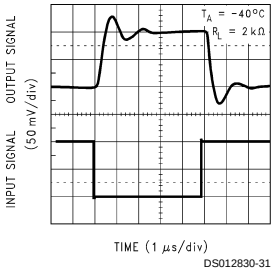
DS012830-29

Inverting Small Signal Response



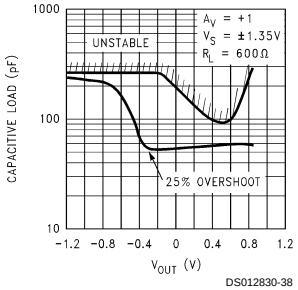
DS012830-30

Inverting Small Signal Response



DS012830-31

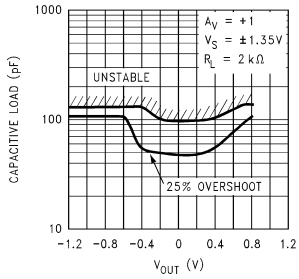
Stability vs Capacitive Load



DS012830-38

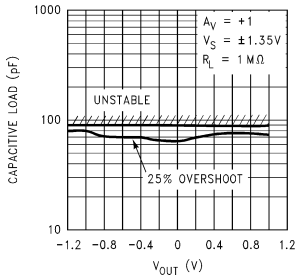
Typical Performance Characteristics Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25˚C (Continued)

Stability vs Capacitive Load



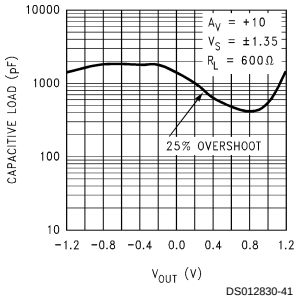
DS012830-39

Stability vs Capacitive Load



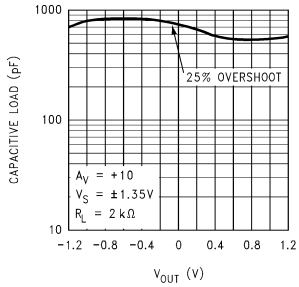
DS012830-40

Stability vs Capacitive Load



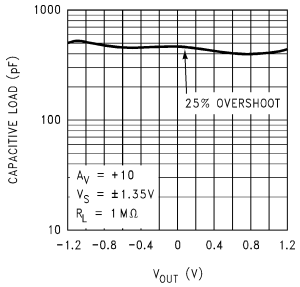
DS012830-41

Stability vs Capacitive Load



DS012830-42

Stability vs Capacitive Load



DS012830-43

1.0 Application Notes

1.1 Background

The LMC6035/6 is exceptionally well suited for low voltage applications. A desirable feature that the LMC6035/6 brings to low voltage applications is its output drive capability — a hallmark for National's CMOS amplifiers. The circuit of *Figure 1* illustrates the drive capability of the LMC6035/6 at 3V of supply. It is a differential output driver for a one-to-one audio transformer, like those used for isolating ground from the telephone lines. The transformer (T1) loads the op amps with about 600Ω of AC load, at 1 kHz. Capacitor C1 functions to block DC from the low winding resistance of T1. Although the value of C1 is relatively high, its load reactance (Xc) is negligible compared to inductive reactance (X_l) of T1.

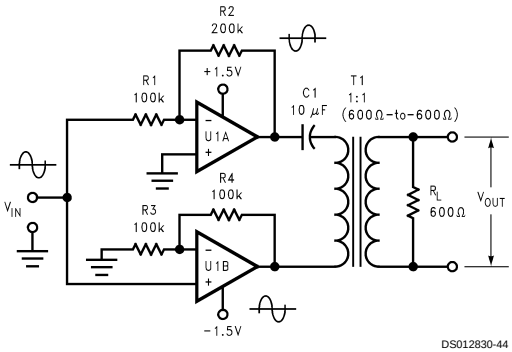


FIGURE 1. Differential Driver

The circuit in *Figure 1* consists of one input signal and two output signals. U1A amplifies the input with an inverting gain of −2, while the U1B amplifies the input with a noninverting gain of +2. Since the two outputs are 180° out of phase with each other, the gain across the differential output is 4. As the differential output swings between the supply rails, one of the op amps sources the current to the load, while the other op amp sinks the current.

How good a CMOS op amp can sink or source a current is an important factor in determining its output swing capability. The output stage of the LMC6035/6 — like many op amps — sources and sinks output current through two complementary transistors in series. This "totem pole" arrangement translates to a channel resistance (R_{dson}) at each supply rail which acts to limit the output swing. Most CMOS op amps are able to swing the outputs very close to the rails — except, however, under the difficult conditions of low supply voltage and heavy load. The LMC6035/6 exhibits exceptional output swing capability under these conditions.

The scope photos of *Figure 2* and *Figure 3* represent measurements taken directly at the output (relative to GND) of U1A, in *Figure 1*. *Figure 2* illustrates the output swing capability of the LMC6035, while *Figure 3* provides a benchmark comparison. (The benchmark op amp is another low voltage (3V) op amp manufactured by one of our reputable competitors.)

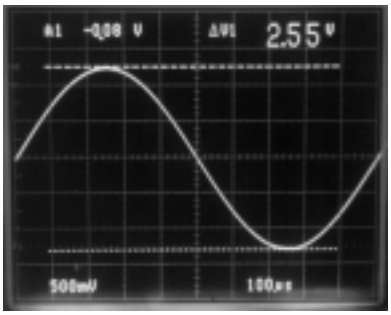


FIGURE 2. Output Swing Performance of the LMC6035 per the Circuit of *Figure 1*

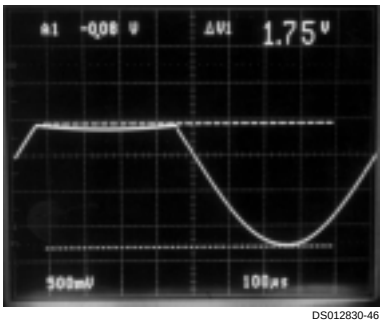


FIGURE 3. Output Swing Performance of Benchmark Op Amp per the Circuit of *Figure 1*

Notice the superior drive capability of LMC6035 when compared with the benchmark measurement — even though the benchmark op amp uses twice the supply current.

Not only does the LMC6035/6 provide excellent output swing capability at low supply voltages, it also maintains high open loop gain (A_{VOL}) with heavy loads. To illustrate this, the LMC6035 and the benchmark op amp were compared for their distortion performance in the circuit of *Figure 1*. The graph of *Figure 4* shows this comparison. The y-axis represents percent Total Harmonic Distortion (THD plus noise) across the loaded secondary of T1. The x-axis represents the input amplitude of a 1 kHz sine wave. (Note that T1 loses about 20% of the voltage to the voltage divider of R_L (600Ω) and T1's winding resistances — a performance deficiency of the transformer.)

1.0 Application Notes (Continued)

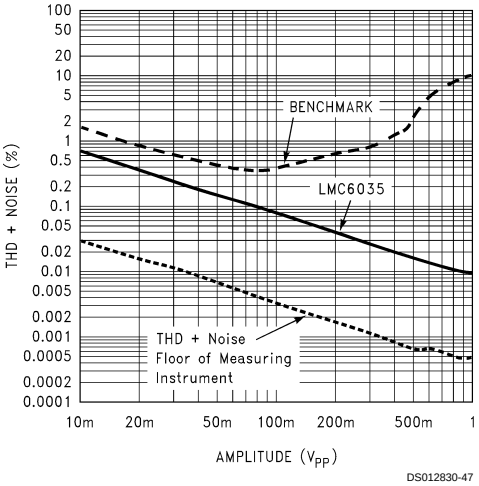


FIGURE 4. THD+Noise Performance of LMC6035 and "Benchmark" per Circuit of *Figure 1*

Figure 4 shows the superior distortion performance of LMC6035/6 over that of the benchmark op amp. The heavy loading of the circuit causes the A_{VOL} of the benchmark part to drop significantly which causes increased distortion.

1.2 APPLICATION CIRCUITS

1.2.1 Low-Pass Active Filter

A common application for low voltage systems would be active filters, in cordless and cellular phones for example. The ultra low input currents (I_{IN}) of the LMC6035/6 makes it well suited for low power active filter applications, because it allows the use of higher resistor values and lower capacitor values. This reduces power consumption and space.

Figure 5 shows a low pass, active filter with a Butterworth (maximally flat) frequency response. Its topology is a Sallen and Key filter with unity gain. Note the normalized component values in parenthesis which are obtainable from standard filter design handbooks. These values provide a 1 Hz cutoff frequency, but they can be easily scaled for a desired cutoff frequency (f_c). The bold component values of *Figure 5* provide a cutoff frequency of 3 kHz. An example of the scaling procedure follows *Figure 5*.

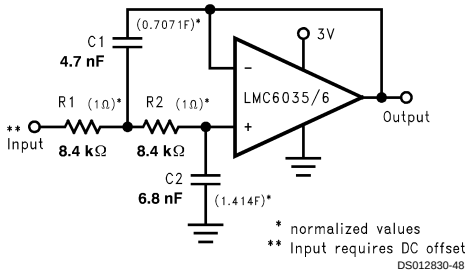


FIGURE 5. 2-Pole, 3 kHz, Active, Sallen and Key, Lowpass Filter with Butterworth Response

1.2.1.1 Low-Pass Frequency Scaling Procedure

The actual component values represented in bold of *Figure 5* were obtained with the following scaling procedure:

1. First determine the frequency scaling factor (FSF) for the desired cutoff frequency. Choosing f_c at 3 kHz, provides the following FSF computation:
   FSF = 2π x 3 kHz $_{(\text{desired cutoff freq.})}$ = 18.84 x 10^3
2. Then divide all of the normalized capacitor values by the FSF as follows:
   C1' = $C_{(\text{Normalized})}$/FSF
   C1' = 0.707/18.84 x 10^3 = 37.93 x 10^{-6}
   C2' = 1.414/18.84 x 10^3 = 75.05 x 10^{-6}
   (C1' and C2': prior to impedance scaling)
3. Last, choose an impedance scaling factor (Z). This Z factor can be calculated from a standard value for C2. Then Z can be used to determine the remaining component values as follows:

Z = C2'/$C2_{(\text{chosen})}$ = 75.05 x 10^{-6}/**6.8 nF** = 8.4k

C1 = C1'/Z = 37.93 x 10^{-6} /8.4k = 4.52 nF

(Standard capacitor value chosen for C1 is **4.7 nF**)

R1 = $R1_{(\text{normalized})}$ x Z = 1Ω x 8.4k = 8.4 kΩ

R2 = $R2_{(\text{normalized})}$ x Z = 1Ω x 8.4k = 8.4 kΩ

(Standard value chosen for R1 and R2 is **8.45 kΩ**)

1.2.2 High Pass Active Filter

The previous low-pass filter circuit of *Figure 5* converts to a high-pass active filter per *Figure 6*.

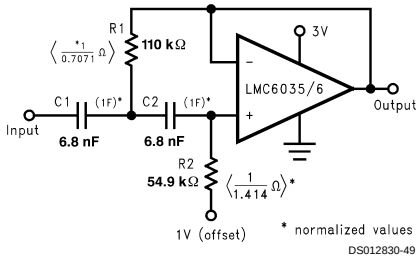


FIGURE 6. 2 Pole, 300 Hz, Sallen and Key, High-Pass Filter

1.2.2.1 High-Pass Frequency Scaling Procedure

Choose a standard capacitor value and scale the impedances in the circuit according to the desired cutoff frequency (300 Hz) as follows:

C = C1 = C2

Z = 1 Farad/$C_{(\text{chosen})}$ x 2π x (desired cutoff freq.)
= 1 Farad/**6.8 nF** x 2π x 300 Hz = 78.05k

R1 = Z x $R1_{(\text{normalized})}$ = 78.05k x (1/0.707) = 110.4 kΩ

(Standard value chosen for R1 is **110 kΩ**)

R2 = Z x $R2_{(\text{normalized})}$ = 78.05k x (1/1.414) = 55.2 kΩ

(Standard value chosen for R1 is **54.9 kΩ**)

1.2.3 Dual Amplifier Bandpass Filter

The dual amplifier bandpass (DABP) filter features the ability to independently adjust f_c and Q. In most other bandpass topologies, the f_c and Q adjustments interact with each other. The DABP filter also offers both low sensitivity to component values and high Qs. The following application of *Figure 7*, provides a 1 kHz center frequency and a Q of 100.

1.0 Application Notes (Continued)

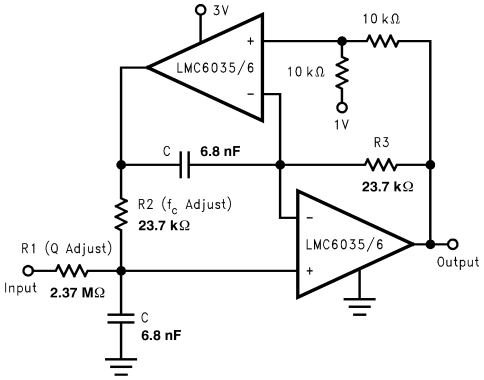


FIGURE 7. 2 Pole, 1 kHz Active, Bandpass Filter

1.2.3.1 DABP Component Selection Procedure

Component selection for the DABP filter is performed as follows:

1. First choose a center frequency (f_c). *Figure 7* represents component values that were obtained from the following computation for a center frequency of 1 kHz.
   $R2 = R3 = 1/(2\pi f_c C)$
   Given: f_c = 1 kHz and $C_{(chosen)}$ = **6.8 nF**
   $R2 = R3 = 1/(2\pi \times 3\ kHz \times 6.8\ nF) = 23.4\ k\Omega$
   (Chosen standard value is **23.7 kΩ**)
2. Then compute R1 for a desired Q (f_c/BW) as follows:
   R1 = Q x R2.
   Choosing a Q of 100,
   R1 = 100 x 23.7 kΩ = **2.37 MΩ.**

1.3 PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with < 1000 pA of leakage current requires special layout of the PC board. If one wishes to take advantage of the ultra-low bias current of the LMC6035/6, typically < 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may at times appear acceptably low. Under conditions of high humidity, dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6035 or LMC6036 inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See *Figure 8*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the amplifiers actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figure 9a, b, c* for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 9 d*.

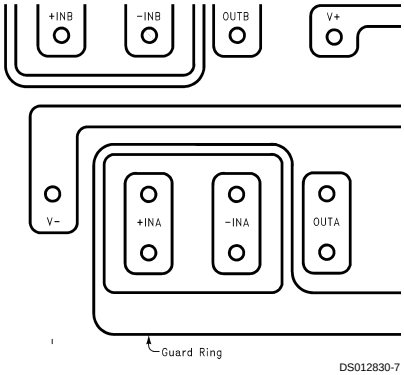
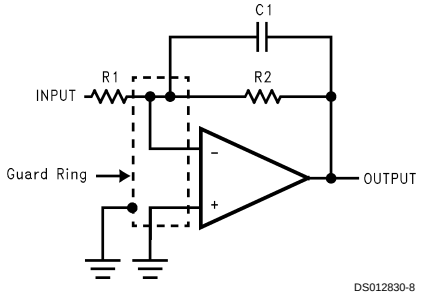
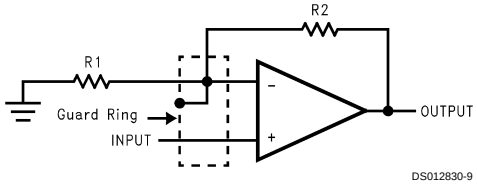


FIGURE 8. Example, using the LMC6036 of Guard Ring in P.C. Board Layout

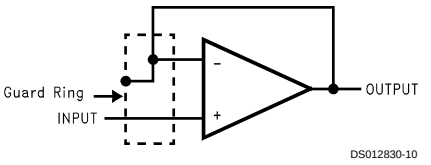
1.0 Application Notes (Continued)



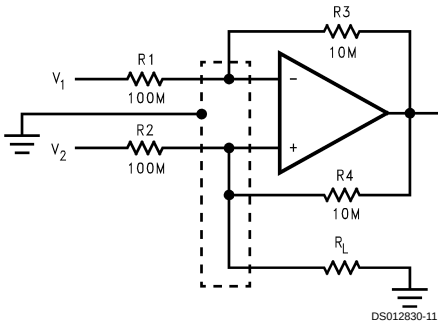
(a) Inverting Amplifier



(b) Non-Inverting Amplifier



(c) Follower



(d) Howland Current Pump

FIGURE 9. Guard Ring Connections

1.3.1 CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6035/6 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 10*, the addition of a small resistor (50Ω–100Ω) in series with the op amp's output, and a capacitor (5 pF–10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

1.4 Micro SMD Considerations

Contrary to what might be guessed, the micro SMD package does not follow the trend of smaller packages having higher thermal resistance. LMC6035 in micro SMD has thermal resistance of 220˚C/W compared to 230˚C/W in MSOP. Even when driving a 600Ω load and operating from ±7.5V supplies, the maximum temperature raise will be under 4.5˚C. For application information specific to micro SMD, see Application note AN-1112.

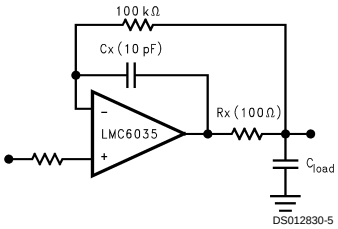


FIGURE 10. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 11*). Typically a pull up resistor conducting 500 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

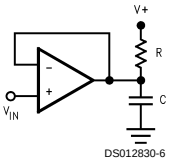
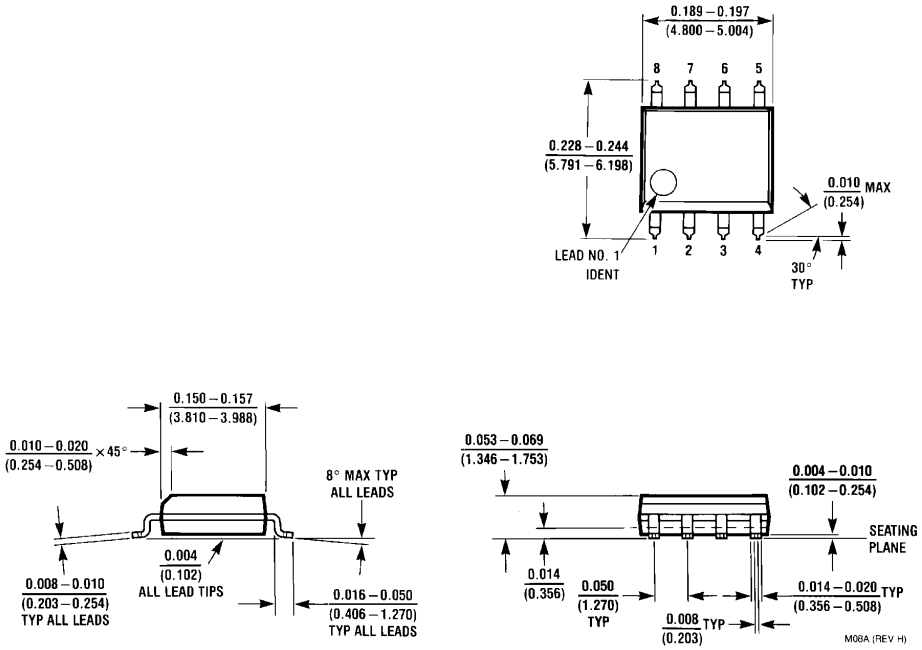


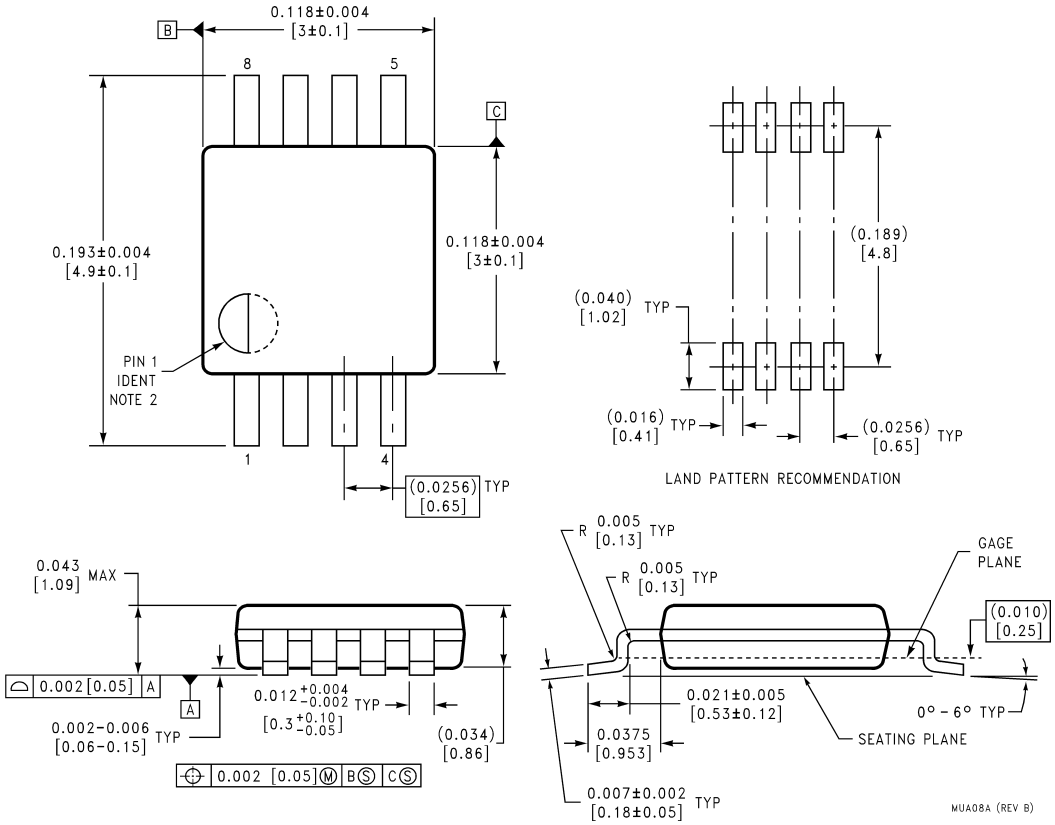
FIGURE 11. Compensating for Large Capacitive Loads with a Pull Up Resistor

Physical Dimensions inches (millimeters) unless otherwise noted



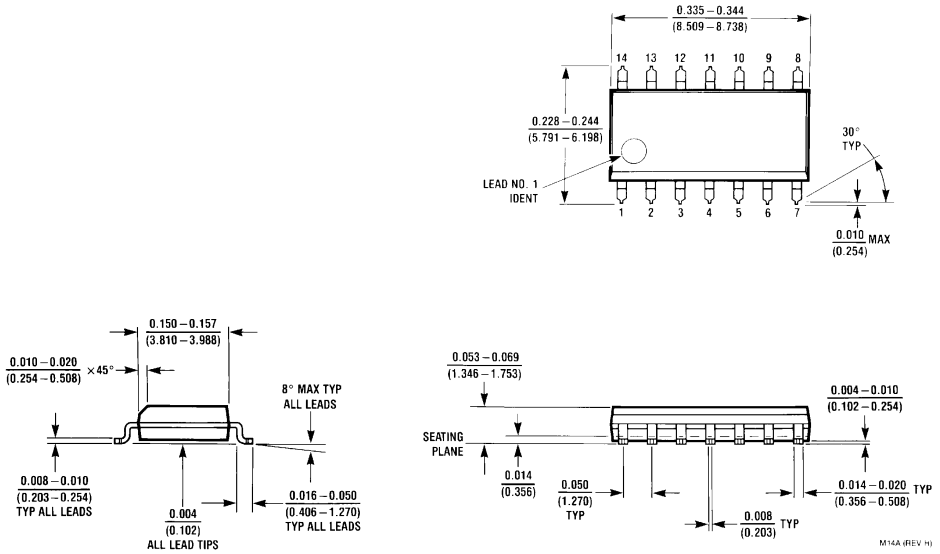
8-Lead (0.150" Wide) Molded
Small Outline Package, JEDEC
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



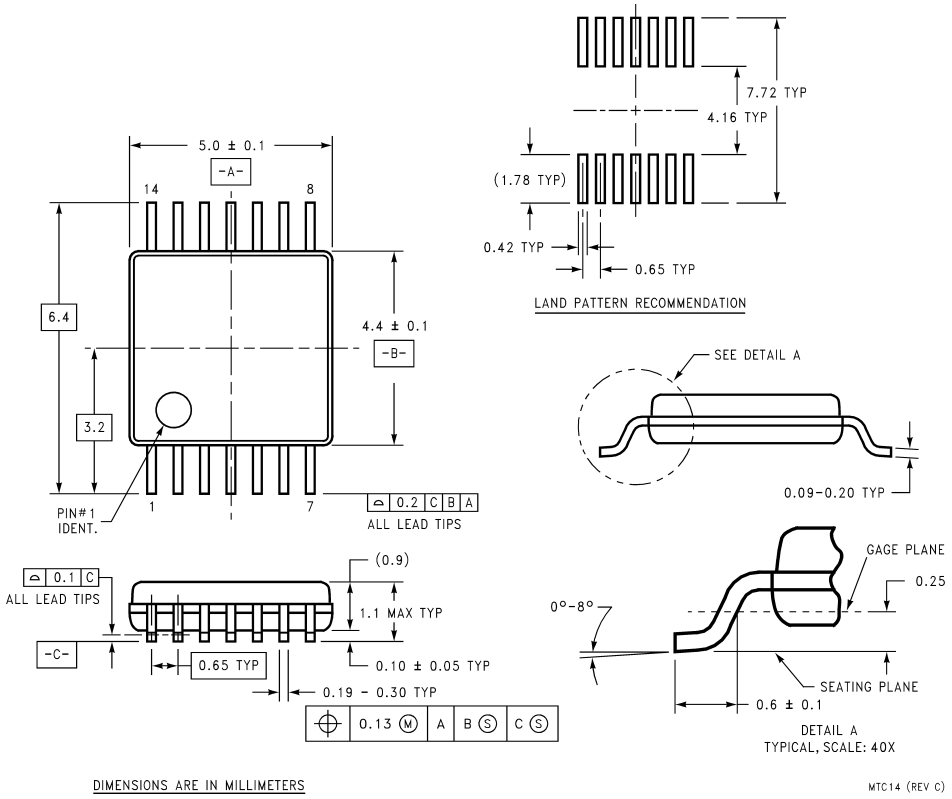
8-Lead (0.150" Wide) Molded
Mini Small Outline Package, JEDEC
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



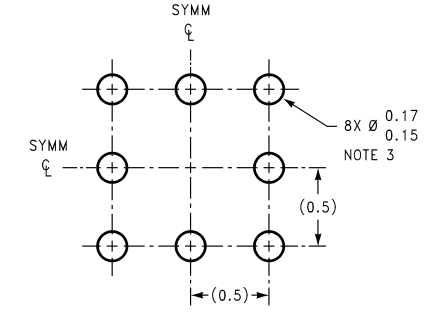
14-Lead (0.150" Wide) Molded
Small Outline Package, JEDEC
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

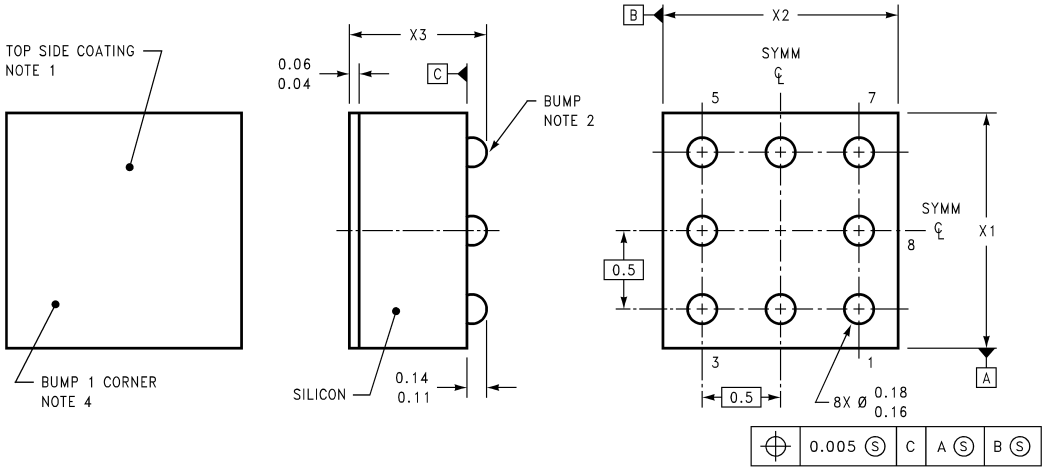


14-Pin TSSOP
NS Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS BPA08XXX (REV A)

NOTE: UNLESS OTHERWISE SPECIFIED.

1. EPOXY COATING.
2. 63Sn/37Pb EUTECTIC BUMP.
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION PINS ARE NUMBERED COUNTERCLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

8-Bump micro SMD
NS Package Number BPA08FFB
X_1 = 1.412 X_2 = 1.412 X_3 = 0.850

Notes

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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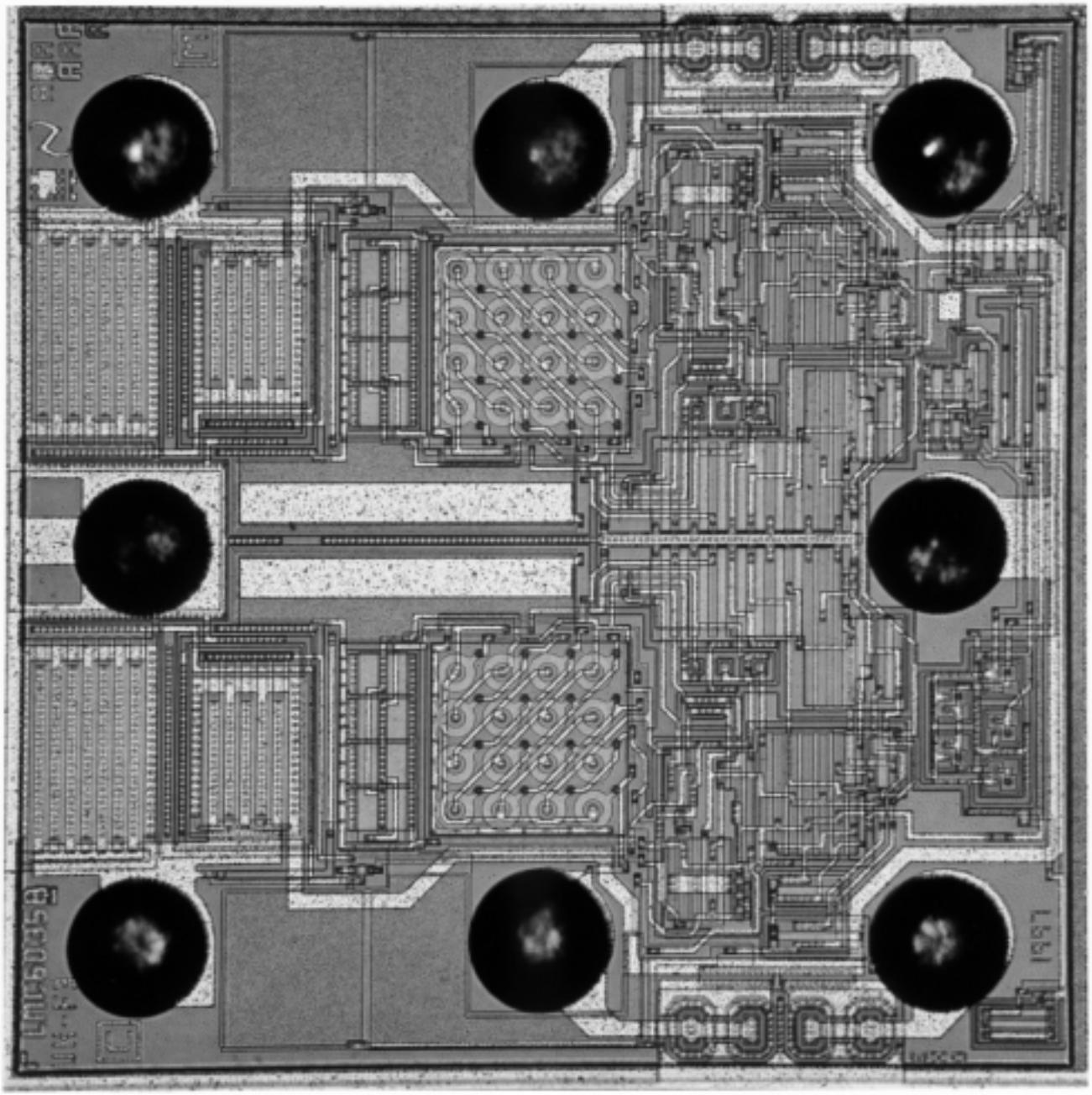
Fax: 81-3-5639-7507

2.2.2 Die Photo



2.3 PROCESS INFORMATION

2.3.1 Process Outline

Fabrication Site: Greenock, Scotland
Process Technology: P2CMOS (double silicon poly gate CMOS)
Minimum Feature Size: 4microns
Wafer Diameter: 6inches
Number of Masks: 17 (including bump assembly)
Metallization: Single Layer Aluminum
Active Side Passivation: Nitride (11,000Å thick) over VOM (5000Å thick) with 2nd Passivation covering the Nitride/VOM
Metallization: Single Layer Aluminum (12,000Å thick)

2.3.2 Process Detail & Masks

1: Initial Oxide
2: **Mask 1.0**, P-
3: P- Implant
4: **Mask 1.4**, N-
5: N- Implant
6: P- Drive
7: Field Oxide
8: **Mask 2.0**, Composite
9: Etch
10: **Mask 3.0**, N- Field Implant
11: N- Field Implant
12: **Mask 4.0**, P- Field Implant
13: P- Field Implant
14: Field Oxide
15: Etch
16: Gate Oxide
17: **Mask 5.0**, Vtp
18: Vtp Implant
19: **Mask 5.3**, P-Deplete
20: P-Deplete Implant
21: Poly Dep
22: Back Etch
23: Poly Dope
24: **Mask 6.0**, Poly1
25: Etch
26: **Mask 7.0**, P+S/D Implant
27: P+ Implant
28: **Mask 8.1**, N+S/D Implant
29: N+ Implant1
30: **Mask 8.2**, N+S/D Implant
31: N+ Implant2
32: Rapid Thermal Anneal
33: Poly Reox
34: Poly Dep
35: Back Etch
36: Poly Dope
37: **Mask 9.0**, Poly2
38: Etch
39: Field Vapox
40: **Mask 10.2**, Contact
41: Etch
42: Ox Reflow
43: Metal Dep
44: **Mask 11.0**, Metal
45: Etch
46: Alloy
47: VOM
48: Nitride
49: **Mask 12.0**, Passivation
50: Etch
51: Final Alloy
52: Ship To Bump Assembly Processing

2.3.3 Assembly Flow

1: Receive Into Bump Assembly Processing [wafer level]
2: 2nd Passivation [wafer level]
3: Passivation Mask [wafer level]
4: Passivation Etch [wafer level]
5: UBM (under bump metal) Application [wafer level]
6: UBM Etch [wafer level]
7: Solder Bump Application [wafer level]
8: Solder Bump Reflow [wafer level]
9: Epoxy Back Side [wafer level]
10: Laser Mark Back Side [wafer level]
11: Electric Test [wafer level]
12: Saw Scribe Singulation [wafer level]
13: Pack in Tape/Reel [individual part level]

2.4 RELIABILITY REPORT

National Semiconductor

Date: August 18, 1998

Reliability Test Report

Purpose

To qualify the new micro SMD micro Surface Mount Device which is an 8 bump wafer level chip scale package - SWA08A - using the LMC6035 die fabricated in UK.

Approvals

Reliability Engineer

Mgr Ref Engineering

Reference File Numbers

RSC199801484	
RSC199801076	RSC199801052
RSC199800814	RSC199801367
RSC199800908	RSC199801366

Distribution List

Abstract

The micro Surface Mount Device (micro SMD) is a version of a wafer level chip scale package where the package size is the same as that of the die. Electrical connection to the outside world is made through solder bump construction on the Aluminum bond pad, where the die is flipped to solder on to the printed circuit board. The die passivation and the 2nd Passivation, along with the solder bumps forms a protective barrier for the active area of the die from outside world contaminants. An Epoxy back coat done to the backside of the die is used for marking.

The LMC6035 is re-laid out so as to provide necessary spacing between the bond pads that enables proper surface mounting of this die. To qualify this new die, 3 die runs assembled in MDIP will be subjected to OPL 150C. Using one die run, 3 lots of the micro SMD devices will be fabricated. All tests except TMCL will be done on these devices mounted on conversion boards. Two TMCL evaluations will be conducted over different temperature ranges since the capability of this package has not yet been established. The devices undergoing TMCL, and THBT will be level 1 preconditioned.

Assembly of micro SMD devices will be done at EM.

Solder joint reliability study will be performed with daisy chain configuration of micro SMD devices. TMCL (0/100C) will be performed on these daisy chained devices (as per IPC specification IPC-SM-785).

Description

Test Request	Device Name	Sbgp	Wafer Die Run	Fab Loc	Fab Line	Pkg Code	# Leads	Assy Loc	Date Cd	Mold C
RSC199800814	LMC6035	A	W#01	UK		SWA08A	8	EM		Epoxy globtop
RSC199800814	LMC6035	B	W#09	UK		SWA08A	8	EM		Epxoy globtop
RSC199800814	LMC6035	C	W#10	UK		SWA08A	8	EM		Epxoy globtop
RSC199800908	LMC6035	A	JM087R26A	UK		SWA08A	8	EM		Epoxy globtop
RSC199800908	LMC6035	B	JM087R26A	UK		SWA08A	8	EM		Epxoy globtop
RSC199800908	LMC6035	C	JM087R26A	UK		SWA08A	8	EM		Epxoy globtop
RSC199801052	LMC6035	A		UK		SWA08A	8	EM		Epoxy globtop
RSC199801052	LMC6035	B		UK		SWA08A	8	EM		Epxoy globtop
RSC199801052	LMC6035	C		UK		SWA08A	8	EM		Epxoy globtop
RSC199801076	LMC6035N	A	JM087R26	UK		N\MDIP	8	EM	9812	B8
RSC199801076	LMC6035N	B	JM087V42	UK		N\MDIP	8	EM	9812	B8
RSC199801076	LMC6035N	C	JM088V53	UK		N\MDIP	8	EM	9812	B8
RSC199801484	LMC6035	A		UK		SWA08A	8	EM		Epoxy globtop
RSC199801484	LMC6035	B		UK		SWA08A	8	EM		Epxoy globtop
RSC199801484	LMC6035	C		UK		SWA08A	8	EM		Epxoy globtop

2.4 RELIABILITY DATA

Tests Performed

1. Preconditioning-IB1
   a. temp cycle - 5 cycles at -40/60C
   b. bake - 16 hours at 125C
   c. moisture sensitivity level 1 - moisture soak for 168 hours at 85C and 85%RH
   d. IR reflow 235C 3 passes
   e. Flux immersion
   f. clean

2. ESD - Five units for each level.
   a. Human Body Model = 1000V, 1500V, 2000V, 2500V, 3000V, 3500V
   b. Machine Model = 50V, 100V, 200V, 300V , 350V, 400V

3. Latch-Up Testing - Six units passed for each level.
   a. 200ma at 25C, micro SMD package, 200ma at 85C MDIP, 200ma at 125C MDIP

4. Test: Operating Life Test (Static) (SOPL) (150C, static bias, ckt 2526RE-B1) - Release at 500 hours.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199800908	LMC6035	A	0	0	150	0
RSC199800908	LMC6035	B	0	0	150	0
RSC199800908	LMC6035	C	0	0	150	0
RSC199801076	LMC6035N	A	0	0	150	0
RSC199801076	LMC6035N	B	0	0	150	0
RSC199801076	LMC6035N	C	0	0	150	0

5. Test: Temperature Cycle (TMCL)) (-65 to +150C, air-air, unbiased) - Release at 500 cycles.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199801484	LMC6035	A	0	0	150	-65
RSC199801484	LMC6035	B	0	0	150	-65
RSC199801484	LMC6035	C	0	0	150	-65

6. Test: Temperature Cycle (TMCL)) (-40 to +125C, air-air, unbiased) - Release at 1440 cycles.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199801052	LMC6035	A	0	0	125	-40
RSC199801052	LMC6035	B	0	0	125	-40
RSC199801052	LMC6035	C	0	0	125	-40

7. Test: Daisy Chain Temperature Cycle (TMCL)) (0 to +100C per IPC specification IPC-SM-785) - Release at 1000 cycles.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
0605 Daisy Chain	A	0	0	100	0	

8. Test: Daisy Chain Temperature Cycle (TMCL)) (-40 to +125C per IPC specification IPC-SM-785) - For information only.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
0605 Daisy Chain	A	0	0	125	-40	

9. Test: Temperature Humidity Bias Test (THBT) (85C, 85% RH, Biased, ckt 2161RE-A) - Release at 500 hours.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199800814	LMC6035	A	85	0	85	0
RSC199800814	LMC6035	B	85	0	85	0
RSC199800814	LMC6035	C	85	0	85	0

Table Showing Results after Reliability Tests for Qualification

LMC6035 micro SMD wafer level chip scale package Qualification					
Tests	**Time/Cycles**	**Sbgrp A**	**Sbgrp B**	**Sbgrp C**	**Status**
SOPL - micro SMD	168	0/77	0/77	0/77	Passed
	500	0/77	0/77	0/77	Passed
SOPL - MDIP	168	0/77	0/77	0/77	Passed
	500	0/77	0/77	0/77	Passed
	1000	0/77	0/77	0/77	Passed
THBT - micro SMD	168	0/77	0/77	0/77	Passed
	500	0/77	0/77	0/77	Passed
	1000	0/77	0/77	0/77	Passed
TMCL - micro SMD	500	0/80	0/80	0/79[1]	Passed
-40C to 125C	1440	0/80	0/80	0/79	Passed
TMCL - micro SMD -65C to 150C	500	0/80	0/80	0/80	Passed
TMCL - Daisy	500	0/62			Passed
Chain	1000	0/62			Passed
0C to 100C	2300	0/62			Passed
TMCL - Daisy Chain -40C to +125C	800	0/61			Information only

Table Showing Results of ESD and Latch-Up Tests for Qualification

LMC6035 micro SMD wafer level chip scale package Qualification					
Tests		**Levels**			**Status**
ESD - HMB	2000V	2500V	3000V	3500V	Passed to
(rejects/tested)	0/5	0/5	0/5	5/5	3000V
ESD - MM	200V	250V	300V	350V	Passed to
(rejects/tested)	0/5	0/5	0/5	2/5	300V
Latch-Up	25C - micro SMD	85C - MDIP	125C - MDIP		Passed to
(rejects/tested)	0/6	0/6	0/6		125C

Notes

TMCL - micro SMD

[1]Unit was lost. Since the TMCL parts were not mounted on conversion boards they are very difficult to handle due to their small size and one unit was lost. No corrective action is necessary.

Conclusion

The wafer level chip scale package SWA08A has passed the SOPL, TMCL, and THBT legs using the LMC6035 die. The package/part also passed ESD and Latch-Up.

Appendix: Board Level Testing

In addition to above device level and mechanical joint integrity reliability, the following board level testing was done.

1. Drop Test, 3 mutually exclusive axes from height of 750 mm onto non-cushioning vinyl tile surface
2. Three-Point Bend Test, test board span of 100 mm with cross-head speed of 9.45 mm/min and 25 mm deflection
3. Sinusoidal Vibration Test, frequency sweep of 260 Hz to 320 Hz for board response of 20 G to 40 G
4. Random Vibration Test, 2 G RMS with frequencies from 20 Hz to 2,000 Hz

3.1 LM431AIBP INTRODUCTION

3.1.1 General Product Description

This qualification booklet covers the LM431 adjustable precision shunt regulator in the micro SMD (Surface Mount Device) package. The LM431 is a 3-terminal adjustable shunt regulator with guaranteed temperature stability over the entire temperature range of operation. It features a programmable output voltage, fast turn-on response, and low output noise in the micro SMD package. Since there is no package, micro SMD is the smallest package possible, making it ideal for applications that can take advantage of a surface mount package that is smaller than SOT-23 and SC-70.

For more information concerning application and use of micro SMD, please refer to Application Note AN-1112 included in this booklet.

The LM431 is also available in SOT23-3, SOIC-8, and TO-92 packages. Please refer to the datasheet included in this booklet or visit National Semiconductor's website (http://www.national.com) for more information on these packages.

3.1.2 Technical Product Description

As with previous versions of the LM431, the LM431AIBP is manufactured using National's dual-layer metal bipolar process.

National's name for the wafer-level chip-scale package used for LM431 is micro SMD. Since assembly of the die is done at wafer level, there are additional wafer processing steps that are used instead of the usual assembly of a molded plastic surface mount package. These additional steps are covered under Packaging Information section of this qualification booklet.

The micro SMD version of the LM431 is assembled with 4 eutectic solder bumps (functioning as pins) on the active side of the die. The non-active side of the die is coated with epoxy and laser marked with a part number identification code and a die lot/date code. The LM431 in micro SMD is shipped in standard 250 and 3,000 unit tape and reel. The devices are mounted on printed circuit boards bump side down using same methods as other small surface mount packages.

3.1.3 Reliability/Qualification Overview

The LM431 underwent a redistribution utilizing dual layer metal process technology to convert the die for assembly in the 4-bump micro SMD package. The new die was subjected to reliability testing where the micro SMD devices were mounted on conversion boards in MDIP layout configuration for pre and post testing. Three lots of the Rev D die passed 500 hours of Static Operating Life Test in the 8 lead MDIP conversion boards for qualification of the new layout. Human Body Model Electrostatic Discharge and Machine Model Electrostatic Discharge testing yielded passing results. Three lots of the LM431 in the micro SMD package were subjected to preconditioned Autoclave Test and Temperature Humidity Bias Test with no valid failures incurred through the respective release time-points for each test. Two lots in the micro SMD package were also subjected to preconditioned Temperature Cycle with zero valid failures.

3.1.4 Technical Assistance

Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

Europe
Fax: +49 (0) 1 80 5 30 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80 5 30 85 85
English Tel: +49 (0) 1 80 5 32 78 32

Japan
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

Asia Pacific
Fax: 65-2504466
Email: sea.support@nsc.com
Tel: 65-2544466
(IDD telephone charge to be paid by caller)

See us on the Worldwide Web @ http://www.national.com

3.2 DEVICE INFORMATION

3.2.1 Datasheet

National Semiconductor

December 1999

LM431
Adjustable Precision Zener Shunt Regulator

General Description

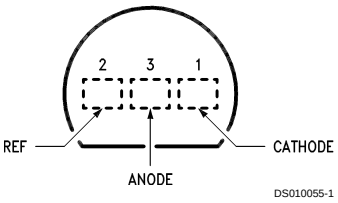
The LM431 is a 3-terminal adjustable shunt regulator with guaranteed temperature stability over the entire temperature range of operation. It is now available in a chip sized package (4-Bump micro SMD) using National's micro SMD package technology. The output voltage may be set at any level greater than 2.5V (V_{REF}) up to 36V merely by selecting two external resistors that act as a voltage divided network. Due to the sharp turn-on characteristics this device is an excellent replacement for many zener diode applications.

Features

- Average temperature coefficient 50 ppm/°C
- Temperature compensated for operation over the full temperature range
- Programmable output voltage
- Fast turn-on response
- Low output noise
- LM431 in micro SMD package

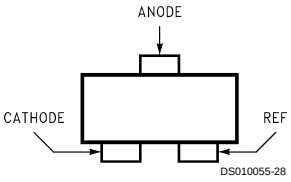
Connection Diagrams

TO-92: Plastic Package



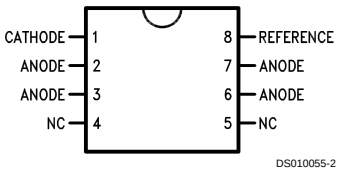
Top View

SOT-23: 3-Lead Small Outline



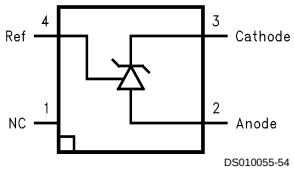
Top View

SO-8: 8-Pin Surface Mount



Top view

4-Bump micro SMD



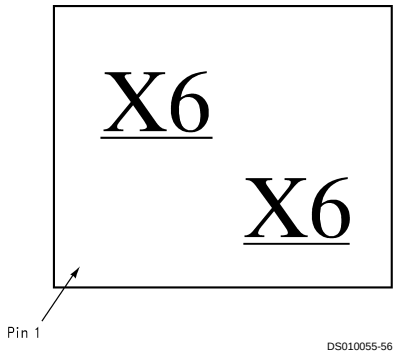
Top View
(bump side down)

Ordering Information

Package	Typical Accuracy Order Number/Package Marking			Temperature Range	Transport Media	NSC Drawing
	0.5%	1%	2%			
TO-92	LM431CCZ/ LM431CCZ	LM431BCZ/ LM431BCZ	LM431ACZ/ LM431ACZ	0˚C to +70˚C	Rails	Z03A
	LM431CIZ/ LM431CIZ	LM431BIZ/ LM431BIZ	LM431AIZ/ LM431AIZ	−40˚C to +85˚C		
SO-8	LM431CCM/ 431CCM	LM431BCM/ 431BCM	LM431ACM/ LM431ACM	0˚C to +70˚C	Rails and Tape &Reel	M08A
	LM431CIM/ 431CIM	LM431BIM/ 431BIM	LM431AIM/ LM431AIM	−40˚C to +85˚C		
SOT-23	LM431CCM3/ N1B	LM431BCM3/ N1D	LM431ACM3/ N1F	0˚C to +70˚C	Rails and Tape &Reel	MA03B
	LM431CIM3 N1A	LM431BIM3 N1C	LM431AIM3 N1E	−40˚C to +85˚C		
micro SMD	–	–	LM431AIBP LM431AIBPX(Note 1)	−40˚C to +85˚C	250 Units Tape and Reel 3k Units Tape and Reel	BPA04AFA

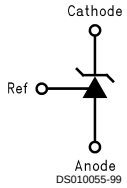
Note 1: The micro SMD package marking is a 2 digit manufacturing Date Code only

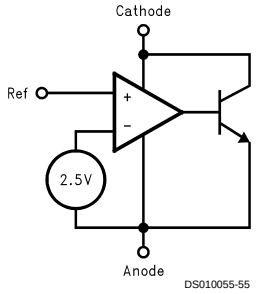
micro SMD Top View Marking Example



The LM431 micro SMD Package will be marked with a two digit date manufacturing code. The underline indicates the bottom of the marking. Pin one will be placed at the bottom left hand corner, and the rest of the pin numbers will follow counter-clockwise.

Symbol and Functional Diagrams





DC Test Circuits

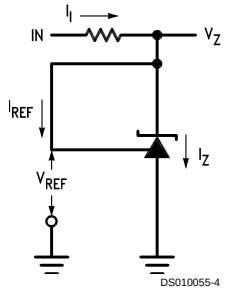
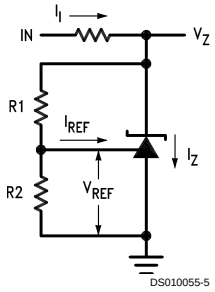


FIGURE 1. Test Circuit for $V_Z = V_{REF}$



Note: $V_Z = V_{REF} (1 + R1/R2) + I_{REF} \cdot R1$

FIGURE 2. Test Circuit for $V_Z > V_{REF}$

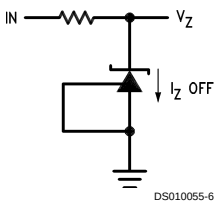


FIGURE 3. Test Circuit for Off-State Current

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65˚C to +150˚C
Operating Temperature Range	
Industrial (LM431xI)	−40˚C to +85˚C
Commercial (LM431xC)	0˚C to +70˚C
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C (lead temp.)
Cathode Voltage	37V
Continuous Cathode Current	−10 mA to +150 mA
Reference Voltage	−0.5V
Reference Input Current	10 mA
Internal Power Dissipation (Notes 3, 4)	
TO-92 Package	0.78W
SO-8 Package	0.81W
SOT-23 Package	0.28W
micro SMD Package	0.30W

Operating Conditions

	Min	Max
Cathode Voltage	V_{REF}	37V
Cathode Current	1.0 mA	100 mA

LM431 Electrical Characteristics

T_A = 25˚C unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{REF}	Reference Voltage	$V_Z = V_{REF}$, I_I = 10 mA LM431A *(Figure 1)*		2.440	2.495	2.550	V
		$V_Z = V_{REF}$, I_I = 10 mA LM431B *(Figure 1)*		2.470	2.495	2.520	V
		$V_Z = V_{REF}$, I_I = 10 mA LM431C *(Figure 1)*		2.485	2.500	2.510	V
V_{DEV}	Deviation of Reference Input Voltage Over Temperature (Note 5)	$V_Z = V_{REF}$, I_I = 10 mA, T_A = Full Range *(Figure 1)*			8.0	17	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I_Z = 10 mA *(Figure 2)*	V_Z from V_{REF} to 10V		−1.4	−2.7	mV/V
			V_Z from 10V to 36V		−1.0	−2.0	
I_{REF}	Reference Input Current	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA *(Figure 2)*			2.0	4.0	µA
$\propto I_{REF}$	Deviation of Reference Input Current over Temperature	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA, T_A = Full Range *(Figure 2)*			0.4	1.2	µA
$I_{Z(MIN)}$	Minimum Cathode Current for Regulation	$V_Z = V_{REF}$ *(Figure 1)*			0.4	1.0	mA
$I_{Z(OFF)}$	Off-State Current	V_Z = 36V, V_{REF} = 0V *(Figure 3)*			0.3	1.0	µA
r_Z	Dynamic Output Impedance (Note 6)	$V_Z = V_{REF}$, LM431A, Frequency = 0 Hz *(Figure 1)*				0.75	Ω
		$V_Z = V_{REF}$, LM431B, LM431C Frequency = 0 Hz *(Figure 1)*				0.50	Ω

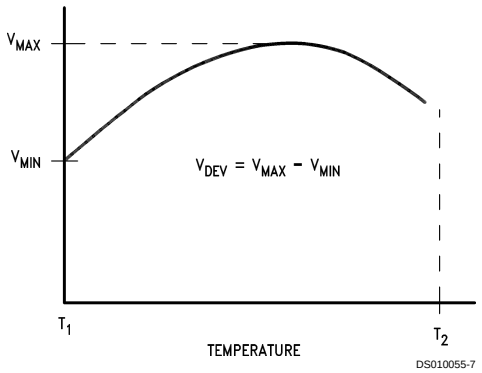
Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 3: $T_{J\ Max}$ = 150˚C.

Note 4: Ratings apply to ambient temperature at 25˚C. Above this temperature, derate the TO-92 at 6.2 mW/˚C, the SO-8 at 6.5 mW/˚C, the SOT-23 at 2.2 mW/˚C and the micro SMD at 3mW/˚C.

Note 5: Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range.

LM431
Electrical Characteristics (Continued)



The average temperature coefficient of the reference input voltage, $\propto V_{REF}$, is defined as:

$$\propto V_{REF} \frac{ppm}{°C} = \frac{\pm\left[\frac{V_{Max} - V_{Min}}{V_{REF\ (at\ 25°C)}}\right]10^6}{T_2 - T_1} = \frac{\pm\left[\frac{V_{DEV}}{V_{REF\ (at\ 25°C)}}\right]10^6}{T_2 - T_1}$$

Where:

$T_2 - T_1$ = full temperature change (0-70˚C).

$\propto V_{REF}$ can be positive or negative depending on whether the slope is positive or negative.

Example: V_{DEV} = 8.0 mV, V_{REF} = 2495 mV, $T_2 - T_1$ = 70˚C, slope is positive.

$$\propto V_{REF} = \frac{\left[\frac{8.0\ mV}{2495\ mV}\right]10^6}{70°C} = +46\ ppm/°C$$

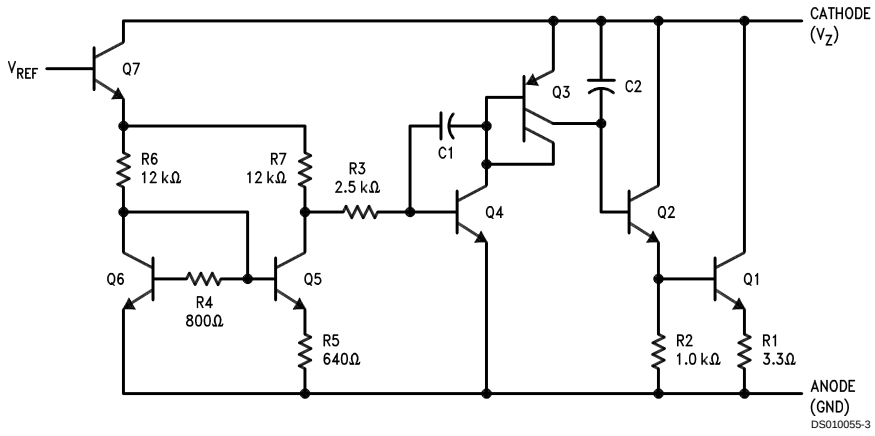
Note 6: The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (see *Figure 2*), the dynamic output impedance of the overall circuit, r_Z, is defined as:

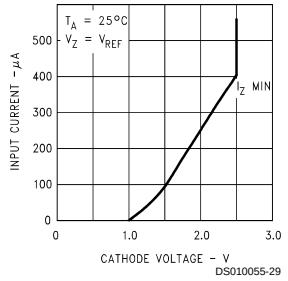
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z\left(1 + \frac{R1}{R2}\right)\right]$$

Equivalent Circuit

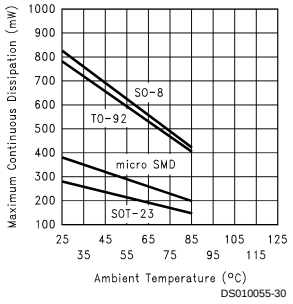


Typical Performance Characteristics

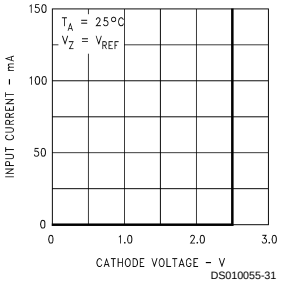
Input Current vs V_Z



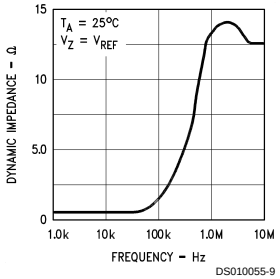
Thermal Information

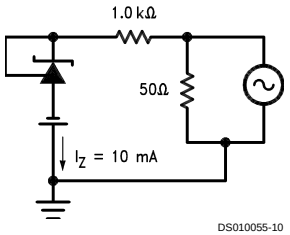


Input Current vs V_Z

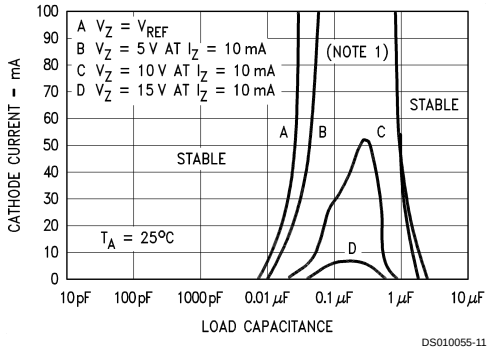


Dynamic Impedance vs Frequency



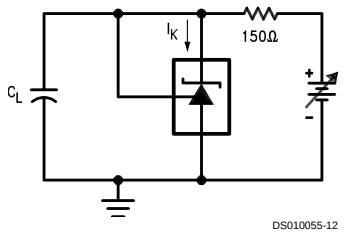


Stability Boundary Conditions

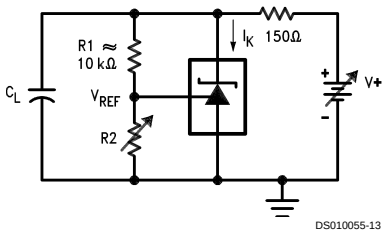


Note: The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V^+ were adjusted to establish the initial V_Z and I_Z conditions with C_L = 0. V^+ and C_L were then adjusted to determine the ranges of stability.

Test Circuit for Curve A Above

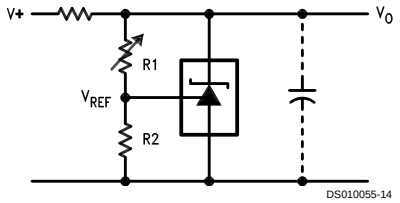


Test Circuit for Curves B, C and D Above



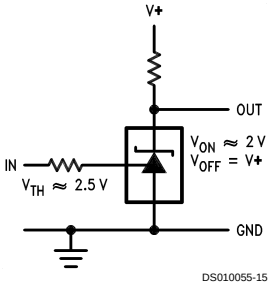
Typical Applications

Shunt Regulator

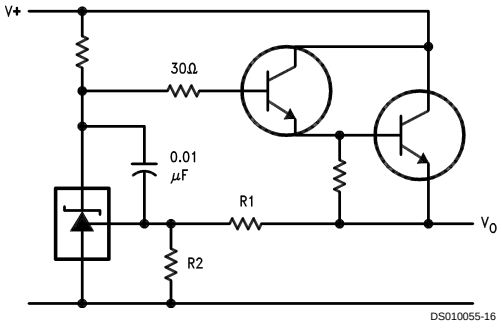


$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{REF}$$

Single Supply Comparator with Temperature Compensated Threshold

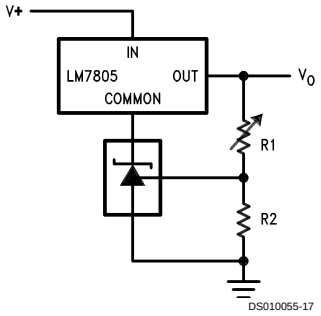


Series Regulator



$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{REF}$$

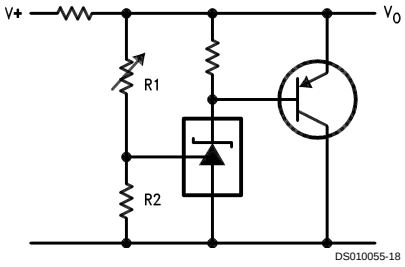
Output Control of a Three Terminal Fixed Regulator



$$V_O = \left(1 + \frac{R1}{R2}\right) V_{REF}$$

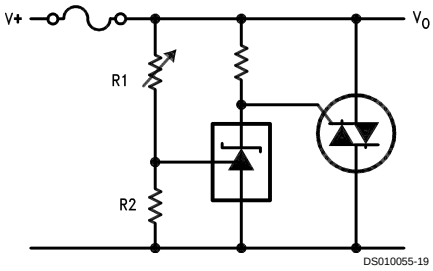
$$V_{O\,MIN} = V_{REF} + 5V$$

Higher Current Shunt Regulator



$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{REF}$$

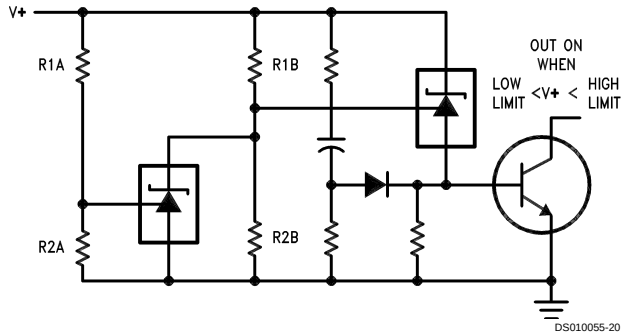
Crow Bar



$$V_{LIMIT} \approx \left(1 + \frac{R1}{R2}\right) V_{REF}$$

Typical Applications (Continued)

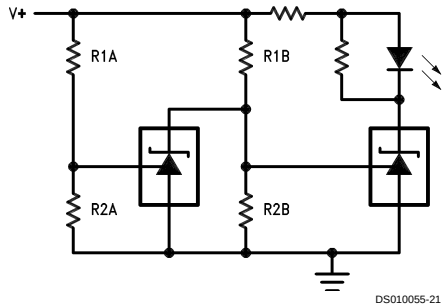
Over Voltage/Under Voltage Protection Circuit



$$\text{LOW LIMIT} \approx V_{REF}\left(1+\frac{R1B}{R2B}\right)+V_{BE}$$

$$\text{HIGH LIMIT} \approx V_{REF}\left(1+\frac{R1A}{R2A}\right)$$

Voltage Monitor



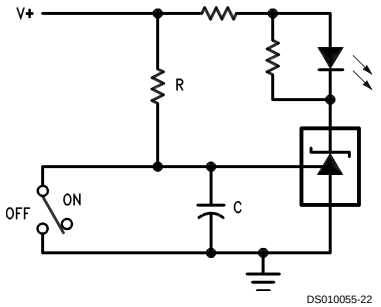
$$\text{LOW LIMIT} \approx V_{REF}\left(1+\frac{R1B}{R2B}\right)$$

$$\text{HIGH LIMIT} \approx V_{REF}\left(1+\frac{R1A}{R2A}\right)$$

LED ON WHEN
LOW LIMIT $< V^{+} <$ HIGH LIMIT

Typical Applications (Continued)

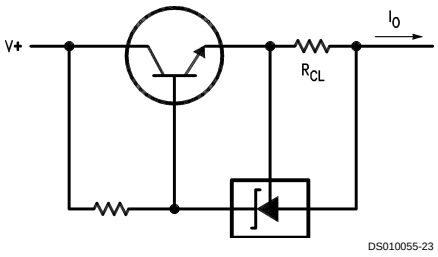
Delay Timer



DS010055-22

$$\text{DELAY} = R \bullet C \bullet \ell n \frac{V+}{(V^+) - V_{REF}}$$

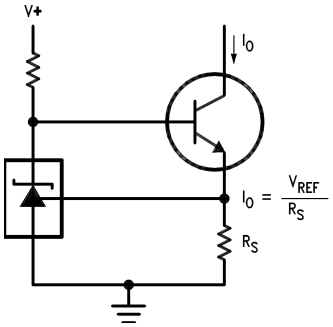
Current Limiter or Current Source



DS010055-23

$$I_O = \frac{V_{REF}}{R_{CL}}$$

Constant Current Sink



DS010055-24

Application Info

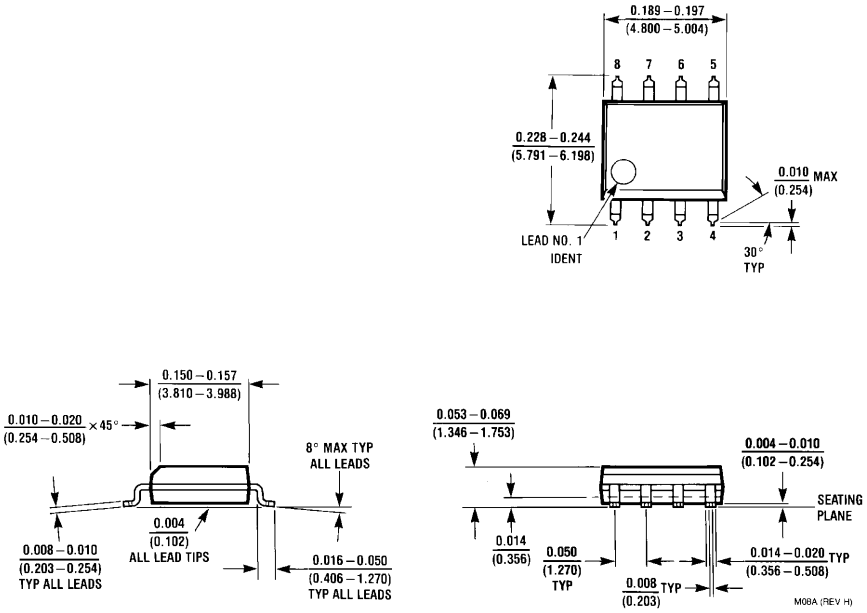
1.0 Mounting

To ensure that the geometry of the micro SMD package maintains good physical contact with the printed circuit board, pin 1 (NC) must be soldered to the pcb. Please see AN-1112 for more detailed information regarding board mounting techniques for the micro SMD package.

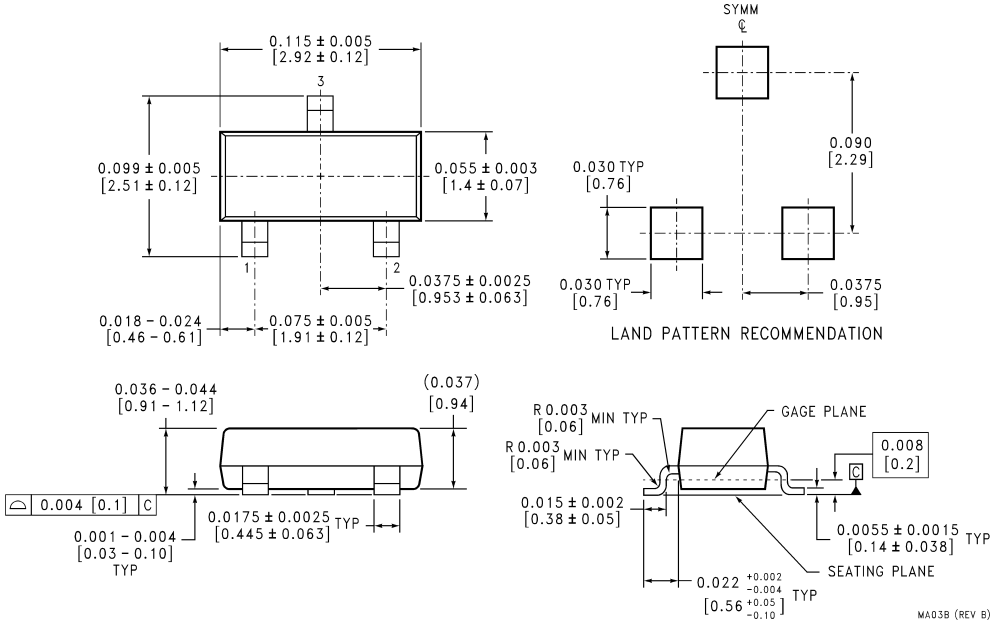
2.0 LM431 micro SMD Light Sensitivity

When the LM431 micro SMD package is exposed to bright sunlight, normal office fluorescent light, and other LED's and lasers, it operates within the guaranteed limits specified in the electrical characteristics table.

Physical Dimensions inches (millimeters) unless otherwise noted

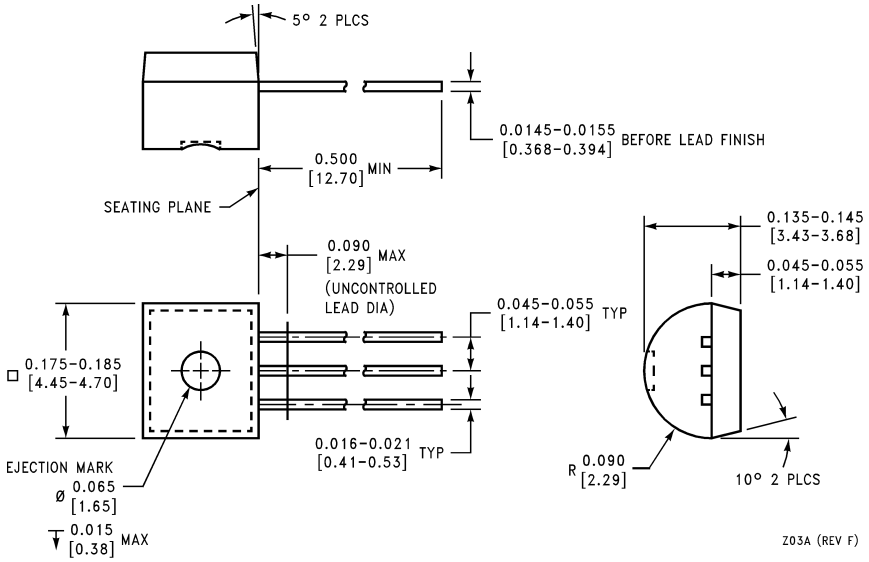


NS Package Number M08A



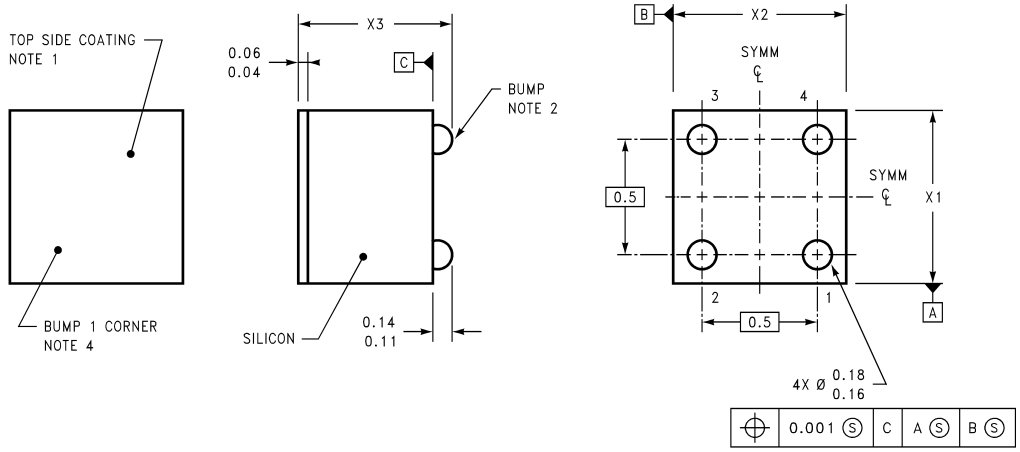
SOT-23 Molded Small Outline Transistor Package (M3)
NS Package Number MA03B

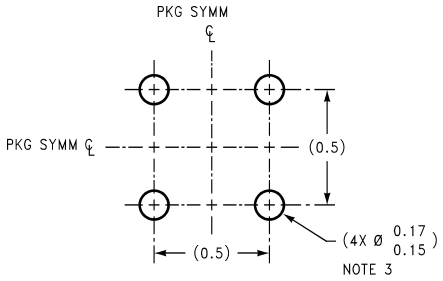
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NS Package Number Z03A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





DIMENSIONS ARE IN MILLIMETERS

LAND PATTERN RECOMMENDATION

BPA04XXX (REV A)

NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BA.

4-Bump micro SMD
X1 = 0.780 X2 = 0.900 X3 = 0.700
NS Package Number BPA04AFA

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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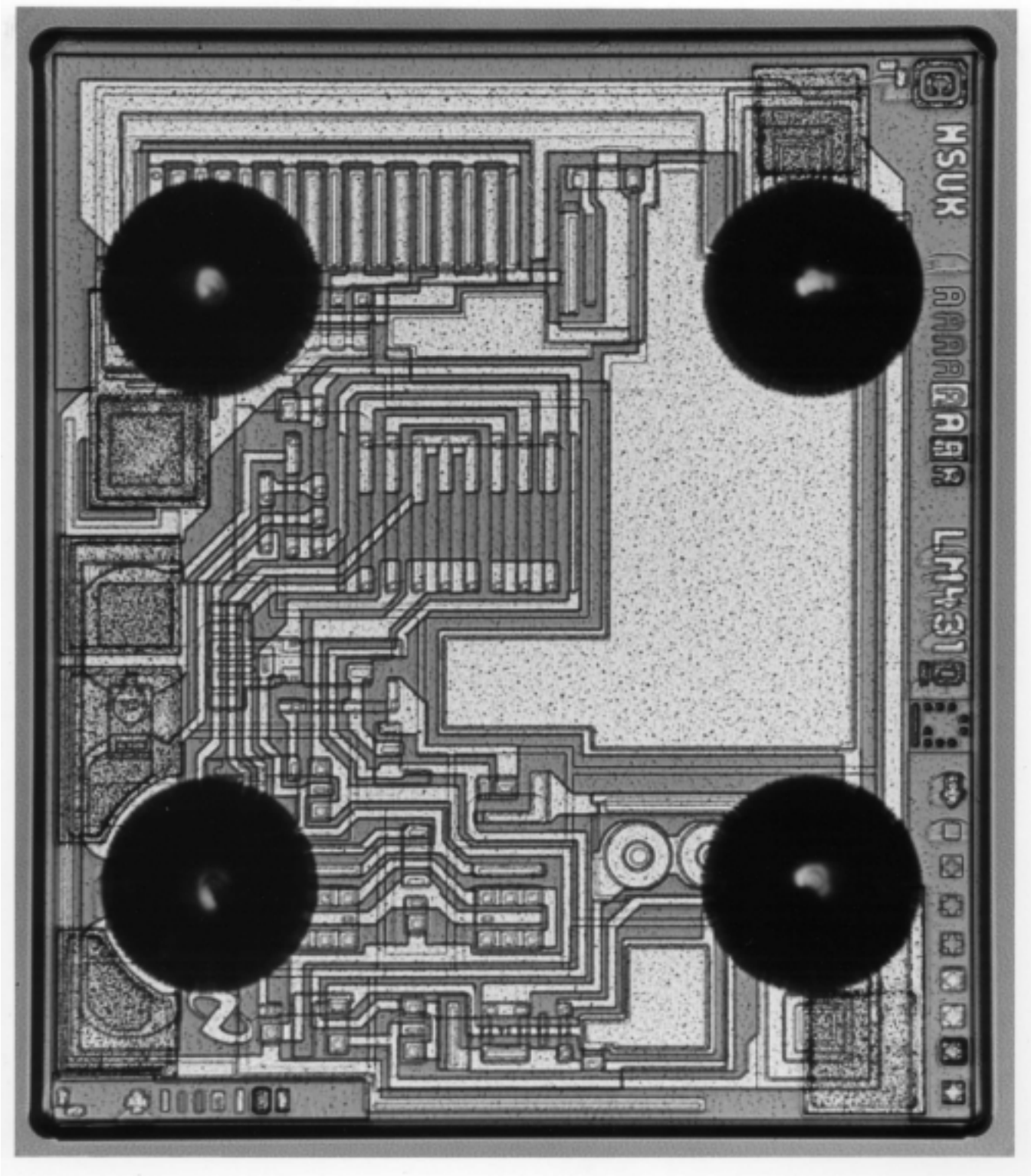
Fax: 81-3-5639-7507

3.2.2 Die Photo



3.3 PROCESS INFORMATION

3.3.1 Process Details

Fabrication Site:	Greenock, Scotland
Process Technology:	Bipolar DLM
Wafer diameter:	4 inches
No. of masks:	12
Starting:	P-type <111> Substrate
Metalisation:	Metal 110KA 4% Cual Metal 2 8.5 KA 4% Cual then 8.5KA pure Al TiW
Passivation:	10KA VOM 10KA Nitride

3.3.2 Masking Sequence

Mask #	Name
10	Collector
19	Up iso
20	Isolation
30	Base
40	Emitter
42	Capacitor
50	Contact
60	Metal 1
61	Via
61X	Via X (oversize)
65	Metal 2
70	Pad

3.3.3 Process Flow

1. Initial oxidation
2. Mask 10
3. SB implant
4. SB drive
5. Mask 19
6. Up iso implant
7. Epitaxial growth
8. Epitaxial Reoxidation
9. Mask 20
10. Isolation predeposition
11. Isolation drive
12. FTA adjust
13. FTA reoxidation
14. Mask 30
15. Pre base implant oxidation
16. Base implant
17. Base diffusion
18. Mask 40
19. Emitter diffusion
20. VOE
21. Getter
22. Mask 42
23. Mosox
24. Mask 50
25. Metal 1 Sputter
26. Mask 60
27. Via VOM
28. Mask 61
29. Mask 61X
30. TiW Sputter
31. Metal 2 sputter
32. Mask 65
33. VOM
34. Plasma Nitride
35. Mask 70 (Nitride)
36. Mask 70 (VOM)
37. EOL Anneal
38. Wafer test

3.3.4 Micro SMD Assembly Flow

1: Receive into Bump Assembly Processing	[wafer level]
2: 2nd Passivation	[wafer level]
3: Passivation Mask	[wafer level]
4: Passivation Etch	[wafer level]
5: UBM (under bump metal) Application	[wafer level]
6: UBM Etch	[wafer level]
7: Solder Bump Application	[wafer level]
8: Solder Bump Reflow	[wafer level]
9: Epoxy Back Side	[wafer level]
10: Laser Mark Back Side	[wafer level]
11: Electric Test	[wafer level]
12: Saw Scribe Singulation	[wafer level]
13: Pack in Tape/Reel	[individual part level]

3.4 RELIABILITY DATA

3.4.1 Reliability Report

National Semiconductor

	Reliability Test Report	File Number: FSC19990148 Originator: Alex Ruiz Date:May 10, 1999

Purpose

Qualification of the redesigned LM431 in the 4-Bump micro SMD package

Approvals

Reliability Engineer

Reliability Engineering Manager

Product Engineer

Product Engineering Manager

Reference File Numbers

RSC199900874
RSC199900923
RSC199901056
RSC199900995
RSC199900851
RSC199901415
RSC199900852
Q19980548

Distribution List

Product Line:
CK Tai

QA&R:
Bhatt MN, Alex Ruiz, Violetta Luis

Abstract

The LM431 underwent a redistribution utilizing dual layer metal process technology to convert the die for assembly in the 4-bump micro SMD package. The new die was subjected to reliability testing where the micro SMD devices were mounted on FR4 conversion boards in MDIP layout configuration for pre and post testing per qualification plan Q19980548. Three lots of the Rev D die passed 500 hours of SOPL in the 8L MDIP conversion board for qualification of the new layout. HBM ESD and MM ESD testing yields passing results. Three lots of the LM431 in the micro SMD package were subjected to preconditioned ACLV and THBT with no valid failures incurred through the respective release time-points for each test. Two lots in the micro SMD package were also subjected to preconditioned TMCL with zero valid failures.

Description

Test Request	Device Name	Sbgp	Wafer Die Run	Fab Loc	Tech Code	Pkg Code	# Leads	Assy Loc	Date Cd	Mold Comp
RSC199900851	LM431ACM	A		UK	LF	N/MDIP	8	SC		N/A
RSC199900852	LM431ACM	A		UK	LF	N/MDIP	8	SC	9431	N/A
RSC199900874	LM431ACM	A		UK	LF	N/MDIP	8	SC	9431	N/A
RSC199900923	LM431ACM	B		UK	LF	N/MDIP	8	SC		N/A
RSC199900995	LM431ACM	A		UK	LF	N/MDIP	8	SC		N/A
RSC199900995	LM431ACM	B		UK	LF	N/MDIP	8	SC		N/A
RSC199900995	LM431ACM	C		UK	LF	N/MDIP	8	SC		N/A
RSC199901056	LM431ACM	C		UK	LF	N/MDIP	8	SC		N/A
RSC199901415	LM431ACM	A		UK	LF	N/MDIP	8	SC		N/A

3.4 RELIABILITY DATA

Tests Performed

Test: Autoclave Test (ACLV)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900874	LM431ACM	A	100	15	121	
RSC199900923	LM431ACM	B	100	15	121	
RSC199901056	LM431ACM	C	100	15	121	

Timepoints:	Test Request	TP	Duration
	RSC199900874	1	96
	RSC199900923	1	96
	RSC199901056	1	96

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900995	LM431ACM	A			100	
RSC199900995	LM431ACM	B			100	
RSC199900995	LM431ACM	C			100	

Timepoints:	Test Request	TP	Duration
	RSC199900995	1	168
	RSC199900995	2	500

Test: Temperature Cycle (TMCL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900874	LM431ACM	A			150	-65
RSC199900923	LM431ACM	B			150	-65

Timepoints:	Test Request	TP	Duration
	RSC199900874	1	500
	RSC199900923	1	500

Test: Temperature Humidity Bias Test (THBT)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900851	LM431ACM	A	85		85	
RSC199900923	LM431ACM	B	85		85	
RSC199901056	LM431ACM	C	85		85	

Timepoints:	Test Request	TP	Duration
	RSC199900851	1	168
	RSC199900851	2	500
	RSC199900923	1	168
	RSC199900923	2	500
	RSC199901056	1	168
	RSC199901056	2	500

Test: Electrostatic Discharge - Machine Model (ESDM)

Test Request	Device	Method
RSC199900852	LM431ACM	ATE
(Tst# 2)	Sublot	Voltage
	1	50
	2	100
	3	150
	4	200
	5	250

Test: Electrostatic Discharge - Human Body Model (ESDH)

Test Request	Device	Method
RSC199901415	LM431ACM	ATE
(Tst# 1)	Sublot	Voltage
	1	1000
	2	1500
	3	2000
	4	2500

Preconditioning Flow: temp cycle - 5 cycles at -40/60C → bake - 16 hours at 125C → moisture sensitivity level 1 - moisture soak for 168 hours at 85C and 85%RH → 235C IR reflow , 3 passes → Flux immersion → DI water rinse → dry → electrical test (this is the IB1 MSL 1 flow)

Results/Discussion

LM431 RELIABILITY TEST RESULTS
(rejects/sample size)

Test	Time/Cycles	LM431 Test Lot 1	LM431 Test Lot 2	LM431 Test Lot 3
SOPL	168 hours	0/100	0/100	0/100
	500 hours	0/100	0/100	0/100
THBT	Post-precon	0/99*	0/100	0/99*
	168 hours	0/99	0/100	N/A
	500 hours	0/99	0/100	0/99
ACLV	Post-precon	0/49*	0/47*	0/48*
	96 hours	0/49	0/47	0/48
TMCL	Post-precon	0/94*	0/100	N/A
	500 cycles	0/94	0/100	N/A

Results/Discussion(cont)

LM431 ESD & LATCH-UP TEST RESULTS
(rejects/sample size)

Tests	Voltage	LM431
HBM ESD	500 VOLTS	0/4
	1000 VOLTS	0/4
	1500 VOLTS	0/4
	2000 VOLTS	0/4
	2500 VOLTS	0/4
MM ESD	50 VOLTS	0/4
	100 VOLTS	0/4
	150 VOLTS	0/4
	200 VOLTS	0/4
	250 VOLTS	0/4

Conclusion

The LM431 in the 4-bump micro SMD package is now fully qualified and approved for production release.

4.1 LM78L05IBP INTRODUCTION

4.1.1 General Product Description

The LM78L05IBP is a three terminal positive regulator with a fixed 5.0V output in the micro SMD (surface mount device) package. When used as a zener diode/resistor combination replacement, the LM78L05 is usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. The device can provide local on card regulation, eliminating the distribution problems associated with single point regulation.

Since the die is the package, the micro SMD is the smallest package possible, making it ideal for applications that can take advantage of a surface mount package that is smaller than SOT-23 and SC-70. The LM78L05 is also available in standard SO-8 and TO-92 packages. Please refer to the datasheet included in this booklet or visit National Semiconductor's website (http://www.national.com) for more information on those packages.

4.1.2 Technical Product Description

As with previous versions of the LM78L05, the LM78L05IBP is manufactured using National's single-layer metal bipolar process. National's name for the wafer-level chi-scale package used for the LM78L05 is micro SMD. Since assembly of the die is done at wafer level, there are additional wafer processing steps that are used instead of the usual assembly of a molded plastic surface mount package. These additional steps are covered under the Packaging Information section of this booklet.

The micro SMD version of the LM78L05 is assembled with 8 eutectic solder bumps (functioning as pins) on the active side of the die. The non-active side of the die is coated with epoxy and laser marked with a part number identification code, a die lot/date code, and a bump one identifier. The LM78L05 in micro SMD is shipped in standard 250 and 3,000 unit tape and reel. The devices are mounted on printed circuit boards bump side down using the same methods as other small surface mount packages.

For more information concerning application and use of the micro SMD package, please refer to Application Note AN-1112 included in this booklet

4.1.3 Reliability/Qualification Overview

The LM78L05 underwent a re-layout to provide the necessary spacing between the bond pads that enables proper surface mounting of the die. To qualify this new die, one lot of the micro SMD device was fabricated and mounted on conversion boards and went through operating life testing. Additional units were used to for human body model and machine model electrostatic discharge testing. The 8-bump micro SMD package was qualified by extension to the successful LMC6035 8-bump qualification.

4.1.4 Technical Assistance

Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

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Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80 5 30 85 85
English Tel: +49 (0) 1 80 5 32 78 32

Japan
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

Asia Pacific
Fax: 65-2504466
Email: sea.support@nsc.com
Tel: 65-2544466
(IDD telephone charge to be paid by caller)

See us on the Worldwide Web @ http://www.national.com

4.2 DEVICE INFORMATION

4.2.1 Datasheet

National Semiconductor

January 2000

LM78LXX Series
3-Terminal Positive Regulators

General Description

The LM78LXX series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a zener diode/resistor combination replacement, the LM78LXX usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM78LXX to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment.

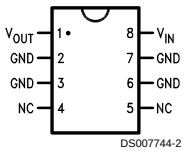
The LM78LXX is available in the plastic TO-92 (Z) package, the plastic SO-8 (M) package and a chip sized package (8-Bump micro SMD) using National's micro SMD package technology. With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistors is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Features

- LM78L05 in micro SMD package
- Output voltage tolerances of ±5% over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and plastic SO-8 low profile packages
- No external components
- Output voltages of 5.0V, 6.2V, 8.2V, 9.0V, 12V, 15V

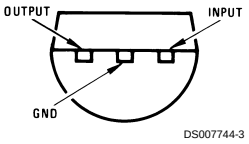
Connection Diagrams

SO-8 Plastic (M)
(Narrow Body)



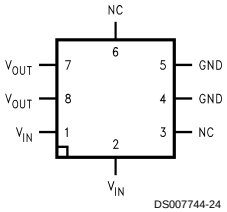
Top View

(TO-92)
Plastic Package (Z)



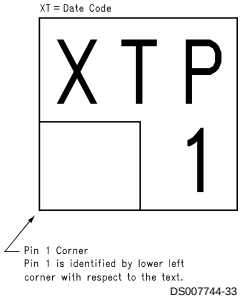
Bottom View

8-Bump micro SMD



Top View
(Bump Side Down)

micro SMD Marking Orientation



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation (Note 5)	Internally Limited
Input Voltage	35V
Storage Temperature	−65˚C to +150˚C
Operating Junction Temperature	
SO-8	0˚C to 125˚C
micro SMD	−40˚C to 85˚C
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C (lead time)
ESD Susceptibility (Note 2)	1kV

LM78LXX Electrical Characteristics

Limits in standard typeface are for T_J = 25˚C, **Bold typeface applies over 0ûC to 125ûC for SO-8 package and •40ûC to 85ûC for micro SMD package.** Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF.

LM78L05

Unless otherwise specified, V_{IN} = 10V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		4.8	5	5.2	V
		7V ≤ V_{IN} ≤ 20V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**4.75**		**5.25**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**4.75**		**5.25**	
ΔV_O	Line Regulation	7V ≤ V_{IN} ≤ 20V		18	75	mV
		8V ≤ V_{IN} ≤ 20V		10	54	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		20	60	
		1 mA ≤ I_O ≤ 40 mA		5	30	
I_Q	Quiescent Current			3	5	mA
ΔI_Q	Quiescent Current Change	8V ≤ V_{IN} ≤ 20V			**1.0**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage	f = 10 Hz to 100 kHz (Note 4)		40		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 8V ≤ V_{IN} ≤ 16V	47	62		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−0.65		mV/˚C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			6.7	7	V
θ_{JA}	Thermal Resistance (8-Bump micro SMD)			230.9		˚C/W

LM78L62AC

Unless otherwise specified, V_{IN} = 12V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		5.95	6.2	6.45	V
		8.5V ≤ V_{IN} ≤ 20V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**5.9**		**6.5**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**5.9**		**6.5**	
ΔV_O	Line Regulation	8.5V ≤ V_{IN} ≤ 20V		65	175	mV
		9V ≤ V_{IN} ≤ 20V		55	125	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		13	80	
		1 mA ≤ I_O ≤ 40 mA		6	40	

LM78L62AC (Continued)

Unless otherwise specified, V_{IN} = 12V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_Q	Quiescent Current			2	5.5	mA
ΔI_Q	Quiescent Current Change	8V ≤ V_{IN} ≤ 20V			**1.5**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage	f = 10 Hz to 100 kHz (Note 4)		50		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 10V ≤ V_{IN} ≤ 20V	40	46		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−0.75		mV/°C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			7.9		V

LM78L82AC

Unless otherwise specified, V_{IN} = 14V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		7.87	8.2	8.53	V
		11V ≤ V_{IN} ≤ 23V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**7.8**		**8.6**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**7.8**		**8.6**	
ΔV_O	Line Regulation	11V ≤ V_{IN} ≤ 23V		80	175	mV
		12V ≤ V_{IN} ≤ 23V		70	125	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		15	80	
		1 mA ≤ I_O ≤ 40 mA		8	40	
I_Q	Quiescent Current			2	5.5	mA
ΔI_Q	Quiescent Current Change	12V ≤ V_{IN} ≤ 23V			**1.5**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage	f = 10 Hz to 100 kHz (Note 4)		60		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 12V ≤ V_{IN} ≤ 22V	39	45		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−0.8		mV/°C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			9.9		V

LM78L09AC

Unless otherwise specified, V_{IN} = 15V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		8.64	9.0	9.36	V
		11.5V ≤ V_{IN} ≤ 24V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**8.55**		**9.45**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**8.55**		**9.45**	

LM78L09AC (Continued)

Unless otherwise specified, V_{IN} = 15V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ΔV_O	Line Regulation	11.5V ≤ V_{IN} ≤ 24V		100	200	mV
		13V ≤ V_{IN} ≤ 24V		90	150	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		20	90	
		1 mA ≤ I_O ≤ 40 mA		10	45	
I_Q	Quiescent Current			2	5.5	mA
ΔI_Q	Quiescent Current Change	11.5V ≤ V_{IN} ≤ 24V			**1.5**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage			70		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 15V ≤ V_{IN} ≤ 25V	38	44		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−0.9		mV/°C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			10.7		V

LM78L12AC

Unless otherwise specified, V_{IN} = 19V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		11.5	12	12.5	V
		14.5V ≤ V_{IN} ≤ 27V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**11.4**		**12.6**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**11.4**		**12.6**	
ΔV_O	Line Regulation	14.5V ≤ V_{IN} ≤ 27V		30	180	mV
		16V ≤ V_{IN} ≤ 27V		20	110	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		30	100	
		1 mA ≤ I_O ≤ 40 mA		10	50	
I_Q	Quiescent Current			3	5	mA
ΔI_Q	Quiescent Current Change	16V ≤ V_{IN} ≤ 27V			**1**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage			80		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 15V ≤ V_{IN} ≤ 25	40	54		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−1.0		mV/°C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			13.7	14.5	V

LM78L15AC

Unless otherwise specified, V_{IN} = 23V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		14.4	15.0	15.6	V
		17.5V ≤ V_{IN} ≤ 30V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**14.25**		**15.75**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**14.25**		**15.75**	
ΔV_O	Line Regulation	17.5V ≤ V_{IN} ≤ 30V		37	250	mV
		20V ≤ V_{IN} ≤ 30V		25	140	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		35	150	
		1 mA ≤ I_O ≤ 40 mA		12	75	
I_Q	Quiescent Current			3	5	mA
ΔI_Q	Quiescent Current Change	20V ≤ V_{IN} ≤ 30V			**1**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 18.5V ≤ V_{IN} ≤ 28.5V	37	51		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−1.3		mV/˚C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			16.7	17.5	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device outside of its stated operating conditions.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Power dissipation ≤ 0.75W.

Note 4: Recommended minimum load capacitance of 0.01 µF to limit high frequency noise.

Note 5: Typical thermal resistance values for the packages are:

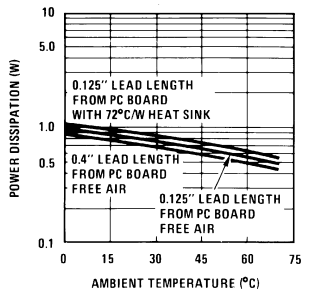
Z Package: θ_{JC} = 60 ˚C/W, = θ_{JA} = 230 ˚C/W

M Package: θ_{JA} = 180 ˚C/W

micro SMD Package: θ_{JA} = 230.9˚C/W

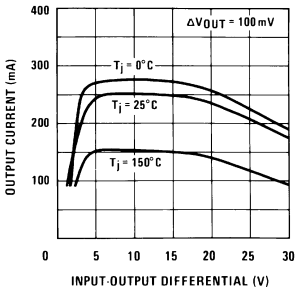
Typical Performance Characteristics

Maximum Average Power Dissipation (Z Package)



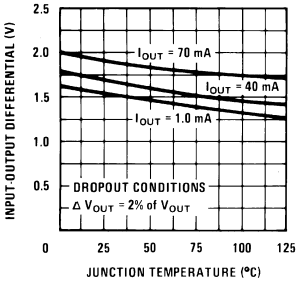
DS007744-14

Peak Output Current



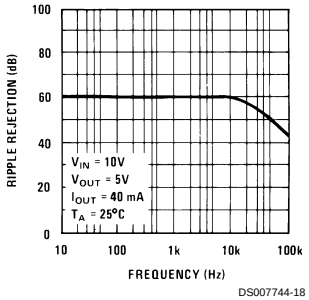
DS007744-16

Dropout Voltage



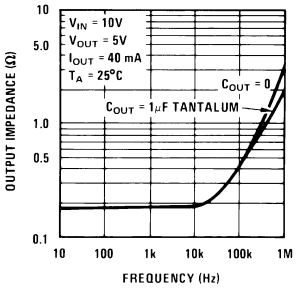
DS007744-17

Ripple Rejection



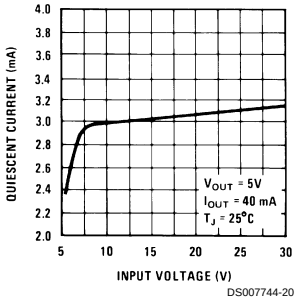
DS007744-18

Output Impedance



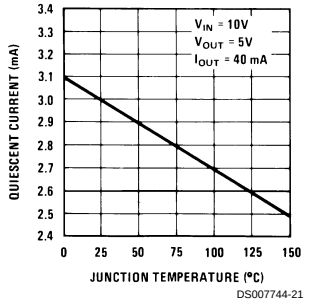
DS007744-19

Quiescent Current



DS007744-20

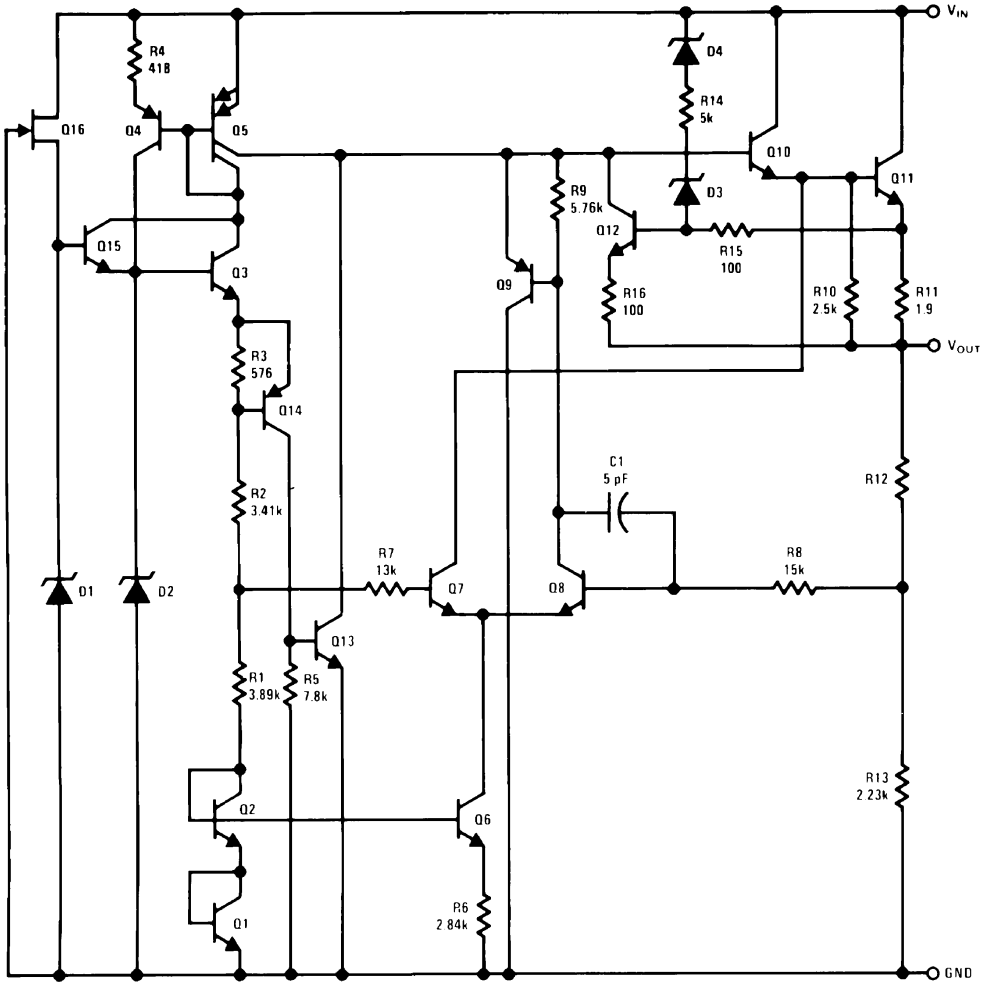
Quiescent Current



DS007744-21

Equivalent Circuit

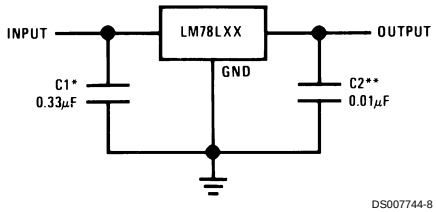
LM78LXX



DS007744-7

Typical Applications

Fixed Output Regulator

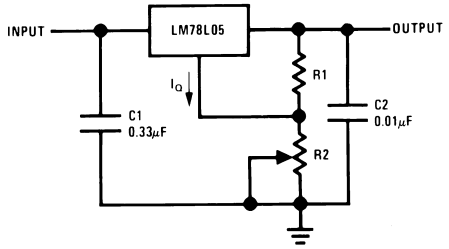


DS007744-8

*Required if the regulator is located more than 3" from the power supply filter.
**See (Note 4) in the electrical characteristics table.

Typical Applications (Continued)

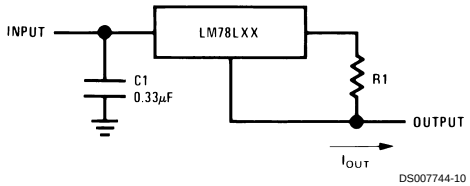
Adjustable Output Regulator



DS007744-9

V_{OUT} = 5V + (5V/R1 + I_Q) R2
5V/R1 > 3 I_Q, load regulation (L_r) ≈ [(R1 + R2)/R1] (L_r of LM78L05)

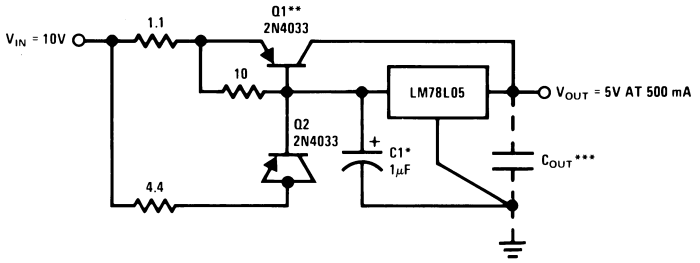
Current Regulator



DS007744-10

I_{OUT} = (V_{OUT}/R1) + I_Q
>I_Q = 1.5 mA over line and load changes

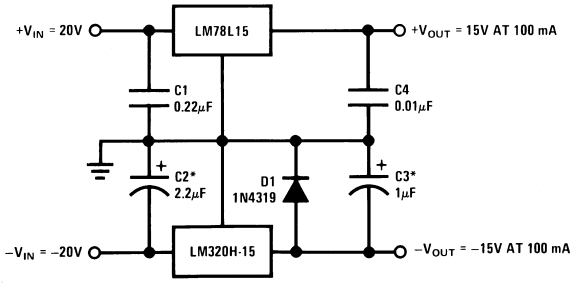
5V, 500 mA Regulator with Short Circuit Protection



DS007744-11

*Solid tantalum.
**Heat sink Q1.
***Optional: Improves ripple rejection and transient response.
Load Regulation: 0.6% 0 ≤ I_L ≤ 250 mA pulsed with t_{ON} = 50 ms.

±15V, 100 mA Dual Power Supply

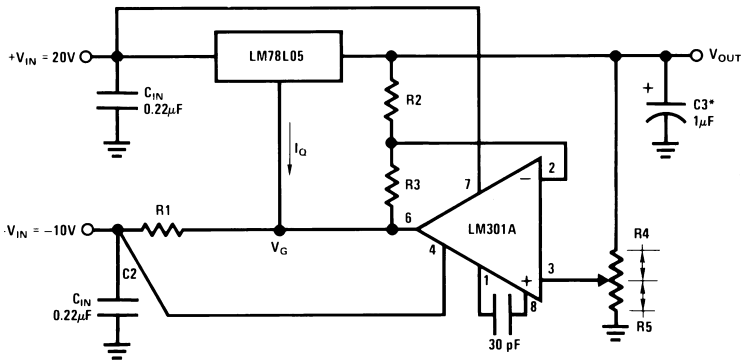


DS007744-12

*Solid tantalum.

Typical Applications (Continued)

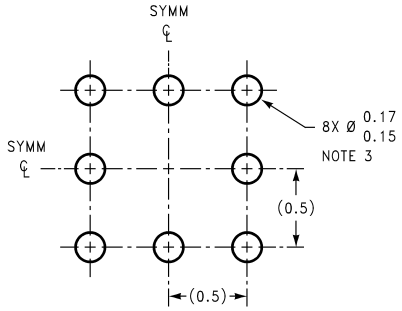
Variable Output Regulator 0.5V-18V



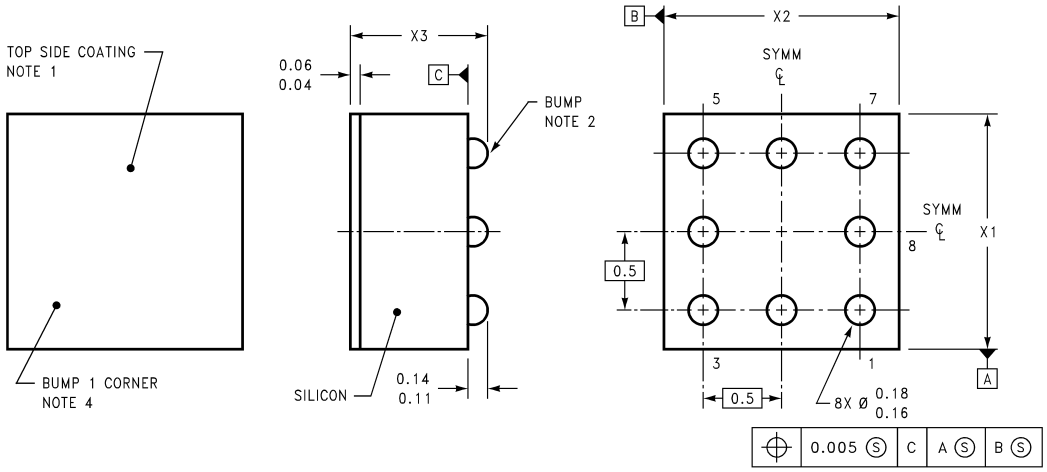
DS007744-13

*Solid tantalum.
$V_{OUT} = V_G + 5V$, $R1 = (-V_{IN}/I_{Q\ LM78L05})$
$V_{OUT} = 5V\ (R2/R4)$ for $(R2 + R3) = (R4 + R5)$
A 0.5V output will correspond to $(R2/R4) = 0.1\ (R3/R4) = 0.9$

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



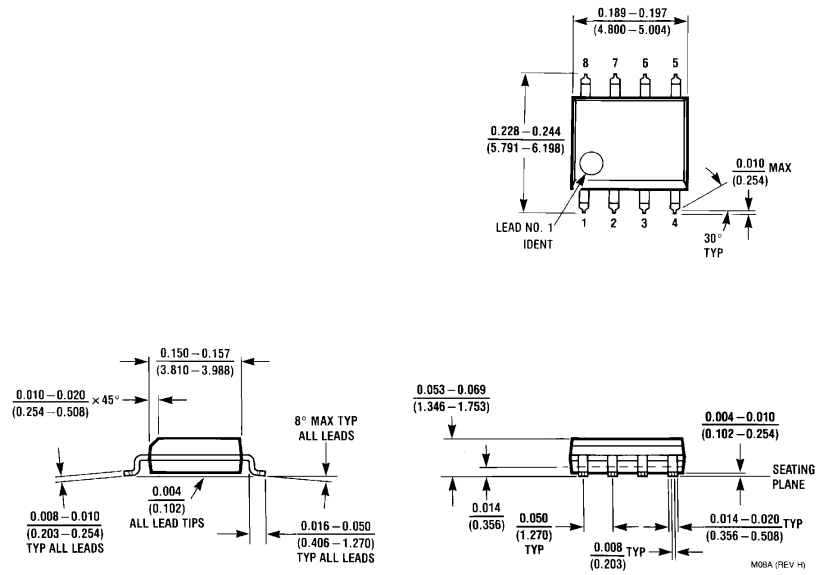
DIMENSIONS ARE IN MILLIMETERS BPA08XXX (REV A)

NOTES: UNLESS OTHERWISE SPECIFIED

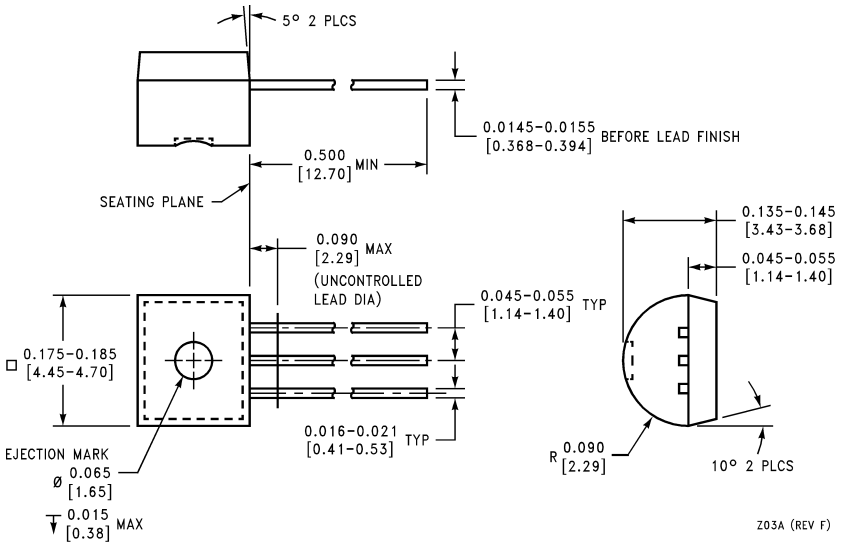
1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTERCLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X_1 IS PACKAGE WIDTH, X_2 IS PACKAGE LENGTH AND X_3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

8-Bump micro SMD
Order Number LM78L05IBP or LM78L05IBPX
NS Package Number BPA08AAA
X_1 = 1.285 X_2 = 1.285 X_3 = 0.7

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



S.O. Package (M)
Order Number LM78L05ACM, LM78L12ACM or LM78L15ACM
NS Package Number M08A



Molded Offset TO-92 (Z)
Order Number LM78L05ACZ, LM78L09ACZ, LM78L12ACZ,
LM78L15ACZ, LM78L62ACZ or LM78L82ACZ
NS Package Number Z03A

Notes

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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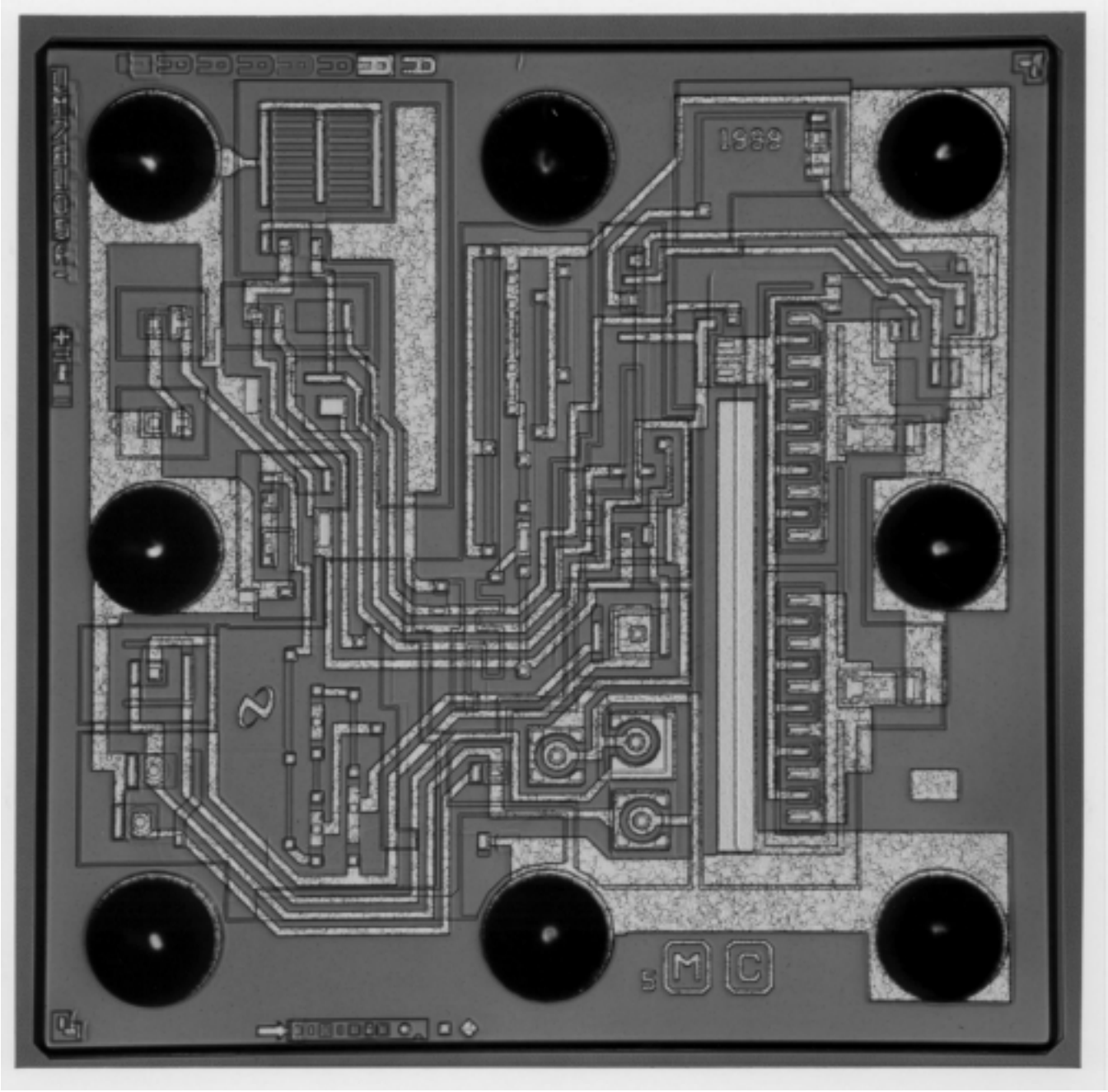
4.2.2 Die Photo



4.3 PROCESS INFORMATION

4.3.1 Process Details

Fabrication Site	Greenock, Scotland
Process Technology	Bipolar SLM
Wafer Diameter	4 inches
Number of Masks	9
Starting Material Substrate	P-type <111>
Metalization	0.5% CuAl
Passivation	10KA VOM 10KA Plasma Nitride

4.3.2 Masking Sequence

Mask #	Name
10	Collector
20	Isolation
30	Base
40	Emitter
41	Resistor Implant
42	Capacitor
50	Contact
60	Metal
70	Pad

4.3.3 Process Flow

1. Initial Oxidation
2. Mask 10
3. SB implant
4. SB drive
5. Epitaxial growth
6. Epitaxial re-oxidation
7. Mask 20
8. Iso Predeposition
9. Iso drive
10. FTA implant
11. Mask 30
12. Pre base oxidation
13. Base implant
14. Base diffusion
15. Mask 40
16. Emitter diffusion
17. Mask 41
18. Ion implant
19. VOE
20. Getter
21. Mask 42
22. Mosox
23. Mask 50
24. 0.5% CuAl sputter
25. Mask 60
26. VOM
27. Plasma Nitride
28. Mask 70
29. EOL Anneal
30. Wafer test

4.3.4 Micro SMD Assembly Flow

1: Receive into Bump Assembly Processing	[wafer level]
2: 2nd Passivation	[wafer level]
3: Passivation Mask	[wafer level]
4: Passivation Etch	[wafer level]
5: UBM (under bump metal) Application	[wafer level]
6: UBM Etch	[wafer level]
7: Solder Bump Application	[wafer level]
8: Solder Bump Reflow	[wafer level]
9: Epoxy Back Side	[wafer level]
10: Laser Mark Back Side	[wafer level]
11: Electric Test	[wafer level]
12: Saw Scribe Singulation	[wafer level]
13: Pack in Tape/Reel	[individual part level]

4.4 RELIABILITY DATA

4.4.1 Reliability Report

National Semiconductor

Reliability Test Report

File Number: FSC19990252
Originator: Alex Ruiz
Date: July 14, 1999

Purpose

Qualification of the redesigned LM78L05IBP in the 8-bump micro SMD package.

Approvals

Reliability Engineer	Date
Reliability Engineering Manager	Date
Product Line Engineer	Date
Product Line Engineering Manager	Date
Product Line General Manger	Date
Product Line V.P.	Date
Corporate Reliability Director	Date
QA&R V.P.	Date

Reference File Numbers

RSC199901849
RSC199901908
Q19990190

Distribution List

Standard Analog Product Group:
CK Tai, Sharon Ignaut

QA&R:
MN Bhatt, Richard Rosales, Gil Alcaraz, Violetta Luis, Alex Ruiz

Abstract

The Micro Surface Mount Device (micro SMD) is a version of a wafer level chip scale package where the package-size is the same as that of the die. Electrical connection to the outside world is made through solder bump construction on the Aluminum bond pad, where the die is flipped to solder on to the printed circuit board. The passivation and the BCB, along with the solder bumps form a protective barrier for the active area of the die from outside world contaminants. An Epoxy back coat done to the backside of the die is used for marking.

The LM78L05IBP is re-laid out so as to provide necessary spacing between the bond pads that enables proper surface mounting of this die. To qualify this new die, one lot of the micro SMD device was fabricated and mounted on conversion boards and tested through OPL. Additional units was also ESD tested.

The 8-bump micro SMD package was qualified by extension to the successful LMC6035 8-bump qualification (Q19980548, FSC19980255).

1) The LM78L05IBP has passed 500 hours OPL with no failure.
2) After completion of all ESD testing, it was found that the device only has 1500V HBM ESD rating. This data shows that the ESD rating is better than previous control unit ESD rating. Based on the HBM ESD comparison, the redesigned die has no impact on HBM ESD capability.
3) The datasheet for the LM78L05 states 2000V HBM ESD rating – a rating higher that the current ESD data. The LM78L05 datasheet information will be change by the product line to reflect the 1000V HBM ESD capability (see FSC19990221 action item).
4) There have been zero PQAs in the last two years for ESD related failures for the LM78L05 device.

Therefore, the LM78L05IBP is being released to production with a waiver for HBM ESD performance with no corrective action required.

4.4 RELIABILITY DATA

Description

Test Request	Device Name	Sbgp	Wafer Die Run	Fab Loc	Tech Code	Pkg Code	# Leads	Assy Loc	Date Cd	Mold Cmpnd
RSC199901849	LM78L05IBP	A	HL09A23G	UK	LF	C\SSWA	8	EM	9918	N/A
RSC199901908	LM78L05IBP	A	HL09A23G	UK	LF	C\SSWA	8	EM	9918	N/A

Tests Performed

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	High Temp
RSC199901849	LM78L05IBP	A	150

Timepoints:	Test Request	TP	Duration
	RSC199901849	1	168
	RSC199901849	2	500

Test: Electrostatic Discharge – Human Body Model (ESDH)

Test Request	Device	Method
RSC199901849	LM78L05IBP	ATE
(Tst# 1)	Sublot	Voltage
	1	500
	2	1000
	3	1500
	4	2000
	5	2500

Test: Electrostatic Discharge – Machine Model (ESDM)

Test Request	Device	Method
RSC199901908	LM78L05IBP	ATE
(Tst# 1)	Sublot	Voltage
	1	50
	2	100
	3	150
	4	200
	5	250

Results/Discussion

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199901849	LM78L05IBP	A	1	168	100	0
RSC199901849	LM78L05IBP	A	2	500	100	0

Test: Electrostatic Discharge – Human Body Model (ESDH)

Test Request	Device	Sbgrp	Sublot	Voltage	SS	#Failures	#ETRejects
RSC199901849	LM78L05IBP	A	1	500	5	0	0
RSC199901849	LM78L05IBP	A	2	1000	5	0	0
RSC199901849	LM78L05IBP	A	3	1500	5	0	0
RSC199901849	LM78L05IBP	A	4	2000	5	5	5
RSC199901849	LM78L05IBP	A	5	2500	5	0	5

Test: Electrostatic Discharge – Machine Model (ESDM)

Test Request	Device	Sbgrp	Sublot	Voltage	SS	#Failures	#ETRejects
RSC199901908	LM78L05IBP	A	1	50	5	0	0
RSC199901908	LM78L05IBP	A	2	100	5	0	0
RSC199901908	LM78L05IBP	A	3	150	5	0	0
RSC199901908	LM78L05IBP	A	4	200	5	0	0
RSC199901908	LM78L05IBP	A	5	250	5	0	0

Conclusion

The LM78L05IBP micro SMD qualification has successfully satisfied all reliability requirements as per qualification plan Q19990190 with the exception of Human Body Model (HBM) ESD testing. The LM78L05IBP device is being released to production with a waiver for HBM ESD performance with no requirement for corrective action.

The LM78L05IBP device, fabbed on the NSUK BIP Linear process and packaged in the 8-bump micro SMD package, is now fully qualified and approved for production release.

5.1 LMC555CBP INTRODUCTION

5.1.1 General Product Description

This qualification booklet covers the LMC555 CMOS timer in the 8-bump micro SMD (micro Surface Mount Device) package. The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation and supply current spikes. Since there is no package, the LMC555 in micro SMD is the smallest package possible, making it ideal for applications with board size constraints.

For more information concerning application and use of micro SMD, please refer to Application Note AN-1112 included in this booklet.

The LMC555 is also available in MSOP-8, SOIC-8, and MDIP-8 packages. Please refer to the datasheet included in this booklet or visit National Semiconductor's website (http://www.national.com) for more information on these packages.

5.1.2 Technical Product Description

As with previous versions of the LMC555, the LMC555CBP is manufactured using National's LMCMOS™ silicon poly gate CMOS process with 4-micron minimum channel length and single-layer metal on 6-inch wafers.

National's name for the wafer-level chip-scale package used for LMC555 is micro SMD (micro Surface Mount Device). Since assembly of the die is done at wafer level, there are additional wafer processing steps that are used instead of the usual assembly of a molded plastic surface mount package. These additional steps are covered under Packaging Information section of this qualification booklet.

The micro SMD version of LMC555 is assembled with 8 eutectic solder bumps (functioning as pins) on the active side of the die. The non-active side of the die is coated with epoxy and laser marked with a part number identification code and a die lot/date code. The LMC555 in micro SMD is shipped in standard 250 and 3,000 unit tape and reel. The devices are mounted on printed circuit boards bump side down using same methods as other small surface mount packages.

5.1.3 Reliability/Qualification Overview

The LMC555 underwent a complete re-layout to convert the die for assembly in the 8-bump micro SMD package. The new Rev B die was subjected to reliability testing in both the MDIP and micro SMD packages with passing results achieved on all stress tests. Two lots of the Rev B die passed 500 hours of Static Operating Life Testing in the 8-lead MDIP package for qualification of the new layout. Human Body Model ESD, Machine Model ESD, and Latch-up testing yielded equivalent or better results on the new Rev B die compared to the Rev A die. Two lots of the LMC555 in micro SMD package were subjected to preconditioned Autoclave, Temperature Cycle, and Temperature Humidity Bias testing with no failures incurred through the respective release timepoints for each test.

5.1.4 Technical Assistance

Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

Europe
Fax: +49 (0) 1 80 5 30 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80 5 30 85 85
English Tel: +49 (0) 1 80 5 32 78 32

Japan
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

Asia Pacific
Fax: 65-2504466
Email: sea.support@nsc.com
Tel: 65-2544466
(IDD telephone charge to be paid by caller)

See us on the Worldwide Web @ http://www.national.com

5.2 DEVICE INFORMATION

5.2.1 Datasheet

National Semiconductor

August 1999

LMC555
CMOS Timer

General Description

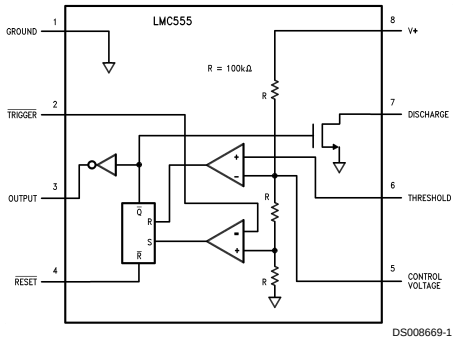
The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. In addition to the standard package (SOIC, MSOP, and MDIP) the LMC555 is also available in a chip sized package (8 Bump micro SMD) using National's micro SMD package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the stable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of National Semiconductor's LMCMOS™ process extends both the frequency range and low supply capability.

Features

- Less than 1 mW typical power dissipation at 5V supply
- 3 MHz astable frequency capability
- 1.5V supply operating voltage guaranteed
- Output fully compatible with TTL and CMOS logic at 5V supply
- Tested to −10 mA, +50 mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers
- Available in 8 pin MSOP Package and 8-Bump micro SMD package

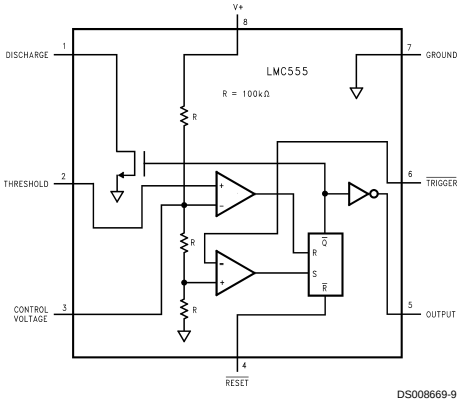
Block and Connection Diagrams

8-Pin SOIC, MSOP, and MDIP Packages



Top View

8-Bump micro SMD



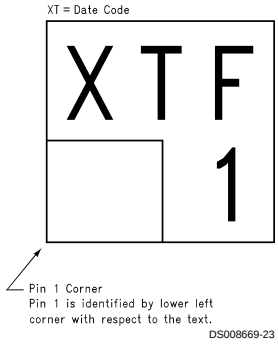
Top View
(bump side down)

LMCMOS™ is a trademark of National Semiconductor Corp.

Ordering Information

Package	Temperature Range	Package Marking	Transport Media	NSC Drawing
	Industrial −40˚C to +85˚C			
8-LeadSmall Outline (SO)	LMC555CM	LMC555CM	Rails	M08A
	LMC555CMX	LMC555CM	Tape and Reel	
8-Lead Mini Small Outline (MSOP)	LMC555CMM	ZC5	Rails	MUA08A
	LMC555CMX	ZC5	Tape and Reel	
8-Lead Molded Dip (MDIP)	LMC555CN	LMC555CN	Rails	N08E
8-Bump micro SMD	LMC555CBP	F1	250 Units Tape and Reel	BPA08EFB
	LMC555CBPX	F1	3k Units Tape and Reel	

micro SMD Marking Orientation
Top View



Bumps are numbered counter-clockwise

Absolute Maximum Ratings (Notes 2, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V^+	15V
Input Voltages, V_{TRIG}, V_{RES}, V_{CTRL}, V_{THRESH}	−0.3V to V_S + 0.3V
Output Voltages, V_O, V_{DIS}	15V
Output Current I_O, I_{DIS}	100 mA
Storage Temperature Range	−65˚C to +150˚C
Soldering Information	
MDIP Soldering (10 seconds)	260˚C
SOIC, MSOP Vapor Phase (60 sec)	215˚C
SOIC, MSOP Infrared (15 sec)	220˚C

Note: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Notes 2, 3)

Termperature Range	−40˚C to +85˚C
Thermal Resistance (θ_{JA}) (Note 2)	
SO, 8-lead Small Outline	169˚C/W
MSOP, 8-lead Mini Small Outline	225˚C/W
MDIP, 8-lead Molded Dip	111˚C/W
8-Bump micro SMD	220˚C/W
Maximum Allowable Power Dissipation @25˚C	
MDIP-8	1126mW
SO-8	740mW
MSOP-8	555mW
8 Bump micro SMD	568mW

Electrical Characteristics (Notes 1, 2)

Test Circuit, T = 25˚C, all switches open, $\overline{RESET}$ to V_S unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units (Limits)
I_S	Supply Current	V_S = 1.5V V_S = 5V V_S = 12V		50 100 150	150 250 400	µA
V_{CTRL}	Control Voltage	V_S = 1.5V V_S = 5V V_S = 12V	0.8 2.9 7.4	1.0 3.3 8.0	1.2 3.8 8.6	V
V_{DIS}	Discharge Saturation Voltage	V_S = 1.5V, I_{DIS} = 1 mA V_S = 5V, I_{DIS} = 10 mA		75 150	150 300	mV
V_{OL}	Output Voltage (Low)	V_S = 1.5V, I_O = 1 mA V_S = 5V, I_O = 8 mA V_S = 12V, I_O = 50 mA		0.2 0.3 1.0	0.4 0.6 2.0	V
V_{OH}	Output Voltage (High)	V_S = 1.5V, I_O = −0.25 mA V_S = 5V, I_O = −2 mA V_S = 12V, I_O = −10 mA	1.0 4.4 10.5	1.25 4.7 11.3		V
V_{TRIG}	Trigger Voltage	V_S = 1.5V V_S = 12V	0.4 3.7	0.5 4.0	0.6 4.3	V
I_{TRIG}	Trigger Current	V_S = 5V		10		pA
V_{RES}	Reset Voltage	V_S = 1.5V (Note 4) V_S = 12V	0.4 0.4	0.7 0.75	1.0 1.1	V
I_{RES}	Reset Current	V_S = 5V		10		pA
I_{THRESH}	Threshold Current	V_S = 5V		10		pA
I_{DIS}	Discharge Leakage	V_S = 12V		1.0	100	nA
t	Timing Accuracy	SW 2, 4 Closed V_S = 1.5V V_S = 5V V_S = 12V	 0.9 1.0 1.0	 1.1 1.1 1.1	 1.25 1.20 1.25	ms
$\Delta t/\Delta V_S$	Timing Shift with Supply	V_S = 5V ± 1V		0.3		%/V
$\Delta t/\Delta T$	Timing Shift with Temperature	V_S = 5V −40˚C ≤ T ≤ +85˚C		75		ppm/˚C
f_A	Astable Frequency	SW 1, 3 Closed, V_S = 12V	4.0	4.8	5.6	kHz
f_{MAX}	Maximum Frequency	Max. Freq. Test Circuit, V_S = 5V		3.0		MHz
t_R, t_F	Output Rise and Fall Times	Max. Freq. Test Circuit V_S = 5V, C_L = 10 pF		15		ns

Electrical Characteristics (Notes 1, 2)

Test Circuit, T = 25˚C, all switches open, $\overline{\text{RESET}}$ to V_S unless otherwise noted (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units (Limits)
t_{PD}	Trigger Propagation Delay	V_S = 5V, Measure Delay from Trigger to Output		100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

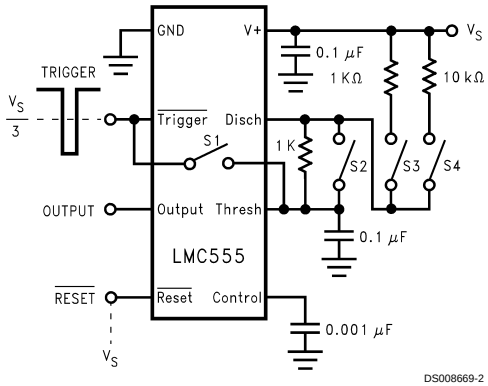
Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: See AN-450 for other methods of soldering surface mount devices, and also AN-1112 for micro SMD considerations.

Note 4: If the $\overline{\text{RESET}}$ pin is to be used at temperatures of −20˚C and below V_S is required to be 2.0V or greater.

Note 5: For device pinout please refer to table 1

Test Circuit (Note 5)



Maximum Frequency Test Circuit (Note 5)

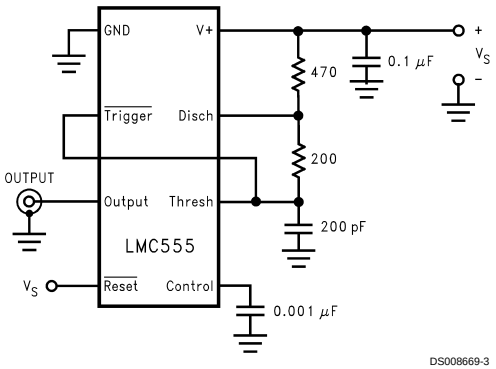


TABLE 1. Package Pinout Names vs. Pin Function

Pin Function	Package Pin numbers	
	8-Pin SO,MSOP, and MDIP	8-Bump micro SMD
GND	1	7
$\overline{\text{Trigger}}$	2	6
Output	3	5
$\overline{\text{Reset}}$	4	4
Control Voltage	5	3
Threshold	6	2
Discharge	7	1
V^+	8	8

Application Info

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by internal circuitry. Upon application of a negative trigger pulse of less than 1/3 V_S to the $\overline{\text{Trigger}}$ terminal, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

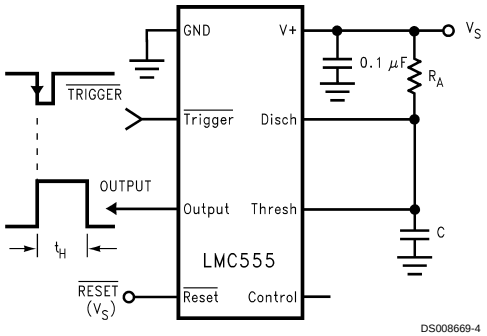
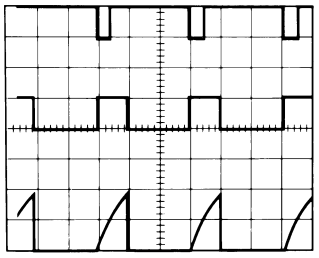


FIGURE 1. Monostable (One-Shot)

The voltage across the capacitor then increases exponentially for a period of $t_H = 1.1\ R_AC$, which is also the time that the output stays high, at the end of which time the voltage equals 2/3 V_S. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



V_{CC} = 5V
TIME = 0.1 ms/Div.
R_A = 9.1kΩ
C = 0.01µF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

FIGURE 2. Monostable Waveforms

Reset overrides Trigger, which can override threshold. Therefore the trigger pulse must be shorter than the desired t_H. The minimum pulse width for the Trigger is 20ns, and it is 400ns for the Reset. During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal. The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not use, it is recommended that it be connected to V_+ to avoid any possibility of false triggering. *Figure 3* is a nomograph for easy determination of RC values for various time delays.

Note: In monstable operation, the trigger should be driven high before the end of timing cycle.

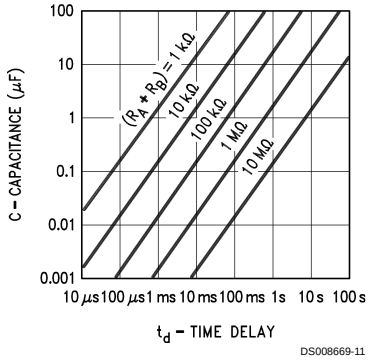


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* ($\overline{\text{Trigger}}$ and Threshold terminals connected together) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

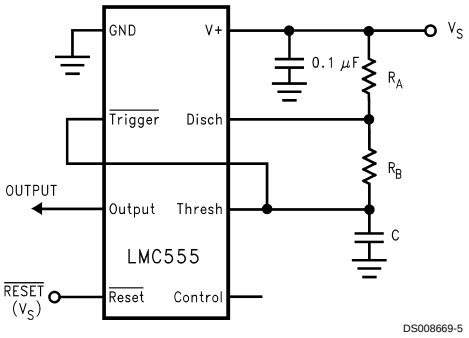
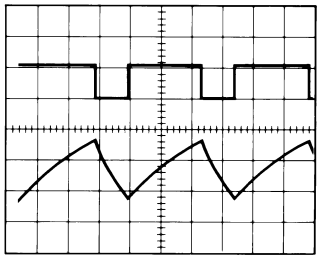


FIGURE 4. Astable (Variable Duty Cycle Oscillator)

In this mode of operation, the capacitor charges and discharges between 1/3 V_S and 2/3 V_S. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveform generated in this mode of operation.

Application Info (Continued)



V_{CC} = 5V Top Trace: Output 5V/Div.
TIME = 20 µs/Div. Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 9kΩ
C = 0.01µF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by

$$t_1 = Ln2\ (R_A + R_B)C$$

And the discharge time (output low) by:

$$t_2 = Ln2\ (R_B)C$$

Thus the total period is:

$$T = t_1 + t_2 = Ln2\ (R_A + R_B)C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\,C}$$

Figure 6 may be used for quick determination of these RC Values. The duty cycle, as a fraction of total period that the output is low, is:

$$D = \frac{R_B}{R_A + 2R_B}$$

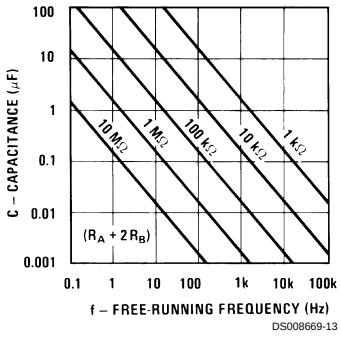
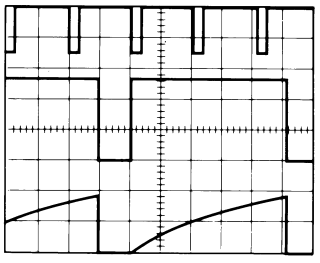


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



V_{CC} = 5V Top Trace: Input 4V/Div.
TIME = 20 µs/Div. Middle Trace: Output 2V/Div.
R_A = 9.1 kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01µF

FIGURE 7. Frequency Divider Waveforms

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to the Control Voltage Terminal. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

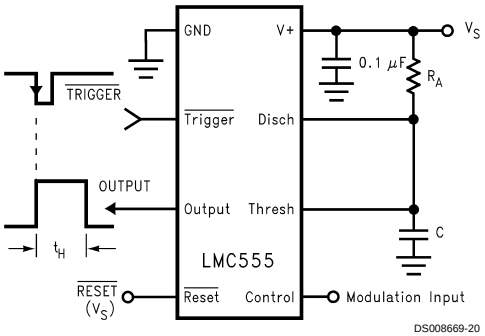
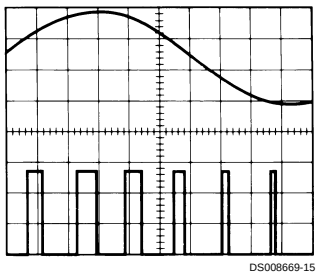


FIGURE 8. Pulse Width Modulator



V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/Div. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1 kΩ
C = 0.01µF

FIGURE 9. Pulse Width Modulator Waveforms

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with

Application Info (Continued)

the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

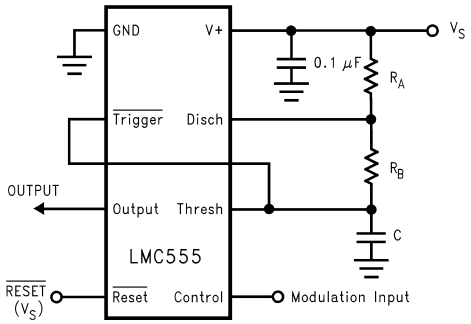
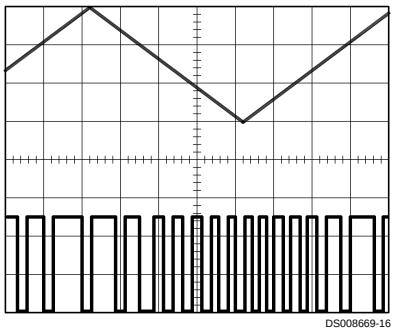


FIGURE 10. Pulse Position Modulator



V_{CC} = 5V
TIME = 0.1 ms/Div.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01µF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output Voltage 2V/Div.

FIGURE 11. Pulse Position Modulator Waveforms

50% DUTY CYCLE OSCILLATOR

The frequency of oscillation is

$$f = 1/(1.4\ R_C C)$$

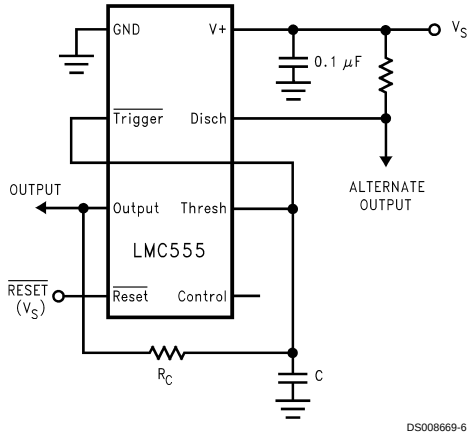
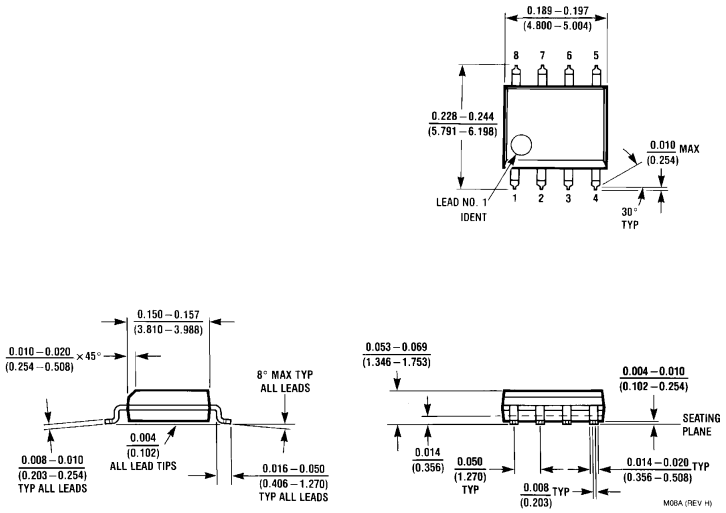


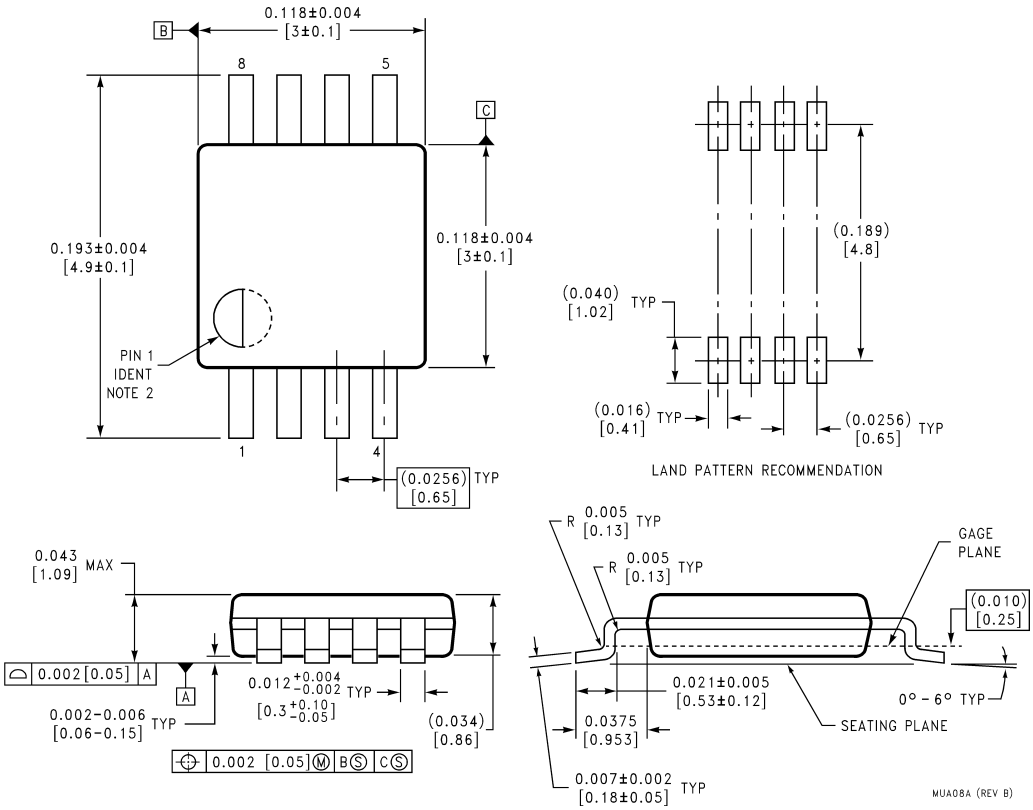
FIGURE 12. 50% Duty Cycle Oscillator

Physical Dimensions inches (millimeters) unless otherwise noted



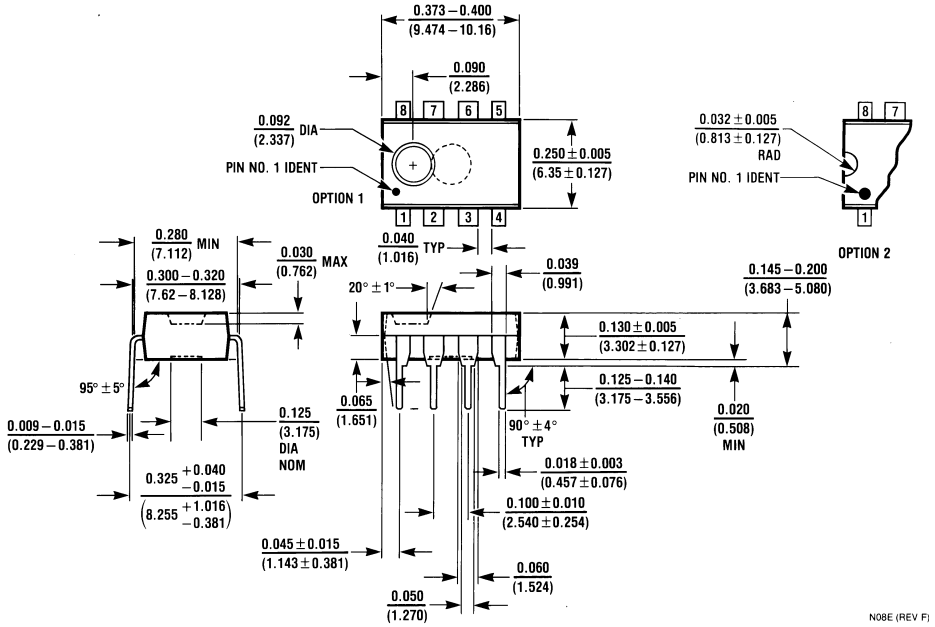
Molded Small Outline (SO) Package (M)
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



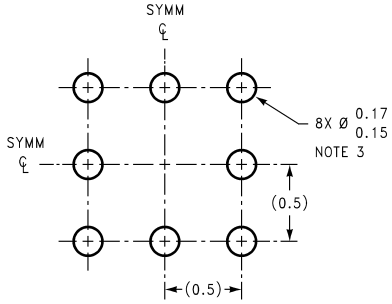
8-Lead (0.118ÓWide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

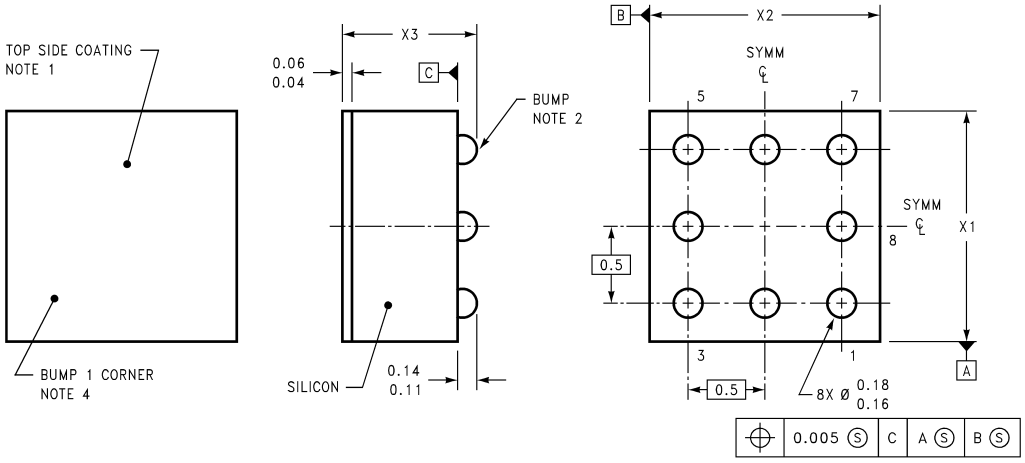


Molded Dual-in-line Package (N)
NS Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS BPA08XXX (REV A)

NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTERCLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

micro SMD Package
NS Package Number BPA08EFB
X_1 = 1.387 X_2 = 1.412 X_3 = 0.850

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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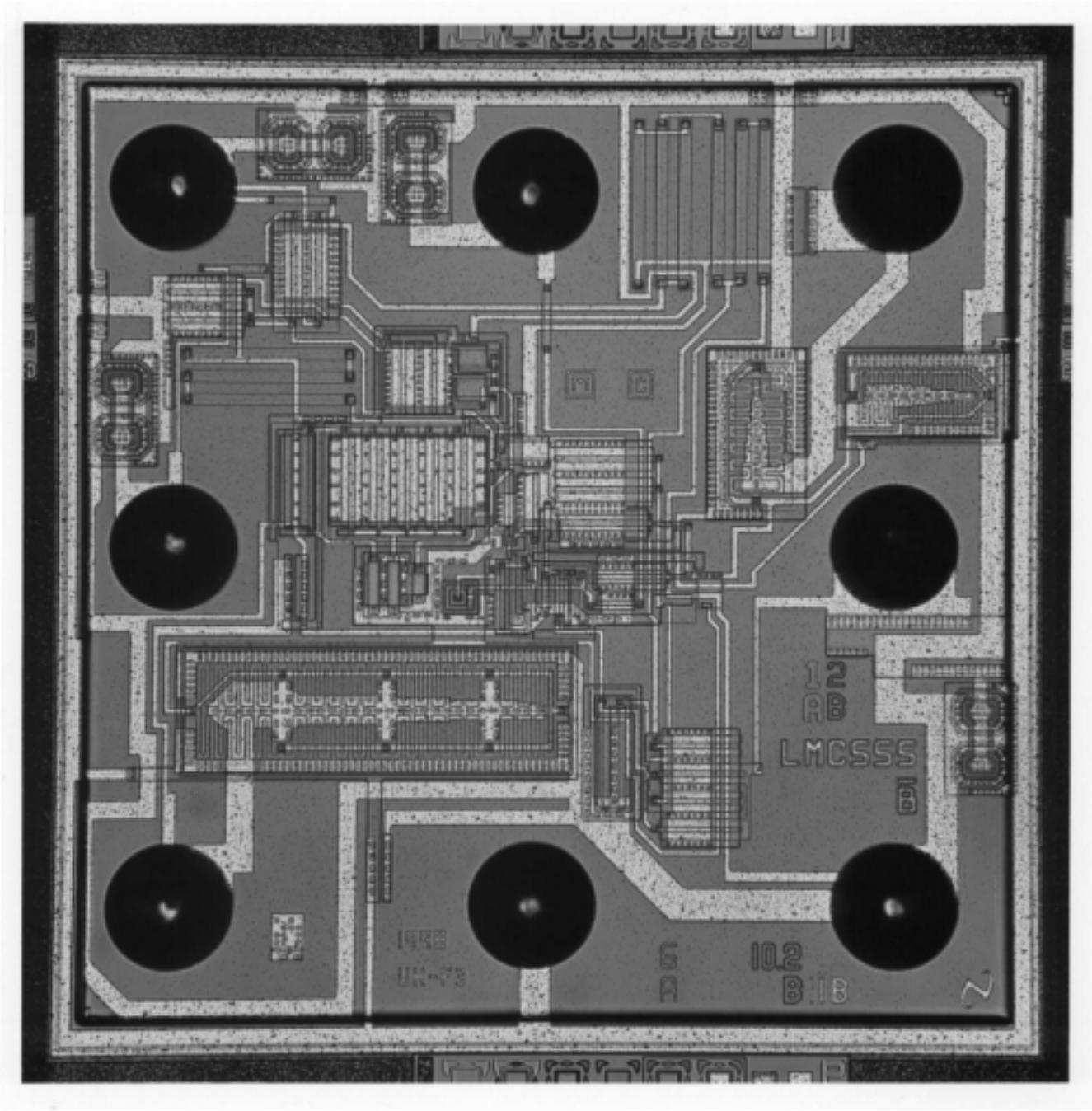
National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

5.2.2 Die Photo



5.3 PROCESS INFORMATION

5.3.1 Process Details

Fabrication Site: Greenock, Scotland
Process Technology: P2CMOS (silicon poly gate CMOS)
Minimum Feature Size: 4 microns
Wafer Diameter: 6 inches
Number of Masks: 14 (including bump assembly)
Metalization: Single Layer Aluminum (12,000Å thick)
Active Side Passivation: Nitride (11,000Å thick) over VOM (5000Å thick) with 2nd Passivation covering the Nitride/VOM

5.3.2 Process Mask Steps

Mask #	Name
1.0	P-
2.0	Composite
3.0	N- Field Implant
4.0	P- Field Implant
5.0	Vtp
6.0	Poly1
7.0	P+S/D Implant
8.0	N+S/D Implant
10.2	Contact
11.0	Metal
12.0	Passivation

5.3.3 Process Flow

1: Initial Oxide
2: Mask 1.0, P-
3: P- Implant
4: P- Drive
5: Field Oxide
6: Mask 2.0, Composite
7: Etch
8: Mask 3.0, N- Field Implant
9: N- Field Implant
10: Mask 4.0, P- Field Implant
11: P- Field Implant
12: Field Oxide
13: Etch
14: Gate Oxide
15: Mask 5.0, Vtp
16: Vtp Implant
17: Poly Dep
18: Back Etch
19: Poly Dope
20: Mask 6.0, Poly1
21: Etch
22: Mask 7.0, P+S/D Implant
23: P+ Implant
24: Mask 8.0, N+S/D Implant
25: N+ Implant
26: Rapid Thermal Anneal
27: Poly Reox
28: Poly Dep
29: Back Etch
30: Field Vapox
31: Mask 10.2, Contact
32: Etch
33: Ox Reflow
34: Metal Dep
35: Mask 11.0, Metal
36: Etch
37: Alloy
38: VOM
39: Nitride
40: Mask 12.0, Passivation
41: Etch
42: Final Alloy
43: Ship To Bump Assembly Processing

5.3.4 Micro SMD Assembly Flow

1: Receive into Bump Assembly Processing	[wafer level]
2: 2nd Passivation	[wafer level]
3: Passivation Mask	[wafer level]
4: Passivation Etch	[wafer level]
5: UBM (under bump metal) Application	[wafer level]
6: UBM Etch	[wafer level]
7: Solder Bump Application	[wafer level]
8: Solder Bump Reflow	[wafer level]
9: Epoxy Back Side	[wafer level]
10: Laser Mark Back Side	[wafer level]
11: Electric Test	[wafer level]
12: Saw Scribe Singulation	[wafer level]
13: Pack in Tape/Reel	[individual part level]

5.4 RELIABILITY DATA

5.4.1 Reliability Report

National Semiconductor

Reliability Test Report

File Number:
FSC19990124
Originator:
Nick Stanco
Date:April 21, 1999

Purpose

Qualification of the Redesigned LMC555 in the uSMD Package

Approvals

Nick Stanco — Reliability Engineer — Date: 4-22-99

Nick Stanco — Mgr. Rel. Engineering — Date: 4-22-99

Reference File Numbers

RSC199900961	RSC199901220
RSC199900964	RSC199901136
RSC199900966	Q19990124

Distribution List

Doug Simin
Nick Stanco

Abstract

The LMC555 underwent a complete re-layout to convert the die for assembly in the 8-bump uSMD package. The new Rev B die was subjected to reliability testing in both the MDIP and uSMD packages per qual plan Q19990124 with passing results achieved on all stress tests. Two lots of the Rev B die passed 500 hours of SOPL in the 8L MDIP package for qualification of the new layout. HBM ESD, MM ESD and Latch-up testing yielded equivalent or better results on the new Rev B die compared to the Rev A die. Two lots of the LMC555 in the uSMD package were subjected to preconditioned ACLV, TMCL and THBT with no failures incurred through the respective release timepoints for each test.

Description

Test Request	Device Name	Sbgp	Lot Description	Fab Loc	Tech Code	Pkg Code	# Leads	Assy Loc	Date Cd	Mold Cmpd
RSC199900961	LMC555CBP	A	Rev B Lot 1	UK	SH	C\SSWA	8	FCT	9906	N/A
RSC199900961	LMC555CBP	B	Rev B Lot 2	UK	SH	C\SSWA	8	FCT	9906	N/A
RSC199900966	LMC555CBP	A	Rev B Lot 1	UK	SH	C\SSWA	8	FCT	9906	N/A
RSC199900966	LMC555CBP	B	Rev B Lot 2	UK	SH	C\SSWA	8	FCT	9906	N/A
RSC199901136	LMC555CN	A	Rev B Lot 1	UK	SH	NWDIP	8	B1	9915	B8
RSC199901136	LMC555CN	B	Rev B Lot 2	UK	SH	NWDIP	8	B1	9915	B8
RSC199901136	LMC555CN	C	Rev A Control	UK	SH	NWDIP	8	EM	9852	B8
RSC199901220	LMC555CN	A	Rev A Control	UK	SH	NWDIP	8	EM	9852	B8
RSC199901220	LMC555CN	B	Rev B Lot 1	UK	SH	NWDIP	8	B1	9915	B8

Tests Performed

Test: Autoclave Test (ACLV)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900966	LMC555CBP	A	100	15	121	
RSC199900966	LMC555CBP	B	100	15	121	

Tests Performed (continued)

Test: Operating Life Test (Static) (SOPL)(static bias, ckt = 1353RE-B1, Vcc=5V)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199901136	LMC555CN	A			150	
RSC199901136	LMC555CN	B			150	
RSC199901136	LMC555CN	C			150	

Test: Temperature Cycle (TMCL)(preconditioned, air-air, 30 minutes/cycle)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900961	LMC555CBP	A			150	-65
RSC199900961	LMC555CBP	B			150	-65

Test: Temperature Humidity Bias Test (THBT)(preconditioned, static bias, ckt = 2989RE-A1, Vcc = 5V)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900966	LMC555CBP	A	85		85	
RSC199900966	LMC555CBP	B	85		85	

Test: Autoclave (ACLV)(preconditioned, unbiased)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199900966	LMC555CBP	A	100	2 atm	121	
RSC199900966	LMC555CBP	B	100	2 atm	121	

Test: Electrostatic Discharge - Human Body Model (ESDH)(1500Ω, 100 pf)

Test Request	Device	Method
RSC199901220	LMC555CN	ATE

Test: Electrostatic Discharge - Machine Model (ESDM)(0Ω, 200 pf)

Test Request	Device	Method
RSC199901220	LMC555CN	ATE

Test: Latch Up -Static (LUPS)(per RAI-5-050)

Test Request	Device	Fail Criteria	Method
RSC199901220	LMC555CN	0002	ATE

Preconditioning Flow: temp cycle - 5 cycles at -40/60C → bake - 16 hours at 125C → moisture sensitivity level 1 - moisture soak for 168 hours at 85C and 85%RH → 235C IR reflow , 3 passes → Flux immersion → DI water rinse → dry → electrical test (this is the IB1 MSL 1 flow)

Results/Discussion

LMC555 RELIABILITY TEST RESULTS
(rejects/sample size)

Test	Time/Cycles	LMC555 Die Rev A Control Lot	LMC555 Die Rev B Test Lot 1	LMC555 Die Rev B Test Lot 2
SOPL (8L MDIP)	168 hours	0/25	0/100	0/100
	500 hours	0/25	0/100	0/100
THBT (8-bump uSMD)	Post-precon		0/100	0/100
	500 hours		0/100	0/100
ACLV (8-bump uSMD)	Post-precon		0/50	0/50
	96 hours		0/50	0/50
TMCL (8-bump uSMD)	Post-precon		0/100	0/100
	500 cycles		0/100	0/97

Results/Discussion (continued)

LMC555 ESD & LATCH-UP TEST RESULTS (rejects/sample size)			
Tests	Voltage	LMC555 Die Rev A Control Lot	LMC555 Die Rev B Test Lot 1
HBM ESD	500 VOLTS	0/4	0/4
	1000 VOLTS	4/4	0/4
	1500 VOLTS	4/4	0/4
	2000 VOLTS	4/4	1/4
	2500 VOLTS	4/4	2/4
MM ESD	50 VOLTS	0/4	0/4
	100 VOLTS	0/4	0/4
	150 VOLTS	1/4	0/4
	200 VOLTS	4/4	0/4
	250 VOLTS	4/4	0/4
LATCH-UP	25°C	0/5	0/5
	85°C	0/5	0/5

Conclusion

Die Revision B of the LMC555 in the 8-bump uSMD package is now fully qualified and approved for production release.

6.1 PACKAGING INFORMATION

6.1 Package Material

	LM358BP	LMC6035IBP	LM431AIBP
Generic Package Type	8-Bump Micro SMD	8-Bump Micro SMD	4-Bump Micro SMD
NS Package Number	BPA08AAA	BPA08FFB	BPA04AFA
Bump Material	Eutectic Solder	Eutectic Solder	Eutectic Solder
Bump Mechanical: Stress Buffer Material (Active side of die)	2nd Passivation	2nd Passivation	2nd Passivation
Back Side Coating Material (Non-active side of die)	Epoxy	Epoxy	Epoxy
Package Thermal	230°C/W	220°C/W	337°C/W

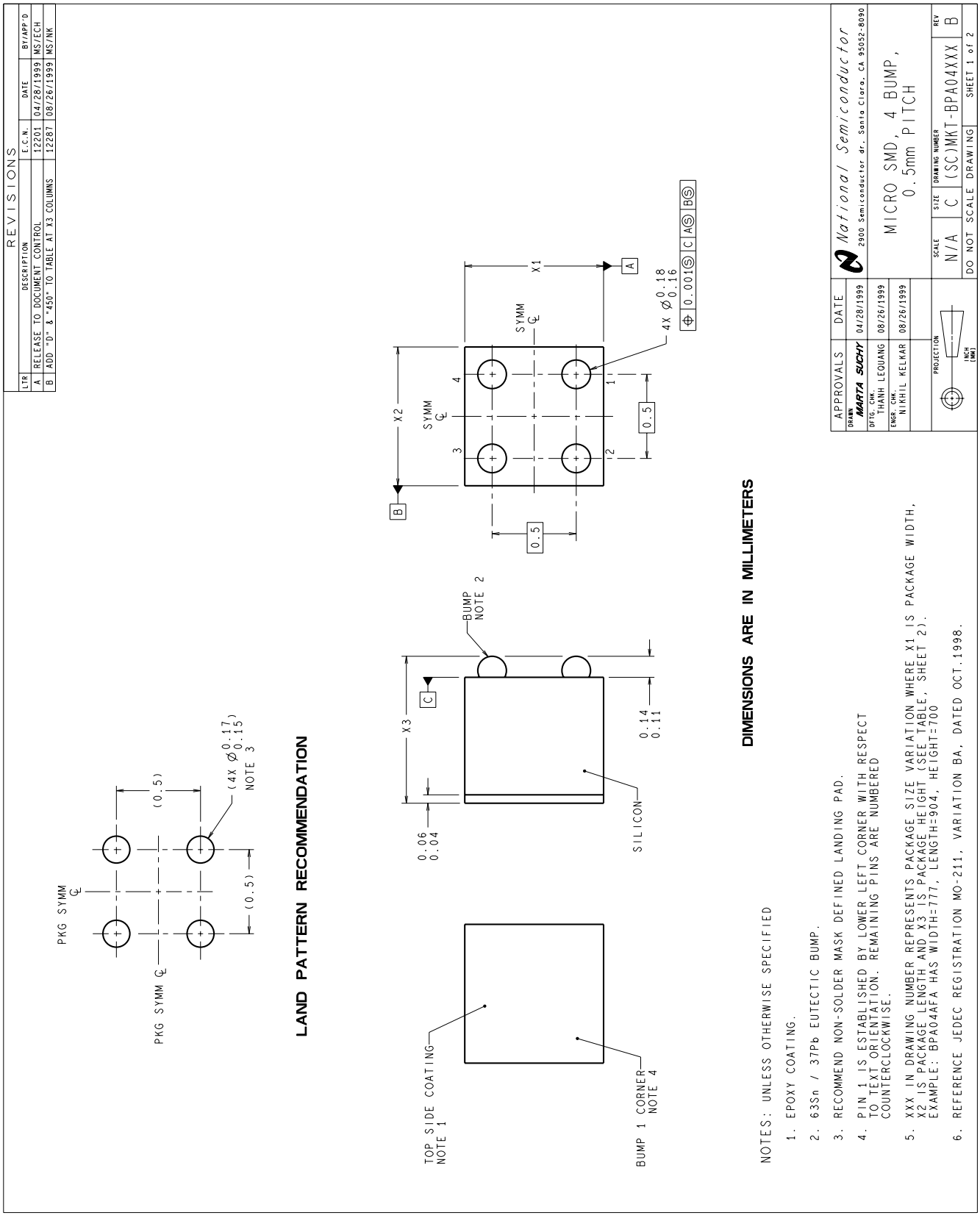
	LM78L05IBP	LMC555CBP
Generic Package Type	8-Bump Micro SMD	8-Bump Micro SMD
NS Package Number	BPA08AAA	BPA08EFB
Bump Material	Eutectic Solder	Eutectic Solder
Bump Mechanical: Back Side Coating Material (Active side of die)	2nd Passivation	2nd Passivation
Back Side Coating Material (Non-active side of die)	Epoxy	Epoxy
Package Thermal	230°C/W	220°C/W

6.2 PACKAGE DIMENSIONS

6.2.1 Reference Table

Part Number	Drawing Number	X1 Designator	X2 Designator	X3 Designator
LM358BP	BPA08XXX	A	A	A
LMC6035IBP	BPA08XXX	F	F	B
LM431AIBP	BPA04XXX	A	F	A
LM78L05IBP	BPA08XXX	A	A	A
LMC555CBP	BPA08XXX	E	F	B

6.2.2 4-Bump micro SMD



REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
	SEE SHEET 1			

PACKAGE DIMENSIONS					
X1 DESIGNATOR	X1 PACKAGE WIDTH ±30µm	X2 DESIGNATOR	X2 PACKAGE LENGTH ±30µm	X3 DESIGNATOR	X3 PACKAGE HEIGHT ±50µm
A	777	A	777	A	700
B	803	B	803	B	850
C	828	C	828	C	900
D	853	D	853	D	450
E	879	E	879		
F	904	F	904		
G	930	G	930		
H	955	H	955		
J	980	J	980		
K	1006	K	1006		
L	1031	L	1031		
M	1057	M	1057		
N	1082	N	1082		
P	1107	P	1107		
Q	1133	Q	1133		
R	1158	R	1158		
S	1184	S	1184		
T	1209	T	1209		
U	1234	U	1234		
V	1260	V	1260		
W	1285	W	1285		
X	1311	X	1311		
Y	1336	Y	1336		
2	1361	2	1361		
3	1387	3	1387		
4	1412	4	1412		
5	1438	5	1438		
6	1463	6	1463		

APPROVALS	DATE
DRAWN MARTA SUCHY	04/28/1999
DFTG. CHK. THANH LEQUANG	08/26/1999
ENGR. CHK. NIKHIL KELKAR	08/26/1999

PROJECTION

INCH [MM]

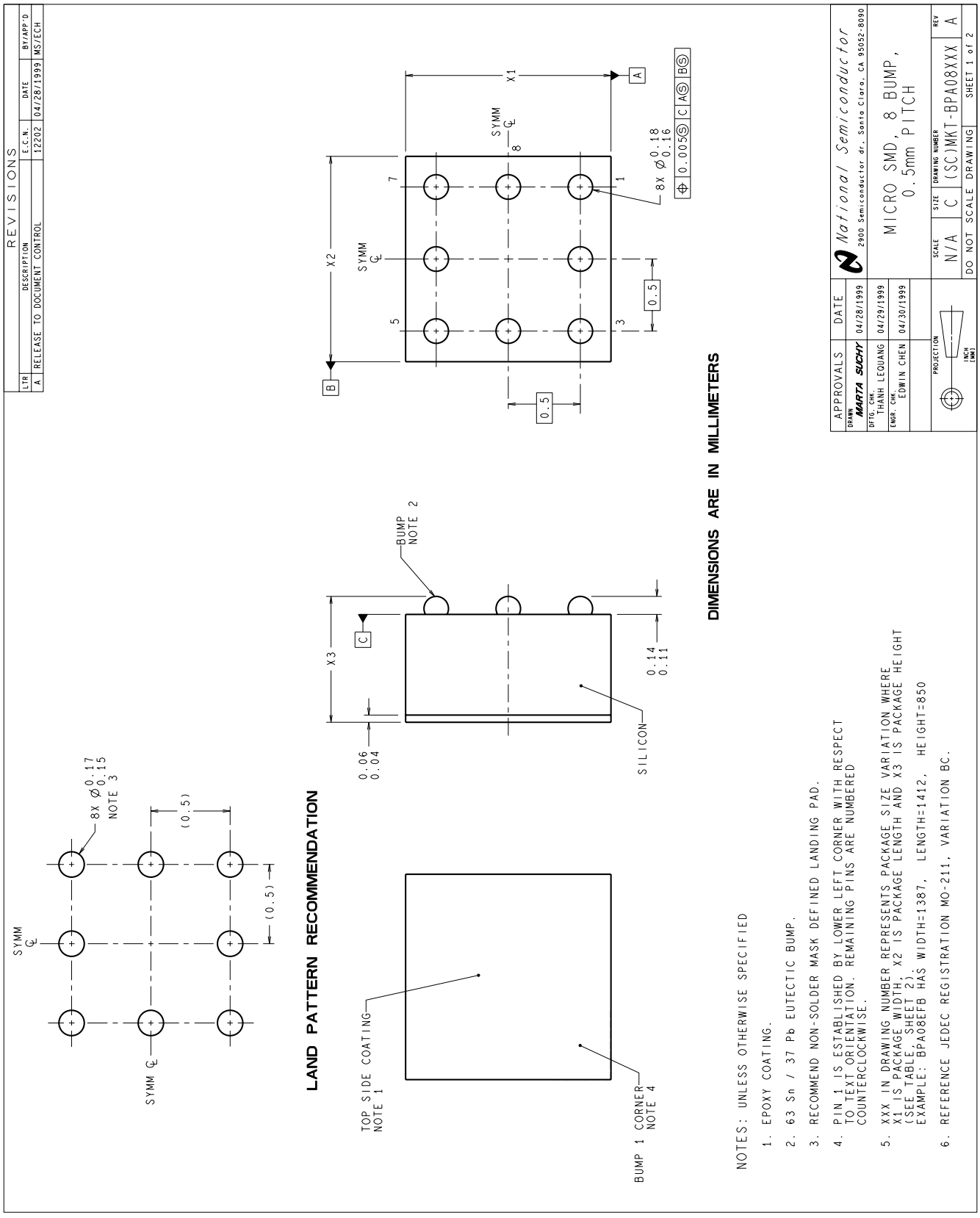
National Semiconductor
2900 Semiconductor dr. Santa Clara, CA 95052-8090

MICRO SMD, 4 BUMP, 0.5mm PITCH

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-BPA04XXX	B

DO NOT SCALE DRAWING | SHEET 2 of 2

6.2.3 8-Bump micro SMD



REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
	SEE SHEET 1			

8 BUMP NOMINAL PACKAGE DIMENSIONS					
X1 DESIGNATOR	X1 PACKAGE WIDTH (±30µm)	X2 DESIGNATOR	X2 PACKAGE LENGTH (±30µm)	X3 DESIGNATOR	X3 PACKAGE HEIGHT (±50µm)
A	1285	A	1285	A	700
B	1311	B	1311	B	850
C	1336	C	1336	C	900
D	1361	D	1361		
E	1387	E	1387		
F	1412	F	1412		
G	1438	G	1438		
H	1463	H	1463		
J	1488	J	1488		
K	1514	K	1514		
L	1539	L	1539		
M	1565	M	1565		
N	1590	N	1590		
P	1615	P	1615		
Q	1641	Q	1641		
R	1666	R	1666		
S	1692	S	1692		
T	1717	T	1717		
U	1742	U	1742		
V	1768	V	1768		
W	1793	W	1793		
X	1819	X	1819		
Y	1844	Y	1844		
2	1869	2	1869		
3	1895	3	1895		
4	1920	4	1920		
5	1946	5	1946		
6	1971	6	1971		

APPROVALS	DATE
DRAWN MARTA SUCHY	04/28/1999
DFTG. CHK. THANH LEQUANG	04/29/1999
ENGR. CHK. EDWIN CHEN	04/30/1999

PROJECTION

INCH [MM]

National Semiconductor
2900 Semiconductor dr., Santa Clara, CA 95052-8090

MICRO SMD, 8 BUMP, 0.5mm PITCH

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-BPA08XXX	A

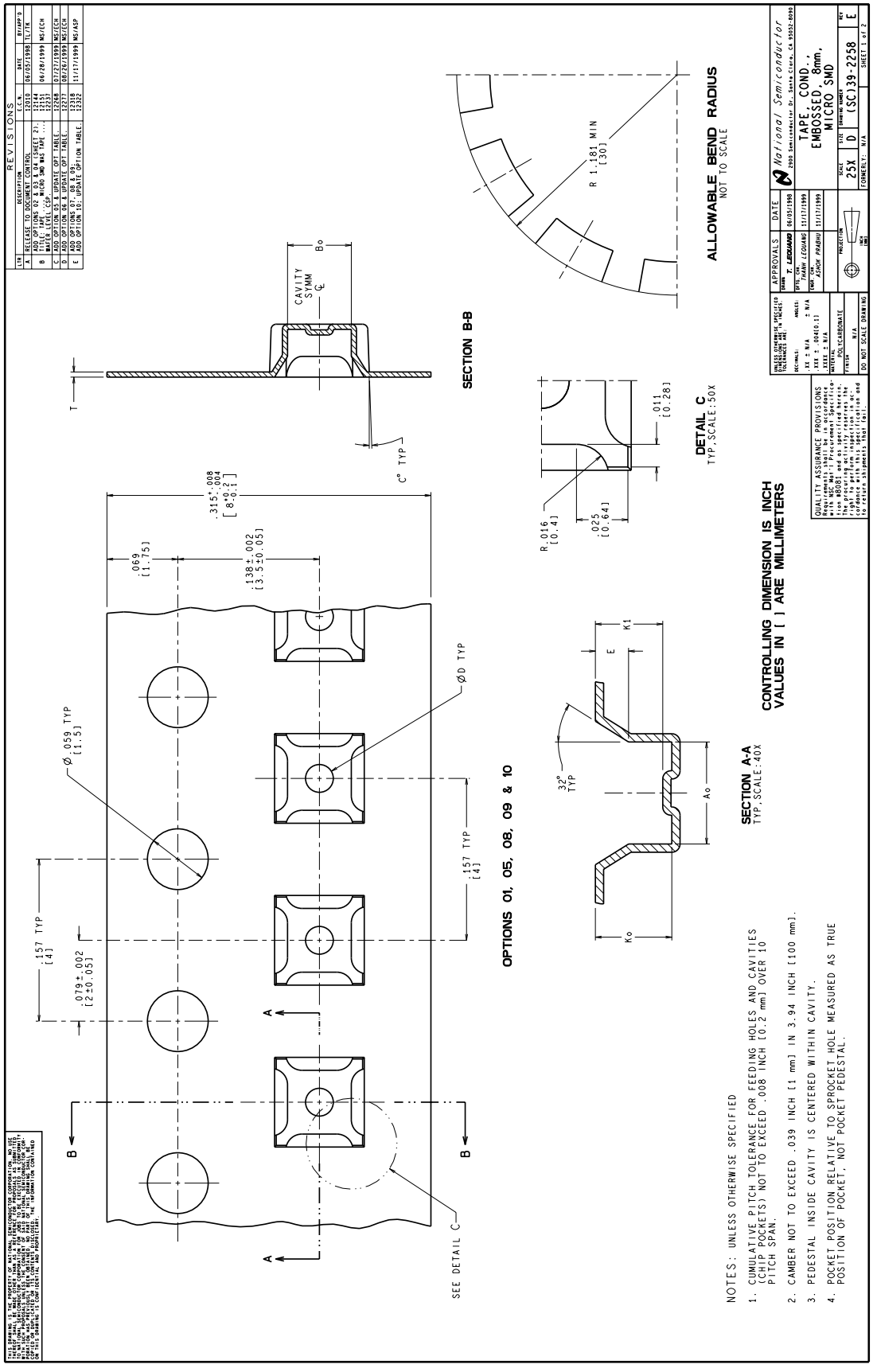
DO NOT SCALE DRAWING | SHEET 2 of 2

6.3 TAPE & REEL DIMENSIONS

6.3.1 Reference Table

Part Number	Option
LM358BP	01
LMC6035IBP	01
LM431AIBP	03
LM78L05IBP	01
LMC555CBP	01

6.3.2 Tape & Reel Drawing



REVISIONS

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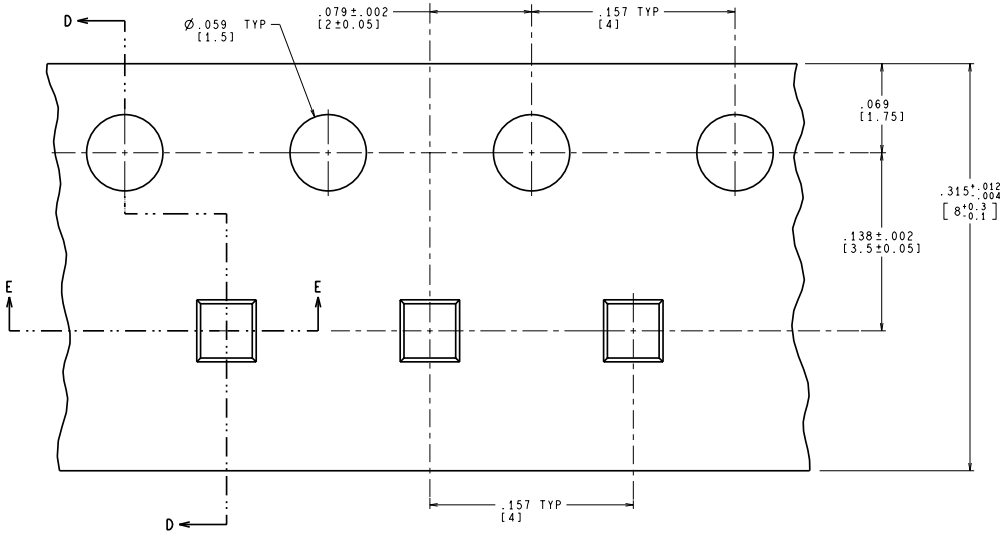
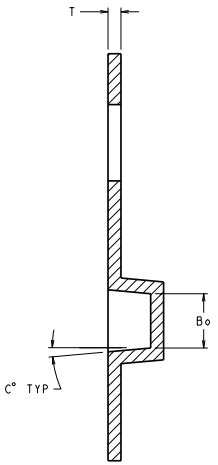
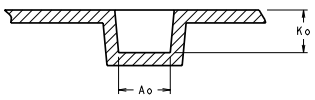
	SEE SHEET 1			



OPTIONS 02, 03, 04, 06 & 07
SCALE: 25X



SECTION D-D



SECTION E-E

OPTION	STOCK #	PIN COUNT	DIM Ao	DIM Bo	DIM C	DIM D	DIM E	DIM Ko	DIM K1	DIM T
10	071922	10	.086±.002 [2.03±0.05]	.106±.002 [2.69±0.05]	5° MAX	.027 [0.69]	.02 [0.51]	.044±.002 [1.12±0.05]	.039 [0.99]	.0100±.0005 [0.254±0.013]
09	071833	10	.071±.002 [1.8±0.05]	.085±.002 [2.16±0.05]	5° MAX	.027 [0.69]	.02 [0.51]	.044±.002 [1.12±0.05]	.039 [0.99]	.0100±.0005 [0.254±0.013]
08	071832	8	.062±.002 [1.57±0.05]	.073±.002 [1.85±0.05]	5° MAX	.027 [0.69]	.02 [0.51]	.041±.002 [1.04±0.05]	.036 [0.91]	.0100±.0005 [0.254±0.013]
07	071831	4	.035±.002 [0.89±0.05]	.035±.002 [0.89±0.05]	5° MAX	N/A	N/A	.023±.002 [0.58±0.05]	N/A	.0100±.0005 [0.254±0.013]
06	071504	4 & 5	.044±.002 [1.12±0.05]	.051±.002 [1.30±0.05]	5° MAX	N/A	N/A	.040±.002 [1.02±0.05]	N/A	.0100±.0005 [0.254±0.013]
05	070930	8	.062±.002 [1.57±0.05]	.087±.002 [2.21±0.05]	2° MAX	.027±.002 [0.69±0.05]	.012±.002 [0.3±0.05]	.041±.002 [1.04±0.05]	.036±.002 [0.91±0.05]	.0100±.0008 [0.254±0.02]
04	070269	4	.039±.002 [0.99±0.05]	.039±.002 [0.99±0.05]	2° MAX	N/A	N/A	.040±.002 [1.02±0.05]	N/A	.0100±.0005 [0.254±0.013]
03	069526	4	.037±.002 [0.94±0.05]	.042±.002 [1.07±0.05]	5° MAX	N/A	N/A	.033±.002 [0.84±0.05]	N/A	.0100±.0005 [0.254±0.013]
02	069418	4	.037±.002 [0.94±0.05]	.037±.002 [0.94±0.05]	2° MAX	N/A	N/A	.039±.002 [0.99±0.05]	N/A	.0100±.0005 [0.254±0.013]
01	067816	8	.062±.002 [1.57±0.05]	.062±.002 [1.57±0.05]	2° MAX	.027 [0.69]	.02 [0.51]	.046±.002 [1.18±0.05]	.041 [1.04]	.0100±.0005 [0.254±0.013]

CONTROLLING DIMENSIONS IS INCH VALUES IN [ ] ARE MILLIMETERS

QUALITY ASSURANCE PROVISIONS
Requirements shall be in accordance with NSC Mat'l Procurement Specification #8081 and as specified herein. The procuring activity reserves the right to perform inspection in accordance with this specification and to return shipments that fail.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE:
DECIMALS: ANGLES:
.XX ± N/A ± N/A
.XXX ± .004[0.1]
.XXXX ± N/A
MATERIAL: POLYCARBONATE
FINISH: N/A
DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN T. LEQUANG	06/05/1998
DFTG. CHK. THANH LEQUANG	11/17/1999
ENGR. CHK. ASHOK PRABHU	11/17/1999

PROJECTION (INCH [MM])

National Semiconductor
2900 Semiconductor Dr., Santa Clara, CA 95052-8090

TAPE, COND., EMBOSSED, 8mm, MICRO SMD

SCALE	SIZE	DRAWING NUMBER	REV
25X	D	(SC)39-2258	E

FORMERLY: N/A SHEET 2 of 2

7.1 APPLICATION NOTE AN-1112

Micro SMD Wafer Level Chip Scale Package

National Semiconductor
Application Note 1112
September 1999

CONTENTS

Package Construction
- Key Attributes for Micro SMD 4 and 8 I/O Packages
- Smallest Footprint
- Micro SMD Handling

Surface Mount Technology (SMT) Assembly Considerations
- Printed Circuit Board Layout
- Stencil Printing Solder Paste
- Component Placement
- Solder Paste Reflow and Cleaning
- Micro SMD Rework
- Solder Joint Inspection

Micro SMD Package Qualification
- Preconditioning Stress
- Temperature Humidity Bias Test (THBT)
- Static Operating Life Test (SOPL)
- Temperature Cycling Test (TMCL)

Solder Joint Reliability
- Drop Test
- Three-Point Bend Test
- Vibration Test

Thermal Characterization
Frequently Asked Questions
References

Introduction to Micro SMD

Micro SMD is a wafer level chip scale/size package (CSP). A CSP is designed to have external package dimensions substantially equal to that of the silicon IC. Typical CSP configurations are broadly classified as one with an interposer between the silicon IC and the printed circuit board which acts as an intermediate level interconnect and another without any such interposer. Micro SMD belongs to the latter category. It is manufactured in wafer form and hence further categorized as a wafer level CSP. It extends the flip chip packaging technology to standard surface mount technology and has the following advantages:

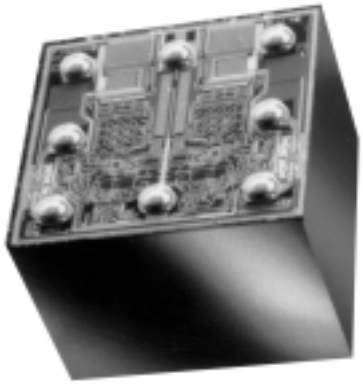
- No need for underfill material
- Smallest footprint per I/O that results in significant real estate savings on PCB
- Leverage standard surface mount assembly technology
- Cost effective manufacturing and assembly
- Matrix interconnect layout at 0.5 mm pitch

PACKAGE CONSTRUCTION

Construction of micro SMD illustrated in *Figure 1* and *Figure 2*. It has solder bumps located in matrix layout on the active side of silicon IC. Backside of silicon is protected with proprietary protective encapsulation. The micro SMD manufacturing process steps include wafer fabrication process, wafer repassivation, deposition of eutectic solder bumps, laser based inspection of bump characteristics, application of protective encapsulation coating, wafer sort testing, laser marking, singulation and shipping in tape and reel. The package is assembled on PCB using standard surface mount assembly techniques (SMT).

AN100926-19

FIGURE 1. Micro SMD 4 I/O



AN100926-20

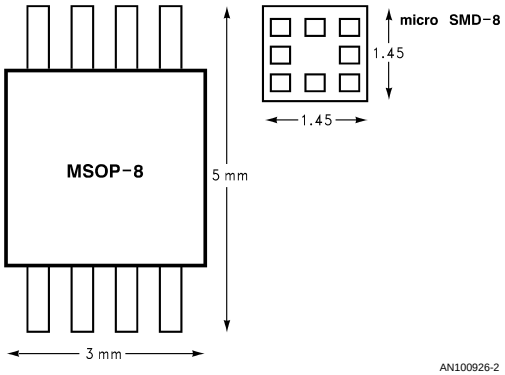
FIGURE 2. Micro SMD 8 I/O

KEY ATTRIBUTES FOR MICRO SMD 4 and 8 I/O PACKAGES

I/O Count	4	8
Pitch	0.5 mm	0.5 mm
Outline	2 x 2	3 x 3 peripheral
Weight	0.001 - 0.004 gm	0.003 - 0.007 gm
Bump Diameter	0.16 - 0.18 mm	0.16 - 0.18mm
Bump Height	0.11 - 0.14 mm	0.11 - 0.14 mm
Bump Coplanarity	±0.015 mm	±0.015 mm
Shipping Media	Tape & Reel	Tape & Reel
Desiccant Pack	Level 1	Level 1

SMALLEST FOOTPRINT

The micro SMD offers significant advantage in terms of footprints available in conventional packages. *Figure 3* compares a 8-lead MSOP - the smallest conventional surface mount 8 I/O package and the micro SMD 8 I/O. Replacing 8-lead MSOP with micro SMD 8 I/O results in 85% savings in real estate. The micro SMD footprint is at 0.5 mm matrix pitch and follows JEDEC Registered Outline M0-211 [1].



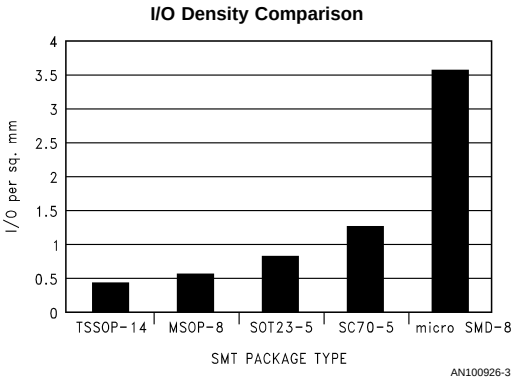


FIGURE 3. Footprint Comparison

MICRO SMD HANDLING

The micro SMD is shipped in standard polycarbonate conductive carrier tape with pressure sensitive adhesive (PSA) cover tape. The micro SMD can be ordered in quantities of 250 (7" reel) and 3000 (7" reel). *Figure 4* shows details of tape cavity design for micro SMD 8 I/O.

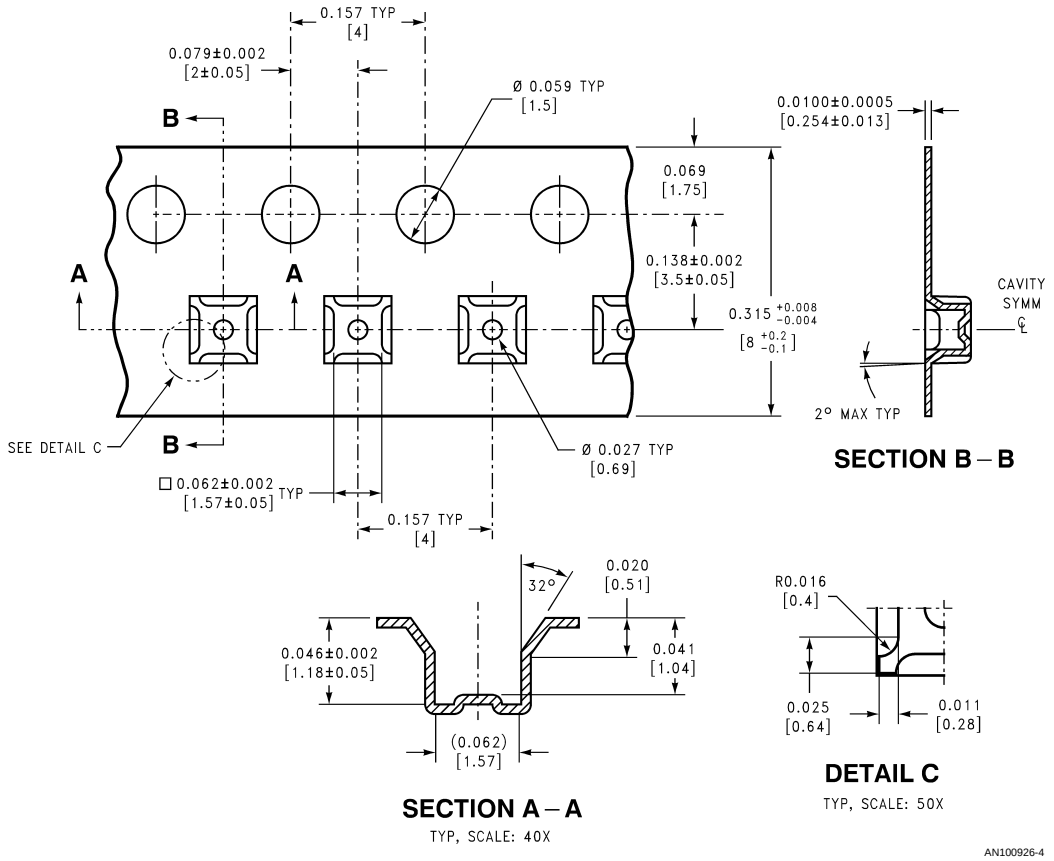


FIGURE 4. Micro SMD Tape & Reel Design

SURFACE MOUNT TECHNOLOGY (SMT) ASSEMBLY CONSIDERATIONS

The micro SMD surface mount assembly operations include printing solder paste on PCB, component placement, solder reflow and cleaning (depending on flux type). The most significant advantage of micro SMD is the ease of surface mount assembly. Contradictory to the conventional flip chip package, it can be placed on board using standard SMT pick and place equipment. Standard tape and reel shipping media facilitates package handling during assembly. Handling damage is minimal due to robust package and interconnects design. Following sections outline specific details of each SMT process step.

PRINTED CIRCUIT BOARD LAYOUT

Two types of land patterns are used for surface mount packages: (1) Solder mask defined (SMD) pads have solder mask opening smaller than metal pad; (2) Non-solder mask defined (NSMD) pads have metal pad smaller than the solder mask opening. *Figure 5* illustrates the two different types of pad geometry.

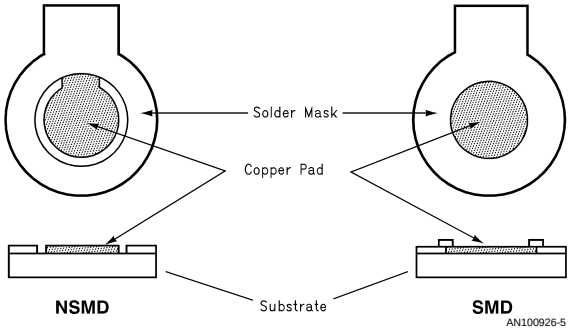


FIGURE 5. NSMD and SMD Pad Definition

NSMD definition is preferred due to tighter control on copper etch process compared to solder mask etch process. Moreover, SMD pad definition introduces stress concentration point near solder mask on the PCB side that may result in solder joint cracking under extreme fatigue conditions. Further a smaller size of copper pad in the case of NSMD definition facilitates escape routing on PCB, if necessary.

SMD pad size on package side is 0.150mm (6 mil). It is recommended to have 0.160 ±0.010 mm pad size on the PCB for optimum reliability. PCB layout assumes 0.100mm (4mil) wide trace and 0.5oz copper layer thickness. A copper pad smaller than 0.150mm may result in a reduced copper to FR4 substrate adhesion causing delamination. *Table 1* summarizes key feature dimensions.

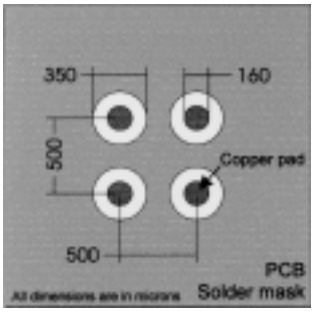
TABLE 1. SMD Pad Dimensions on PCB

Pad Definition	Copper Pad	Solder Mask Opening
NSMD	0.160 ±0.010 mm	0.350 ±0.025 mm
SMD	0.350 ±0.025 mm	0.160 ±0.010 mm

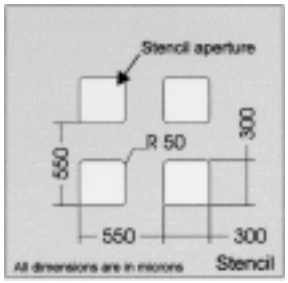
Majority of board level characterization was performed using PCB with organic solderability preservative coating (OSP) finish. A uniform coating thickness is key for high assembly yield. For an electroplated nickel-immersion gold finish, the gold thickness must be less than 0.5 micron to avoid solder joint embrittlement.

STENCIL PRINTING SOLDER PASTE

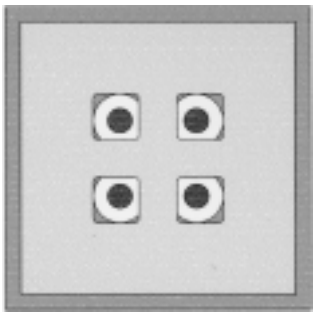
Solder paste deposition using stencil-printing process involves transferring solder paste through pre-defined apertures via application of pressure. Three typical stencil fabrication methods include chem-etch, laser cut and metal additive processes. Laser cut process followed by electro-polish process ensures tapering aperture walls that facilitate paste release. Apertures 0.275 mm X 0.275 mm or 0.300 mm X 0.300 mm square on a 0.125 mm thick laser cut stencil have consistently yielded acceptable results. *Figure 6* and *Figure 7* show sample stencil layouts for micro SMD 4 & 8 bump packages. It is recommended to offset stencil apertures from copper pad locations. This is to maximize separation between solder paste deposits in order to avoid solder bridging. A type 3 or finer solder paste is recommended. Depending on the type of solder paste used subsequent cleaning of flux may be needed. With recommended stencil parameters a vertical stand-off of 0.140 mm in the final assembly can be achieved.



Package Footprint

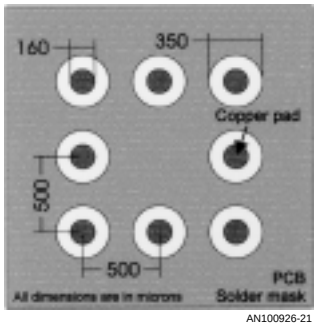


Stencil Layout



Stencil laid over PCB

FIGURE 6. Micro SMD 4 I/O PCB & Stencil Layout



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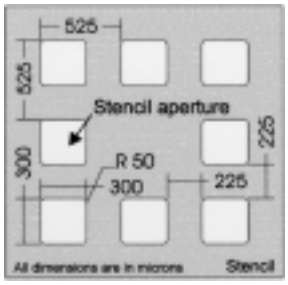
Package Footprint



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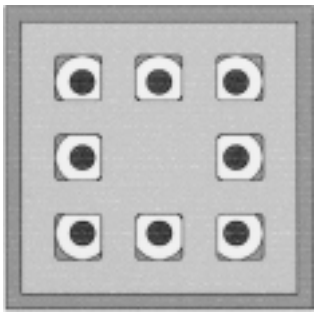
Stencil Layout



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Stencil laid over PCB

FIGURE 7. Micro SMD 8 I/O PCB & Stencil Layout

COMPONENT PLACEMENT

The micro SMD can be placed using standard pick and place equipment. The pick and place systems comprise of a vision system to recognize and position the component and a mechanical system to perform the pick and place operation. Two commonly used types of vision systems for bumped packages are (1) a vision system that locates package silhouette and (2) a vision system that locates individual bumps on the interconnect pattern. Latter type renders more accurate placement but tends to be more expensive and time consuming. Both methods are acceptable for micro SMD because during solder reflow the component aligns due to self-centering feature of the micro SMD solder joint. *Figure 8* illustrates the phenomenon of self-alignment when parts are intentionally placed off the actual location. Results indicate that for the prescribed stencil design (which overprints solder paste on the pad), the micro SMD is forgiving to off placements up to ±0.225 mm in X and Y directions. In the absence of solder paste on PCB (flip chip assembly), it may be off placed to an extent such that the solder bump is in contact with edge of copper pad on the PCB. In the figure it is referred to as process window for the flip chip attachment process. Published results are based on placement using *Amistar PlacePro 5800*.

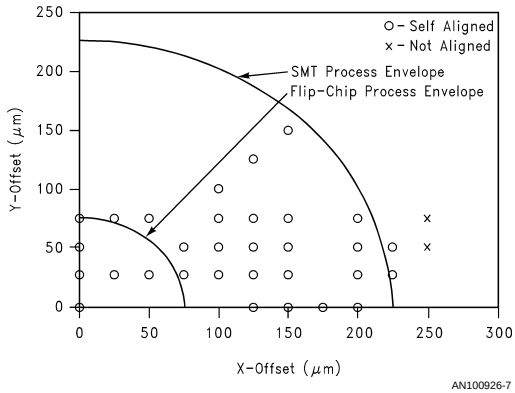

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FIGURE 8. Micro SMD Self Alignment Characteristics

SOLDER PASTE REFLOW AND CLEANING

The micro SMD may be assembled using standard SMT reflow process. Similar to any other package, thermal profile at specific board locations must be determined. Nitrogen purge is recommended during solder reflow operation. *Figure 9* illustrates a typical reflow profile. The micro SMD is qualified for up to three reflow cycles (235° C peak) per J-STD-020[2]. During reflow, eutectic solder bumps and the eutectic solder paste on PCB melt in presence of flux to form a cohesive shiny solder joint (*Figures 10, 11*). Depending on type of flux used the assembly may be cleaned.

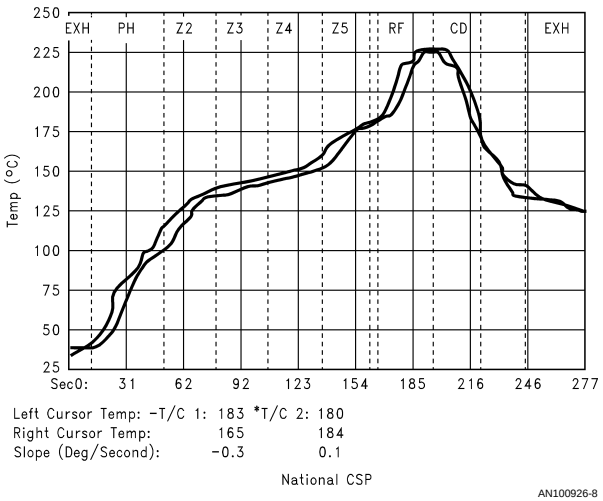


FIGURE 9. Micro SMD Reflow Profile

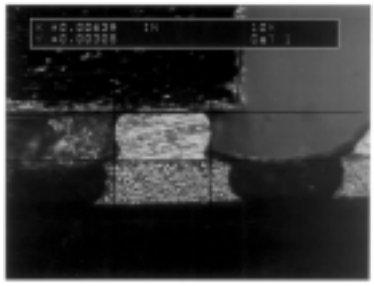


FIGURE 10. Micro SMD Solder Joint on SMD Pad

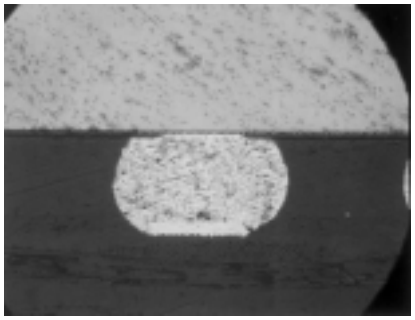


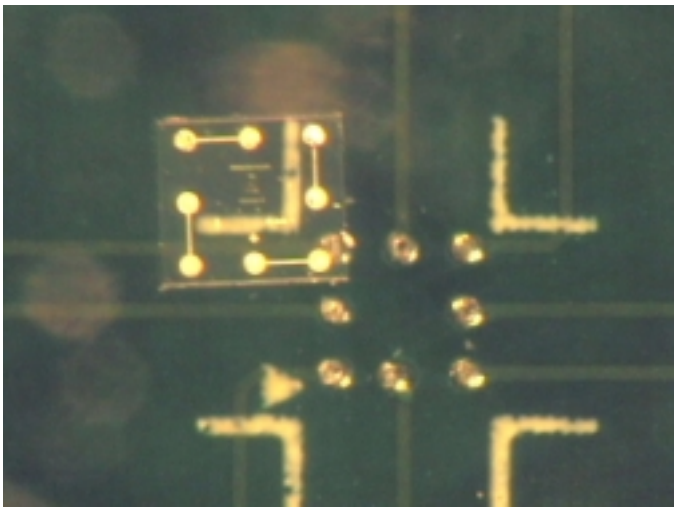
FIGURE 11. Micro SMD Solder Joint on NSMD Pad

MICRO SMD REWORK

Reworking the micro SMD part involves following the same process for reworking a typical BGA or CSP part. In order to maintain component and PC board integrity, and to obtain reliable solder connections, the rework process should duplicate the original reflow profile. For the micro SMD part, a rework system should include a localized convection heating oven with profiling capability, a bottom-side preheater, and a part placer with image overlay for alignment. The following rework process was developed using OK International's BGA-3000 Rework System [3] and can be used as a guide for developing a specific rework process.

The rework process beigns with removing the part. After establishing a rework reflow profile similar to the original reflow profile, the part can easily be removed by heating it with a convection nozzle and bottom-side preheater. Once the sol-

der has reached the liquidus point, it can be lifted off using tweezers. After the part is removed, the site is prepared by tinning the pads with a temperature controlled soldering iron. A gel flux is then applied to the pads using a small paint brush or swab. The replacement part can be picked with a vacuum needle pick-up tip. Using a prism for image overlay, the part is then aligned over the rework site and the component is placed onto the pasted site. Finally, using the convection nozzle and bottom-side preheater, reflow the part using a profile which matches the original reflow profile. For National's process, a three stage hot air convection profile at 8 litres per minute flow rate was used.



AN100926-18

FIGURE 12. Image overlay of 8 I/O micro SMD part

SOLDER JOINT INSPECTION

After surface mount assembly transmission X-ray can be used for sample monitoring of solder attachment process to identify defects such as bridging, shorts, opens and voids. *Figure 13* shows a typical X-ray photograph after assembly.

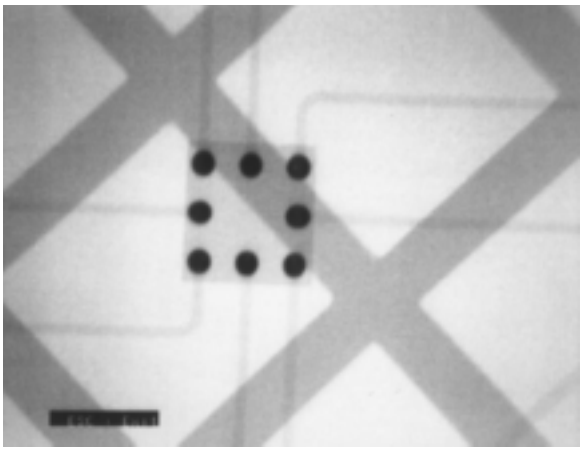


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FIGURE 13. X-Ray Inspection of micro SMD Solder Joints

MICRO SMD PACKAGE QUALIFICATION

The micro SMD package qualification plan included industry standard reliability test such as temperature cycle test (TMCL), temperature humidity bias test (THBT), biased operational life test (SOPL), and preconditioning stress (Precon). *Table 2* summarizes the qualification results.

PRECONDITIONING STRESS

Preconditioning is performed to simulate product shipping, storage and surface mount assembly operations. Micro SMD packages are subjected to the following preconditioning sequence per J-STD-020 “Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices”. [2]

1. temperature cycle – 5 cycles at −40˚C to 60˚C,
2. bake – 16 hours at 125˚C,
3. level 1 moisture soak – at 85˚C/85%RH for 168 hours,
4. 3 IR reflow passes (235˚C peak),
5. flux immersion and clean.

Packaging are subjected to preconditioning prior to THBT and TMCL testing.

TEMPERATURE HUMIDITY BIAS TEST (THBT)

THBT is designed to precipitate reliability failures of nonhermetic parts under humid environments. Typical failure mechanisms include galvanic corrosion of metal layers and threshold shifts due to moisture and contamination.

STATIC OPERATING LIFE TEST (SOPL)

SOPL accelerates oxide breakdown failures. Test is conducted at 150˚C under electrical bias.

TEMPERATURE CYCLING TEST (TMCL)

TMCL is designed to test package integrity and overall ruggedness. It tests mechanical integrity of a package when subjected to temperature cycling under conditions of −65˚C to 150˚C.

TABLE 2. Package Reliability Results

Reliability Test	Test Conditions	Test Point	Test Results		
			Lot A	Lot B	Lot C
THBT	85˚C/85% RH	1000 hours	0/77	0/77	0/77
SOPL	150˚C	500 hours	0/77	0/77	0/77
TMCL	−65˚C to 150˚C	500 cycles	0/80	0/80	0/80

SOLDER JOINT RELIABILITY

The micro SMD extends flip chip technology to cost-effective surface mount assembly. With the absence of compliant leads and underfill, it is necessary to assess solder joint reliability. Following IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments [4], daisy chain micro SMD 8 I/O parts mounted onto 4-layer FR4 PCB (0.062” thick) were subjected to temperature cycling at 0˚C to 100˚C, 1 cycle/hr. For more demanding applications such as automotive and telecom equipment further testing was conducted at −40˚C to 125˚C, 1 cycle/hr. The actual temperature profiles measured at several PCB locations are shown in *Figures 14, 15*. *Table 3* outlines reliability data for the two test conditions. To assess reliability of a reworked part, units with flip chip assembly process (without solder paste printing) were tested. Following optimum assembly conditions described here, micro SMD 8 I/O can pass 2300 cycles under 0˚C to 100˚C, 1 cycle/hr and 800 cycles under −40˚C to 125˚C, 1 cycle/hr without any failure (*Figure 16*).

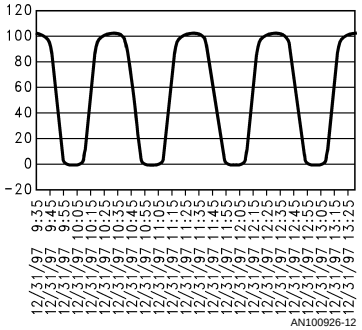

FIGURE 14. 0˚C to 100˚C, 1 cycle/hr Temperature Cycling Profile

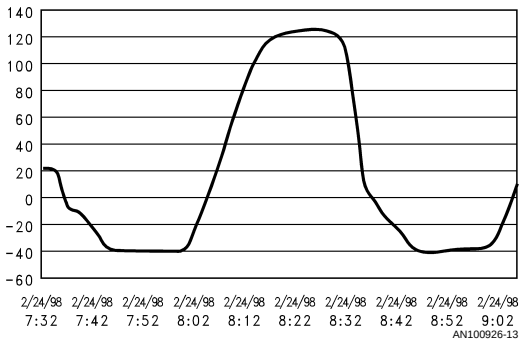

FIGURE 15. • 40ûC to 125ûC, 1 cycle/hr Temperature Cycling Profile

TABLE 3. Micro SMD Solder Joint Reliability Test Matrix

Micro-SMD Assembly	Test Condition	0 cycles	500 cycles	800 cycles	1000 cycles	2300 cycles
8 I/O SMT	0˚C to 100˚C	0/62	0/62	0/62	0/62	0/62
8 I/O Flip Chip	0˚C to 100˚C	0/64	0/64	0/64	0/64	0/64
8 I/O SMT	−40˚C to 125˚C	0/61	0/61	0/61	6/61	N/A
8 I/O Flip Chip	−40˚C to 125˚C	0/32	0/32	0/32	10/32	N/A

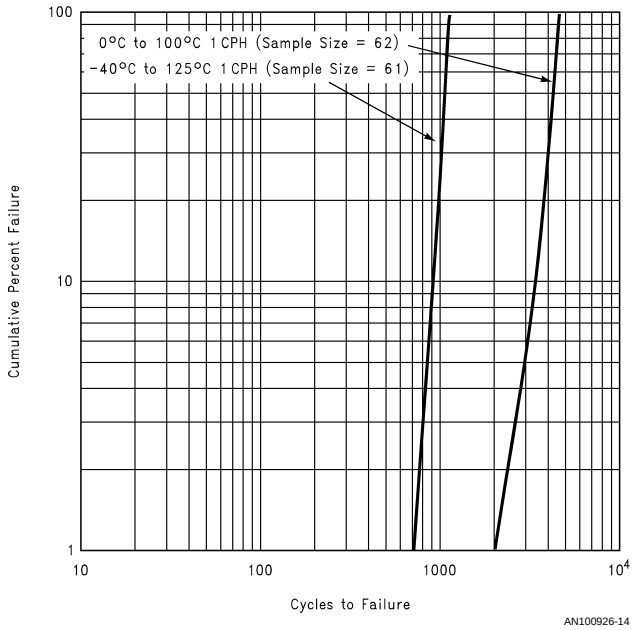

FIGURE 16. Micro SMD Solder Joint Failure Distribution

DROP TEST

Drop Test was performed on micro SMD 8 I/O package following the PC Card Environmental Test standard. Micro SMD 8 I/O assemblies (mounted on PCB) were dropped two (2) times in three (3) mutually exclusive axes from a height of 750 mm onto a noncushioning, vinyl tile surface. 20/20 samples passed the test.

THREE-POINT BEND TEST

The setup for three-point bend test of micro SMD package assemblies included a test board with a span of 100 mm. A deflection was applied at the center of the board at a rate of 9.45mm/min. *Figure 17* shows the time-deflection and time-resistance curves of the test board with the micro SMD 8 I/O. No solder joint failure was observed even with the deflection

greater than 25 mm. For this size of board, this magnitude of deflection is beyond most manufacturing, shipping, handling and operating conditions. Four boards with one unit per board were tested.

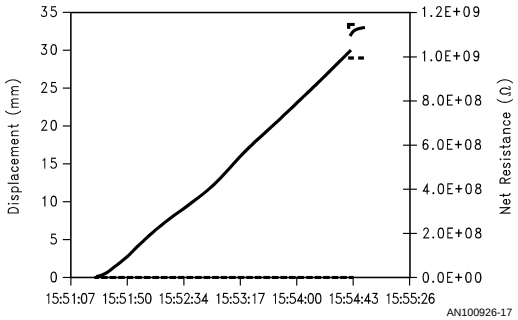

FIGURE 17. Board Deflection and Net Resistance

VIBRATION TEST

Sample size for vibration testing was 16 micro SMD 8 I/O parts mounted on PCB. Both random and sinusoidal excitations were used. Natural frequencies of sample boards were determined using the vibration shaker to sweep at very small magnitudes for a wide range of frequencies. The natural frequencies were found to range from 270 Hz to 320 Hz. The excitation of the shaker was set to perform a sinusoidal excitation with a frequency sweep between 260 Hz to 320 Hz to obtain 20G to 40G responses at the board. micro SMD 8 I/O survived 1 hour of sinusoidal vibration at 20G followed by 3 hours of sinusoidal vibration at 40G without any failure. Additionally micro SMD 8 I/O also passed 3 hours of 2G RMS random vibration with frequencies ranging from 20 Hz to 2000 Hz.

THERMAL CHARACTERIZATION

Thermal performance of micro SMD 4 and 8 I/O packages was assessed using a low effective thermal conductivity test board fabricated per EIA/JESD51-3. *Table 4* summarises θ_{JA} for each package at zero air flow without any thermal enhancement. Enhancement guidelines for improved thermal performance are listed in specific product data sheet.

TABLE 4. θ_{JA} for micro SMD PACKAGES

Micro SMD Package Type	θ_{JA} (°C/W)
4 I/O	340 ± 20
8 I/O	220 ± 20

FREQUENTLY ASKED QUESTIONS

Q1:	Nominal bump/ball diameter	A1:	0.170 mm
Q2:	Pin 1 location	A2:	Laser marked on top side
Q3:	Solder pad dimension & definition	A3:	NSMD 0.160 mm ± 0.01 mm round
Q4:	Solder mask opening	A4:	0.350 mm round
Q5:	Stencil specifications	A5:	0.125 mm thick, laser cut + eletropolished, 0.275 mm square or 0.300 mm square aperture
Q6:	Solder paste specification	A6:	Type 3 paste
Q7:	Flux specification	A7:	Water soluble or no-clean
Q8:	Compatibility with 3 IR reflows	A8:	Can withstand two 235°C peak reflow followed by one 260°C peak reflow (30 sec max. dwell at peak)
Q9:	Shipping media	A9:	Tape & Reel
Q10:	Moisture sensitivity level	A10:	Level 1

REFERENCES

1. JEDEC Registered Outline M0-211-FXBGA - Die Sized Ball Grid Array
2. J-STD-020, “Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices”, October 1996.
3. “A Successful Rework Process for Chip-Scale Packages”, Paul Wood, OK International, Chip Scale Review, Vol. 2, No. 4, 1998, pp. 41–45.
4. IPC-5M-785, “Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments”, November 1992.

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