MSP430G2x52, MSP430G2x32, MSP430G2x12, MSP430G2x02 Device Erratasheet

1 Current Version

See Appendix A for prior silicon revisions.

✓ The checkmark means that the issue is present in that revision.

Device	Rev:	BCL12	BCL14	CPU4	SYS15	TA12	TA16	TA22	USI4	USI5	XOSC5
MSP430G2102	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2112	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2132	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2152	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2202	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2212	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2232	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2252	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2302	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2312	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2332	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2352	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2402	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2412	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2432	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2452	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

2 Package Markings

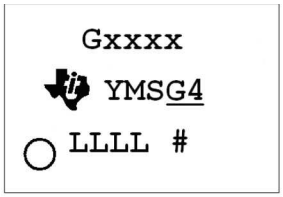
N20

PDIP (N), 20 Pin

YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision

PW14

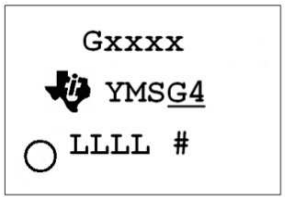
TSSOP (PW), 14 Pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

PW20

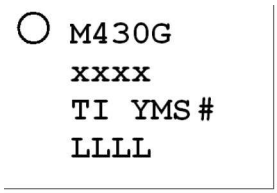
TSSOP (PW), 20 Pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RSA16

QFN (RSA), 16 Pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

3 Detailed Bug Description

BCL12 *Basic Clock Module*

Function Switching RSEL can cause DCO dead time

Description After switching RSELx bits (located in register BCSCTL1) from a value of >13 to a value of <12 OR from a value of <12 to a value of >13, the resulting clock delivered by the DCO can stop before the new clock frequency is applied. This dead time is approximately 20 µs. In some instances, the DCO may completely stop, requiring a power cycle.

Workaround

- When switching RSEL from >13 to <12, use an intermediate frequency step. The intermediate RSEL value should be 13.

CURRENT RSEL	TARGET RSEL	RECOMMENDED TRANSITION SEQUENCE
15	14	Switch directly to target RSEL
14 or 15	13	Switch directly to target RSEL
14 or 15	0 to 12	Switch to 13 first, and then to target RSEL (two step sequence)
0 to 13	0 to 12	Switch directly to target RSEL

- When switching RSEL from <12 to >13, ensure that the maximum system frequency is not exceeded during the transition. This can be achieved by clearing the DCO bits first (DCOCTL control register, bits 7–5), then increasing the RSEL value, and finally applying the target frequency DCO bit values. For more details, see the examples in the "TLV Structure" chapter in the *MSP430F2xx Family User's Guide* (SLAU144).

BCL14 *Basic Clock Module*

Function Oscillator fault forced in bypass mode when P2SEL.7 bit is not set

Description When the LFXT1 oscillator is used in bypass mode and P2SEL.7 is not set, the oscillator fault flag (OFIFG) is forced to set and cannot be cleared. Due to the failsafe logic, LFXT1 cannot be used as MCLK in this case. The bug affects only the behavior of the oscillator fault; the clocking itself works properly.

Workaround Set both P2SEL.6 and P2SEL.7 if the application requires correct function of the oscillator fault flag (for example, for MCLK failsafe logic).

NOTE: Setting the P2SEL.7 bit disables the GPIO functionality and enables the input Schmitt trigger of the pin. P2.7 should be tied to a fixed voltage level (VCC or GND) to prevent cross current.

CPU4 *CPU Module*

Function PUSH #4, PUSH #8

Description The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, –1) can be used. The number of clock cycles is different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1-word instruction

PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2-word instruction

Workaround Workaround implemented in assembler. No fix planned.

SYS15 *System Module*

Function LPM3 and LPM4 currents exceed specified limits

Description LPM3 and LPM4 currents may exceed specified limits if the SMCLK source is switched from DCO to VLO or LFXT1 just before the instruction to enter LPM3 or LPM4 mode.

Workaround After clock switching, a delay of at least four new clock cycles (VLO or LFXT1) must be implemented to complete the clock synchronization before going into LPM3 or LPM4.

TA12 *Timer_A Module*

Function Interrupt is lost (slow ACLK)

Description Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx).

Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt is lost.

Workaround Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterward.

TA16 *Timer_A Module*

Function First increment of TAR erroneous when IDx > 00

Description The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround None

TA22 *Timer_A Module*

Function Timer_A register modification after watchdog timer PUC

Description Unwanted modification of the Timer_A registers TACTL and TAIV can occur when a PUC is generated by the watchdog timer (WDT) in watchdog mode and any Timer_A counter register TACCRx is incremented/decremented (Timer_A does not need to be running).

Workaround Initialize TACTL register after the reset occurs using a MOV instruction (BIS or BIC may not fully initialize the register). TAIV is automatically cleared following this initialization.

Example

```
MOV.W #VAL, &TACTL
```

Where VAL = 0, if Timer is not used in application; otherwise, user defined per desired function.

USI4 — *USI Module*

Function I^2C slave mode can generate a glitch on SCL

Description Applies to USI I^2C slave operation at slow communication rates (less than 20 kbps). During I^2C bus active operation, if USICNT is written while SCL is high, the USI I^2C module generates a glitch on SCL that can corrupt the I^2C bus sequence.

Workaround Verify that SCL is low prior to updating the USICNT register.

USI5 — *USI Module*

Function SPI master generates one additional clock after module reset

Description Initializing the USI in SPI MASTER mode with the USICKPH bit set generates one additional clock pulse than defined by the value in the USICNTx bits on the SCLK pin during the first data transfer after module reset. For example, if the USICNTx bits hold the value eight, nine clock pulses are generated on the SCLK pin for the first transfer only.

Workaround Load USICNTx with a count of N – 1 bytes (where N is the required number of bytes) for the first transfer only.

XOSC5 — *LFXT1 Module*

Function LF crystal failures may not be properly detected by the oscillator fault circuitry

Description The oscillator fault error detection of the LFXT1 oscillator in low-frequency mode (XTS = 0) may not work reliably, causing a failing crystal to go undetected by the CPU; that is, OFIFG is not set.

Workaround None

Appendix A Prior Revisions

None

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