Rail-to-Rail, Very Fast, 2.5 V to 5.5 V, Single-Supply TTL/CMOS Comparators

Preliminary Technical Data

ADCMP600/ADCMP601/ADCMP602

FEATURES

10 mV sensitivity rail to rail at V_{CC} = 2.5 V
Input common-mode voltage from −0.2 V to V_{CC} + 0.2 V
Low glitch CMOS-/TTL-compatible output stage
3 ns propagation delay
15 mW at 3.3 V
Shutdown pin
Single-pin control for programmable hysteresis and latch
Power supply rejection > 60 dB
Improved replacement for MAX999
−40°C to +125°C operation

APPLICATIONS

High speed instrumentation
Clock and data signal restoration
Logic level shifting or translation
Pulse spectroscopy
High speed line receivers
Threshold detection
Peak and zero-crossing detectors
High speed trigger circuitry
Pulse-width modulators
Current-/voltage-controlled oscillators
Automatic test equipment (ATE)

FUNCTIONAL BLOCK DIAGRAM

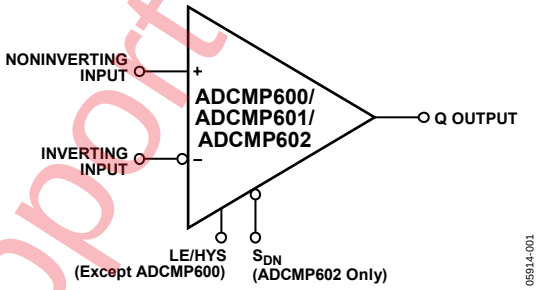

Figure 1.

GENERAL DESCRIPTION

The ADCMP600, ADCMP601, and ADCMP602 are very fast comparators fabricated on Analog Devices' proprietary XFCB2 process. These comparators are exceptionally versatile and easy to use. Features include an input range from V_{EE} − 0.5 V to V_{CC} + 0.5 V, low noise TTL-/CMOS-compatible output drivers, and latch inputs with adjustable hysteresis and/or shutdown inputs.

The devices offer 3 ns propagation delay with 5 mV overdrive on 4 mA typical supply current.

A flexible power supply scheme allows the devices to operate with a single +2.5 V positive supply and a −0.5 V to +3.0 V input signal range up to a +5.5 V positive supply with a −0.5 V to +6 V input signal range. Split input/output supplies with no sequencing restrictions on the ADCMP602 support a wide input signal range while still allowing independent output swing control and power savings.

The TTL-/CMOS-compatible output stage is designed to drive up to 5 pF with full timing specs and to degrade in a graceful and linear fashion as additional capacitance is added. The comparator input stage offers robust protection against large input overdrive, and the outputs do not phase reverse when the valid input signal range is exceeded. High speed latch and programmable hysteresis features are also provided with a unique single-pin control option.

The ADCMP600 is available in both 5-lead SC70 and SOT-23 packages, the ADCMP601 is available in a 6-lead SC70 package, and the ADCMP602 is available in 8-lead MSOP and LSCFP packages.

Rev. PrA

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REVISION HISTORY

3/06—Revision PrA: Preliminary Version

ELECTRICAL CHARACTERISTICS

V_{CCI} = V_{CCO} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
Voltage Range	V_P, V_N	V_{CC} = 2.5 V to 5.5 V	−0.5		V_{CC} + 0.5 V	V
Common-Mode Range		V_{CC} = 2.5 V to 5.5 V	−0.2		V_{CC} + 0.2 V	V
Differential Voltage		V_{CC} = 2.5 V to 5.5 V			V_{CC}	V
Offset Voltage	V_{OS}		−5.0		+5.0	mV
Bias Current	I_P, I_N		−5.0	±2.0	+5.0	µA
Offset Current			2.0		2.0	µA
Capacitance	C_P, C_N			TBD		pF
Resistance, Differential Mode		0.1 V to V_{CC}		100		kΩ
Resistance, Common Mode		−0.5 V to V_{CC} + 0.5 V		100		kΩ
Active Gain	A_V			85		dB
Common-Mode Rejection	CMRR	V_{CCI} = 2.5 V, V_{CCO} = 2.5 V, V_{CM} = −0.2 V to +2.7 V		50		dB
		V_{CCI} = 5.5 V, V_{CCO} = 3.3 V, V_{CM} = −0.2 V to +6.0 V		60		dB
Hysteresis ADCMP600			1.5	2	2.5	mV
Hysteresis ADCMP601/ADCMP602		R_{HYS} = ∞		0.1		mV
LATCH ENABLE PIN CHARACTERISTICS (ADCMP601/ADCMP602 Only)						
V_{IH}		Hysteresis is shut off	2.0		V_{CC}	V
V_{IL}		Latch mode guaranteed	−0.2	+0.4	+0.8	V
I_{IH}		V_{IH} = V_{CC}			0.2	mA
I_{OL}		V_{IL} = 0.4 V			−0.2	mA
HYSTERESIS MODE AND TIMING						
Hysteresis Mode Bias Voltage		Current sink 0 µA	1.145	1.25	1.35	V
Minimum Resistor Value		Hysteresis = 16 mV	150			kΩ
Latch Setup Time	t_S	V_{OD} = 100 mV		2		ns
Latch Hold Time	t_H	V_{OD} = 100 mV		5		ns
Latch-to-Output Delay	t_{PLOH}, t_{PLOL}	V_{OD} = 100 mV		3		ns
Latch Minimum Pulse Width	t_{PL}	V_{OD} = 100 mV		3		ns
SHUTDOWN PIN CHARACTERISTICS (ADCMP602 Only)						
V_{IH}		Comparator is operating	2.0		V_{CCO}	V
V_{IL}		Shutdown guaranteed	−0.2	+0.4	+0.6	V
I_{IH}		V_{IH} = V_{CC}			0.3	mA
I_{OL}		V_{IL} = 0 V			−0.3	mA
Sleep Time	t_{SD}	I_{CC} < 500 µA		60		ns
Wake-Up Time	t_H	V_{OD} = 10 mV, output valid		40		ns
DC OUTPUT CHARACTERISTICS		V_{CCO} = 2.5 V to 6 V				
Output Voltage High Level	V_{OH}	I_{OH} = 12 mA, V_{CCO} = 2.5 V	V_{CC} − 0.4			V
Output Voltage Low Level	V_{OL}	I_{OL} = 12 mA, V_{CCO} = 2.5 V			0.4	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AC PERFORMANCE						
Propagation Delay	t_{PD}	V_{CCO} = 2.5 V to 5.5 V V_{OD} = 5 mV		3		ns
		V_{CCO} = 2.5 V to 5.5 V V_{OD} = 200 mV		2		ns
Propagation Delay Skew—Rising to Falling Transition		V_{OD} = 50 mV		200		ps
Overdrive Dispersion		10 mV < V_{OD} < 2.5 V		TBD		ps
Slew Rate Dispersion		0.05 V/ns to 2.5 V/ns		TBD		ps
Pulse-Width Dispersion		3 ns to 30 ns		TBD		ps
10% to 90% Duty Cycle Dispersion		V_{OD} = 5 V, 1 V/ns, V_{CM} = 2.5 V		TBD		ps
Common-Mode Dispersion		0 < V_{CM} < V_{CC}		TBD		ps
Toggle Rate		>50% output swing, C_{LOAD} = 5 pF, V_{CCO} = 5 V		TBD		Mbps
Deterministic Jitter TTL/CMOS Outputs	DJ	V_{OD} = 200 mV, 5 V/ns, PRBS^{31} − 1 NRZ, 0.25 Gbps		TBD		ns
RMS Random Jitter	RJ	V_{OD} = 200 mV, 5 V/ns, PRBS^{31} − 1 NRZ, 0.525 Gbps		TBD		ps
Minimum Pulse Width	PW_{MIN}	$\Delta t_{PD}/\Delta PW$ < 50 ps		3		ns
Rise Time	t_R	10% to 90%, C_{LOAD} = 5 pF, V_{CCO} = 5 V		2.0		ns
Fall Time	t_F	10% to 90%, C_{LOAD} = 5 pF, V_{CCO} = 5 V		2.0		ns
POWER SUPPLY						
Input Supply Voltage Range	V_{CCI}		2.5		5.5	V
Output Supply Voltage Range	V_{CCO}		2.5		5.5	V
Positive Supply Differential (ADCMP602 Only)	V_{CCI} − V_{CCO}	Operating	−3.0		+3.0	V
Positive Supply Differential (ADCMP602 Only)	V_{CCI} − V_{CCO}	Nonoperating	−5.5		+5.5	V
Positive Supply Current	I_{VCC}	V_{CC} = 2.5 V		3		mA
Input Section Supply Current (ADCMP602 Only)	I_{VCCI}	V_{CCI} = 2.5 V to 5 V		0.8		mA
Output Section Supply Current (ADCMP602 Only)	I_{VCCO}	V_{CCI} = 2.5 V to 5.5 V		2		mA
Power Dissipation	P_D	V_{CC} = 2.5 V		9		mW
	P_D	V_{CC} = 5.5 V		20		mW
Power Supply Rejection	PSRR	V_{CCI} = 2.5 V to 5 V		−50		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages	
Input Supply Voltage (V_{CCI} to GND)	−0.5 V to +6.0 V
Output Supply Voltage (V_{CCO} to GND)	−0.5 V to +6.0 V
Positive Supply Differential ($V_{CCI} – V_{CCO}$)	−6.0 V to +6.0 V
Input Voltages	
Input Voltage	−0.5 V to V_{CCI} + 0.5 V
Differential Input Voltage	±(V_{CCI} + 0.5 V)
Maximum Input/Output Current	±50 mA
Shutdown Control Pin	
Applied Voltage (HYS to GND)	−0.5 V to V_{CCO} + 0.5 V
Maximum Input/Output Current	±50 mA
Latch/Hysteresis Control Pin	
Applied Voltage (HYS to GND)	−0.5 V to V_{CCO} + 0.5 V
Maximum Input/Output Current	±50 mA
Output Current	±50 mA
Temperature	
Operating Temperature, Ambient	−40°C to +125°C
Operating Temperature, Junction	150°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

J_A is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	Unit
ADCMP600 SC70 5-lead	426	°C/W
ADCMP600 SOT-23 5-lead	302	°C/W
ADCMP601 SC70 6-lead	426	°C/W
ADCMP602 MSOP 5-lead	130	°C/W

[1] Measurement in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

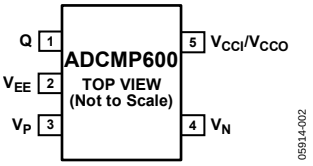

Figure 2. ADCMP600 Pin Configuration

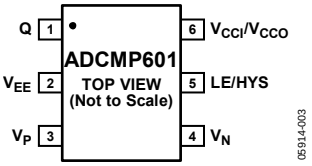

Figure 3. ADCMP601 Pin Configuration

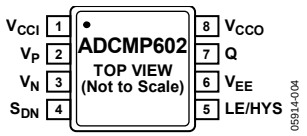

Figure 4. ADCMP602 Pin Configuration

Table 4. ADCMP600 (SOT-23-5 and SC70-5) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N.
2	V_{EE}	Negative Supply Voltage.
3	V_P	Noninverting Analog Input.
4	V_N	Inverting Analog Input.
5	V_{CCI}/V_{CCO}	Input Section Supply/Output Section Supply. Shared pin.

Table 5. ADCMP601 (SC70-6) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, provided that the comparator is in compare mode.
2	V_{EE}	Negative Supply Voltage.
3	V_P	Noninverting Analog Input.
4	V_N	Inverting Analog Input.
5	LE/HYS	Latch/Hysteresis Control. Bias with resistor or current for hysteresis adjustment; drive low to latch.
6	V_{CCI}/V_{CCO}	Input Section Supply/Output Section Supply. Shared pin.

Table 6. ADCMP602 (MSOP-8) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{CCI}	Input Section Supply.
2	V_P	Noninverting Analog Input.
3	V_N	Inverting Analog Input.
4	S_{DN}	Shutdown. Drive this pin low to shut down the device.
5	LE/HYS	Latch/Hysteresis Control. Bias with resistor or current for hysteresis adjustment; drive low to latch.
6	V_{EE}	Negative Supply Voltage.
7	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, provided that the comparator is in compare mode.
8	V_{CCO}	Output Section Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CCI} = V_{CCO} = 2.5 V, T_A = 25°C, unless otherwise noted.

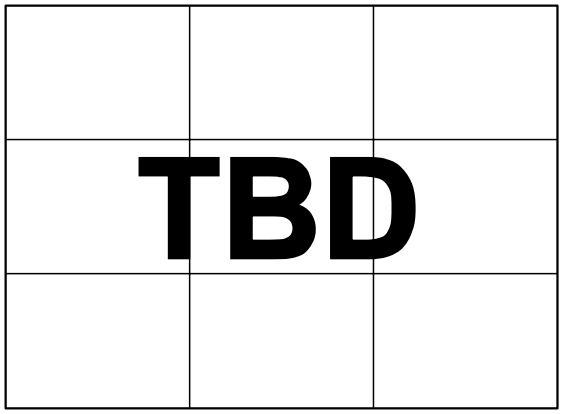

Figure 5. Propagation Delay vs. Input Overdrive

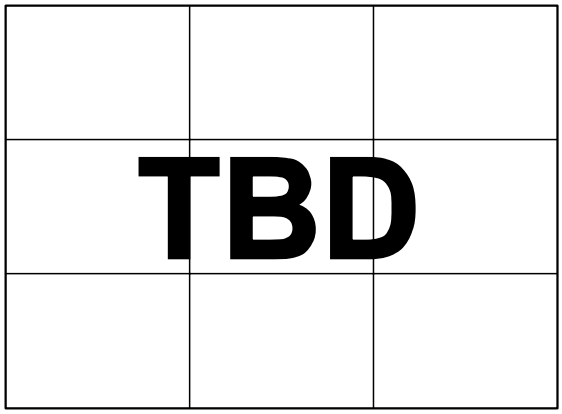

Figure 8. Hysteresis vs. V_{CC}

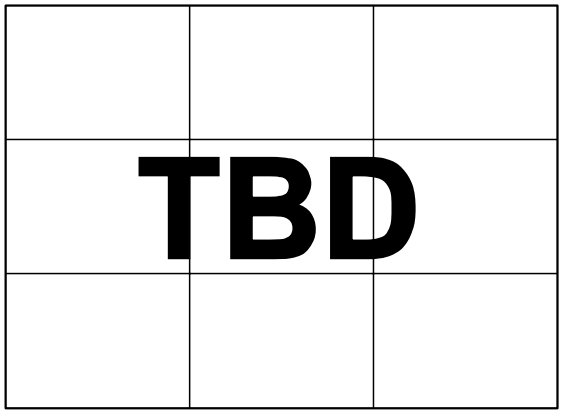

Figure 6. Propagation Delay vs. Input Common Mode

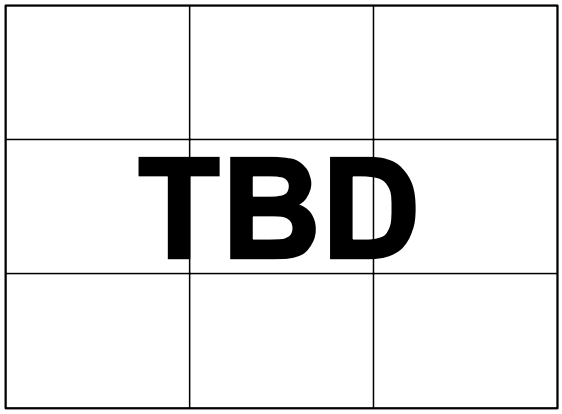

Figure 9. Hysteresis vs. R_{HYS} Control Resistor

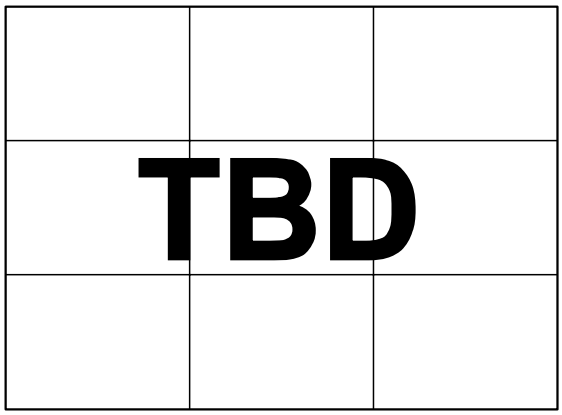

Figure 7. Propagation Delay vs. Temperature

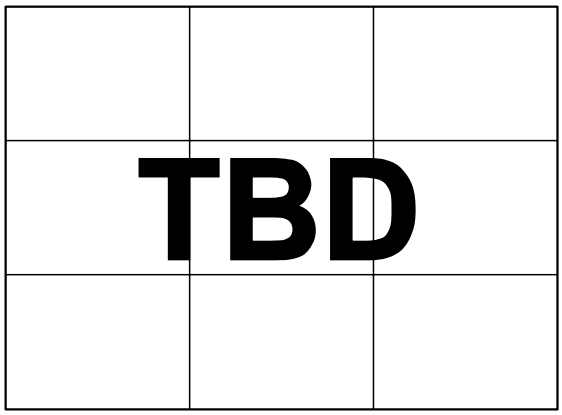

Figure 10. Input Bias Current vs. Input Common Mode

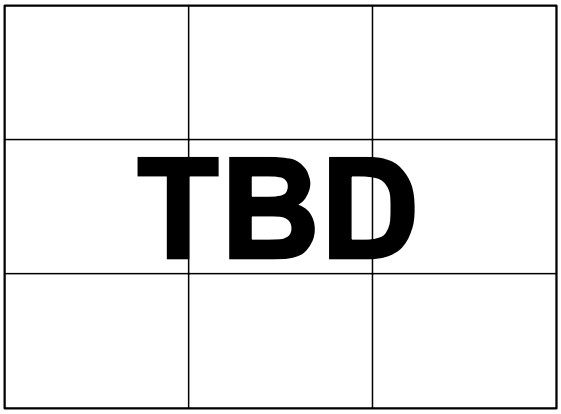

Figure 11. Input Bias Current vs. Temperature

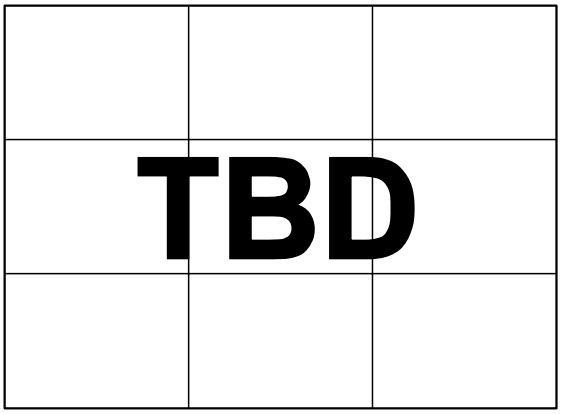

Figure 13. Latch/Hysteresis Control Pin I/V Characteristics

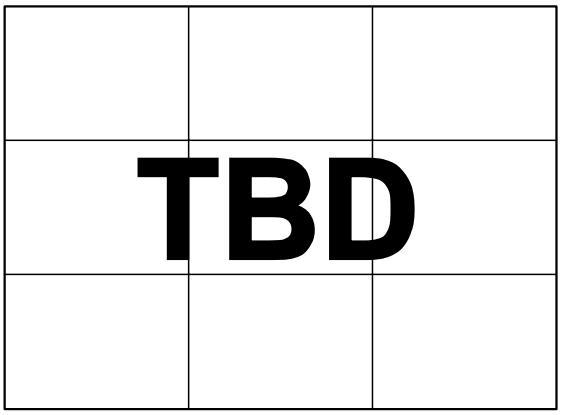

Figure 12. Input Offset Voltage vs. Temperature

APPLICATION INFORMATION

POWER/GROUND LAYOUT AND BYPASSING

The ADCMP600/ADCMP601/ADCMP602 comparators are very high speed devices. Despite the low noise output stage, it is essential to use proper high speed design techniques to achieve the specified performance. Because comparators are uncompensated amplifiers, feedback in any phase relationship is likely to cause oscillations or undesired hysteresis. Of critical importance is the use of low impedance supply planes, particularly the output supply plane (V_{CCO}) and the ground plane (GND). Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. Multiple high quality 0.01 µF bypass capacitors should be placed as close as possible to each of the V_{CCI} and V_{CCO} supply pins and should be connected to the GND plane with redundant vias. At least one of these should be placed to provide a physically short return path for output currents flowing back from ground to the V_{CC} pin. High frequency bypass capacitors should be carefully selected for minimum inductance and ESR. Parasitic layout inductance should also be strictly controlled to maximize the effectiveness of the bypass at high frequencies.

If the package allows and the input and output supplies have been connected separately such that $V_{CCI} \neq V_{CCO}$, care should be taken to bypass each of these supplies separately to the GND plane. A bypass capacitor should never be connected between them. It is recommended that the GND plane separate the V_{CCI} and V_{CCO} planes when the circuit board layout is designed to minimize coupling between the two supplies and to take advantage of the additional bypass capacitance from each respective supply to the ground plane. This enhances the performance when split input/output supplies are used. If the input and output supplies are connected together for single-supply operation such that $V_{CCI} = V_{CCO}$, coupling between the two supplies is unavoidable; however, careful board placement can help keep output return currents away from the inputs.

TTL-/CMOS-COMPATIBLE OUTPUT STAGE

Specified propagation delay performance can be achieved only by keeping the capacitive load at or below the specified minimums. The outputs of the ADCMP600/ADCMP601/ADCMP602 are designed to directly drive one Schottky TTL or three low power Schottky TTL loads or equivalent. For large fan outputs, buses, or transmission lines, an appropriate buffer should be used to maintain the comparator's excellent speed and stability.

With the rated 5 pF load capacitance applied, more than half of the total device propagation delay is output stage slew time, even at 2.5 V V_{CC}. Because of this, the total prop delay decreases as V_{CCO} decreases, and instability in the power supply may appear as excess delay dispersion.

This delay is measured to the 50% point for the supply in use; therefore, the fastest times are observed with the V_{CC} supply at 2.5 V, and larger values are observed when driving loads that switch at other levels.

When duty cycle accuracy is critical, the logic being driven should switch at 50% of V_{CC} and load capacitance should be minimized. When in doubt, it is best to power V_{CCO} or the entire device from the logic supply and rely on the input PSRR and CMRR to reject noise.

Overdrive and input slew rate dispersions are not significantly affected by output loading and V_{CC} variations.

The TTL-/CMOS-compatible output stage is shown in the simplified schematic diagram (Figure 14). Because of its inherent symmetry and generally good behavior, this output stage is readily adaptable for driving various filters and other unusual loads.

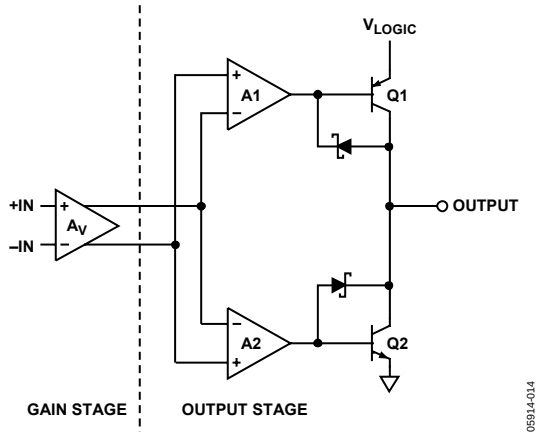

Figure 14. Simplified Schematic Diagram of TTL-/CMOS-Compatible Output Stage

USING/DISABLING THE LATCH FEATURE

The latch input is designed for maximum versatility. It can safely be left floating for fixed hysteresis or be tied to V_{CC} to remove the hysteresis, or it can be driven low by any standard TTL/CMOS device as a high speed latch.

In addition, the pin can be operated as a hysteresis control pin with a bias voltage of 1.25 V nominal and an input resistance of approximately 7000 Ω, allowing the comparator hysteresis to be easily and accurately controlled by either a resistor or an inexpensive CMOS DAC.

Hysteresis control and latch mode can be used together if an open drain, an open collector, or a three-state driver is connected parallel to the hysteresis control resistor or current source.

Due to the programmable hysteresis feature, the logic threshold of the latch pin is approximately 1.1 V regardless of V_{CC}.

OPTIMIZING PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential for obtaining the specified performance. Stray capacitance, inductance, inductive power and ground impedances, or other layout issues can severely limit performance and often cause oscillations. Large discontinuities along input and output transmission lines can also limit the specified pulse-width dispersion performance. The source impedance should be minimized as much as is practicable. High source impedance, in combination with the parasitic input capacitance of the comparator, causes an undesirable degradation in bandwidth at the input, thus degrading the overall response. Thermal noise from large resistances can easily cause extra jitter with slowly slewing input signals; higher impedances encourage undesired coupling.

COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP600/ADCMP601/ADCMP602 comparators are designed to reduce propagation delay dispersion over a wide input overdrive range of 5 mV to TBD. Propagation delay dispersion is the variation in propagation delay that results from a change in the degree of overdrive or slew rate (that is, how far or how fast the input signal exceeds the switching threshold).

Propagation delay dispersion is a specification that becomes important in high speed, time-critical applications, such as data communication, automatic test and measurement, and instrumentation. It is also important in event-driven applications, such as pulse spectroscopy, nuclear instrumentation, and medical imaging. Dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed (Figure 15 and Figure 16).

ADCMP600/ADCMP601/ADCMP602 dispersion is typically <TBD ps as the overdrive varies from 5 mV to 500 mV and the input slew rate varies from TBD V/ns to TBD V/ns. This specification applies to both positive and negative signals because the device has very closely matched delays both for positive-going and negative-going inputs.

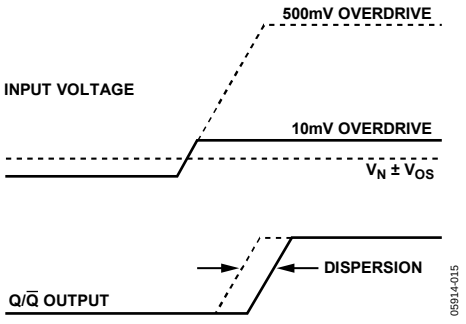

Figure 15. Propagation Delay—Overdrive Dispersion

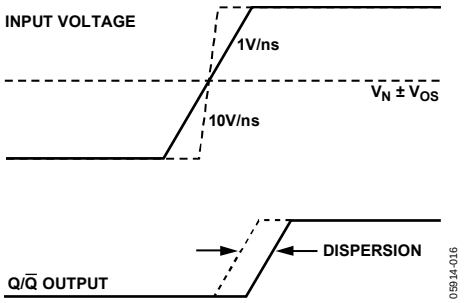

Figure 16. Propagation Delay—Slew Rate Dispersion

COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often desirable in a noisy environment, or when the differential input amplitudes are relatively small or slow moving. Figure 17 shows the transfer function for a comparator with hysteresis. As the input voltage approaches the threshold (0.0 V, in this example) from below the threshold region in a positive direction, the comparator switches from low to high when the input crosses $+V_H/2$, and the new switching threshold becomes $-V_H/2$. The comparator remains in the high state until the new threshold, $-V_H/2$, is crossed from below the threshold region in a negative direction. In this manner, noise or feedback output signals centered on 0.0 V input cannot cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

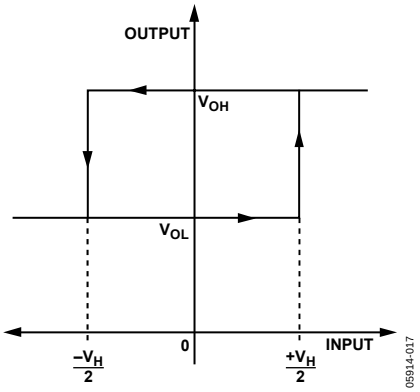

Figure 17. Comparator Hysteresis Transfer Function

The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. One limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that is not symmetric about the threshold. The external feedback network can also introduce significant parasitics that reduce high speed performance and induce oscillation in some cases.

The ADCMP600 features a fixed hysteresis of approximately 2 mV. The ADCMP601 and ADCMP602 comparators offer a programmable hysteresis feature that can significantly improve accuracy and stability. Connecting an external pull-down resistor or a current source from the LE/HYS pin to GND, varies the amount of hysteresis in a predictable, stable manner.

Leaving the LE/HYS pin disconnected results in a fixed hysteresis of 2 mV; driving this pin high removes the hysteresis. The maximum hysteresis that can be applied using this pin is approximately 160 mV. Figure 18 illustrates the amount of hysteresis applied as a function of the external resistor value, and Figure TBD illustrates hysteresis as a function of the current.

The hysteresis control pin appears as a 1.25 V bias voltage seen through a series resistance of 7k ± 20% throughout the hysteresis control range. The advantages of applying hysteresis in this manner are improved accuracy, improved stability, reduced component count, and maximum versatility. An external bypass capacitor is not recommended on the HYS pin because it impairs the latch function and often degrades the jitter performance of the device. As described in the Using/Disabling the Latch Feature section, hysteresis control need not compromise the latch function.

CROSSOVER BIAS POINT

In both op amps and comparators, rail-to-rail inputs of this type have a dual front-end design. Certain devices are active near the V_{CC} rail and others are active near the V_{EE} rail. At some predetermined point in the common-mode range, a crossover occurs. At this point, normally $V_{CC}/2$, the direction of the bias current reverses and the measured offset voltages and currents change.

The ADCMP600/ADCMP601/ADCMP602 slightly elaborate on this scheme. With V_{CC} less than 4 V, this crossover is at the expected $V_{CC}/2$, but with V_{CC} greater than 4 V, the crossover point instead follows V_{CC} 1:1, bringing it to approximately 3 V with V_{CC} at 5 V. This means that when V_{CC} is greater than 4, the comparator input characteristics more closely resemble those of common types of inputs that are not rail to rail.

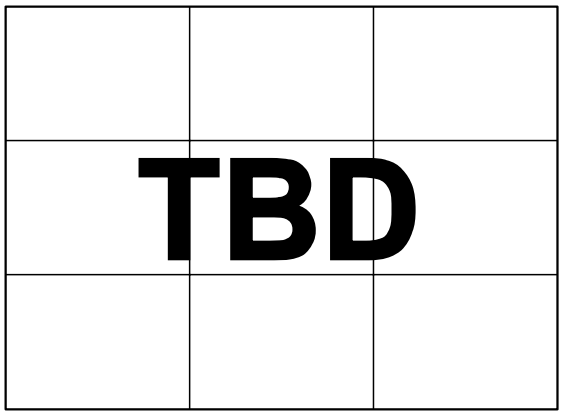

Figure 18. Hysteresis vs. R_{HYS} Control Resistor

MINIMUM INPUT SLEW RATE REQUIREMENT

(Remove if device is stable.)

As with most high speed comparators without hysteresis, a minimum slew rate must be met to ensure that the device does not oscillate as the input signal crosses the threshold. This oscillation is due to the high gain bandwidth of the comparator in combination with feedback parasitics inherent in the package and PC board. A minimum slew rate of TBD V/µs ensures clean output transitions from the ADCMP601 or ADCMP602 comparator without hysteresis. In many applications, chattering is not harmful.

TYPICAL APPLICATION CIRCUITS

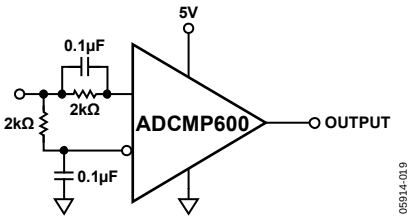

Figure 19. Self-Biased, 50% Slicer

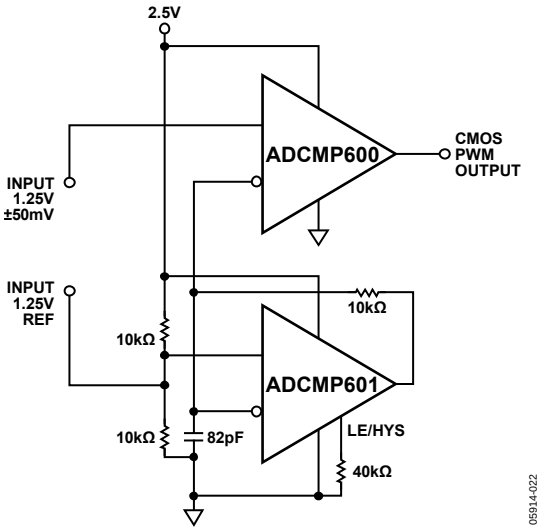

Figure 22. Oscillator and Pulse-Width Modulator

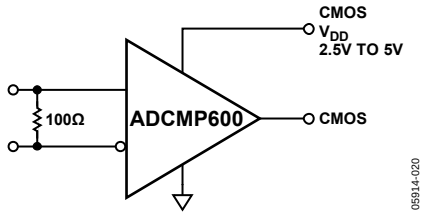

Figure 20. LVDS-to-CMOS Receiver

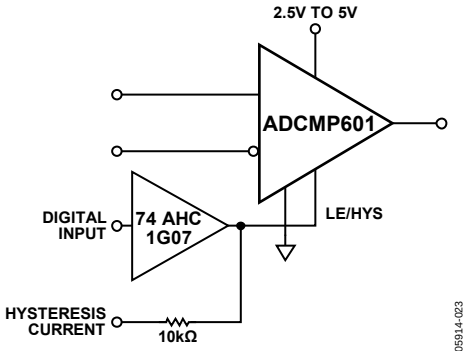

Figure 23. Hysteresis Adjustment with Latch

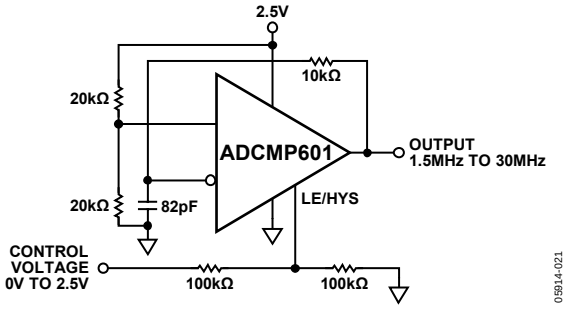

Figure 21. Voltage-Controlled Oscillator

TIMING INFORMATION

Figure 24 illustrates the ADCMP600/ADCMP601/ADCMP602 latch timing relationships. Table 7 provides definitions of the terms shown in the figure.

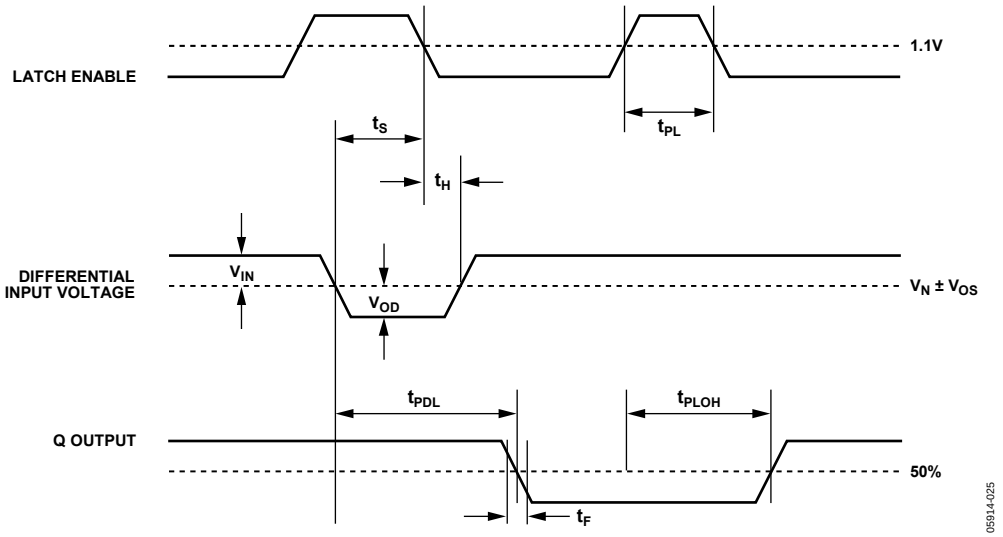

Figure 24. System Timing Diagram

Table 7. Timing Descriptions

Symbol	Timing	Description
t_{PDH}	Input to output high delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition.
t_{PDL}	Input to output low delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition.
t_{PLOH}	Latch enable to output high delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition.
t_{PLOL}	Latch enable to output low delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition.
t_H	Minimum hold time	Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs.
t_{PL}	Minimum latch enable pulse width	Minimum time that the latch enable signal must be high to acquire an input signal change.
t_S	Minimum setup time	Minimum time before the negative transition of the latch enable signal occurs that an input signal change must be present to be acquired and held at the outputs.
t_R	Output rise time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
t_F	Output fall time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
V_{OD}	Voltage overdrive	Difference between the input voltages V_A and V_B.

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