Features

- High Density 72-Mbit
- 166 MHz bus operations with zero wait states – Data is transferred on every clock
- Fully Registered for Pipelined Operation
- User Selectable Linear or Interleaved Burst Order
- Byte Write Capability
- Single 2.5V or 3.3V Power Supply
- Fast Clock to Output Times
  - 3.5 ns (for 166 MHz device)
  - 4.2 ns (for 133 MHz device)
  - 5.0 ns (for 100 MHz device)
- Clock Enable pin to Suspend Operations
- Synchronous Self Timed Writes
- Asynchronous Output Enable
- JEDEC Standard 100-pin TQFP & 119-pin PBGA
- Low Standby Power
- JTAG 1149.1 Compliant Boundary Scan

Description

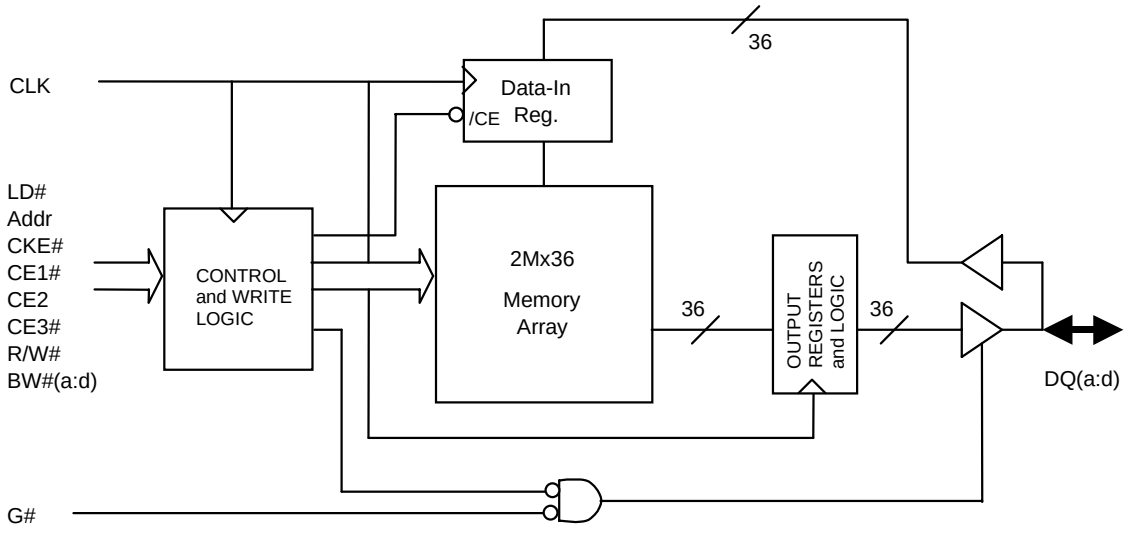
The Enhanced Memory Systems SS2625 is a 72-Mbit synchronous pipelined burst SRAM designed specifically to support back-to-back read/write operations without the insertion of wait states. The device is organized as 2Mx36 and is offered in 3.3V and 2.5V versions. They are designed to transfer data on every clock cycle. This feature dramatically improves throughput, especially in systems that require frequent write/read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable signal, which, when deasserted, suspends operation and extends the previous clock cycle. Maximum access delay from the rising edge of the clock is 3.5 ns (166 MHz device).

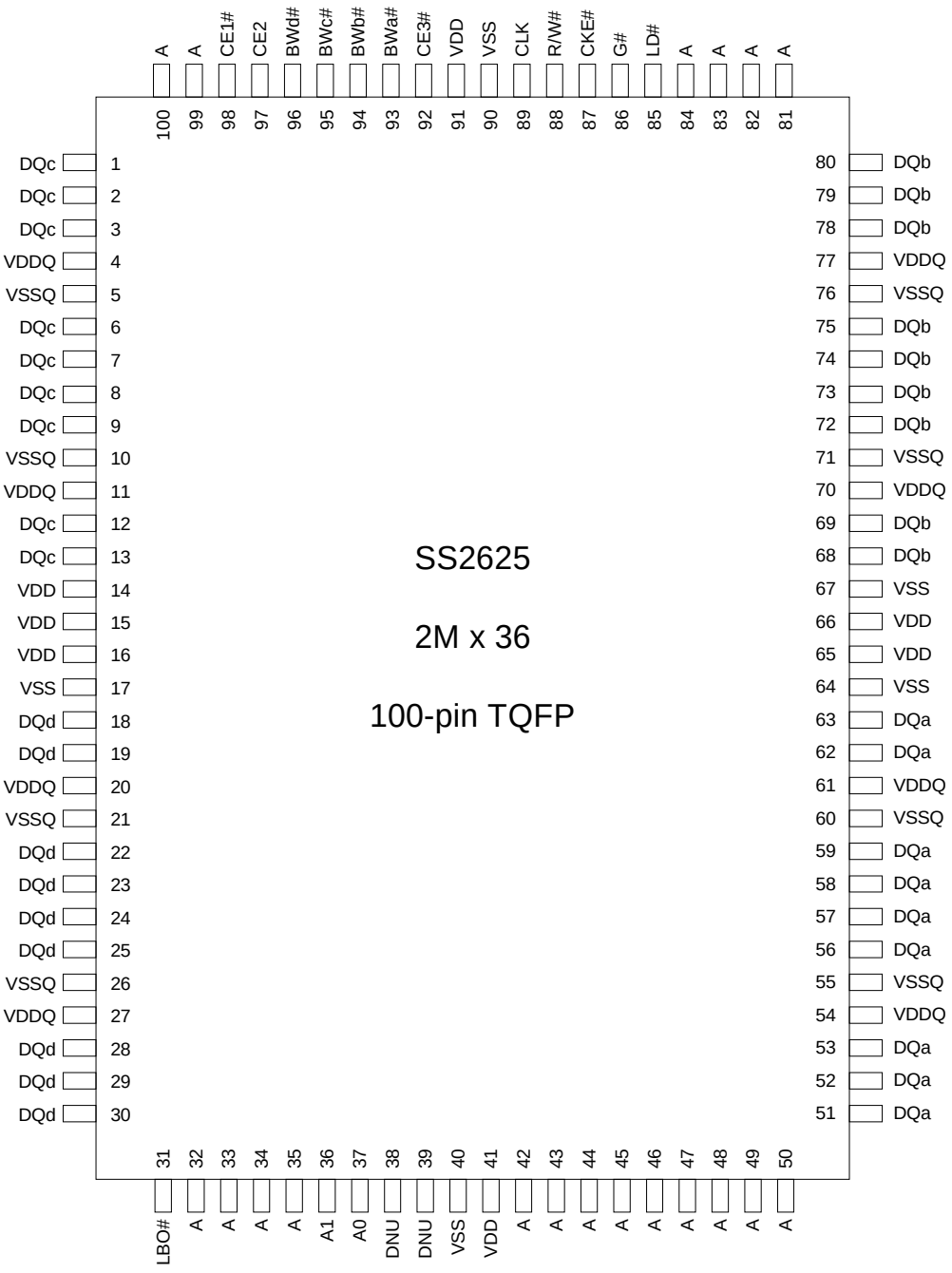
Write operations are controlled by the four Byte Write Select signals and a Read/Write signal. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enable signals and an asynchronous Output Enable signal provide for easy depth expansion and output three-state control. To avoid bus contention, the output drivers are synchronously three-stated during the data portion of a write sequence.

Block Diagram



Pin Assignments (Top View)



Pin Assignments (Top View)

SS2625
2Mx36
119-ball PBGA

	1	2	3	4	5	6	7
A	VDDQ	A	A	A	A	A	VDDQ
B	NC	CE2	A	LD#	A	CE3#	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQc	VSS	NC	VSS	DQb	DQb
E	DQc	DQc	VSS	CE1#	VSS	DQb	DQb
F	VDDQ	DQc	VSS	G#	VSS	DQb	VDDQ
G	DQc	DQc	BWc#	A	BWb#	DQb	DQb
H	DQc	DQc	VSS	R/W#	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	BWd#	NC	BWa#	DQa	DQa
M	VDDQ	DQd	VSS	CKE#	VSS	DQa	VDDQ
N	DQd	DQd	VSS	A1	VSS	DQa	DQa
P	DQd	DQd	VSS	A0	VSS	DQa	DQa
R	NC	A	LBO#	VDD	VDD	A	NC
T	NC	A	A	A	A	A	VSS
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Pin Descriptions

Symbol	Type	Function
CLK	Input	Clock: All input signals (except G#) and output signals are referenced to the rising edge of CLK.
CKE#	Input	Clock Enable: This active low input enables the internal clock signal. If CKE# is driven high, the chip ignores the clock (all signals except G#) and suspends pending operations.
CE1#, CE2, CE3#	Input	Chip Enable Inputs: These inputs determine whether the RAM begins a read, write, or deselect cycle. When qualified by LD# low, all three inputs must be true to select the chip and begin a read or write cycle. When qualified by LD# low, at least one chip enable input must be false to begin a deselect cycle.
LD#	Input	Load Input: This active low input loads the external address, and begins a new read or write cycle. Once a read or write cycle is initiated, LD# must be negated to advance the internal burst counter. LD# cannot be asserted for two consecutive clocks.
R/W#	Input	Read/Write Input: When LD# is asserted and the chip is enabled, this input determines whether the chip begins a read (R/W# high) or write (R/W# low) cycle.
$BW_{[a:d]}$#	Input	Byte Write Inputs: These active low inputs allow write data to be written (BW_x# low) or masked (BW_x# high) during write cycles. During read and deselect cycles, the BW_x# inputs are ignored. BW_a# controls DQ_a, BW_b# controls DQ_b, BW_c# controls DQ_c, and BW_d# controls DQ_d.
A, A1, A0	Input	Address Inputs: Used to select a starting burst address location. The address inputs are sampled when LD# is low and the chip is enabled. Inputs A1 and A0 determine the starting address for all burst cycles.
$DQ_{[a:d]}$	Input/ Output	Data I/O Inputs: These pins deliver output data during burst read cycles. Output data is valid t_{CO} from the rising edge of the clock. These data pins also allow input write data to be written to the chip. Input data must satisfy setup and hold timing specifications.
G#	Input	Output Enable Input: This active low input enables the output data buffers to drive output data during read cycles. When negated, G# three states the data bus. The data output pins are automatically three stated during write and deselect cycles.
LBO#	Input	Linear Burst Order Input: This signal must remain in steady state. Low – Linear burst. High – Interleaved burst.
DNU	Input	Do Not Use Input: These unused pins may be left open circuit, and should be reserved for future address pins.
TCK	Input	Test Clock: Input clock for boundary scan. If boundary scan is not used, TCK must be tied to V_{SS}.
TMS	Input	Test Mode Select: This input controls the TAP controller and is sampled on the rising edge of TCK.
TDI	Input	Test Data In: This is the serial data input for boundary scan testing.
TDO	Output	Test Data Out: This is the serial data output for boundary scan testing.
V_{DD}	Supply	Core Power Supply: Connect to 3.3V or 2.5V.
V_{DDQ}	Supply	I/O Power Supply: Connect to 3.3V (only on V_{DD} = 3.3V devices) or 2.5V.
V_{SS}, V_{SSQ}	Supply	Ground: V_{SS} and V_{SSQ} are connected inside the chip.
NC	-	No Connect: - These pins do not connect to the chip.

Device Operation

The SS2625 is a synchronous pipelined burst SRAM designed specifically to eliminate wait states during write/read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal (CKE#). If CKE# is high, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CKE#. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.5 ns (166 MHz device).

Accesses are initiated by driving all three chip enables (CE1#, CE2, and CE3#) true at the rising edge of the clock. If CKE# and LD# are driven low, an address presented to the device is latched. The access is either a read or write, depending on the status of R/W#. $BW_{[a:d]}$# are used to perform byte write operations. Writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables and an asynchronous Output Enable signal (G#) simplify depth expansion. Reads and writes are pipelined with a two-clock cycle latency. LD# must be driven low to initiate a new transaction. All reads and writes are burst operations. The burst is a non-interruptible sequence of four clock cycles. A burst sequence is determined by the state of the LBO# input signal. Driving LBO# low provides a linear burst order, and driving it high provides an interleaved burst order.

Burst Read Accesses

A burst read access is initiated when the following conditions are satisfied at clock rise: CKE# is driven low; CE1#, CE2, and CE3# are all driven true; R/W# is driven high; and LD# is driven low. The address presented to the inputs A_0-A_x is latched into the Address register and presented to the memory core and control logic. The control logic recognizes a read and allows access to the specified address location. The requested data is allowed to propagate to the data bus within 3.5 ns (166 MHz device) provided G# is driven low. The SS2625 has an on-chip burst counter that is incremented on the rising edge of the clock when LD# is driven high. The device sequences through four address locations for each burst read access.

Once the burst sequence is completed a new read access can be initiated as described above. Reads can be pipelined such that data flows out of the device on every clock edge.

The burst counter uses A0 and A1 in the burst sequence and wraps around when incremented more than four times. See the burst order tables for the burst sequence. The burst sequence is determined by the state of the LBO# input signal. This signal is a strap pin and must remain static during device operation.

Burst Write Accesses

A burst write access is initiated when the following conditions are satisfied at clock rise: CKE# is driven low; CE1#, CE2, and CE3# are all driven true; R/W# is driven low; and LD# is driven low. The address presented to the inputs A_0-A_x is loaded into the Address register and the byte write signals are latched into the control logic block.

On the next rising clock edge the data lines are automatically three-stated regardless of the state of the G# input signal. This allows the external logic to present the data on $DQ_{[a:d]}$.

On the next rising clock edge the data presented to $DQ_{[a:d]}$ inputs (or a subset for byte write operations, see the Write Cycle Description table for details) is latched into the device and stored into the specified address location.

Data written during a write operation is controlled by $BW_{[a:d]}$# signals. The SS2625 provides byte write capability (see the Write Cycle Description table for details). Driving the R/W# input low with the appropriate $BW_{[a:d]}$# input selectively writes to the desired bytes. Bytes not selected during a byte write operation remain unaltered. A synchronous self-timed write mechanism is provided to simplify write operations. Byte write capability is included to greatly simplify read-

-modify-write sequences, which are reduced to simple byte write operations. Because the SS2625 is a common I/O device, data should not be driven into the device while the outputs are active. G# should be driven high before presenting data to the $DQ_{[a:d]}$ inputs. This three-states the output drivers. As a safety precaution, $DQ_{[a:d]}$ are automatically three-stated during the data portion of a write, regardless of the state of G#.

The SS2625 has an on-chip burst counter that increments on the rising edge of the clock when LD# is driven high. The device then sequences through four address locations. If sequencing continues, this counter wraps around to the original location. The appropriate $BW_{[a:d]}$# inputs must be driven in each cycle to write the correct bytes of data.

The burst sequence is determined by the state of the LBO# input. See the Burst Order tables for the sequence. The LBO# input signal is a strap pin and must remain static during device operation.

Deselecting the Device

Deselecting the SS2625 is accomplished by deasserting any of the chip enables while driving LD# low. The deselect process requires four clock cycles to complete. When deselected the device enters a lower power state while still monitoring the input signals to detect any new access. A deselect must occur at least once every 16 us (for example: once every 1600 clock cycles at 100MHz). The $DQ_{[a:d]}$ pins are automatically three-stated two clocks after the deselection.

Truth Table

Operation	Address Used	CLK	CKE#	CE	LD#	R/W#	BW_X#	Notes
Deselect	N/A	↑	L	F	L	X	X	1, 2
Begin Read	External	↑	L	T	L	H	X	2
Continue Read	Next	↑	L	X	H	X	X	
Begin Write	External	↑	L	T	L	L	V	2, 3
Continue Write	Next	↑	L	X	H	X	V	3
Suspend	Current	↑	H	X	X	X	X	4

Notes:
1. A deselect cycle is complete in four clocks.
2. T = True and F = False. CE is true when CE1# and CE3# are low and CE2 is high. CE is false when CE1# is high or CE2 is low or CE3# is high.
3. V = Valid. During write cycles, the BW_X# inputs must be valid (high or low) throughout the burst cycle.
4. If suspend occurs during a read, the DQ bus remains active (low-Z). During write and deselect cycles, the DQ bus remains in a high-Z state. No write operations are performed during suspend.

Electrical Characteristics

Absolute Maximum Ratings

Description	Symbol	Value
Power Supply Voltage (3.3V device)	V_{DD3}	-0.5V to +4.6V
Power Supply Voltage (2.5V device)	V_{DD2}	-0.5V to +3.6V
Voltage on any Pin with Respect to Ground	V_{IN}, V_{OUT}	-0.5V to V_{DDQ} +0.5V
Operating Temperature (ambient)	T_A	-55°C to +125°C
Storage Temperature	T_{stg}	-65°C to +150°C
Power Dissipation	P_D	1.2 W (TQFP), 1.6 W (PBGA)
DC Output Current (I/O pins)	I_{OUT}	20mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these, or any other conditions above those listed in the operational section of the specification, is not implied. Exposure to conditions at absolute maximum ratings for extended periods may affect device reliability.

DC Characteristics (T_A = 0ºC to 70ºC)

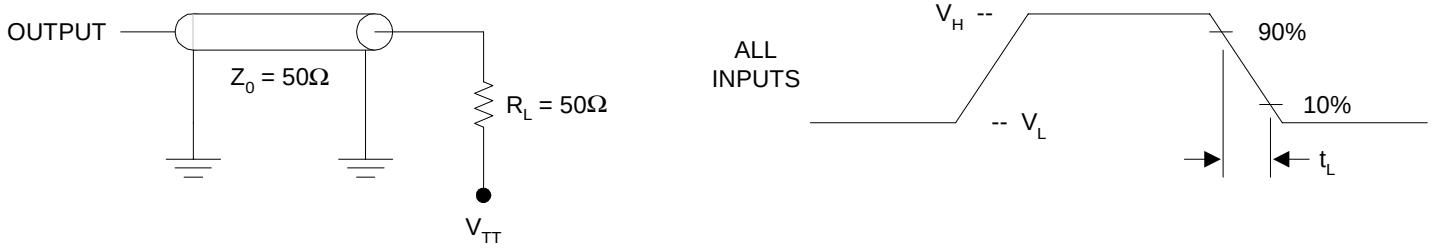
Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DD3}	Power Supply Voltage	3.135	3.3	3.465	V	1
V_{DDQ3}	I/O Supply Voltage	2.375	-	3.465	V	1
V_{DD2}	Power Supply Voltage	2.375	2.5	2.625	V	2
V_{DDQ2}	I/O Supply Voltage	2.375	2.5	2.625	V	2
V_{IHDQ}	Input High Voltage (DQ pins)	2.0	-	V_{DDQ} + 0.3	V	
V_{IH1}	Input High Voltage (Input-only pins)	2.0	-	V_{DD} + 0.3	V	1, 3
V_{IL1}	Input Low Voltage	-0.3	-	0.8	V	1, 3
V_{IH2}	Input High Voltage (Input-only pins)	1.7	-	V_{DD} + 0.3	V	2, 4
V_{IL2}	Input Low Voltage	-0.3	-	0.7	V	2, 4
V_{OH3}	Output High Voltage (I_{OUT} = -4mA)	2.4	-	V_{DDQ}	V	3
V_{OL3}	Output Low Voltage (I_{OUT} = +8mA)	V_{SS}	-	0.4	V	3
V_{OH2}	Output High Voltage (I_{OUT} = -4mA)	2.0	-	V_{DDQ}	V	4
V_{OL2}	Output Low Voltage (I_{OUT} = +4mA)	V_{SS}	-	0.4	V	4
$I_{I(L)}$	Input Leakage Current	-	-	±5	µA	
$I_{O(L)}$	Output Leakage Current	-	-	±5	µA	

Notes:
1. Applies to SM2625Q and SM2625B 3.3V devices.
2. Applies to SM2625Q1 and SM2625B1 2.5V devices.
3. V_{DDQ} = 3.3V ± 5%.
4. V_{DDQ} = 2.5V ± 5%.

Capacitance (T_A = 0ºC to 70ºC)

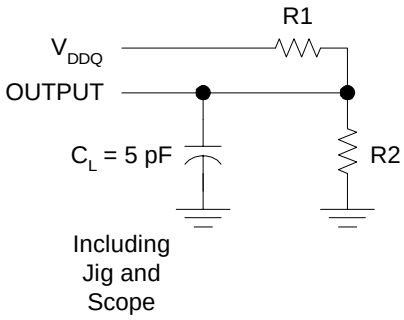
Symbol	Parameter	Min	Typical	Max	Units	Notes
C_{IN}	Input Capacitance	2.5	-	4	pF	
$C_{I/O}$	Input/Output Capacitance	3.5	-	6	pF	

AC Test Load



For V_{DD} = 3.3V, AC timing tests use V_L = 0V and V_H = 3.0V. For V_{DDQ} = 2.5V AC timing tests use V_L = 0V and V_H = 2.5V. In both cases, input transit time t_T must be ≤ 2 ns. Input timings are referenced to (V_H-V_L) / 2. Output timings are referenced to V_{TT} (for V_{DDQ} = 3.3V, V_{TT} = 1.5V and for V_{DDQ} = 2.5V, V_{TT} = 1.25V).

DC Equivalent Load



For VDDQ = 2.5V
R1 = 422Ω
R2 = 390Ω

For VDDQ = 3.3V
R1 = 317Ω
R2 = 351Ω

Package Thermal Characteristics

Symbol	Parameter	TQFP	PBGA	Units	Notes
θ_{JA}	Thermal Resistance (Junction to Ambient)	25	22	°C/W	1, 2, 3
θ_{JC}	Thermal Resistance (Junction to Case)	10	8	°C/W	2

Notes:
1. Tested in still air with device soldered to a 4.25 x 1.125 inch, 4-layer printed circuit board.
2. Tested initially and after any design or process changes that may affect these parameters.
3. Value accounts for thermal conduction through device leads or solder balls.

Operating Currents (T_A = 0°C to 70°C)

Symbol	Parameter	Test Conditions	Value			Units
			-6	-7.5	-10	
I_{CC}	Operating Current	Read or Write Every 4 Cycles V_{DD} = Max., I_{OUT} = 0 mA, f = $1/t_{CK}$	220	200	175	mA
I_{SB1}	Automatic CE Power Down Current-TTL Inputs	V_{DD} = Max., Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = $1/t_{CK}$	50	40	35	mA
I_{SB2}	Automatic CE Power Down Current-CMOS Inputs	V_{DD} = Max., Device Deselected, $V_{IN} \leq 0.3V$ or $V_{IN} \geq V_{DDQ} - 0.3V$, f = 0	20	20	20	mA
I_{SB3}	Automatic CE Power Down Current-CMOS Inputs	V_{DD} = Max., Device Deselected, $V_{IN} \leq 0.3V$ or $V_{IN} \geq V_{DDQ} - 0.3V$, f = $1/t_{CK}$	40	30	25	mA

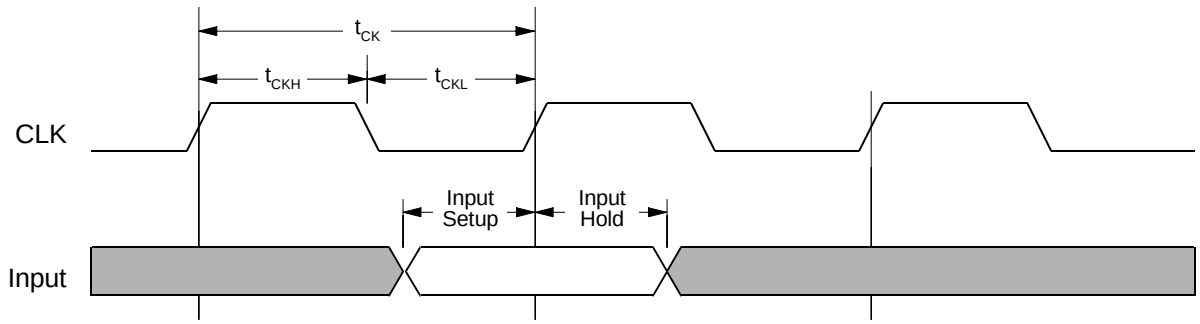
AC Characteristics (T_A = 0°C to 70°C)

Clock

Symbol	Parameter	-6		-7.5		-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
t_{CK}	Clock Cycle Time	6	-	7.5	-	10	-	ns	
t_{CKH}	Clock High Time	2.3	-	2.8	-	3.2	-	ns	1
t_{CKL}	Clock Low Time	2.3	-	2.8	-	3.2	-	ns	1

Notes:
1. This parameter is sampled and not 100% tested.

Clock and Input Timing



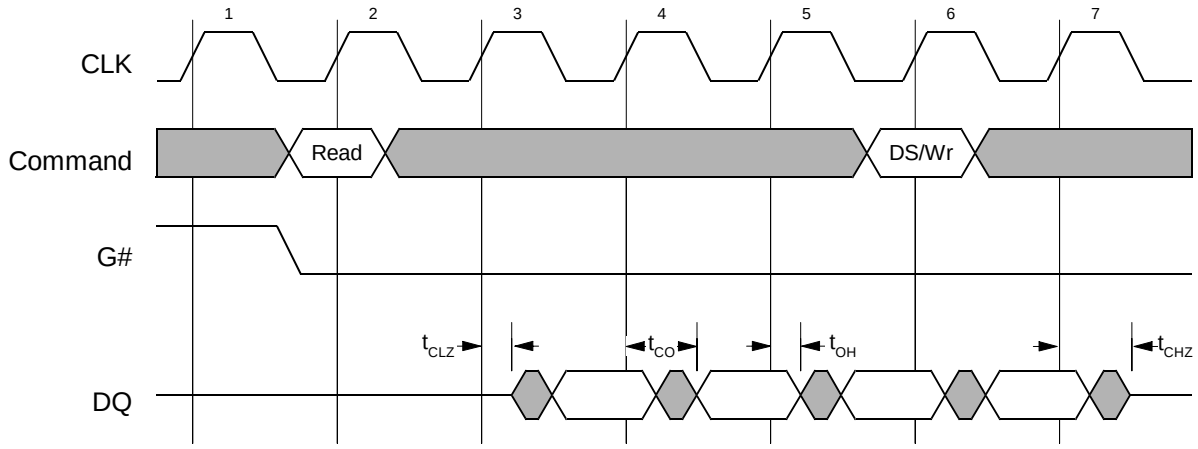
Input Setup

Symbol	Parameter	-6		-7.5		-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
t_{AS}	Address Setup Time	1.5	-	2.0	-	2.0	-	ns	
t_{DS}	Data Input Setup Time	1.5	-	2.0	-	2.0	-	ns	
t_{CKES}	Clock Enable Setup Time	1.5	-	2.0	-	2.0	-	ns	
t_{RWS}	R/W#, $BW_{[a:d]}$ Setup Time	1.5	-	2.0	-	2.0	-	ns	
t_{LDS}	LD# Setup Time	1.5	-	2.0	-	2.0	-	ns	
t_{CES}	Chip Enable Setup Time	1.5	-	2.0	-	2.0	-	ns	

Input Hold

Symbol	Parameter	-6		-7.5		-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
t_{AH}	Address Hold Time	0.5	-	0.5	-	0.5	-	ns	
t_{DH}	Data Input Hold Time	0.5	-	0.5	-	0.5	-	ns	
t_{CKEH}	Clock Enable Hold Time	0.5	-	0.5	-	0.5	-	ns	
t_{RWH}	R/W#, $BW_{[a:d]}$ Hold Time	0.5	-	0.5	-	0.5	-	ns	
t_{LDH}	LD# Hold Time	0.5	-	0.5	-	0.5	-	ns	
t_{CEH}	Chip Enable Hold Time	0.5	-	0.5	-	0.5	-	ns	

Output Timing



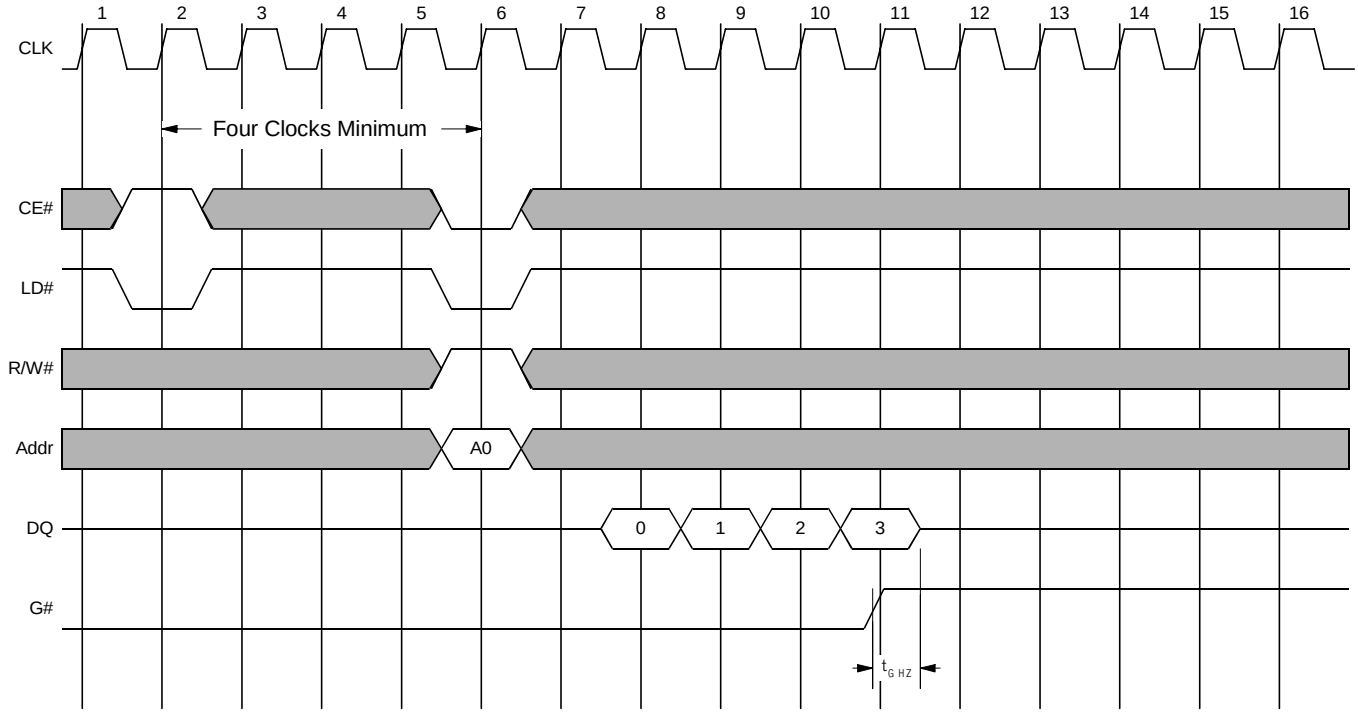
Output

Symbol	Parameter	-6		-7.5		-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
t_{CO}	Data Valid After CLK Rise	-	3.5	-	4.2	-	5.0	ns	1
t_{GV}	G# Low to Output Valid	-	3.5	-	4.2	-	5.0	ns	2,3
t_{OH}	Data Output Hold	1.5	-	1.5	-	1.5	-	ns	
t_{CHZ}	Clock to High-Z	1.5	3.5	1.5	3.5	1.5	3.5	ns	1,2,3,4
t_{CLZ}	Clock to Low-Z	1.5	-	1.5	-	1.5	-	ns	1,2,3,4
t_{GHZ}	G# High to Output High-Z	-	3.3	-	4.0	-	4.8	ns	1,2,4
t_{GLZ}	G# Low to Output Low-Z	0	-	0	-	0	-	ns	1,2,4

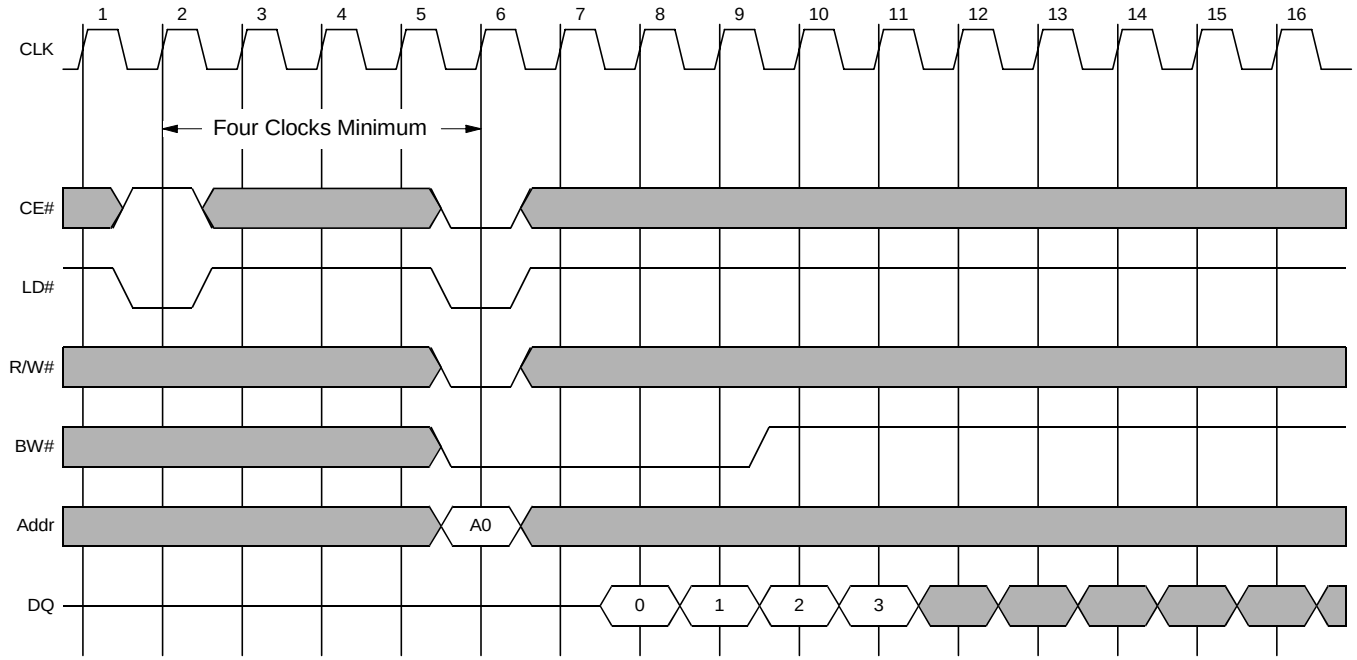
Notes:
1. AC test conditions assume a signal transition time of 2.0 ns or less, timing reference levels, input pulse levels, and output loading as shown in the Test Loads circuit diagram.
2. t_{CHZ}, t_{CLZ}, t_{GHZ}, and t_{GLZ} are specified with AC test conditions shown in the Test Loads circuit diagram. Transition is measured + 200mV from steady-state voltage.
3. At any given voltage and temperature, t_{GHZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst-case user conditions. The device is designed to achieve High-Z prior to Low-Z under the same system conditions.
4. This parameter is sampled and not 100% tested.

Timing Diagrams

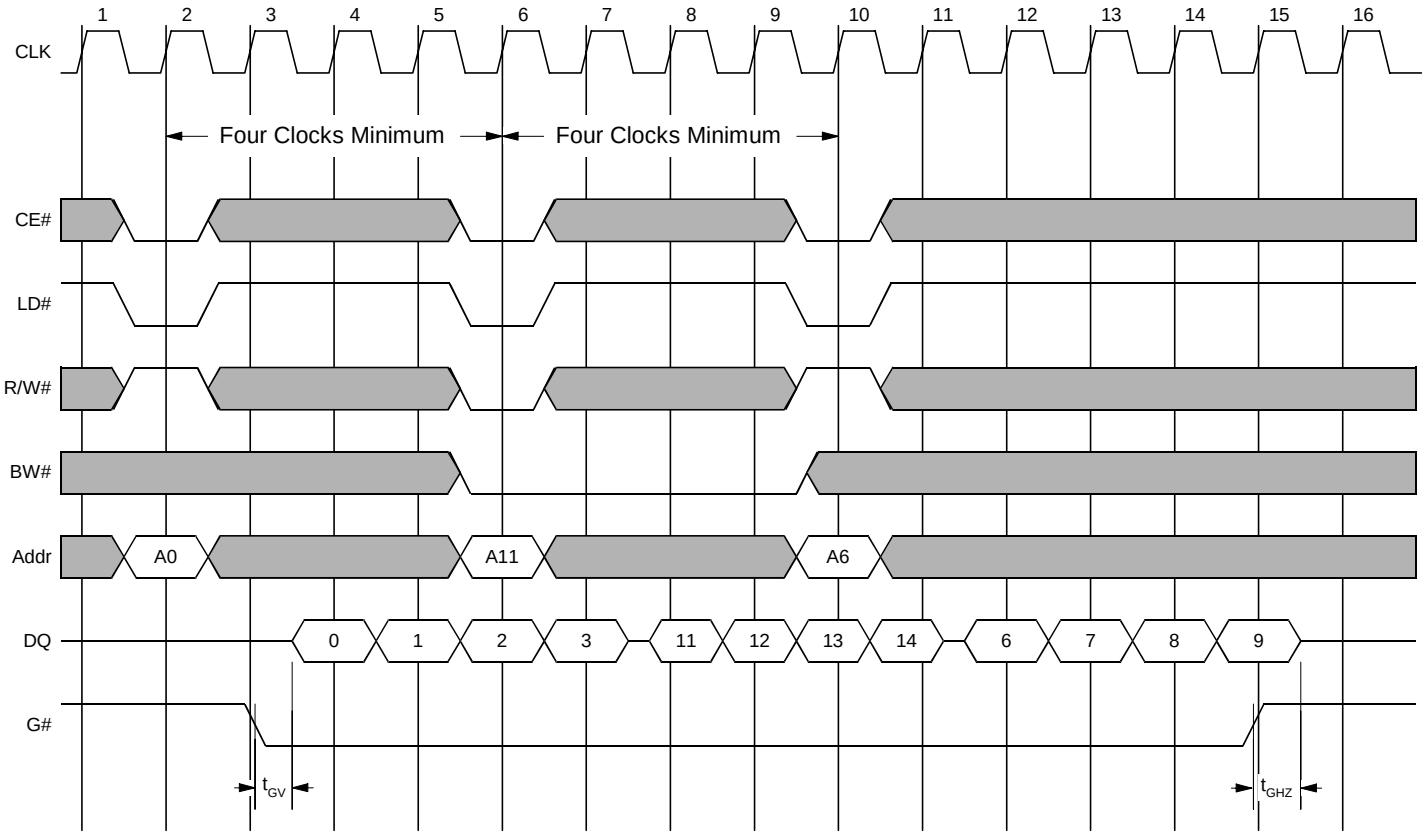
Deselect-Read



Deselect-Write



Read-Write-Read



IEEE 1149.1 Serial Boundary Scan (JTAG)

The SS2625 includes a serial boundary scan Test Access Port (TAP) in the PGBA package only. The TAP is not included in the TQFP package. This port functions in accordance with IEEE Standard 1149.1-1990, but does not have the set of functions required for full 1149.1 compliance. These functions are excluded because they place an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices that use 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 2.5V I/O logic levels.

Disabling the JTAG Feature

The SS2625 can operate without the JTAG feature. To disable the TAP controller, tie TCK to V_{SS} to prevent clocking the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. At power-up the device is now in a reset state, which does not interfere with device operation.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. This pin is pulled up internally.

Test Data In (TDI)

The TDI pin is used to serially input information to the registers. It can be connected to the input of any of the registers. Which register is placed between TDI and TDO is determined by the instruction loaded into the TAP Instruction register. See the TAP Controller State Diagram for more information. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output is used to serially output information from the registers. The output is active depending on the current state of the TAP state machine. See the TAP Controller State Diagram for more information. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A reset is performed by forcing TMS high for five rising edges of TCK. This reset does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow scanning of data into and out of the SRAM test circuitry. Only one register can be selected at a time through the Instruction register. Data is serially loaded through the TDI pin on the rising edge of TCK, and output through the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the Instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. At power-up, the Instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section “Performing a TAP Reset”.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The Bypass register is a single-bit register that can be placed between the TDI and TDO pin, allowing data to shift through the SRAM with minimal delay. The Bypass register is set low when the Bypass instruction is executed.

Boundary Scan Register

This 70-bit register is connected to all input and output pins on the SRAM. Several no-connect (NC) pins are included in the Boundary Scan register to reserve pins for higher density devices.

The Boundary Scan register is loaded with the current states on the inputs and outputs of the pad ring when the TAP controller enters the Capture-DR state, and is then placed between the TDI and TDO pins when the controller enters the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE-Z instructions can be used to capture the contents of the pad ring.

The Boundary Scan Order table shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the Instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is `in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the 3-bit Instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described below.

The TAP controller used in this SRAM is not fully compliant with the 1149.1 conventions because some of the mandatory instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM, and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 instructions EXTEST, INTEST, or the PRELOAD portion of SAMPLE/PRELOAD. Instead it capture the current states on the inputs and outputs of the pad ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the Instruction register is placed between TDI and TDO. During this state, instructions are shifted through the Instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller is moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction that is executed when the Instruction register is loaded with all 0s. EXTEST, as specified, is not implemented in the TAP controller. Therefore, this device is not fully compliant with the 1149.1 standard.

However, the TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the Instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction is loaded. The only difference is that unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a high-Z state.

IDCODE

The IDCODE instruction causes a vendor specific, 32-bit code to load into the ID register. It also places the ID register between the TDI and TDO pins, and allows shifting of the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the Instruction register at power up or when the TAP controller is given a TEST-LOGIC RESET state.

SAMPLE-Z

The SAMPLE-Z instruction places the Boundary Scan register between the TDI and TDO pins when the TAP controller enters a Shift-DR state. It also places all SRAM outputs into a high-Z state.

SAMPLE/PRELOAD

SAMPLE/Preload is a mandatory 1149.1 instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully compliant with the 1149.1 standard.

When the SAMPLE/PRELOAD instruction is loaded into the Instruction register, and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the Boundary Scan register.

An important point is that the TAP controller clock operates at a frequency up to 10 MHz, while the SRAM clock operates more that a magnitude faster. Because of this, it is possible for an input or output to change during the Capture-DR state. If the TAP tries to capture a signal while it is transitioning (metastable state), the device is not harmed, but the results are not guaranteed and possibly not repeatable.

To guarantee that the Boundary Scan register captures the correct value, the signal must be stable long enough to meet TAP controller capture set-up and hold times (t_{CS} and t_{CH}). To capture the SRAM clock input correctly there must be a way to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is not done in the design, it is still possible to capture all other signals and simply ignore the value of CLK captured in the Boundary Scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the Boundary Scan register between the TDI and TDO pins.

Note that since the PRELOAD part of this instruction is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction has the same effect as the Pause-DR instruction.

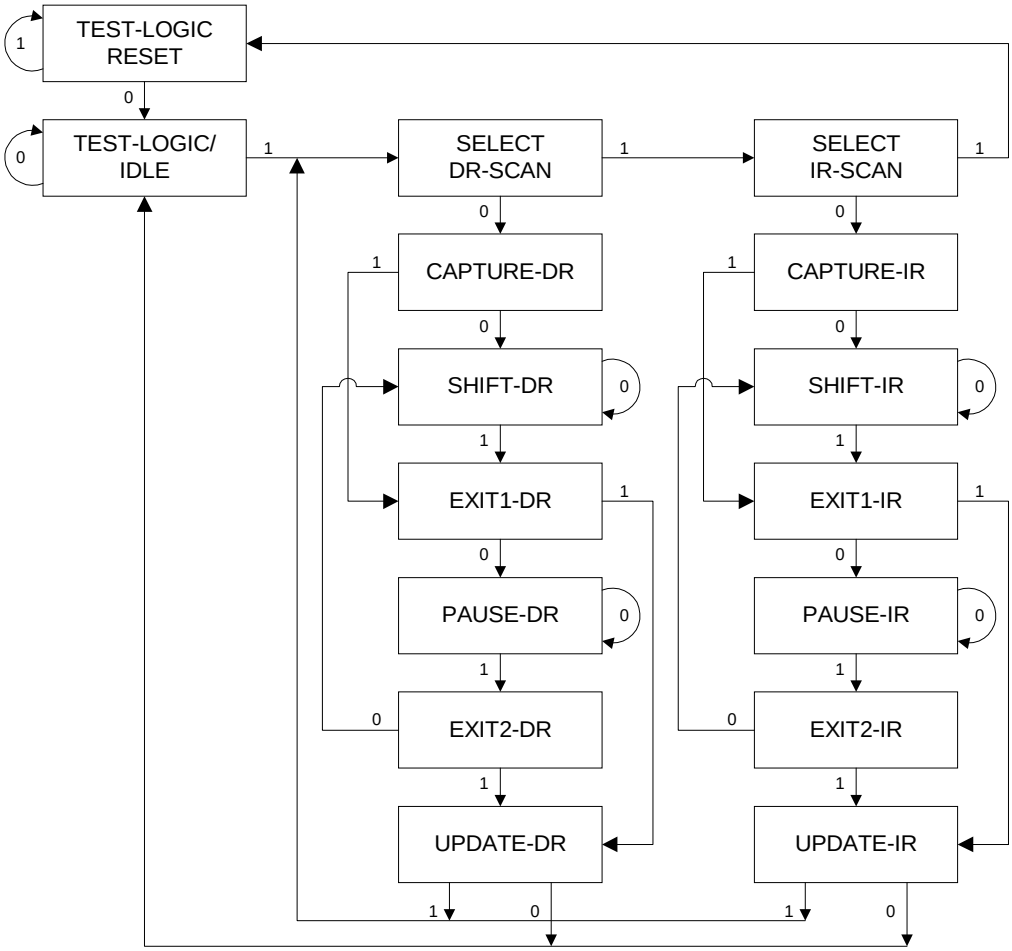
BYPASS

When the BYPASS instruction is loaded in the Instruction register and the TAP is placed in a Shift-DR state, the Bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

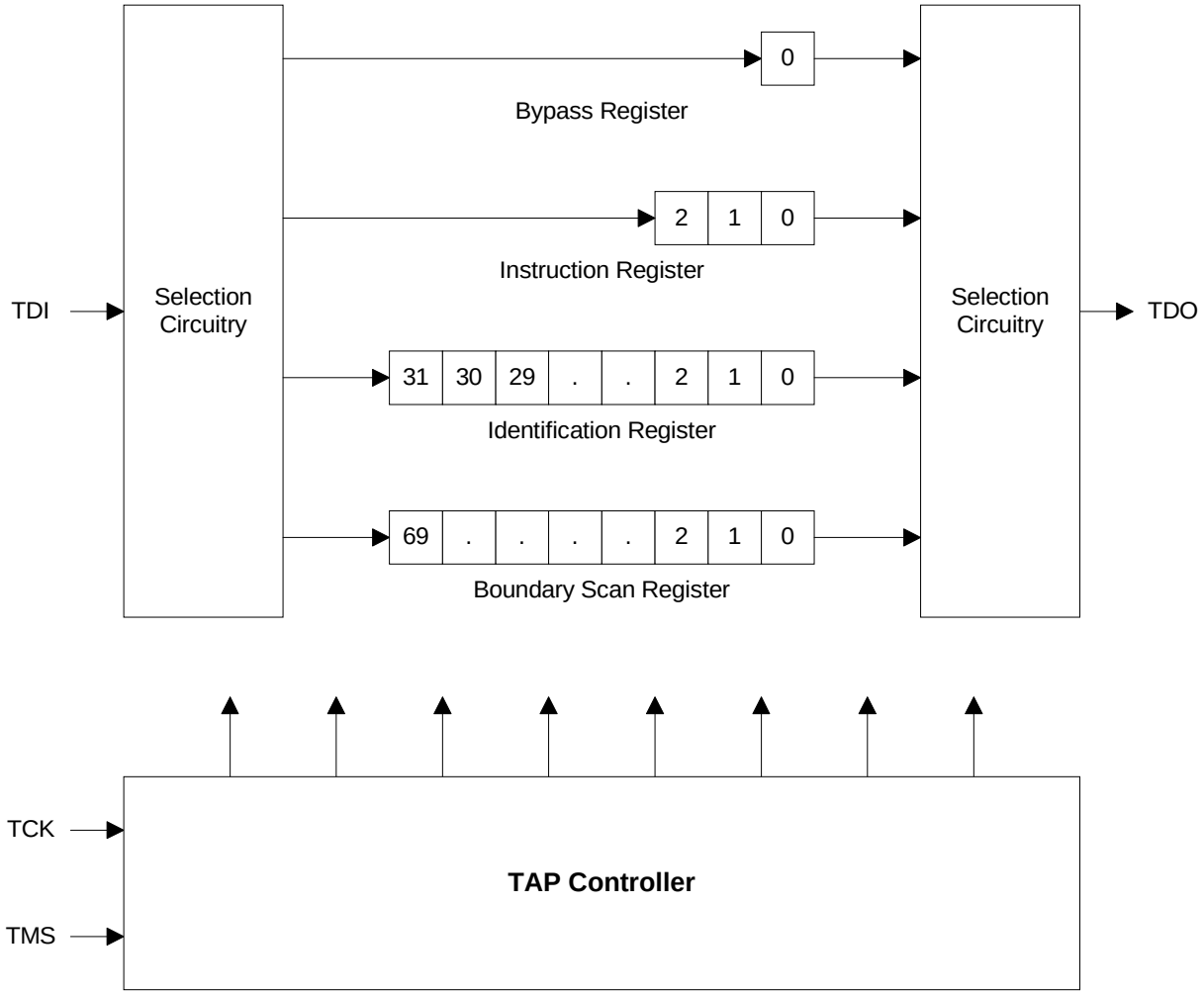
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



NOTE: The 0 or 1 next to each state represents the TMS signal value at the rising edge of TCK.

TAP Controller Block Diagram



TAP DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Max	Units	Notes
V_{OH1}	Output High Voltage	I_{OH} = -2.0 mA	2.0	-	V	1
V_{OH2}	Output High Voltage	I_{OH} = -100 µA	2.2	-	V	1
V_{OL1}	Output Low Voltage	I_{OL} = 2.0 mA	-	0.4	V	1
V_{OL2}	Output Low Voltage	I_{OL} = 100 µA	-	0.2	V	1
V_{IH}	Input High Voltage	–	1.7	V_{DD}+0.3	V	1, 2
V_{IL}	Input Low Voltage	–	-0.3	0.7	V	1, 2
I_X	Input and Output Leakage Current	GND ≤ V_{IN} ≤ V_{DDQ}	-	±5	µA	1

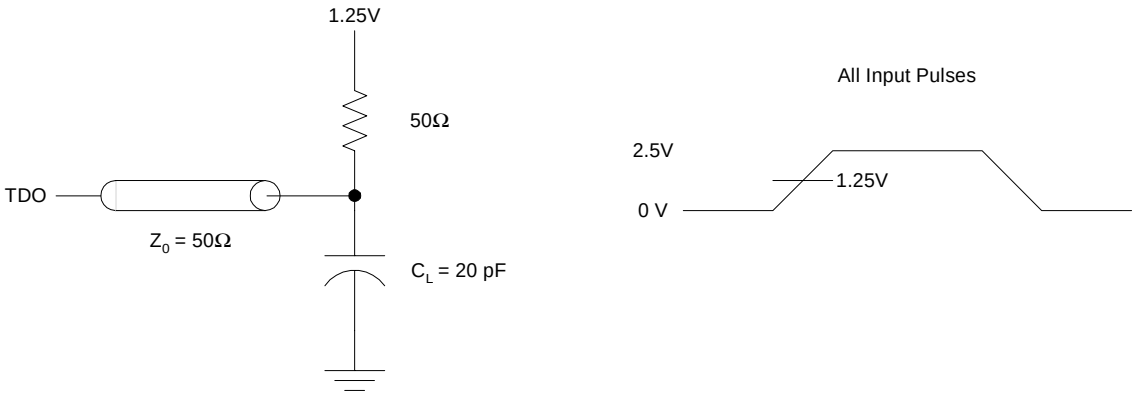
Notes:
1. All voltage referenced to ground.
2. Overshoot: $V_{IH}(AC) \leq V_{DD}+0.7V$ for $t \leq (t_{TCYC} / 2)$,
   Undershoot: $V_{IL}(AC) \leq 0.5V$ for $t \leq (t_{TCYC} / 2)$,
   Power up: $V_{IH} \leq 2.6V$ and $V_{DD}<2.4V$ and $V_{DDQ}<1.4$ for t<200ms.

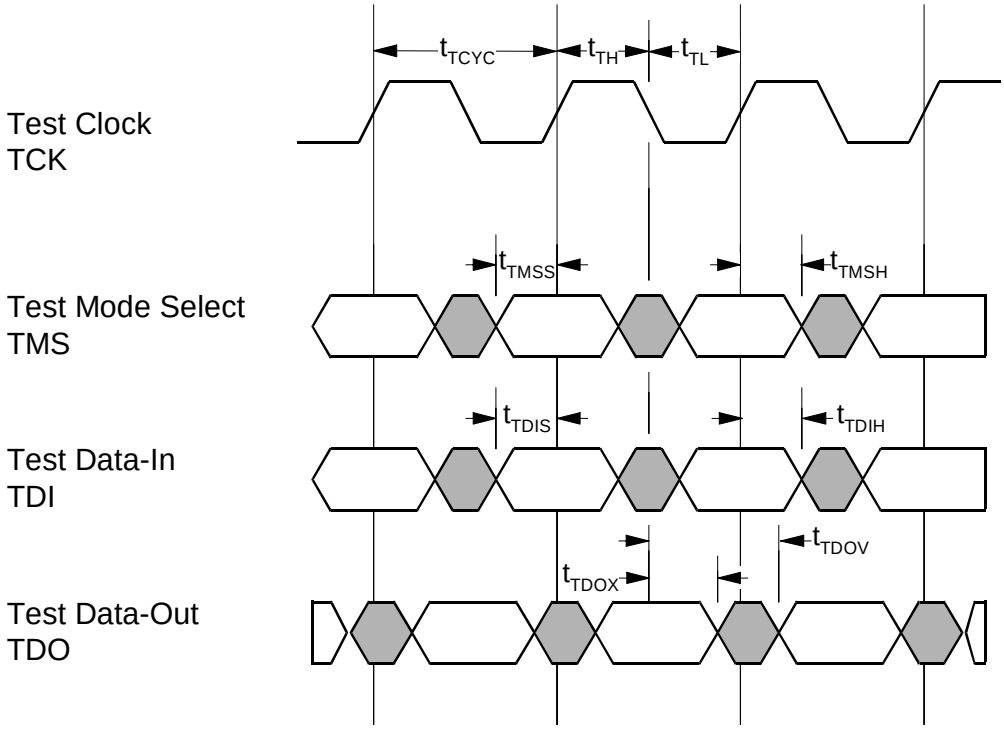
TAP AC Switching Characteristics

Symbol	Parameter	Min	Max	Units	Notes
t_{TCYC}	TCK Clock Cycle Time	100	-	ns	1
t_{TF}	TCK Clock Frequency	-	10	MHz	1
t_{TH}	TCK Clock High	40	-	ns	1
t_{TL}	TCK Clock Low	40	-	ns	1
t_{TMSS}	TMS Setup to TCK Clock Rise	10	-	ns	1
t_{TDIS}	TDI Setup to TCK Clock Rise	10	-	ns	1
t_{CS}	Capture Setup to TCK Clock Rise	10	-	ns	1, 2
t_{TMSH}	TMS Hold after TCK Clock Rise	10	-	ns	1
t_{TDIH}	TDI Hold after Clock Rise	10	-	ns	1
t_{CH}	Capture Hold after Clock Rise	10	-	ns	1, 2
t_{TDOV}	TCK Clock Low to TDO Valid	-	20	ns	1
t_{TDOX}	TCK Clock Low to TDO Invalid	0	-	ns	1

Notes:
1. Test conditions are specified using the loads in TAP AC test conditions. t_R/t_F = 1 ns.
2. t_{CS} and t_{CH} refer to the setup and hold time requirements for latching data from the Boundary Scan register.

TAP Timing and Test Conditions





Boundary Scan Order

Scan Bit #	Signal Name	BGA Pin Location	Scan Bit #	Signal Name	BGA Pin Location	Scan Bit #	Signal Name	BGA Pin Location
0	LBO#	3R	25	DQb	6H	50	A	5B
1	A	3A	26	DQb	7H	51	A	2A
2	A	4A	27	DQb	6G	52	DQc	1H
3	A	5A	28	DQb	7G	53	DQc	2H
4	A	6A	29	DQb	6F	54	DQc	1G
5	A1	4N	30	DQb	6E	55	DQc	2G
6	A0	4P	31	DQb	7E	56	DQc	2F
7	A	2T	32	DQb	6D	57	DQc	1E
8	A	3T	33	DQb	7D	58	DQc	2E
9	A	4T	34	A	3C	59	DQc	1D
10	A	5T	35	A	5C	60	DQc	2D
11	A	6T	36	A	6C	61	DQd	1P
12	A	2R	37	A	3B	62	DQd	2P
13	A	6R	38	LD#	4B	63	DQd	1N
14	A	4G	39	G#	4F	64	DQd	2N
15	A	2C	40	CKE#	4M	65	DQd	2M
16	DQa	6P	41	R/W#	4H	66	DQd	1L
17	DQa	7P	42	CLK	4K	67	DQd	2L
18	DQa	6N	43	CE_3#	6B	68	DQd	1K
19	DQa	7N	44	BW_a#	5L	69	DQd	2K
20	DQa	6M	45	BW_b#	5G			
21	DQa	6L	46	BW_c#	3G			
22	DQa	7L	47	BW_d#	3L			
23	DQa	6K	48	CE_2	2B			
24	DQa	7K	49	CE_1#	4E			

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:29)	XXX	Defines die revision number.
Voltage (28,24)	X,X	Defines VDD voltage of SRAM – 0,0 (3.3V) and 0,1 (2.5V).
Reserved (27:25)	XXX	Reserved.
Architecture (23:21)	001	Defines SRAM architecture (NoBL).
Memory Type (20:18)	011	Defines type of SRAM (pipelined burst 4).
Bus Width (17:15)	100	Defines width of SRAM.
Density (14:12)	100	Defines density of SRAM (64M/72M).
JEDEC Code (11:1)	000 0011 0010	Unique identification of SRAM vendor (32 hex for Enhanced Memory Systems).
ID Register Presence (0)	1	Indicates the presence of an ID register.

Scan Register Sizes

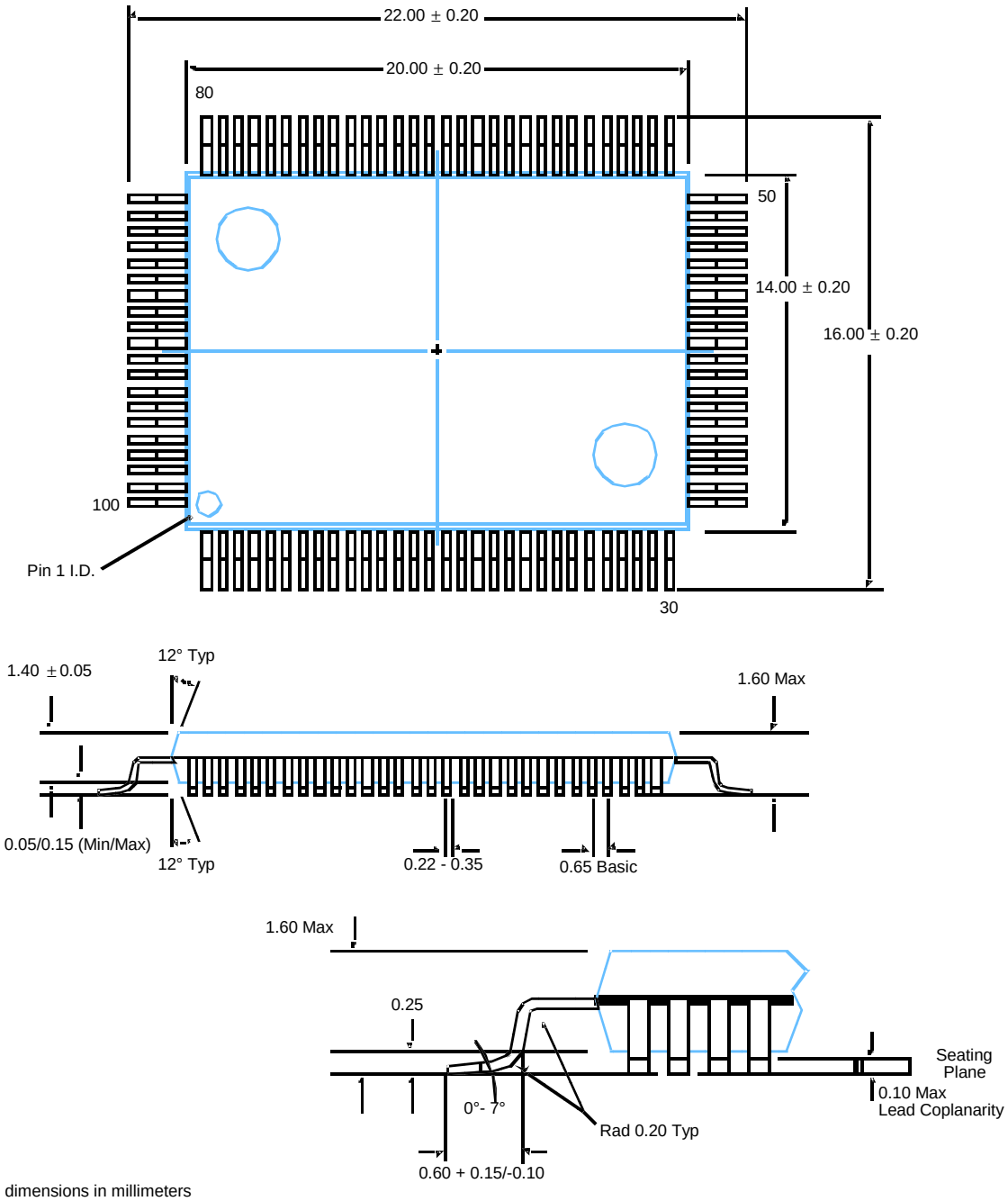
Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	70

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input/output states. Places the Boundary Scan register between TDI and TDO. Forces all SRAM outputs to high-Z state. This instruction is not 1149.1 compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input/output states. Places the Boundary Scan register between TDI and TDO. Forces all SRAM output drivers to a high-Z state
RESERVED	011	Do Not Use: This instruction id reserved for future use.
SAMPLE/PRELOAD	100	Captures the input/output states. Places the Boundary Scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement the 1149.1 preload function and is therefore not 1149.1 compliant
RESERVED	101	Do Not Use: This instruction id reserved for future use.
RESERVED	110	Do Not Use: This instruction id reserved for future use.
BYPASS	111	Places the Bypass register between TDI and TDO. Does not affect SRAM operation.

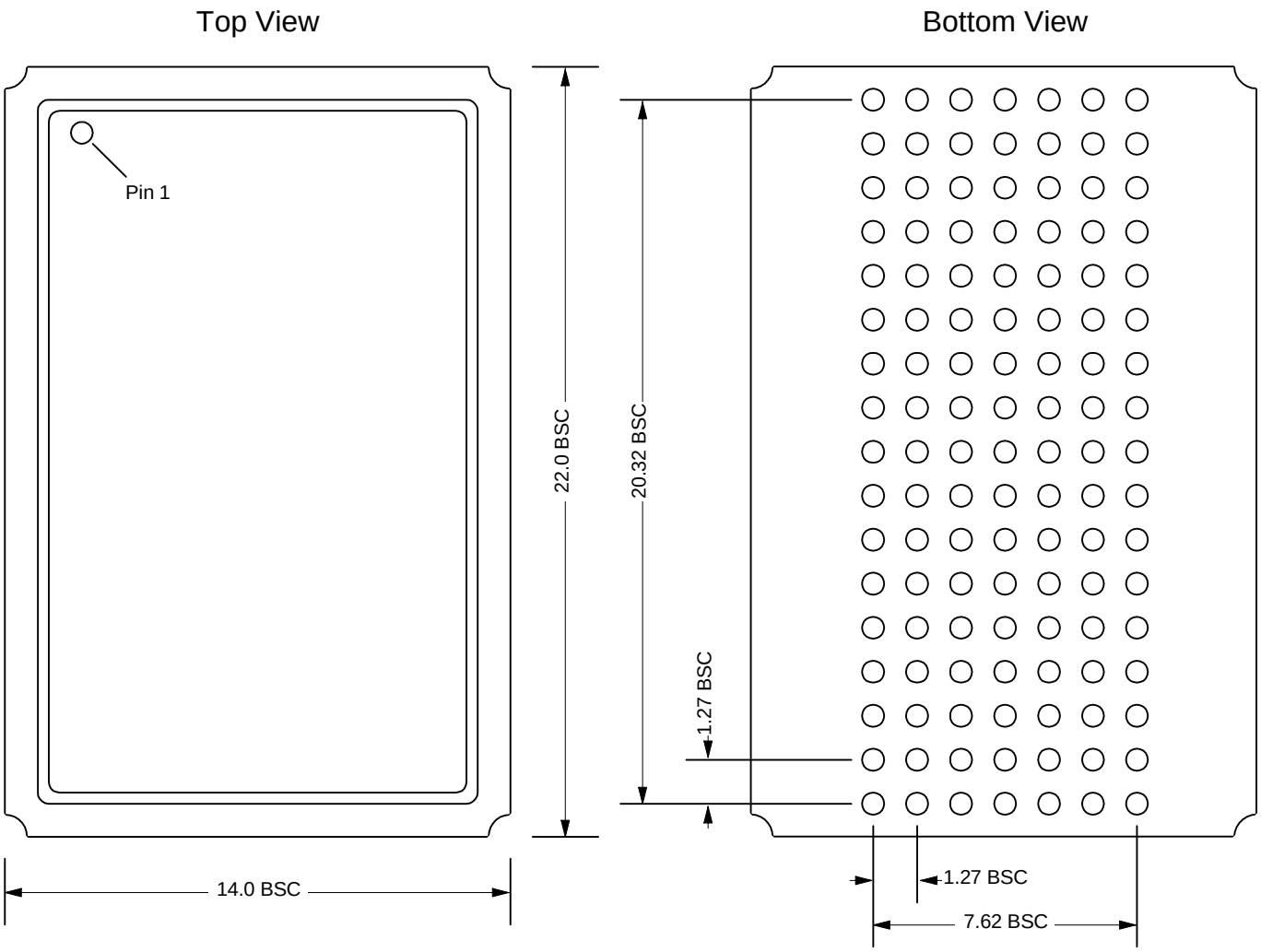
Mechanical Drawings

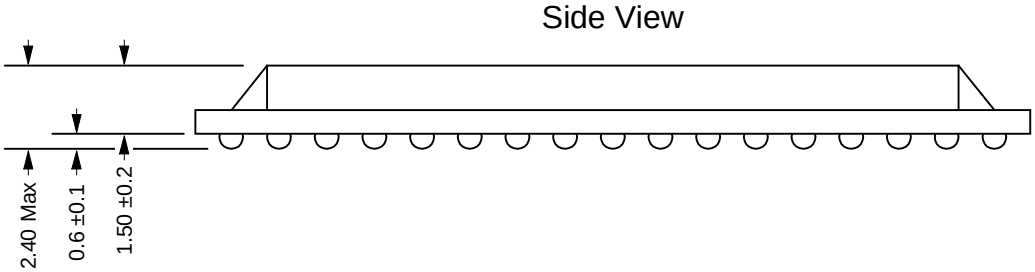
Package Dimensions (100-pin TQFP)



All dimensions in millimeters
Conforms to JEDEC MS-026/Variation BHA

Package Dimensions (119-bump PBGA)





All dimensions in millimeters
Conforms to JEDEC MS-028, variation AA

Revision Log

Revision	Date	Summary of Changes
1.0	10/11/01	Initial release.

Ordering Information

Part Number	Power Supply	Package	I/O Type	Maximum Operating Frequency (MHz)
SS2625Q-6	3.3V	100-pin TQFP	LVTTL, 2.5V	166
SS2625Q-7.5	3.3V	100-pin TQFP	LVTTL, 2.5V	133
SS2625Q-10	3.3V	100-pin TQFP	LVTTL, 2.5V	100
SS2625B-6	3.3V	119-ball PBGA	LVTTL, 2.5V	166
SS2625B-7.5	3.3V	119-ball PBGA	LVTTL, 2.5V	133
SS2625B-10	3.3V	119-ball PBGA	LVTTL, 2.5V	100
SS2625Q1-6	2.5V	100-pin TQFP	2.5V	166
SS2625Q1-7.5	2.5V	100-pin TQFP	2.5V	133
SS2625Q1-10	2.5V	100-pin TQFP	2.5V	100
SS2625B1-6	2.5V	119-ball PBGA	2.5V	166
SS2625B1-7.5	2.5V	119-ball PBGA	2.5V	133
SS2625B1-10	2.5V	119-ball PBGA	2.5V	100

Enhanced Memory Systems Inc., 1850 Ramtron Dr., Colo Spgs, CO 80921
PHONE: (800) 545-DRAM; FAX: (719) 488-9095; http://www.edram.com