

2N6975, 2N6976, 2N6977, 2N6978

April 1995

5A, 400V and 500V N-Channel IGBTs

Features

- 5A, 400V and 500V
- V_{CE(ON)} 2V
- T_{FI} 1μs, 0.5μs
- · Low On-State Voltage
- · Fast Switching Speeds
- · High Input Impedance

Applications

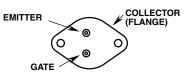
- · Power Supplies
- Motor Drives
- Protection Circuits

Description

The 2N6975, 2N6976, 2N6977 and the 2N6978 are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high-voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low-power integrated circuits.

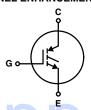
Package

JEDEC TO-204AA BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
2N6975	TO-204AA	
2N6976	TO-204AA	
2N6977	TO-204AA	
2N6978	TO-204AA	

NOTE: When ordering, use the entire part number.

Absolute Maximum Ratings $T_C = +25$ °C, Unless Otherwise Specified.

	2N6975/2N6977 (Note 1)	2N6976/2N6978 (Note 1)	UNITS
Collector-Emitter Voltage	400	500	V
Collector-Gate Voltage ($R_{GE} = 1M\Omega$) V_{CGR}	400	500	V
Reverse Collector-Emitter Voltage	5	5	V
Gate-Emitter VoltageV _{GE}	±20	±20	V
Collector Current Continuous	5	5	Α
Collector Current Pulsed	10	10	Α
Power Dissipation Total at $T_C = +25^{\circ}C$ P_D	100	100	W
Power Dissipation Derating T _C > +25°C	0.8	0.8	W/°C
Operating and Storage Junction Temperature Range	-55 to +150	-55 to +150	°C

1. JEDEC registered value.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641	
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690	
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606	
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951	
4,969,027								

Specifications 2N6975, 2N6976, 2N6977, 2N6978

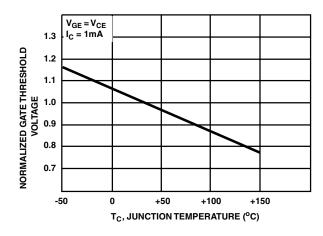
$\textbf{Electrical Specifications} \hspace{0.5cm} \textbf{T}_{C} = +25 \text{\odot}^{o}\text{C}, \, \textbf{Unless Otherwise Specified}$

			LIMITS				
	SYMBOL		2N6975	/2N6977	2N6976/2N6978		LIMIT
PARAMETERS		TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT S
Collector-Emitter Breakdown Voltage	BV _{CES}	I _C = 1 mA, V _{GE} = 0	400 (Note 1)	-∞	500 (Note 1)	-	V
Gate Threshold Voltage	V _{GE(TH)}	$V_{GE} = V_{CE}$, $I_C = 1mA$	2∞ (Note 1)	4.5 (Note 1)	2 (Note 1)	4.5∞ (Note 1)	V
Zero Gate Voltage Collector Current	I _{CES}	V _{CE} = 400V	-	250 (Note 1)	-	-	μА
		V _{CE} = 500V	-	-	-	250 (Note 1)	μА
		T _C = +125°C	-	-	-	-	μΑ
		V _{CE} = 400V	-	∞1000 (Note 1)	-	-	μА
		V _{CE} = 500V	-	-	-	1000 (Note 1)	μА
Gate-Emitter Leakage Current	I _{GES}	$V_{GE} = \pm 20V, V_{CE} = 0V$	-	100 (Note 1)	-	100 (Note 1)	ns
Reverse Collector-Emitter Leakage Current	I _{ECS}	$R_{GE} = 0\Omega$, $V_{EC} = 5V$	-	5 (Note 1)	-	5 (Note 1)	mA
Collector-Emitter On Voltage	V _{CE(ON)}	I _C = 5A, V _{GE} = 10V	-	2 (Note 1)	-	2 (Note 1)	V
		I _C = 10A, V _{GE} = 20V	-	2.5	-	2.5	٧
Gate-Emitter Plateau Voltage	V _{GEP}	I _C = 5A, V _{CE} = 10V	3.4 (Note 1)	6.8 (Note 1)	3.4 (Note 1)	6.8 (Note 1)	V
On-State Gate Charge	Q _{G(ON)}	I _C = 5A, V _{CE} = 10V	12 (Note 1)	25 (Note 1)	12 (Note 1)	25 (Note 1)	nC
Turn-On Delay Time	t _{D(ON)}	I _C = 5A	50 Max		•	ns	
Rise Time	t _R	V _{CE(CLP)} = 300V L = 50μH		50 Max			ns
Turn-Off Delay Time	t _{D(ON)}	$T_{J} = +125^{\circ}C$ $V_{GE} = 10V$ $R_{G} = 50\Omega$		400 Max (Note 1)			ns
Fall Time	t _{FI}	t _{FI}	2N6975 1000 Max 2N6976 (Note 1)			ns	
			2N6977 2N6978		500 Max (Note 1)		ns
Turn-Off Energy Loss per Cycle (Off Switching Dissipation-	$\begin{array}{c} W_{OFF} & I_{C} = 5A \\ V_{CE(CLP)} = 300V \\ L = 50 \mu H \\ T_{J} = +125^{\circ} C \\ V_{GE} = 10V \\ R_{G} = 50 \Omega \end{array}$	$V_{CE(CLP)} = 300V$	2N6975 2N6976		1000 Max (Note 1)		μJ
(Off Switching Dissipation= W _{OFF} x Frequency)		2N6977 2N6978		500 Max (Note 1)		μJ	
Thermal Resistance Junction-to-Case	$R_{ heta JC}$				25 te 1)		°C/V

NOTE:

1. JEDEC registered value.

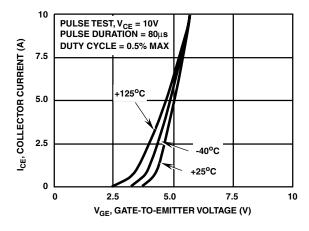
Typical Performance Curves



$$\begin{split} Z\theta_{JC}(t) &= r(t)R\theta_{JC} \\ D \text{ CURVES APPLY FOR POWER PULSE} \end{split}$$
EFFECTIVE TRANSIENT THERMAL IMPEDANCE (NORMALIZED) TRAIN SHOWN READ TIME AT t1 $T_{J(PEAK)} - T_C = P_{(PEAK)}Z\theta_{JC}(t)$ 10 D = 0.51.0 0.1 SINGLE PULSE 0.01 0.01 1.0 10 100 1000 t, TIME (ms)

FIGURE 1. TYPICAL NORMALIZED GATETHRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE FOR ALL TYPES

FIGURE 2. NORMALIZED THERMAL RESPONSE CHARACTERISTICS FOR ALL TYPES



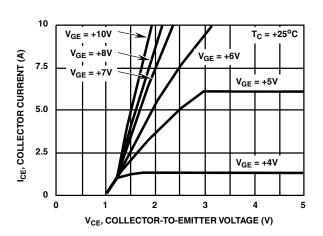


FIGURE 3. TYPICAL TRANSFER CHARACTERISTICS FOR ALL TYPES

FIGURE 4. TYPICAL SATURATION CHARACTERISTICS FOR ALL TYPES

Typical Performance Curves (Continued)

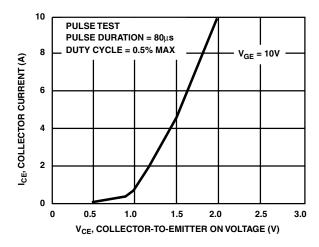


FIGURE 5. TYPICAL COLLECTOR-TO-EMITTER ON-VOLTAGE
AS A FUNCTION OF COLLECTOR CURRENT FOR
ALL TYPES

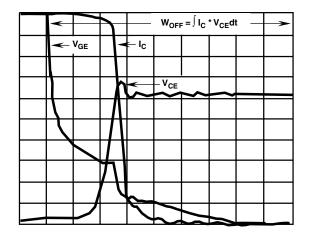


FIGURE 7. TYPICAL INDUCTIVE SWITCHING WAVEFORMS

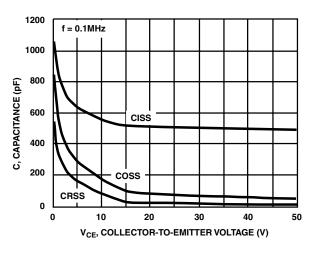
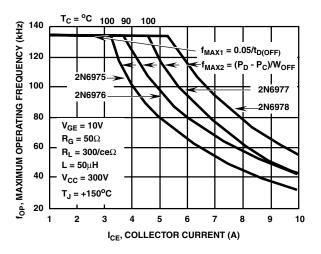


FIGURE 6. CAPACITANCE AS A FUNCTION OF COLLECTOR-TO-EMITTER VOLTAGE FOR ALL TYPES



P_D: ALLOWABLE DISSIPATION P_C: CONDUCTION DISSIPATION

FIGURE 8. MAXIMUM OPERATING FREQUENCY vs COLLECTOR CURRENT (TYPICAL)

Typical Performance Curves (Continued)

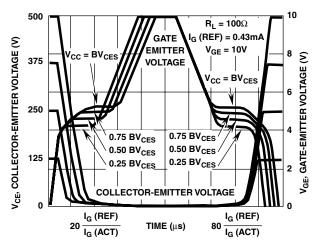


FIGURE 9. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

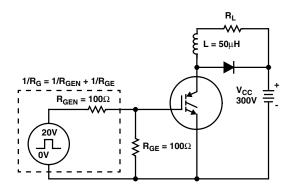


FIGURE 10. INDUCTIVE SWITCHING TEST CIRCUIT

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