8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89470 Series

MB89475/P475/PV470

■ DESCRIPTION

The MB89470 series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontroller contains a variety of peripheral functions such as 21-bit time-base timer, watch prescaler, PWC timer, PWM timer, 8/16-bit timer/counter, external interrupt 1 (edge), external interrupt 2 (level), 10-bit A/D converter, UART/SIO, buzzer, watchdog timer reset.

The MB89470 series is designed suitable for home appliance as well as in a wide range of applications for consumer product.

*: F²MC stands for FUJITSU Flexible Microcontroller.

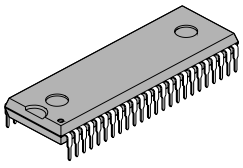
■ FEATURES

- Package used
  QFP package and SH-DIP package for MB89P475, MB89475
  MQFP package for MB89PV470
- High-speed operating capability at low voltage
- Minimum execution time: 0.32 µs/12.5MHz

(Continued)

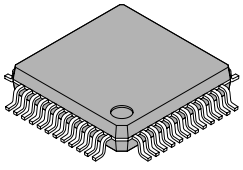
■ PACKAGE

48-pin Plastic SH-DIP



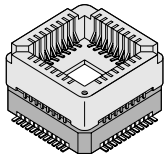
(DIP-48P-M01)

48-pin Plastic QFP



(FPT-48P-M05)

48-pin Ceramic MQFP



(MQP-48C-P01)

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- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- Six timers
  PWC timer (also usable as a interval timer)
  PWM timer
  8/16-bit timer/counter x 2
  21-bit timebase timer
  Watch prescaler
- Buzzer
  7 frequency types are selectable by software
- External interrupts
  Edge detection (Selectable edge) : 4 channels
  Low-level interrupt (Wake-up function) : 5 channels
- A/D converter (8 channels)
  10-bit successive approximation type
- UART/SIO
  Synchronous/asynchronous data transfer capable
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
  Subclock mode (for dual clock product)
  Watch mode (for dual clock product)
- Watch dog timer reset
- I/O ports: max. 39 channels

■ PRODUCT LINEUP

Part number / Parameter	MB89475	MB89P475	MB89PV470
Classification	Mass production products (mask ROM product)	OTP (read protection)	Piggy-back
ROM size	16K x 8-bit (internal ROM)	16K x 8-bit (internal PROM, can be written to by FLASH programmer)	32K x 8-bit (external ROM)
RAM size	512 x 8 bits		1K × 8 bits
CPU functions	Number of instructions: : 136 Instruction bit length: : 8 bits Instruction length: : 1 to 3 bytes Data bit length: : 1, 8, 16 bits Minimum execution time: : 0.32 µs/12.5 MHz Minimum interrupt processing time: : 2.88 µs/12.5 MHz		
Ports	Output-only ports (N-channel open drain) : 7 pins Input-only ports : 3 pins (1 pin in product with dual clock) I/O ports (CMOS) : 29 pins Total : 39 pins		
21-Bit Time-base timer	Interrupt period (0.82ms, 3.3 ms, 26.2 ms, 419.4 ms) at 10 MHz Interrupt period (0.66ms, 2.6 ms, 21.0 ms, 335.5 ms) at 12.5 MHz		
Watchdog timer	Reset period (209.7 ms to 419.4 ms) at 10 MHz Reset period (167.8 ms to 335.5 ms) at 12.5 MHz		
Pulse width count timer	2 channels 8-bit one-shot timer operation (supports underflow output, operating clock period: 1, 4, 32 tinst, external) 8-bit reload timer operation (supports square wave output, operating clock period: 1, 4, 32 tinst, external) 8-bit pulse width measurement operation (supports continuous measurement, H width, L width, rising edge to rising edge, falling edge to falling edge measurement and both edge measurement)		
PWM timer	8-bit reload timer operation (supports square wave output, operating clock period: 1, 4, 32 tinst, external) 8-bit resolution PWM operation		
8/16-Bit timer/counter 1, 2	Can be operated either as a 2-channel 8-bit timer/counter (Timer 1 and Timer 2, each with its own independent operating clock cycle), or as one 16-bit timer/counter In Timer 1 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capable		
8/16-Bit timer/counter 3, 4	Can be operated either as a 2-channel 8-bit timer/counter (Timer 3 and Timer 4, each with its own independent operating clock cycle), or as one 16-bit timer/counter In Timer 3 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capable		
External interrupt	4 independent channels (selectable edge, interrupt vector, request flag) 5 channels (low level interrupt)		
A/D converter	10-bit resolution × 8 channels A/D conversion function (conversion time: 60 tinst) Supports repeated activation by internal clock.		
UART/SIO	Synchronous/asynchronous data transfer capable (Max. baud rate: 78.125 Kbps at 10 MHz) (7 and 8 bits with parity bit ; 8 and 9 bits without parity bit)		

Note : 1 tinst = one instruction cycle (execution time) which can be selected as 1/4, 1/8, 1/16, or 1/64 of main clock.

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Part number / Parameter	MB89475	MB89P475	MB89PV470
Buzzer output	7 frequency types ($F_{CH}/2^{12}$, $F_{CH}/2^{11}$, $F_{CH}/2^{10}$, $F_{CH}/2^{9}$, $F_{CL}/2^{5}$, $F_{CL}/2^{4}$, $F_{CL}/2^{3}$,) are selectable by software.		
Standby mode	Sleep mode, stop mode, subclock mode(dual clock product) and watch mode(dual clock product)		
Process	CMOS		
Operating Voltage	2.2V ~ 5.5V	3.5V ~ 5.5V	2.7V ~ 5.5V

■ PACKAGE AND CORRESPONDING PRODUCTS

Device / Package	MB89475	MB89P475	MB89PV470
DIP-48P-M01	O	O	X
FPT-48P-M05	O	O	X
MQP-48C-P01	X	X	O

O : Availabe
X : Not available

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- The stack area, etc., is set at the upper limit of the RAM.

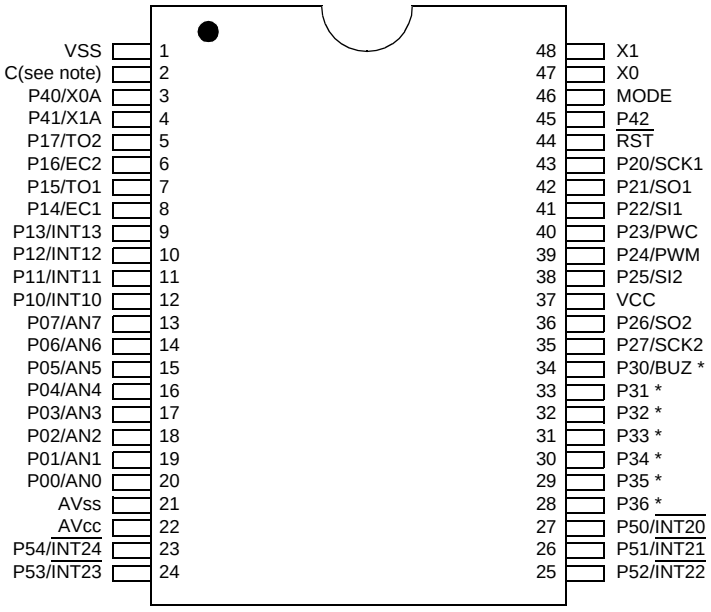
2. Current Consumption

- For the MB89PV470, add the current consumed by the EPROM mounted in the piggy-back socket.
- When operating at low speed, the current consumed by the one-time PROM product is greater than that for the mask ROM product. However, the current consumption are roughly the same in sleep or stop mode.
- For more information, see "■ Electrical Characteristics."

3. Oscillation stabilization time after power-on reset

- For MB89PV470, there is no power-on stabilization time after power-on reset
- For MB89P475, there is power-on stabilization time after power-on reset
- For MB89475, the power-on stabilization time can be select.
- For more information, refer to "■ Mask Option".

■ PIN ASSIGNMENT

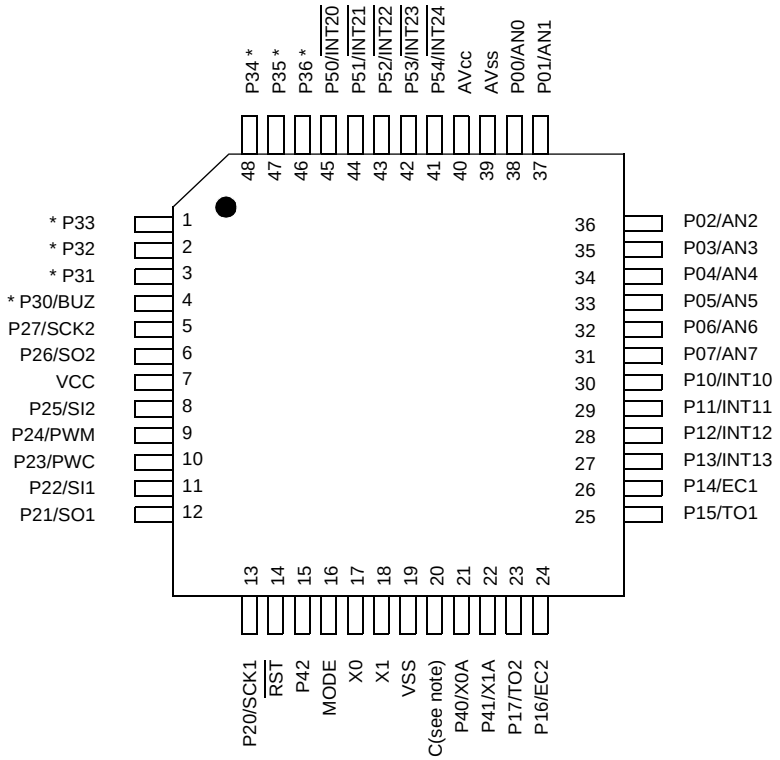


(DIP-48P-M01)

Note : For pin no. 2, connect this pin to an external 0.1µF capacitor to ground (for MB89P475 only). For MB89PV470 and MB89475, this pin should be left unconnected.

* High current drive type

(TOP VIEW)

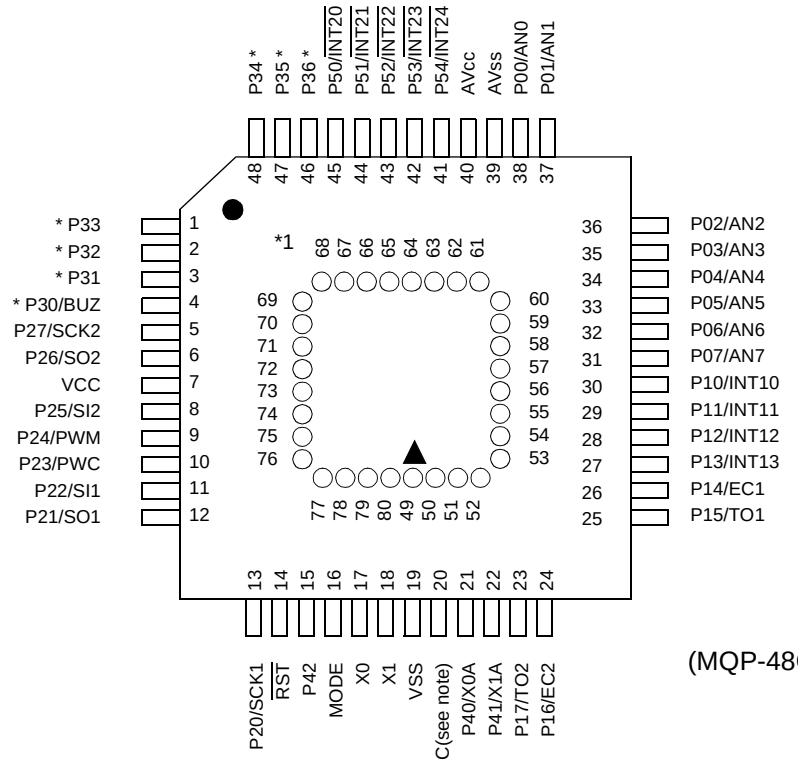


(FPT-48P-M05)

Note : For pin no. 20, connect this pin to an external 0.1µF capacitor to ground (for MB89P475only). For MB89PV470 and MB89475, this pin should be left unconnected.

* High current drive type

(TOP VIEW)



(MQP-48C-P01)

*1: Package upper-side pin assignment (MB89PV470 only)

Pin No.	Pin Symbol	Pin No.	Pin Symbol	Pin No.	Pin Symbol	Pin No.	Pin Symbol
49	Vpp	57	N.C.	65	O4	73	$\overline{OE}$
50	A12	58	A2	66	O5	74	N.C.
51	A7	59	A1	67	O6	75	A11
52	A6	60	A0	68	O7	76	A9
53	A5	61	O1	69	O8	77	A8
54	A4	62	O2	70	$\overline{CE}$	78	A13
55	A3	63	O3	71	A10	79	A14
56	N.C.	64	Vss	72	N.C.	80	Vcc

N.C.: As connected internally, do not use.
Note : Pin no. 20 should be left unconnected.

* High current drive type

■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit	Function
QFP/MQFP*2	SDIP*1			
17	47	X0	A	Connection pins for a crystal or other oscillator. An external clock can be connected to X0. In this case, leave X1 open.
18	48	X1		
16	46	MODE	B	Input pins for setting the memory access mode. Connect directly to V_{SS}.
14	44	$\overline{RST}$	C	Reset I/O pin. The pin is a N-ch open-drain type with pull-up resistor and a hysteresis input. The pin outputs a “L” level when an internal reset request is present. Inputting an “L” level initializes internal circuits.
38 - 31	20 - 13	P00/AN0 - P07/AN7	D	General-purpose I/O port. The pins are shared with the analog inputs for the A/D converter.
30 - 27	12 - 9	P10/INT10 - P13/INT13	E	General-purpose I/O port. A hysteresis input for INT10~13. The pin is shared with an external interrupt 1 input.
26	8	P14/EC1	E	General-purpose I/O port. A hysteresis input for EC1. The pin is shared with the 8/16 bit timer 1 input.
25	7	P15/TO1	F	General-purpose I/O port. The pin is shared with the output of 8/16-bit timer 1.
24	6	P16/EC2	E	General-purpose I/O port. A hysteresis input for EC2. The pin is shared with the 8/16 bit timer 2 input.
23	5	P17/TO2	F	General-purpose I/O port. The pin is shared with the output of 8/16-bit timer 2.
13	43	P20/SCK1	E	General-purpose I/O port. A hysteresis input for SCK1. The pin is shared with the clock I/O of UART/SIO 1.
12	42	P21/SO1	F	General-purpose I/O port. The pin is shared with the serial data output of UART/SIO 1.
11	41	P22/SI1	E	General-purpose I/O port. A hysteresis input for SI1. The pin is shared with the serial data input of UART/SIO 1.
10	40	P23/PWC	E	General-purpose I/O port. A hysteresis input for PWC. This pin is shared with PWC input.
9	39	P24/PWM	F	General-purpose input port. This pin is shared with PWM output.
8	38	P25/SI2	E	General-purpose I/O port. A hysteresis input for SI2. The pin is shared with the serial data input of UART/SIO 2.
6	36	P26/SO2	F	General-purpose I/O port. The pin is shared with the serial data output of UART/SIO 2.
5	35	P27/SCK2	E	General-purpose I/O port. A hysteresis input for SCK2. The pin is shared with the clock I/O of UART/SIO 2.

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Pin no.		Pin name	I/O circuit	Function
QFP/MQFP*2	SDIP*1			
4	34	P30/BUZ	G	N-channel open-drain output. The pin is shared with buzzer output.
3 - 1, 48 - 46	33 - 28	P31 - P36	G	N-channel open-drain output.
21	4	P40/X0A	H	General-purpose input port. (single clock system)
			A	Connection pins for a crystal or other oscillator. (dual clock system) An external clock can be connected to X0A. In this case, leave X1A open.
22	3	P41/X1A	H	General-purpose input port. (single clock system)
			A	Connection pins for a crystal or other oscillator. (dual clock system) An external clock can be connected to X0A. In this case, leave X1A open.
15	45	P42	H	General-purpose input port.
45 - 41	27 - 23	P50/$\overline{\text{INT20}}$ - P54/$\overline{\text{INT24}}$	E	General-purpose I/O port. A hysteresis input for $\overline{\text{INT20}}$~$\overline{\text{INT24}}$. The pin is shared with an external interrupt 2 input.
20	2	C	—	Capacitor connection pin *3
7	37	V_{CC}	—	Power supply pin (+5V).
19	1	V_{SS}	—	Power supply pin (GND).
40	22	AV_{CC}	—	A/D converter power supply pin.
39	21	AV_{SS}	—	A/D converter power supply pin. Use at the same voltage level as V_{SS}.

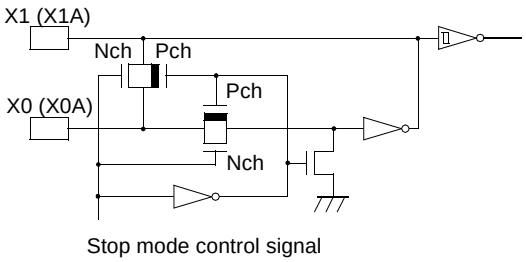
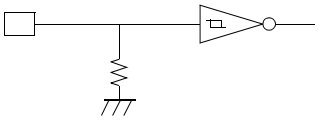
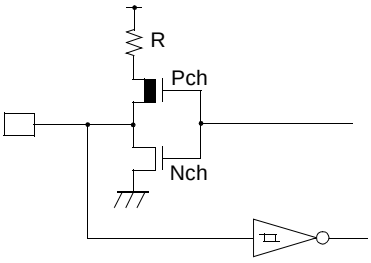
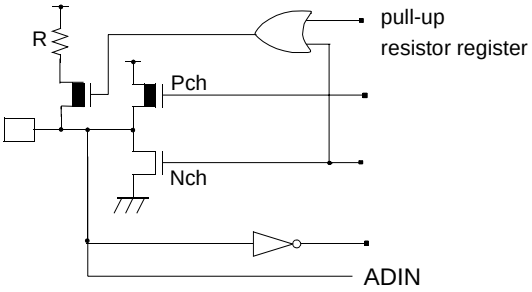
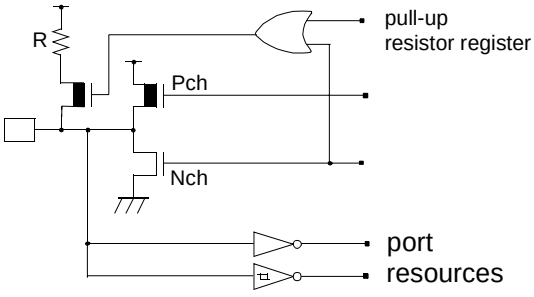
*1: DIP-48P-M01
*2: FPT-48P-M05 / MQP-48C-P01
*3: When MB89475 or MB89PV470 is used, this pin will become a N.C. pin without internal connection.
When MB89P475 is used, connect this pin to an external 0.1uF capacitor to ground.

• External EPROM Socket (MB89PV470 only)

Pin Number MQFP*1	Pin Name	I/O	Function
49	V_{pp}	O	“H” level output pin
50 51 52 53 54 55 58 59 60	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins.
61 62 63	O1 O2 O3	I	Data input pins.
64	V_{SS}	O	Power supply pin (GND).
65 66 67 68 69	O4 O5 O6 O7 O8	I	Data input pins.
70	$\overline{CE}$	O	Chip enable pin for the ROM. Outputs “H” in standby mode.
71	A10	O	Address output pin.
72	$\overline{OE}$	O	Output enable pin for the ROM. Always outputs “L”.
75 76 77 78 79	A11 A9 A8 A13 A14	O	Address output pins.
80	V_{CC}	O	Power supply pin for the EPROM.
56 57 72 74	N.C.	—	Internally connected pins. Always leave open.

*1: MQP-48C-P01

■ I/O CIRCUIT TYPE

Circuit Class	Circuit	Remarks
A		• Main and sub-clock circuits
B		• Hysteresis input • The pull-down resistor is approx. 50kΩ. (No pull-down resistor in MB89P475)
C		• The pull-up resistance (P-channel) is approx. 50 kΩ. • Hysteresis input
D		• CMOS output • CMOS input • Selectable pull-up resistor Approx. 50 kΩ
E		• CMOS output • CMOS input • Selectable pull-up resistor Approx. 50 kΩ

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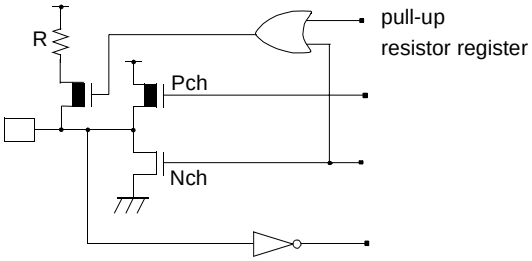
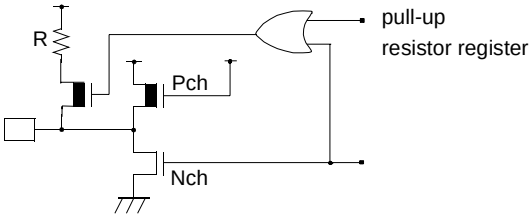
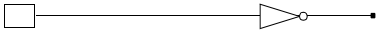
F		• CMOS output • CMOS input • Selectable pull-up resistor Approx. 50 kΩ
G		• N-channel open-drain output • Selectable pull-up resistor Approx. 50 kΩ
H		• CMOS input

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC}) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$ even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING OTPROM IN MB89P475 WITH SERIAL PROGRAMMER

1. Programming the OTPROM with serial programmer

- All OTP products can be programmed with serial programmer

2. Programming the OTPROM

- To program the OTPROM using EPROM programmer AF200 (manufacturer: Yokogawa Digital Computer Corp.).

  Inquiry : Yokogawa Digital Computer Corp. : TEL (81)-42-333-6224

- To program the OTPROM using FUJITSU MCU programmer MB91919-001.

  Inquiry : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65)-2810770

  FAX (65)-2810220

3. Programming Adaptor for OTPROM

- To program the OTPROM using EPROM programmer AF200, use the programming adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Compatible socker adaptor
DIP-48P-M01	N/A
FPT-48P-M05	T.B.D.

Inquiry : Sun Hayato Co., Ltd : TEL (81)-3-3986-0403

FAX (81)-3-5396-9106

- To program the OTPROM using FUJITSU MCU programmer MB91919-001, use the programming adapter listed below.

Package	Compatible socker adaptor
DIP-48P-M01	T.B.D.
FPT-48P-M05	T.B.D.

Inquiry : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65)-2810770

FAX (65)-2810220

4. OTPROM Content Protection

For product with OTPROM content protection feature (MB89P475-102, MB89P475-202), OTPROM content can be read using serial programmer if the OTPROM content protection mechanism is not activated.

One predefined area of the OTPROM ($FFFC_H$) is assigned to be used for preventing the read access of OTPROM content. If the protection code "00_H" is written in this address ($FFFC_H$), the OTPROM content cannot be read by any serial programmer.

Note: The program written into the OTPROM cannot be verified once the OTPROM protection code is written ("00_H" in $FFFC_H$). It is advised to write the OTPROM protection code at last.

5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

■ PROGRAMMING OTPROM IN MB89P475 WITH GENERAL PURPOSE EPROM PROGRAMMER

1. Programming OTPROM with general purpose EPROM programmmer

- Only products without protection feature (i.e. MB89P475-101 and MB89P475-201) can be programmed with general purpose EPROM programmer. Product with protection feature (i.e. MB89P475-102 and MB89P475-202) cannot be programmed with general purpose programmer.

2. ROM Writer Adapters and Recommended ROM Writers

- The following shows ROM writer adapters and recommended ROM writers.

Package name	Applicable adapter model	Recommended writer maker and writer
	San Hayato Co., Ltd.	Minato electronics Co., Ltd.
		MODEL1890A
DIP-64P-M01	N/A	N/A
FPT-48P-M05	T.B.D	Under evaluation

- Contact information

  Sun Hayato Co., Ltd.: Phone 03-3986-0403

  Minato electronics Co., Ltd.: Phone 045-591-5611

3. Writing data to the EPROM

(1) Set the EPROM writer for the CU50-OTP (device code: cdB6DC).

(2) Load the program data to the EPROM writer.

(3) Write data using the EPROM writer.

4. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TVM

2. Programming Socket Adapter

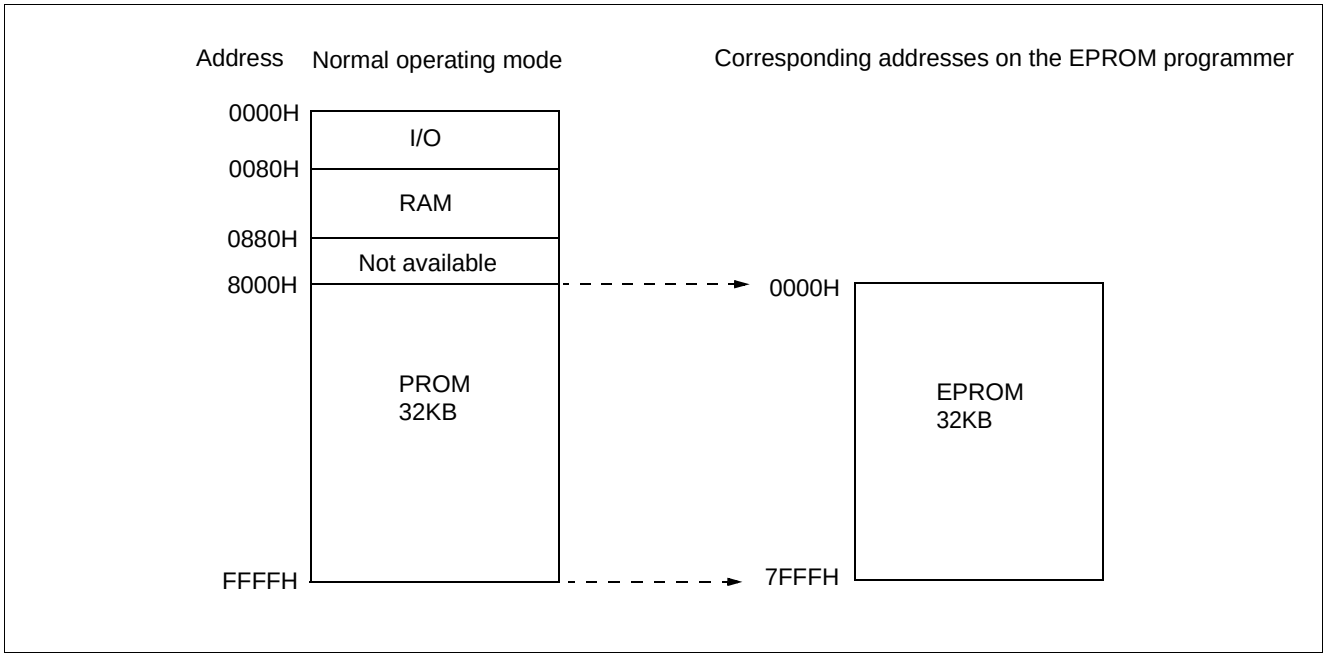
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Square)	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3986-0403

3. Memory Space

Memory space in each mode is diagrammed below.



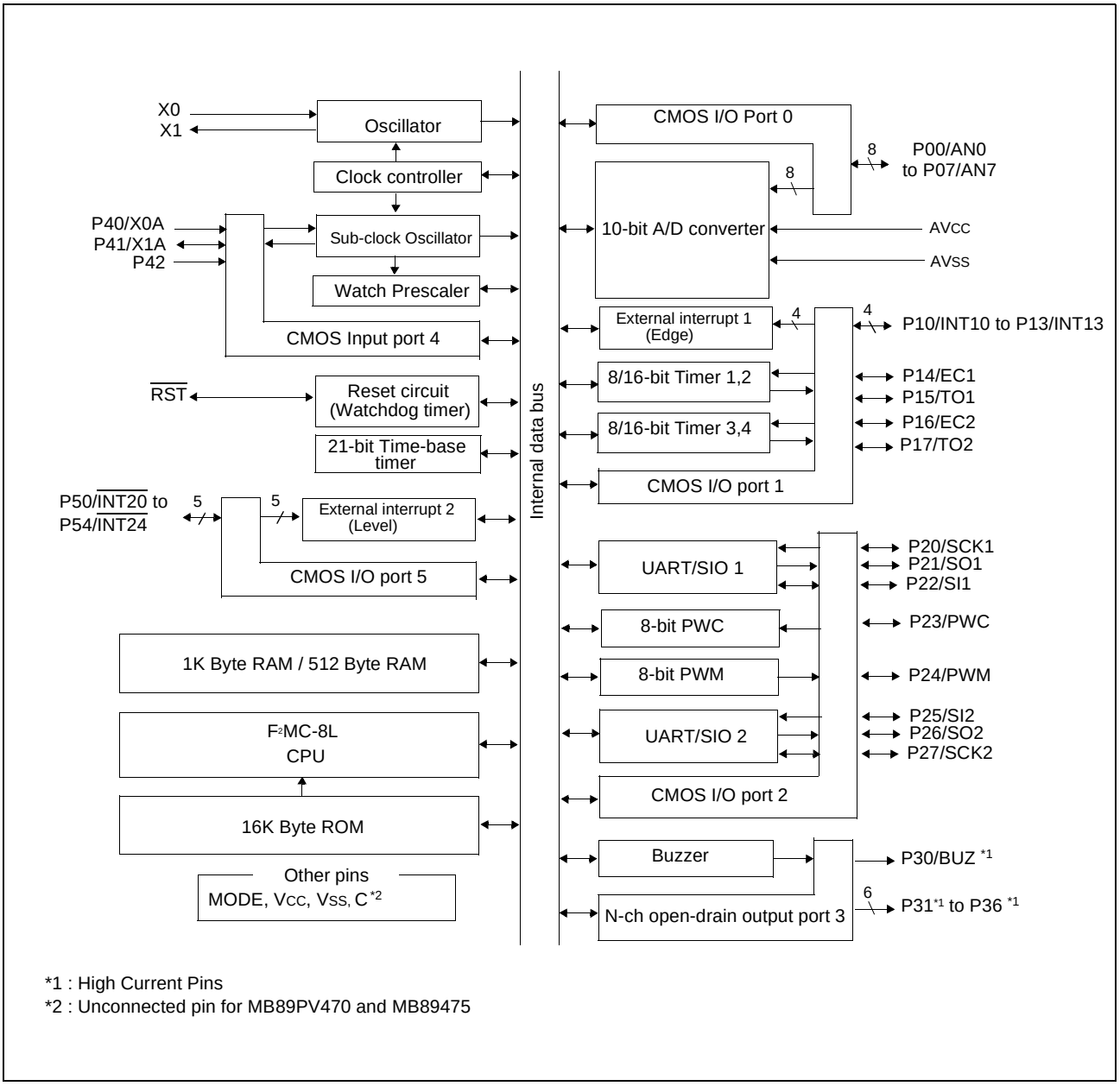
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ Block Diagram



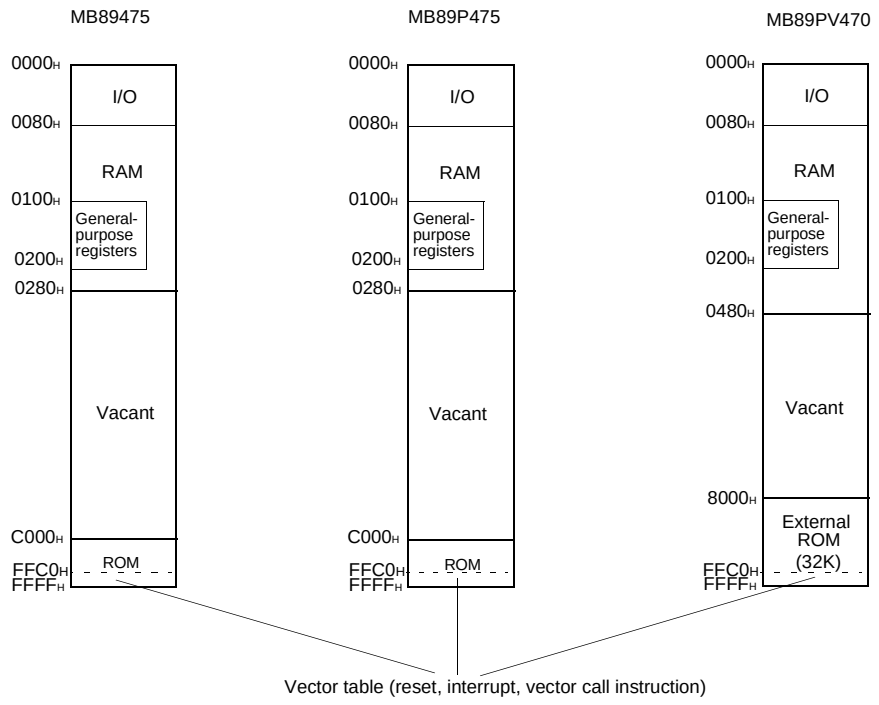
*1 : High Current Pins
*2 : Unconnected pin for MB89PV470 and MB89475

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89470 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89470 series is structured as illustrated below.

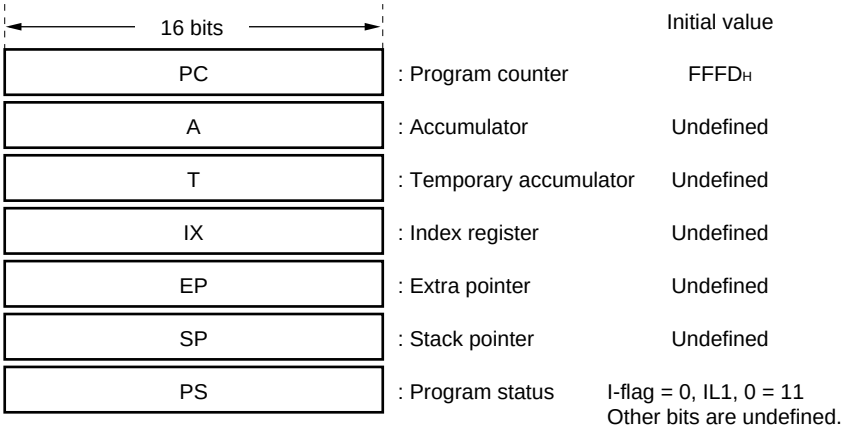
Memory Space



2. Registers

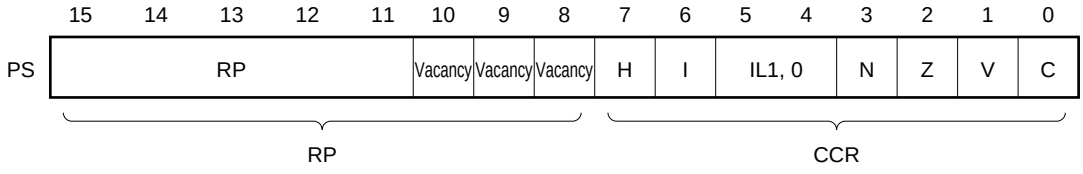
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



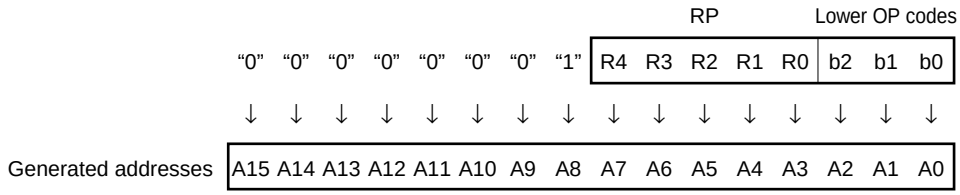
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

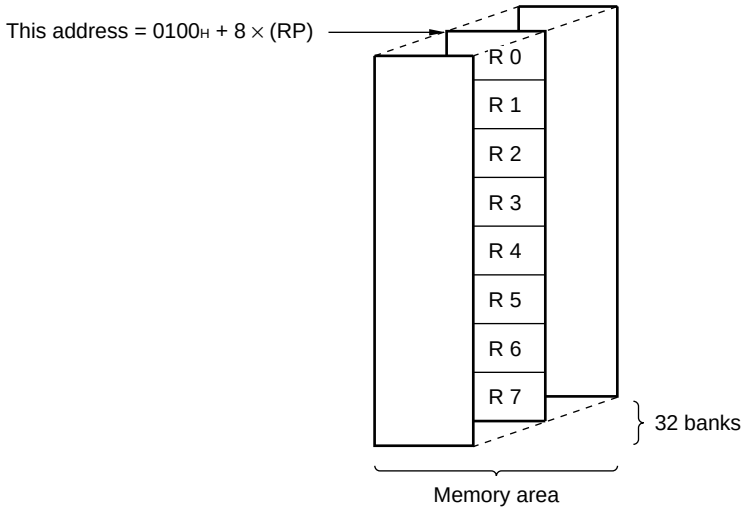
C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit resister for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB89470 series. The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration



■ I/O MAP

Address	Register name	Register Description	Read/Write	Initial value
00H	PDR0	Port 0 data register	R/W	XXXXXXXXB
01H	DDR0	Port 0 data direction register	W*	00000000B
02H	PDR1	Port 1 data register	R/W	XXXXXXXXB
03H	DDR1	Port 1 data direction register	W*	00000000B
04H	PDR2	Port 2 data register	R/W	00000000B
05H	(Reserved)			
06H	DDR2	Port 2 data direction register	R/W	00000000B
07H	SYCC	System clock control register	R/W	-XXMM-00B
08H	STBC	Standby control register	R/W	0001XXXXB
09H	WDTC	Watchdog timer control register	W*	0---XXXXB
0AH	TBTC	Timebase timer control register	R/W	00---000B
0BH	WPCR	Watch prescaler control register	R/W	00--0000B
0CH	PDR3	Port 3 data register	R/W	-1111111B
0DH	PDR4	Port 4 data register	R	-----XXXB
0EH	RSFR	Reset flag register	R	XXXX----B
0FH	BUZR	Buzzer register	R/W	-----000B
10H	PDR5	Port 5 data register	R/W	---XXXXXB
11H	DDR5	Port 5 data direction register	R/W	---00000B
12H to 13H	(Reserved)			
14H	T4CR	Timer 4 control register	R/W	000000X0B
15H	T3CR	Timer 3 control register	R/W	000000X0B
16H	T4DR	Timer 4 data register	R/W	XXXXXXXXB
17H	T3DR	Timer 3 data register	R/W	XXXXXXXXB
18H	T2CR	Timer 2 control register	R/W	000000X0B
19H	T1CR	Timer 1 control register	R/W	000000X0B
1AH	T2DR	Timer 2 data register	R/W	XXXXXXXXB
1BH	T1DR	Timer 1 data register	R/W	XXXXXXXXB
1CH to 1FH	(Reserved)			
20H	ADC1	A/D control register 1	R/W	-00000X0B
21H	ADC2	A/D control register 2	R/W	-0000001B
22H	ADDH	A/D data register (Upper byte)	R	------XXB
23H	ADDL	A/D data register (Lower byte)	R	XXXXXXXXB
24H	ADER	A/D input enable register	R/W	11111111B
25H	(Reserved)			
26H	SMC11	UART/SIO serial mode control register 11	R/W	00000000B
27H	SMC12	UART/SIO serial mode control register 12	R/W	00000000B
28H	SSD1	UART/SIO serial status and data register 1	R	00001---B
29H	SIDR1/SODR1	UART/SIO serial data register 1	R/W *	XXXXXXXXB
2AH	SRC1	UART/SIO serial rate control register 1	R/W	XXXXXXXXB

(Continued)

(Continued)

Address	Register name	Register Description	Read/Write	Initial value
2B$_H$	SMC21	UART serial mode control register 21	R/W	00000000$_B$
2C$_H$	SMC22	UART serial mode control register 22	R/W	00000000$_B$
2D$_H$	SSD2	UART serial status and data register 2	R	00001---$_B$
2E$_H$	SIDR2/SODR2	UART serial data register 2	R/W *	XXXXXXXX$_B$
2F$_H$	SRC2	UART serial rate control register 2	R/W	XXXXXXXX$_B$
30$_H$	EIC1	External interrupt 1 control register 1	R/W	00000000$_B$
31$_H$	EIC2	External interrupt 1 control register 2	R/W	00000000$_B$
32$_H$	EIE2	External interrupt 2 enable register	R/W	---00000$_B$
33$_H$	EIF2	External interrupt 2 flag register	R/W	-------0$_B$
34$_H$	PCR1	PWC control register 1	R/W	0-0--000$_B$
35$_H$	PCR2	PWC control register 2	R/W	00000000$_B$
36$_H$	PLBR	PWC reload buffer register	R/W	XXXXXXXX$_B$
37$_H$	(Reserved)			
38$_H$	CNTR	PWM timer control register	R/W	0-00000000$_B$
39$_H$	COMR	PWM timer compare register	W*	XXXXXXXX$_B$
3A$_H$ to 6F$_H$	(Reserved)			
70$_H$	PURC0	Port 0 pull up resistor control register	R/W	11111111$_B$
71$_H$	PURC1	Port 1 pull up resistor control register	R/W	11111111$_B$
72$_H$	PURC2	Port 2 pull up resistor control register	R/W	11111111$_B$
73$_H$	PURC3	Port 3 pull up resistor control register	R/W	-1111111$_B$
74$_H$	(Reserved)			
75$_H$	PURC5	Port 5 pull up resistor control register	R/W	---1111$_B$
76$_H$ to 7A$_H$	(Reserved)			
7B$_H$	ILR1	Interrupt level setting register 1	W*	11111111$_B$
7C$_H$	ILR2	Interrupt level setting register 2	W*	11111111$_B$
7D$_H$	ILR3	Interrupt level setting register 3	W*	11111111$_B$
7E$_H$	ILR4	Interrupt level setting register 4	W*	11111111$_B$
7F$_H$	(Reserved)			

* Bit manipulation instruction cannot be used.

● **Read/write access symbols**

R/W : Readable and writable
R : Read-only
W : Write-only

● **Initial value symbols**

0: The initial value of this bit is “0”.
1: The initial value of this bit is “1”.
X: The initial value of this bit is undefined.
- : Unused bit.
M: The initial value of this bit is determined by mask option.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	AV_{CC} must not exceed V_{CC}
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks	
		Min.	Max.			
Power supply voltage	V_{CC} AV_{CC}	2.2*	5.5	V	Operation assurance range	MB89475
		3.5*	5.5	V	Operation assurance range	MB89P475
		2.7*	5.5	V	Operation assurance range	MB89PV470
		1.5	5.5	V	Retains the RAM state in stop mode	
Operating temperature	T_A	–40	+85	°C		

* : These values depend on the operating conditions and the analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics."

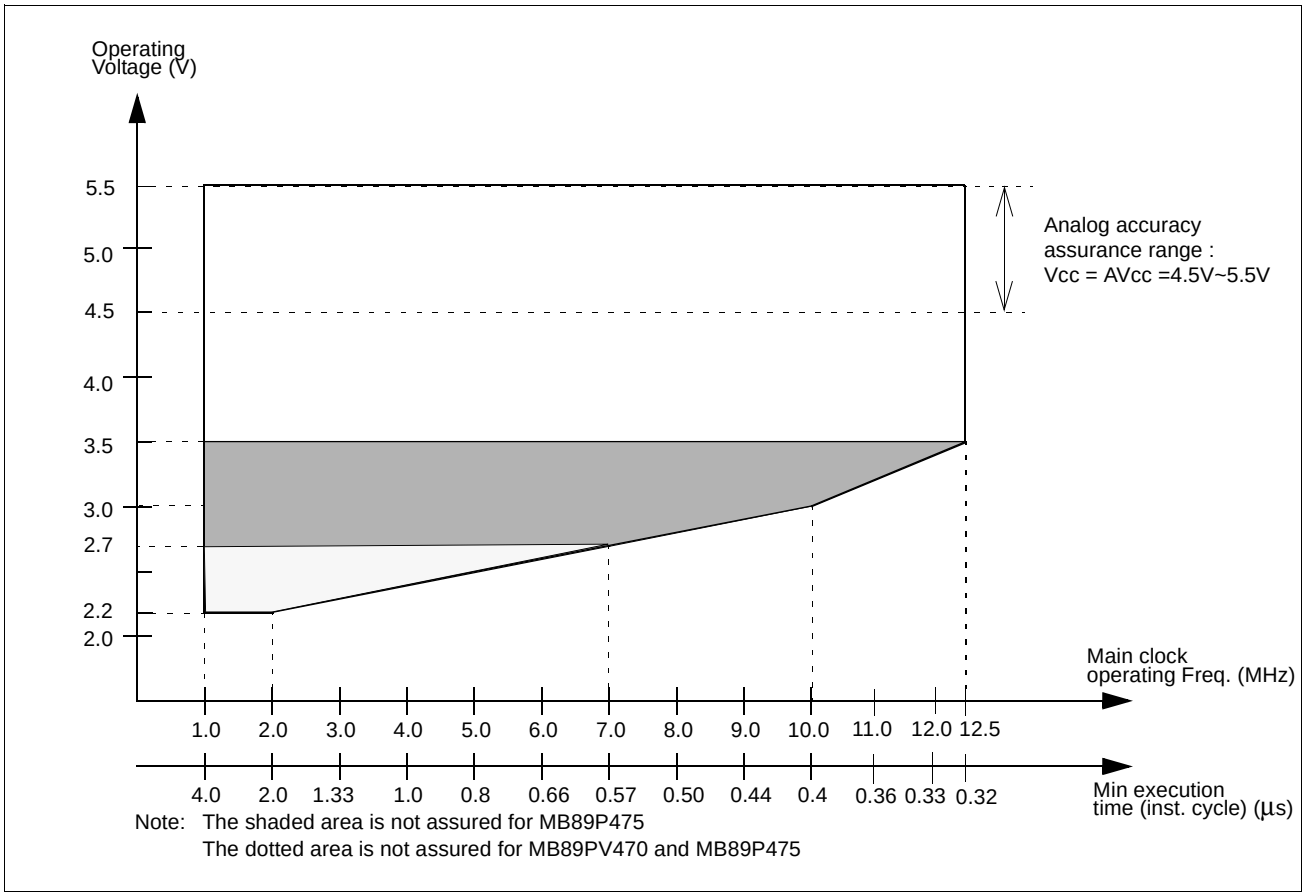


Figure 1 Operating Voltage vs. Main Clock Operating Frequency

Figure 1 indicate the operating frequency of the external oscillator at an instruction cycle of 4/F_{CH}.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

3. DC Characteristics

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P40 ~ P42, P50 ~ P54	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MODE, EC1, EC2, SCK1, SI1, SCK2, SI2, PWC, INT10 ~ INT13, INT20 ~ INT24	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P40 ~ P42, P50 ~ P54	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MODE, EC1, EC2, SCK1, SI1, SCK2, SI2, PWC, INT10 ~ INT13, INT20 ~ INT24	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P30 ~ P36	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P50 ~ P54	I_{OH} = –2.0mA	4.0	—	—	V	
"L" level output voltage	V_{OL1}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P50 ~ P54, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P30 ~ P36	I_{OL} = 12.0 mA	—	—	0.4	V	
Input leakage current	I_{LI}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P50 ~ P54	0.45 V < V_I < V_{CC}	-5	—	+5	µA	Without pull-up Resister
Open drain output leakage current	I_{LOD}	P30 ~ P36	0.45 V < V_I < V_{CC}	-5	—	+5	µA	
Pull-down resistance	R_{DOWN}	MODE	V_I = V_{CC}	25	50	100	kΩ	Except MB89P475
Pull-up resistance	R_{PULL}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P30 ~ P36, P50 ~ P54, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	When pull-up resistor is selected (except $\overline{RST}$)

(Continued)

(Continued)

$AV_{CC} = V_{CC} = 5.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current	I_{CC1}	V_{CC}	F_{CH} = 10.0MHz t_{inst} = 0.4 µs Main clock run mode	—	8	13	mA	
	I_{CC2}		F_{CH} = 10.0MHz t_{inst} = 6.4 µs Main clock run mode	—	0.7	3	mA	
	I_{CCS1}		F_{CH} = 10.0MHz t_{inst} = 0.4 µs Main clock sleep mode	—	2.5	5	mA	
	I_{CCS2}		F_{CH} = 10.0MHz t_{inst} = 6.4 µs Main clock sleep mode	—	0.8	2	mA	
	I_{CCL}		F_{CL} = 32.768kHz Subclock mode	—	50	85	µA	MB89PV470 MB89475
				—	350	785	µA	MB89P475
	I_{CCLS}		F_{CL} = 32.768kHz Subclock sleep mode	—	15	30	µA	MB89PV470 MB89475
				—	19	36	µA	MB89P475
	I_{CCT}		F_{CL} = 32.768kHz • Watch mode	—	1.6	15	µA	MB89PV470 MB89475
			• Main clock stop mode	—	5.6	21	µA	MB89P475
	I_{CCH}		Ta=+25°C Subclock stop mode		3	10	µA	
	I_A	AV_{cc}	F_{CH}=10MHz	—	2.8	5.5	mA	A/D converting, MB89PV470. MB89475
				—	2.3	6	mA	MB89P475
	I_{AH}		Ta=+25°C	—	1	5	µA	A/D stop
Input capacitance	C_{IN}	Other than V_{CC},V_{SS},AV_{CC},AV_{SS}	f=1MHz	—	10	—	pF	

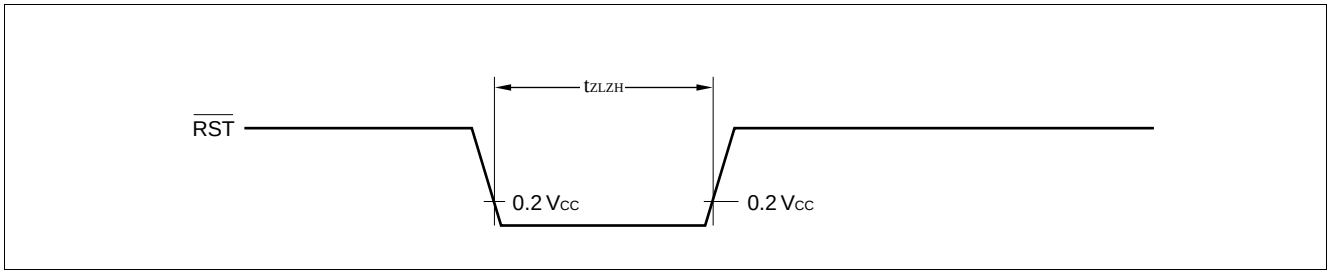
4. AC Characteristics

(1) Reset Timing

(V_{CC} = 5.0V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

Note: t_{HCYL} is the oscillation cycle (1/F_C) to input to the X0 pin.
The MCU operation is not guaranteed when the "L" pulse width is shorter than t_{ZLZH}.

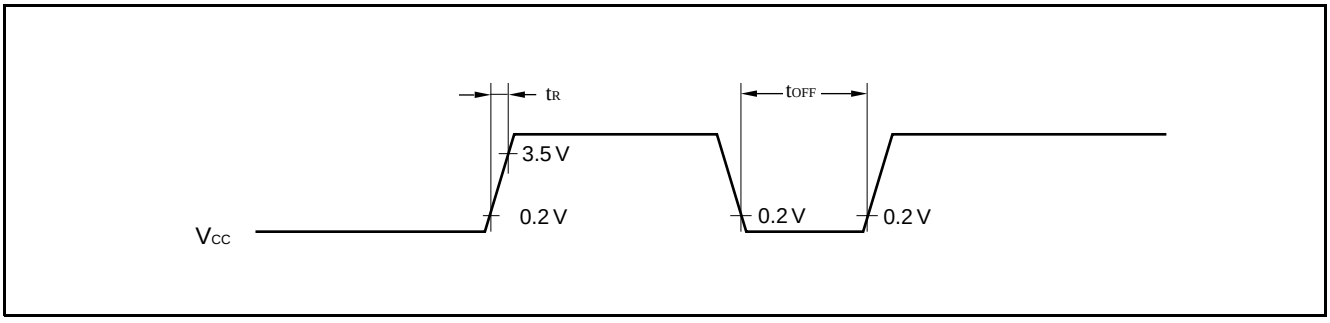


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
Rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

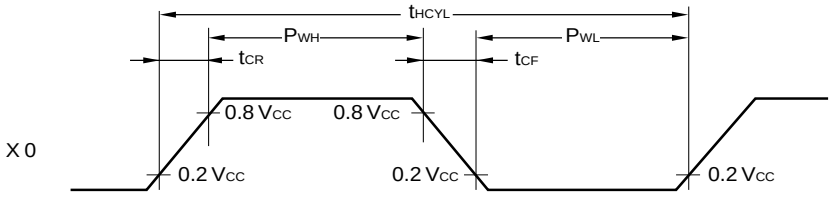


(3) Clock Timing

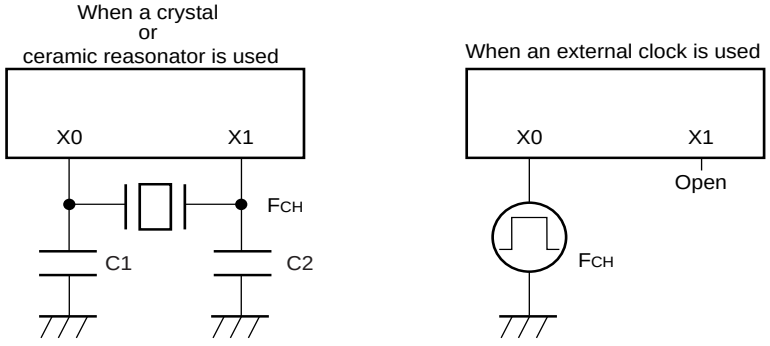
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	1	—	12.5	MHz	
	F_{CL}	X0A, X1A	—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1	80	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0	20	—	—	ns	External clock
	P_{WHL} P_{WLL}	X0A	—	15.2	—	µs	
Input clock rising/falling time	t_{CR} t_{CF}	X0, X0A	—	—	10	ns	

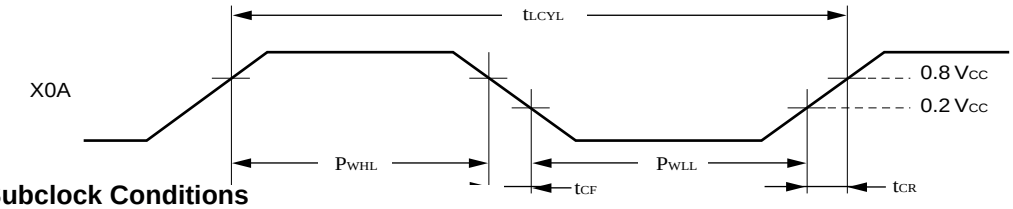
X0 and X1 Timing and Conditions



Main Clock Conditions

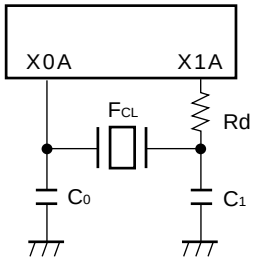


Subclock Timing and Conditions

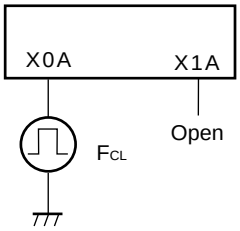


Subclock Conditions

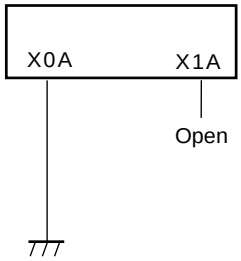
When a crystal or ceramic oscillator is used



When an external clock is used



When sub-clock is not used in dual clock product



(4) Instruction Cycle

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_{CH})t_{inst}$ = 0.32 µs when operating at F_{CH} = 12.5 MHz
		$2/F_{CL}$	µs	t_{inst} = 61.036 µs when operating at F_{CL} = 32.768 kHz

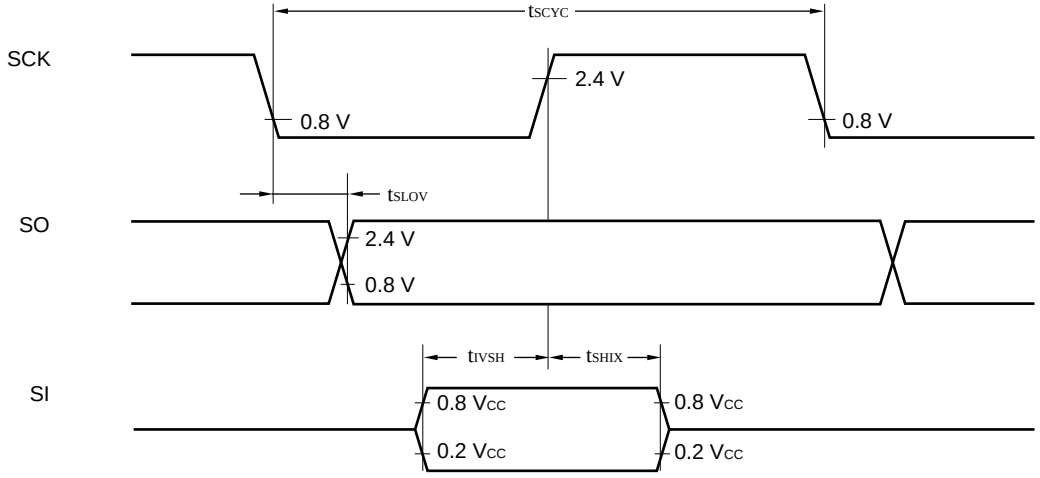
(5) Serial I/O Timing

(V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

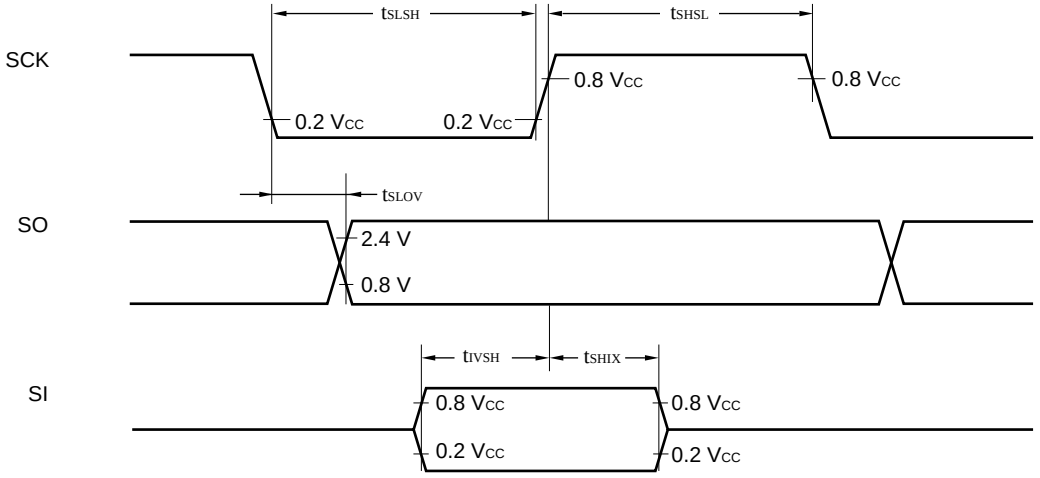
Parameter	Symbol	Pin	Condition	Value		Unit
				Min.	Max.	
Serial clock cycle time	t_{SCYC}	SCK1, SCK2	Internal shift clock mode	2 t_{inst}*	—	µs
SCK ↓ → SO time	t_{SLOV}	SCK1, SO1, SCK2, SO2,		–200	200	ns
Valid SI → SCK ↑	t_{IVSH}	SI1, SCK1, SI2, SCK2		1/2 t_{inst}*	—	ns
SCK ↑ → valid SI hold time	t_{SHIX}	SCK1, SI1, SCK2, SI2		1/2 t_{inst}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK1, SCK2	External shift clock mode	1 t_{inst}*	—	µs
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs
SCK ↓ → SO time	t_{SLOV}	SCK1, SO1, SCK2, SO2		0	200	ns
Valid SI → SCK ↑	t_{IVSH}	SI1, SCK1, SI2, SCK2		1/2 t_{inst}*	—	ns
SCK ↑ → valid SI hold time	t_{SHIX}	SCK1, SI1, SCK2, SI2		1/2 t_{inst}*	—	ns

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Clock Operation



External Clock Operation

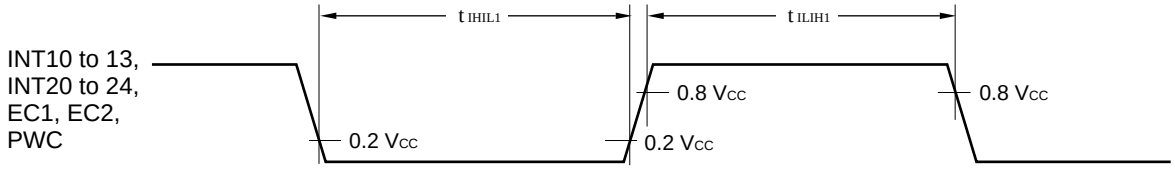


(6) Peripheral Input Timing

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	INT10 ~ 13, $\overline{INT20}$ ~ INT24, EC1, EC2, PWC	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

(1) A/D Converter Electrical Characteristics

(AV_{CC} = V_{CC} = 4.5 V ~ 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

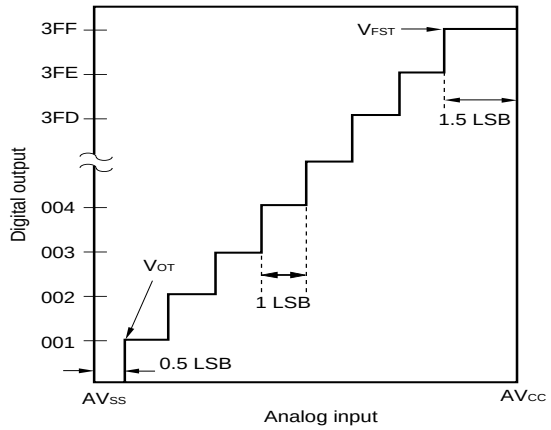
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	10	—	bit	
Total error			—	—	±3.0	LSB	
Linearity error			—	—	±2.5	LSB	
Differential linearity error			—	—	±1.9	LSB	
Zero transition voltage	V_{OT}		AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	LSB	
Full-scale transition voltage	V_{FST}		AV_{CC} – 3.5 LSB	AV_{CC} – 1.5 LSB	AV_{CC} + 0.5 LSB	LSB	
A/D mode conversion time	—		—	—	60 tinst*	µs	
Analog port input current	I_{AIN}	AN0 to AN3	—	—	10	µA	
Analog input voltage	V_{AIN}		AV_{SS}	—	AV_{CC}	V	

* : For information on t_{inst}, see "(4) Instruction Cycle" in "4. AC Characteristics".

(2) A/D Converter Glossary

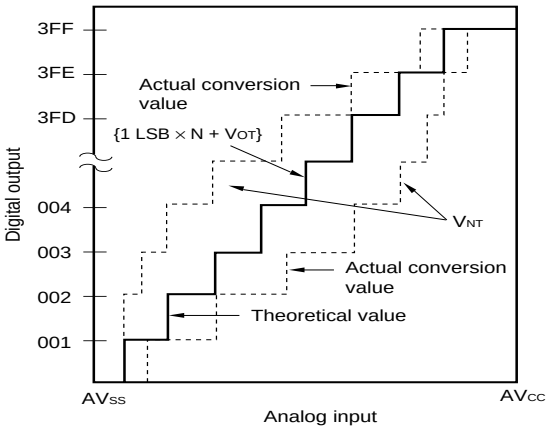
- Resolution
  Analog changes that are identifiable with the A/D converter
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1111" ↔ "11 1111 1110") from actual conversion characteristics.
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values.

Theoretical I/O characteristics



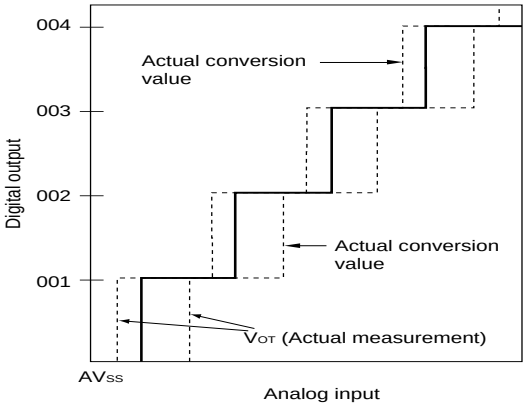
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ (\text{V})$$

Total error

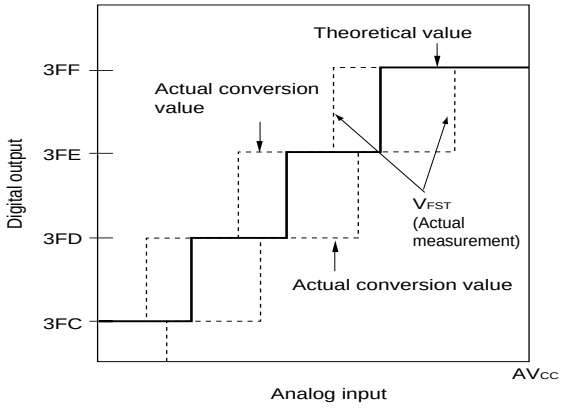


$$\text{Total error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

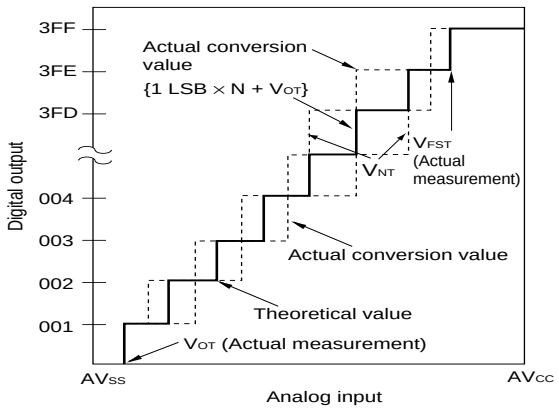
Zero transition error



Full-scale transition error

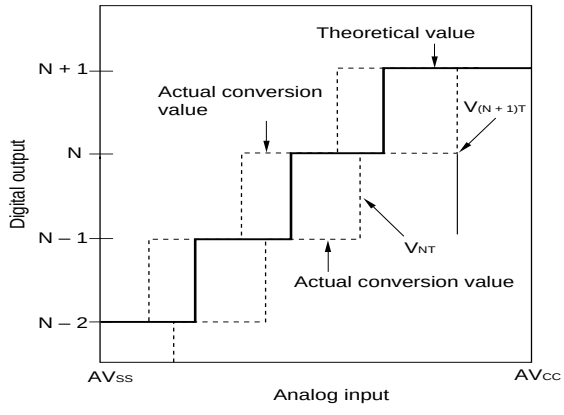


Linearity error



$$\text{Linearity error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

Differential linearity error



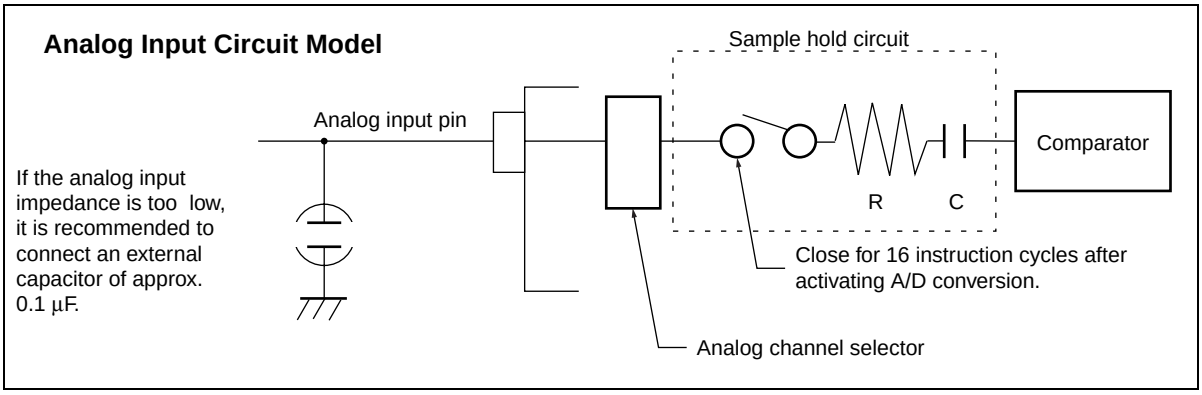
$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

(3) Notes on Using A/D Converter

- Input impedance of the analog input pins
  The A/D converter used for the MB89470 series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for 16 instruction cycles after activation A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low.

  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 µF for the analog input pin.



	MB89475 MB89PV470	MB89P475
R: analog input equivalent resistance	2.2 kΩ	2.6 kΩ
C: analog input equivalent capacitance	45 pF	28 pF

- Error
  The smaller the |AVR - AV_{SS}|, the greater the error would become relatively.

■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

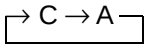
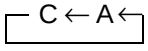
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1		–	–	–	+ + – +	03
ROLC A	2	1		–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR @A,IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

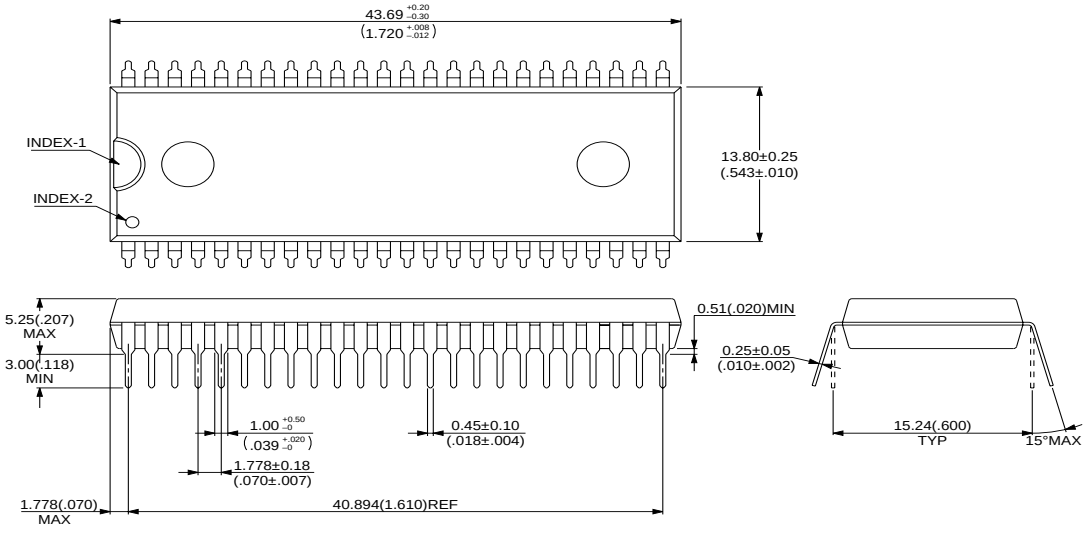
No.	Part number	MB89475	MB89P475	MB89PV470
	Specifying procedure	Specify when ordering masking	Setting not possible	Setting not possible
1	Selection of clock mode • Single clock mode • Dual clock mode	Selectable	101/102: Single clock 201/202: Dual clock	101: Single clock 201: Dual clock
2	Selection of OTPROM content protection feature • No protection feature • With protection feature	--	101/201: No protection 102/202: with protection	--
3	Selection of oscillation stabilization time (OSC) • The initial value of the oscillation stabilization time for the main clock can be set by selecting the values of the WTM1 and WTM0 bits on the right.	Selectable OSC 1 : $2^{14}/F_{CH}$ 2 : $2^{17}/F_{CH}$ 3 : $2^{18}/F_{CH}$	Fixed to oscillation stabilization time of $2^{18}/F_{CH}$	Fixed to oscillation stabilization time of $2^{18}/F_{CH}$
4	Selection of power-on stabilization time • Nil • $2^{17}/F_{CH}$	Selectable	Fixed to power-on stabilization time of $2^{17}/F_{CH}$	Fixed to nil

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89475PFV MB89P475PFV-101 MB89P475PFV-102 MB89P475PFV-201 MB89P475PFV-202	48-pin Plastic QFP (FPT-48P-M05)	101: Single clock, without content protection 102: Single clock, with content protection 201: Dual clock, without content protection 202: Dual clock, with content protection
MB89475P-SH MB89P475P-SH-101 MB89P475P-SH-102 MB89P475P-SH-201 MB89P475P-SH-202	48-pin Plastic SH-DIP (DIP-48P-M01)	
MB89PV470CF-101 MB89PV470CF-201	48-pin Ceramic MQFP (MQP-48C-P01)	

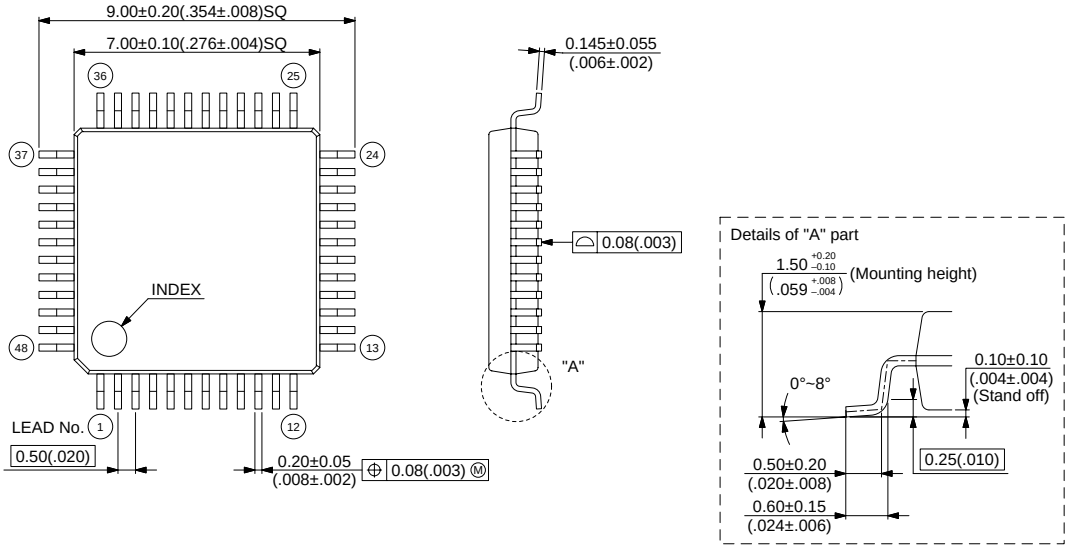
■ PACKAGE DIMENSIONS

48-pin Plastic SH-DIP
DIP-48P-M01



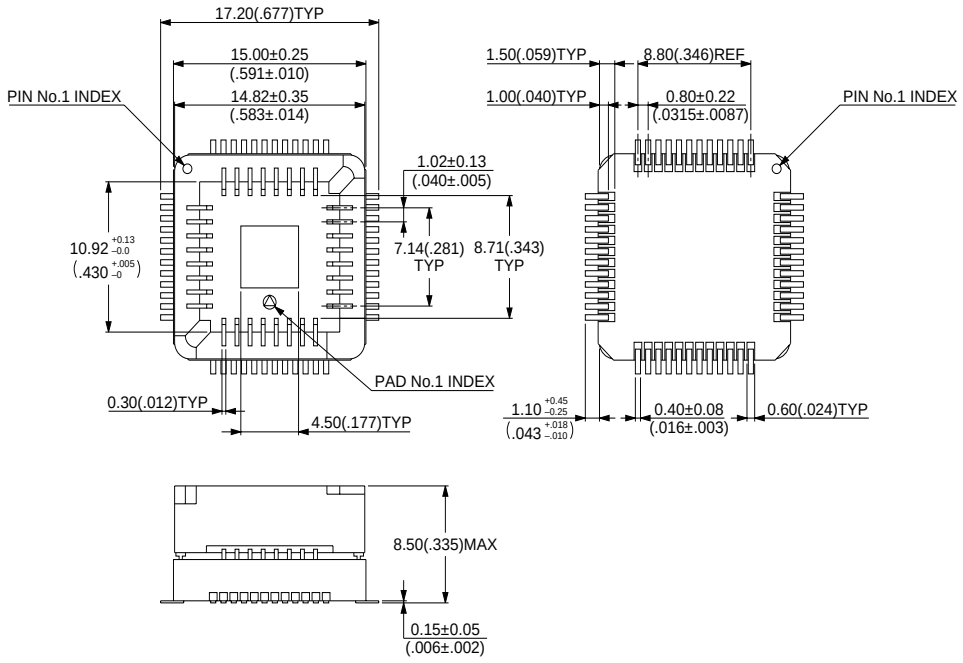
Dimensions in mm (inches)

48-pin Plastic LQFP
FPT-48P-M05



Dimensions in mm (inches)

48-pin Ceramic MQFP
MQP-48C-P01



Dimensions in mm (inches)

MEMO

FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-8588, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

http://www.fujitsu.co.jp/

North and South America
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, USA
Tel: (408) 922-9000
Fax: (408) 922-9179

Customer Response Center

Mon. - Fri.: 7 am - 5 pm (PST)

Tel: (800) 866-8608
Fax: (408) 922-9179

http://www.fujitsumicro.com/

Europe
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

http://www.fujitsu-ede.com/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

http://www.fmap.com.sg/