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# **TMS320VC5505 Evaluation Module (EVM)**

*Technical  
Reference*

Datasheet.Support



# **TMS320VC5505 Evaluation Module (EVM) Technical Reference**

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## **WARNING**

To minimize risk of electric shock hazard, use only the following power supply for the EVM module with Medical Development Applications: SL Power AULT Model MW173KB0503F01.

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## About This Manual

This document describes the board level operations of the TMS320VC5505 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320VC5505 Digital Signal Processor.

The TMS320VC5505 EVM is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320VC5505 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

The TMS320VC5505 EVM can be used to develop TMS320VC5504 applications since the TMS320VC5504 processor is a subset of the TMS320VC5505.

## Notational Conventions

This document uses the following conventions.

The TMS320VC5505 will sometimes be referred to as the C55XX.

The TMS320VC5505 EVM will sometimes be referred to as the EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

*equations*  
*!rd = !strobe&rw;*

## Information About Cautions

This book may contain cautions.

### ***This is an example of a caution statement.***

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

## Related Documents

Texas Instruments TMS320VC55XX DSP CPU Reference Guide

Texas Instruments TMS320VC55XX DSP Peripherals Reference Guide

**Table 1: Hardware History**

Revision	History
A	Prototype Release
B	Alpha Release
C	Beta Release
D	Production Release

**Table 2: Manual History**

Revision	History
A	Alpha Release
B	Production Release

# **Chapter 1**

## **Introduction to the TMS320VC5505 EVM**

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Chapter One provides a description of the TMS320VC5505 EVM along with the key features and a block diagram of the circuit board.

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## 1.1 Key Features

The VC5505 EVM is a standalone development platform that enables users to evaluate and develop applications for the TI TMS320VC5505 Digital Signal Processor (DSP). The EVM also serves as a hardware reference design for the TMS320VC5505 DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

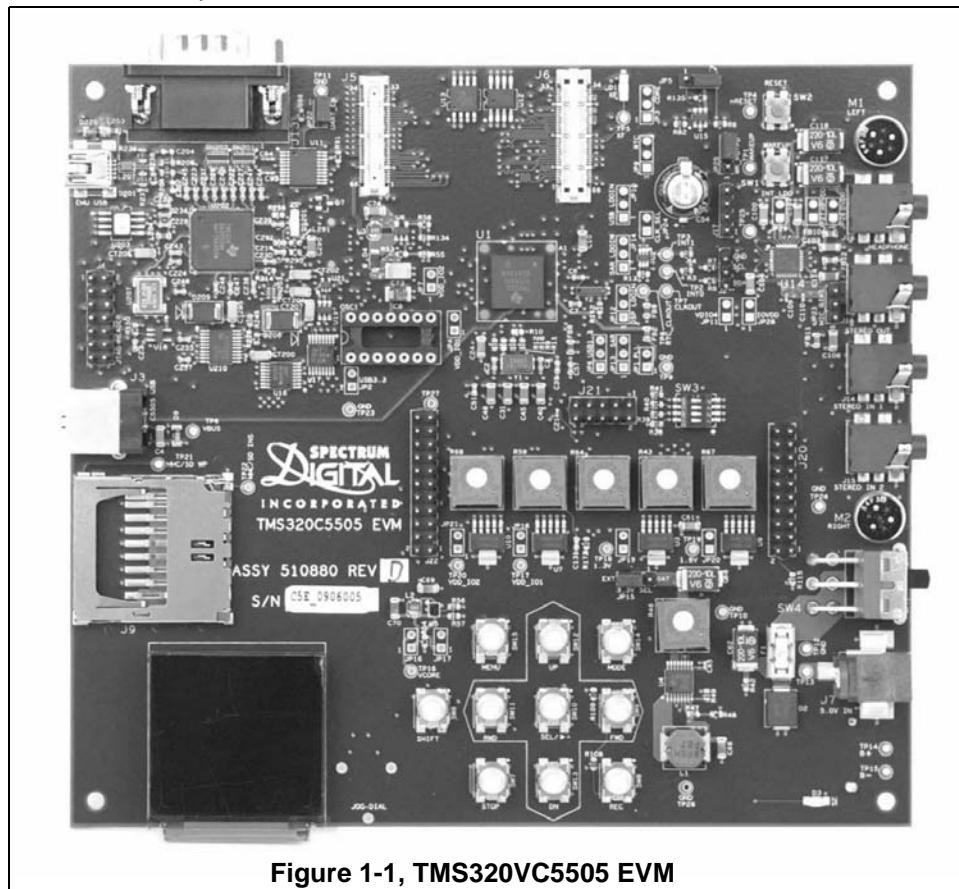


Figure 1-1, TMS320VC5505 EVM

The EVM comes with a full complement of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320VC5505 operating up to 100 Mhz.
- Flexible/variable power supply for each VC5505 power rail and scalable power supply core
- TLV320AIC3254 stereo codec
- MMC / SD connector
- User USB port via VC5505

- I<sup>2</sup>C EEPROM (256Kbits) and SPI EEPROM (256Kbits)
- EMIF, I<sup>2</sup>S, I<sup>2</sup>S, UART, SPI interfaces on expansion connectors
- External JTAG emulation interface
- Embedded JTAG controller
- Color LCD Display
- 10 User push button switches

## **1.2 Development Tools**

The EVM is designed to work with TI's Code Composer Studio (CCS) Integrated Development Environment (IDE). Code Composer Studio communicates with the EVM board through the external emulator header, or on board emulation. An EVM specific version of Code Composer Studio ships with the EVM.

## **1.3 Memory Map**

Refer to the TMS320VC5505 device documentation for a more specific memory information on the VC5505 device.

## **1.4 Power Supply**

The EVM operates from a +5V external power supply or battery.

### **WARNING**

To minimize risk of electric shock hazard, use only the following power supply for the EVM module with Medical Development Applications: SL Power AULT Model MW173KB0503F01.

## **1.5 VC5505 GIO Schedule**

The VC5505 has multiple GIO signals that can be used for system level tasks. The GIO signals are connected to various jumpers on the EVM. By using jumper plugs, these GIO signals can be used to control different functions on the VC5505 EVM. Refer to the discussion of the jumper setting later in this document for details of the jumper locations and options they provide. The table below describes how the GIO lines are used on the EVM.

**Table 1: VC5505 GIO Schedule**

<b>VC5505 EVM Function Description</b>	<b>VC5505 Default Multiplexed Function</b>	<b>GPIO Pin</b>	<b>Wired To</b>
Wakeup core from power off	External Interrupt	Wakeup	SW1, Expansion connector
User interrupt input	INT0	INT0	Low battery from U4 Expansion connector.
User interrupt input	INT1	INT1	Interrupt from J22-15, Expansion connector
S00	MMC0_CLK	GPIO0	J22-12, MMC/SD connector
S01	MMC0_CMD	GPIO1	J22-8, MMC/SD connector
S02	MMC0_D0	GPIO2	J22-22, MMC/SD connector
S03	MMC0_D1	GPIO3	J22-21, MMC/SD connector
S04	MMC0_D2	GPIO4	J22-1, MMC/SD connector
S05	MMC0_D3	GPIO5	TP27, MMC/SD connector
S10	MMC1_CLK	GPIO6	J22-5
S11	MMC1_CMD	GPIO7	J22-9
S12	MMC1_D0	GPIO8	J22-19
S13	MMC1_D1	GPIO9	J22-14
S14	MMC1_D2	GPIO10	J22-6
S15	MMC1_D3	GPIO11	J22-2
PD2	LCD_D2	GPIO12	Expansion connector, LCD connector
PD3	LCD_D3	GPIO13	Expansion connector, LCD connector
PD4	LCD_D4	GPIO14	Expansion connector, LCD connector.
PD5	LCD_D5	GPIO15	Expansion connector, LCD connector
PD6	LCD_D6	GPIO16	Expansion connector, LCD connector.
PD7	LCD_D7	GPIO17	Expansion connector, LCD connector.
PD8	LCD_D8	GPIO18	Expansion connector, LCD connector, AIC3254 (I2S2_CLK), SPI EEPROM (SPI_CLK), J22-3 (SPI_CLK)
PD9	LCD_D9	GPIO19	Expansion connector, LCD connector, AIC3254 (I2S2_FS), SPI EEPROM (SPI_CS0), J22-7 (SPI_CS0)
PD10	LCD_D10	GPIO20	Expansion connector, LCD connector, AIC3254 (I2S2_RX), SPI EEPROM (SPI_RX), J22-13 (SPI_RX)
A15	EMIF_A15	GPIO21	Expansion connector
A16	EMIF_A16	GPIO22	Expansion connector
A17	EMIF_A17	GPIO23	Expansion connector
A18	EMIF_A18	GPIO24	Expansion connector
A19	EMIF_A19	GPIO25	Expansion connector
A20	EMIF_A20	GPIO26	Expansion connector
PD11	LCD_D11	GPIO27	Expansion connector, LCD connector, AIC3254 (I2S2_DX), SPI EEPROM (SPI_DX), J22-11 (SPI_DX)
PD12	LCD_D12	GPIO28	Expansion connector, LCD connector, RS232 connector (UART_RTS)
PD13	LCD_D13	GPIO29	Expansion connector, LCD connector, RS232 connector (UART_CTS)
PD14	LCD_D14	GPIO30	Expansion connector, LCD connector, RS232 connector (UART_RX)
PD15	LCD_D15	GPIO31	Expansion connector, LCD connector, RS232 connector (UART_TX)

## 1.6 VC5505 I<sup>2</sup>C Addressing

The VC5505 EVM has multiple I<sup>2</sup>C devices for different purposes. The table below shows the addresses of these devices on the I<sup>2</sup>C bus.

**Table 2: VC5505 GIO Schedule**

EVM I <sup>2</sup> C Device	I <sup>2</sup> C Address	Wired To
TPS62354	0x4A	Core Power Supply, I <sup>2</sup> C EEPROM
CAT24WC256X	0x50	
TLP320AIC3254	0x18	CODEC ADS J22, Expansion connector J2, Test Point



# **Chapter 2**

## **Physical Description**

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This chapter describes the physical layout of the TMS320VC5505 EVM and its connectors.

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## 2.1 Board Layout

The VC5505 EVM is a 6.35 x 5.75 inch (161 x 146 mm.) ten (10) layer board which is powered by an external +5 volt only power supply. Figure 2-1 shows the layout of the top side of the VC5505 EVM.

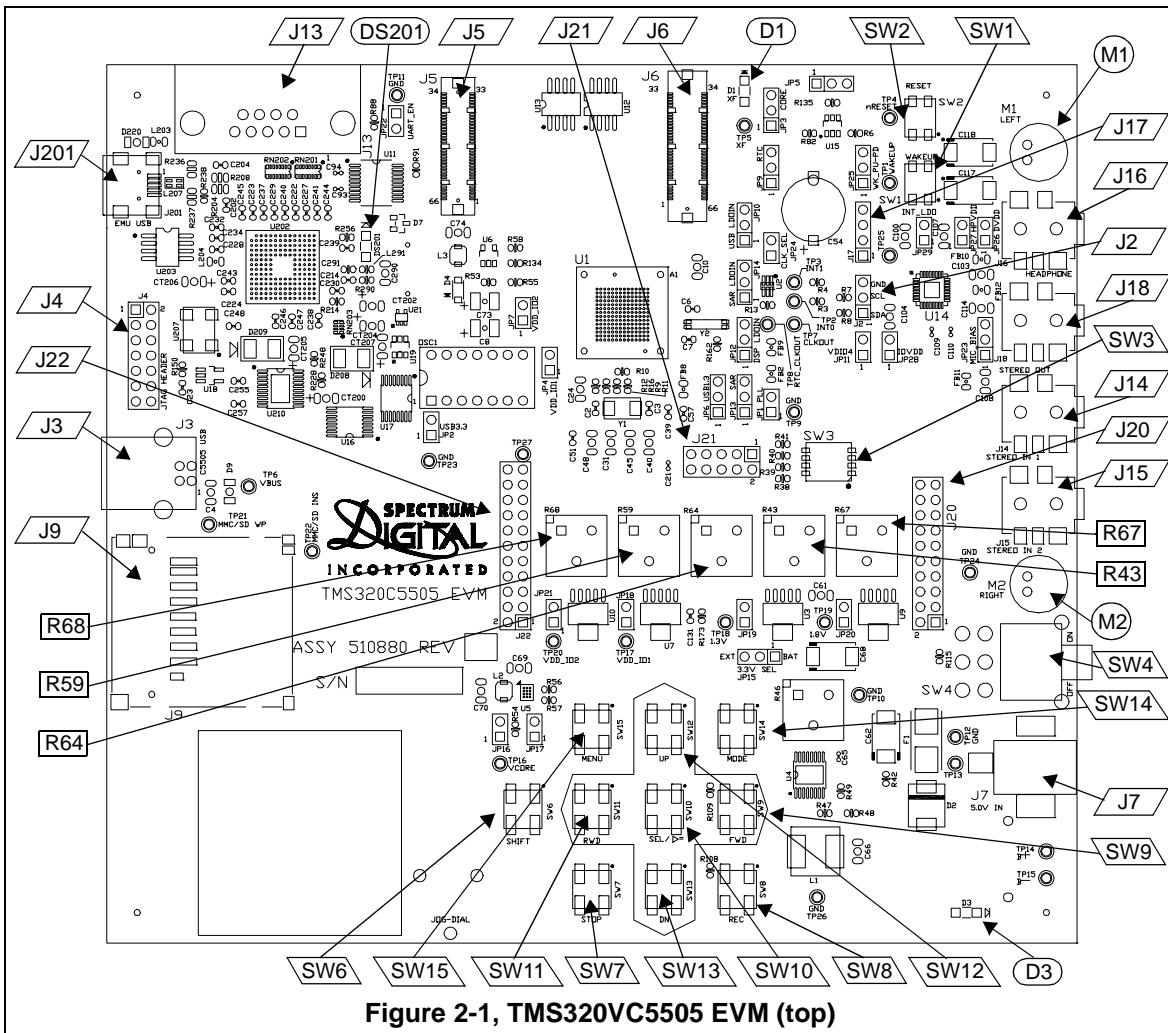
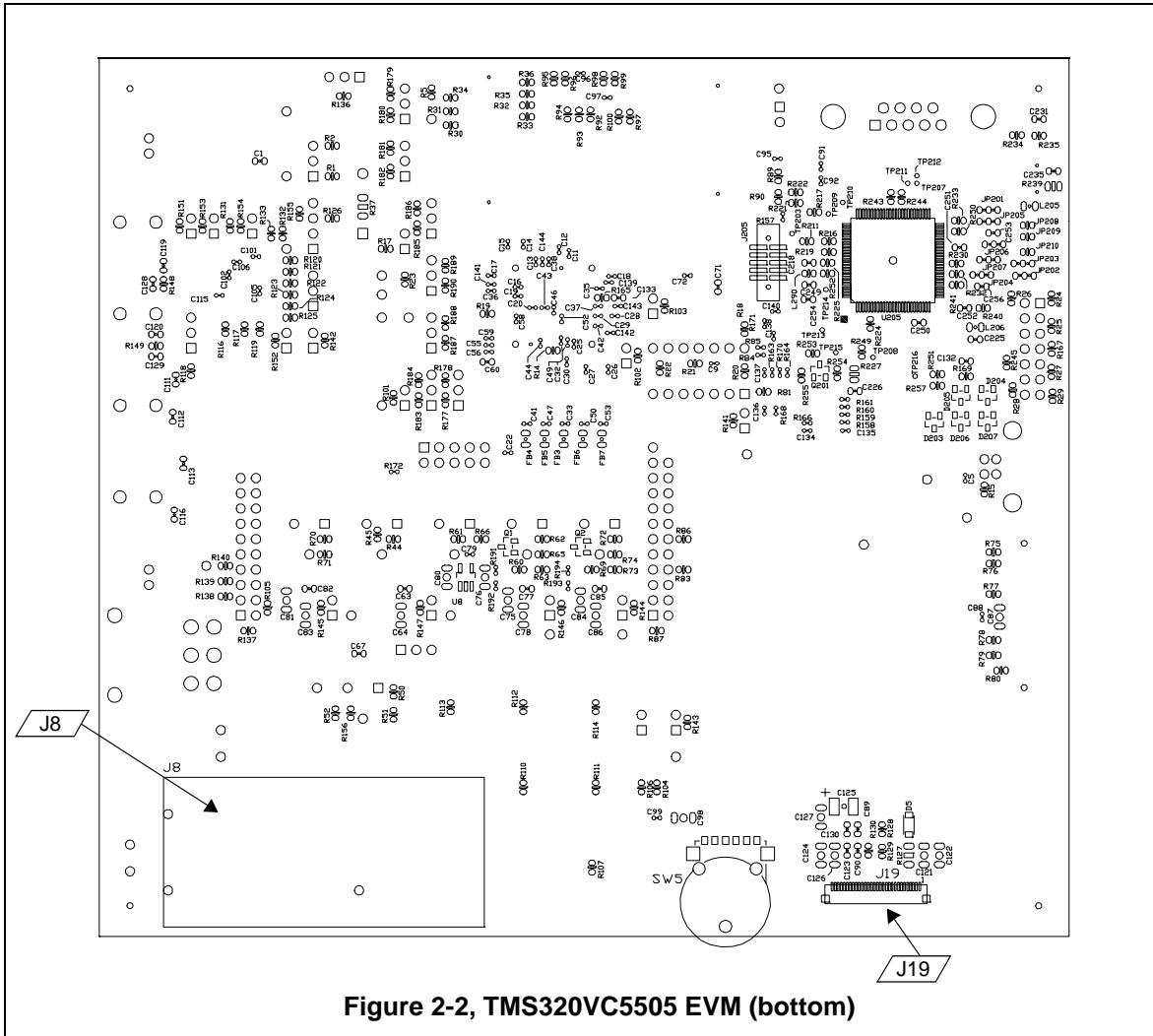


Figure 2-2 shows the layout of the bottom side of the VC5505 EVM.



## 2.2 Connector Index

The TMS320VC5505 EVM has twenty-two (22) connectors which provide the user access to the various signals on the EVM.

**Table 1: TMS320VC5505 EVM Connectors**

Connector	# Pins	Function	Schematic Page	Board Side
J2	3	I2C Probe Headers	2	Top
J3	4	USB Type B Connector	3	Top
J4	14	JTAG Header	4	Top
J5	66	Expansion	6	Top
J6	66	Expansion	6	Top
J7	2	+5 Volt In	8	Top
J8	2	Battery Holder	8	Bottom
J9	18	MMC/SD	11	Top
J13	9	RS-232	12	Top
J14	2	Stereo In 1	14	Top
J15	2	Stereo In 2	14	Top
J16	2	Headphones Out	14	Top
J17	4	AIC3254 Control Signals	14	Top
J18	2	Stereo Out	14	Top
J19	30	Display Interface	15	Bottom
J20	20	Daughter Card Interface	13	Top
J21	10	Daughter Card Interface	13	Top
J22	22	Daughter Card interface	13	Top
J201	5	Embedded USB Emulation Port	4	Top
M1	2	Left Microphone	14	Top
M2	2	Right Microphone	14	Top

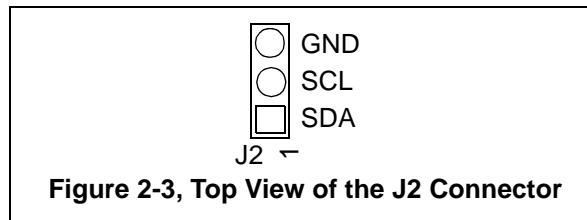
### 2.2.1 J2, I<sup>2</sup>C Probe Headers

Connector J2 brings out the I<sup>2</sup>C signals from the VC5505 processor. The signals are shown in the table below.

**Table 2: J2, I<sup>2</sup>C Probe Headers**

Pin #	Signal Name
1	I2C_SDA
2	I2C_SCL
3	GND

Shown below is a top view of the J2 connector.



**Figure 2-3, Top View of the J2 Connector**

### 2.2.2 J3, USB Type B Connector

The J3 connector is a USB Type B connector. This connector interfaces directly to the VC5505 processor. The signals on this connector are shown in the table below.

**Table 3: J3, USB Type B Connector**

Pin #	USB Signal	VC5505 Signal, Pin
1	VBUS	USB_VBUS, J12
2	D-	USB_DM, J14
3	D+	USB_DP, H14
4	GND	
5	GND	
5	GND	

### 2.2.3 J4, External JTAG Header

The TMS320VC5505 EVM is supplied with a 14 pin header interface, J4. This is the standard interface used by JTAG emulators to interface to Texas Instruments processors. The pinout for the connector is shown in the figure below.

TMS	1	2	TRST-	Header Dimensions
TDI	3	4	GND	Pin-to-Pin spacing, 0.100 in. (X,Y)
Vcc	5	6	<b>no pin (key)</b>	Pin width, 0.025-in. square post
TDO	7	8	GND *	Pin length, 0.235-in. nominal
RTCK	9	10	GND	
TCK	11	12	GND	* Embed/External EMU Select
EMU0	13	14	EMU1	

**Figure 2-4, JTAG INTERFACE**

#### 2.2.4 J5, Expansion Connector

Expansion connector J5 is a male header used for attaching daughter cards to the EVM. The pin out for this connector is shown in the figure below.

**Table 4: J5, Expansion Connector**

Pin #	Signal Name	Pin #	Signal Name
1	SDRAS	66	SDCE0
2	SDCAS	65	SDCE1
3	BA0	64	NC
4	BA1	63	NC
5	A0	62	NC
6	GND	61	GND
7	A1	60	NC
8	A2	59	NC
9	A3	58	NC
10	A4	57	LCD_DATA2 / GPIO12
11	A5	56	LCD_DATA3 / GPIO13
12	A6	55	LCD_DATA4 / GPIO14
13	A7	54	LCD_DATA5 / GPIO15
14	A8	53	LCD_DATA6 / GPIO16
15	A9	52	LCD_DATA7 / GPIO17
16	A10	51	UART_RTS / LCD_DATA12 / I2S3_CLK
17	GND	50	GND
18	ALE A11	49	UART_CTS / LCD_DATA13 / I2S3_FS
19	CLE A12	48	UART_RX / LCD_DATA14 / I2S3_RX
20	A13	47	UART_TX / LCD_DATA15 / I2S3_DX
21	A14	46	NC
22	A15	45	I2S2_CLK / LCD_DATA8 / SPI_CLK
23	A16	44	I2S2_FS / LCD_DATA9 / SPI_CS0
24	A17	43	I2S2_RX / LCD_DATA10 / SPI_RX
25	A18	42	I2S2_DX / LCD_DATA11 / SPI_DX
26	A19	41	LCD_RE / SPI_ALT_CLK
27	A20	40	LCD_DATA0 / SPI_ALT_RX
28	GND	39	GND
29	SDCLK	38	LCD_DATA1 / SPI_ALT_DX
30	SDCLKE	37	LCD_BIAS_OE / SPI_CS0
31	NC	36	LCD_MCLK / SPI_ALT_CS1
32	NC	35	LCD_nWE / SPI_ALT_CS2
33	NC	34	LCD_ALE / SPI_ALT_CS3

### 2.2.5 J6, Expansion Connector

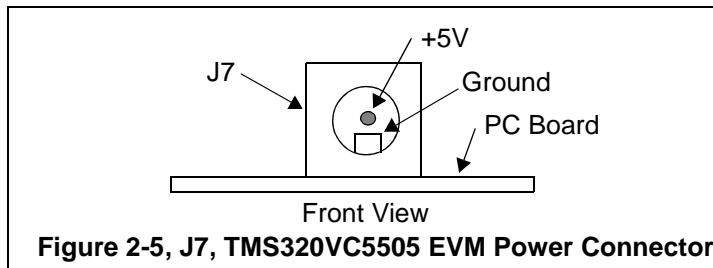
Expansion connector J6 is a female receptacle used for attaching daughter cards to the EVM. The pin out for this connector is shown in the figure below.

**Table 5: J6, Expansion Connector**

Pin #	Signal Name	Pin #	Signal Name
1	D0	66	RnW
2	D1	65	WE
3	D2	64	OE
4	D3	63	NC
5	DOM0	62	NC
6	GND	61	GND
7	D4	60	NAND_RDY0
8	D5	59	NAND_RDY1
9	D6	58	NAND_CE0
10	D7	57	NAND_CE1
11	D8	56	NC
12	D9	55	NC
13	D10	54	WAKEUP
14	D11	53	INT0
15	DOM1	52	INT1
16	D12	51	XF
17	GND	50	GND
18	D13	49	NC
19	D14	48	NC
20	D15	47	NC
21	A_RDY0	46	V3.3
22	A_RDY1	45	V3.3
23	A_CE0	44	V3.3
24	A_CE1	43	V3.3
25	I2C_SDA	42	VDD_IO1
26	I2C_SCL	41	VDD_IO1
27	GPAIN0	40	VDD_IO1
28	GND	39	GND
29	GPAIN1	38	VDD_IO2
30	GPAIN2	37	VDD_IO2
31	GPAIN3	36	VDD_IO2
32	Exp_Power_Control_IO2	35	NC
33	Exp_Power_Control_IO1	34	nRESET

### **2.2.6 J7, +5 Volt In Connector**

Power (+5 volts) is brought onto the TMS320VC5505 EVM via the J7 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The diagram of J7 is shown below.



**Figure 2-5, J7, TMS320VC5505 EVM Power Connector**

### **2.2.7 J8, Battery Holder**

Connector J8 is a battery holder on the bottom side of the board. This battery holder will accommodate two (2) "AA" size batteries. The ground and positive voltage from the battery go to the voltage regulator U4, TPS61030-ADJ. Jumper JP15 is used to select the voltage input source (power jack or the battery holder).

### 2.2.8 J9, MMC/SD Connector

Connector J9 is used to provide a MMC/SD interface to the VC5505 processor. The signals on this connector are shown in the table below.

**Table 6: J9, MMC/SD Connector**

Pin #	Signal Name
1	MMC0.DATA3
2	MMC0.CMD
3	GND
4	VDD_IO1
5	MMC0.CLK
6	GND
7	MMC0.DATA0
8	MMC0.DATA1
9	MMC0.DATA2
10	MMC0.WP / TP21
11	GND
12	MMC0.INS / TP22
13	No Connect
14	No Connect
15	No Connect
16	No Connect
17	No Connect
18	No Connect

### 2.2.9 J13, RS-232 Connector

The VC5505 EVM has an RS-232 connector, J13, which brings out the transmit and receive of the processor. This EVM uses the MAX3222 RS-232 line driver. The pin positions for the J13 connector as viewed from the edge of the printed circuit board are shown below.

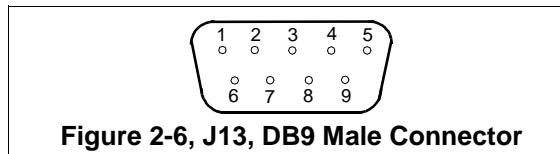


Figure 2-6, J13, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a DB-9 connector interface used on personal computers.

Table 7: J13, RS-232 UART Pinout

Pin #	Signal Name
1	No Connect
2	RXD
3	TXD
4	No Connect
5	No Connect
6	No Connect
7	RTS
8	CTS
9	GND

### 2.2.10 J14, Stereo In 1 Connector

The J14 connector in is a stereo input. The input connector is a 3.5 mm stereo jack. These inputs connect to AIC LINE2L and AIC LINE2R of the TLV320AIC3254. The signals on the mating plug are shown in the figure below.

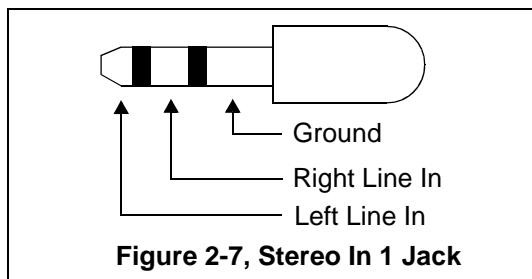


Figure 2-7, Stereo In 1 Jack

### 2.2.11 J15, Stereo In 2 Connector

The J15 connector in is a stereo input. The input connector is a 3.5 mm stereo jack. These inputs connect to AIC LINE3L and AIC LINE3R of the TLV320AIC3254. The signals on the mating plug are shown in the figure below.

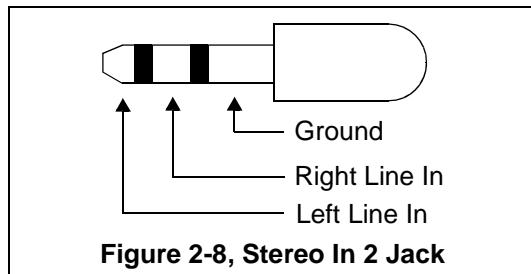


Figure 2-8, Stereo In 2 Jack

### 2.2.12 J16, Headphone Connector

Connector J16 is a headphone/speaker jack. It can drive standard headphones or a high impedance speaker directly. These outputs connect to AIC HEADPHONE LOUT and AIC HEADPHONE ROUT of the TLV320AIC3254. The standard 3.5 mm jack is shown in the figure below.

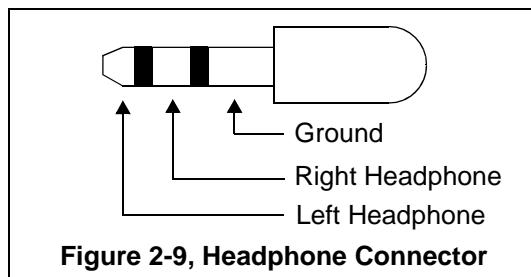


Figure 2-9, Headphone Connector

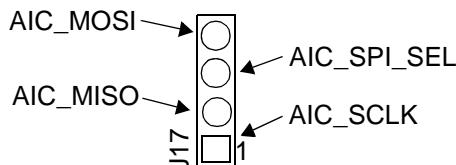
### 2.2.13 J17, HDR4 Connector

The HDR4 connector brings out 4 signals from the TLV320AIC3254. These signals are shown in the table below.

**Table 8: J17, HDR4 Connector**

Pin #	Signal Name
1	AIC_SCLK
2	AIC_MISO
3	AIC_SPI_SEL
4	AIC_MOSI

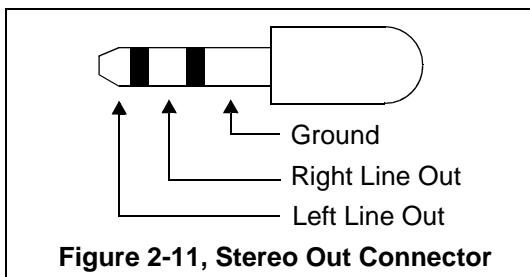
Shown below is a top view of the J17 connector.



**Figure 2-10, Top View of the J17 Connector**

### 2.2.14 J18, Stereo Out Connector

The audio line out, J18, is a stereo output. These outputs connect to AIC3254 LOUT and AIC3254 ROUT of the TLV320AIC3254. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.



**Figure 2-11, Stereo Out Connector**

### 2.2.15 J19, Display Interface

Connector J19 provides an interface to a display module. This connector is located on the bottom side of the board. The signals on this connector are shown in the table below.

**Table 9: J19, Display Interface**

Pin #	Signal Name	Pin #	Signal Name
1	NC	16	LCD_nWE / R/W
2	V13 / VCC-1	17	V3.3 or GND / BS1
3	VCOMH	18	V3.3 / BS2
4	VDD_IO1 / VDDIO	19	LCD_BIAS_OE / CE
5	VSL	20	LCD_ALE / D/C
6	NC / D8	21	nRESET / RESET
7	LCD_DATA7 / D7	22	IREF
8	LCD_DATA6 / D6	23	VP_C
9	LCD_DATA5 / D5	24	VP_B
10	LCD_DATA4 / D4	25	VP_A
11	LCD_DATA3 / D3	26	VBREF
12	LCD_DATA2 / D2	27	V3.3 / VDD
13	LCD_DATA1 / D1	28	GND / VSS
14	LCD_DATA0 / D0	29	V13 / VCC-2
15	LCD_RE / E	30	NC

### **2.2.16 Daughter Card Interfaces**

The TMS320VC5505 EVM has 3 daughter card interfaces. The Medical Development Kit (MDK) daughter cards from Texas Instruments use these interfaces. For more information about these cards refer to the following web sites:

<http://focus.ti.com/docs/toolsw/folders/print/tmdxmdkek1258.html>  
<http://focus.ti.com/docs/toolsw/folders/print/tmdxmdkds3254.html>  
<http://focus.ti.com/docs/toolsw/folders/print/tmdxmdkpo8328.html>

#### **2.2.16.1 J20, Daughter Card Interface**

Connector J20 is a 2 x 10 double row male header (.1 in. centers) used to interface to plug on daughter cards. The signals on this connector are shown in the table below.

**Table 10: J20, Daughter Card Interface**

<b>Pin #</b>	<b>Signal Name</b>	<b>Pin #</b>	<b>Signal Name</b>
2	GPAIN0	1	Through R137 to GPAIN
4	GPAIN1	3	Through R138 to GPAIN
6	GPAIN2	5	Through R139 to GPAIN
8	GPAIN3	7	Through R140 to GPAIN
10	NC	9	GND
12	NC	11	GND
14	NC	13	GND
16	NC	15	NC
18	NC	17	GND
20	NC	19	GND

#### **2.2.16.2 J21, Daughter Card Interface**

Connector J21 is a 2 x 5 double row male header (.1 in. centers) used to interface to plug on daughter cards. The signals on this connector are shown in the table below.

**Table 11: J21, Daughter Card Interface**

<b>Pin #</b>	<b>Signal Name</b>	<b>Pin #</b>	<b>Signal Name</b>
2	NC	1	NC
4	NC	3	NC
6	NC	5	GND
8	NC	7	V1.8
10	V5	9	V3.3

### 2.2.16.3 J22, Daughter Card Interface

Connector J22 is a 2 x 11 double row male header (.1 in. centers) used to interface to plug on daughter cards. The signals on this connector are shown in the table below.

**Table 12: J22, Daughter Card Interface**

Pin #	Signal Name	Pin #	Signal Name
1	GPIO4 / GPIO4	2	GPIO11 / GPIO11
3	SPI_CLK	4	GND
5	GPIO6 / I2S1_CLK	6	GPIO10 / GPIO10
7	SPI_CS0	8	GPIO1 / I2S0_FS
9	GPIO7 / I2S1_FS	10	GND
11	SPI_RX	12	GPIO0 / I2S0_CLK
13	SPI_RX	14	GPIO9 / I2S1_RX
15	INT1	16	I2C_SCL
17	XF	18	GND
19	GPIO8 / I2S12_DX	20	I2C_SDA
21	GPIO3 / I2S0_RX	22	GPIO2 / I2S0_DX

### 2.2.17 J201, Embedded USB Emulation Connector

Connector J201 provides a Universal Serial Bus (USB) Interface to the embedded JTAG emulation logic on the EVM. This allows for code development and debug without the use of an external emulator. This USB connector is not available for VC5505 applications. The signals on this connector are shown in the below.

**Table 13: J201, USB Connector**

Pin #	USB Signal Name
1	USBVdd
2	D+
3	D-
4	USB Vss
5	Shield
6	Shield

### **2.2.18 M1, Left Microphone**

The M1 microphone (left channel) connects to the AIC\_MIC1L line of the TLV320AIC3254.

### **2.2.19 M2, Right Microphone**

The M2 microphone (right channel) connects to the AIC\_MIC1R line of the TLV320AIC3254.

## **2.3 System LEDs**

The TMS320VC5505 EVM has three light emitting diodes (LEDs). These LEDs indicate various conditions on the EVM. These function of each LED is shown in the table below.

**Table 14: System LEDs**

Reference Designator	Color	Function	Schematic Page
D1	Green	Connected to the XF bit on the VC5505 processor	2
D3	Red	Indicates +5 volts is applied at the J7 connector	8
DS201	Green	USB activity, blinks during USB access to embedded emulation	4

## 2.4 VC5505 EVM Adjustable Power Rails

The VC5505 EVM has 5 potentiometers that allow the user to evaluate the low power features of the processor. These adjustable resistors and the voltage they control are shown in the table below.

**Table 15: TMS320VC5505 EVM Potentiometers**

Resistor #	Voltage Controlled	Schematic Page	Board Side
R43	+3.3 Volts	8	Top
R59	VDD_IO1	9	Top
R64	+1.3 Volts	10	Top
R67	+1.8 Volts	10	Top
R68	VDD_IO2	9	Top

## 2.5 VC5505 EVM Switches

The VC5505 EVM has 14 switches. A list of the switches is shown in the table below:

**Table 16: TMS320VC5505 EVM Switches**

Switch	Silkscreen Nomenclature/ Function	Schematic Page	Board Side
SW1	WAKEUP	2	Top
SW2	RESET	8	Top
SW3	4 Position DIP	7	Top
SW4	On/Off	8	Top
SW6	SHIFT	12	Top
SW7	STOP	12	Top
SW8	REC	12	Top
SW9	FORWARD (FWD)	12	Top
SW10	SELECT (SEL)	12	Top
SW11	REWIND (RWD)	12	Top
SW12	UP	12	Top
SW13	DOWN (DN)	12	Top
SW14	MODE	12	Top
SW15	MENU	12	Top

### 2.5.1 SW1, WAKEUP Switch

“Wakeup” is an active high external input signal used to wake up the core from the power off state. It can be configured as an active low open drain output signal. A pull up / pull-down jumper (JP25) is provided to accommodate both active high and active low states.

### 2.5.2 SW2, RESET Switch

This switch asserts the nRESET signal to all major components on the VC5505 EVM board. The nRESET signal is kept low for a short time via an optional supervisory circuit (TP3106K33 enabled by JP5). This is needed if not using the VC5505 on-chip LDOS.

### 2.5.3 SW3, LDO Option DIP Switches

SW3 is a 4 position DIP used to select LDO options. The table below shows the functions of the 4 positions. When switch is in the “ON” position a logic “0” is applied to the signal. When the switch is in the “OFF” position a logic “1” is applied to the signal.

**Table 17: System LEDs**

Switch Position	Signal State	Signal	Function	Default Setting
1 - ON	Low	DSP_LDO_V	For proper device operation, this switch <b>must</b> be in the OFF position	OFF/High
1 - OFF	High	DSP_LDO_V		
2 - ON	Low	DSP_LDO_EN	For proper device operation, this switch <b>must</b> be in the ON position	ON/Low
2 - OFF	High	DSP_LDO_EN		
3 - ON	Low	RSV3	For proper device operation, this switch <b>must</b> be in the ON position	ON/Low
3 - OFF	High	RSV3		
4 - ON	Low	RSV0	For proper device operation, this switch <b>must</b> be in the ON position	ON/Low
4 - OFF	High	RSV0		

### 2.5.4 SW4, On/Off Switch

The On/Off switch provides +5 volts to the logic on the board. In the “OFF” position this switch interrupts the power from the power supply as well as the battery holder.

### 2.5.5 SW6 - SW15, Function Switches

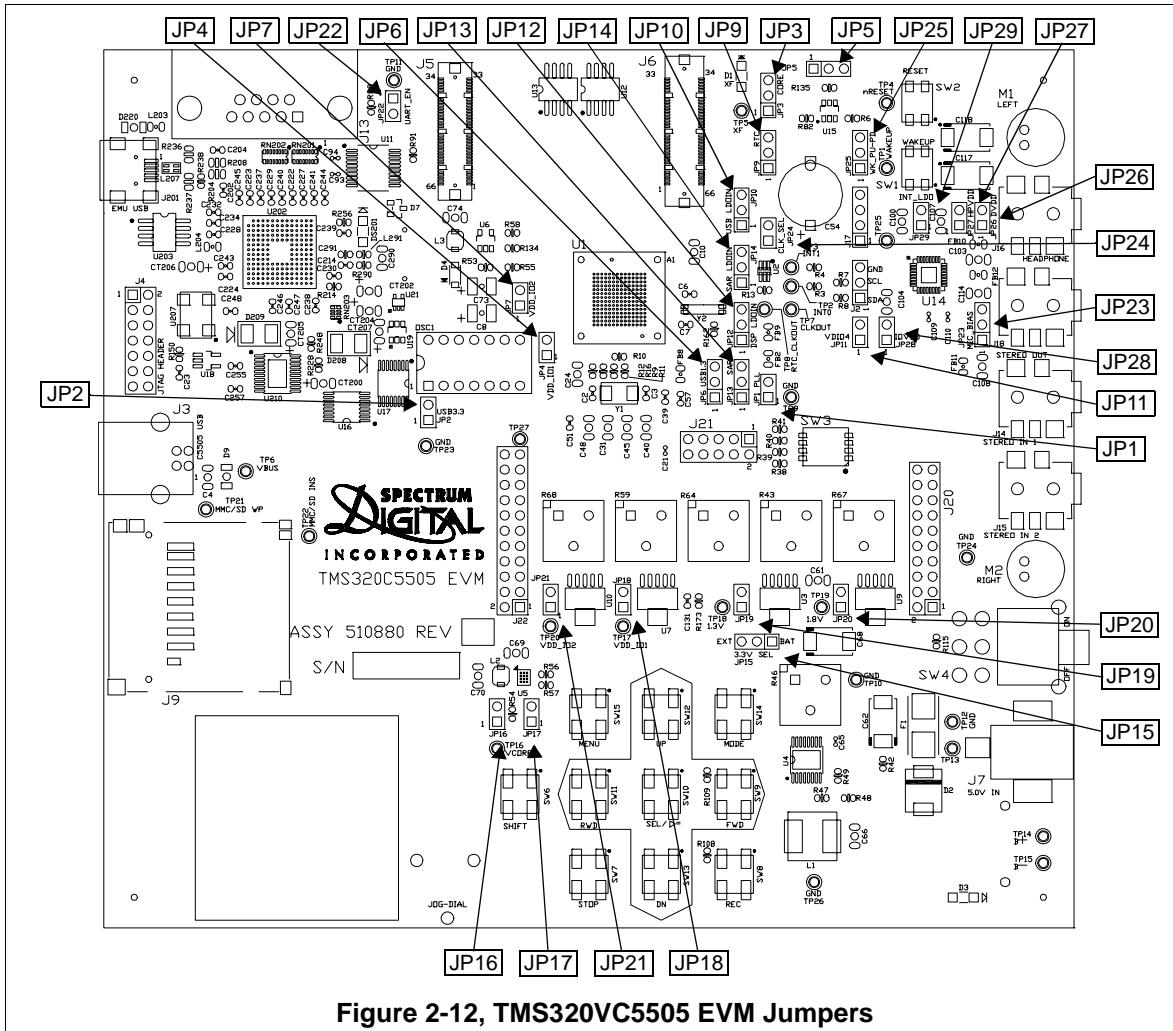
Switches SW6-SW15 are push button momentary switches which are read by the processor. These switches can take on any function defined by user software. The silk screen nomenclature is provided for user convenience and are shown in the table below.

**Table 18: Function Switches**

Switch #	Silk Screen Name
SW6	SHIFT
SW7	STOP
SW8	REC
SW9	FWD
SW10	SEL/PLAY
SW11	RWD
SW12	UP
SW13	DN
SW14	MODE
SW15	MENU

## 2.6 Jumpers

The VC5505 EVM has twenty-eight (28) jumpers locations. These jumpers can be divided into 3 classes; factory installed options, user options, and power domain probe points. The following sections describe the jumpers in these classes. The position of these jumpers on the top side of the EVM board are shown in the figure below.



### 2.6.1 VC5505 EVM Option Jumpers

The fourteen (14) option jumpers fall into two categories; factory installed(9), and user selectable(5). The factory installed jumpers are pre-configured with a zero ohm resistor at the factory and are **not** meant to be changed by users. The table below lists the factory installed option jumpers and their function.

**Table 19: VC5505 EVM Factory Installed Option Jumpers**

Jumper #	Nomenclature or Function	# of Positions	Jumper Populated	Factory Default	Schematic Page
JP3	CORE Select	3	No	2 - 3	7
JP6	USB1.3	3	No	2 - 3	7
JP9	RTC	3	No	1 - 2	7
JP10	USB LDOI SEL	3	No		7
JP12	DSP LDOI SEL	3	No	1 - 2	7
JP13	VDD_ANA	3	No	1 - 2	7
JP14	ANA LDOI SEL	3	No	1 - 2	7
JP24	CLK_SEL	2	No		3
JP25	WK_PU-PD	3	Yes	2 - 3	2

The table below shows lists the user option jumpers and their function.

**Table 20: VC5505 EVM User Option Jumpers**

Jumper #	Nomenclature or Function	# of Positions	Jumper Populated	Factory Default	Schematic Page
JP5	Reset Select	3	Yes	2 - 3	8
JP15	3.3V SEL	3	Yes	2 - 3	8
JP17	VSEL Select	2	Yes	Shorted	8
JP22	UART_EN	2	Yes	Shorted	12
JP23	MIC_BIAS	3	No		14

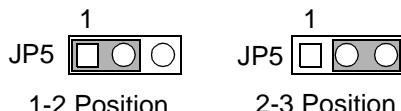
### 2.6.1.1 JP5, nRESET Source Select

Jumper JP5 is a three position jumper that allows the user to select the source of the nRESET signal to the VC5505 processor. This jumper is pre-configured at the factory with a jumper in the 2-3 position (\*). The table below shows the positions and their function.

**Table 21: JP5, nRESET Source Select**

Jumper Position	Function
1-2	PWR_RSTn is the source of the nRESET signal to the VC5505 Processor
2-3 *	SW2 is the source of the nRESET signal to the VC5505 Processor

Shown below is a top view of the JP5.



**Figure 2-14, Top View of the Jumper JP5**

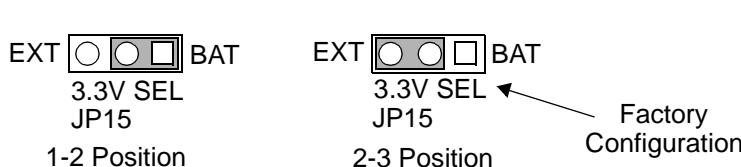
### 2.6.1.2 JP15, V3.3 Source Select

Jumper JP15 is a three position populated jumper that selects the source of the V3.3 voltage to the VC5505 processor. This jumper is pre-configured at the factory with a jumper in the 2-3 position (\*). The table below shows the positions and their function.

**Table 22: JP15, V3.3 Source Select**

Jumper Position	Function
1-2	V3.3 is sourced from the battery
2-3 *	V3.3 is sourced from the +5 volt power supply

Shown below is a top view of the JP15.



**Figure 2-21, Top View of the Jumper JP15**

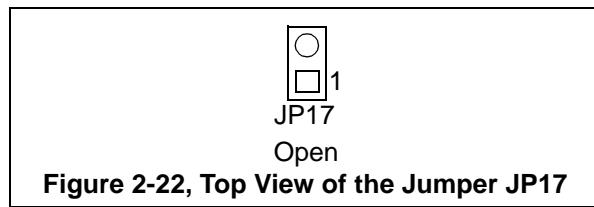
### 2.6.1.3 JP17, Vsel Select

Jumper JP17 is a two position unpopulated jumper that routes V3.3 to the VSEL of the TPS6254. This jumper is pre-configured at the factory to be shorted (\*). The table below shows the positions and their function.

**Table 23: JP17, Vsel Select**

Jumper Position	Function
Open	Set Vcore to 1.05V
Shorted *	Set Vcore to 1.3V

Shown below is a top view of the JP17.



**Figure 2-22, Top View of the Jumper JP17**

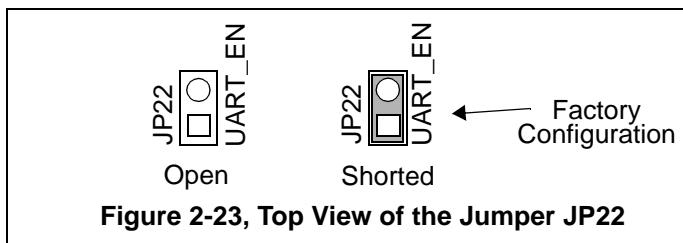
### 2.6.1.4 JP22, UART Enable Jumper

Jumper JP21 is a two position populated jumper that enables/disables the UART driver on the EVM. This jumper is pre-configured at the factory with a jumper in place (\*). The table below shows the positions and their function.

**Table 24: JP22, UART Enable Jumper**

Jumper Position	Function
Open	EN_L pulled to GND thereby disabling the MAX3222 line driver
Shorted *	EN_L pulled to +3.3 thereby enabling the MAX3222 line driver

Shown below is a top view of the JP22.



**Figure 2-23, Top View of the Jumper JP22**

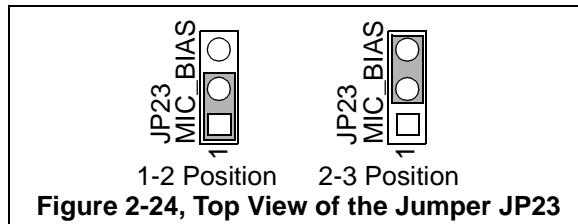
### 2.6.1.5 JP23, Microphone Bias Select

Jumper JP23 is a three position populated jumper that selects the source of the signal used for AIC MIC1L and AIC MIC1R biasing signals on the TLV320AIC3254. There is no factory selection. The table below shows the positions and their function.

**Table 25: JP23, Microphone Bias Select**

Jumper Position	Function
1-2	Ground coupled through a capacitor is used as the source for bias
2-3	MICBIAS from the TLV320AIC325 is used as the source for bias

Shown below is a top view of the JP23.



**Figure 2-24, Top View of the Jumper JP23**

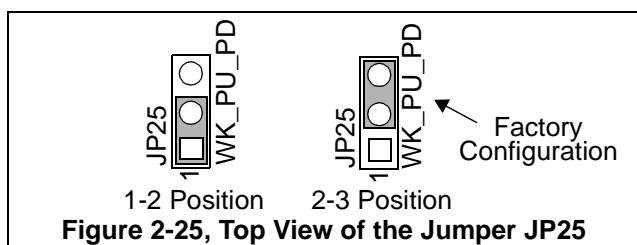
### 2.6.1.6 JP25, WAKEUP Source Select

Jumper JP25 is a three position populated jumper that selects the source of the WAKEUP signal going to the VC5505 processor. This jumper is pre-configured at the factory with a jumper in the 2-3 position (\*).The table below shows the positions and their function.

**Table 26: JP25, WAKEUP Source Select**

Jumper Position	Function
1-2	VDDIO4 pullup is the source to the WAKEUP signal of the VC5505 processor
2-3 *	GND pulldown is the signal level sourced to the WAKEUP signal of the VC5505 processor

Shown below is a top view of the JP25.



**Figure 2-25, Top View of the Jumper JP25**

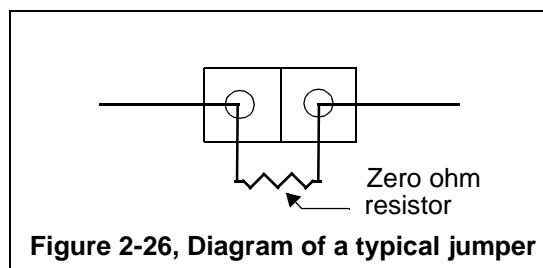
### 2.6.2 VC5505 EVM Power Domain Probe Points

The VC5505 EVM has pre-designed probe points in the circuitry which could be used to observe power domains. These measurement points consist of a 2 pin 0.1 inch spaced printed circuit board (pcb) footprint jumper shorted by a zero ohm resistor. The probe points are shown in the table below.

**Table 27: VC5505 EVM Power Domain Probe Points**

Jumper #	Signal	# of Positions	0 Ohm shunt Resistor Installed at factory	Schematic Page
JP1	VC5505 PLL	2	Yes	7
JP2	VC5505 USB3.3	2	Yes	7
JP4	VC5505 VDD_IO1	2	Yes	7
JP7	VC5505 VDD_IO2	2	Yes	7
JP11	VC5505 VDIO4	2	Yes	7
JP16	VC5505 VCORE	2	Yes	8
JP18	VC5505 VDD_IO1	2	Yes	9
JP19	+1.3 Volts	2	Yes	10
JP20	+1.8 Volts	2	Yes	10
JP21	VDD_IO2	2	Yes	9
JP26	AIC DVDD	2	Yes	14
JP27	AIC HPVDD	2	Yes	14
JP28	AIC IOVDD	2	Yes	14
JP29	AIC INT_LDO	2	No	14

Shown below is a diagram of a typical Power Domain Probe Point.



**Figure 2-26, Diagram of a typical jumper**

## 2.7 Test Points

The VC5505 EVM has twenty-seven (27) test points. The position of these test points on the top side of the VC5505 EVM are shown in the figure below.

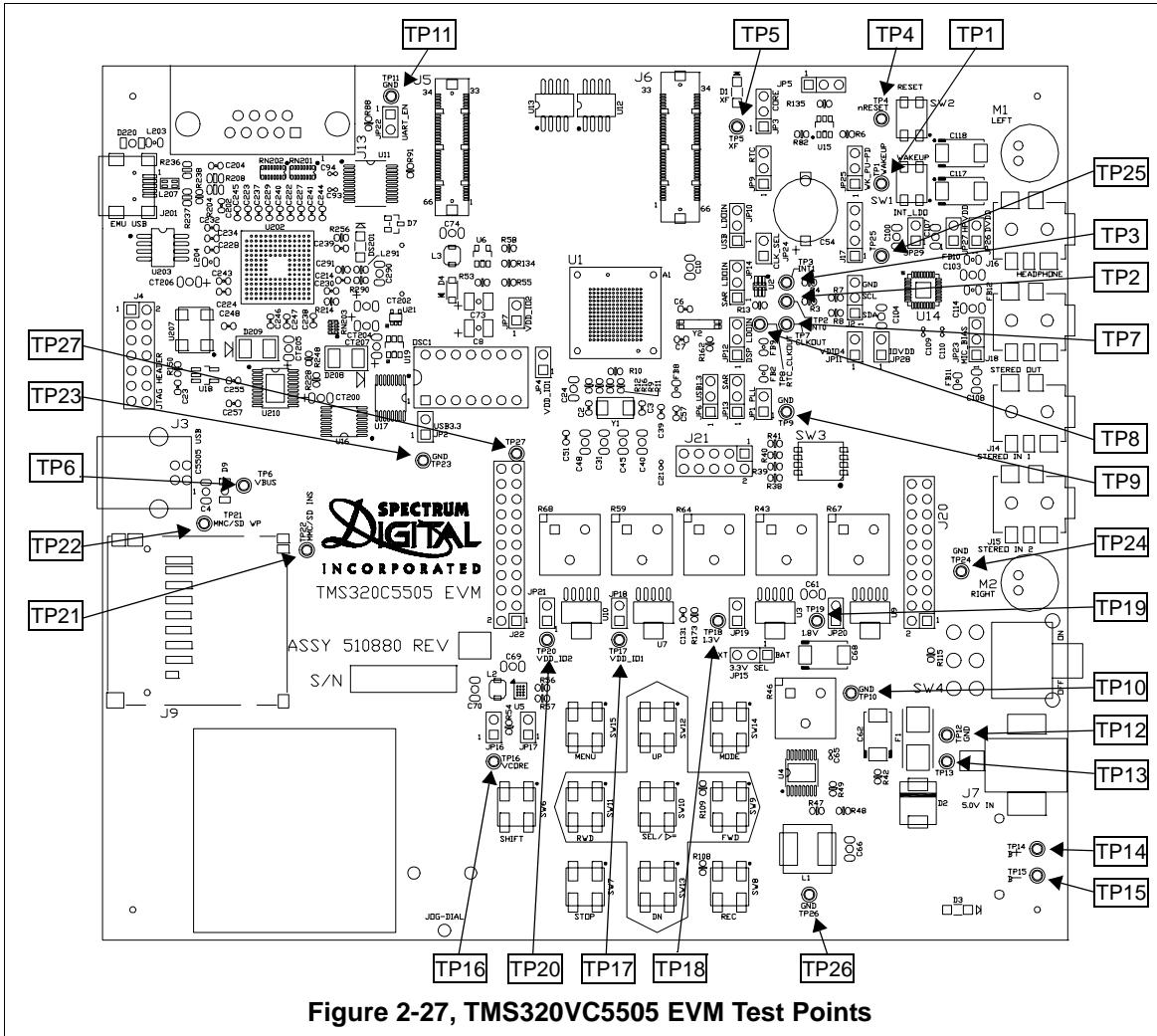


Figure 2-27, TMS320VC5505 EVM Test Points

The table below shows the signals present on each test point.

**Table 28: VC5505 EVM Test Points**

Test Point #	Signal	Schematic Page
TP1	WAKEUP	2
TP2	INT0	2
TP3	INT1	2
TP4	nRESET	8
TP5	XF	2
TP6	VBUS	3
TP7	CLKOUT	3
TP8	RTC_CLKOUT	3
TP9	GND	9
TP10	GND	13
TP11	GND	7
TP12	GND	8
TP13	+5 Volt In	8
TP14	B+	8
TP15	B-	8
TP16	VCORE	8
TP17	VDD_IO1	9
TP18	+1.3V	10
TP19	+1.8V	10
TP20	VDD_IO2	9
TP21	MMC0.WP	11
TP22	MM0.INS	11
TP23	GND	14
TP24	GND	12
TP25	AIC_GPIO	14
TP26	GND	3
TP27	GPIO5	13



# **Appendix A**

## **Schematics**

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This appendix contains the schematics for the TMS320VC5505 EVM. Board components with designators over 200 (e.g. DS210, R211) are part of Spectrum Digital's embedded JTAG emulator and are not included in these schematics.

REVISION TRACKING - FOR SPECIFIC CHANGES SEE REVISION PAGE AT BACK OF SCHEMATIC					
	Assembly	PWB	Schematic	TI Marking	Spectrum Revision
1.	510540-0001A	510541-0001A	510542-0001A	Version 1.0	A
2.	510880-0001A	510881-0001A	510881-0001B	Version 1.1	A
3.	510880-0001B	510881-0001B	510881-0001B	Version 1.2	B
4.	510880-0001C	510881-0001B	510881-0001B	Version 1.2	C
5.	510880-0001D	510881-0001D	510881-0001D	Removed	D
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NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.
2. CAPACITANCE VALUES IN MICROFARADS.
3. REFERENCE DESIGNATORS USED:
4. ALL 0.1 UF AND 0.01UF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS. OTHERWISE THEY SHOULD BE PLACED NEAR THE INTEGRATED CIRCUITS.

C5505 Schematic Contents

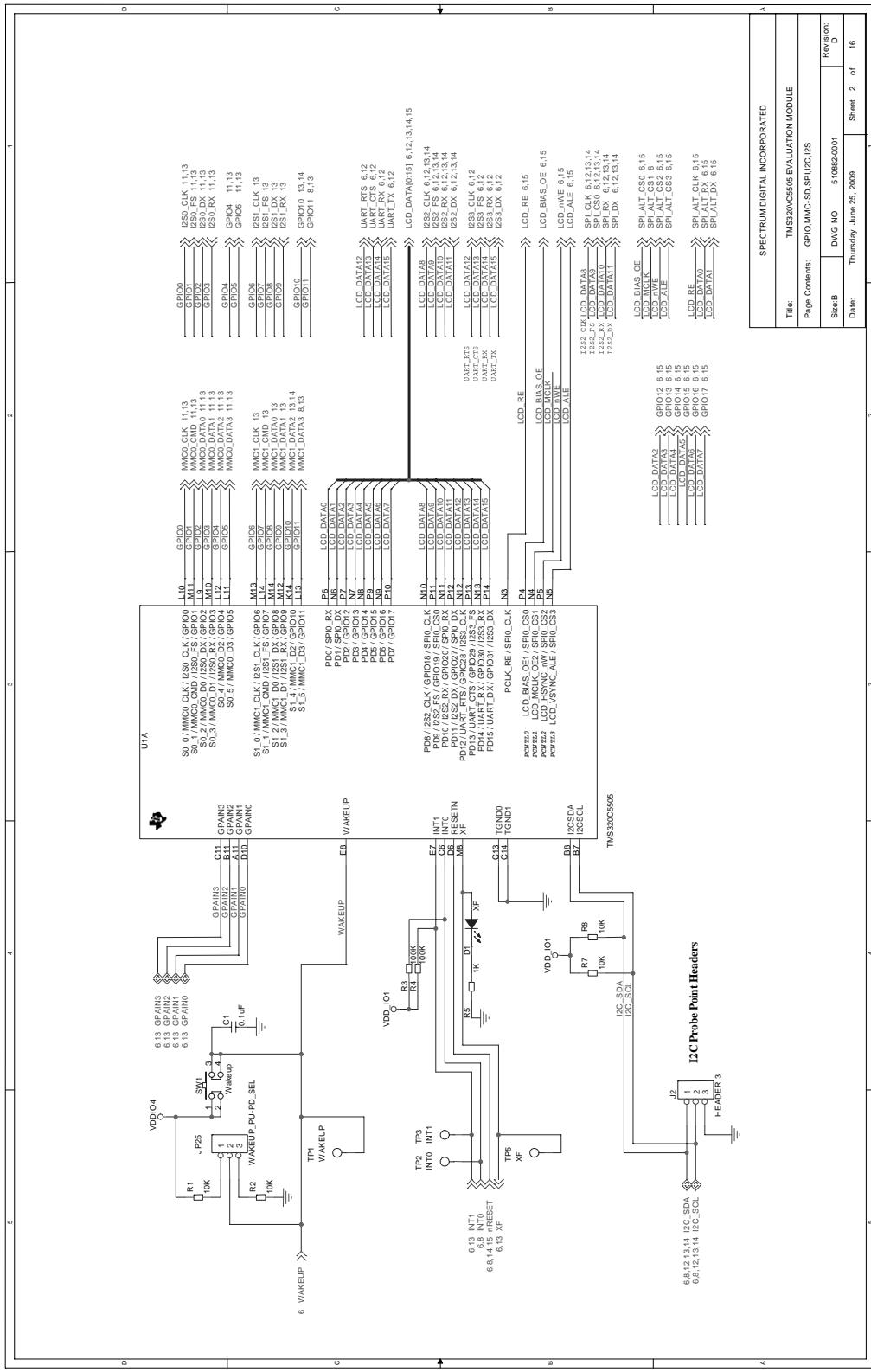
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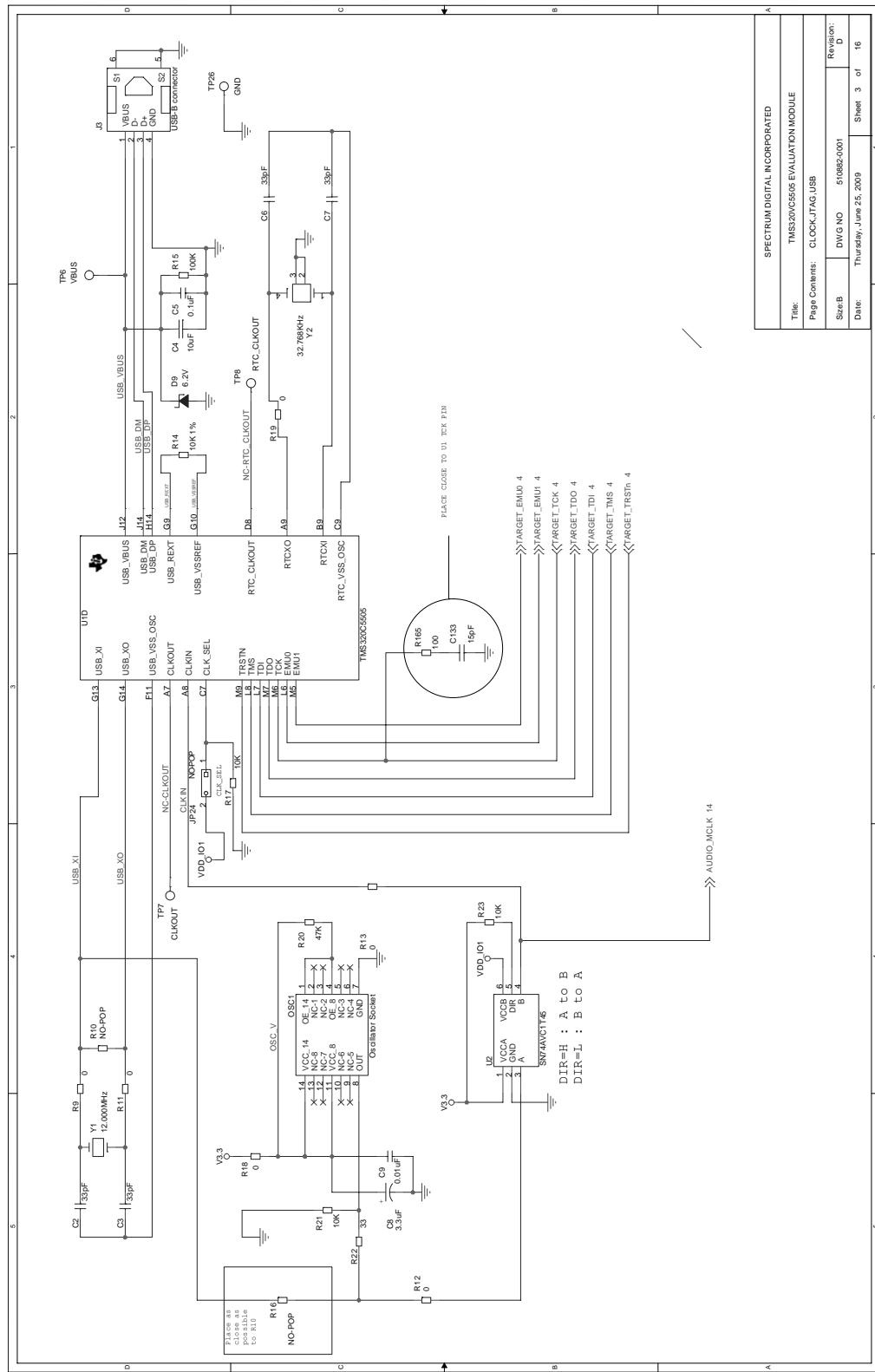
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03 - C5505 CLOCKS / JTAG / USB
04 - EMULATION - JTAG
05 - C5505 BMIF
06 - EMIF Expansion Conn
07 - C5505 Power
08 - POWER VDDIO1 / VDDIO2
09 - POWER 1.3V / 1.8V / VDDIO
10 - MMC / SD
11 - UART / EPROMS
12 - SAR Register Network
13 - COLOR LCD INTERFACE
14 - CODIC
15 - REVISTON SUMMARY
16 - REVISTON SUMMARY

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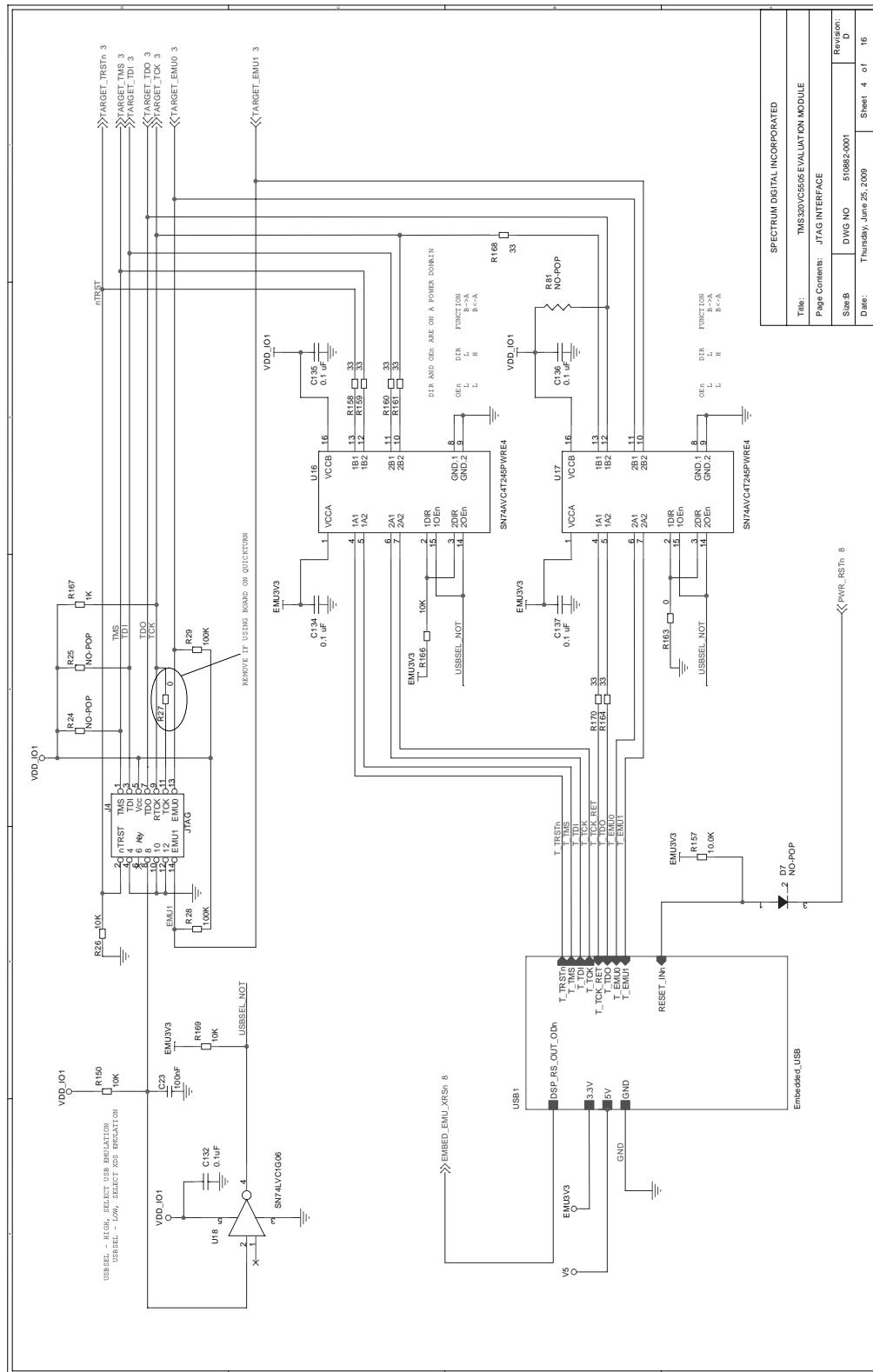
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|----------|--------|------------|
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| DNGR/MGR | R.R.P. | 05/15/2009 |
| GAR      | C.M.P. | 05/15/2009 |
| KFG      | R.R.P. | 05/15/2009 |
| MUE      | R.R.P. | 05/15/2009 |

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| Page Contains:                | TITLE SHEET            |             |               |
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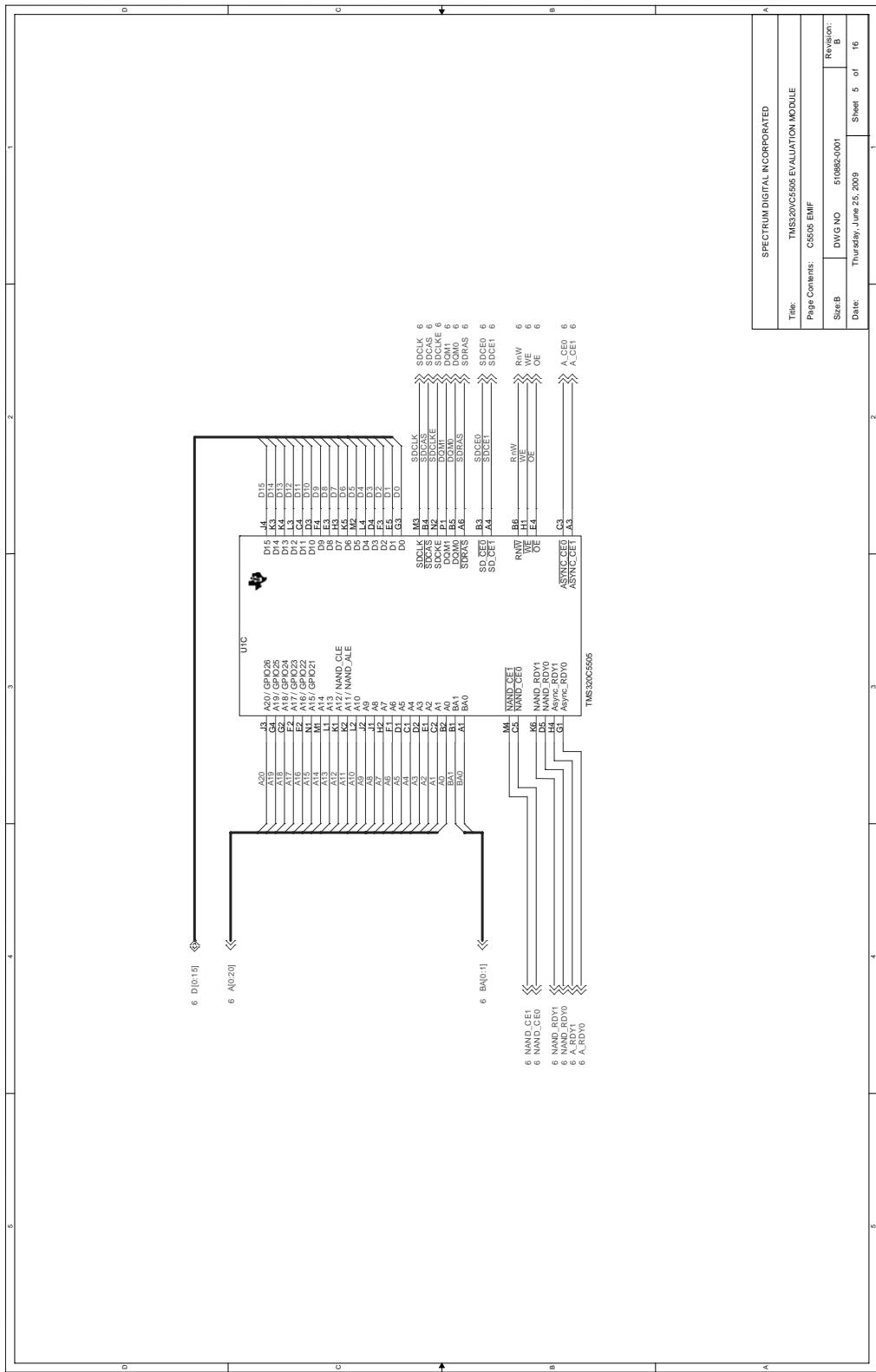


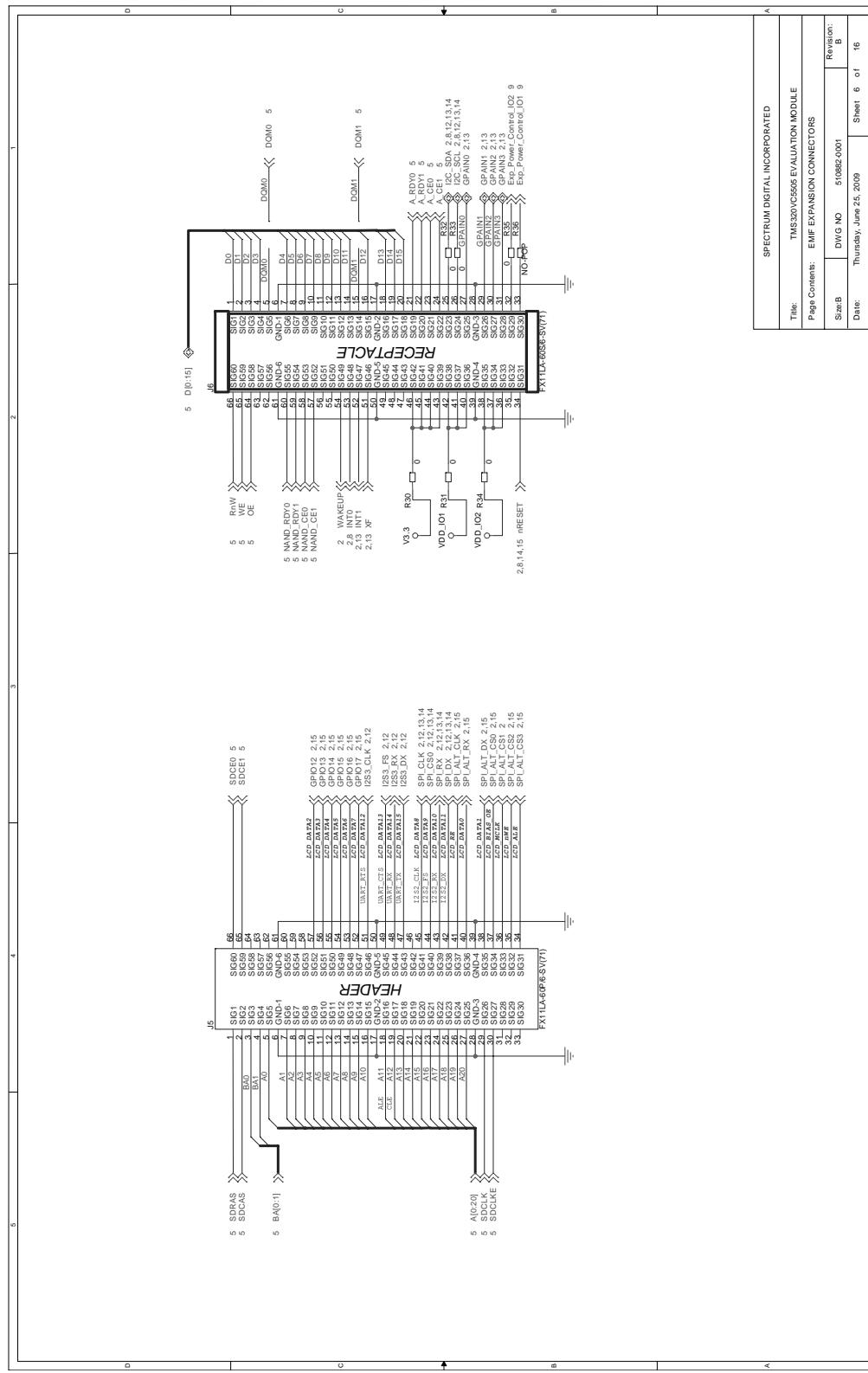


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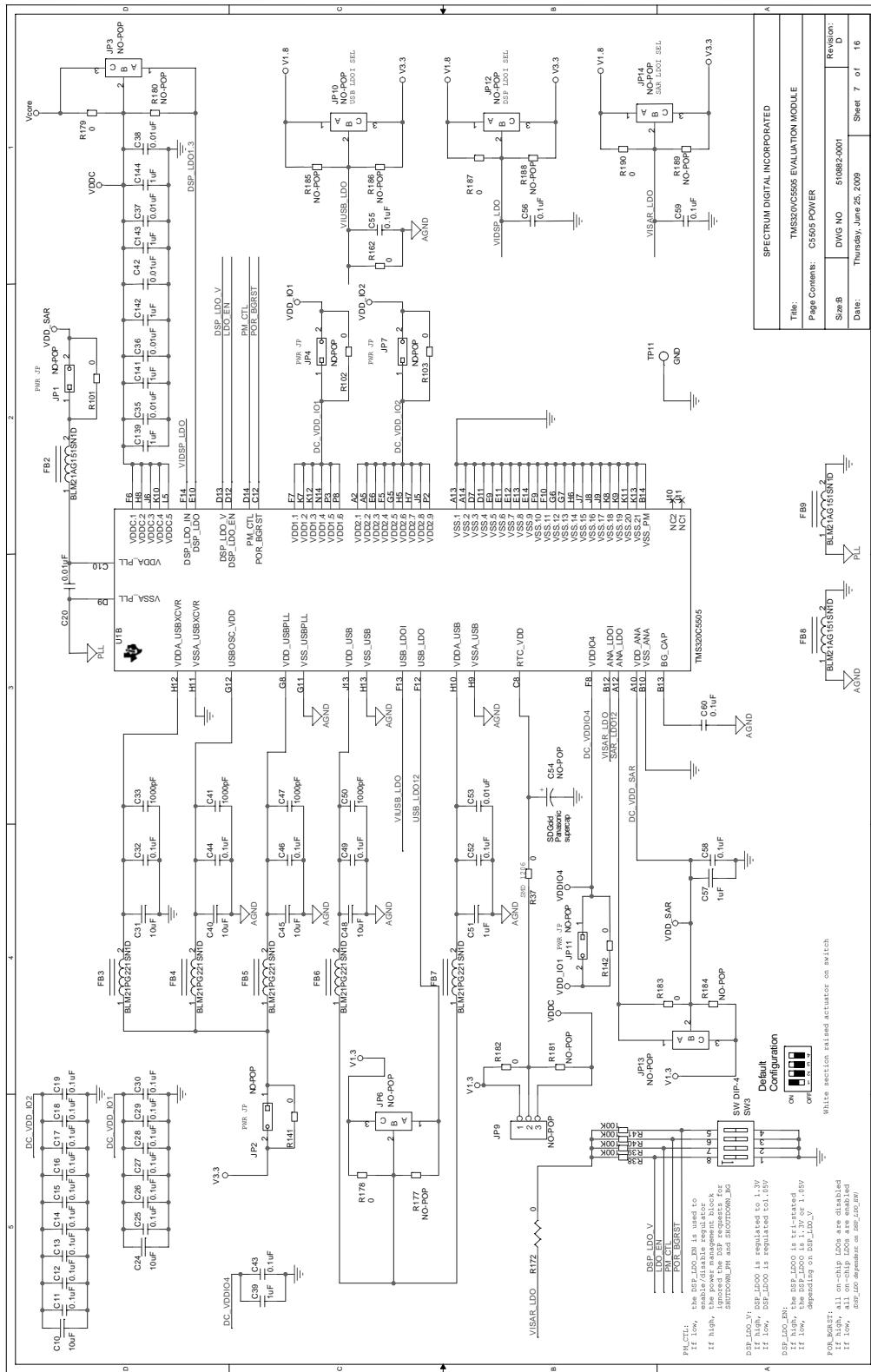


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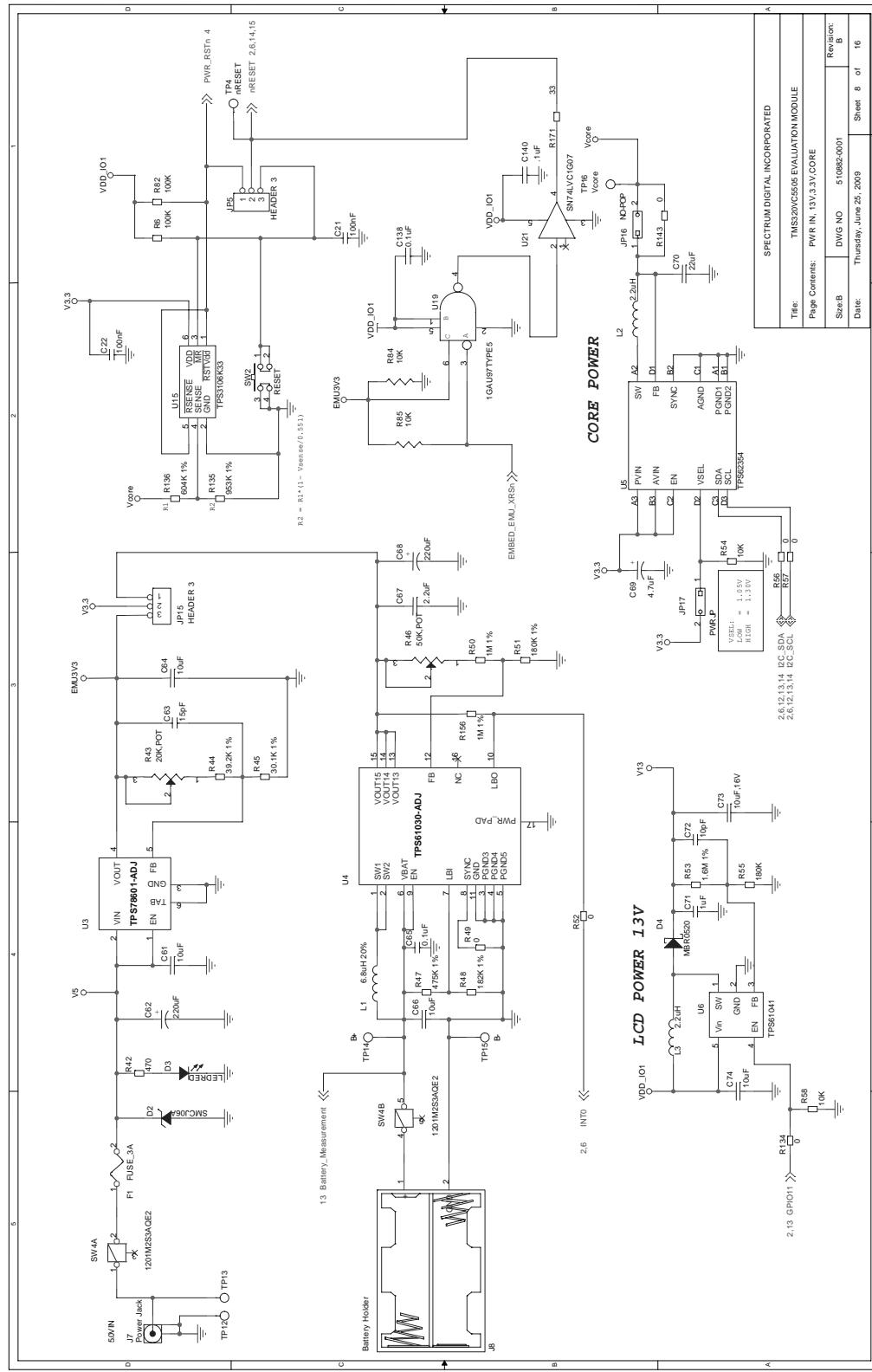


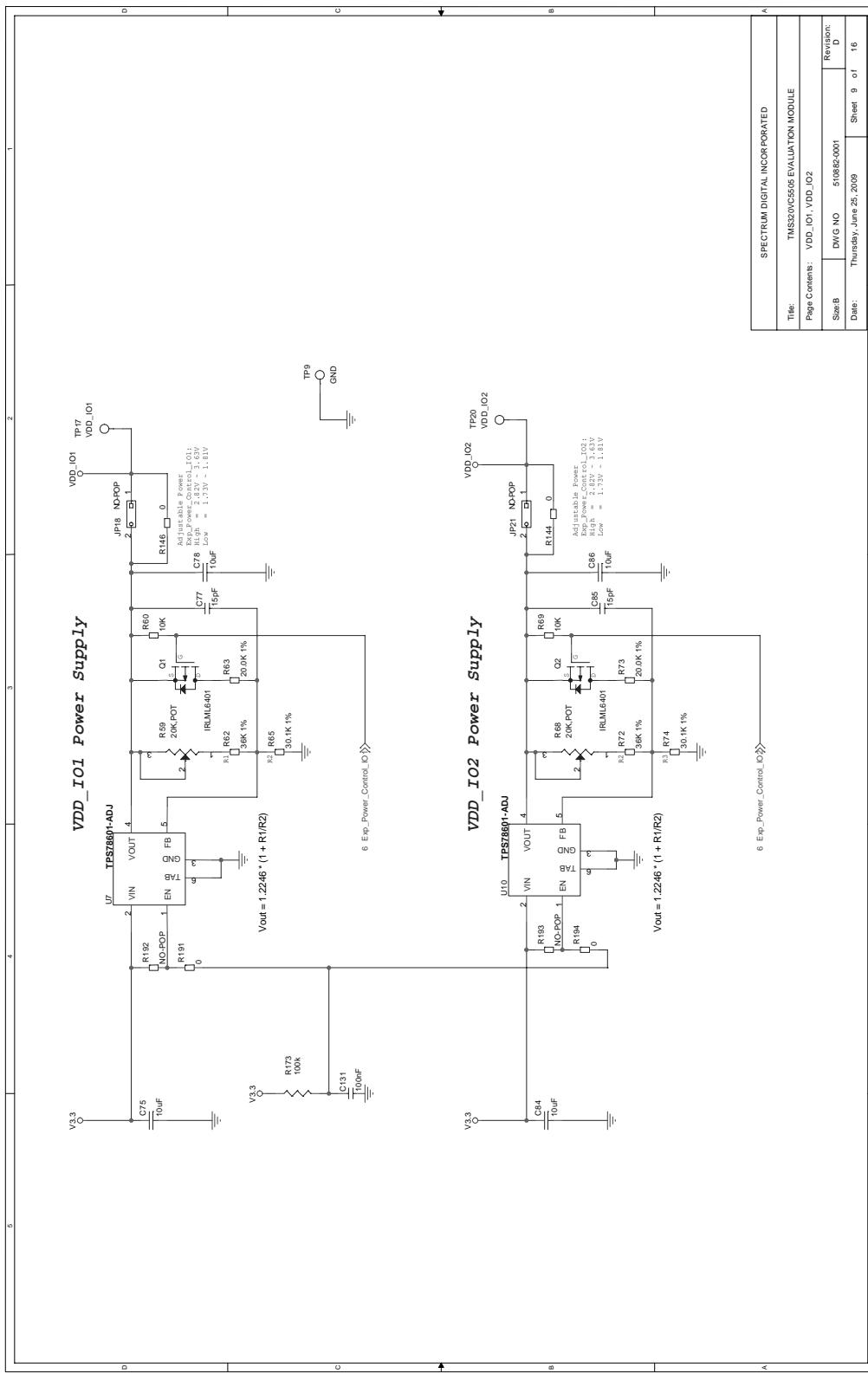


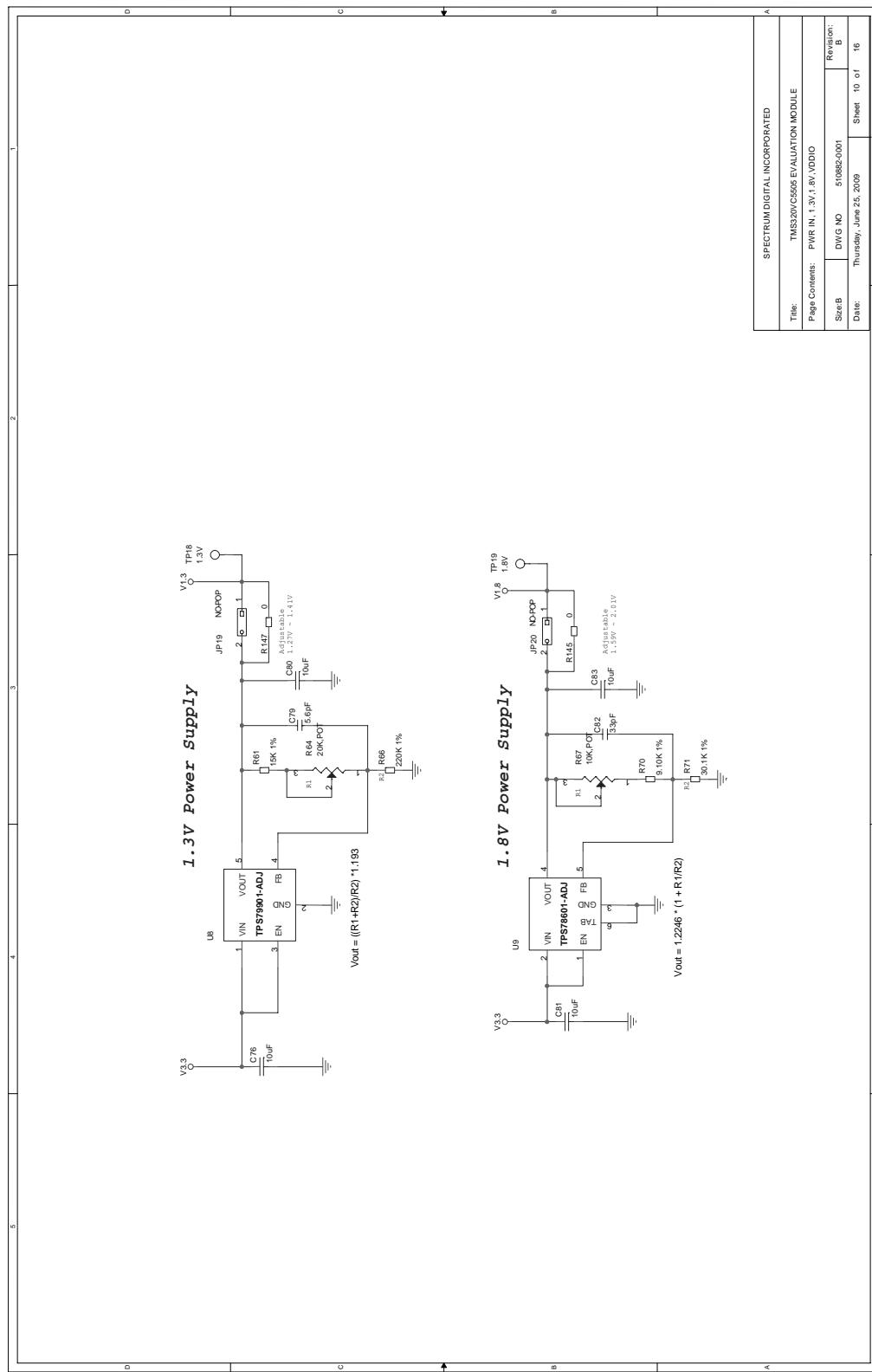
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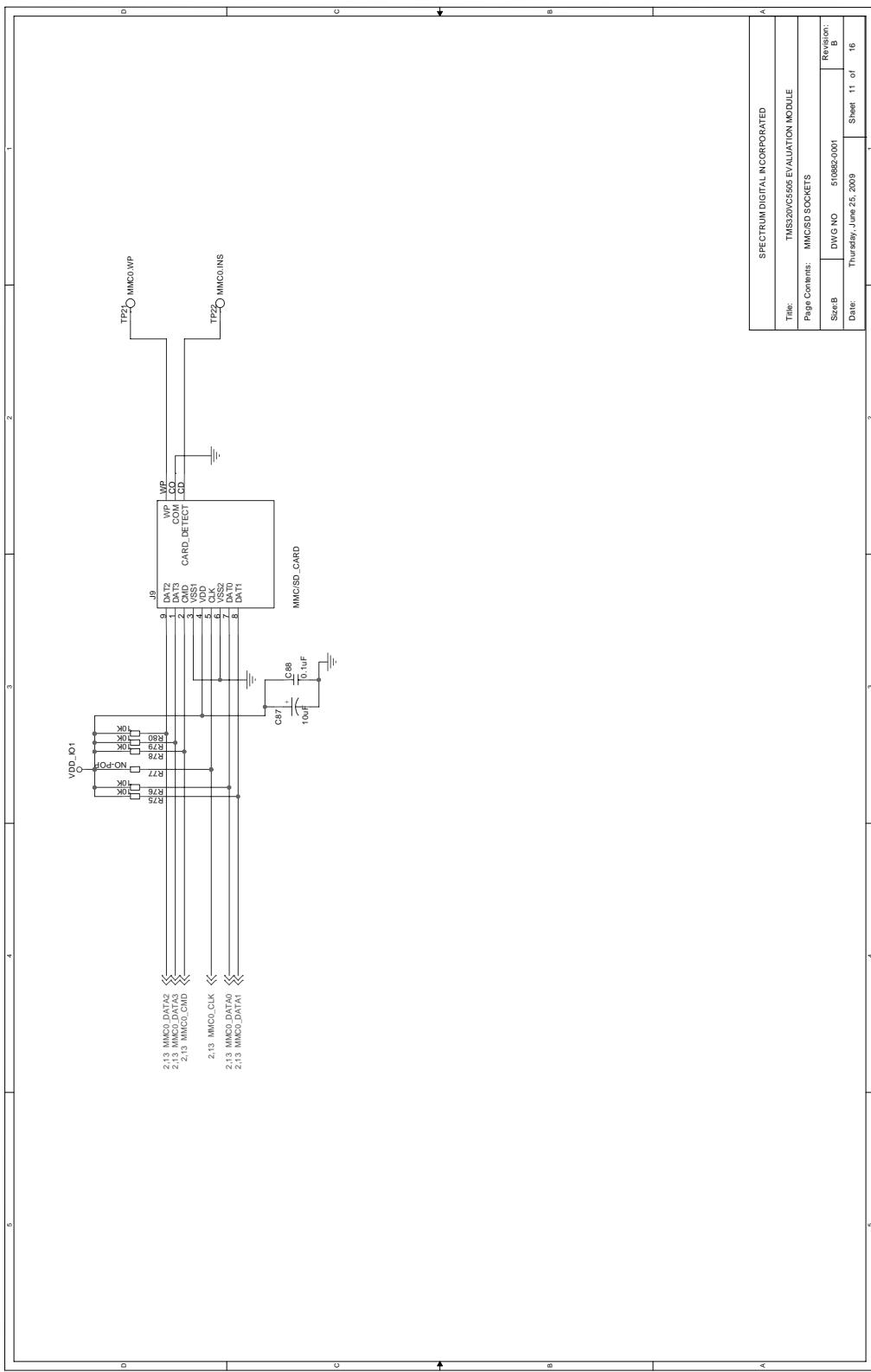


TMS320VC5505 EVM Technical Reference

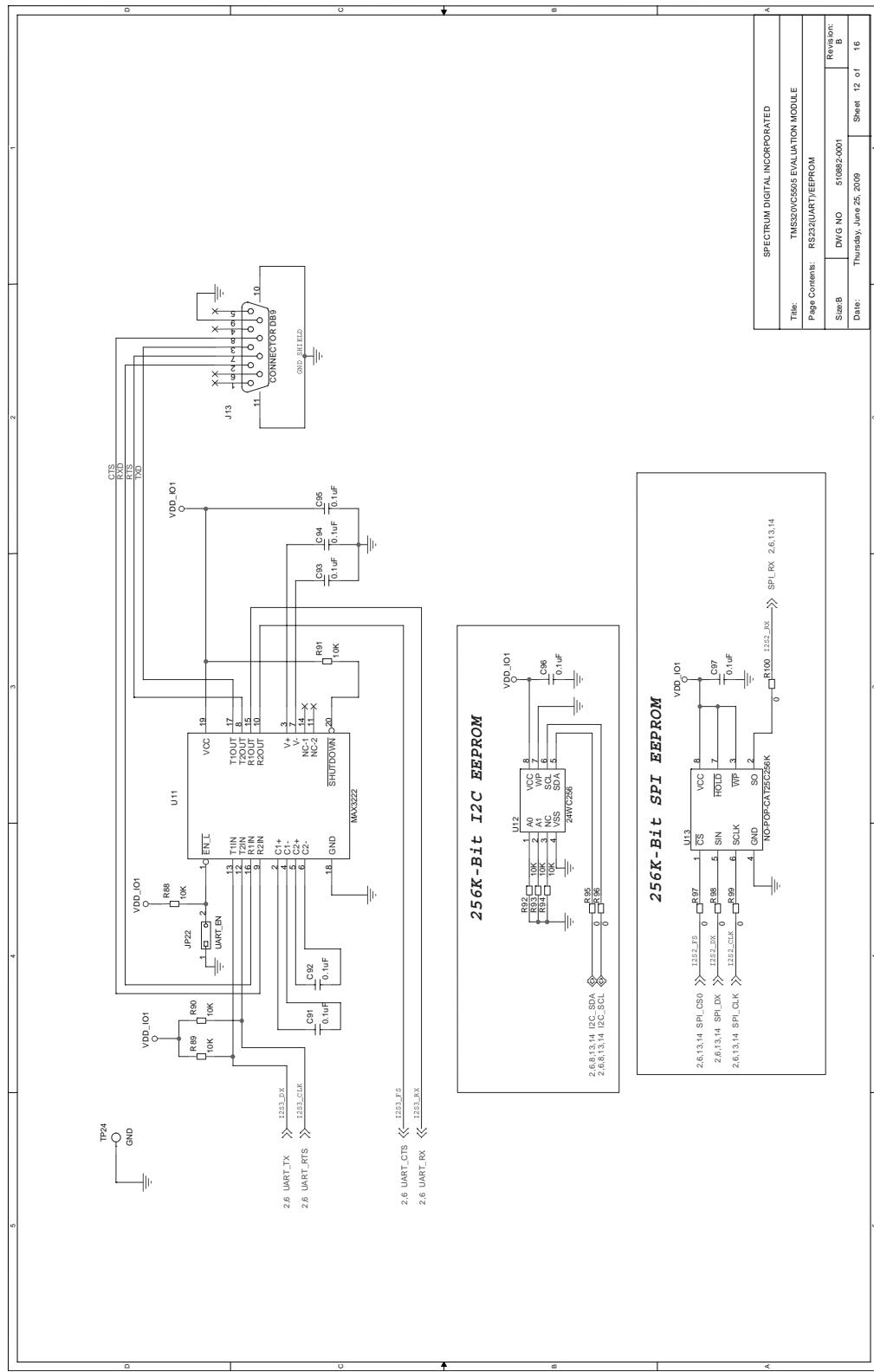


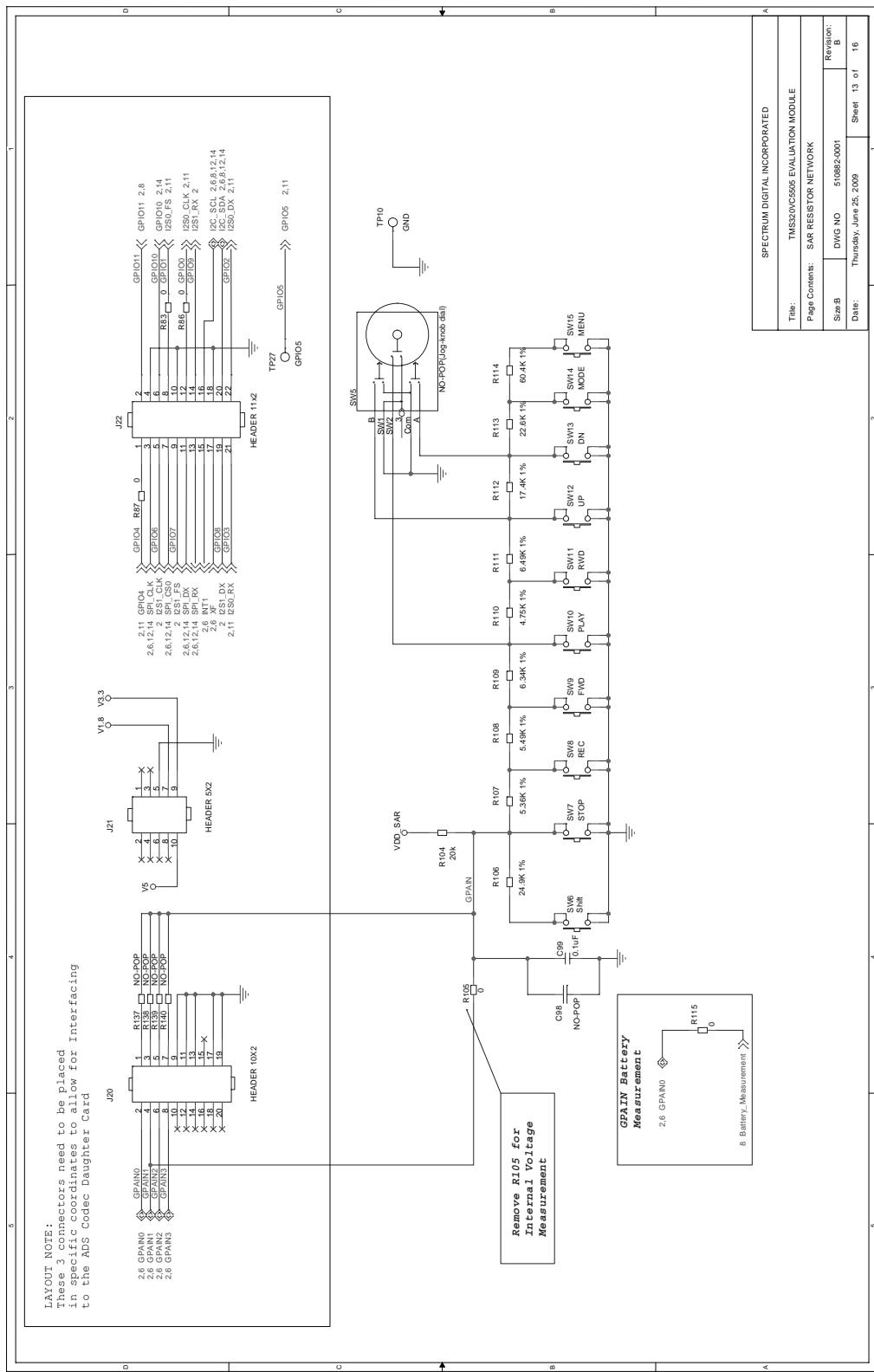


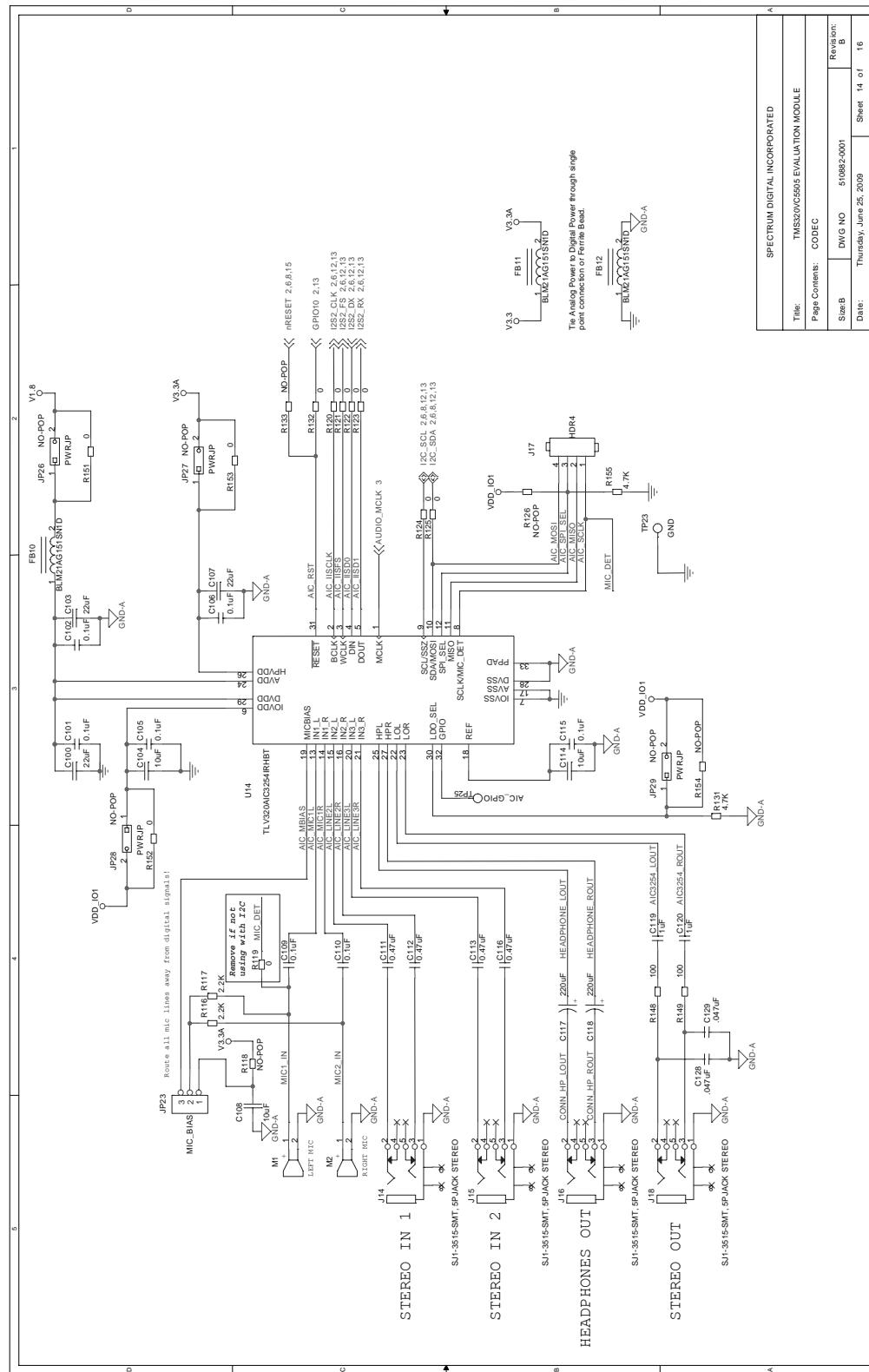


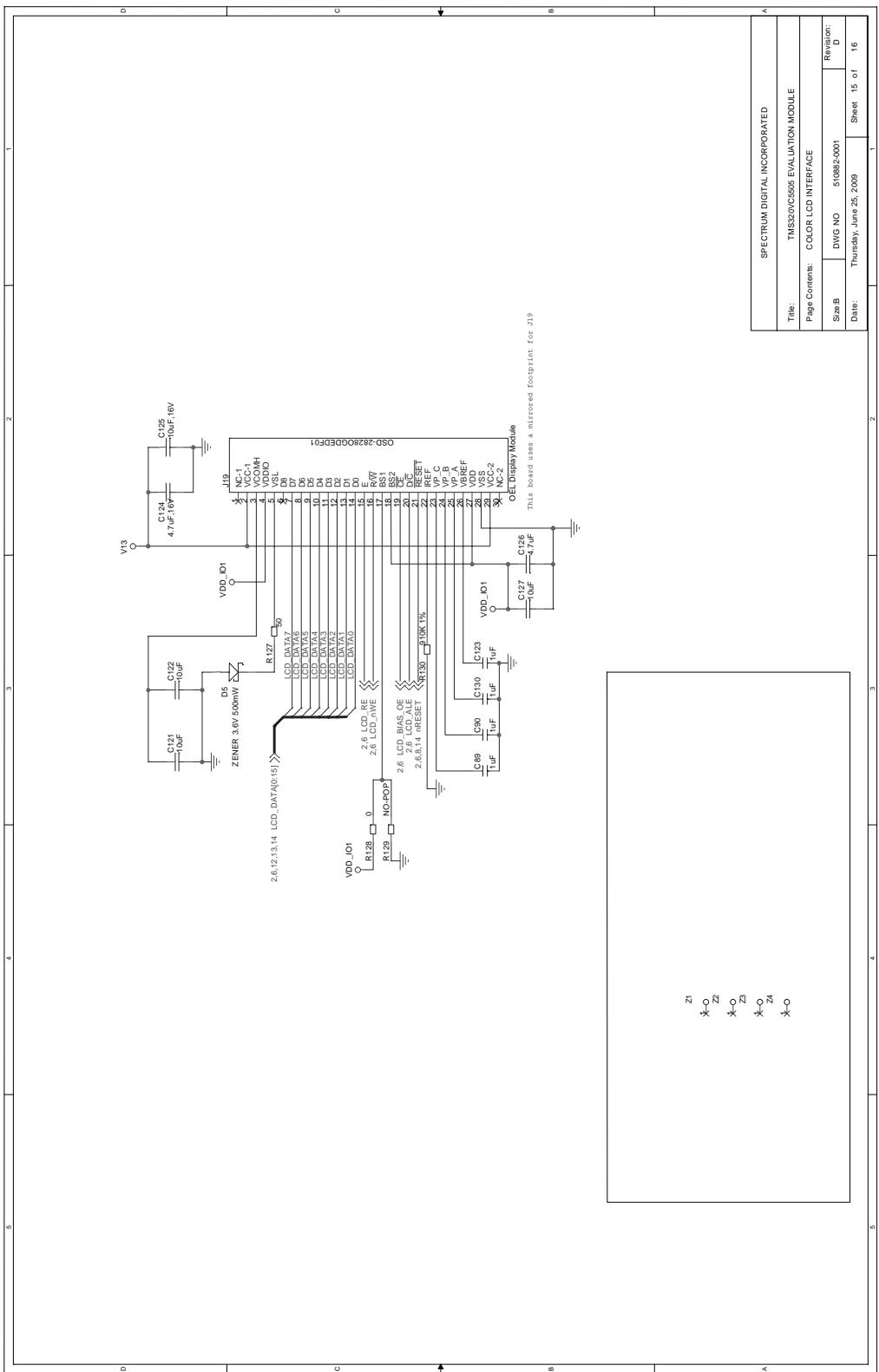


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| Size: B                       | DWG NO:                        | 510882-0001 | Revision: B |
| Date: Thursday, June 25, 2009 | Sheet 11 of 16                 |             | 1           |









| Revision     | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | DATE                 |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| 5.0540-0001B | Initial Release.<br>Updated Known bugs and notes on pages 2 and 6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 12/26/07<br>01/08/08 |
| 5.0880-0001A | <ul style="list-style-type: none"> <li>1. Change R50 to 1M</li> <li>2. Fix power on LCD connector. Swap 3.3V with 13V</li> <li>3. Fix ball F8 to be used as VSS_OSC</li> <li>4. Fix INIT0 and INIT1 swapped</li> <li>5. Fix CODEC so that I2C is selected by default</li> <li>6. Changed revision ID to 16 to USB_X instead of USB_XI</li> <li>7. Replaced D22 with 11V (same XY on pin 1)</li> <li>8. Replaced L25 on J22 with SPH</li> <li>9. Added test pin to Q1 P10</li> <li>10. Changes value of RER_R72 to 36K</li> <li>11. Added Embedded USB emulation option</li> </ul> | 02/18/08             |
| 5.0880-0001B | <ul style="list-style-type: none"> <li>1. Fixed Jog-Dial so that common dial switches ties to Qnd</li> <li>2. Fixed pull-up resistor net connected to DSP_LDO_V and LDO_EN</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                             | 03/09/08             |
| 5.0880-0001C | <ul style="list-style-type: none"> <li>1. NEW CPU REVISION</li> <li>2. ECN ON R21</li> <li>3. R13 CHANGED TO 0 OHM</li> <li>4. C54 NOT POPULATED</li> <li>5. C80 CHANGED TO 0.1uF</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                      | 12/09/08             |
| 5.0880-0001D | <ul style="list-style-type: none"> <li>1. NEW CPU REVISION</li> <li>2. MODIFIED POWER SEQUENCING</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                      |

|                                |                    |
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| SPECTRUM DIGITAL INCORPORATED  |                    |
| TMSS20/C5502 EVALUATION MODULE |                    |
| Page Content:                  | REVISION SUMMARY   |
| Size B                         | DWG NO 510882-0001 |
| Date: Thursday, June 25, 2009  | Sheet 16 of 16     |



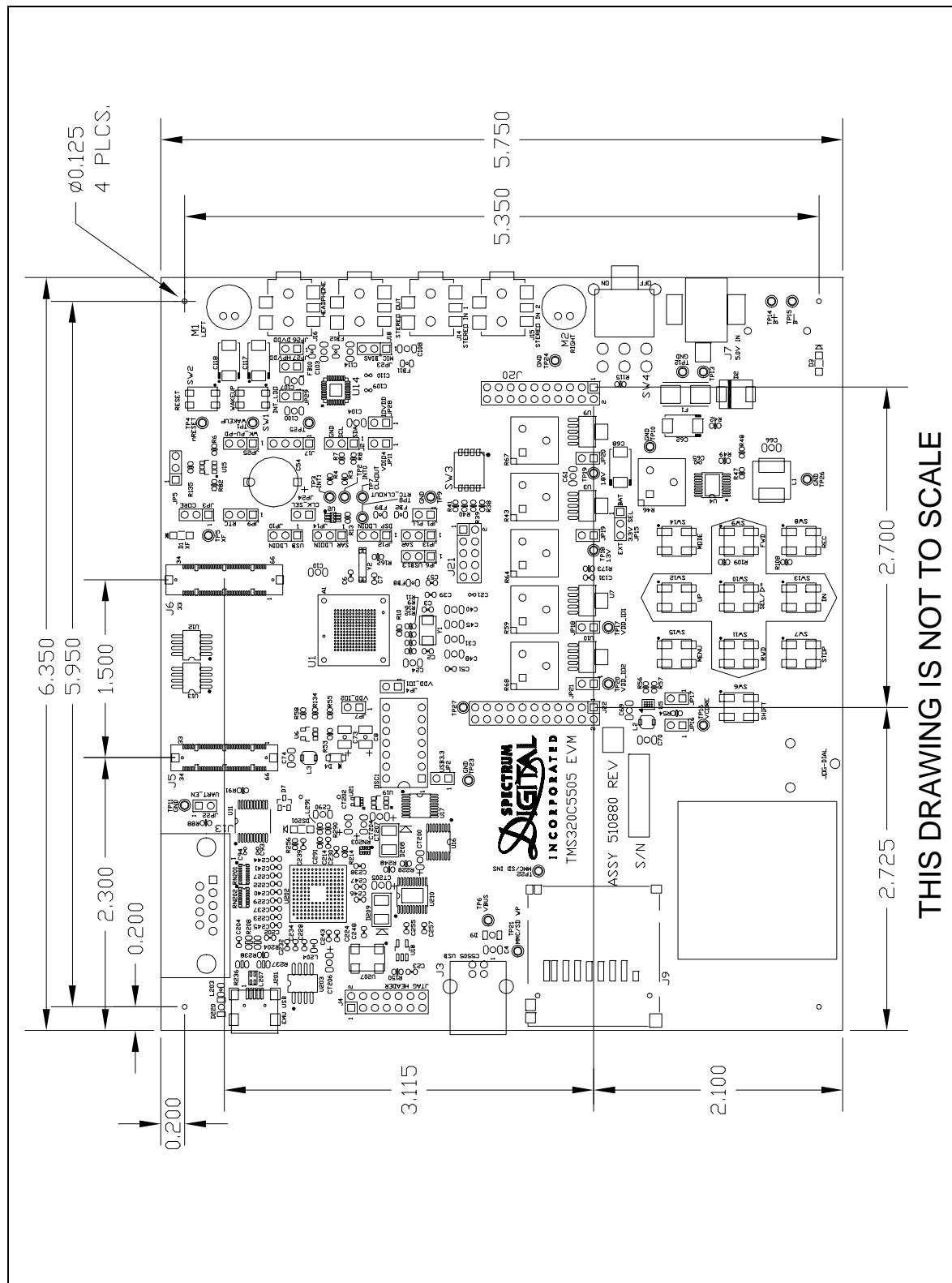
## **Appendix B**

### **Mechanical Information**

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This appendix contains the mechanical information about the TMS320VC5505 EVM produced by Spectrum Digital.

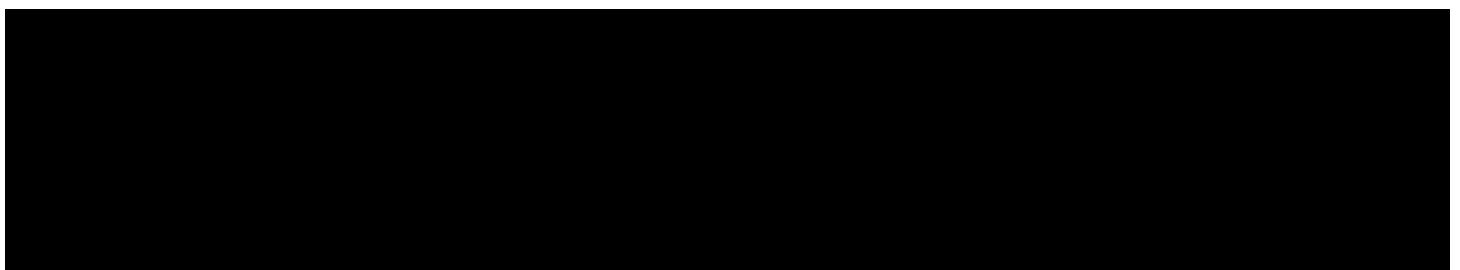


*Spectrum Digital, Inc*

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Printed in U.S.A., July 2009  
510885-0001 Rev. B