## 74LVC541A

## Low－Voltage CMOS Octal Buffer Flow Through Pinout

## With 5 V－Tolerant Inputs and Outputs （3－State，Non－Inverting）

The 74LVC541A is a high performance，non－inverting octal buffer operating from a 1.2 to 3.6 V supply．This device is similar in function to the MC74LCX244，while providing flow through architecture． High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance．A $\mathrm{V}_{\mathrm{I}}$ specification of 5.5 V allows 74LVC541A inputs to be safely driven from 5 V devices．The 74LVC541A is suitable for memory address driving and all TTL level bus oriented transceiver applications．

Current drive capability is 24 mA at the outputs．The Output Enable （ $\overline{\mathrm{OE} 1} . \overline{\mathrm{OE} 2}$ ）inputs，when HIGH ，disables the output by placing them in a HIGH Z condition．

## Features

－Designed for 1.2 to $3.6 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ Operation
－ 5 V Tolerant－Interface Capability With 5 V TTL Logic
－Supports Live Insertion and Withdrawal
－ $\mathrm{I}_{\mathrm{OFF}}$ Specification Guarantees High Impedance When $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$
－ 24 mA Output Sink and Source Capability
－Near Zero Static Supply Current in All Three Logic States（10 $\mu \mathrm{A}$ ）
Substantially Reduces System Power Requirements
－Latchup Performance Exceeds 250 mA
－ESD Performance：
－Human Body Model＞ 2000 V
－Machine Model＞ 200 V
－These Devices are $\mathrm{Pb}-$ Free，Halogen Free／BFR Free and are RoHS Compliant

ON Semiconductor ${ }^{\circledR}$
www．onsemi．com


MARKING DIAGRAMS

20日月月明日月月
LVC541A AWLYYWWG

1日时
SOIC－20 WB
20日月


TSSOP－20
A＝Assembly Location
L，WL＝Wafer Lot
Y，YY＝Year
W，WW＝Work Week
G or •＝Pb－Free Package
（Note：Microdot may be in either location）

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet．

## 74LVC541A



Figure 1. Pinout: 20-Lead (Top View)

PIN NAMES

| Pins | Function |
| :---: | :---: |
| $\overline{\mathrm{OEn}}$ | Output Enable Inputs |
| Dn | Data Inputs |
| On | 3-State Outputs |

TRUTH TABLE

| Inputs |  |  | Outputs |
| :---: | :---: | :---: | :---: |
| OE1 | OE2 | Dn | On |
| L | L | L | L |
| L | L | H | H |
| X | H | X | Z |
| H | X | X | Z |

[^0]

Figure 2. Logic Diagram

MAXIMUM RATINGS

| Symbol | Parameter | Value | Condition | Unit |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC Supply Voltage | -0.5 to +6.5 |  | V |
| $V_{1}$ | DC Input Voltage | $-0.5 \leq \mathrm{V}_{1} \leq+6.5$ |  | V |
| $\mathrm{V}_{\mathrm{O}}$ | DC Output Voltage | $-0.5 \leq \mathrm{V}_{\mathrm{O}} \leq+6.5$ | Output in 3-State | V |
|  |  | $-0.5 \leq \mathrm{V}_{\mathrm{O}} \leq \mathrm{V}_{\mathrm{CC}}+0.5$ | Output in HIGH or LOW State (Note 1) | V |
| IIK | DC Input Diode Current | -50 | $\mathrm{V}_{1}<$ GND | mA |
| $\mathrm{l}_{\text {OK }}$ | DC Output Diode Current | -50 | $\mathrm{V}_{\mathrm{O}}<$ GND | mA |
|  |  | +50 | $\mathrm{V}_{\mathrm{O}}>\mathrm{V}_{\mathrm{CC}}$ | mA |
| 10 | DC Output Source/Sink Current | $\pm 50$ |  | mA |
| $\mathrm{I}_{\mathrm{CC}}$ | DC Supply Current Per Supply Pin | $\pm 100$ |  | mA |
| $\mathrm{I}_{\text {GND }}$ | DC Ground Current Per Ground Pin | $\pm 100$ |  | mA |
| $\mathrm{T}_{\text {STG }}$ | Storage Temperature Range | -65 to +150 |  | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{L}}$ | Lead Temperature, 1 mm from Case for 10 Seconds | $\mathrm{T}_{\mathrm{L}}=260$ |  | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{J}$ | Junction Temperature Under Bias | $\mathrm{T}_{\mathrm{J}}=135$ |  | ${ }^{\circ} \mathrm{C}$ |
| $\theta_{\mathrm{JA}}$ | Thermal Resistance (Note 2) | $\begin{aligned} \text { SOIC } & =65.8 \\ \text { TSSOP } & =110.7 \end{aligned}$ |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| MSL | Moisture Sensitivity |  | Level 1 |  |
| ILATCHUP | Latch-up Performance at $\mathrm{V}_{\mathrm{CC}}=3.6 \mathrm{~V}$ and $125^{\circ} \mathrm{C}$ (Note 3) |  | $\pm 250$ | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Io absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm -by-1 inch, 2 ounce copper trace no air flow.
3. Tested to EIA/JESO78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage Operating Functional | $\begin{gathered} 1.65 \\ 1.2 \end{gathered}$ |  | $\begin{aligned} & 3.6 \\ & 3.6 \end{aligned}$ | V |
| $V_{1}$ | Input Voltage | 0 |  | 5.5 | V |
| $\mathrm{V}_{\mathrm{O}}$ | Output Voltage HIGH or LOW State 3-State | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\begin{gathered} V_{\mathrm{CC}} \\ 5.5 \end{gathered}$ | V |
| IOH | $\begin{gathered} \text { HIGH Level Output Current } \\ \mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}-3.6 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=2.7 \mathrm{~V}-3.0 \mathrm{~V} \end{gathered}$ |  |  | $\begin{aligned} & -24 \\ & -12 \end{aligned}$ | mA |
| lOL | $\begin{gathered} \text { LOW Level Output Current } \\ \mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}-3.6 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=2.7 \mathrm{~V}-3.0 \mathrm{~V} \end{gathered}$ |  |  | $\begin{aligned} & 24 \\ & 12 \end{aligned}$ | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Operating Free-Air Temperature | -40 |  | +125 | ${ }^{\circ} \mathrm{C}$ |
| $\Delta \mathrm{t} / \Delta \mathrm{V}$ | Input Transition Rise or Fall Rate, $\mathrm{V}_{\text {IN }}$ from 0.8 V to $2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ | 0 |  | 10 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |  | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | $\begin{array}{\|c\|} \hline \text { Typ } \\ \text { (Note 4) } \end{array}$ | Max | Min | $\begin{array}{\|c\|} \hline \text { Typ } \\ \text { (Note 4) } \end{array}$ | Max |  |
| VIH | HIGH-level input voltage | $\mathrm{V}_{\mathrm{CC}}=1.2 \mathrm{~V}$ | 1.08 | - | - | 1.08 | - | - | V |
|  |  | $\mathrm{V}_{\mathrm{CC}}=1.65 \mathrm{~V}$ to 1.95 V | $\begin{aligned} & 0.65 x \\ & V_{C C} \end{aligned}$ | - | - | $0.65 x$ | - | - |  |
|  |  | $\mathrm{V}_{\text {CC }}=2.3 \mathrm{~V}$ to 2.7 V | 1.7 | - | - | 1.7 | - | - |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$ to 3.6 V | 2.0 | - | - | 2.0 | - | - |  |
| $\mathrm{V}_{\text {IL }}$ | LOW-level input voltage | $\mathrm{V}_{\mathrm{CC}}=1.2 \mathrm{~V}$ | - | - | 0.12 | - | - | 0.12 | V |
|  |  | $\mathrm{V}_{\mathrm{CC}}=1.65 \mathrm{~V}$ to 1.95 V | - | - | $\begin{gathered} 0.35 x \\ V_{C C} \end{gathered}$ | - | - | $\begin{aligned} & 0.35 x \\ & V_{C C} \end{aligned}$ |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=2.3 \mathrm{~V}$ to 2.7 V | - | - | 0.7 | - | - | 0.7 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$ to 3.6 V | - | - | 0.8 | - | - | 0.8 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH-level output voltage | $\mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IH}}$ or $\mathrm{V}_{\mathrm{IL}}$ |  |  |  |  |  |  | V |
|  |  | $\begin{gathered} \mathrm{I}_{\mathrm{O}}=-100 \mu \mathrm{~A} ; \\ \mathrm{V}_{\mathrm{CC}}=1.65 \mathrm{~V} \text { to } 3.6 \mathrm{~V} \end{gathered}$ | $\begin{gathered} \mathrm{V}_{\mathrm{CC}-}- \\ 0.2 \end{gathered}$ | - | - | $\begin{gathered} \mathrm{V}_{\mathrm{CC}-}- \\ 0.3 \end{gathered}$ | - | - |  |
|  |  | $\mathrm{I}_{\mathrm{O}}=-4 \mathrm{~mA} ; \mathrm{V}_{\mathrm{CC}}=1.65 \mathrm{~V}$ | 1.2 | - | - | 1.05 | - | - |  |
|  |  | $\mathrm{l}_{\mathrm{O}}=-8 \mathrm{~mA} ; \mathrm{V}_{\mathrm{CC}}=2.3 \mathrm{~V}$ | 1.8 | - | - | 1.65 | - | - |  |
|  |  | $\mathrm{I}_{\mathrm{O}}=-12 \mathrm{~mA} ; \mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$ | 2.2 | - | - | 2.05 | - | - |  |
|  |  | $\mathrm{I}_{\mathrm{O}}=-18 \mathrm{~mA} ; \mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ | 2.4 | - | - | 2.25 | - | - |  |
|  |  | $\mathrm{I}_{\mathrm{O}}=-24 \mathrm{~mA} ; \mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ | 2.2 | - | - | 2.0 | - | - |  |
| VOL | LOW-level output voltage | $\mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IH}}$ or $\mathrm{V}_{\mathrm{IL}}$ |  |  |  |  |  |  | V |
|  |  | $\begin{gathered} \mathrm{I}_{\mathrm{O}}=100 \mu \mathrm{~A} ; \\ \mathrm{V}_{\mathrm{CC}}=1.65 \mathrm{~V} \text { to } 3.6 \mathrm{~V} \end{gathered}$ | - | - | 0.2 | - | - | 0.3 |  |
|  |  | $\mathrm{l}_{\mathrm{O}}=4 \mathrm{~mA} ; \mathrm{V}_{\mathrm{CC}}=1.65 \mathrm{~V}$ | - | - | 0.45 | - | - | 0.65 |  |
|  |  | $\mathrm{l}_{\mathrm{O}}=8 \mathrm{~mA} ; \mathrm{V}_{\mathrm{CC}}=2.3 \mathrm{~V}$ | - | - | 0.6 | - | - | 0.8 |  |
|  |  | $\mathrm{I}_{\mathrm{O}}=12 \mathrm{~mA} ; \mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$ | - | - | 0.4 | - | - | 0.6 |  |
|  |  | $\mathrm{I}_{\mathrm{O}}=-24 \mathrm{~mA} ; \mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ | - | - | 0.55 | - | - | 0.8 |  |
| 1 | Input leakage current | $\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}$ or GND $\mathrm{V}_{\mathrm{CC}}=3.6 \mathrm{~V}$ | - | $\pm 0.1$ | $\pm 5$ | - | $\pm 0.1$ | $\pm 20$ | $\mu \mathrm{A}$ |
| loz | OFF-state output current | $\begin{gathered} \mathrm{VI}=\mathrm{VIH} \text { or VIL; } \\ \mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V} \text { or GND; } \mathrm{V}_{\mathrm{CC}}=3.6 \mathrm{~V} \end{gathered}$ | - | $\pm 0.1$ | $\pm 5$ | - | $\pm 0.1$ | $\pm 20$ | $\mu \mathrm{A}$ |
| IOFF | Power-off leakage current | $\mathrm{V}_{1}$ or $\mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC}}=0.0 \mathrm{~V}$ | - | $\pm 0.1$ | $\pm 10$ | - | $\pm 0.1$ | $\pm 20$ | $\mu \mathrm{A}$ |
| $I_{\text {cc }}$ | Supply current | $\begin{gathered} V_{I}=V_{C C} \text { or } G N D ; I_{O}=0 A ; \\ V_{C C}=3.6 \mathrm{~V} \end{gathered}$ | - | 0.1 | 10 | - | 0.1 | 40 | $\mu \mathrm{A}$ |
| $\Delta \mathrm{l}_{\mathrm{CC}}$ | Additional supply current | $\begin{gathered} \text { per input pin; } \\ \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{CC}}-0.6 \mathrm{~V} ; \mathrm{I}_{\mathrm{O}}=0 \mathrm{~A} ; \\ \mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V} \text { to } 3.6 \mathrm{~V} \end{gathered}$ | - | 5 | 500 | - | 5 | 5000 | $\mu \mathrm{A}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. All typical values are measured at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}$, unless stated otherwise.

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{t}_{\mathrm{R}}=\mathrm{t}_{\mathrm{F}}=2.5 \mathrm{~ns}\right)$

| Symbol | Parameter | Conditions | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |  | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ ${ }^{1}$ | Max | Min | Typ ${ }^{1}$ | Max |  |
| $\mathrm{t}_{\mathrm{pd}}$ | Propagation Delay (Note 6) nAn to nYn | $\mathrm{V}_{\mathrm{CC}}=1.2 \mathrm{~V}$ | - | 14.0 | - | - | - | - | ns |
|  |  | $\mathrm{V}_{\mathrm{CC}}=1.65 \mathrm{~V}$ to 1.95 V | 1.5 | 6.5 | 13.8 | 1.5 | - | 16.0 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=2.3 \mathrm{~V}$ to 2.7 V | 1.0 | 3.5 | 6.8 | 1.0 | - | 7.9 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$ | 1.5 | 3.5 | 5.6 | 1.5 | - | 7.0 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ to 3.6 V | 1.0 | 2.9 | 5.1 | 1.0 | - | 6.5 |  |
| $\mathrm{t}_{\text {en }}$ | Enable Time (Note 7) nOE to nYn | $\mathrm{V}_{\mathrm{CC}}=1.2 \mathrm{~V}$ | - | 20.0 | - | - | - | - | ns |
|  |  | $\mathrm{V}_{\mathrm{CC}}=1.65 \mathrm{~V}$ to 1.95 V | 1.8 | 7.7 | 16.0 | 1.8 | - | 18.5 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=2.3 \mathrm{~V}$ to 2.7 V | 1.5 | 4.3 | 8.8 | 1.5 | - | 10.2 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$ | 1.5 | 4.4 | 7.5 | 1.5 | - | 9.5 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ to 3.6 V | 1.0 | 3.5 | 7.0 | 1.0 | - | 9.0 |  |
| $\mathrm{t}_{\text {dis }}$ | Disable Time (Note 8) nOE to nYn | $\mathrm{V}_{\mathrm{CC}}=1.2 \mathrm{~V}$ | - | 11.0 | - | - | - | - | ns |
|  |  | $\mathrm{V}_{\mathrm{CC}}=1.65 \mathrm{~V}$ to 1.95 V | 3.0 | 4.9 | 10.3 | 3.0 | - | 11.9 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=2.3 \mathrm{~V}$ to 2.7 V | 1.0 | 2.7 | 5.9 | 1.0 | - | 6.8 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$ | 1.5 | 3.7 | 7.0 | 1.5 | - | 9.0 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ to 3.6 V | 1.0 | 3.3 | 6.0 | 1.0 | - | 7.5 |  |
| $\mathrm{t}_{\text {sk(0) }}$ | Output Skew Time (Note 9) |  | - | - | 1 | - | - | 1.5 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. Typical values are measured at $\mathrm{TA}=25^{\circ} \mathrm{C}$ and $\mathrm{Vcc}=3.3 \mathrm{~V}$, unless stated otherwise.
6. $\mathrm{t}_{\mathrm{pd}}$ is the same as $\mathrm{t}_{\mathrm{PLH}}$ and $\mathrm{t}_{\mathrm{PHL}}$.
7. $\mathrm{t}_{\mathrm{en}}$ is the same as tpzL and tpzH.
8. $t_{\text {dis }}$ is the same as $t_{P L Z}$ and $t_{P H Z}$.
9. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

## DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Characteristic | Condition | $\mathrm{T}_{\mathrm{A}}=+\mathbf{2 5}{ }^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| VoLP | Dynamic LOW Peak Voltage (Note 10) | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{~V}_{\mathrm{IH}}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{C}_{\mathrm{L}}=30 \mathrm{pF}, \mathrm{~V}_{\mathrm{IH}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & \hline 0.8 \\ & 0.6 \end{aligned}$ |  | V |
| $\mathrm{V}_{\text {OLV }}$ | Dynamic LOW Valley Voltage (Note 10) | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{~V}_{\mathrm{IH}}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{C}_{\mathrm{L}}=30 \mathrm{pF}, \mathrm{~V}_{\mathrm{IH}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & \hline-0.8 \\ & -0.6 \end{aligned}$ |  | V |

10. Number of outputs defined as " $n$ ". Measured with " $n-1$ " outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Unit |
| :---: | :---: | :---: | :---: | :---: |
| CIN | Input Capacitance | $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{I}}=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{CC}}$ | 4.0 | pF |
| Cout | Output Capacitance | $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{I}}=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{CC}}$ | 5.0 | pF |
| $\mathrm{C}_{\text {PD }}$ | Power Dissipation Capacitance (Note 11) | Per input; $\mathrm{V}_{\mathrm{I}}=\mathrm{GND}$ or $\mathrm{V}_{\mathrm{CC}}$ |  | pF |
|  |  | $\mathrm{V}_{\mathrm{CC}}=1.65 \mathrm{~V}$ to 1.95 V | 7.7 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=2.3 \mathrm{~V}$ to 2.7 V | 11.3 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ to 3.6 V | 14.4 |  |

11. $C_{P D}$ is used to determine the dynamic power dissipation ( $P_{D}$ in $\mu W$ ).
$P_{D}=C_{P D} * V_{C C}{ }^{2} \times f i * N+\Sigma\left(C_{L} \times V_{C C}{ }^{2} \times f 0\right)$ where:
$\mathrm{fi}=$ input frequency in MHz ; fo = output frequency in MHz
$\mathrm{C}_{\mathrm{L}}=$ output load capacitance in $\mathrm{pF} \mathrm{V}_{\mathrm{CC}}=$ supply voltage in Volts
$\mathrm{N}=$ number of outputs switching
$\Sigma\left(\mathrm{C}_{\mathrm{L}} * \mathrm{~V}_{\mathrm{CC}}{ }^{2} \times \mathrm{fo}\right)=$ sum of the outputs.

## 74LVC541A



Figure 3. AC Waveforms

|  | $\mathrm{V}_{\mathbf{C C}}$ |  |  |
| :---: | :---: | :---: | :---: |
| Symbol | $\mathbf{3 . 3} \mathbf{V} \pm \mathbf{0 . 3} \mathrm{V}$ | $\mathbf{2 . 7} \mathrm{V}$ | $\mathrm{V}_{\mathbf{C C}}<\mathbf{2 . 7} \mathbf{V}$ |
| $\mathrm{Vmi}^{2}$ | 1.5 V | 1.5 V | $\mathrm{~V}_{\mathrm{CC}} / 2$ |
| $\mathrm{Vmo}^{2}$ | 1.5 V | 1.5 V | $\mathrm{~V}_{\mathrm{CC}} / 2$ |
| $\mathrm{~V}_{\mathrm{HZ}}$ | $\mathrm{V}_{\mathrm{OL}}+0.3 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{OL}}+0.3 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{OL}}+0.15 \mathrm{~V}$ |
| $\mathrm{~V}_{\mathrm{LZ}}$ | $\mathrm{V}_{\mathrm{OH}}-0.3 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{OH}}-0.3 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{OH}}-015 \mathrm{~V}$ |

## 74LVC541A



| Supply Voltage | Input |  | Load |  | $\mathrm{V}_{\text {EXT }}$ |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{Cc}}$ (V) | $\mathrm{V}_{1}$ | $t_{r}, t_{f}$ | $\mathrm{C}_{\mathrm{L}}$ | $\mathbf{R}_{\mathrm{L}}$ | $\mathrm{t}_{\text {PLH }}, \mathrm{t}_{\text {PHL }}$ | $\mathrm{t}_{\text {PLZ }}, \mathrm{t}_{\text {PZL }}$ | $\mathrm{t}_{\text {PHZ }}, \mathrm{t}_{\text {PZH }}$ |
| 1.2 | $\mathrm{V}_{\mathrm{CC}}$ | $\leq 2 \mathrm{~ns}$ | 30 pF | $1 \mathrm{k} \Omega$ | Open | $2 \times V_{\text {CC }}$ | GND |
| 1.65-1.95 | $\mathrm{V}_{\mathrm{CC}}$ | $\leq 2 \mathrm{~ns}$ | 30 pF | $1 \mathrm{k} \Omega$ | Open | $2 \times V_{C C}$ | GND |
| 2.3-2.7 | $\mathrm{V}_{\mathrm{CC}}$ | $\leq 2 \mathrm{~ns}$ | 30 pF | $500 \Omega$ | Open | $2 \times V_{\text {CC }}$ | GND |
| 2.7 | 2.7 V | $\leq 2.5 \mathrm{~ns}$ | 50 pF | $500 \Omega$ | Open | $2 \times V_{\text {CC }}$ | GND |
| 3-3.6 | 2.7 V | $\leq 2.5 \mathrm{~ns}$ | 50 pF | $500 \Omega$ | Open | $2 \times V_{C C}$ | GND |

Figure 4. Test Circuit
ORDERING INFORMATION

| Device | Package | Shipping $^{\dagger}$ |
| :--- | :--- | :---: |
| 74LVC541ADWR2G | SOIC-20 <br> (Pb-Free) | $1000 /$ Tape \& Reel |
| 74LVC541ADTR2G | TSSOP-20 <br> (Pb-Free) | $2500 /$ Tape \& Reel |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## 74LVC541A

## PACKAGE DIMENSIONS

TSSOP-20
CASE 948E-02
ISSUE C


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION

MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE

MOLD FLASH, PROTRUSIONS OR GATE
BURRS. MOLD FLASH OR GATE BURRS
SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION. SHALL NOT EXCEED 0.25 (0.010) PER SIDE 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08
$(0.003)$ TOTAL IN EXCESS OF THE K (0.003) TOTAL IN EXCESS OF THE K
DIMENSION AT MAXIMUM MATERIAL DIMENSION
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
|  | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC |  | 0.026 |  |
| BSC |  |  |  |  |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | 0.252 BSC |  |  |
| M | $0^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ |

SOLDERING FOOTPRINT*

*For additional information on our $\mathrm{Pb}-$ Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

SOIC-20 WB
CASE 751D-05
ISSUE G


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B SHALL BE 0.13 TOTAL IN EXCESS OF
DIMENSION AT MAXIMUM MATERIAL DIMENSION
CONDITION.

|  | MILLIMETERS |  |
| :---: | :---: | ---: |
|  | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 | BSC |
| $\mathbf{H}$ | 10.05 | 10.55 |
| $\mathbf{h}$ | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| $\boldsymbol{\theta}$ | $0^{\circ}$ | $7^{\circ}$ |

[^1]
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[^0]:    H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable, for ICC reasons, DO NOT FLOAT Inputs

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