

# Bipolar Power Transistor Data

**ON Semiconductor™**

Datasheet Support

The logo consists of a large green circle with a white shadow underneath. Inside the circle, the letters "ON" are written in a bold, white, sans-serif font. The "O" is a simple circle, and the "N" is a simple vertical bar with a diagonal stroke. The letters have a slight drop shadow, making them appear to float slightly above the green background.

**ON**

# Bipolar Power Transistor Data

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# **CHAPTER 1**

## **Selector Guide**

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# Bipolar Power Transistors

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## In Brief . . .



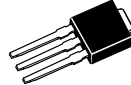


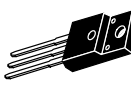
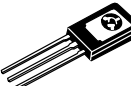


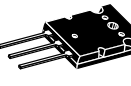

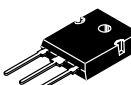

ON Semiconductor's broad line of Bipolar Power Transistors includes discrete and Darlington transistors in a variety of packages from the popular surface mount DPAK at 1.75 watts to the 250 watt TO-3. We now have transistors in SO-8 (Dual Transistors) and SOT-223. We have a broad line of Electronic Lamp Ballast Transistors, in the BUL Series and MJD18002D2T4, MJE18002, and MJE18004D24. New products include low  $V_{CE(sat)}$  devices in surface mount SOT-223 package, MMJT9435T1/MMJT9410T1 and in the SO-8 package (Dual Transistors), MMDJ3N03BJTR2/MMDJ3P03BJTR2. We also have a broad line of high performance Audio Output Transistors in TO-3, TO-264 and new products in the Isolated Hole Plastic TO-247 package. The new TO-247 devices are designated MJW21191/2/3/4/5/6 and high  $f_T$ , MJW3281A/1302A. These have excellent high voltage FBSOA performance. ON Semiconductor has a commitment to quality and total customer satisfaction.

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# BIPOLAR POWER TRANSISTORS SELECTOR GUIDE

## SELECTION BY PACKAGE

Package		$I_C$ Range (Amps)	$V_{CE}$ Range (Volts)	$P_D$ (Watts)
	TO-204AA (TO-3)	4.0-30	40-250	115-250
	TO-204AE (TO-3)	30-60	60-120	150-300
	DPAK	0.5-10	40-450	12.5-20
	DPAK	0.5-10	40-450	12.5-20
	TO-220AB	0.5-15	60-400	30-125
	Isolated TO-220 Type	1.0-12	60-450	20-45
	TO-225AA (TO-126 Type)	0.3-5.0	25-400	12.5-40
	SOT-223	3.0	30	2.0 (Note 1.)
	SO-8	3.0	30	2.0 (Note 2.)
	TO-264	15-16	200-250	250
	D²PAK	5.0-8.0	80-450	50-65
	TO-247	8.0-16	150-250	200
	TO-218	5.0-10	60-350	125-150

1. Tested on 1" sq. FR4 Board
2. Tested on 1" sq., 2 oz. copper

## Plastic TO–220AB

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min (Note 7.)	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Resistive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
1.0	80	TIP29B	TIP30B	15/75	1.0	0.6 typ	0.3 typ	1.0	3.0	30	725
	100	TIP29C	TIP30C	15/75	1.0	0.6 typ	0.3 typ	1.0	3.0	30	725
	250	TIP47		30/150	0.3	2.0 typ	0.18 typ	0.3	10	40	747
	300	TIP48	MJE5730	30/150	0.3	2.0 typ	0.18 typ	0.3	10	40	747, 581
	350		<b>MJE5731</b>	30/150	0.3	2.0 typ	0.18 typ	0.3	10	40	581
	400	<b>TIP50</b>	<b>MJE5731A</b> (Note 6.)	30/150	0.3	2.0 typ	0.18 typ	0.3	10	40	747, 581
2.0	60	TIP110 (Note 4.)	TIP115 (Note 4.)	500 min	2.0	1.7 typ	1.3 typ	2.0	25 (Note 3.)	50	709
	80	TIP111 (Note 4.)	TIP116 (Note 4.)	500 min	2.0	1.7 typ	1.3 typ	2.0	25 (Note 3.)	50	709
	100	<b>TIP112</b> (Note 4.)	<b>TIP117</b> (Note 4.)	500 min	2.0	1.7 typ	1.3 typ	2.0	25 (Note 3.)	50	709
	400/700	<b>BUL44</b>		14/36	0.4	2.75 (Note 5.)	0.175 (Note 5.)	1.0	13 typ	50	279
	450/1000	<b>BUX85</b>		30	0.1	3.5	1.4	1.0	4.0	50	313
	450/1000	<b>MJE18002</b>		14/34	0.2	3.0 (Note 5.)	0.17 (Note 5.)	1.0	12 typ	40	505
3.0	60	TIP31A	TIP32A	25 min	1.0	0.6 typ	0.3 typ	1.0	3.0	40	729
	80	<b>TIP31B</b>	<b>TIP32B</b>	25 min	1.0	0.6 typ	0.3 typ	1.0	3.0	40	729
	100	BD241C	BD242C	25 min	1.0				3.0	40	157
		<b>TIP31C</b>	<b>TIP32C</b>	25 min	1.0	0.6 typ	0.3 typ	1.0	3.0	40	729
4.0	80	<b>D44C12</b>	<b>D45C12</b>	40/120	0.2			1.0	40 typ	30	320
	400/700	<b>MJE13005</b>		6/30	3.0	3.0	0.7	3.0	4.0	60	468
5.0	60	TIP120 (Note 4.)	TIP125 (Note 4.)	1k min	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 3.)	65	715
	80	TIP121 (Note 4.)	TIP126 (Note 4.)	1k min	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 3.)	65	715
	100	<b>TIP122</b> (Note 4.)	<b>TIP127</b> (Note 4.)	1k min	3.0	1.5 typ	1.5 typ	4.0	4.0 (Note 3.)	75	715
	250	2N6497		10/75	2.5	1.8	0.8	2.5	5.0	80	133
	400/700	<b>BUL45</b>		14/34	0.3	1.7 (Note 5.)	0.15 (Note 5.)	1.0	12 typ	75	296
	450/1000	<b>MJE18004</b>		14/34	0.3	1.7	0.15	1.0	13	75	522
		MJE18004D2*									512

3. |h<sub>FE</sub>| @ 1.0 MHz

4. Darlington

5. Switching tests performed with special application simulator circuit. See data sheet for details.

6. V<sub>CEO</sub> = 375 V

7. When 2 voltages are given, the format is V<sub>CEO(sus)</sub>/V<sub>CES</sub>.

\*D2 suffix indicates transistor with built in C–E freewheeling diode and antisaturation network.

Devices listed in **bold**, *italic* are ON Semiconductor preferred devices.

## Plastic TO-220AB (continued)

I <sub>C</sub> Cont Amps Max	V <sub>CE0(sus)</sub> Volts Min (Note 11.)	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Resistive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
6.0	60	TIP41A	TIP42A	15/75	3.0	0.4 typ	0.15 typ	3.0	3.0	65	742
	80	TIP41B	TIP42B	15/75	3.0	0.4 typ	0.15 typ	3.0	3.0	65	742
		<b>BD243B</b>	<b>BD244B</b>	15 min	3.0	0.4 typ	0.15 typ	3.0	3.0	65	162
	100	<b>BD243C</b>	<b>BD244C</b>	15 min	3.0	0.4 typ	0.15 typ	3.0	3.0	65	162
		<b>TIP41C</b>	<b>TIP42C</b>	15/75	3.0	0.4 typ	0.15 typ	3.0	3.0	65	742
	400/700	<b>BUL146</b>		14/34	0.5	1.75 (Note 10.)	0.15 (Note 10.)	3.0	14 typ	100	263
	450/1000	<b>MJE18006</b>		14/34	0.5	3.2 (Note 10.)	0.13 (Note 10.)	3.0	14 typ	100	531
7.0	30	2N6288	2N6111	30/150	3.0	0.4 typ	0.15 typ	3.0	4.0	40	107
	50		2N6109	30/150	2.5	0.4 typ	0.15 typ	3.0	4.0	40	107
	70	2N6292	2N6107	30/150	2.0	0.4 typ	0.15 typ	3.0	4.0	40	107
	150	BU407		30 min	1.5		0.75	5.0	10	60	214
	200	<b>BU406</b>		30 min	1.5		0.75	5.0	10	60	214
8.0	60	2N6043 (Note 9.)	2N6040 (Note 9.)	1k/10k	4.0	1.5 typ	1.5 typ	3.0	4.0 (Note 8.)	75	98
		TIP100 (Note 9.)	TIP105 (Note 9.)	1k/20k	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 8.)	80	704
	80	<b>BDX53B</b> (Note 9.)	<b>BDX54B</b> (Note 9.)	750 min	3.0				4.0 (Note 8.)	60	203
		<b>TIP101</b> (Note 9.)	<b>TIP106</b> (Note 9.)	1k/20k	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 8.)	80	704
	100	<b>2N6045</b> (Note 9.)	<b>2N6042</b> (Note 9.)	1k/10k	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 8.)	75	98
		<b>BDX53C</b> (Note 9.)	<b>BDX54C</b> (Note 9.)	750 min	3.0						203
		<b>TIP102</b> (Note 9.)	<b>TIP107</b> (Note 9.)	1k/20k	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 8.)	80	704
	120	MJE15028	MJE15029	20 min	4.0				30	50	492
	150	<b>MJE15030</b>	<b>MJE15031</b>	20 min	4.0				30	50	492
	300/600	MJE5740 (Note 9.)		200 min	4.0	8.0 typ	2.0 typ	6.0	4.0	80	585
	300		MJE5850	15 min	2.0	2.0	0.5	4.0		80	590
	350		<b>MJE5851</b>	15 min	2.0	2.0	0.5	4.0		80	590
	400	<b>MJE5742</b> (Note 9.)		200 min	4.0	8.0 typ	2.0 typ	6.0		80	585
		<b>MJE13007</b>		5/30	5.0	3.0	0.7	5.0		80	474
			<b>MJE5852</b>	15 min	2.0	2.0	0.5	4.0		80	590

8. |h<sub>FE</sub>| @ 1.0 MHz

9. Darlington

10. Switching tests performed with special application simulator circuit. See data sheet for details.

11. When 2 voltages are given, the format is V<sub>CE0(sus)</sub>/V<sub>CES</sub>.

Plastic TO–220AB (continued)

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min (Note 15.)	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Resistive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
8.0	400/700	<b>BUL147</b>		14/34	1.0	2.5 (Note 14.)	0.18 (Note 14.)	2.0	14 typ	125	272
	450/1000	<b>MJE18008</b>		16/34	1.0	2.75 (Note 14.)	0.18 (Note 14.)	2.0	13 typ	125	538
10	60	D44H8	D45H8	40 min	4.0					50	320
		<b>MJE3055T</b>	<b>MJE2955T</b>	20/70	4.0					75	560
		<b>2N6387</b> (Note 13.)	<b>2N6667</b> (Note 13.)	1k/20k	5.0				20 (Note 12.)	65	121, 137
	80	<b>BDX33B</b> (Note 13.)	<b>BDX34B</b> (Note 13.)	750 min	3.0				3.0	70	197
		<b>BD809</b>	<b>BD810</b>	15 min	4.0				1.5	90	183
		<b>2N6388</b> (Note 13.)	<b>2N6668</b> (Note 13.)	1k/20k	5.0				20 (Note 12.)	65	121, 137
		D44H10	D45H10	20 min	4.0	0.5 typ	0.14 typ	5.0	50 typ	50	316
		<b>D44H11</b>	<b>D45H11</b>	40 min	4.0	0.5 typ	0.14 typ	5.0	50 typ	50	316
	100	<b>BDX33C</b> (Note 13.)	<b>BDX34C</b> (Note 13.)	750 min	3.0				3.0	70	197
12	400/700	<b>MJE13009</b>		6/30	8.0	3.0	0.7	8.0	4.0	100	483
15	60	2N6487	2N6490	20/150	5.0	0.6 typ	0.3 typ	5.0	5.0	75	127
	80	<b>2N6488</b>	<b>2N6491</b>	20/150	5.0	0.6 typ	0.3 typ	5.0	5.0	75	127
		<b>D44VH10</b>	<b>D45VH10</b>	20 min	4.0	0.5	0.09	8.0	50 typ	83	318
	100	<b>BDW42</b> (Note 13.)	<b>BDW47</b> (Note 13.)	1k min	5.0	1.0 typ	1.5 typ	5.0	4.0	85	190

12. |h<sub>FE</sub>| @ 1.0 MHz

13. Darlington

14. Switching tests performed with special application simulator circuit. See data sheet for details.

15. When 2 voltages are given, the format is V<sub>CEO(sus)</sub>/V<sub>CES</sub>.

## Plastic TO–218 Type

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min (Note 18.)	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Resistive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
10	60	TIP140 (Note 17.)	TIP145 (Note 17.)	500 min	10	2.5 typ	2.5 typ	5.0	4.0 (Note 16.)	125	720
		TIP141 (Note 17.)	TIP146 (Note 17.)	500 min	10	2.5 typ	2.5 typ	5.0	4.0 (Note 16.)	125	720
	100	<b>BDV65B</b> (Note 17.)	<b>BDV64B</b> (Note 17.)	1k min	5.0					125	187
		TIP33C	TIP34C	20/100	3.0				3.0	80	734
		<b>TIP142</b> (Note 17.)	<b>TIP147</b> (Note 17.)	500 min	10	2.5 typ	2.5 typ	5.0	4.0 (Note 16.)	125	720
	350	BU323Z (Note 17.)		500/3400	5.0			6.0		150	209
15	60	<b>TIP3055</b>	<b>TIP2955</b>	5 min	10				2.5	80	727
	150	MJH11018 (Note 17.)	MJH11017 (Note 17.)	400/15k	10				3.0	150	634
	200	MJH11020 (Note 17.)	MJH11019 (Note 17.)	400/15k	10				3.0	150	634
	250	<b>MJH11022</b> (Note 17.)	<b>MJH11021</b> (Note 17.)	400/15k	10				3.0	150	634
16	160	<b>MJE4343</b>	<b>MJE4353</b>	15 min	8.0	1.2 typ	1.2 typ	8.0	1.0	125	574
20	100	<b>MJH6284</b> (Note 17.)	<b>MJH6287</b> (Note 17.)	750/18k	10				4.0	125	640
25	60	TIP35A	TIP36A	15/75	15	0.6 typ	0.3 typ	10	3.0	125	737
	100	<b>TIP35C</b>	<b>TIP36C</b>	15/75	15	0.6 typ	0.3 typ	10	3.0	125	737

16. |h<sub>FE</sub>| @ 1.0 MHz

17. Darlington

18. When 2 voltages are given, the format is V<sub>CEO(sus)</sub>/V<sub>CES</sub>.

## Plastic (Isolated TO-220 Type)

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	V <sub>CES</sub> Volts Min	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Resistive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
			NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
1.0	250		<i>MJF47</i>		30/150	0.3	2.0 typ	0.17 typ	0.3	10	28	622
3.0	100		<i>MJF31C</i>	<i>MJF32C</i>	10 min	1.0	0.6	0.3	1.0	3.0	28	729
5.0	100		<i>MJF122</i> (Note 20.)	<i>MJF127</i> (Note 20.)	2000 min	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 19.)	28	601
	450	1000	<i>MJF18004</i>		14/34	0.3	1.7 (Note 21.)	0.15 (Note 21.)	1.0	13 typ	35	522
8.0	150		<i>MJF15030</i>	<i>MJF15031</i>	40 min	3.0	1.0 typ	0.15 typ	3.0	30	35	608
	450	1000	<i>MJF18008</i>		16/34	1.0	2.75 (Note 21.)	0.18 (Note 21.)	2.0	13 typ	45	538
10	60		<i>MJF3055</i>	<i>MJF2955</i>	20/100	4.0				2.0	40	614
	80		<i>MJF44H11</i>	<i>MJF45H11</i>	40/100	4.0	0.5 typ	0.14 typ	5.0	40	35	618
	100		<i>MJF6388</i> (Note 20.)	<i>MJF6668</i> (Note 20.)	3k/20k	3.0	1.5 typ	1.5 typ		20 (Note 19.)	40	627

## Large Plastic TO-264

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Resistive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
15	200	<i>MJL3281A</i>	<i>MJL1302A</i>	60/175	5.0				30 typ	200	655
16	250	<i>MJL21194</i>	<i>MJL21193</i>	25/75	8.0				4.0	200	644
		<i>MJL21196</i>	<i>MJL21195</i>	25/75	8.0				4.0	200	649

19. |h<sub>FE</sub>| @ 1.0 MHz

20. Darlington

21. Switching tests performed with special application simulator circuit. See data sheet for details.

## Plastic TO–225AA Type (Formerly TO–126 Type)

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Resistive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
0.3	350	<b>MJE3439</b>		40/160	0.02				15	15	566
0.5	200	<b>MJE344</b>		30/300	0.05				15	20.8	568
	250	2N5655		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20	80
	300	<b>MJE340</b>	<b>MJE350</b>	30/240	0.05					20.8	563, 570
	350	<b>2N5657</b>		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20	80
		<b>BD159</b>		30/240	0.05					20	146
1.0	40	2N4921	2N4918	20/100	0.5	0.6 typ	0.3 typ	0.5	3.0	30	55, 50
	60	2N4922	2N4919	20/100	0.5	0.6 typ	0.3 typ	0.5	3.0	30	55, 50
	80	<b>2N4923</b>	<b>2N4920</b>	20/100	0.5	0.6 typ	0.3 typ	0.5	3.0	30	55, 50
1.5	45	BD135	BD136	40/250	0.15					12.5	142, 144
	60	BD137	BD138	40/250	0.15					12.5	142, 144
	80	<b>BD139</b>	<b>BD140</b>	40/250	0.15					12.5	142, 144
	400	<b>MJE13003</b> (Note 24.)		5/25	1.0	4.0	0.7	1.0	5.0	40	461
2.0	80	<b>BD237</b>	<b>BD238</b>	25 min	1.0				3.0	25	154
	100	<b>MJE270</b> (Notes 23. & 24.)	<b>MJE271</b> (Notes 23. & 24.)	1.5k min	0.12				6.0	15	558
3.0	60	MJE181	MJE171	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5	501
	80	<b>BD179</b>	<b>BD180</b>	40/250	0.15					25	148, 151
		<b>MJE182</b>	<b>MJE172</b>	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5	501
	500	<b>BUH51</b> (Note 24.)		8.0 min	1.0					50	254
4.0	40	<b>MJE521</b>	<b>MJE371</b>	40 min	1.0					40	579, 572
	45	<b>BD437</b>	<b>BD438</b>	40 min	2.0				3.0	36	166, 169
	60	<b>BD439</b>	<b>BD440</b>	25 min	2.0				3.0	36	166, 169
		<b>BD677</b> (Note 23.)	<b>BD678</b> (Note 23.)	750 min	1.5					40	172, 175
		<b>BD677A</b> (Note 23.)	<b>BD678A</b> (Note 23.)	750 min	1.5					40	172, 175
		<b>BD787</b>	<b>BD788</b>	20 min	2.0				50	15	178
		<b>2N5191</b>	<b>2N5194</b>	25/100	1.5	0.4 typ	0.4 typ	1.5	2.0	40	62, 67
		<b>MJE800</b> (Note 23.)	<b>MJE700</b> (Note 23.)	750 min	1.5				1.0 (Note 22.)	40	596
		<b>2N6038</b> (Note 23.)	<b>2N6035</b> (Note 23.)	750/18k	2.0	1.7 typ	1.2 typ	2.0	25	40	92

22. |h<sub>FE</sub>| @ 1.0 MHz  
 23. Darlington  
 24. Case 77, Style 3

Plastic TO–225AA Type (Formerly TO–126 Type) (continued)

I <sub>C</sub> Cont Amps Max	V <sub>CE0(sus)</sub> Volts Min	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Resistive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
4.0	80	<b>2N5192</b>	<b>2N5195</b>	25/100	1.5	0.4 typ	0.4 typ	1.5	2.0	40	62, 67
		<b>BD441</b>	<b>BD442</b>	15 min	2.0				3.0	36	166, 169
		<b>BD679</b> (Note 26.)	<b>BD680</b> (Note 26.)	750 min	1.5					40	172, 175
		<b>BD679A</b> (Note 26.)	<b>BD680A</b> (Note 26.)	750 min	2.0					40	172, 175
		<b>MJE802</b> (Note 26.)	<b>MJE702</b> (Note 26.)	750 min	1.5				1.0 (Note 25.)	40	596
		<b>MJE803</b> (Note 26.)	<b>MJE703</b> (Note 26.)	750 min	2.0				1.0 (Note 25.)	40	596
		<b>2N6039</b> (Note 26.)	<b>2N6036</b> (Note 26.)	750/18k	2.0	1.7 typ	1.2 typ	2.0	25	40	92
	100	<b>BD681</b> (Note 26.)	<b>BD682</b> (Note 26.)	750 min	1.5					40	172, 175
		<b>MJE243</b>	<b>MJE253</b>	40/120	0.2	0.15 typ	0.07 typ	2.0	40	15	553
5.0	25	<b>MJE200</b>	<b>MJE210</b>	45/180	2	0.13 typ	0.035 typ	2.0	65	15	548

25. |h<sub>FE</sub>| @ 1.0 MHz  
26. Darlington



## DPAK – Surface Mount Power Packages

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Resistive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
0.5	300	<b>MJD340T4</b>	<b>MJD350T4</b>	30/240	0.05					15	438
1.0	250	MJD47T4		30/150	0.3	2.0	0.2	0.3	10	15	452
	400	<b>MJD50T4</b>		30/150	0.3	2.0	0.2	0.3	10	15	452
2.0	100	<b>MJD112T4</b> (Note 28.)	<b>MJD117T4</b> (Note 28.)	1000 min	2.0	1.7	1.3	2.0	25 (Note 27.)	20	395
	450	<b>MJD18002D2T4</b>		6.0 min	2.0	1.0 typ	0.15 typ	1.0	13 typ	25	407
3.0	40	MJD31T4	MJD32T4	10 min	1.0	0.6	0.3	1.0	3.0	15	433
	100	<b>MJD31CT4</b>	<b>MJD32CT4</b>	10 min	1.0	0.6	0.3	1.0	3.0	15	433
4.0	80	<b>MJD6039T4</b> (Note 28.)	<b>MJD6036T4</b> (Note 28.)	1k/2k	2.0	1.7	1.2	2.0	25	20	456
	100	<b>MJD243T4</b>	<b>MJD253T4</b>	40/180	0.2	0.16	0.04	1.0	40	12.5	423
5.0	25	<b>MJD200T4</b>	<b>MJD210T4</b>	45/180	2.0	0.15	0.04	2.0	65	12.5	418
6.0	100	<b>MJD41CT4</b>	<b>MJD42CT4</b>	15/75	3.0	0.4	0.15	3.0	3.0	20	442
8.0	80	<b>MJD44H11T4</b>	<b>MJD45H11T4</b>	40 min	4.0	0.5	0.14	5.0	50 typ	20	448
	100	<b>MJD122T4</b> (Note 28.)	<b>MJD127T4</b> (Note 28.)	1k/2k	4.0	1.5	2.0	4.0	4 (Note 27.)	20	401
10	60	<b>MJD3055T4</b>	<b>MJD2955T4</b>	20/100	4.0	1.5	1.5	3.0	2.0	20	429
	80	<b>MJD44ET4</b> (Note 28.)		1k min	5.0	2.0	0.5	10		20	446

27. |h<sub>FE</sub>| @ 1.0 MHz

28. Darlington

## Metal TO-204AA (Formerly TO-3)

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min (Note 31.)	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Resistive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
4.0	250	<b>MJ15020</b>	<b>MJ15021</b>	30 min	1.0				20	150	344
10	140	2N3442		20/70	4.0					117	35
	250	<b>MJ15011</b>	<b>MJ15012</b>	20/100	2.0					200	342
12	100		<b>2N6052</b> (Note 30.)	750/18k	6.0	1.6 typ	1.5 typ	6.0	4.0 (Note 29.)	150	102
15	60	<b>2N3055</b>	<b>MJ2955</b>	20/70	4.0	0.7 typ	0.3 typ	4.0	2.5	115	31
		<b>2N3055A</b>		20/70	4.0				0.8	115	25
	120	<b>MJ15015</b>	<b>MJ15016</b>	20/70	4.0	0.7 typ	0.3 typ	4.0	1.0	180	25
	140	MJ15001	MJ15002	25/150	4.0				2.0	200	337
	250	<b>MJ11022</b> (Note 30.)	<b>MJ11021</b> (Note 30.)	100 min	15				3.0 (Note 29.)	175	325
16	140	<b>2N3773</b>	2N6609	15/60	8.0	1.1 typ	1.5 typ	8.0	4.0	150	46
		2N5631	2N6031	15/60	8.0	1.2 typ	1.2 typ	8.0	1.0	200	76
	200	MJ15022	MJ15023	15/60	8.0				5.0	250	346, 349
	250	<b>MJ15024</b>	<b>MJ15025</b>	15/60	8.0				5.0	250	346, 349
		<b>MJ21194</b>	<b>MJ21193</b>	25/75	8.0				4.0	250	352
		<b>MJ21196</b>	<b>MJ21195</b>	25/75	8.0				4.0	250	357
20	60	<b>2N3772</b>		15/60	10				2.0	150	38
	80	<b>2N6283</b> (Note 30.)	2N6286 (Note 30.)	750/18k	10	2.5 typ	2.5 typ	10	4.0 (Note 29.)	160	112
	90	2N5038		20/100	12	1.5	0.5	12	60	140	60
	100	<b>2N6284</b> (Note 30.)	<b>2N6287</b> (Note 30.)	750/18k	10	2.5 typ	2.5 typ	10	4.0 (Note 29.)	160	112
	140	<b>MJ15003</b>	<b>MJ15004</b>	25/150	5.0				2.0	250	340
25	60	2N5885	2N5883	20/100	10	1.0	0.8	10	4.0	200	87
	80	<b>2N5886</b>	<b>2N5884</b>	20/100	10	1.0	0.8	10	4.0	200	87
	100	2N6338		30/120	10	1.0	0.25	10	40	200	118
	150	<b>2N6341</b>		30/120	10	1.0	0.25	10	40	200	118

29. |h<sub>FE</sub>| @ 1.0 MHz

30. Darlington

31. When 2 voltages are given, the format is V<sub>CEO(sus)</sub>/V<sub>CES</sub>.

**Metal TO–204AA (Formerly TO–3) (continued)**

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min (Note 34.)	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Resistive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
30	40	<b>2N3771</b>		15/60	15				2.0	150	42
	60	2N5302		15/60	15	2.0	1.0	10	2.0	200	72
		MJ11012 (Note 33.)		1k min	20				4.0 (Note 32.)	200	322
	100	<b>MJ802</b>	<b>MJ4502</b>	25/100	7.5				2.0	200	364, 362
	120	<b>MJ11016</b> (Note 33.)	<b>MJ11015</b> (Note 33.)	1k min	20				4.0 (Note 32.)	200	322
	250	<b>MJ11022</b> (Note 33.)	<b>MJ11021</b> (Note 33.)	400/15k	10				3.0 (Note 32.)	200	325
40	200	BUV21 (Note 35.)		10 min	25	1.8	0.4	25	8.0	150	307
	250	<b>BUV22</b> (Note 35.)		10 min	20	1.1	0.35	20	8.0	250	310
50	80	<b>2N5686</b> (Note 35.)	<b>2N5684</b> (Note 35.)	15/60	25	0.5 typ	0.3 typ	25	2.0	300	83
	120	<b>MJ11032</b> (Note 33. & 35.)	<b>MJ11033</b> (Note 33. & 35.)	400 min	50					300	330
	125	<b>BUV20</b> (Note 35.)		10 min	50	1.2	0.25	50	8.0	250	304
		<b>BUV60</b> (Note 35.)		10 min	80	1.1	0.25	80		250	304
60	80	<b>MJ14002</b> (Note 35.)	<b>MJ14003</b> (Note 35.)	15/100	50					300	333

32. |h<sub>FE</sub>| @ 1.0 MHz

33. Darlington

34. When 2 voltages are given, the format is V<sub>CEO(sus)</sub>/V<sub>CES</sub>.

35. Case 197A–03 (TO–204AE)

## Isolated Mounting Hole – Plastic TO–247

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Inductive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
8.0	150	MJW21192	MJW21191	15 min	8.0				4.0	100	660
16	250	MJW21194*	MJW21193*	20/60	8.0				4.0	200	665
16	250	MJW21196*	MJW21195*	20/60	8.0				4.0	200	671
15	230	MJW3281A*	MJW1302A*	60/175	5.0				30	200	677

## D<sup>2</sup>PAK

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Inductive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
5.0	450/1000	MJB18004D2T4		6.0	2.0	2.4	0.175	2.5	13 typ	75	367
6.0	100		MJB42CT4	15/75	3.0				3.0	65	381
8.0	80	MJB44H11T4	MJB45H11T4	40/100	4.0	0.5 typ	0.14	5.0	40	50	388

## SOT–223

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Inductive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
3.0	30	MMJT9410T1	MMJT9435T1	50	1.0					0.8	694, 699
0.5	30		MMJT350T1	30/240	0.05					0.8	692

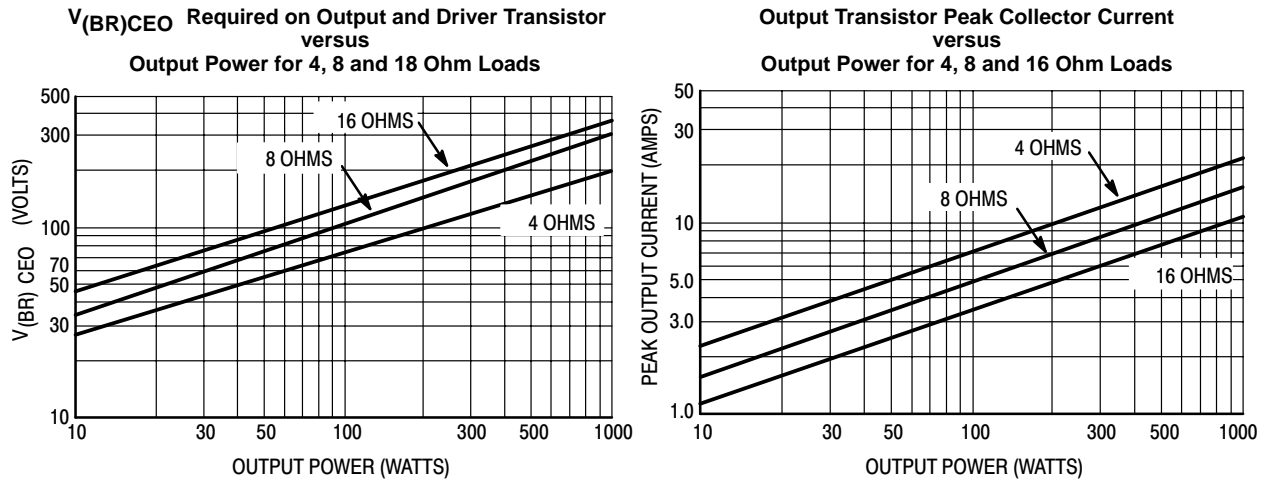
## SO–8 (Dual Transistors)

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Inductive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
3.0	30	MMDJ3N03BJTR2	MMDJ3P03BJTR2	50	1.0				30	2.0	682, 687

\*Available in Q2, 2001.

# Audio

## GENERAL DESIGN CURVES FOR POWER AUDIO OUTPUT STAGES



Another important parameter that must be considered before selecting the output transistors is the safe-operating area these devices must withstand. For a complete discussion see Application Note AN485.

### Recommended Power Transistors for Audio/Servo Loads

RMS Power Output	NPN	PNP	Case	P <sub>D</sub> Watts @ 25°C	V <sub>CEO</sub>	h <sub>FE</sub> @ Min/Max	I <sub>C</sub> Amps	f <sub>T</sub> MHz Typ	ISB Volts/Amps	Page
To 25 W	MJE15030	MJE15031	TO-220	50	150	20 min	4.0	30	14/3.6	492
	MJE15032	MJE15033	TO-220	50	250	50 min	1.0	30	50/1.0	497
25 to 50 W	2N3055A	MJ2955A	TO-204	120	120	20/70	4.0	3.0	60/2.0	25
	MJ15001	MJ15002	TO-204	200	140	25/150	4.0	3.0	40/5.0	337
50 to 100 W	MJ15015	MJ15016	TO-204	180	120	20/70	4.0	3.0	60/3.0	25
	MJ15003	MJ15004	TO-204	250	140	25/150	5.0	3.0	100/1.0	340
	MJ15020	MJ15021	TO-204	150	250	30 min	1.0	30	50/3.0	344
Over 100 W	MJ15024	MJ15025	TO-204	250	250	15/60	8.0	4.0	80/2.2	346, 349
	MJL3281A	MJL1302A	340G-02	150	200	60/175	7.0	30	40/4.0	655
	MJ21194	MJ21193	TO-204	250	250	25/75	8.0	4.0	100/2.0	352
	MJL21194	MJL21193	340G-02	200	200	25/75	8.0	4.0	100/2.0	644
	MJL21196	MJL21195	340G-02	200	200	25/75	8.0	4.0	100/2.0	649
	MJW21192	MJW21191	340K-01	100	150	15 min	4.0	4.0	50/3.0	660
	MJW21194	MJW21193	340K-01	200	250	20/60	8.0	4.0	50/4.0	665
	MJW21196	MJW21195	340K-01	200	250	25/60	8.0	4.0	50/4.0	671
MJW3281A	MJW1302A	340K-01	200	200	60/175	5.0	30	50/4.0	677	

The Power Transistors shown are provided for reference only and show device capability. The final choice of the Power Transistors used is left to the circuit designer and depends upon the particular safe-operating area required and the mounting and heat sinking configuration used.

# Bipolar Power Transistors for Electronic Lamp Ballasts

## Plastic TO-220AB

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	V <sub>CES</sub> Volts Min	Device Type	I <sub>C</sub> Operating Amps	h <sub>FE</sub> min @ I <sub>C</sub> Operating V <sub>CE</sub> = 1.0 V	Inductive Switching @ I <sub>C</sub> Operating T <sub>si</sub> Min/Max (μs)	P <sub>D</sub> (Case) Watts @ 25°C	Page
2.0	400	700	BUL44	0.8	10	2.6 / 3.8	50	279
	450	1000	MJE18002	1.0	6.0	/ 2.75	50	505
4.0	500	800	BUH50	2.0	8.0 typ	/ 2.5	50	246
5.0	400	700	BUL45	2.0	7.0	2.6 / 3.8	75	296
	400	700	BUL45D2*	2.0	10	1.95 / 2.25	75	286
	450	1000	MJE18004	2.0	6.0	/ 2.5	75	522
	450	1000	MJE18004D2*	2.0	6.0	2.1 / 2.4	75	512
6.0	400	700	BUL146	3.0	8.0	2.6 / 3.8	100	263
	450	1000	MJE18006	3.0	6.0	/ 3.2	100	531
8.0	400	700	BUL147	4.5	8.0	2.6 / 3.8	125	272
	450	1000	MJE18008	4.5	6.0	/ 3.2	125	538
10	400	700	BUH100	5.0	10 typ	/ 3.0	100	226
15	400	700	BUH150	10	8.0 typ	/ 2.75	150	236

BUHXXX Series are specified for Halogen applications.

\*D2 suffix indicates transistor with built in C-E freewheeling diode and antisaturation network.

# Bipolar Power Transistors for Electronic Lamp Ballasts

Case 221D-02 is UL RECOGNIZED for its isolation feature. Case 221D-02 has been evaluated to 3500 volts RMS. Actual isolation rating depends on specific mounting position and maintaining required strike and creepage distances.

## Plastic (Isolated TO-220 Type)

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	V <sub>CES</sub> Volts Min	Device Type	I <sub>C</sub> Operating Amps	h <sub>FE</sub> min @ I <sub>C</sub> Operating V <sub>CE</sub> = 1.0 V	Inductive Switching @ I <sub>C</sub> Operating T <sub>si</sub> Min/Max (μs)	P <sub>D</sub> (Case) Watts @ 25°C	Page
5.0	450	1000	MJF18004	2.0	6.0	/ 2.5	35	522
6.0	400	700	BUL146F	3.0	8.0	2.6 / 3.8	40	263
8.0	450	1000	MJF18008	4.5	6.0	/ 3.2	45	538

## Surface Mount Power Packages – DPAK

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	V <sub>CES</sub> Volts Min	Device Type	I <sub>C</sub> Operating Amps	h <sub>FE</sub> min @ I <sub>C</sub> Operating V <sub>CE</sub> = 1.0 V	Inductive Switching @ I <sub>C</sub> Operating T <sub>si</sub> Min/Max (μs)	P <sub>D</sub> (Case) Watts @ 25°C	Page
2.0	400	700	BUD44D2-1*	0.8	20 typ	2.05 / 2.35	25	216

## Surface Mount Power Packages – DPAK

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> / V <sub>CES</sub> Volts Min	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Inductive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
2.0	450/1000	MJD18002D2T4		6.0	1.0	1.2	0.150	1.0 A	13 typ	25	407

## D<sup>2</sup>PAK

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> / V <sub>CES</sub> Volts Min	Device Type		h <sub>FE</sub> Min/Max	@ I <sub>C</sub> Amp	Inductive Switching			f <sub>T</sub> MHz Min	P <sub>D</sub> (Case) Watts @ 25°C	Page
		NPN	PNP			t <sub>s</sub> μs Max	t <sub>f</sub> μs Max	@ I <sub>C</sub> Amp			
5.0	450/1000	MJB18004D2T4		6.0	2.0	2.4	0.175	2.5 A	13 typ	75	367

## Plastic TO-225AA Type (Formerly TO-126 Type)

I <sub>C</sub> Cont Amps Max	V <sub>CEO(sus)</sub> Volts Min	V <sub>CES</sub> Volts Min	Device Type	I <sub>C</sub> Operating Amps	h <sub>FE</sub> min @ I <sub>C</sub> Operating V <sub>CE</sub> = 1.0 V	Inductive Switching @ I <sub>C</sub> Operating T <sub>si</sub> Min/Max (μs)	P <sub>D</sub> (Case) Watts @ 25°C	Page
1.5	400	700	MJE13003 (Note 36.)	1.0	6.0 typ	/ 3.0	40	461
3.0	500	800	BUH51 (Note 36.)	1.0	8.0	/ 3.75	50	254

36. Case 77, Style 3

BUHXXX Series are specified for Halogen applications.

\*D2 suffix indicates transistor with built in C-E freewheeling diode and antisaturation network.

# **CHAPTER 2**

## **Data Sheets**

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# Complementary Silicon High-Power Transistors

...PowerBase™ complementary transistors designed for high power audio, stepping motor and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters, inverters, or for inductive loads requiring higher safe operating area than the 2N3055.

- Current-Gain — Bandwidth-Product @  $I_C = 1.0 \text{ Adc}$   
 $f_T = 0.8 \text{ MHz (Min) - NPN}$   
 $= 2.2 \text{ MHz (Min) - PNP}$
- Safe Operating Area — Rated to 60 V and 120 V, Respectively

### \*MAXIMUM RATINGS

Rating	Symbol	2N3055A	MJ15015 MJ15016	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	120	Vdc
Collector-Base Voltage	$V_{CBO}$	100	200	Vdc
Collector-Emitter Voltage Base Reversed Biased	$V_{CEV}$	100	200	Vdc
Emitter-Base Voltage	$V_{EBO}$	7.0		Vdc
Collector Current — Continuous	$I_C$	15		Adc
Base Current	$I_B$	7.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	115 0.65	180 1.03	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200		$^\circ\text{C}$

### THERMAL CHARACTERISTICS

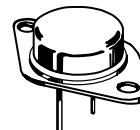
Characteristic	Symbol	Max	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	0.98	$^\circ\text{C/W}$

\*Indicates JEDEC Registered Data. (2N3055A)

**NPN**  
**2N3055A**  
**MJ15015 \***  
**PNP**  
**MJ15016 \***

\*ON Semiconductor Preferred Device

**15 AMPERE**  
**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**60, 120 VOLTS**  
**115, 180 WATTS**



**CASE 1-07**  
**TO-204AA**  
**(TO-3)**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# 2N3055A MJ15015 MJ15016

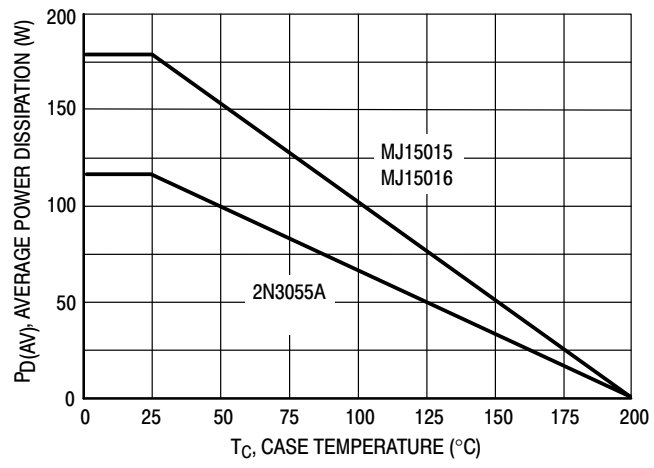


Figure 1. Power Derating

## 2N3055A MJ15015 MJ15016

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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#### OFF CHARACTERISTICS (1)

*Collector–Emitter Sustaining Voltage ( $I_C = 200\text{ mA}$ , $I_B = 0$ )	2N3055A MJ15015, MJ15016	$V_{CEO(sus)}$	60 120	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $V_{BE(off)} = 0\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{BE(off)} = 0\text{ Vdc}$ )	2N3055A MJ15015, MJ15016	$I_{CEO}$	— —	0.7 0.1	mA
*Collector Cutoff Current ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ )	2N3055A MJ15015, MJ15016	$I_{CEV}$	— —	5.0 1.0	mA
Collector Cutoff Current ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	2N3055A MJ15015, MJ15016	$I_{CEV}$	— —	30 6.0	mA
Emitter Cutoff Current ( $V_{EB} = 7.0\text{ Vdc}$ , $I_C = 0$ )	2N3055A MJ15015, MJ15016	$I_{EBO}$	— —	5.0 0.2	mA

#### \*SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ( $t = 0.5\text{ s}$ non-repetitive) ( $V_{CE} = 60\text{ Vdc}$ )	2N3055A MJ15015, MJ15016	$I_{S/b}$	1.95 3.0	— —	A
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#### \*ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 4.0\text{ A}$ , $V_{CE} = 2.0\text{ Vdc}$ ) ( $I_C = 4.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 10\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	10 20 5.0	70 70 —	—
Collector–Emitter Saturation Voltage ( $I_C = 4.0\text{ A}$ , $I_B = 400\text{ mA}$ ) ( $I_C = 10\text{ A}$ , $I_B = 3.3\text{ A}$ ) ( $I_C = 15\text{ A}$ , $I_B = 7.0\text{ A}$ )	$V_{CE(sat)}$	— — —	1.1 3.0 5.0	Vdc
Base–Emitter On Voltage ( $I_C = 4.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	0.7	1.8	Vdc

#### \*DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 1.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	2N3055A, MJ15015 MJ15016	$f_T$	0.8 2.2	6.0 18	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )		$C_{ob}$	60	600	pF

#### \*SWITCHING CHARACTERISTICS (2N3055A only)

RESISTIVE LOAD					
Delay Time	$(V_{CC} = 30\text{ Vdc}$ , $I_C = 4.0\text{ A}$ , $I_{B1} = I_{B2} = 0.4\text{ A}$ , $t_p = 25\text{ }\mu\text{s}$ Duty Cycle $\leq 2\%$ )	$t_d$	—	0.5	$\mu\text{s}$
Rise Time		$t_r$	—	4.0	$\mu\text{s}$
Storage Time		$t_s$	—	3.0	$\mu\text{s}$
Fall Time		$t_f$	—	6.0	$\mu\text{s}$

(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

\*Indicates JEDEC Registered Data. (2N3055A)

2N3055A MJ15015 MJ15016

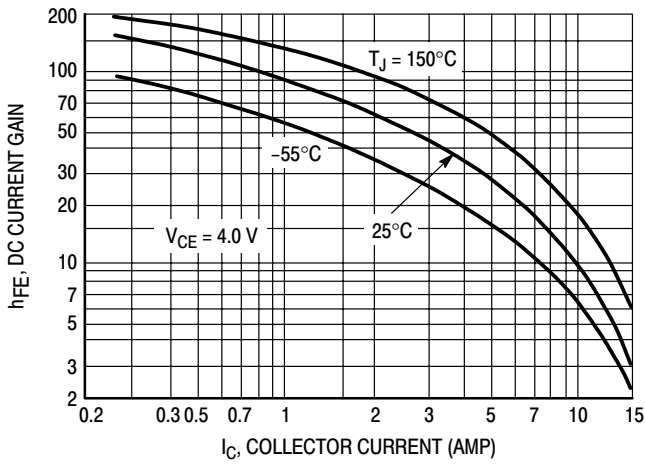


Figure 2. DC Current Gain

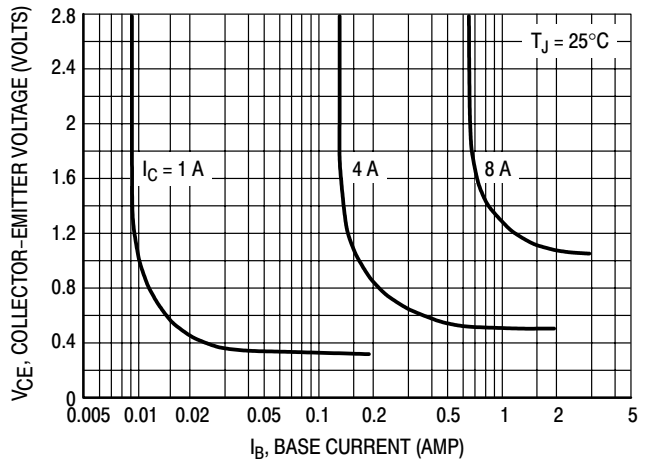


Figure 3. Collector Saturation Region

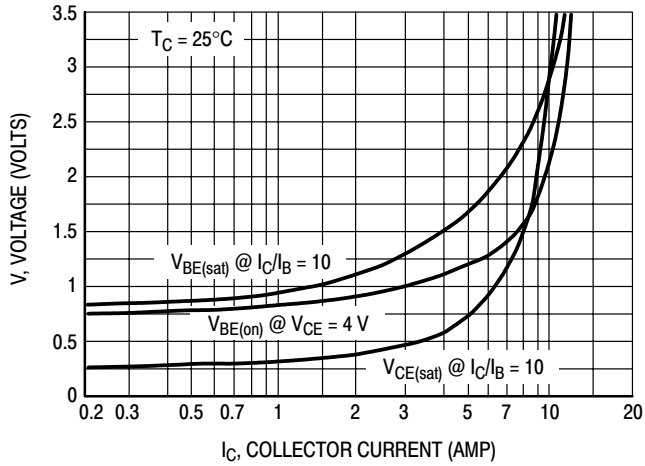


Figure 4. "On" Voltages

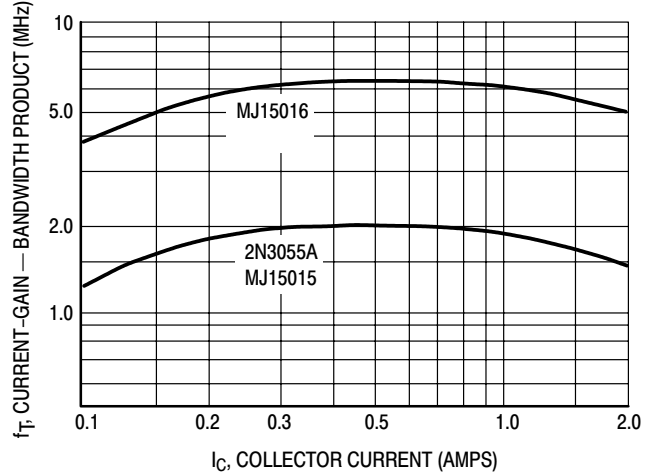


Figure 5. Current-Gain — Bandwidth Product

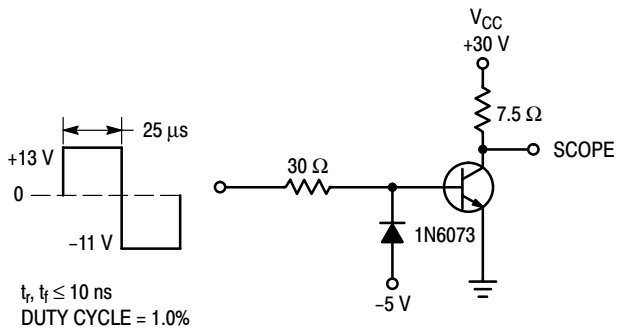


Figure 6. Switching Times Test Circuit (Circuit shown is for NPN)

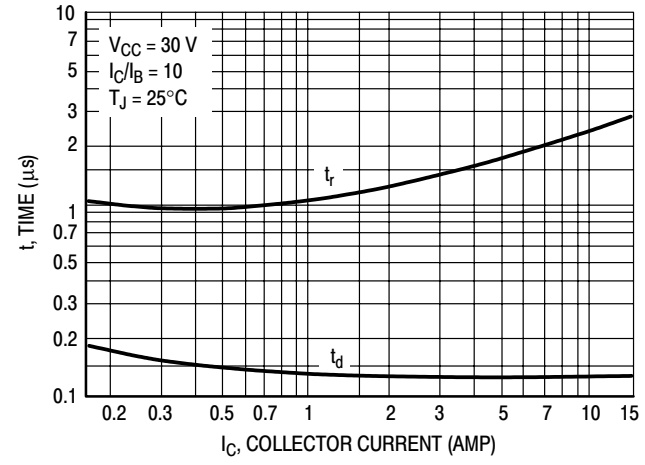
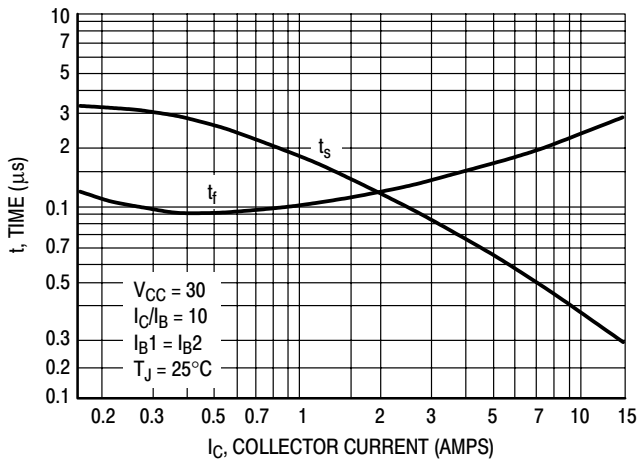
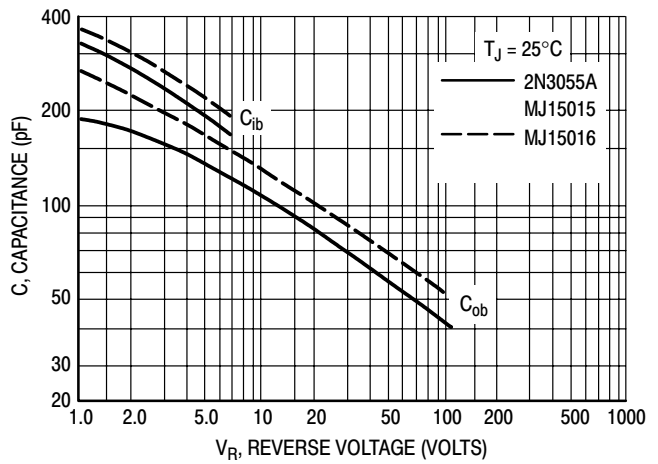


Figure 7. Turn-On Time

## 2N3055A MJ15015 MJ15016

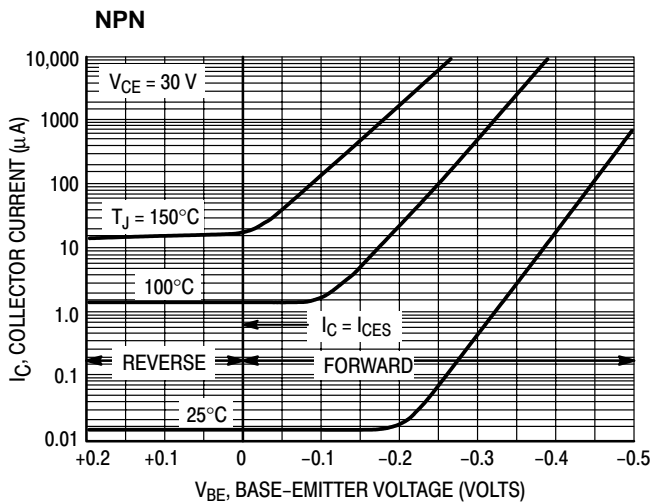


**Figure 8. Turn-Off Times**

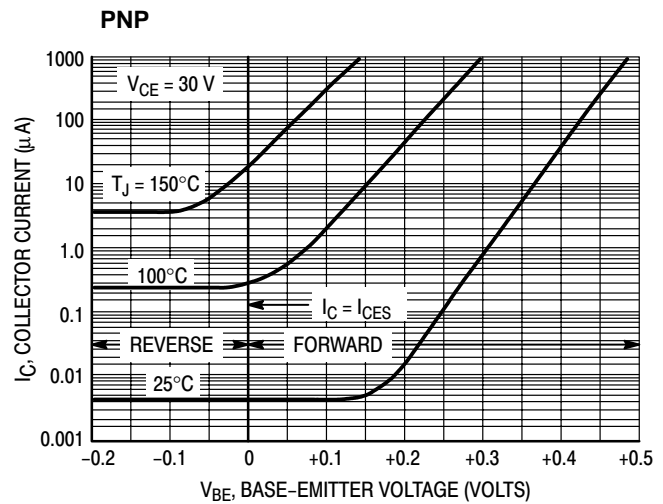


**Figure 9. Capacitances**

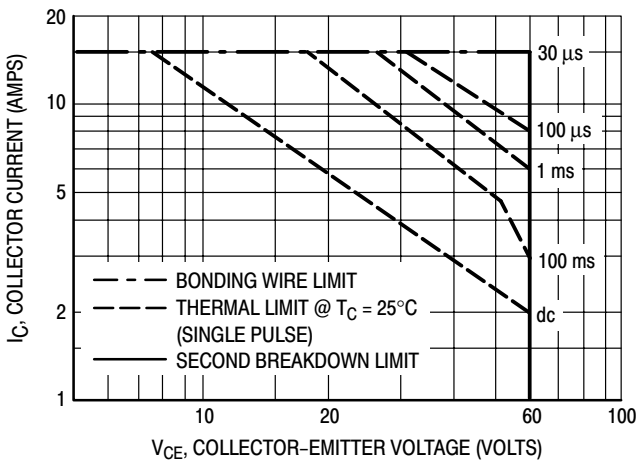
### COLLECTOR CUT-OFF REGION



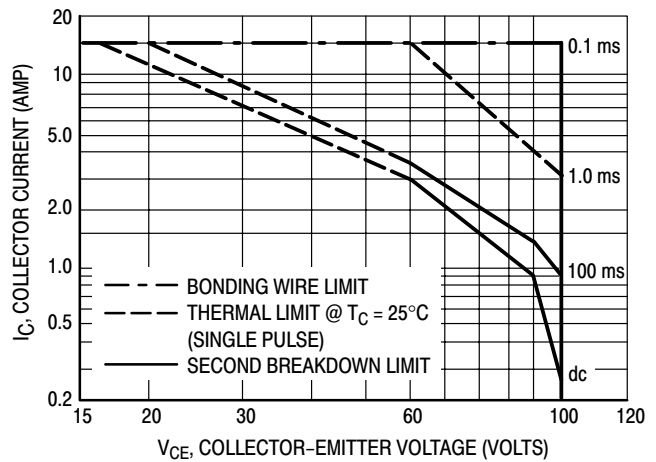
**Figure 10. 2N3055A, MJ15015**



**Figure 11. MJ15016**



**Figure 12. Forward Bias Safe Operating Area  
2N3055A**



**Figure 13. Forward Bias Safe Operating Area  
MJ15015, MJ15016**

## 2N3055A MJ15015 MJ15016

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

# Complementary Silicon Power Transistors

... designed for general-purpose switching and amplifier applications.

- DC Current Gain —  $h_{FE} = 20-70 @ I_C = 4 \text{ Adc}$
- Collector-Emitter Saturation Voltage —  $V_{CE(sat)} = 1.1 \text{ Vdc (Max) @ } I_C = 4 \text{ Adc}$
- Excellent Safe Operating Area

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	Vdc
Collector-Emitter Voltage	$V_{CER}$	70	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	7	Vdc
Collector Current — Continuous	$I_C$	15	A <sub>dc</sub>
Base Current	$I_B$	7	A <sub>dc</sub>
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	115 0.657	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	$^\circ\text{C/W}$

**NPN**  
**2N3055 \***  
**PNP**  
**MJ2955 \***

\*ON Semiconductor Preferred Device

**15 AMPERE  
POWER TRANSISTORS  
COMPLEMENTARY  
SILICON  
60 VOLTS  
115 WATTS**

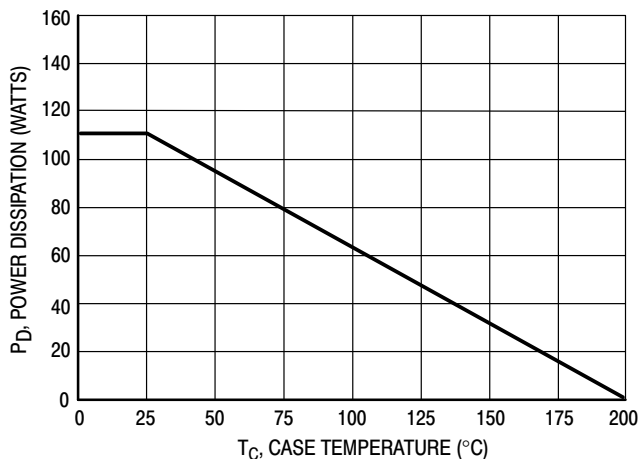
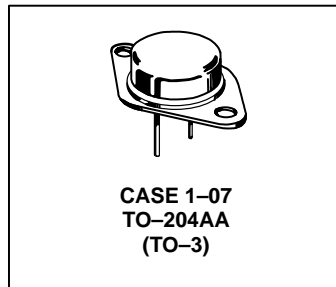


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.



## 2N3055 MJ2955

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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#### \*OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) ( $I_C = 200\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	60	—	Vdc
Collector–Emitter Sustaining Voltage (1) ( $I_C = 200\text{ mA}$ , $R_{BE} = 100\text{ Ohms}$ )	$V_{CER(sus)}$	70	—	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	0.7	mA
Collector Cutoff Current ( $V_{CE} = 100\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 100\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	—	1.0 5.0	mA
Emitter Cutoff Current ( $V_{BE} = 7.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	5.0	mA

#### \*ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 4.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 10\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	20 5.0	70 —	—
Collector–Emitter Saturation Voltage ( $I_C = 4.0\text{ A}$ , $I_B = 400\text{ mA}$ ) ( $I_C = 10\text{ A}$ , $I_B = 3.3\text{ A}$ )	$V_{CE(sat)}$	—	1.1 3.0	Vdc
Base–Emitter On Voltage ( $I_C = 4.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	1.5	Vdc

#### SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 40\text{ Vdc}$ , $t = 1.0\text{ s}$ , Nonrepetitive)	$I_{S/b}$	2.87	—	A
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#### DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ( $I_C = 0.5\text{ A}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	2.5	—	MHz
*Small–Signal Current Gain ( $I_C = 1.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	15	120	—
*Small–Signal Current Gain Cutoff Frequency ( $V_{CE} = 4.0\text{ Vdc}$ , $I_C = 1.0\text{ A}$ , $f = 1.0\text{ kHz}$ )	$f_{hfe}$	10	—	kHz

\*Indicates Within JEDEC Registration. (2N3055)

(1) Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## 2N3055 MJ2955

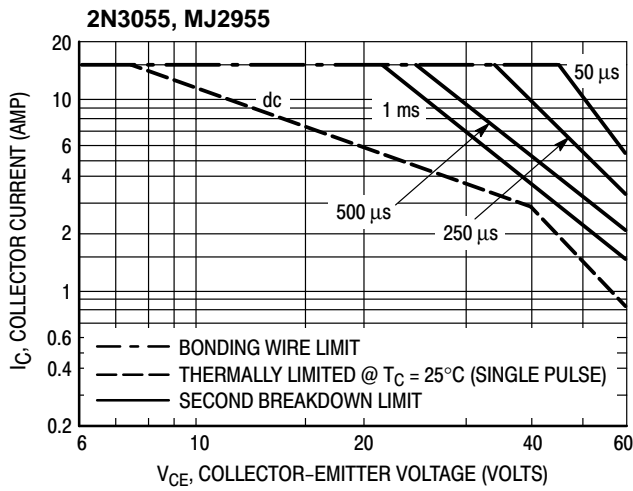


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

# 2N3055 MJ2955

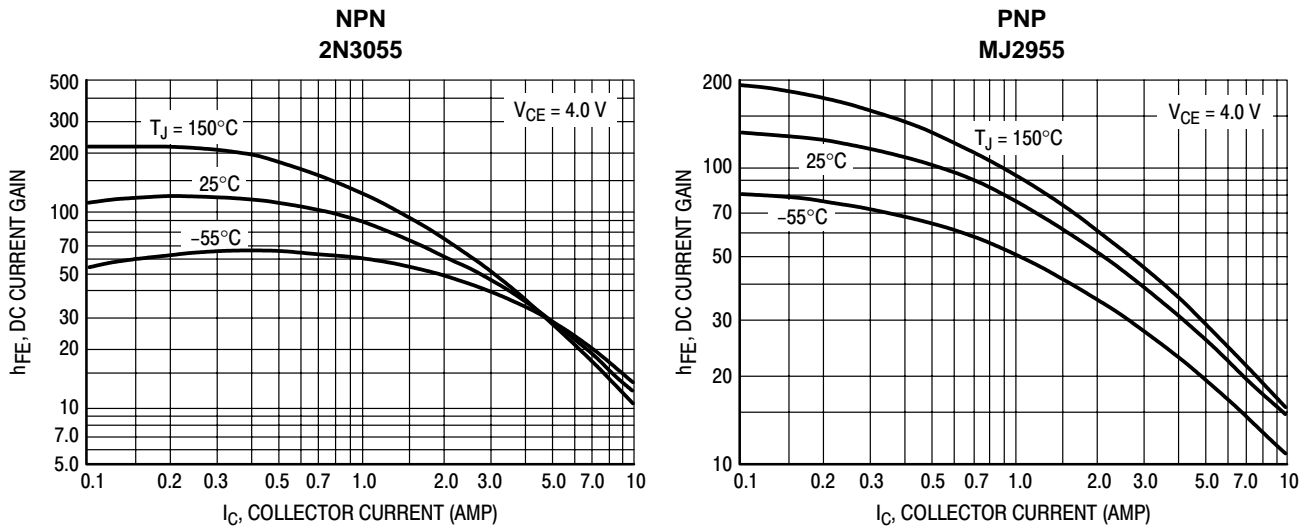


Figure 3. DC Current Gain

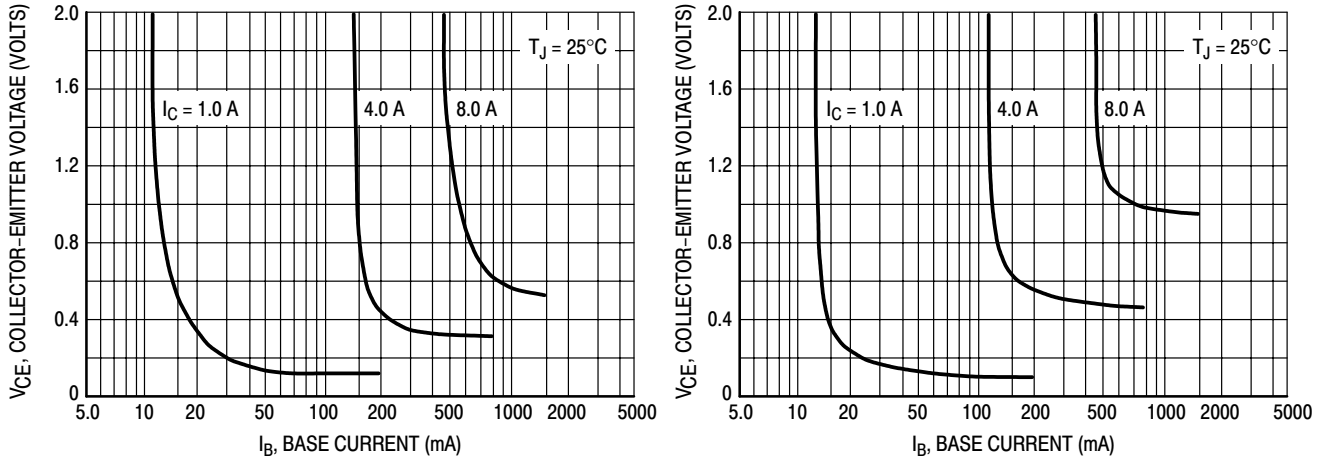


Figure 4. Collector Saturation Region

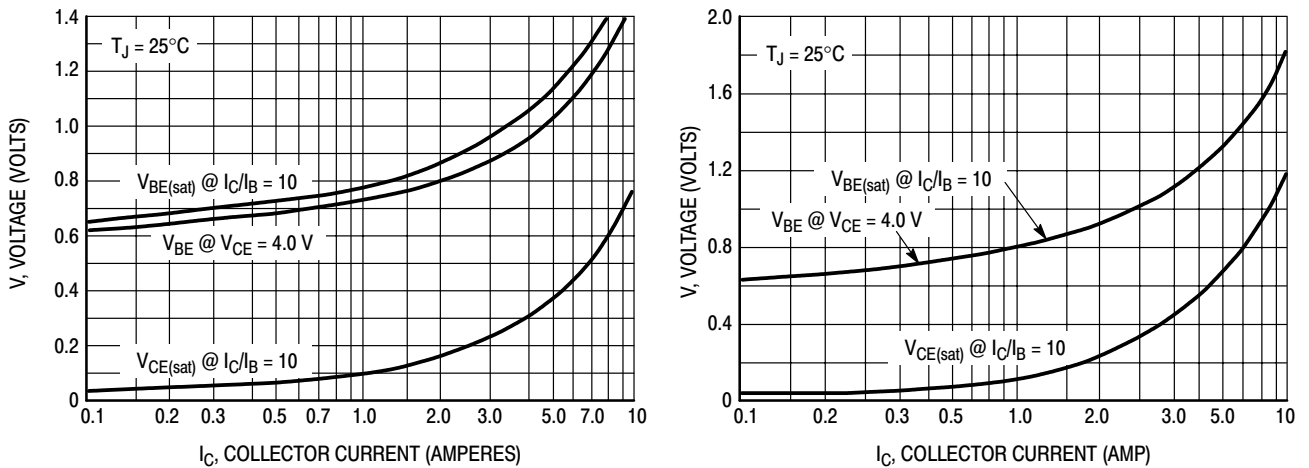


Figure 5. "On" Voltages

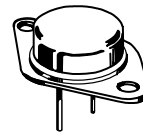
# High-Power Industrial Transistors

NPN silicon power transistor designed for applications in industrial and commercial equipment including high fidelity audio amplifiers, series and shunt regulators and power switches.

- Collector–Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 140 \text{ Vdc (Min)}$
- Excellent Second Breakdown Capability

## 2N3442

**10 AMPERE  
POWER TRANSISTOR  
NPN SILICON  
140 VOLTS  
117 WATTS**



**CASE 1-07  
TO-204AA  
(TO-3)**

### \*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	140	Vdc
Collector–Base Voltage	$V_{CB}$	160	Vdc
Emitter–Base Voltage	$V_{EB}$	7.0	Vdc
Collector Current — Continuous Peak	$I_C$	10 15**	Adc
Base Current — Continuous Peak	$I_B$	7.0 —	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	117 0.67	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +200	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	$^\circ\text{C/W}$

\* Indicates JEDEC Registered Data.

\*\* This data guaranteed in addition to JEDEC registered data.

# 2N3442

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	140	—	Vdc
Collector Cutoff Current ( $V_{CE} = 140\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	200	mAdc
Collector Cutoff Current ( $V_{CE} = 140\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 140\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	—	5.0 30	mAdc
Emitter Cutoff Current ( $V_{BE} = 7.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	5.0	mAdc

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 10\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	20 7.5	70 —	—
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ Adc}$ , $I_B = 2.0\text{ Adc}$ )	$V_{CE(sat)}$	—	5.0	Vdc
Base–Emitter On Voltage ( $I_C = 10\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	5.7	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product (2) ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f_{test} = 40\text{ kHz}$ )	$f_T$	80	—	kHz
Small–Signal Current Gain ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	12	72	—

\*Indicates JEDEC Registered Data.

### NOTES:

1. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .
2.  $f_T = |h_{fe}| \cdot f_{test}$

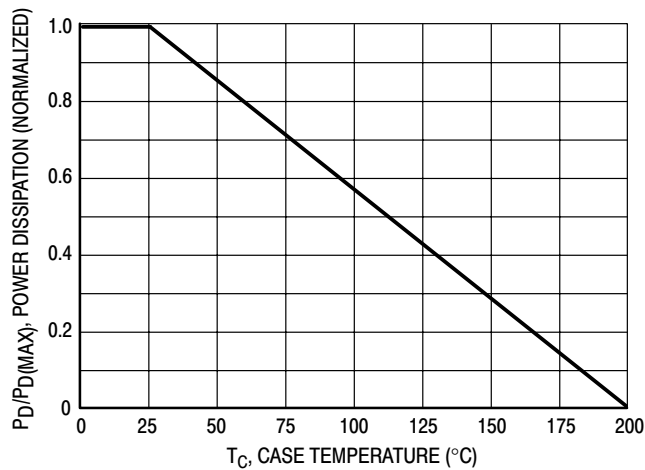


Figure 1. Power Derating

ACTIVE REGION SAFE OPERATING AREA INFORMATION

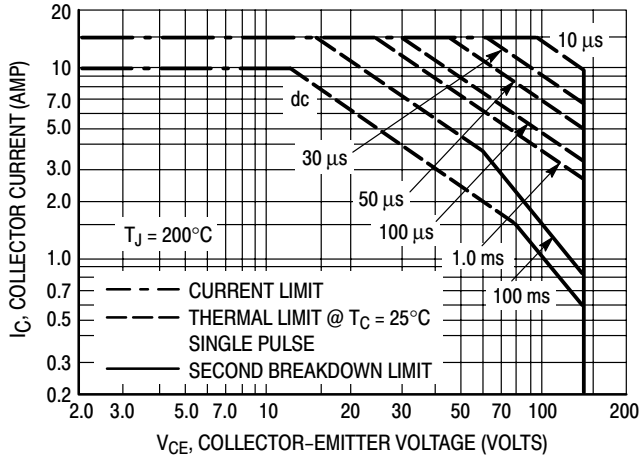


Figure 2. 2N3442

There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

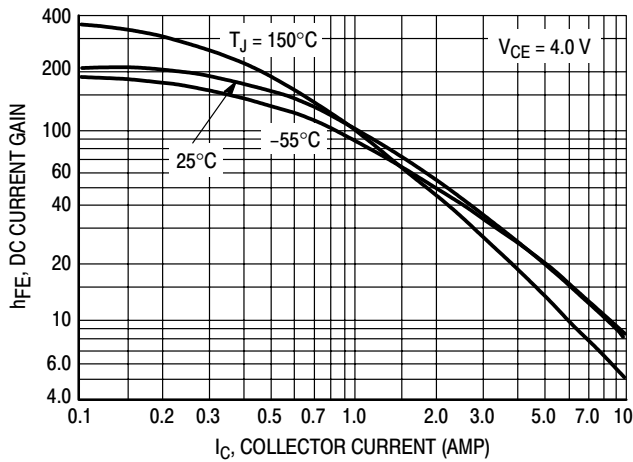


Figure 3. DC Current Gain

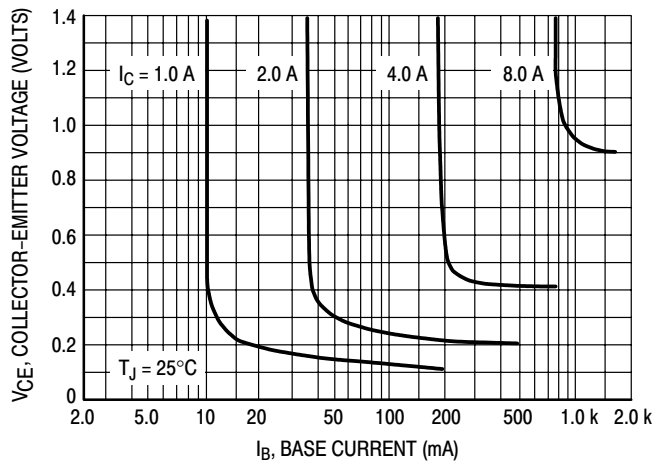


Figure 4. Collector-Saturation Region

# High Power NPN Silicon Power Transistors

...designed for linear amplifiers, series pass regulators, and inductive switching applications.

- Forward Biased Second Breakdown Current Capability  
 $I_{S/b} = 3.75 \text{ A}_{dc} @ V_{CE} = 40 \text{ V}_{dc} \text{ — } 2N3771$   
 $= 2.5 \text{ A}_{dc} @ V_{CE} = 60 \text{ V}_{dc} \text{ — } 2N3772$

**\*MAXIMUM RATINGS**

Rating	Symbol	2N3771	2N3772	Unit
Collector–Emitter Voltage	$V_{CEO}$	40	60	Vdc
Collector–Emitter Voltage	$V_{CEX}$	50	80	Vdc
Collector–Base Voltage	$V_{CB}$	50	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	7.0	Vdc
Collector Current — Continuous Peak	$I_C$	30 30	20 30	A <sub>dc</sub>
Base Current — Continuous Peak	$I_B$	7.5 15	5.0 15	A <sub>dc</sub>
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	150 0.855		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +200		$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

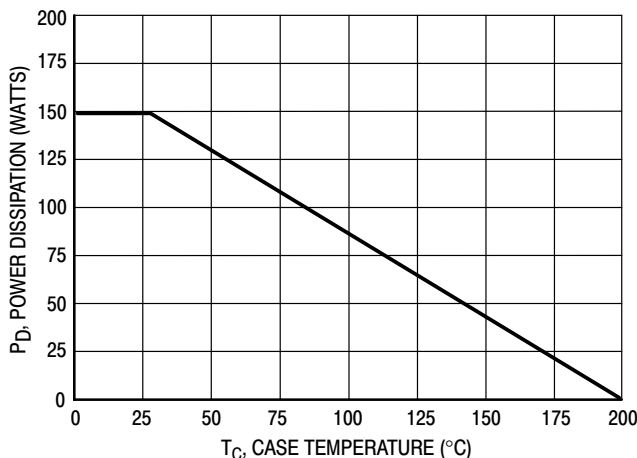
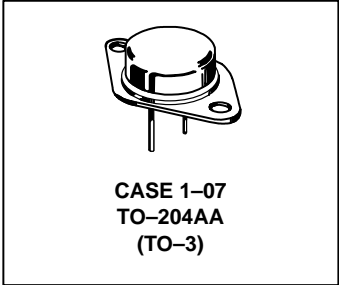
Characteristics	Symbol	2N3771, 2N3772	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	1.17	$^\circ\text{C}/\text{W}$

\*Indicates JEDEC Registered Data.

**2N3771\***  
**2N3772**

\*ON Semiconductor Preferred Device

**20 and 30 AMPERE  
POWER TRANSISTORS  
NPN SILICON  
40 and 60 VOLTS  
150 WATTS**



**Figure 1. Power Derating**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

## 2N3771 2N3772

### ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

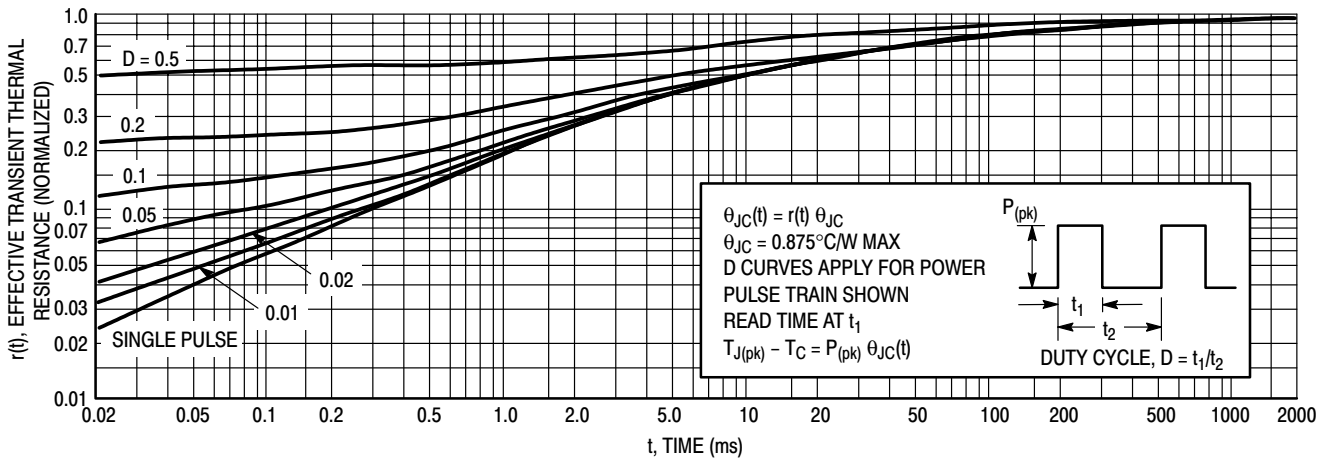
Characteristic		Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>					
*Collector–Emitter Sustaining Voltage (1) (I <sub>C</sub> = 0.2 Adc, I <sub>B</sub> = 0)	2N3771 2N3772	V <sub>CEO(sus)</sub>	40 60	— —	Vdc
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 0.2 Adc, V <sub>EB(off)</sub> = 1.5 Vdc, R <sub>BE</sub> = 100 Ohms)	2N3771 2N3772	V <sub>CEX(sus)</sub>	50 80	— —	Vdc
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 0.2 Adc, R <sub>BE</sub> = 100 Ohms)	2N3771 2N3772	V <sub>CER(sus)</sub>	45 70	— —	Vdc
*Collector Cutoff Current (V <sub>CE</sub> = 30 Vdc, I <sub>B</sub> = 0) (V <sub>CE</sub> = 50 Vdc, I <sub>B</sub> = 0) (V <sub>CE</sub> = 25 Vdc, I <sub>B</sub> = 0)	2N3771 2N3772	I <sub>CEO</sub>	— —	10 10	mAdc
*Collector Cutoff Current (V <sub>CE</sub> = 50 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = 100 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = 45 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = 30 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 150°C)  (V <sub>CE</sub> = 45 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 150°C)	2N3771 2N3772 2N6257 2N3771 2N3772	I <sub>CEV</sub>	— — — — —	2.0 5.0 4.0 10 10	mAdc
*Collector Cutoff Current (V <sub>CB</sub> = 50 Vdc, I <sub>E</sub> = 0) (V <sub>CB</sub> = 100 Vdc, I <sub>E</sub> = 0)	2N3771 2N3772	I <sub>CBO</sub>	— —	2.0 5.0	mAdc
*Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0) (V <sub>BE</sub> = 7.0 Vdc, I <sub>C</sub> = 0)	2N3771 2N3772	I <sub>EBO</sub>	— —	5.0 5.0	mAdc
<b>*ON CHARACTERISTICS</b>					
DC Current Gain (1) (I <sub>C</sub> = 15 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 8.0 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 30 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 20 Adc, V <sub>CE</sub> = 4.0 Vdc)	2N3771 2N3772 2N3771 2N3772	h <sub>FE</sub>	15 15 5.0 5.0	60 60 — —	—
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 15 Adc, I <sub>B</sub> = 1.5 Adc) (I <sub>C</sub> = 10 Adc, I <sub>B</sub> = 1.0 Adc) (I <sub>C</sub> = 30 Adc, I <sub>B</sub> = 6.0 Adc) (I <sub>C</sub> = 20 Adc, I <sub>B</sub> = 4.0 Adc)	2N3771 2N3772 2N3771 2N3772	V <sub>CE(sat)</sub>	— — — —	2.0 1.4 4.0 4.0	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 15 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 8.0 Adc, V <sub>CE</sub> = 4.0 Vdc)	2N3771 2N3772	V <sub>BE(on)</sub>	— —	2.7 2.2	Vdc
<b>*DYNAMIC CHARACTERISTICS</b>					
Current–Gain — Bandwidth Product (I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 4.0 Vdc, f <sub>test</sub> = 50 kHz)		f <sub>T</sub>	0.2	—	MHz
Small–Signal Current Gain (I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 4.0 Vdc, f = 1.0 kHz)		h <sub>fe</sub>	40	—	—
<b>SECOND BREAKDOWN</b>					
Second Breakdown Energy with Base Forward Biased, t = 1.0 s (non–repetitive) (V <sub>CE</sub> = 40 Vdc) (V <sub>CE</sub> = 60 Vdc)	2N3771 2N3772	I <sub>S/b</sub>	3.75 2.5	— —	Adc

\*Indicates JEDEC Registered Data.

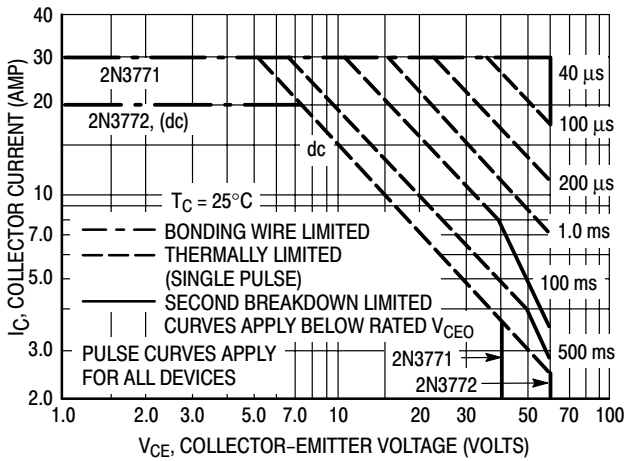
(1) Pulse Test: 300 μs, Rep. Rate 60 cps.



## 2N3771 2N3772



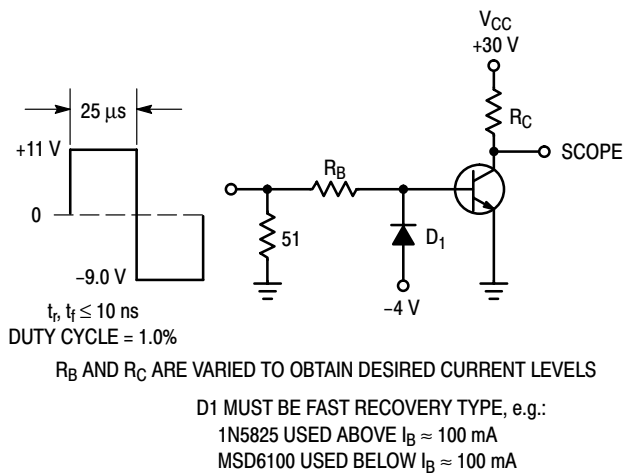
**Figure 2. Thermal Response — 2N3771, 2N3772**



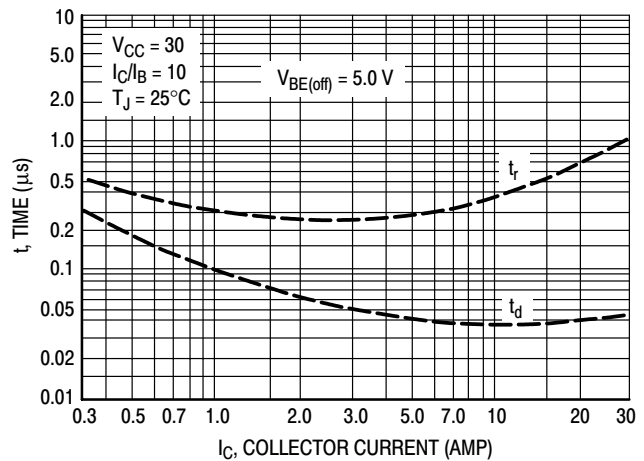
**Figure 3. Active-Region Safe Operating Area — 2N3771, 2N3772**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based on JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 200^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3,  $T_{J(pk)}$  will be found to be less than  $T_{J(max)}$  for pulse widths of 1 ms and less. When using ON Semiconductor transistors, it is permissible to increase the pulse power limits until limited by  $T_{J(max)}$ .



**Figure 4. Switching Time Test Circuit**



**Figure 5. Turn-On Time**

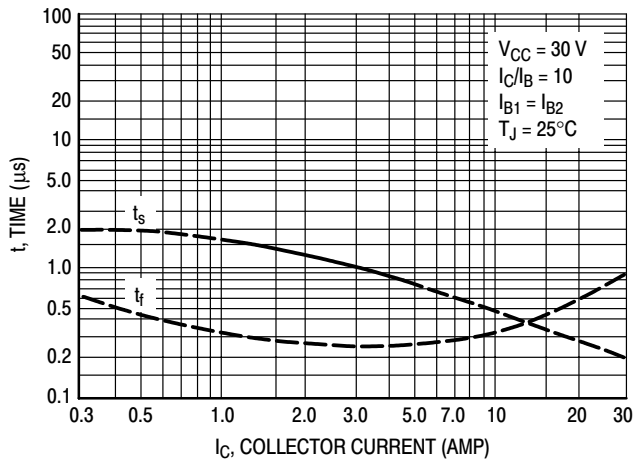


Figure 6. Turn-Off Time

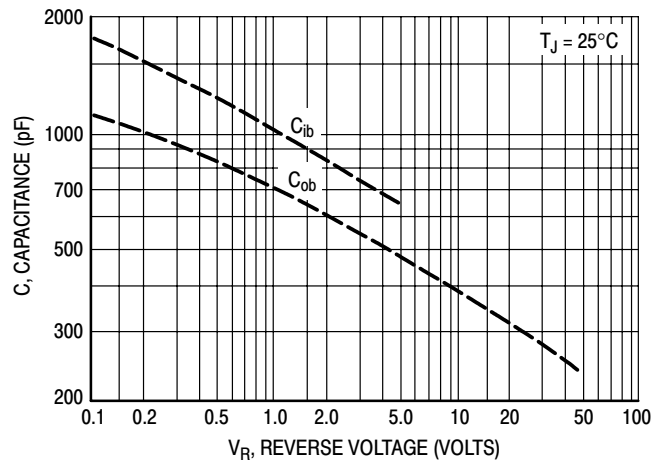


Figure 7. Capacitance

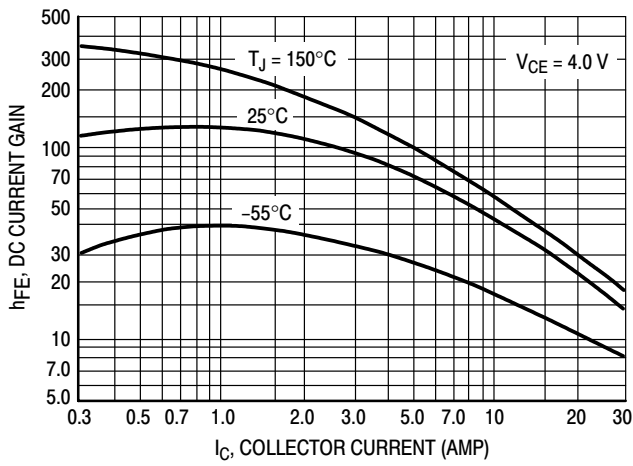


Figure 8. DC Current Gain

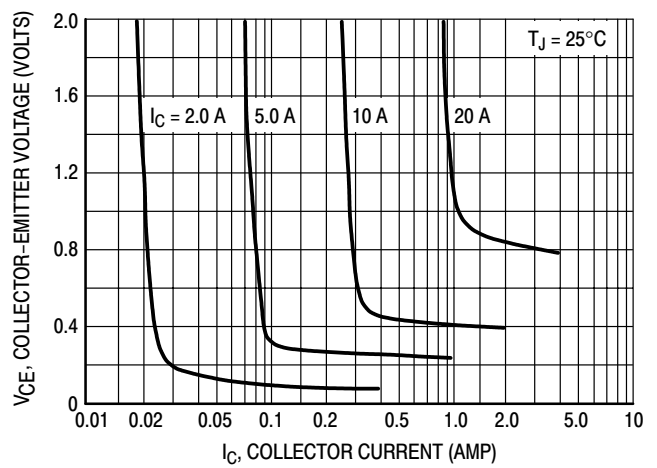


Figure 9. Collector Saturation Region

# High Power NPN Silicon Power Transistors

...designed for linear amplifiers, series pass regulators, and inductive switching applications.

- Forward Biased Second Breakdown Current Capability  
 $I_{S/b} = 3.75 \text{ A}_{dc} @ V_{CE} = 40 \text{ V}_{dc} \text{ — } 2N3771$   
 $= 2.5 \text{ A}_{dc} @ V_{CE} = 60 \text{ V}_{dc} \text{ — } 2N3772$

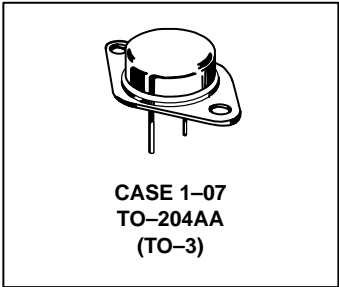
**\*MAXIMUM RATINGS**

Rating	Symbol	2N3771	2N3772	Unit
Collector–Emitter Voltage	$V_{CEO}$	40	60	Vdc
Collector–Emitter Voltage	$V_{CEX}$	50	80	Vdc
Collector–Base Voltage	$V_{CB}$	50	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	7.0	Vdc
Collector Current — Continuous Peak	$I_C$	30 30	20 30	A <sub>dc</sub>
Base Current — Continuous Peak	$I_B$	7.5 15	5.0 15	A <sub>dc</sub>
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	150 0.855		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +200		$^\circ\text{C}$

**2N3771\***  
**2N3772**

\*ON Semiconductor Preferred Device

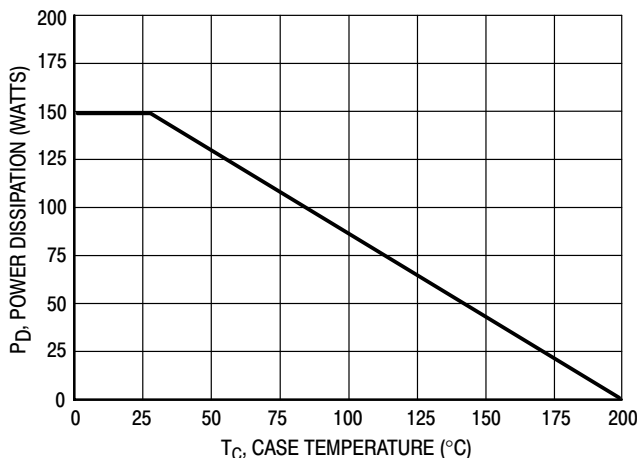
**20 and 30 AMPERE  
POWER TRANSISTORS  
NPN SILICON  
40 and 60 VOLTS  
150 WATTS**



**THERMAL CHARACTERISTICS**

Characteristics	Symbol	2N3771, 2N3772	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	1.17	$^\circ\text{C}/\text{W}$

\*Indicates JEDEC Registered Data.



**Figure 1. Power Derating**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

## 2N3771 2N3772

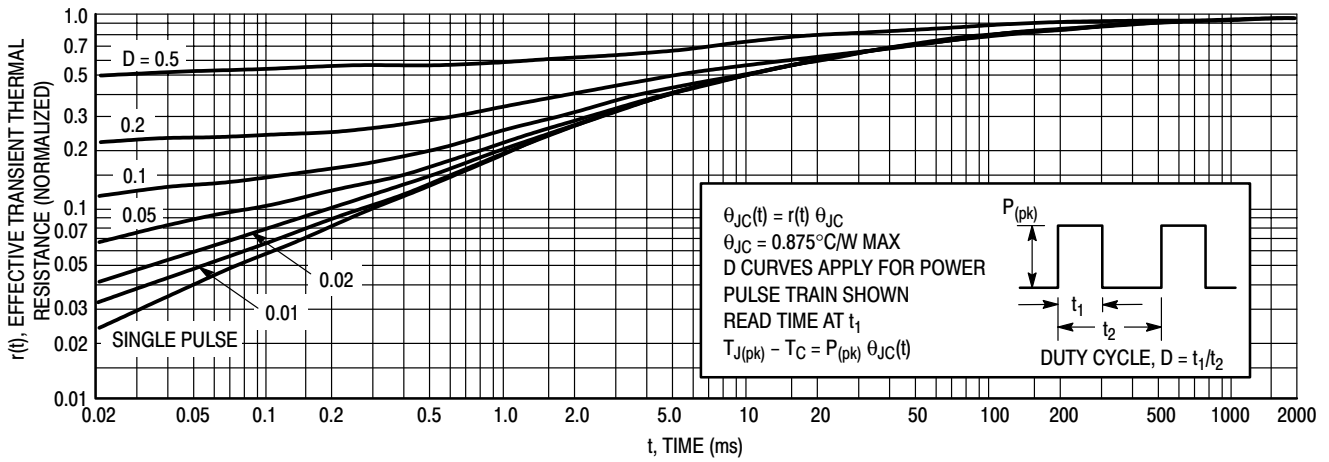
### ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>					
*Collector–Emitter Sustaining Voltage (1) (I <sub>C</sub> = 0.2 Adc, I <sub>B</sub> = 0)	2N3771 2N3772	V <sub>CEO(sus)</sub>	40 60	— —	Vdc
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 0.2 Adc, V <sub>EB(off)</sub> = 1.5 Vdc, R <sub>BE</sub> = 100 Ohms)	2N3771 2N3772	V <sub>CEX(sus)</sub>	50 80	— —	Vdc
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 0.2 Adc, R <sub>BE</sub> = 100 Ohms)	2N3771 2N3772	V <sub>CER(sus)</sub>	45 70	— —	Vdc
*Collector Cutoff Current (V <sub>CE</sub> = 30 Vdc, I <sub>B</sub> = 0) (V <sub>CE</sub> = 50 Vdc, I <sub>B</sub> = 0) (V <sub>CE</sub> = 25 Vdc, I <sub>B</sub> = 0)	2N3771 2N3772	I <sub>CEO</sub>	— —	10 10	mAdc
*Collector Cutoff Current (V <sub>CE</sub> = 50 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = 100 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = 45 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = 30 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 150°C)  (V <sub>CE</sub> = 45 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 150°C)	2N3771 2N3772 2N6257 2N3771 2N3772	I <sub>CEV</sub>	— — — — —	2.0 5.0 4.0 10 10	mAdc
*Collector Cutoff Current (V <sub>CB</sub> = 50 Vdc, I <sub>E</sub> = 0) (V <sub>CB</sub> = 100 Vdc, I <sub>E</sub> = 0)	2N3771 2N3772	I <sub>CBO</sub>	— —	2.0 5.0	mAdc
*Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0) (V <sub>BE</sub> = 7.0 Vdc, I <sub>C</sub> = 0)	2N3771 2N3772	I <sub>EBO</sub>	— —	5.0 5.0	mAdc
<b>*ON CHARACTERISTICS</b>					
DC Current Gain (1) (I <sub>C</sub> = 15 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 8.0 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 30 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 20 Adc, V <sub>CE</sub> = 4.0 Vdc)	2N3771 2N3772  2N3771 2N3772	h <sub>FE</sub>	15 15  5.0 5.0	60 60  — —	—
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 15 Adc, I <sub>B</sub> = 1.5 Adc) (I <sub>C</sub> = 10 Adc, I <sub>B</sub> = 1.0 Adc) (I <sub>C</sub> = 30 Adc, I <sub>B</sub> = 6.0 Adc) (I <sub>C</sub> = 20 Adc, I <sub>B</sub> = 4.0 Adc)	2N3771 2N3772 2N3771 2N3772	V <sub>CE(sat)</sub>	— — — —	2.0 1.4 4.0 4.0	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 15 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 8.0 Adc, V <sub>CE</sub> = 4.0 Vdc)	2N3771 2N3772	V <sub>BE(on)</sub>	— —	2.7 2.2	Vdc
<b>*DYNAMIC CHARACTERISTICS</b>					
Current–Gain — Bandwidth Product (I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 4.0 Vdc, f <sub>test</sub> = 50 kHz)		f <sub>T</sub>	0.2	—	MHz
Small–Signal Current Gain (I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 4.0 Vdc, f = 1.0 kHz)		h <sub>fe</sub>	40	—	—
<b>SECOND BREAKDOWN</b>					
Second Breakdown Energy with Base Forward Biased, t = 1.0 s (non–repetitive) (V <sub>CE</sub> = 40 Vdc) (V <sub>CE</sub> = 60 Vdc)	2N3771 2N3772	I <sub>S/b</sub>	3.75 2.5	— —	Adc

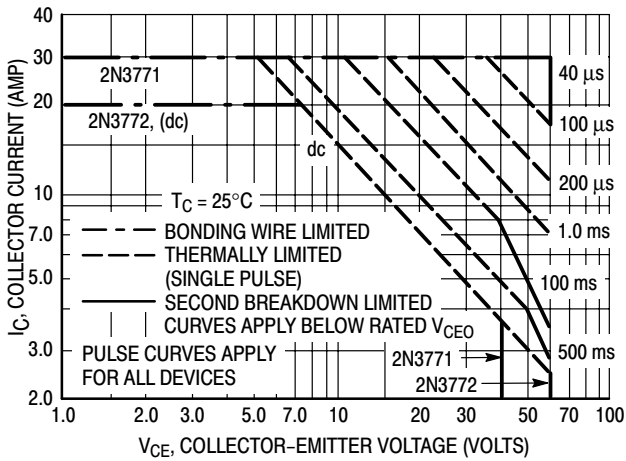
\*Indicates JEDEC Registered Data.

(1) Pulse Test: 300 μs, Rep. Rate 60 cps.

## 2N3771 2N3772



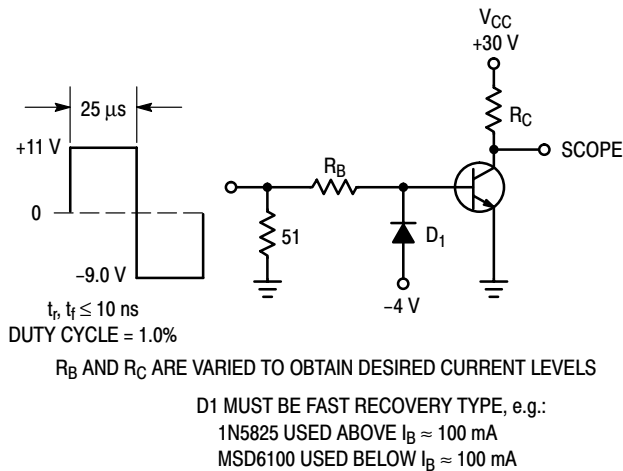
**Figure 2. Thermal Response — 2N3771, 2N3772**



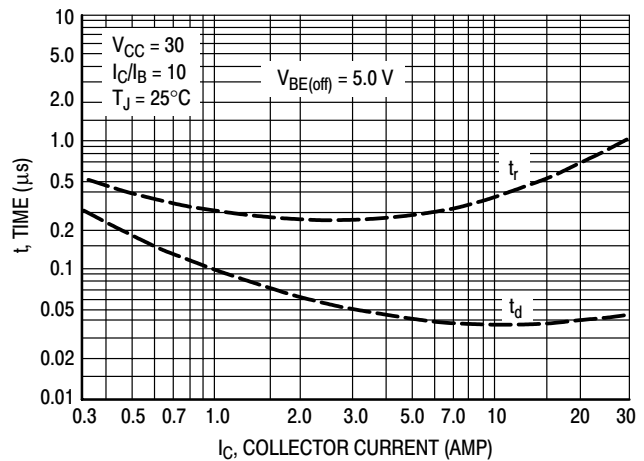
**Figure 3. Active-Region Safe Operating Area — 2N3771, 2N3772**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based on JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 200^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3,  $T_{J(pk)}$  will be found to be less than  $T_{J(max)}$  for pulse widths of 1 ms and less. When using ON Semiconductor transistors, it is permissible to increase the pulse power limits until limited by  $T_{J(max)}$ .



**Figure 4. Switching Time Test Circuit**



**Figure 5. Turn-On Time**

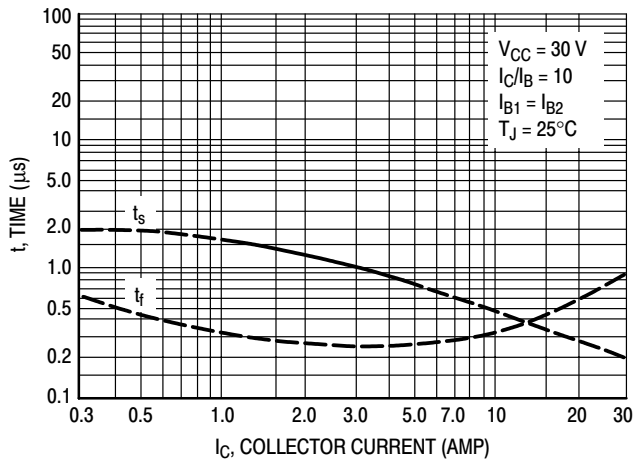


Figure 6. Turn-Off Time

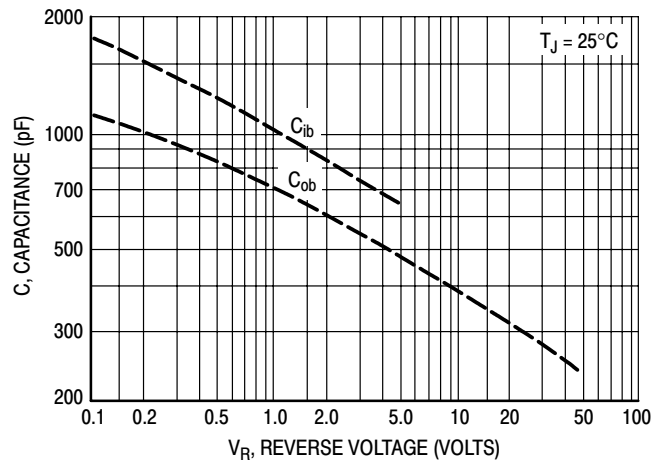


Figure 7. Capacitance

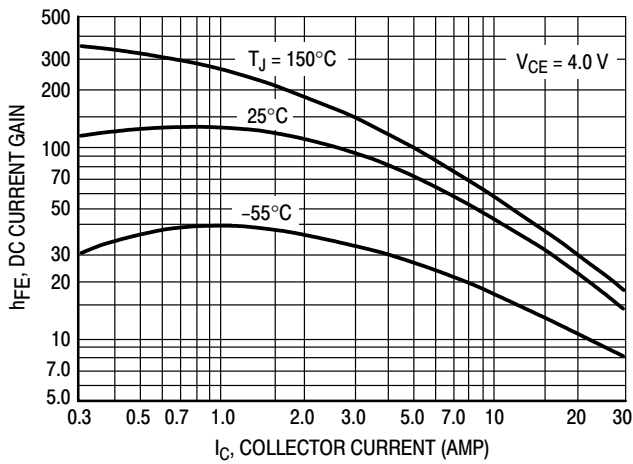


Figure 8. DC Current Gain

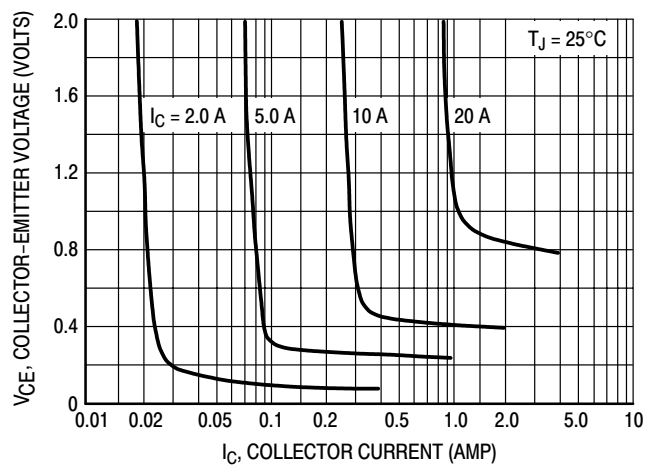


Figure 9. Collector Saturation Region

# Complementary Silicon Power Transistors

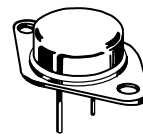
The 2N3773 and 2N6609 are PowerBase™ power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc to dc converters or inverters.

- High Safe Operating Area (100% Tested) 150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  - $h_{FE} = 15$  (Min) @ 8 A, 4 V
  - $V_{CE(sat)} = 1.4$  V (Max) @  $I_C = 8$  A,  $I_B = 0.8$  A
- For Low Distortion Complementary Designs

**NPN**  
**2N3773\***  
**PNP**  
**2N6609**

\*ON Semiconductor Preferred Device

**16 AMPERE**  
**COMPLEMENTARY**  
**POWER TRANSISTORS**  
**140 VOLTS**  
**150 WATTS**



**CASE 1-07**  
**TO-204AA**  
**(TO-3)**

## \*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Emitter Voltage	$V_{CEO}$	140	Vdc
Collector-Emitter Voltage	$V_{CEX}$	160	Vdc
Collector-Base Voltage	$V_{CBO}$	160	Vdc
Emitter-Base Voltage	$V_{EBO}$	7	Vdc
Collector Current — Continuous — Peak (1)	$I_C$	16 30	Adc
Base Current — Continuous — Peak (1)	$I_B$	4 15	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	150 0.855	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	$^\circ\text{C/W}$

\*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq$  10%.

**Preferred** devices are ON Semiconductor recommended choices for future use and best overall value.

## 2N3773 2N6609

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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#### OFF CHARACTERISTICS (2)

*Collector–Emitter Breakdown Voltage ( $I_C = 0.2\text{ Adc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	140	—	Vdc
*Collector–Emitter Sustaining Voltage ( $I_C = 0.1\text{ Adc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $R_{BE} = 100\text{ Ohms}$ )	$V_{CEX(sus)}$	160	—	Vdc
Collector–Emitter Sustaining Voltage ( $I_C = 0.2\text{ Adc}$ , $R_{BE} = 100\text{ Ohms}$ )	$V_{CER(sus)}$	150	—	Vdc
*Collector Cutoff Current ( $V_{CE} = 120\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	10	mAdc
*Collector Cutoff Current ( $V_{CE} = 140\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 140\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	— —	2 10	mAdc
Collector Cutoff Current ( $V_{CB} = 140\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	2	mAdc
*Emitter Cutoff Current ( $V_{BE} = 7\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	5	mAdc

#### ON CHARACTERISTICS (2)

DC Current Gain *( $I_C = 8\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 16\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$h_{FE}$	15 5	60 —	—
Collector–Emitter Saturation Voltage *( $I_C = 8\text{ Adc}$ , $I_B = 800\text{ mAdc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 3.2\text{ Adc}$ )	$V_{CE(sat)}$	— —	1.4 4	Vdc
*Base–Emitter On Voltage ( $I_C = 8\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$V_{BE(on)}$	—	2.2	Vdc

#### DYNAMIC CHARACTERISTICS

Magnitude of Common–Emitter Small–Signal, Short–Circuit, Forward Current Transfer Ratio ( $I_C = 1\text{ A}$ , $f = 50\text{ kHz}$ )	$ h_{fe} $	4	—	—
*Small–Signal Current Gain ( $I_C = 1\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ , $f = 1\text{ kHz}$ )	$h_{fe}$	40	—	—

#### SECOND BREAKDOWN CHARACTERISTICS

Second Breakdown Collector Current with Base Forward Biased $t = 1\text{ s}$ (non–repetitive), $V_{CE} = 100\text{ V}$ , See Figure 12	$I_{S/b}$	1.5	—	Adc
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(2) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

\*Indicates JEDEC Registered Data.



NPN

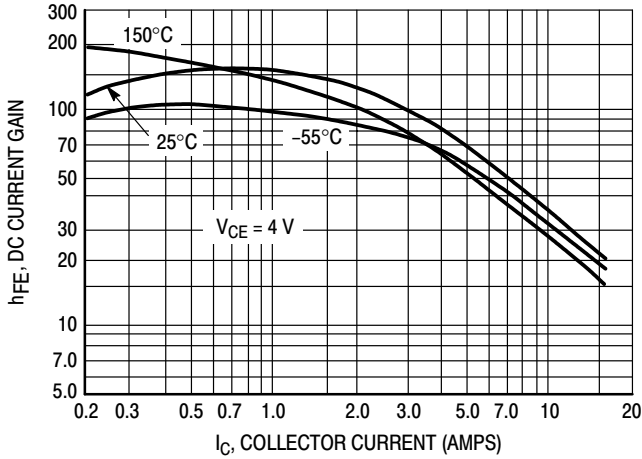


Figure 10. DC Current Gain

PNP

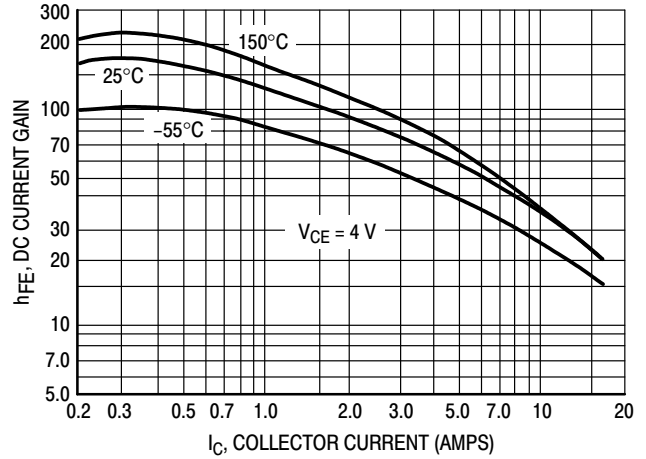


Figure 11. DC Current Gain

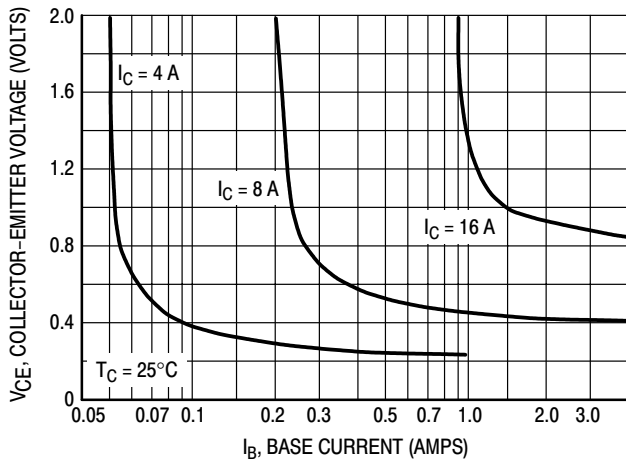


Figure 12. Collector Saturation Region

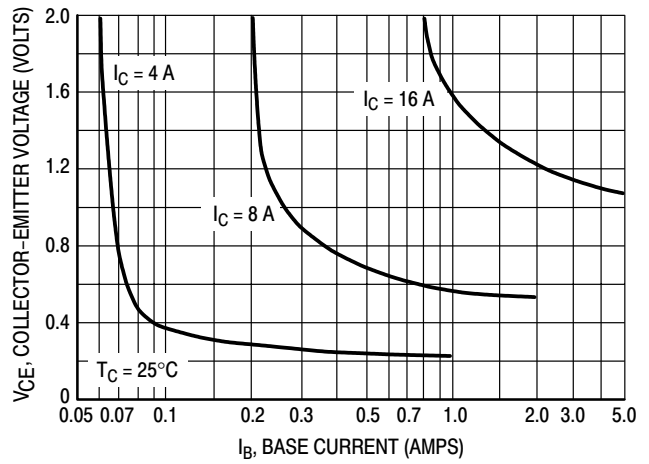


Figure 13. Collector Saturation Region

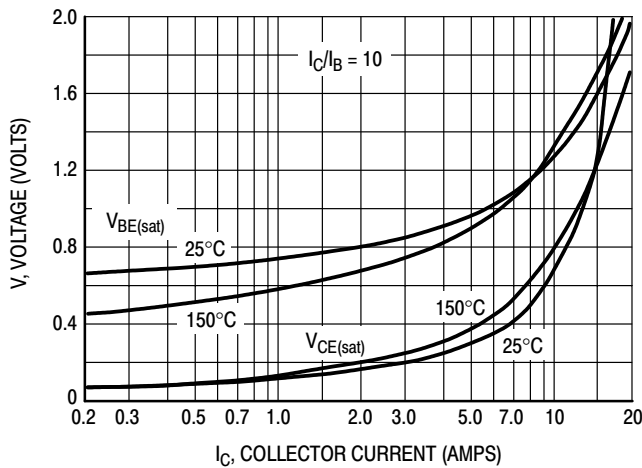


Figure 14. "On" Voltage

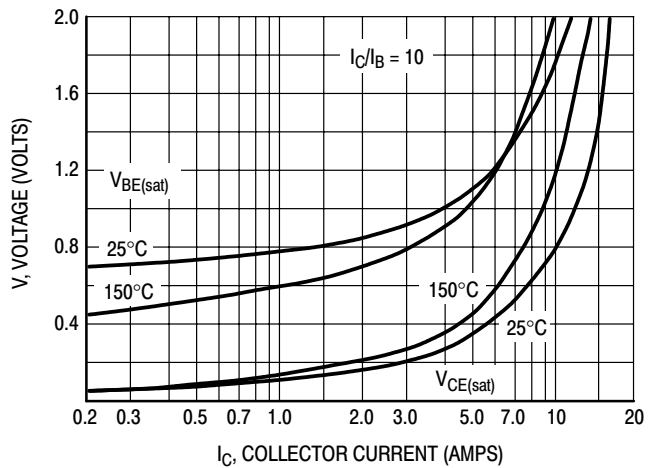
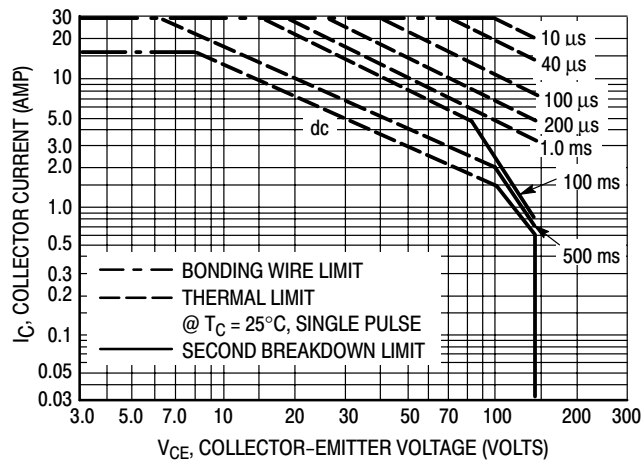


Figure 15. "On" Voltage

## 2N3773 2N6609

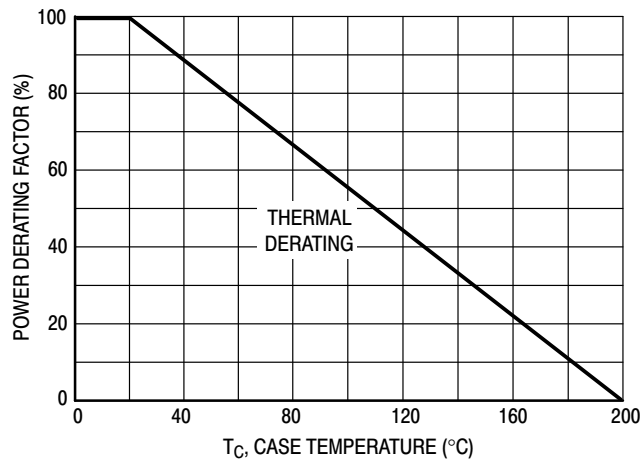


**Figure 16. Forward Bias Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse

limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 200^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 17. Power Derating**

## Medium-Power Plastic PNP Silicon Transistors

... designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage —  
 $V_{CE(sat)} = 0.6 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Amp}$
- Excellent Power Dissipation Due to Thermopad Construction —  
 $P_D = 30 \text{ W @ } T_C = 25^\circ\text{C}$
- Excellent Safe Operating Area
- Gain Specified to  $I_C = 1.0 \text{ Amp}$
- Complement to NPN 2N4921, 2N4922, 2N4923

### \*MAXIMUM RATINGS

Ratings	Symbol	2N4918	2N4919	2N4920	Unit
Collector–Emitter Voltage	$V_{CEO}$	40	60	80	Vdc
Collector–Base Voltage	$V_{CB}$	40	60	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous (1)	$I_C^*$	1.0 3.0			Adc
Base Current	$I_B$	1.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	30 0.24			Watts W/ $^\circ\text{C}$
Operating & Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150			$^\circ\text{C}$

### THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	4.16	$^\circ\text{C/W}$

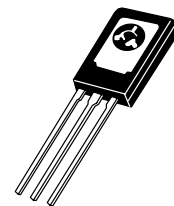
\*Indicates JEDEC Registered Data for 2N4918 Series.

- (1) The 1.0 Amp maximum  $I_C$  value is based upon JEDEC current gain requirements.  
The 3.0 Amp maximum value is based upon actual current-handling capability of the device (See Figure 5).
- (2) Recommend use of thermal compound for lowest thermal resistance.

## 2N4918 thru 2N4920\*

\*ON Semiconductor Preferred Device

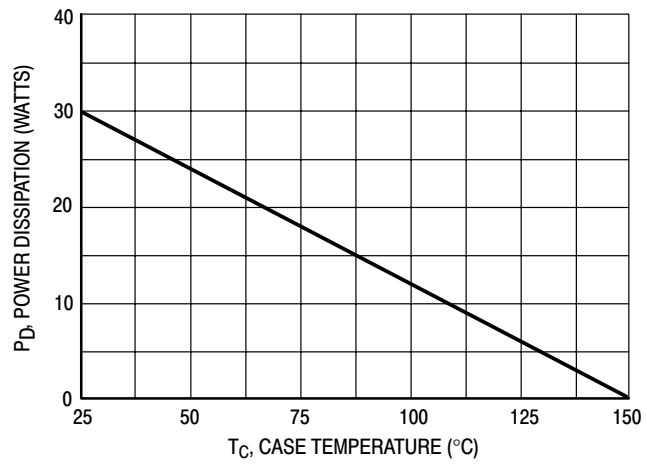
**3 AMPERE  
GENERAL-PURPOSE  
POWER TRANSISTORS  
40–80 VOLTS  
30 WATTS**



**CASE 77–09  
TO–225AA TYPE**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

## 2N4918 thru 2N4920



**Figure 1. Power Derating**

## 2N4918 thru 2N4920

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (1) ( $I_C = 0.1 \text{ Adc}$ , $I_B = 0$ )	2N4918 2N4919 2N4920	$V_{CEO(sus)}$	40 60 80	— — —	Vdc
Collector Cutoff Current ( $V_{CE} = 20 \text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 30 \text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40 \text{ Vdc}$ , $I_B = 0$ )	2N4918 2N4919 2N4920	$I_{CEO}$	— — —	0.5 0.5 0.5	mAdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{BE(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{BE(off)} = 1.5 \text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )		$I_{CEX}$	— —	0.1 0.5	mAdc
Collector Cutoff Current ( $V_{CB} = \text{Rated } V_{CB}$ , $I_E = 0$ )		$I_{CBO}$	—	0.1	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	1.0	mAdc

### ON CHARACTERISTICS

DC Current Gain (1) ( $I_C = 50 \text{ mAdc}$ , $V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 500 \text{ mAdc}$ , $V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 1.0 \text{ Adc}$ , $V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$	40 30 10	— 150 —	—
Collector–Emitter Saturation Voltage (1) ( $I_C = 1.0 \text{ Adc}$ , $I_B = 0.1 \text{ Adc}$ )	$V_{CE(sat)}$	—	0.6	Vdc
Base–Emitter Saturation Voltage (1) ( $I_C = 1.0 \text{ Adc}$ , $I_B = 0.1 \text{ Adc}$ )	$V_{BE(sat)}$	—	1.3	Vdc
Base–Emitter On Voltage (1) ( $I_C = 1.0 \text{ Adc}$ , $V_{CE} = 1.0 \text{ Vdc}$ )	$V_{BE(on)}$	—	1.3	Vdc

### SMALL–SIGNAL CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 250 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	$f_T$	3.0	—	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 100 \text{ kHz}$ )	$C_{ob}$	—	100	pF
Small–Signal Current Gain ( $I_C = 250 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ )	$h_{fe}$	25	—	—

\*Indicates JEDEC Registered Data.

(1) Pulse Test:  $PW \approx 300 \mu\text{s}$ , Duty Cycle  $\approx 2.0\%$

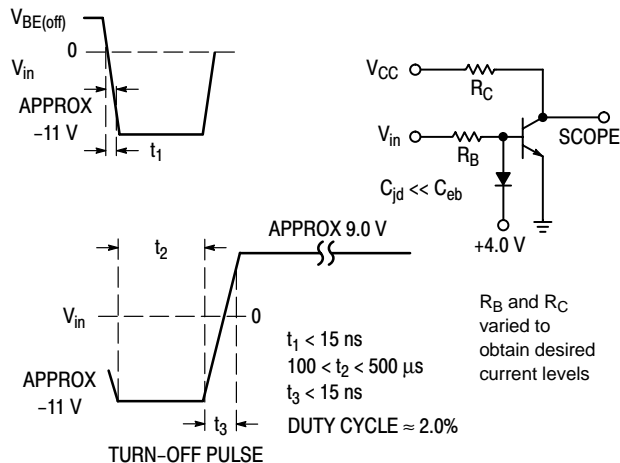


Figure 2. Switching Time Equivalent Test Circuit

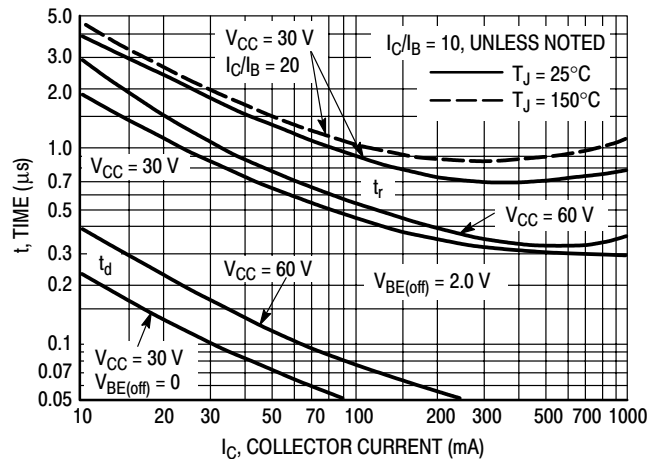
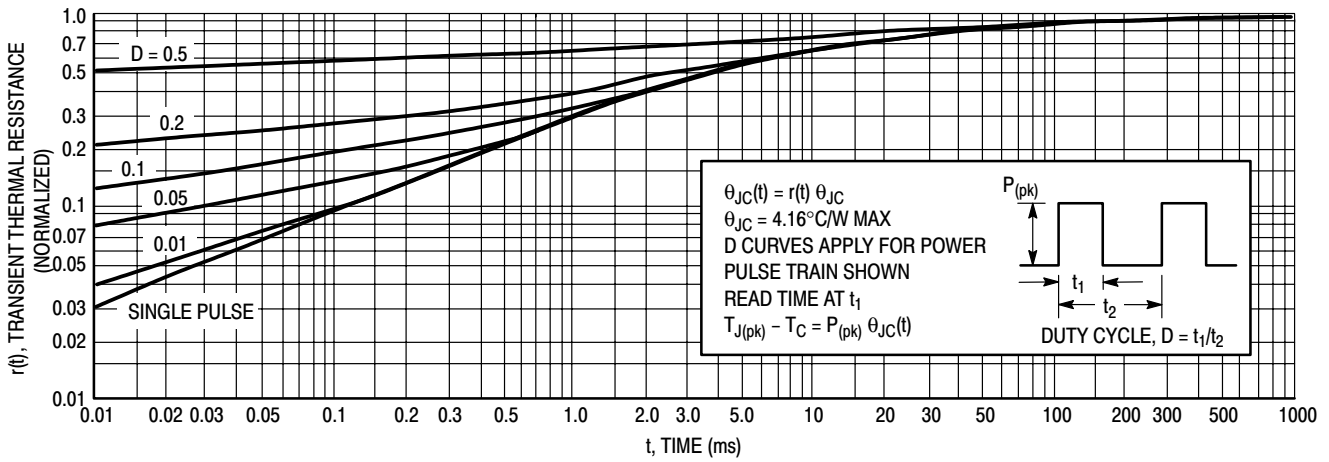
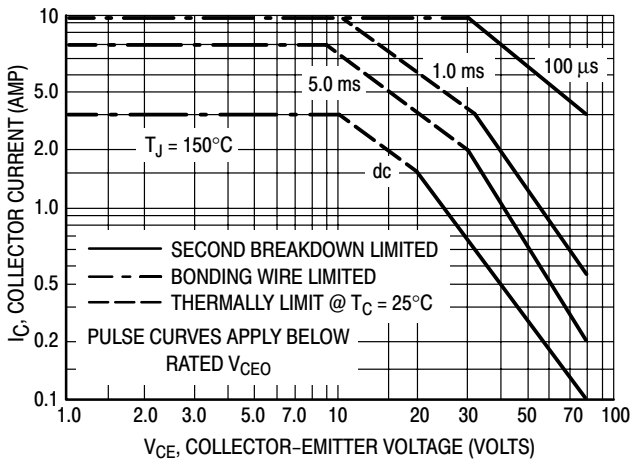


Figure 3. Turn–On Time

## 2N4918 thru 2N4920



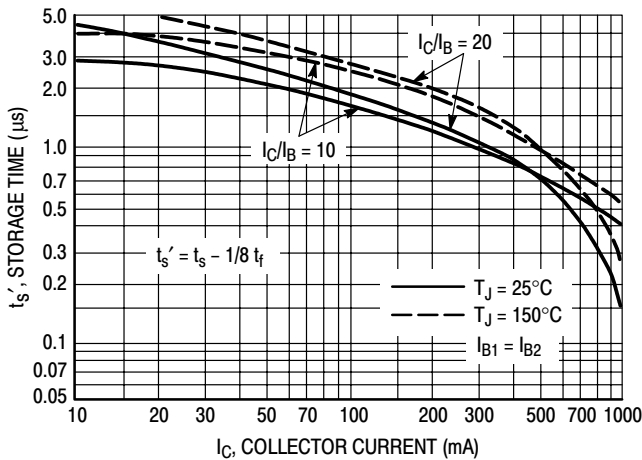
**Figure 4. Thermal Response**



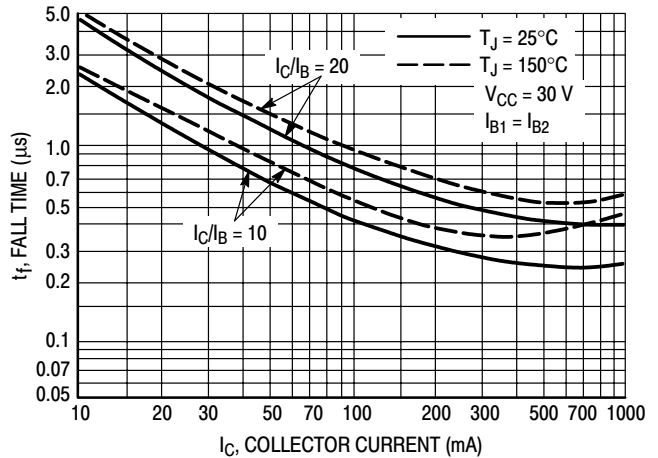
**Figure 5. Active-Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 6. Storage Time**



**Figure 7. Fall Time**

TYPICAL DC CHARACTERISTICS

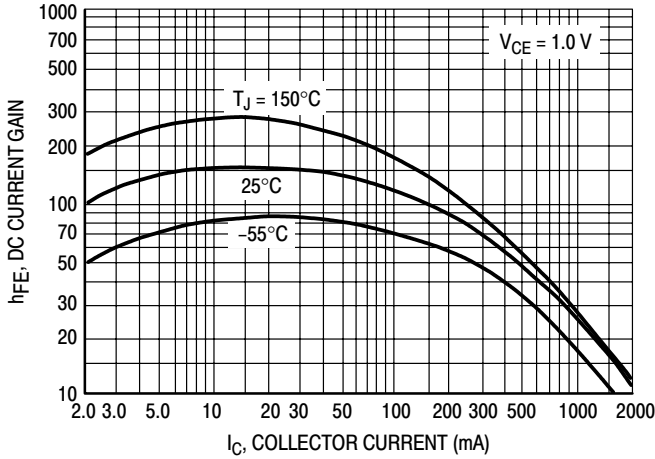


Figure 8. Current Gain

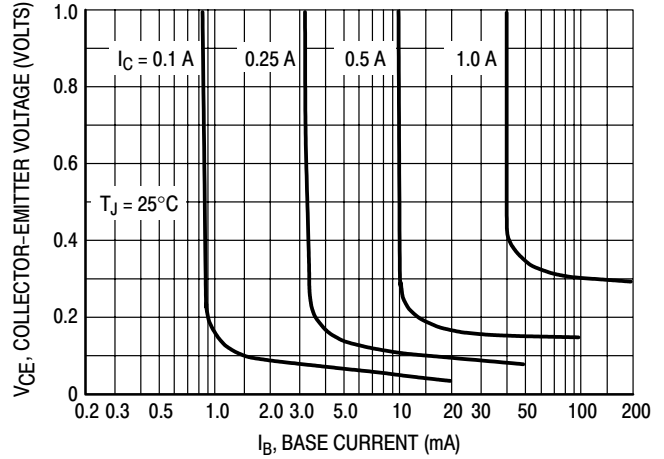


Figure 9. Collector Saturation Region

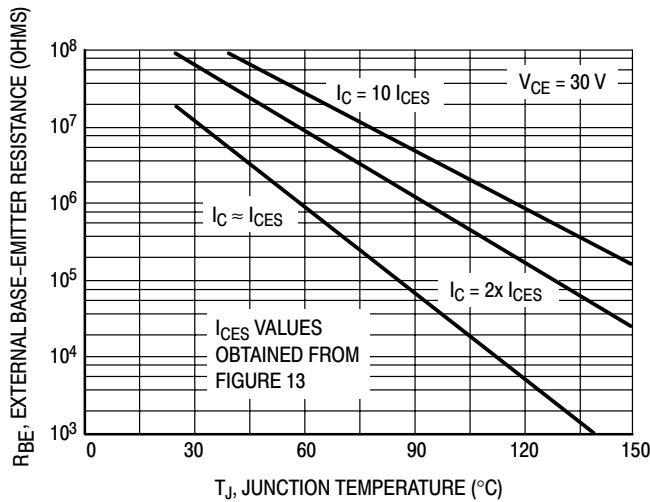


Figure 10. Effects of Base-Emitter Resistance

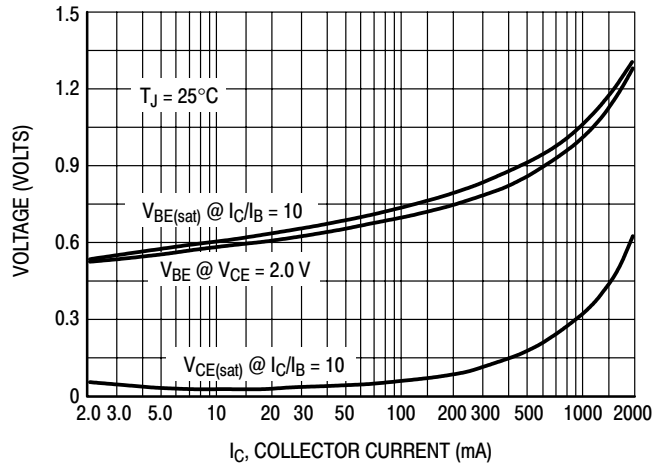


Figure 11. "On" Voltage

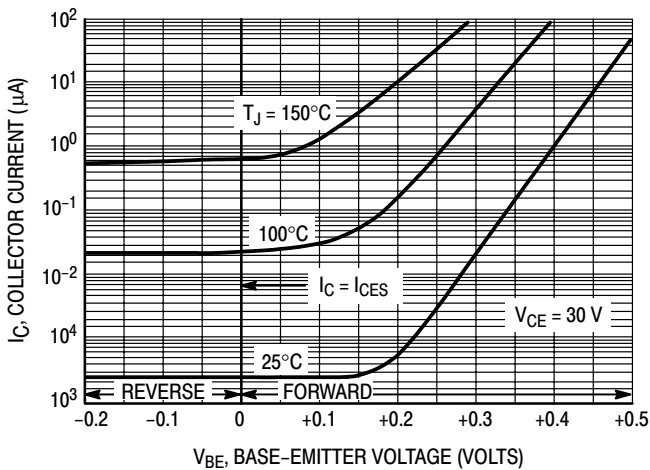


Figure 12. Collector Cut-Off Region

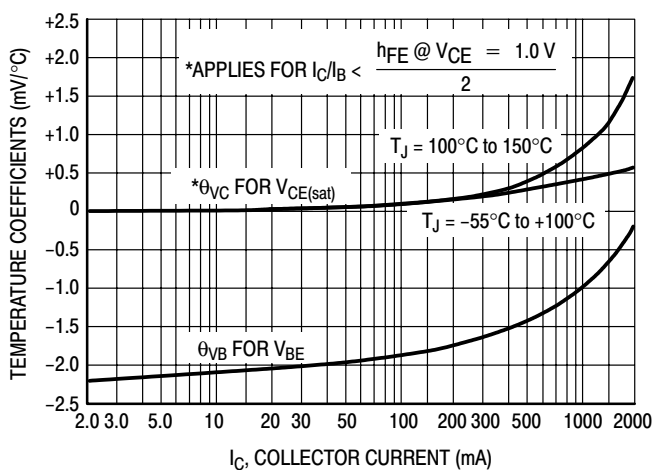


Figure 13. Temperature Coefficients

## Medium-Power Plastic NPN Silicon Transistors

... designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage —  
 $V_{CE(sat)} = 0.6 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Amp}$
- Excellent Power Dissipation Due to Thermopad Construction —  
 $P_D = 30 \text{ W @ } T_C = 25^\circ\text{C}$
- Excellent Safe Operating Area
- Gain Specified to  $I_C = 1.0 \text{ Amp}$
- Complement to PNP 2N4918, 2N4919, 2N4920

### \*MAXIMUM RATINGS

Rating	Symbol	2N4921	2N4922	2N4923	Unit
Collector–Emitter Voltage	$V_{CEO}$	40	60	80	Vdc
Collector–Base Voltage	$V_{CB}$	40	60	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous (1)	$I_C$	1.0 3.0			Adc
Base Current — Continuous	$I_B$	1.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	30 0.24			Watts W/ $^\circ\text{C}$
Operating & Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150			$^\circ\text{C}$

### THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	4.16	$^\circ\text{C/W}$

(1) The 1.0 Amp maximum  $I_C$  value is based upon JEDEC current gain requirements.  
The 3.0 Amp maximum value is based upon actual current handling capability of the device (see Figures 5 and 6)

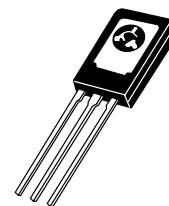
(2) Recommend use of thermal compound for lowest thermal resistance.

\*Indicates JEDEC Registered Data.

**2N4921  
thru  
2N4923 \***

\*ON Semiconductor Preferred Device

**1 AMPERE  
GENERAL-PURPOSE  
POWER TRANSISTORS  
40–80 VOLTS  
30 WATTS**

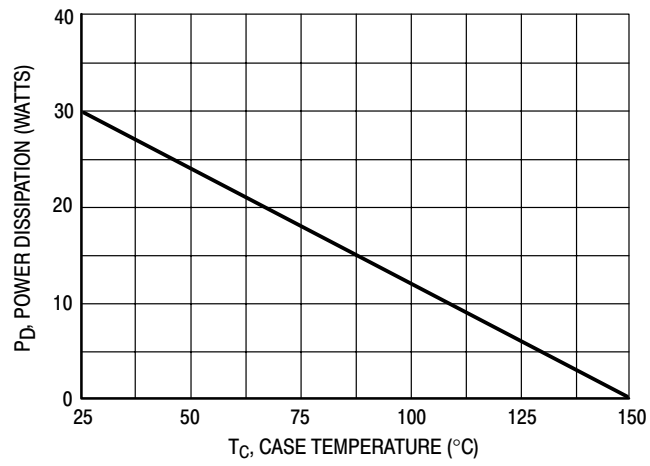


**CASE 77-09  
TO-225AA TYPE**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.



## 2N4921 thru 2N4923



**Figure 1. Power Derating**

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

# 2N4921 thru 2N4923

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (3) ( $I_C = 0.1 \text{ Adc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	40 60 80	—	Vdc
Collector Cutoff Current ( $V_{CE} = 20 \text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 30 \text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40 \text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— — —	0.5 0.5 0.5	mAdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB(off)} = 1.5 \text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$	— —	0.1 0.5	mAdc
Collector Cutoff Current ( $V_{CB} = \text{Rated } V_{CB}$ , $I_E = 0$ )	$I_{CBO}$	—	0.1	mAdc
Emitter Cutoff Current ( $V_{EB} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc

## ON CHARACTERISTICS

DC Current Gain (3) ( $I_C = 50 \text{ mAdc}$ , $V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 500 \text{ mAdc}$ , $V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 1.0 \text{ Adc}$ , $V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$	40 30 10	— 150 —	—
Collector–Emitter Saturation Voltage (3) ( $I_C = 1.0 \text{ Adc}$ , $I_B = 0.1 \text{ Adc}$ )	$V_{CE(sat)}$	—	0.6	Vdc
Base–Emitter Saturation Voltage (3) ( $I_C = 1.0 \text{ Adc}$ , $I_B = 0.1 \text{ Adc}$ )	$V_{BE(sat)}$	—	1.3	Vdc
Base–Emitter On Voltage (3) ( $I_C = 1.0 \text{ Adc}$ , $V_{CE} = 1.0 \text{ Vdc}$ )	$V_{BE(on)}$	—	1.3	Vdc

## SMALL–SIGNAL CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 250 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	$f_T$	3.0	—	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 100 \text{ kHz}$ )	$C_{ob}$	—	100	pF
Small–Signal Current Gain ( $I_C = 250 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ )	$h_{fe}$	25	—	—

(3) Pulse Test:  $PW \approx 300 \mu\text{s}$ , Duty Cycle  $\approx 2.0\%$ .

\*Indicates JEDEC Registered Data.

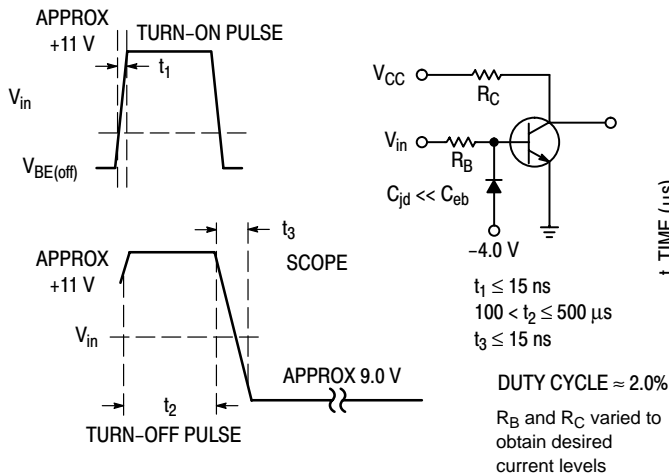


Figure 2. Switching Time Equivalent Circuit

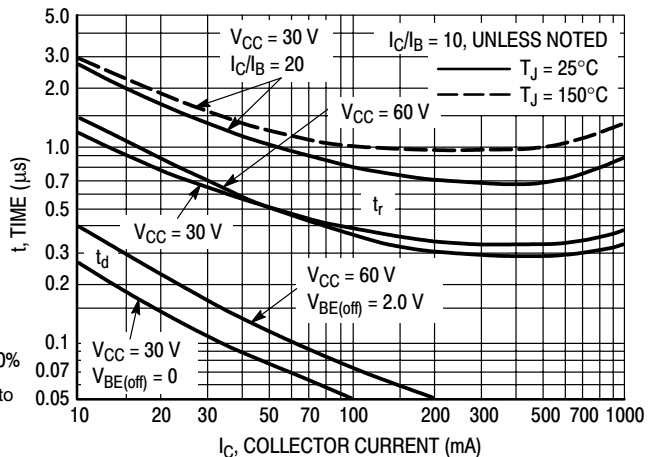
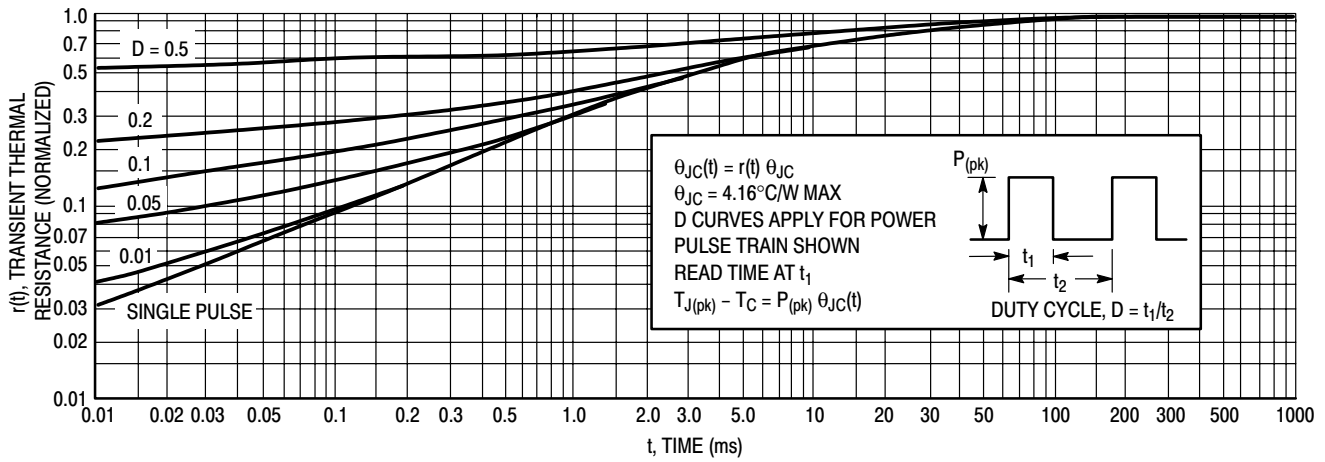
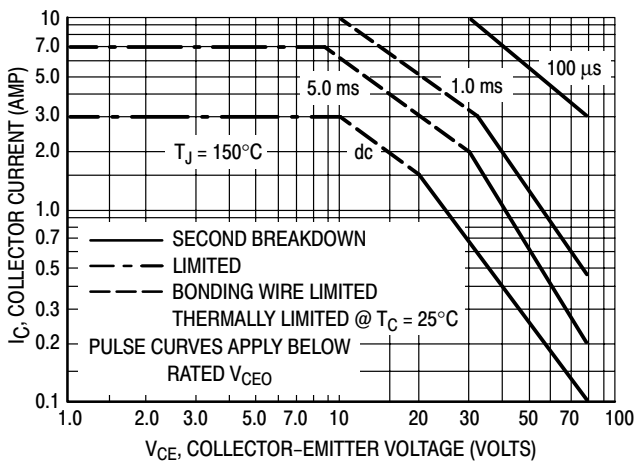


Figure 3. Turn-On Time

## 2N4921 thru 2N4923



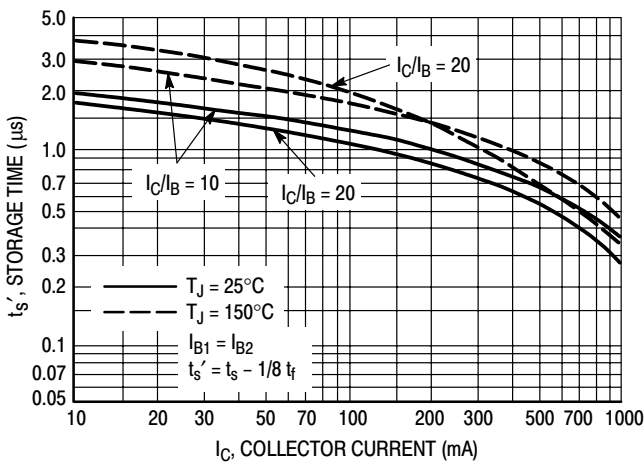
**Figure 4. Thermal Response**



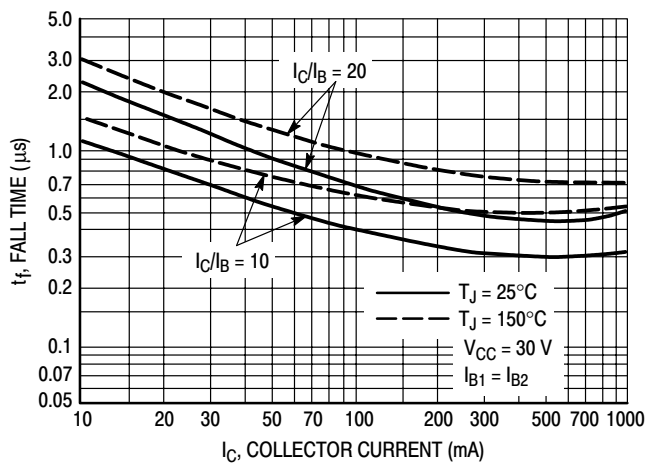
**Figure 5. Active-Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 6. Storage Time**



**Figure 7. Fall Time**

2N4921 thru 2N4923

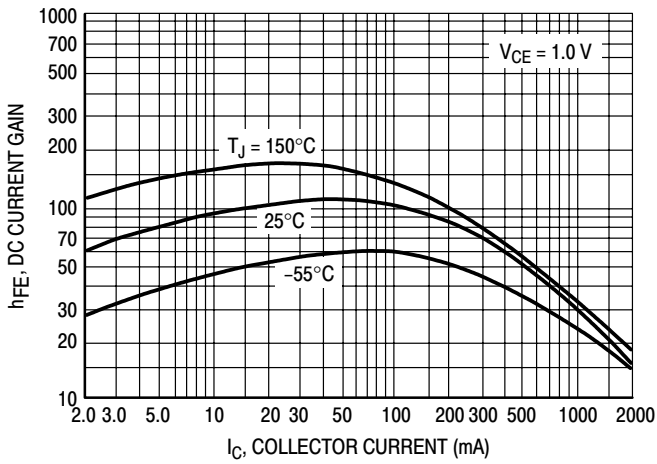


Figure 8. Current Gain

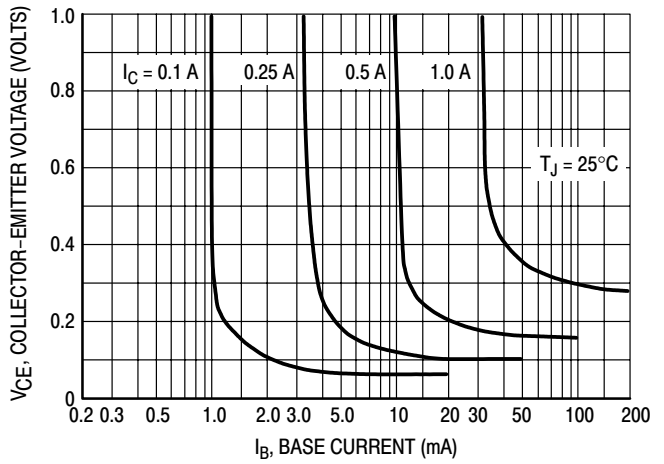


Figure 9. Collector Saturation Region

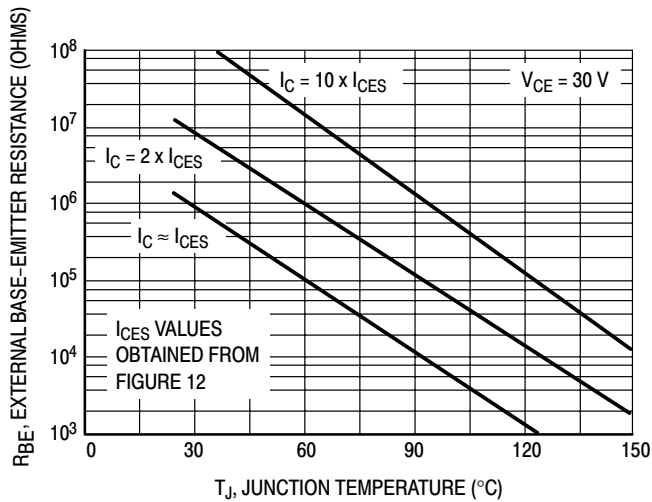


Figure 10. Effects of Base-Emitter Resistance

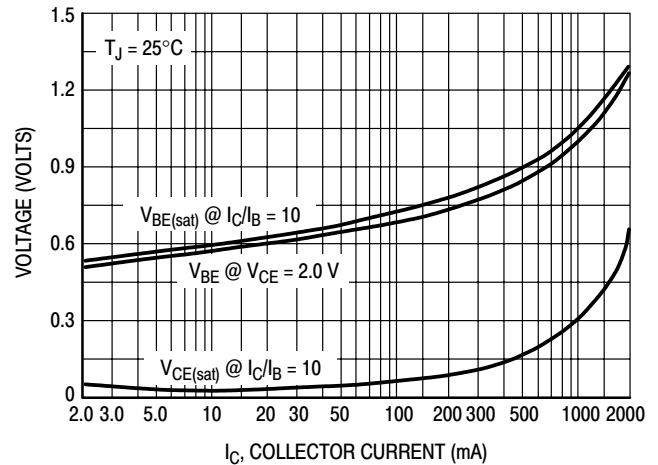


Figure 11. "On" Voltage

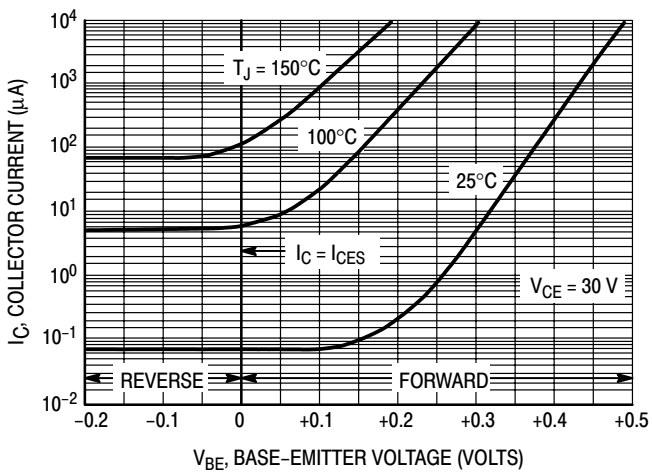


Figure 12. Collector Cut-Off Region

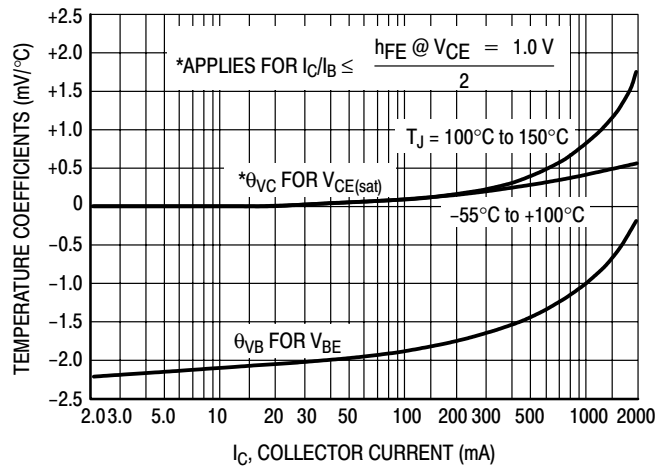


Figure 13. Temperature Coefficients

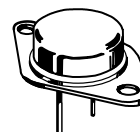
# NPN Silicon Transistors

... fast switching speeds and high current capacity ideally suit these parts for use in switching regulators, inverters, wide-band amplifiers and power oscillators in industrial and commercial applications.

- High Speed –  $t_f = 0.5 \mu\text{s}$  (Max)
- High Current –  $I_{C(\text{max})} = 30$  Amps
- Low Saturation –  $V_{CE(\text{sat})} = 2.5$  V (Max) @  $I_C = 20$  Amps

**2N5038**

**20 AMPERE  
NPN SILICON  
POWER TRANSISTOR  
90 VOLTS  
140 WATTS**



CASE 1-07  
TO-204AA  
(TO-3)

**\*MAXIMUM RATINGS**

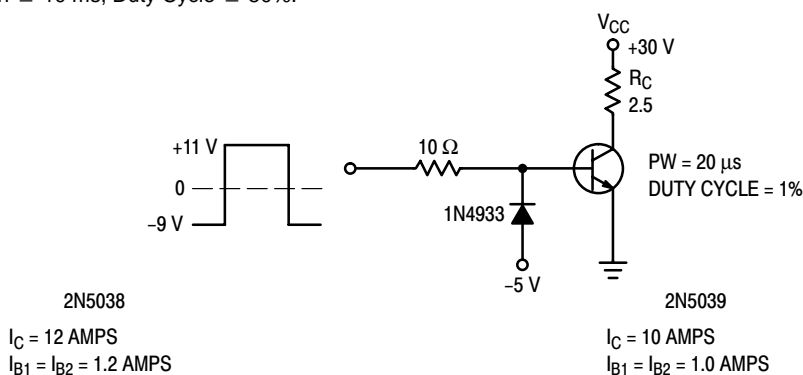
Rating	Symbol	Value	Unit
Collector–Base Voltage	$V_{CB0}$	150	Vdc
Collector–Emitter Voltage	$V_{CEV}$	150	Vdc
Emitter–Base Voltage	$V_{EB0}$	7	Vdc
Collector Current – Continuous Peak (1)	$I_C$ $I_{CM}$	20 30	Adc
Base Current – Continuous	$I_B$	5	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	140 0.8	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^\circ\text{C/W}$

\*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width  $\leq 10$  ms, Duty Cycle  $\leq 50\%$ .



**Figure 1. Switching Time Test Circuit**

# 2N5038

\*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (2) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	90	–	Vdc
Collector Cutoff Current ( $V_{CE} = 140\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ V}$ ) ( $V_{CE} = 100\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	– –	50 10	mAdc
Emitter Cutoff Current ( $V_{EB} = 5\text{ Vdc}$ , $I_C = 0$ ) ( $V_{EB} = 7\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	– –	5 50	mAdc

## ON CHARACTERISTICS (2)

DC Current Gain ( $I_C = 12\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$h_{FE}$	20	100	–
Collector–Emitter Saturation Voltage ( $I_C = 20\text{ Adc}$ , $I_B = 5\text{ Adc}$ )	$V_{CE(sat)}$	–	2.5	Vdc
Base–Emitter Saturation Voltage ( $I_C = 20\text{ Adc}$ , $I_B = 5\text{ Adc}$ )	$V_{BE(sat)}$	–	3.3	Vdc

## DYNAMIC CHARACTERISTICS

Magnitude of Common–Emitter Small–Signal Short–Circuit Forward Current Transfer Ratio ( $I_C = 2\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 5\text{ MHz}$ )	$ h_{fe} $	12	–	–
---	------------	----	---	---

## SWITCHING CHARACTERISTICS

RESISTIVE LOAD					
Rise Time	( $V_{CC} = 30\text{ Vdc}$ ) ( $I_C = 12\text{ Adc}$ , $I_{B1} = I_{B2} = 1.2\text{ Adc}$ )	$t_r$	–	0.5	$\mu\text{s}$
Storage Time		$t_s$	–	1.5	$\mu\text{s}$

\*Indicates JEDEC Registered Data.

(2) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

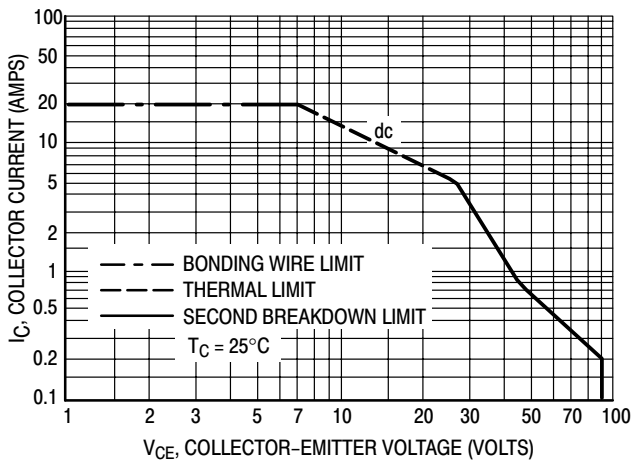


Figure 2. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Second breakdown pulse limits are valid for duty cycles to 10%. At high case temperatures, thermal limitations may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# Silicon NPN Power Transistors

... for use in power amplifier and switching circuits, — excellent safe area limits. Complement to PNP 2N5194, 2N5195.

**2N5191**  
**2N5192\***

\*ON Semiconductor Preferred Device

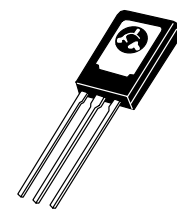
**4 AMPERE**  
**POWER TRANSISTORS**  
**SILICON NPN**  
**60–80 VOLTS**  
**40 WATTS**

**\*MAXIMUM RATINGS**

Rating	Symbol	2N5191	2N5192	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	80	Vdc
Collector–Base Voltage	$V_{CB}$	60	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current	$I_C$	4.0		Adc
Base Current	$I_B$	1.0		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40	320	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	3.12	$^\circ\text{C}$



**CASE 77–09**  
**TO–225AA TYPE**

**\*ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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**OFF CHARACTERISTICS**

Collector–Emitter Sustaining Voltage (1) ( $I_C = 0.1 \text{ Adc}, I_B = 0$ )	2N5191 2N5192	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 60 \text{ Vdc}, I_B = 0$ ) ( $V_{CE} = 80 \text{ Vdc}, I_B = 0$ )	2N5191 2N5192	$I_{CEO}$	— —	1.0 1.0	mAdc
Collector Cutoff Current ( $V_{CE} = 60 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 80 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 60 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 80 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$ )	2N5191 2N5192 2N5191 2N5192	$I_{CEX}$	— — — —	0.1 0.1 2.0 2.0	mAdc
Collector Cutoff Current ( $V_{CB} = 60 \text{ Vdc}, I_E = 0$ ) ( $V_{CB} = 80 \text{ Vdc}, I_E = 0$ )	2N5191 2N5192	$I_{CBO}$	— —	0.1 0.1	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}, I_C = 0$ )		$I_{EBO}$	—	1.0	mAdc

(1) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

\*Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# 2N5191 2N5192

\*ELECTRICAL CHARACTERISTICS — continued ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>ON CHARACTERISTICS</b>					
DC Current Gain (2) ( $I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ )	2N5191	25	100	—	
	2N5192	20	80	—	
	( $I_C = 4.0 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ )	2N5191	10	—	—
	2N5192	7.0	—	—	
Collector–Emitter Saturation Voltage (2) ( $I_C = 1.5 \text{ Adc}, I_B = 0.15 \text{ Adc}$ ) ( $I_C = 4.0 \text{ Adc}, I_B = 1.0 \text{ Adc}$ )	$V_{CE(sat)}$	—	0.6	Vdc	
		—	1.4	Vdc	
Base–Emitter On Voltage (2) ( $I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ )	$V_{BE(on)}$	—	1.2	Vdc	
<b>DYNAMIC CHARACTERISTICS</b>					
Current–Gain — Bandwidth Product ( $I_C = 1.0 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$ )	$f_T$	2.0	—	MHz	

(2) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

\*Indicates JEDEC Registered Data.

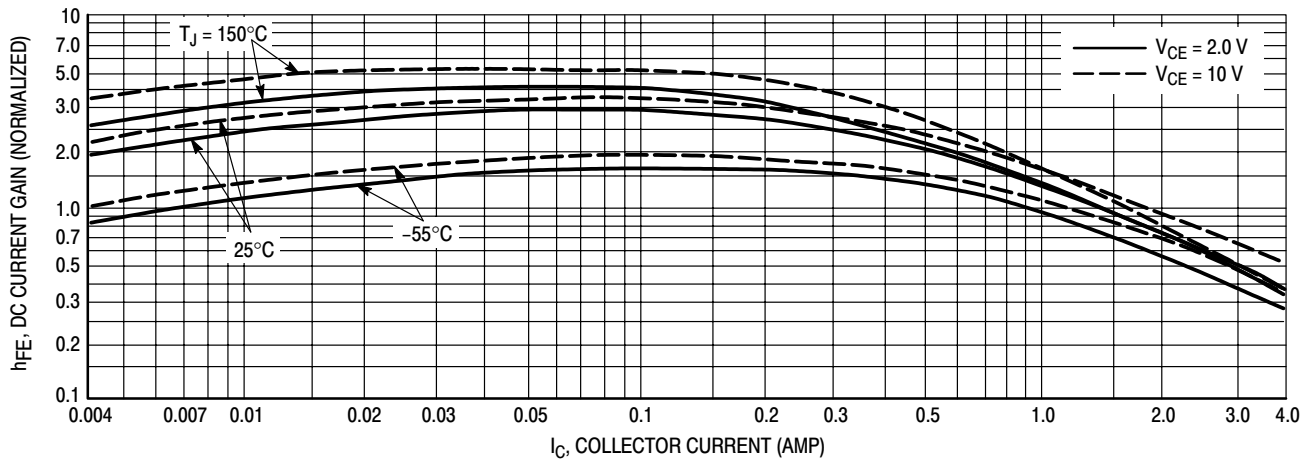


Figure 1. DC Current Gain

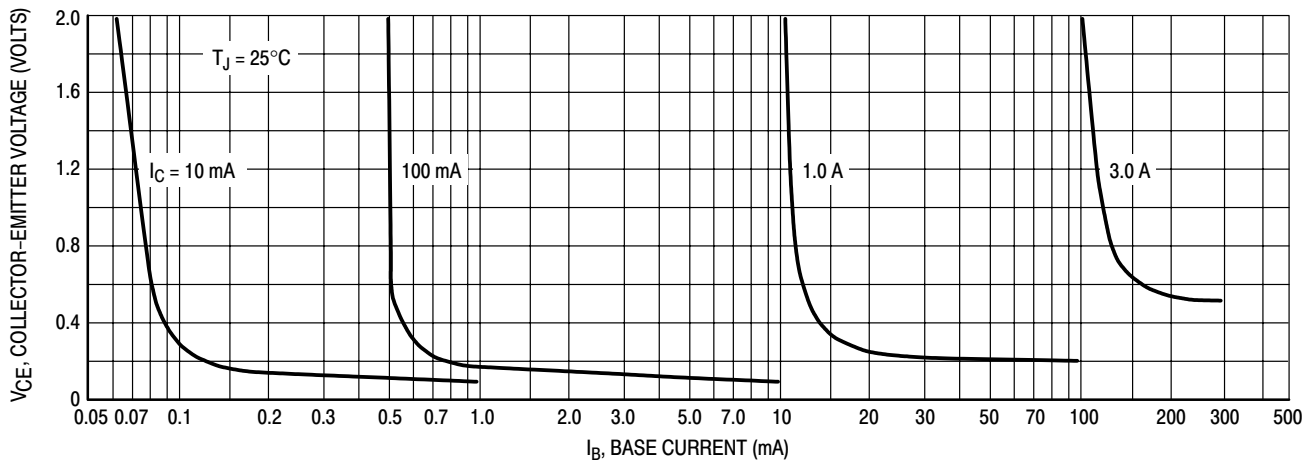


Figure 2. Collector Saturation Region



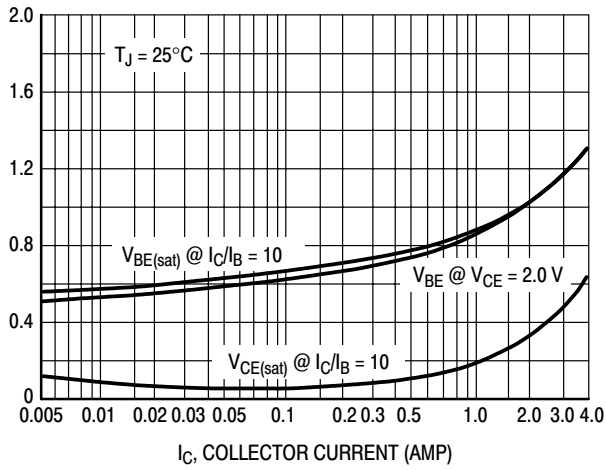


Figure 3. "On" Voltages

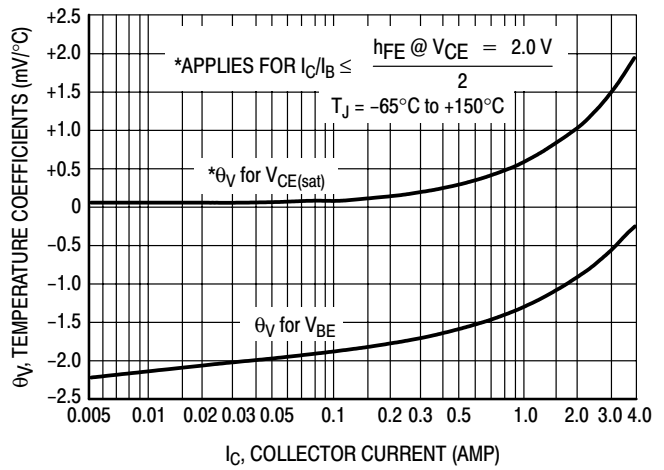


Figure 4. Temperature Coefficients

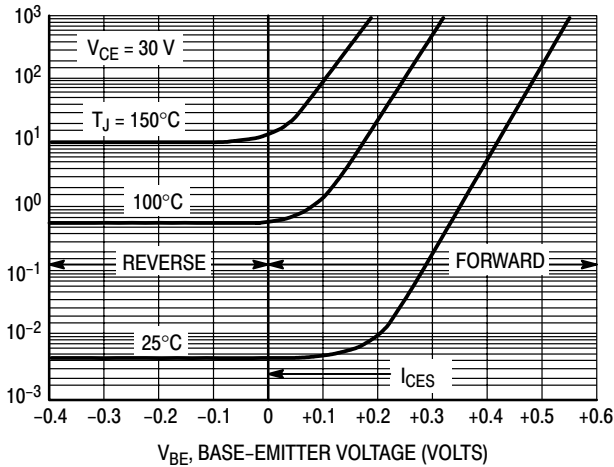


Figure 5. Collector Cut-Off Region

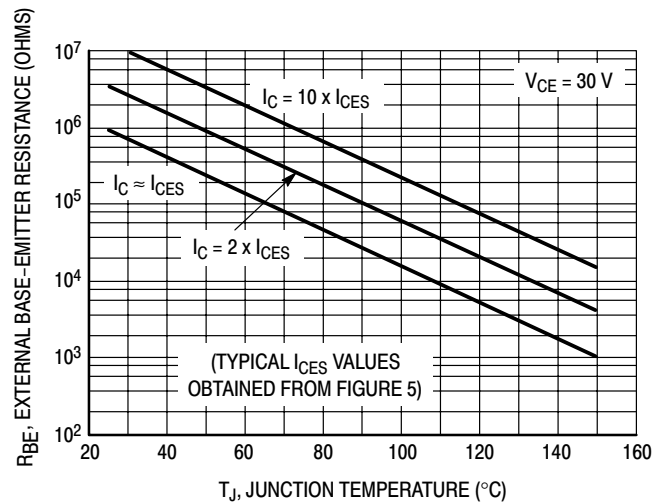


Figure 6. Effects of Base-Emitter Resistance

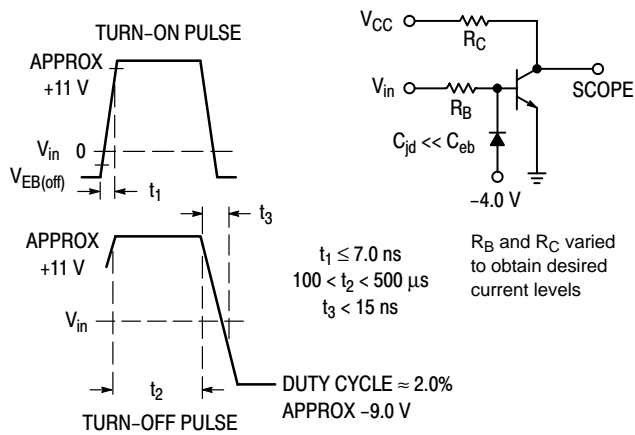


Figure 7. Switching Time Equivalent Test Circuit

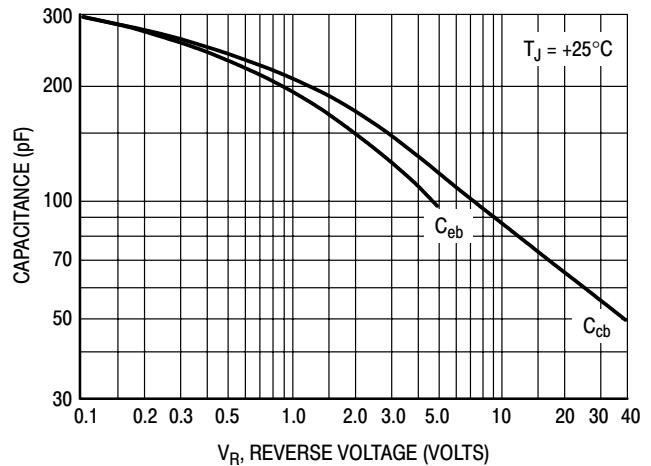


Figure 8. Capacitance

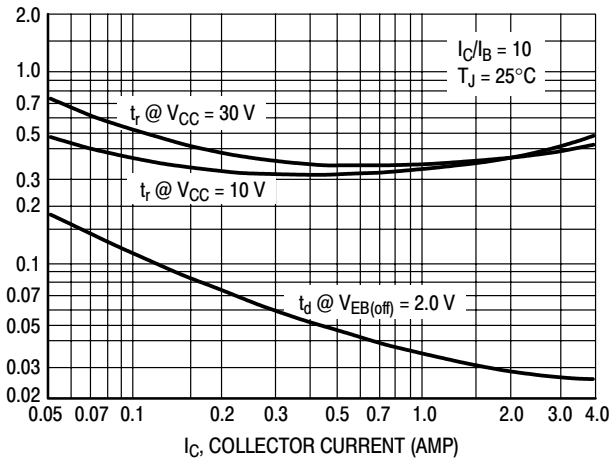


Figure 9. Turn-On Time

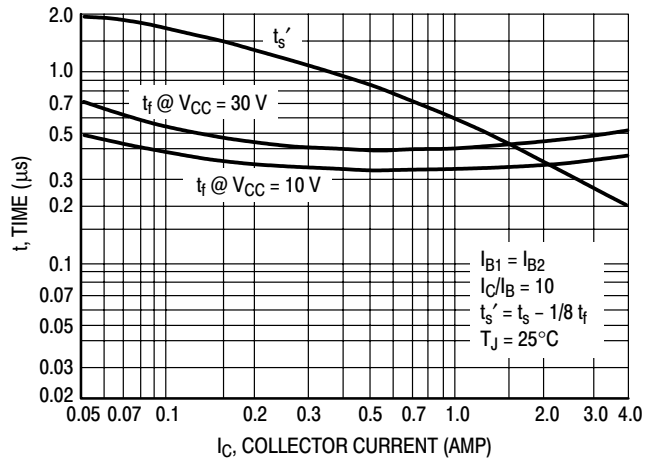


Figure 10. Turn-Off Time

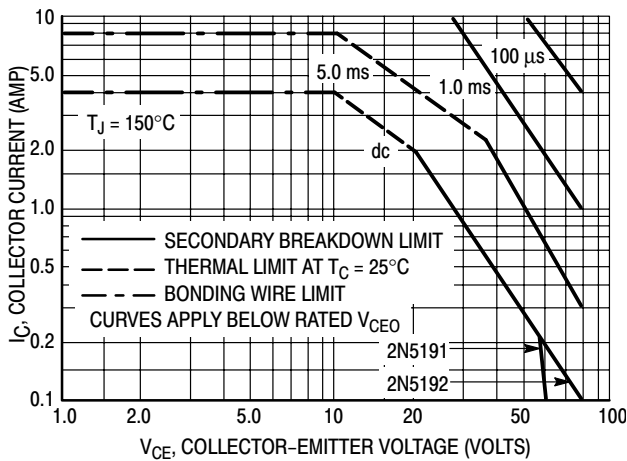


Figure 11. Rating and Thermal Data Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

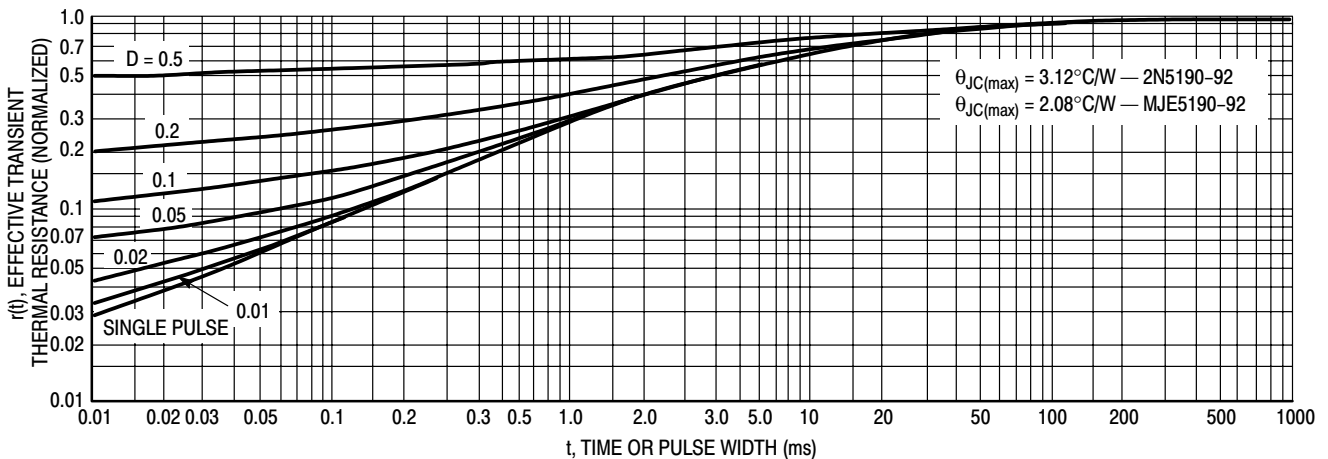


Figure 12. Thermal Response

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

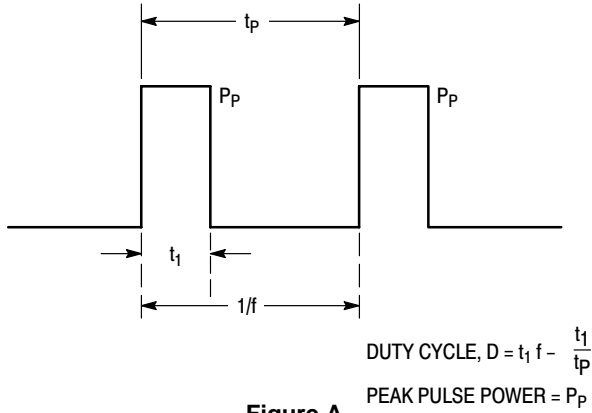


Figure A

A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find  $\theta_{JC}(t)$ , multiply the value obtained from Figure 12 by the steady state value  $\theta_{JC}$ .

Example:

The 2N5190 is dissipating 50 watts under the following conditions:  $t_1 = 0.1$  ms,  $t_p = 0.5$  ms. ( $D = 0.2$ ).

Using Figure 12, at a pulse width of 0.1 ms and  $D = 0.2$ , the reading of  $r(t_1, D)$  is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ\text{C}$$

# Silicon PNP Power Transistors

... for use in power amplifier and switching circuits, — excellent safe area limits. Complement to NPN 2N5191, 2N5192

## 2N5194 2N5195\*

\*ON Semiconductor Preferred Device

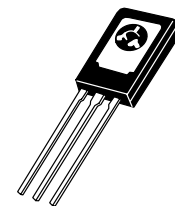
**4 AMPERE  
POWER TRANSISTORS  
SILICON PNP  
60–80 VOLTS**

### \*MAXIMUM RATINGS

Rating	Symbol	2N5194	2N5195	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	80	Vdc
Collector–Base Voltage	$V_{CB}$	60	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current	$I_C$	4.0		Adc
Base Current	$I_B$	1.0		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40	320	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C/W}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	3.12	$^\circ\text{C/W}$



**CASE 77–09  
TO–225AA TYPE**

### \*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 0.1 \text{ Adc}, I_B = 0$ )	2N5194 2N5195	$V_{CEO(sus)}$	60 80	— — Vdc
Collector Cutoff Current ( $V_{CE} = 60 \text{ Vdc}, I_B = 0$ ) ( $V_{CE} = 80 \text{ Vdc}, I_B = 0$ )	2N5194 2N5195	$I_{CEO}$	— —	1.0 1.0 mAdc
Collector Cutoff Current ( $V_{CE} = 60 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 60 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$ )	2N5194 2N5195 2N5194 2N5195	$I_{CEX}$	— — — —	0.1 0.1 2.0 2.0 mAdc
Collector Cutoff Current ( $V_{CB} = 60 \text{ Vdc}, I_E = 0$ ) ( $V_{CB} = 80 \text{ Vdc}, I_E = 0$ )	2N5194 2N5195	$I_{CBO}$	— —	0.1 0.1 mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}, I_C = 0$ )		$I_{EBO}$	—	1.0 mAdc

\*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# 2N5194 2N5195

\*ELECTRICAL CHARACTERISTICS — continued ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>ON CHARACTERISTICS</b>				
DC Current Gain (2) ( $I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ )	2N5194	25	100	—
	2N5195	20	80	—
	( $I_C = 4.0 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ )	10	—	—
	2N5194	7.0	—	—
2N5195	—	—	—	—
Collector–Emitter Saturation Voltage (2) ( $I_C = 1.5 \text{ Adc}, I_B = 0.15 \text{ Adc}$ ) ( $I_C = 4.0 \text{ Adc}, I_B = 1.0 \text{ Adc}$ )	$V_{CE(sat)}$	—	0.6	Vdc
	—	—	1.4	—
Base–Emitter On Voltage (2) ( $I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ )	$V_{BE(on)}$	—	1.2	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain — Bandwidth Product ( $I_C = 1.0 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$ )	$f_T$	2.0	—	MHz

\*Indicates JEDEC Registered Data.

(2) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

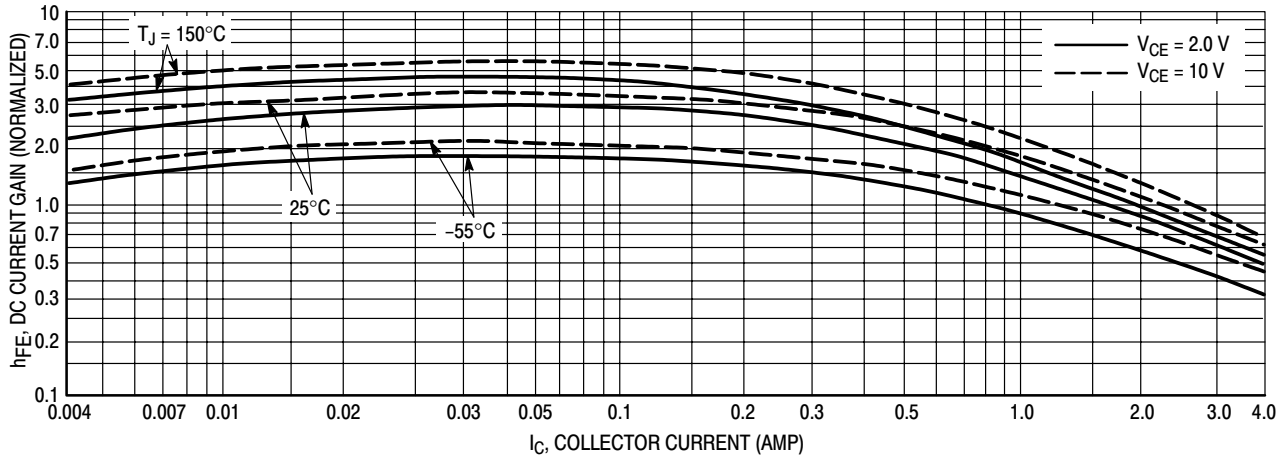


Figure 1. DC Current Gain

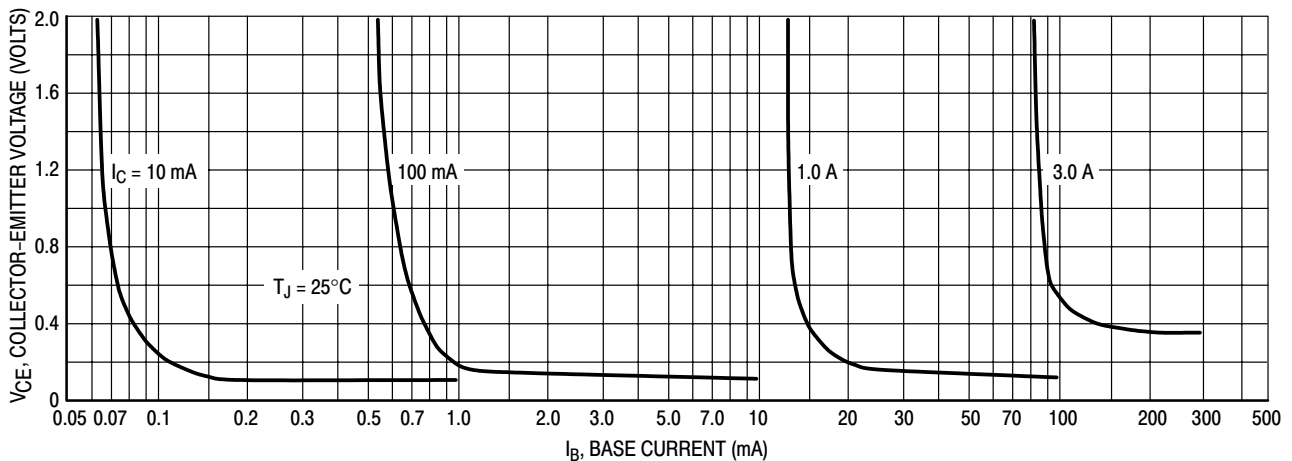


Figure 2. Collector Saturation Region

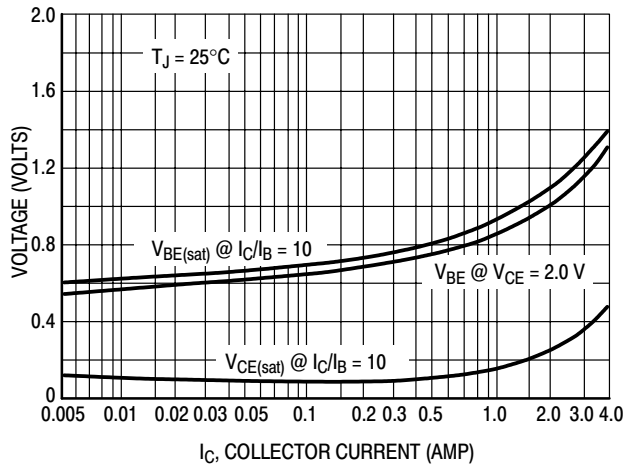


Figure 3. "On" Voltage

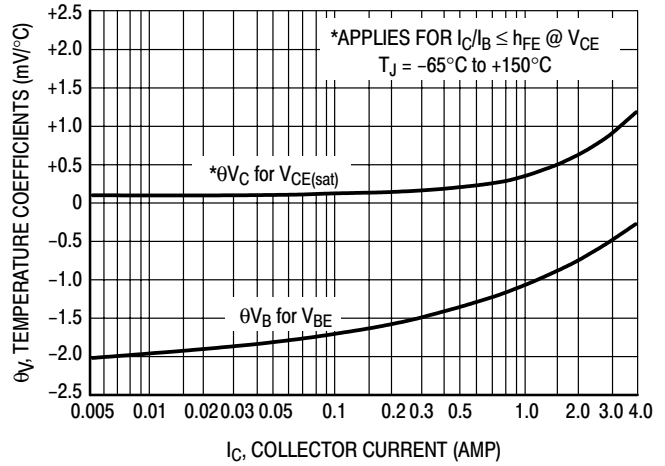


Figure 4. Temperature Coefficients

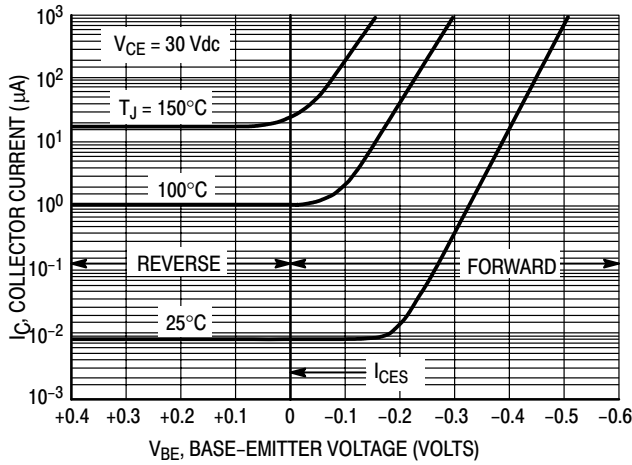


Figure 5. Collector Cut-Off Region

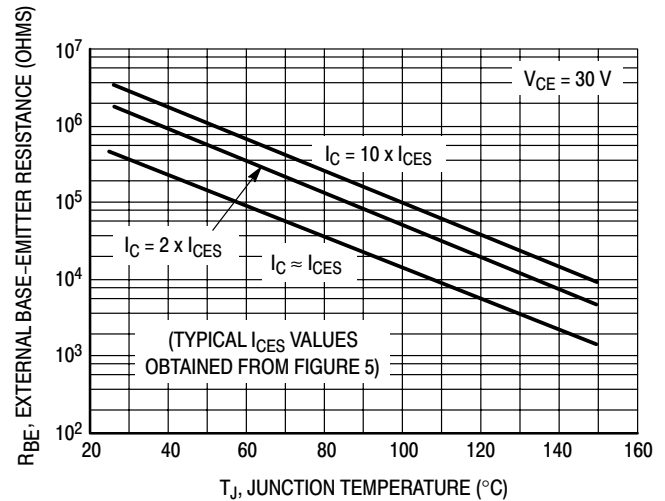


Figure 6. Effects of Base-Emitter Resistance

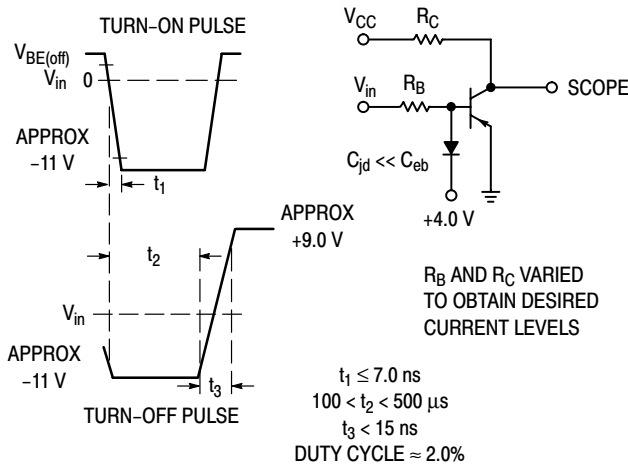


Figure 7. Switching Time Equivalent Test Circuit

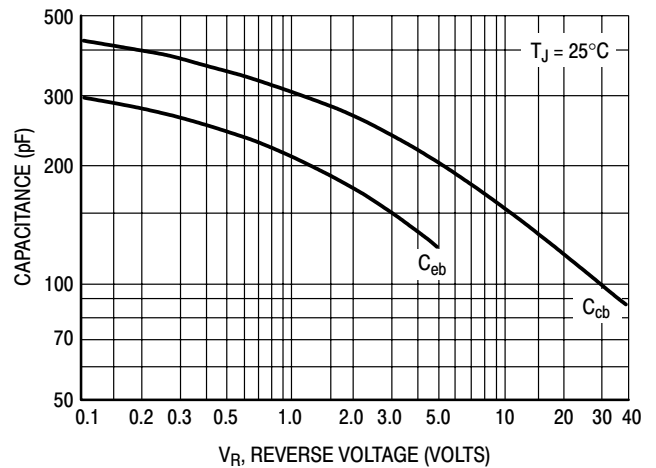
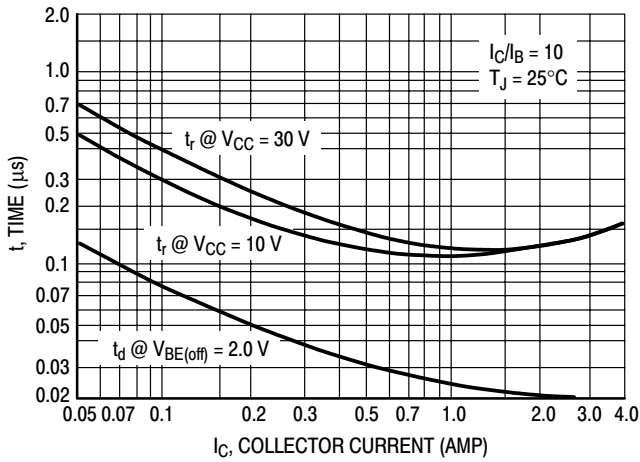
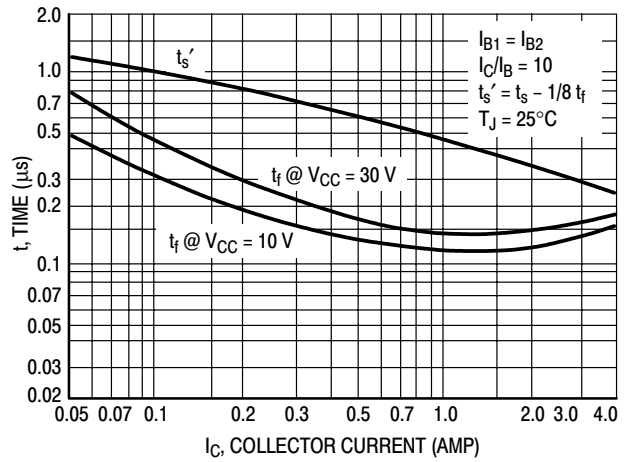


Figure 8. Capacitance

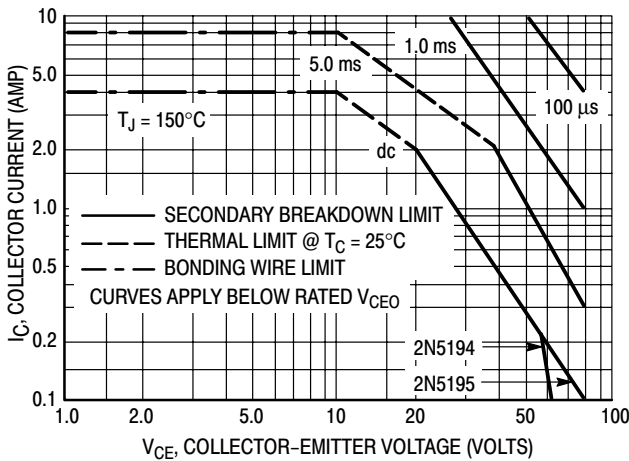
## 2N5194 2N5195



**Figure 9. Turn-On Time**



**Figure 10. Turn-Off Time**

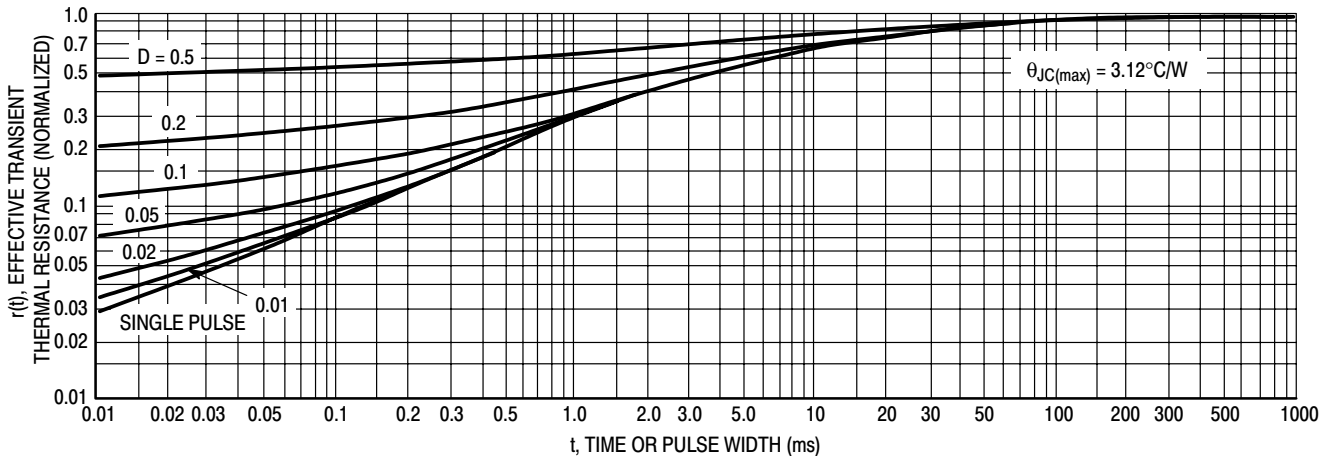


**Figure 11. Rating and Thermal Data  
Active-Region Safe Operating Area**

**Note 1:**

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on  $T_{J(pk)} = 150^\circ\text{C}$ .  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high-case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 12. Thermal Response**

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

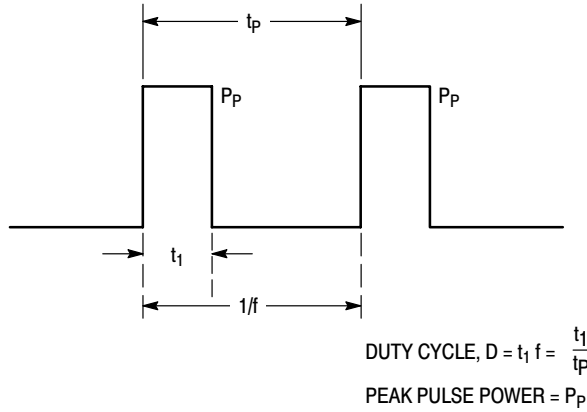


Figure 13.

A train of periodical power pulses can be represented by the model shown in Figure 13. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find  $\theta_{JC}(t)$ , multiply the value obtained from Figure 12 by the steady state value  $\theta_{JC}$ .

Example:

The 2N5193 is dissipating 50 watts under the following conditions:  $t_1 = 0.1$  ms,  $t_p = 0.5$  ms. ( $D = 0.2$ ).

Using Figure 12, at a pulse width of 0.1 ms and  $D = 0.2$ , the reading of  $r(t_1, D)$  is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ\text{C}$$



# High-Power NPN Silicon Transistor

... for use in power amplifier and switching circuits applications.

- Low Collector–Emitter Saturation Voltage –  
 $V_{CE(sat)} = 0.75 \text{ Vdc (Max) @ } I_C = 10 \text{ Adc}$

## \*MAXIMUM RATINGS

Rating	Symbol	2N5302	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	Vdc
Collector–Base Voltage	$V_{CB}$	60	Vdc
Collector Current – Continuous	$I_C$	30	Adc
Base Current	$I_B$	7.5	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.14	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.875	$^\circ\text{C/W}$
Thermal Resistance, Case to Ambient	$\theta_{CA}$	34	$^\circ\text{C/W}$

\*Indicates JEDEC Registered Data.

**2N5302**

**30 AMPERE  
POWER TRANSISTOR  
NPN SILICON  
60 VOLTS  
200 WATTS**

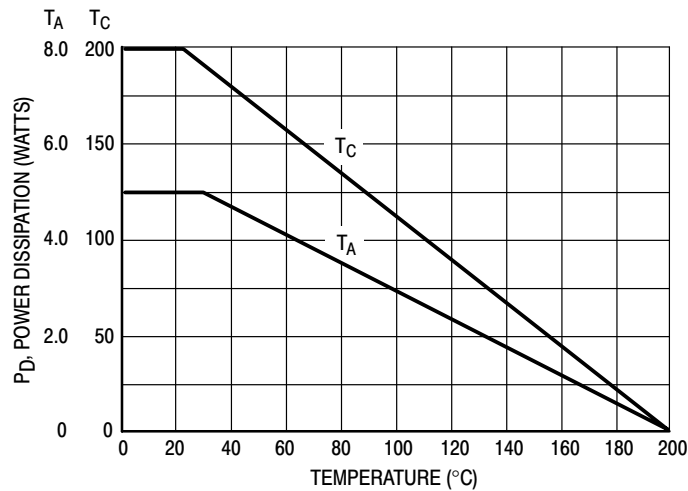
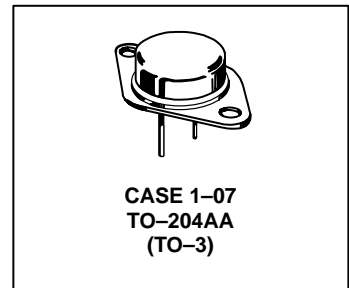


Figure 1. Power Temperature Derating Curve

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>*OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 1) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	5.0	mAcd
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ )	$I_{CEX}$	–	1.0	mAcd
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	–	10	mAcd
Collector Cutoff Current ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	1.0	mAcd
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	5.0	mAcd

**ON CHARACTERISTICS**

DC Current Gain (Note 1) *( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ ) *( $I_C = 15\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ ) ( $I_C = 30\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	40 15 5.0	– 60 –	–
*Collector–Emitter Saturation Voltage (Note 1) ( $I_C = 10\text{ Adc}$ , $I_B = 1.0\text{ Adc}$ ) ( $I_C = 20\text{ Adc}$ , $I_B = 2.0\text{ Adc}$ ) <sup>2</sup> ( $I_C = 30\text{ Adc}$ , $I_B = 6.0\text{ Adc}$ )	$V_{CE(sat)}$	– – –	0.75 2.0 3.0	Vdc
*Base Emitter Saturation Voltage (Note 1) ( $I_C = 10\text{ Adc}$ , $I_B = 1.0\text{ Adc}$ ) ( $I_C = 15\text{ Adc}$ , $I_B = 1.5\text{ Adc}$ ) ( $I_C = 20\text{ Adc}$ , $I_B = 2.0\text{ Adc}$ )	$V_{BE(sat)}$	– – –	1.7 1.8 2.5	Vdc
*Base–Emitter On Voltage (Note 1) ( $I_C = 15\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ ) ( $I_C = 30\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	– –	1.7 3.0	Vdc

**\*DYNAMIC CHARACTERISTICS**

Current–Gain – Bandwidth Product ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	2.0	–	MHz
Small–Signal Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	40	–	–

**\*SWITCHING CHARACTERISTICS**

Rise Time	$(V_{CC} = 30\text{ Vdc}$ , $I_C = 10\text{ Adc}$ , $I_{B1} = I_{B2} = 1.0\text{ Adc}$ )	$t_r$	–	1.0	$\mu\text{s}$
Storage Time		$t_s$	–	2.0	$\mu\text{s}$
Fall Time		$t_f$	–	1.0	$\mu\text{s}$

\*Indicates JEDEC Registered Data.

Note 1: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

**SWITCHING TIME EQUIVALENT TEST CIRCUITS**

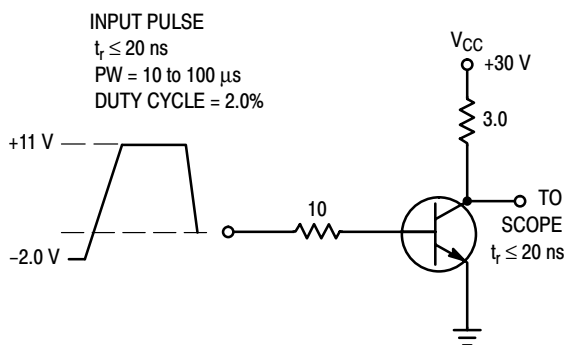


Figure 2. Turn–On time

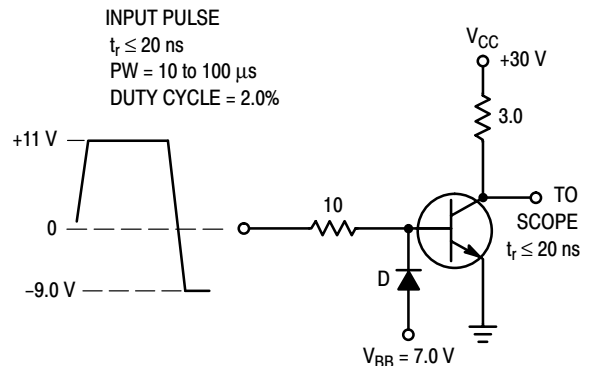


Figure 3. Turn–Off time

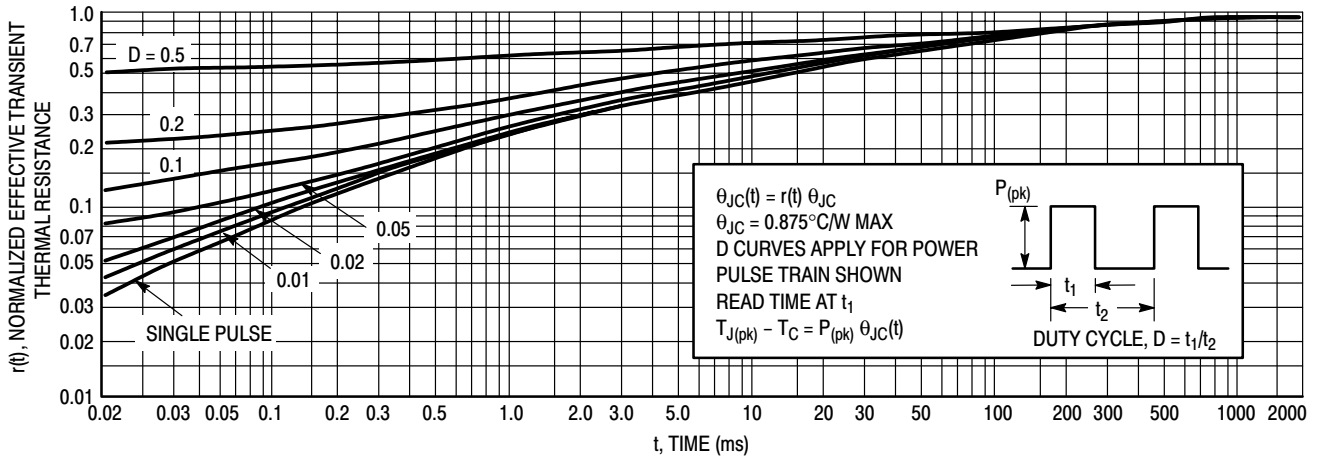


Figure 4. Thermal Response

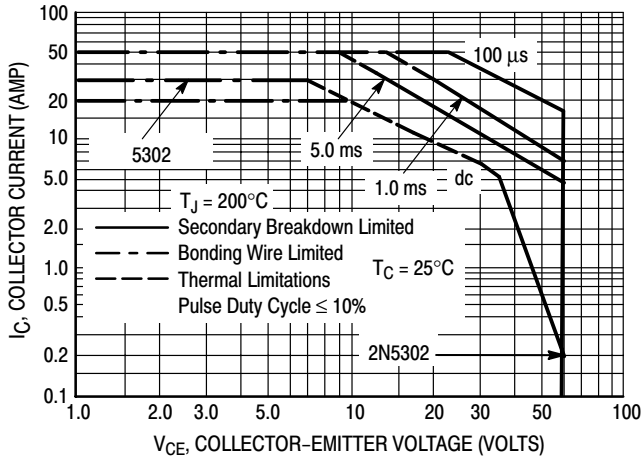


Figure 5. Active-Region Safe Operating Area

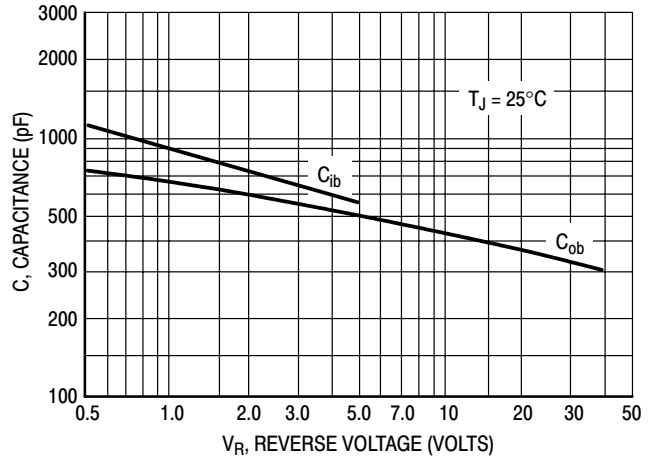


Figure 6. Capacitance versus Voltage

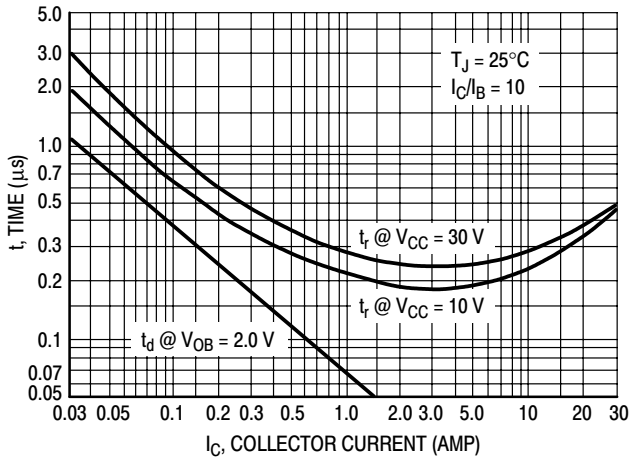


Figure 7. Turn-On Time

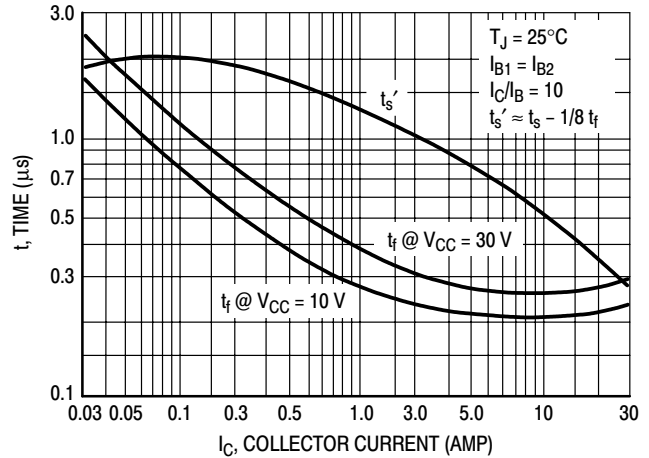


Figure 8. Turn-Off Time

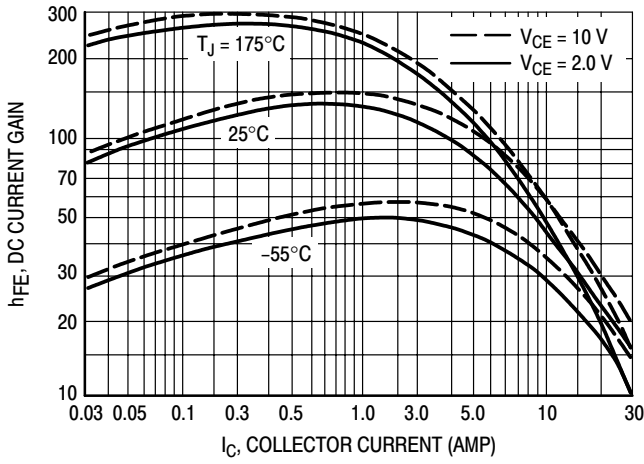


Figure 9. DC Current Gain

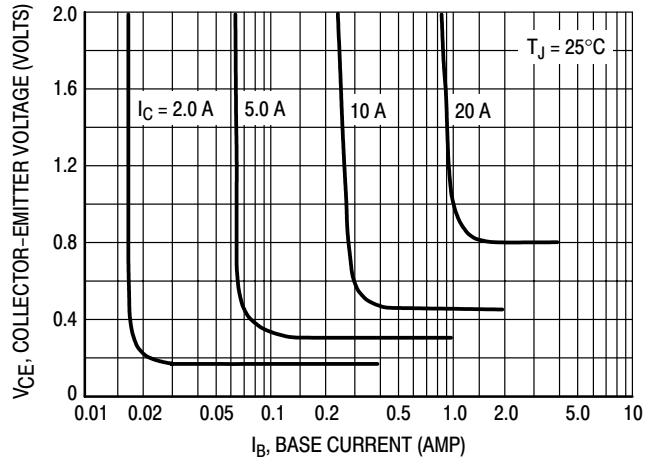


Figure 10. Collector Saturation Region

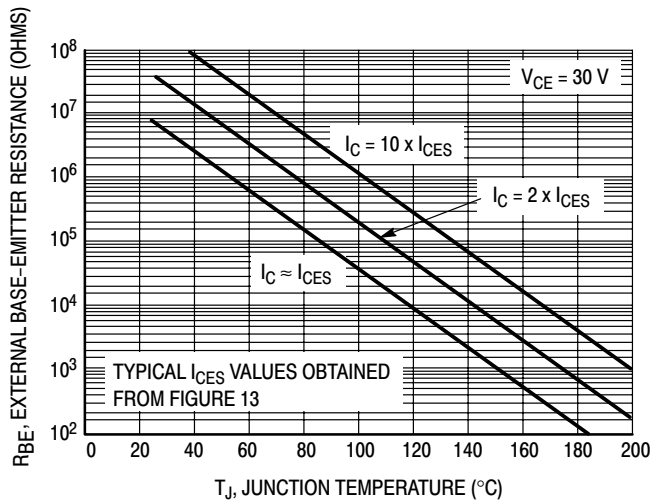


Figure 11. Effects of Base-Emitter Resistance

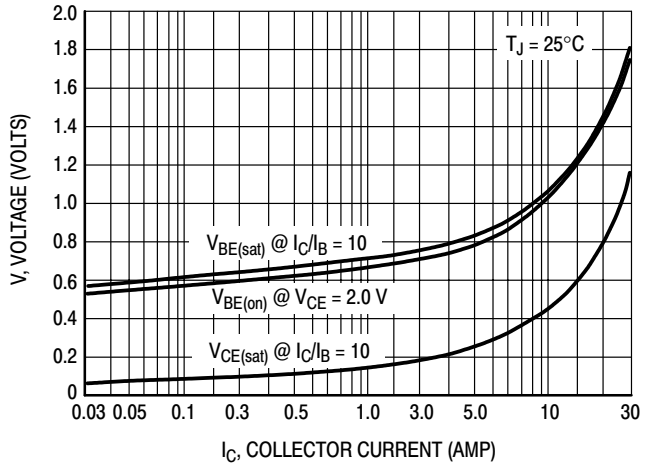


Figure 12. "On" Voltages

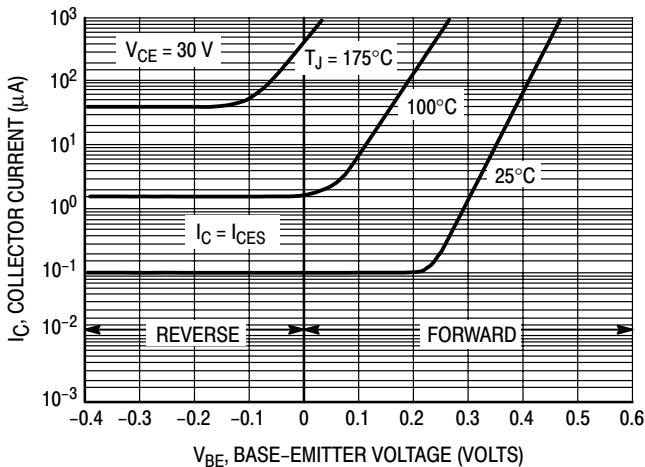


Figure 13. Collector Cut-Off Region

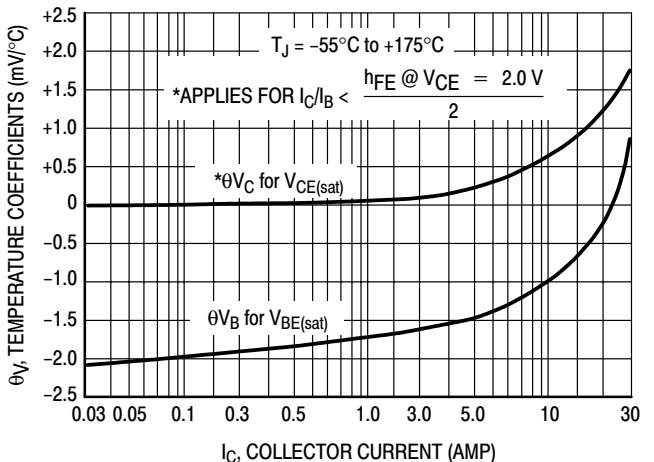


Figure 14. Temperature Coefficients

# High-Voltage - High Power Transistors

... designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector Emitter Sustaining Voltage –  
 $V_{CEO(sus)} = 140 \text{ Vdc}$
- High DC Current Gain – @  $I_C = 8.0 \text{ Adc}$   
 $h_{FE} = 15 \text{ (Min)}$
- Low Collector–Emitter Saturation Voltage –  
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) @ } I_C = 10 \text{ Adc}$

## MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	140	Vdc
Collector–Base Voltage	$V_{CB}$	140	Vdc
Emitter–Base Voltage	$V_{EB}$	7.0	Vdc
Collector Current – Continuous Peak	$I_C$	16 20	A dc
Base Current – Continuous	$I_B$	5.0	A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.14	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.875	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

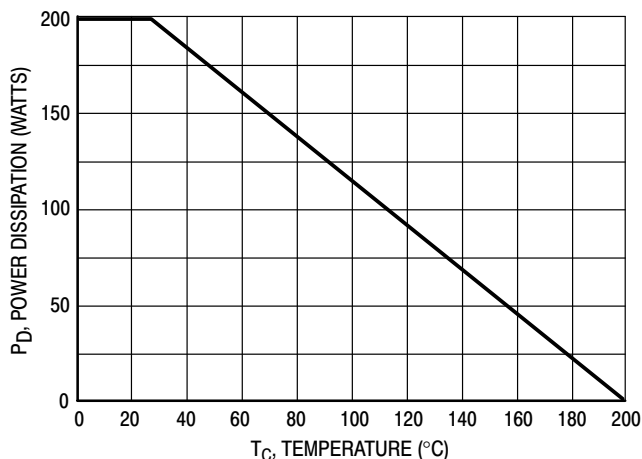


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All Limits are applicable and must be observed.

**NPN  
2N5631  
PNP  
2N6031**

**16 AMPERE  
POWER TRANSISTORS  
COMPLEMENTARY  
SILICON  
140 VOLTS  
200 WATTS**

**CASE 1-07  
TO-204AA  
(TO-3)**

# 2N5631 2N6031

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (2) ( $I_C = 200\text{ mA}$ , $I_B = 0$ )	$V_{CE(sus)}$	140	–	Vdc
Collector–Emitter Cutoff Current ( $V_{CE} = 70\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	2.0	mAdc
Collector–Emitter Cutoff Current ( $V_{CE} = \text{Rated } V_{CB}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CB}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	–	2.0 7.0	mAdc
Collector–Base Cutoff Current ( $V_{CB} = \text{Rated } V_{CB}$ , $I_E = 0$ )	$I_{CBO}$	–	2.0	mAdc
Emitter–Base Cutoff Current ( $V_{BE} = 7.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	5.0	mAdc

## ON CHARACTERISTICS (2)

DC Current Gain ( $I_C = 8\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ ) ( $I_C = 16\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$h_{FE}$	15 4.0	60 –	–
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ Adc}$ , $I_B = 1.0\text{ Adc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 4.0\text{ Adc}$ )	$V_{CE(sat)}$	– –	1.0 2.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 10\text{ Adc}$ , $I_B = 1.0\text{ Adc}$ )	$V_{BE(sat)}$	–	1.8	Vdc
Base–Emitter On Voltage ( $I_C = 8.0\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$V_{BE(on)}$	–	1.5	Vdc

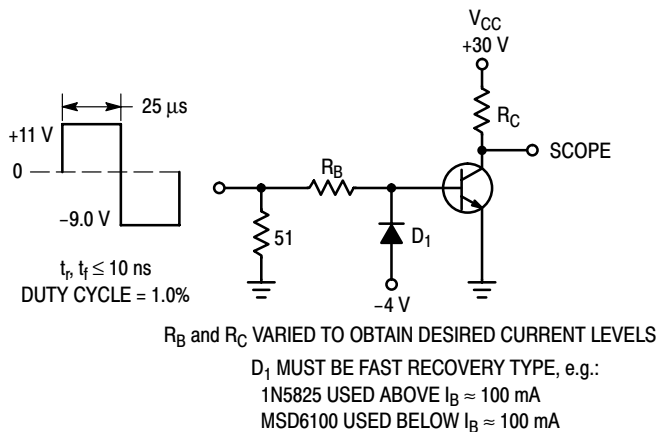
## DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product (3) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 20\text{ Vdc}$ , $f_{test} = 0.5\text{ MHz}$ )	$f_T$	1.0	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	2N5631 2N6031 $C_{ob}$	– –	500 1000	pF
Small–Signal Current Gain ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	15	–	–

\*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\geq 2.0\%$ .

(2)  $f_T = |h_{fe}| \cdot f_{test}$



For PNP test circuit, reverse all polarities and D1.

Figure 2. Switching Times Test Circuit

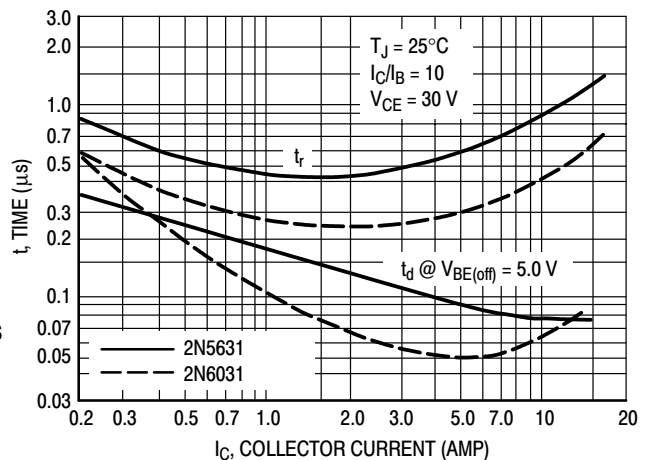


Figure 3. Turn–On Time

# 2N5631 2N6031

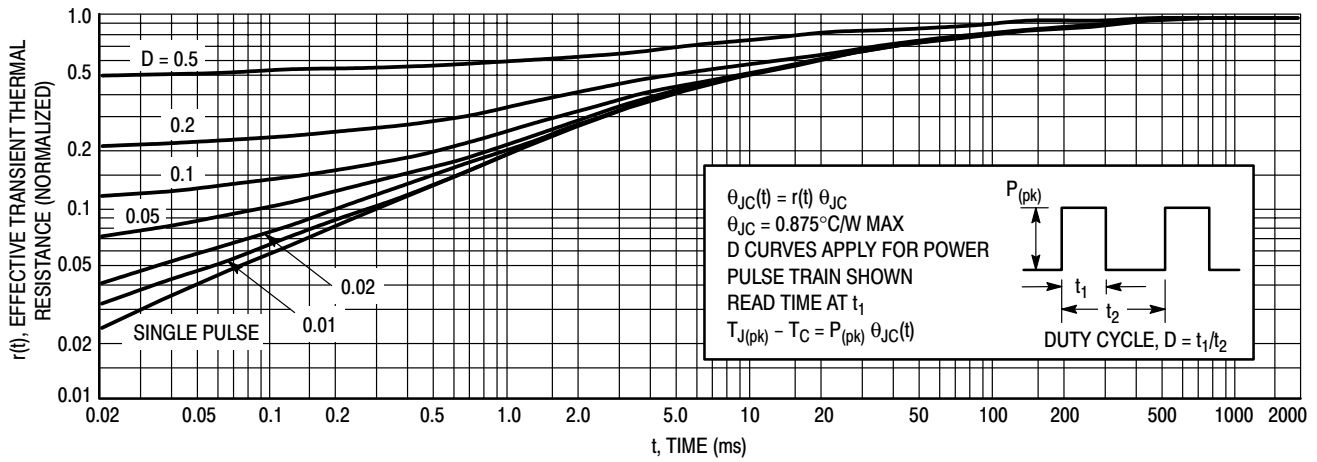


Figure 4. Thermal Response

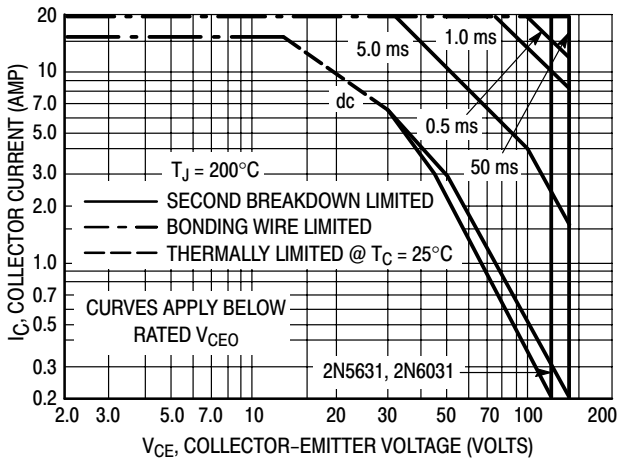
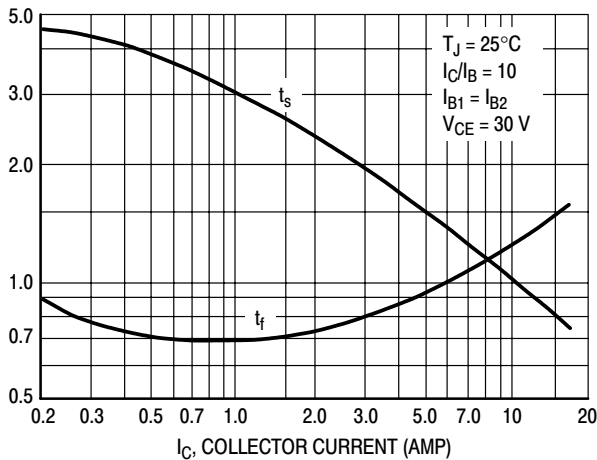


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 200^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

## NPN 2N5631



## PNP 2N6031

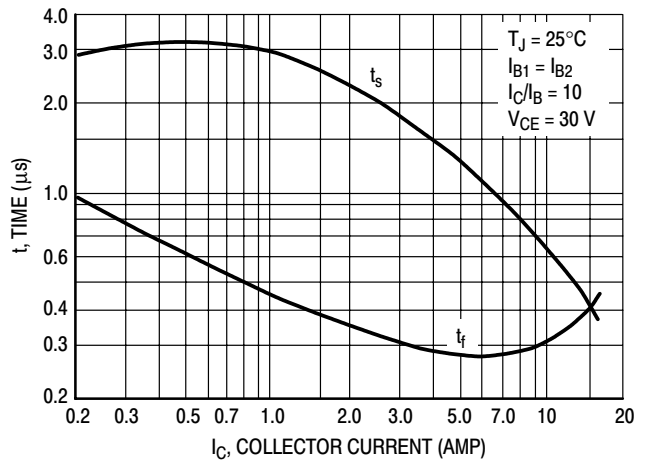


Figure 6. Turn-Off Time

# 2N5631 2N6031

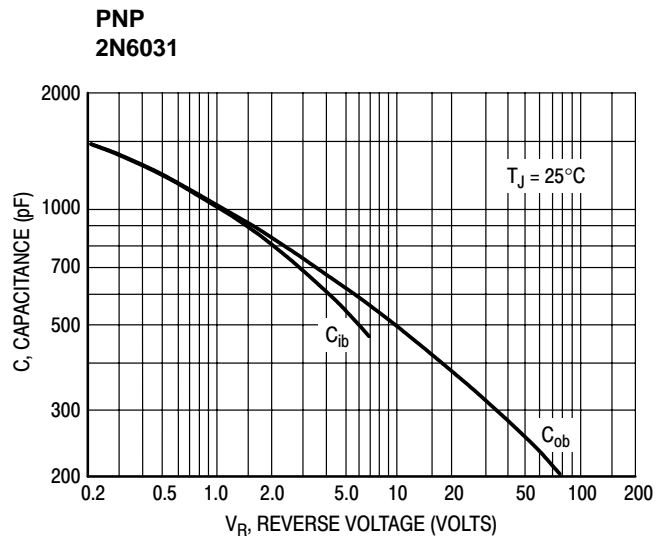
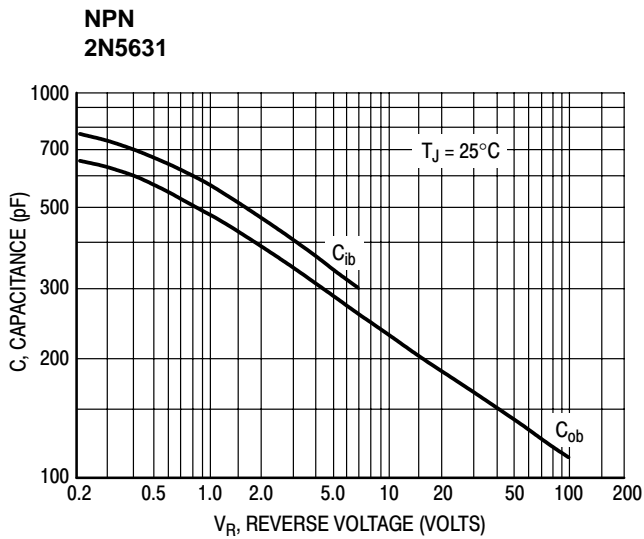


Figure 7. Capacitance

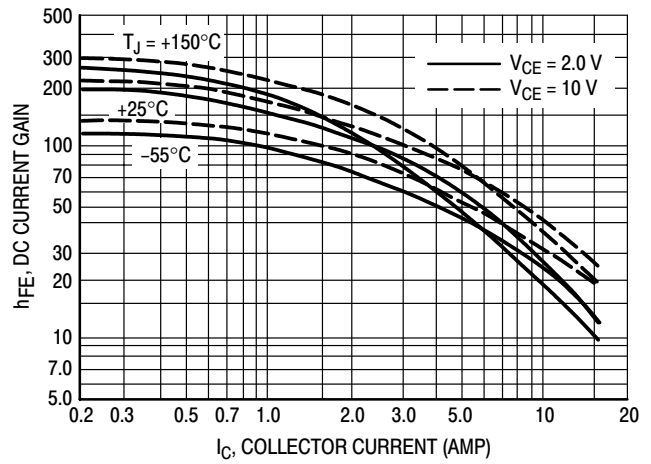
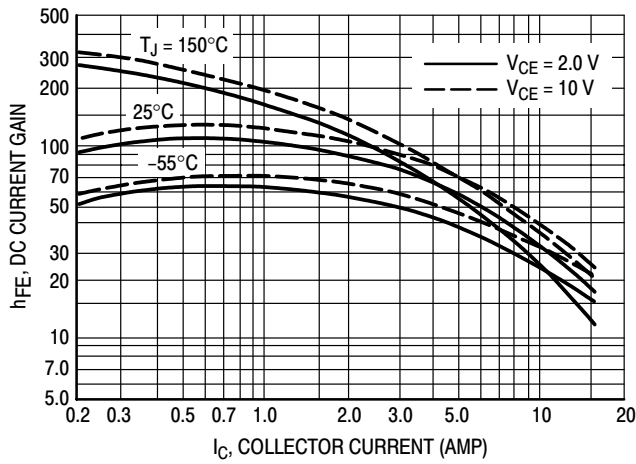


Figure 8. DC Current Gain

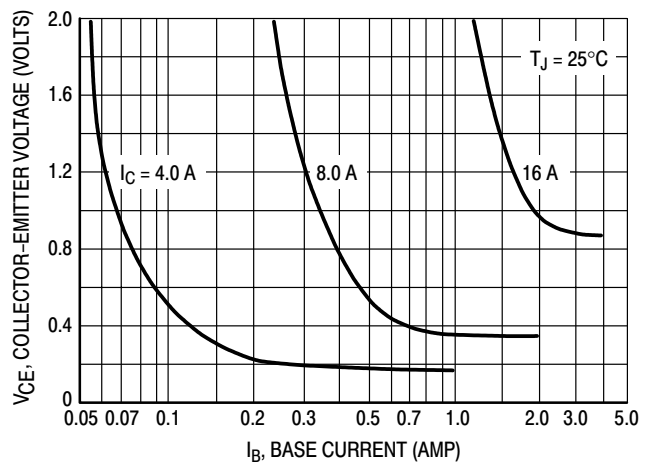
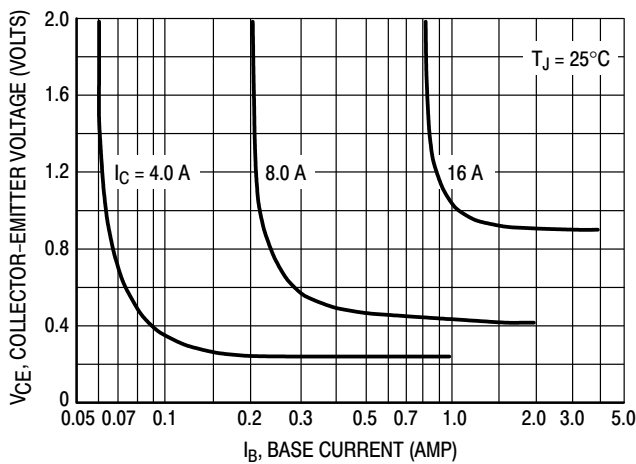


Figure 9. Collector Saturation Region



# Plastic NPN Silicon High-Voltage Power Transistor

... designed for use in line-operated equipment such as audio output amplifiers; low-current, high-voltage converters; and AC line relays.

- Excellent DC Current Gain –  $h_{FE} = 30-250 @ I_C = 100 \text{ mAdc}$
- Current-Gain – Bandwidth Product –  $f_T = 10 \text{ MHz (Min) @ } I_C = 50 \text{ mAdc}$

### MAXIMUM RATINGS (1)

Rating	Symbol	2N5655	2N5657	Unit
Collector-Emitter Voltage	$V_{CEO}$	250	350	Vdc
Collector-Base Voltage	$V_{CB}$	275	375	Vdc
Emitter-Base Voltage	$V_{EB}$	6.0		Vdc
Collector Current – Continuous Peak	$I_C$	0.5 1.0		Adc
Base Current	$I_B$	0.25		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150		$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	6.25	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

**2N5655  
2N5657**

**0.5 AMPERE  
POWER TRANSISTORS  
NPN SILICON  
250-350 VOLTS  
20 WATTS**

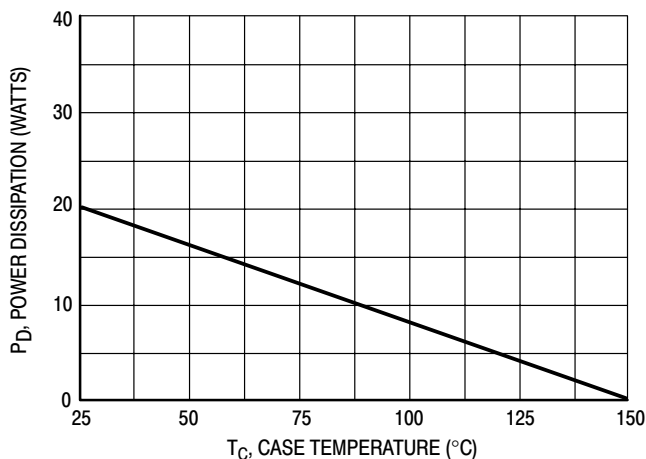
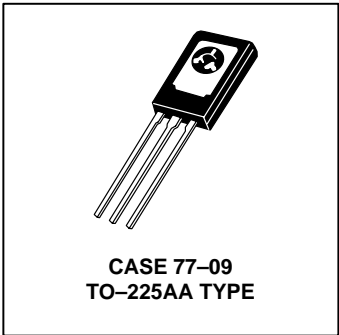


Figure 1. Power Derating

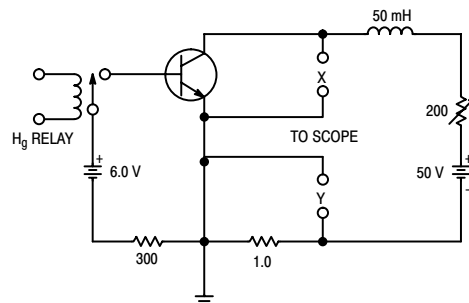


Figure 2. Sustaining Voltage Test Circuit

Safe Area Limits are indicated by Figures 3 and 4. Both limits are applicable and must be observed.

## 2N5655 2N5657

**\*ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mAdc}$ (inductive), $L = 50\text{ mH}$ )	2N5655 2N5657	$V_{CEO(sus)}$	250 350	– –	Vdc
Collector–Emitter Breakdown Voltage ( $I_C = 1.0\text{ mAdc}$ , $I_B = 0$ )	2N5655 2N5657	$V_{(BR)CEO}$	250 350	– –	Vdc
Collector Cutoff Current ( $V_{CE} = 150\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 250\text{ Vdc}$ , $I_B = 0$ )	2N5655 2N5657	$I_{CEO}$	– –	0.1 0.1	mAcd
Collector Cutoff Current ( $V_{CE} = 250\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 350\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 150\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 100^\circ\text{C}$ ) ( $V_{CE} = 250\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 100^\circ\text{C}$ )	2N5655 2N5657 2N5655 2N5657	$I_{CEX}$	– – – –	0.1 0.1 1.0 1.0	mAcd
Collector Cutoff Current ( $V_{CB} = 275\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 375\text{ Vdc}$ , $I_E = 0$ )	2N5655 2N5657	$I_{CBO}$	– –	10 10	$\mu\text{Acd}$
Emitter Cutoff Current ( $V_{EB} = 6.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	–	10	$\mu\text{Acd}$

### ON CHARACTERISTICS

DC Current Gain (1) ( $I_C = 50\text{ mAcd}$ , $V_{CE} = 10\text{ Vdc}$ ) ( $I_C = 100\text{ mAcd}$ , $V_{CE} = 10\text{ Vdc}$ ) ( $I_C = 250\text{ mAcd}$ , $V_{CE} = 10\text{ Vdc}$ ) ( $I_C = 500\text{ mAcd}$ , $V_{CE} = 10\text{ Vdc}$ )	$h_{FE}$	25 30 15 5.0	– 250 – –	–
Collector–Emitter Saturation Voltage (1) ( $I_C = 100\text{ mAcd}$ , $I_B = 10\text{ mAcd}$ ) ( $I_C = 250\text{ mAcd}$ , $I_B = 25\text{ mAcd}$ ) ( $I_C = 500\text{ mAcd}$ , $I_B = 100\text{ mAcd}$ )	$V_{CE(sat)}$	– – –	1.0 2.5 10	Vdc
Base–Emitter Voltage (1) ( $I_C = 100\text{ mAcd}$ , $V_{CE} = 10\text{ Vdc}$ )	$V_{BE}$	–	1.0	Vdc

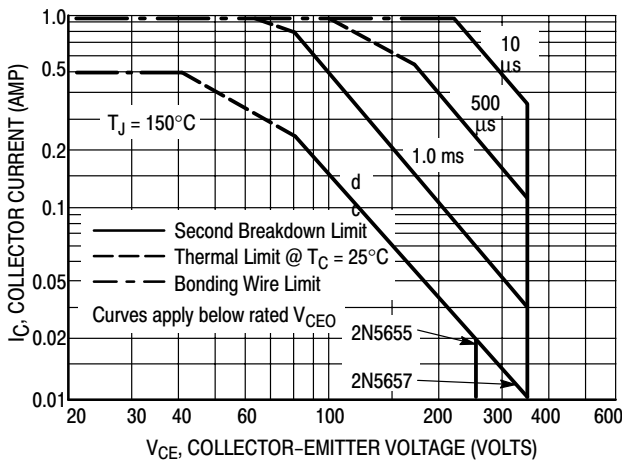
### DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product (2) ( $I_C = 50\text{ mAcd}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 10\text{ MHz}$ )	$f_T$	10	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 100\text{ kHz}$ )	$C_{ob}$	–	25	pF
Small–Signal Current Gain ( $I_C = 100\text{ mAcd}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	20	–	–

\*Indicates JEDEC Registered Data for 2N5655 Series.

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

(2)  $f_T$  is defined as the frequency at which  $|h_{fe}|$  extrapolates to unity.



**Figure 3. Active–Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# 2N5655 2N5657

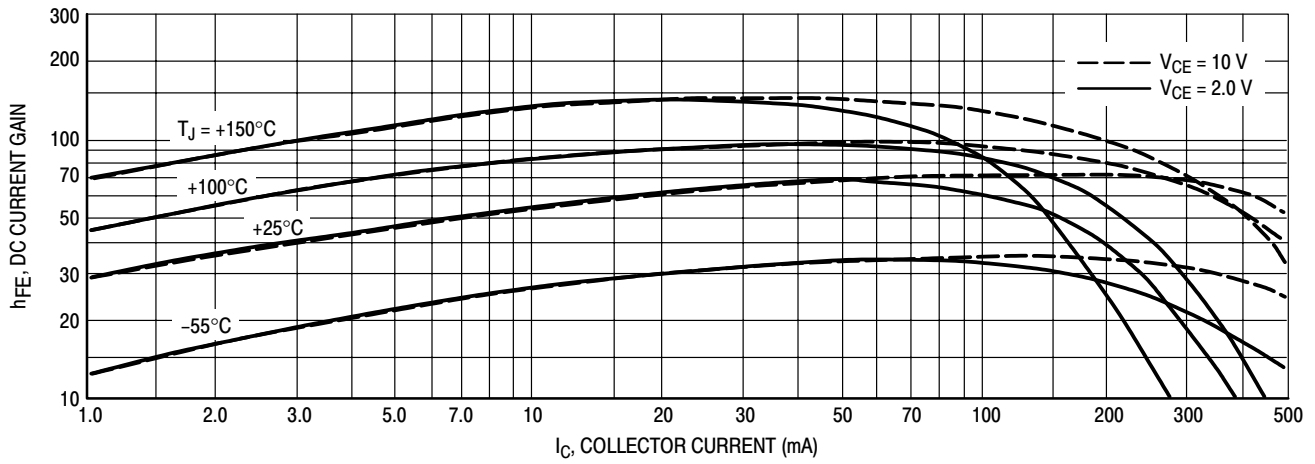


Figure 4. Current Gain

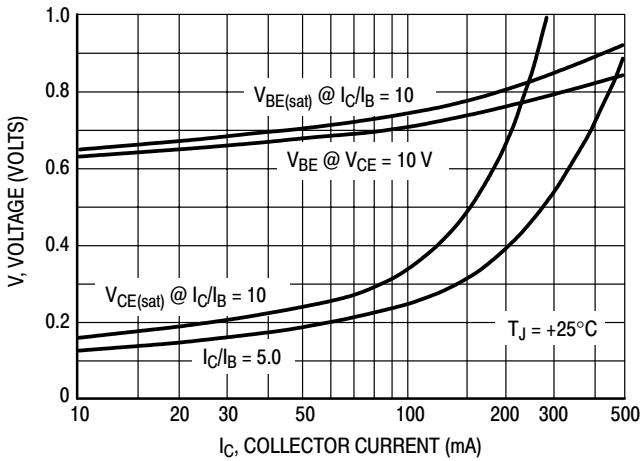


Figure 5. "On" Voltages

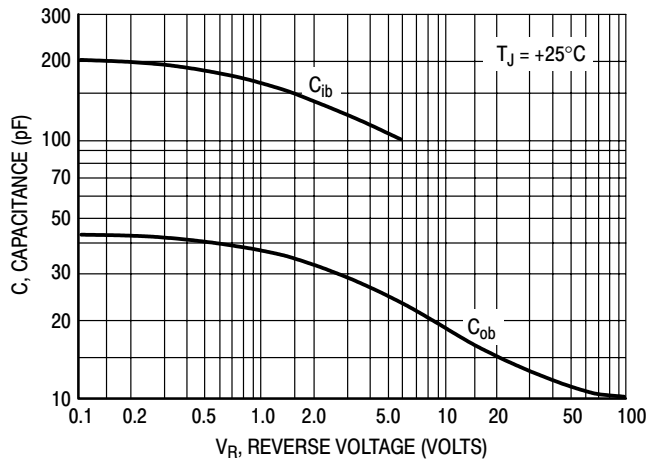


Figure 6. Capacitance

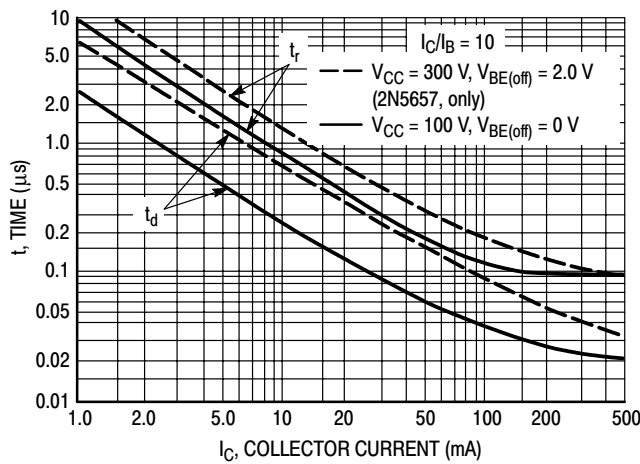


Figure 7. Turn-On Time

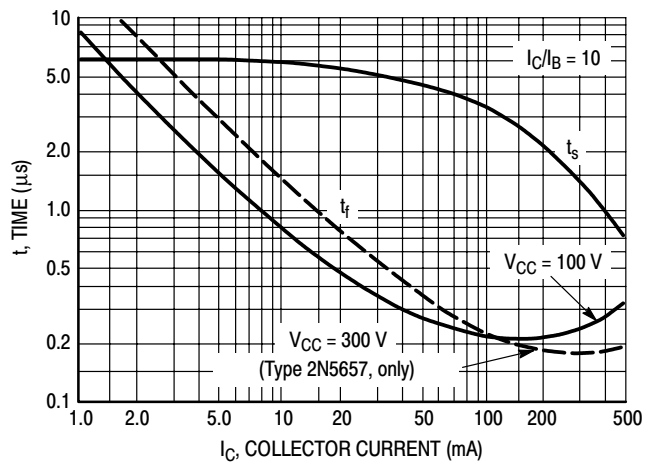


Figure 8. Turn-Off Time

# High-Current Complementary Silicon Power Transistors

... designed for use in high-power amplifier and switching circuit applications.

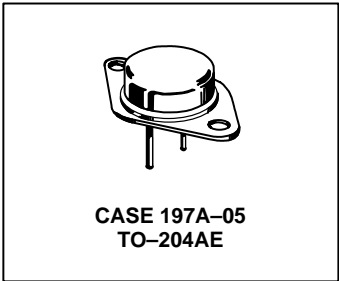
- High Current Capability –  
 $I_C$  Continuous = 50 Amperes.
- DC Current Gain –  
 $h_{FE} = 15-60 @ I_C = 25 \text{ A dc}$
- Low Collector-Emmitter Saturation Voltage –  
 $V_{CE(sat)} = 1.0 \text{ V dc (Max) @ } I_C = 25 \text{ A dc}$

**PNP  
2N5684  
NPN  
2N5686**

**50 AMPERE  
COMPLEMENTARY  
SILICON  
POWER TRANSISTORS  
60-80 VOLTS  
300 WATTS**

## MAXIMUM RATINGS (1)

Rating	Symbol	2N5684 2N5686	Unit
Collector-Emmitter Voltage	$V_{CEO}$	80	Vdc
Collector-Base Voltage	$V_{CB}$	80	Vdc
Emmitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current – Continuous	$I_C$	50	A dc
Base Current	$I_B$	15	A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 1.715	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$



## THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.584	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

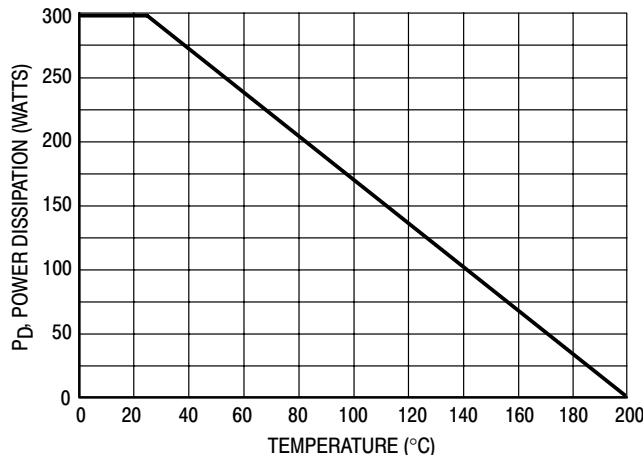


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

# 2N5684 2N5686

\*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

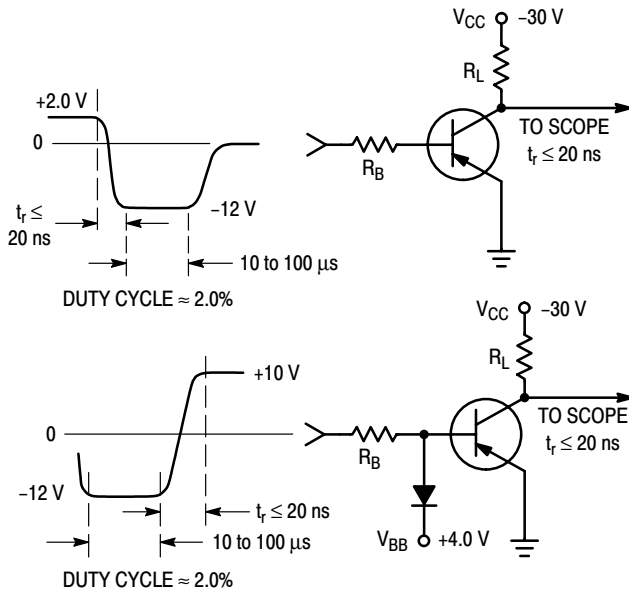
Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 2) ( $I_C = 0.2 \text{ Adc}$ , $I_B = 0$ )	$V_{CE(sus)}$	80	–	Vdc
Collector Cutoff Current ( $V_{CE} = 40 \text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	1.0	mAdc
Collector Cutoff Current ( $V_{CE} = 80 \text{ Vdc}$ , $V_{EB(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 80 \text{ Vdc}$ , $V_{EB(off)} = 1.5 \text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	–	2.0 10	mAdc
Collector Cutoff Current ( $V_{CB} = 80 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	2.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	5.0	mAdc

<b>ON CHARACTERISTICS</b>				
DC Current Gain (Note 2) ( $I_C = 25 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ ) ( $I_C = 50 \text{ Adc}$ , $V_{CE} = 5.0 \text{ Vdc}$ )	$h_{FE}$	15 5.0	60 –	–
Collector–Emitter Saturation Voltage (Note 2) ( $I_C = 25 \text{ Adc}$ , $I_B = 2.5 \text{ Adc}$ ) ( $I_C = 50 \text{ Adc}$ , $I_B = 10 \text{ Adc}$ )	$V_{CE(sat)}$	– –	1.0 5.0	Vdc
Base–Emitter Saturation Voltage (Note 1) ( $I_C = 25 \text{ Adc}$ , $I_B = 2.5 \text{ Adc}$ )	$V_{BE(sat)}$	–	2.0	Vdc
Base–Emitter On Voltage (Note 1) ( $I_C = 25 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ )	$V_{BE(on)}$	–	2.0	Vdc

<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain – Bandwidth Product ( $I_C = 5.0 \text{ Adc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	$f_T$	2.0	–	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 0.1 \text{ MHz}$ )	$C_{ob}$	–	2000 1200	pF
Small–Signal Current Gain ( $I_C = 10 \text{ Adc}$ , $V_{CE} = 5.0 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ )	$h_{fe}$	15	–	

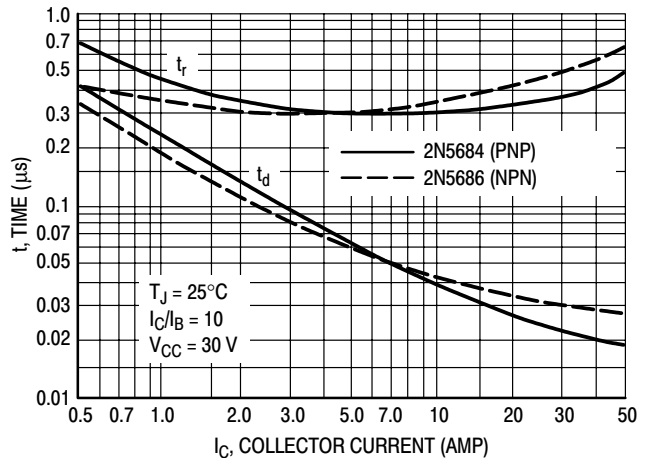
\*Indicates JEDEC Registered Data.

Note 2: Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



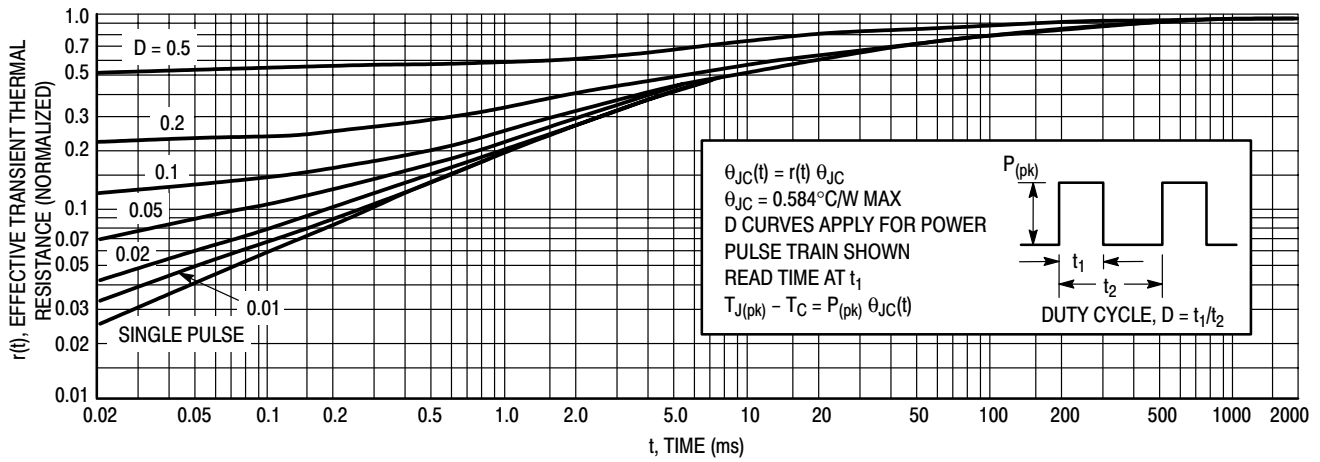
FOR CURVES OF FIGURES 3 & 6,  $R_B$  &  $R_L$  ARE VARIED.  
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.  
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

**Figure 2. Switching Time Test Circuit**

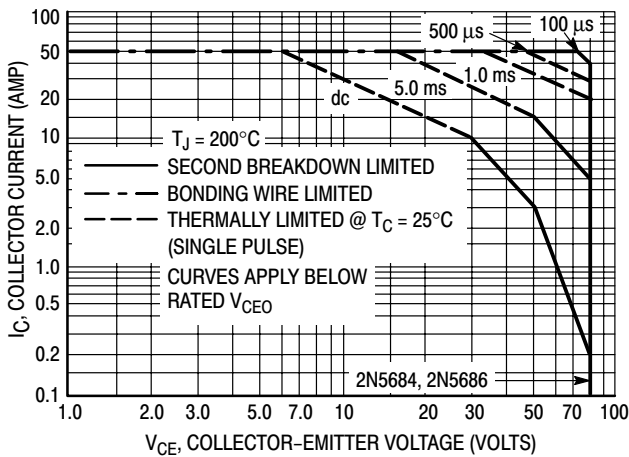


**Figure 3. Turn–On Time**

## 2N5684 2N5686



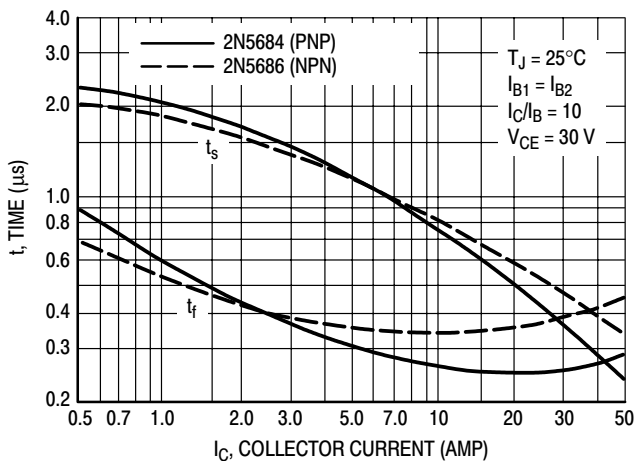
**Figure 4. Thermal Response**



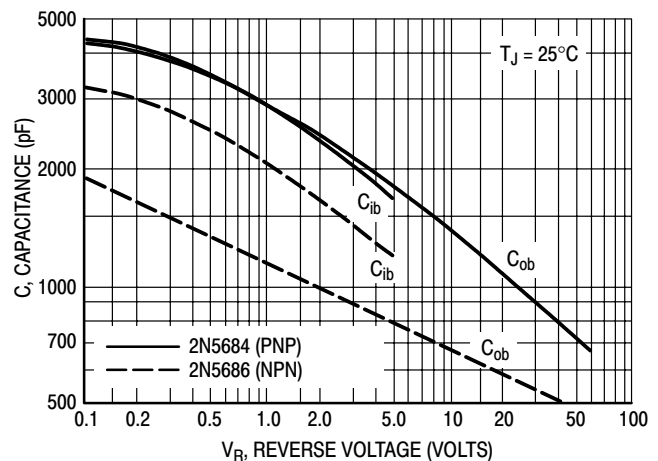
**Figure 5. Active-Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 200^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



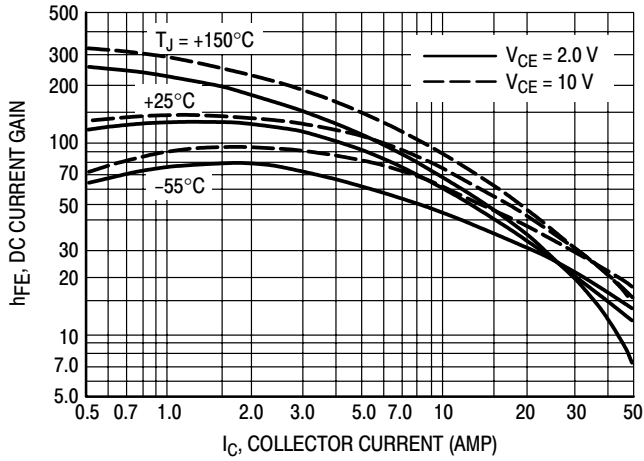
**Figure 6. Turn-Off Time**



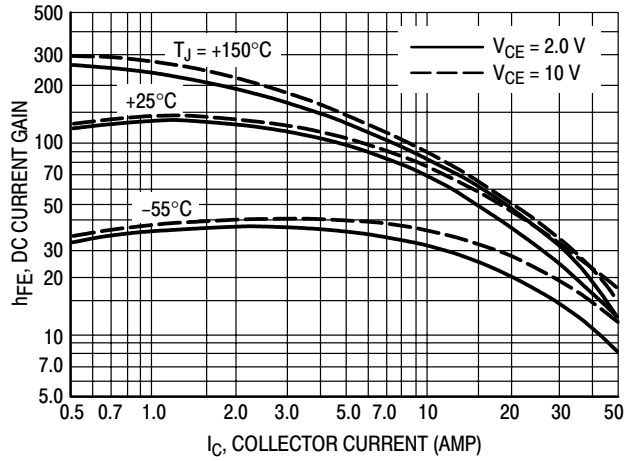
**Figure 7. Capacitance**

# 2N5684 2N5686

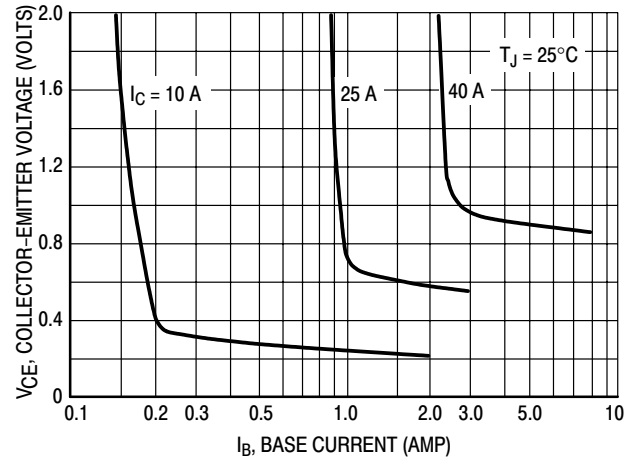
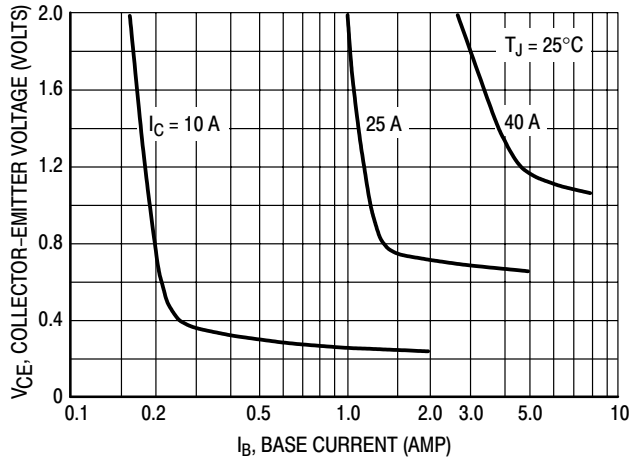
**PNP  
2N5684**



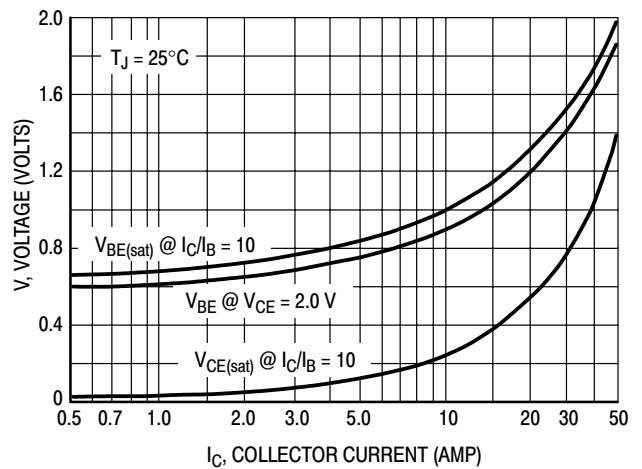
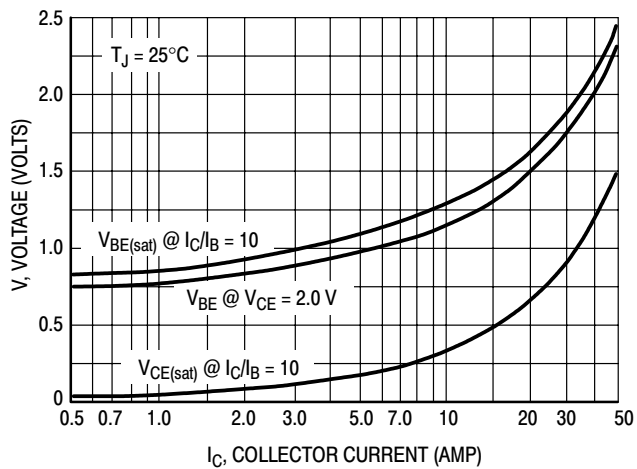
**NPN  
2N5686**



**Figure 8. DC Current Gain**



**Figure 9. Collector Saturation Region**



**Figure 10. "On" Voltages**

# Complementary Silicon High-Power Transistors

... designed for general-purpose power amplifier and switching applications.

- Low Collector–Emitter Saturation Voltage —  
 $V_{CE(sat)} = 1.0 \text{ Vdc}$ , (max) at  $I_C = 15 \text{ Adc}$
- Low Leakage Current  
 $I_{CEX} = 1.0 \text{ mA}$ dc (max) at Rated Voltage
- Excellent DC Current Gain —  
 $h_{FE} = 20$  (min) at  $I_C = 10 \text{ Adc}$
- High Current Gain Bandwidth Product —  
 $f_T = 4.0 \text{ MHz}$  (min) at  $I_C = 1.0 \text{ Adc}$

## MAXIMUM RATINGS (1)

Rating	Symbol	2N5883 2N5885	2N5884 2N5886	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	80	Vdc
Collector–Base Voltage	$V_{CB}$	60	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous Peak	$I_C$	25 50		Adc
Base Current	$I_B$	7.5		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.15		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +200		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.875	$^\circ\text{C/W}$

(1) Indicates JEDEC registered data. Units and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values most or exceed present JEDEC registered data.

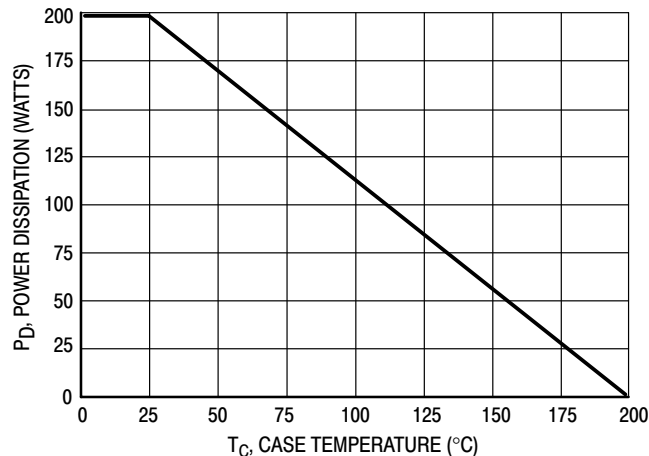


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**PNP**  
**2N5883**  
  
**2N5884\***  
**NPN**  
**2N5885**  
  
**2N5886\***

\*ON Semiconductor Preferred Device

**25 AMPERE**  
**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**60–80 VOLTS**  
**200 WATTS**

**CASE 1–07**  
**TO–204AA**  
**(TO–3)**



## 2N5883 2N5884 2N5885 2N5886

**\*ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (2) ( $I_C = 200\text{ mA}$ , $I_B = 0$ )	2N5883, 2N5885 2N5884, 2N5886	$V_{CE(sus)}$	60 80	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ )	2N5883, 2N5885 2N5884, 2N5886	$I_{CEO}$	— —	2.0 2.0	mAdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	2N5883, 2N5885 2N5884, 2N5886 2N5883, 2N5885 2N5884, 2N5886	$I_{CEX}$	— — — —	1.0 1.0 10 10	mAdc
Collector Cutoff Current ( $V_{CB} = 60\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ )	2N5883, 2N5885 2N5884, 2N5886	$I_{CBO}$	— —	1.0 1.0	mAdc
Emitter Cutoff Current ( $V_{EB} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	1.0	mAdc

### ON CHARACTERISTICS

DC Current Gain (2) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 10\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 25\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )		$h_{FE}$	35 20 4.0	— 100	—
Collector–Emitter Saturation Voltage (2) ( $I_C = 15\text{ Adc}$ , $I_B = 1.5\text{ Adc}$ ) ( $I_C = 25\text{ Adc}$ , $I_B = 6.25\text{ Adc}$ )		$V_{CE(sat)}$	— —	1.0 4.0	Vdc
Base–Emitter Saturation Voltage (2) ( $I_C = 25\text{ Adc}$ , $I_B = 6.25\text{ Adc}$ )		$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (2) ( $I_C = 10\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )		$V_{BE(on)}$	—	1.5	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product (3) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )		$f_T$	4.0	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	2N5883, 2N5884 2N5885, 2N5886	$C_{ob}$	— —	1000 500	pF
Small–Signal Current Gain ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f_{test} = 1.0\text{ kHz}$ )		$h_{fe}$	20	—	—

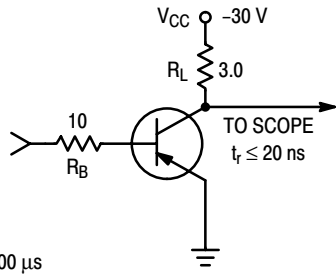
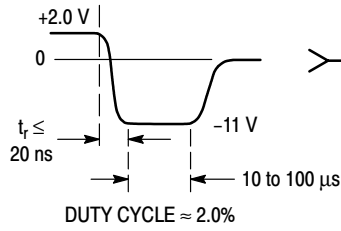
### SWITCHING CHARACTERISTICS

Rise Time	$(V_{CC} = 30\text{ Vdc}$ , $I_C = 10\text{ Adc}$ , $I_{B1} = I_{B2} = 1.0\text{ Adc}$ )	$t_r$	—	0.7	$\mu\text{s}$
Storage Time		$t_s$	—	1.0	$\mu\text{s}$
Fall Time		$t_f$	—	0.8	$\mu\text{s}$

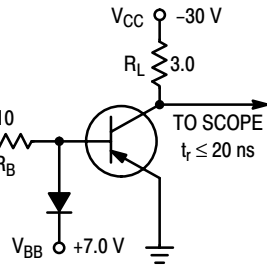
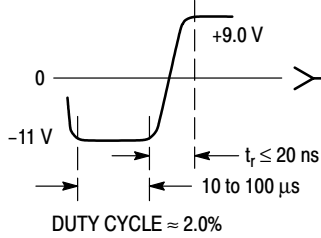
\*Indicates JEDEC Registered Data.

(2) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ . (3)  $f_T = |h_{fe}| \cdot f_{test}$ .

**TURN-ON TIME**

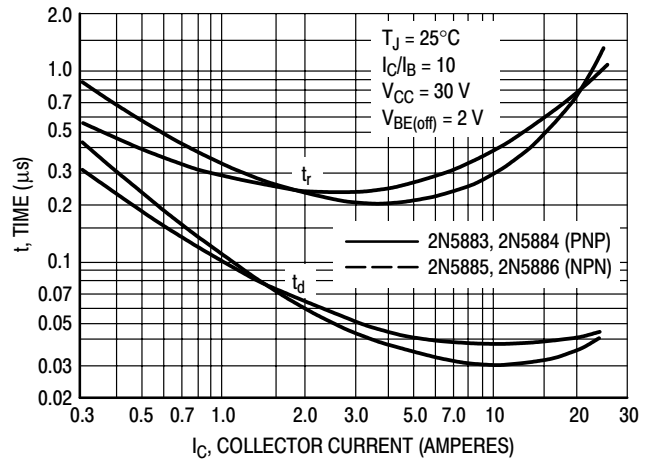


**TURN-OFF TIME**



FOR CURVES OF FIGURES 3 & 6,  $R_B$  &  $R_L$  ARE VARIED.  
 INPUT LEVELS ARE APPROXIMATELY AS SHOWN.  
 FOR NPN, REVERSE ALL POLARITIES.

**Figure 2. Switching Time Equivalent Test Circuits**



**Figure 3. Turn-On Time**

2N5883 2N5884 2N5885 2N5886

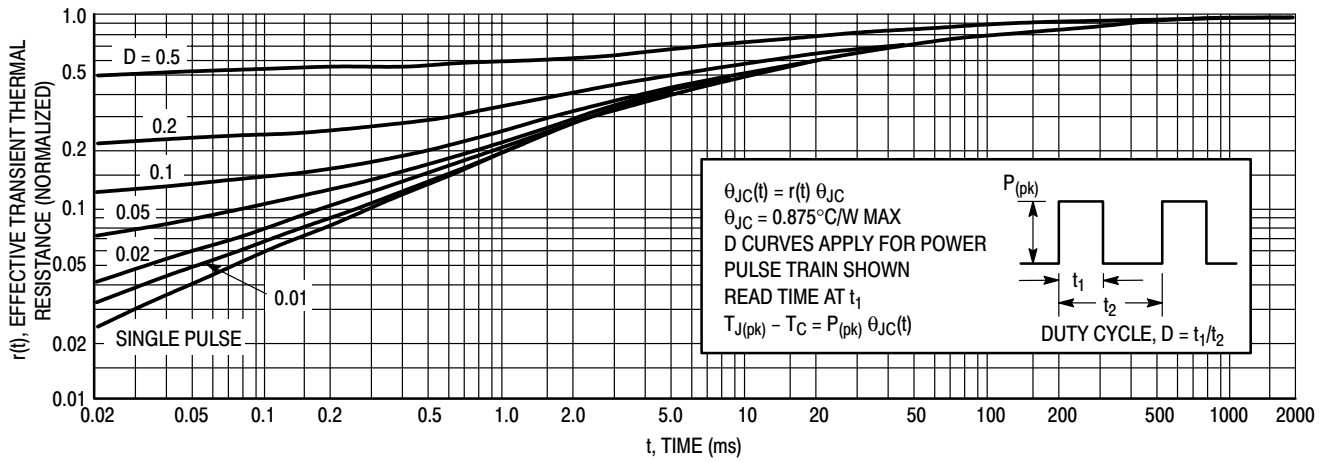


Figure 4. Thermal Response

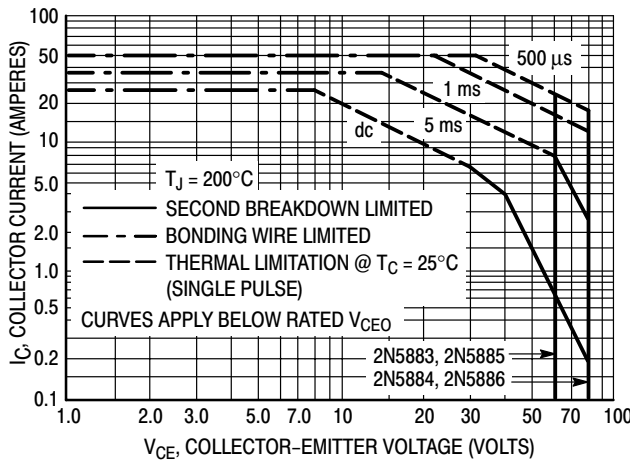


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

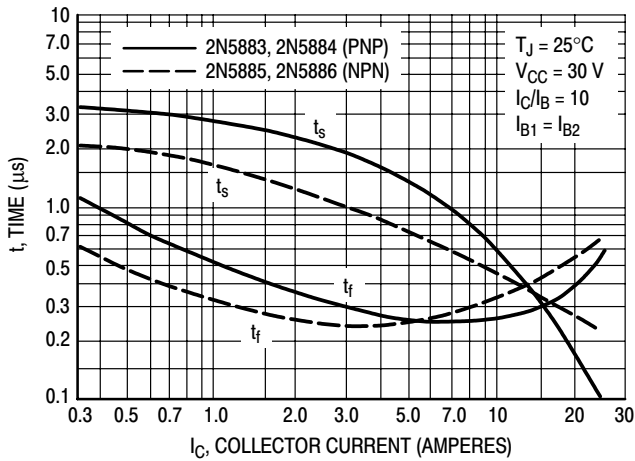


Figure 6. Turn-Off Time

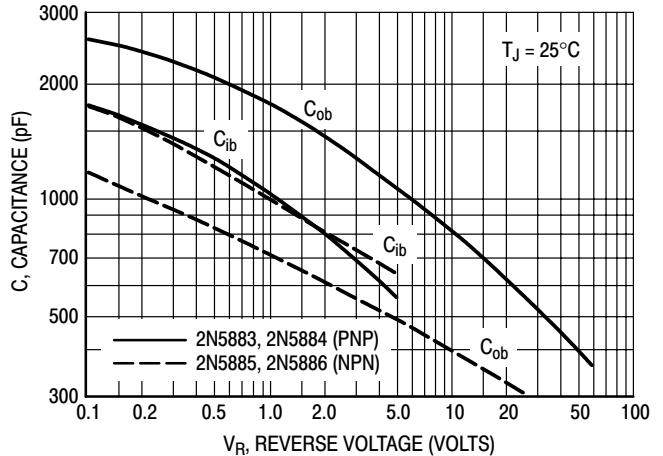
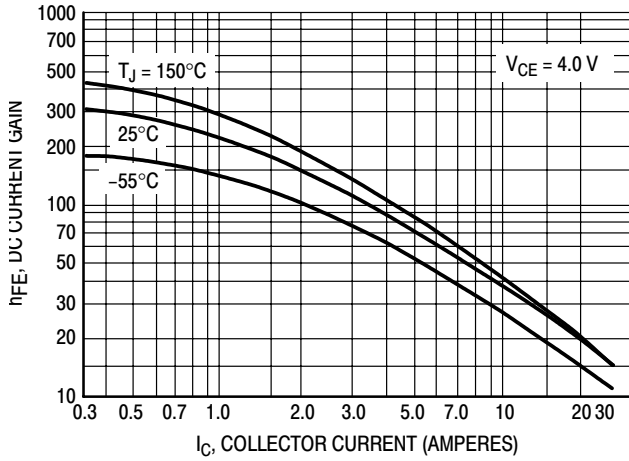


Figure 7. Capacitance

**PNP DEVICES**  
2N5883 and 2N5884



**NPN DEVICES**  
2N5885 and 2N5886

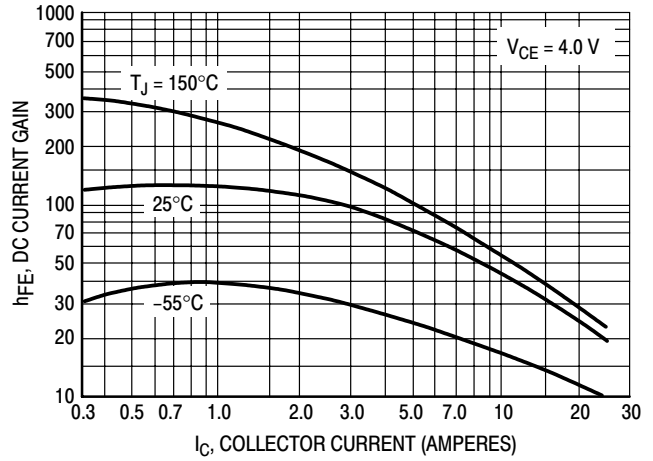


Figure 8. DC Current Gain

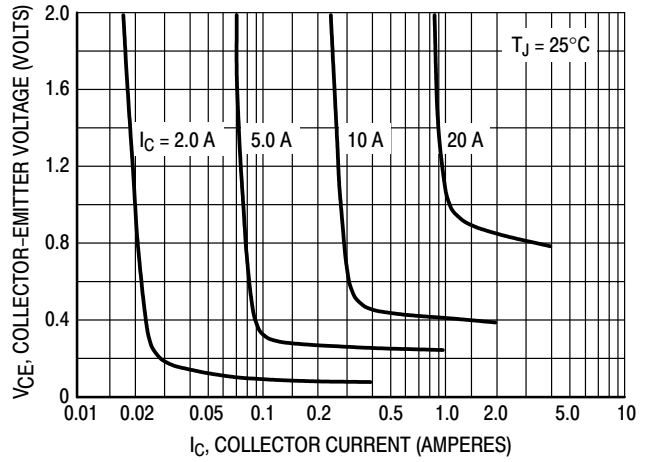
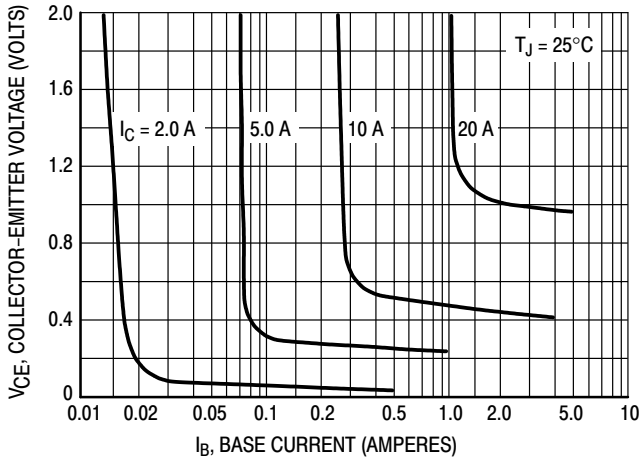


Figure 9. Collector Saturation Region

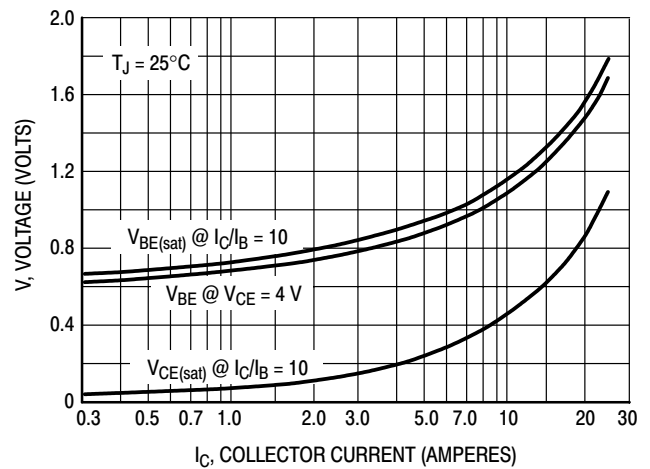
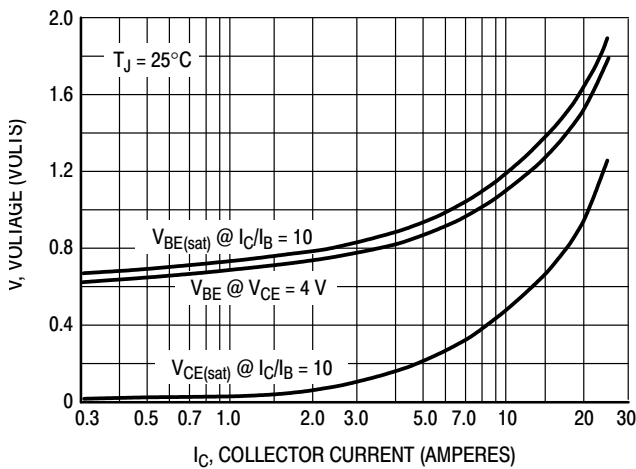


Figure 10. "On" Voltages

# Plastic Darlington Complementary Silicon Power Transistors

...designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —  
 $h_{FE} = 2000$  (Typ) @  $I_C = 2.0$  Adc
- Collector–Emitter Sustaining Voltage — @ 100 mA dc  
 $V_{CEO(sus)} = 60$  Vdc (Min) — 2N6035, 2N6038 = 80 Vdc (Min) — 2N6036, 2N6039
- Forward Biased Second Breakdown Current Capability  
 $I_{S/b} = 1.5$  Adc @ 25 Vdc
- Monolithic Construction with Built–In Base–Emitter Resistors to Limit Leakage Multiplication
- Space–Saving High Performance–to–Cost Ratio TO–225AA Plastic Package

## MAXIMUM RATINGS (1)

Rating	Symbol	2N6035 2N6038	2N6036 2N6039	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	80	Vdc
Collector–Base Voltage	$V_{CB}$	60	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous Peak	$I_C$	4.0 8.0		A dc
Base Current	$I_B$	100		mA dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.32		Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.5 0.012		Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

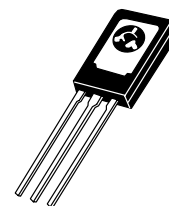
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	3.12	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	83.3	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

PNP  
**2N6035**  
**2N6036\***  
NPN  
**2N6038**  
**2N6039\***

\*ON Semiconductor Preferred Device

DARLINGTON  
4-AMPERE  
COMPLEMENTARY  
SILICON  
POWER TRANSISTORS  
60, 80 VOLTS  
40 WATTS



CASE 77–09  
TO–225AA TYPE

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

2N6035 2N6036 2N6038 2N6039

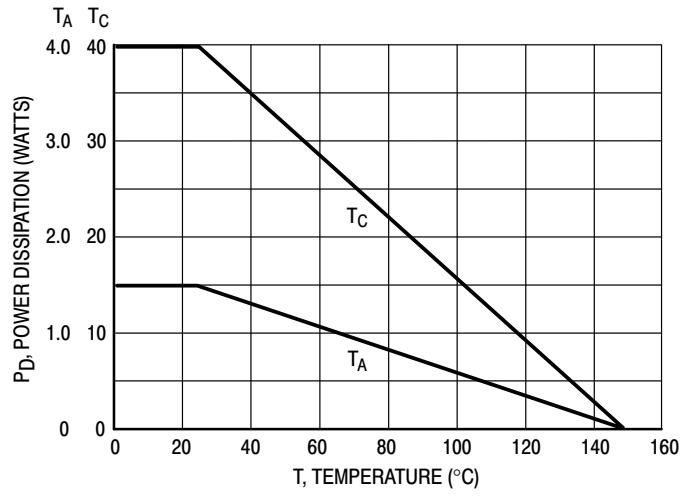


Figure 1. Power Derating

## 2N6035 2N6036 2N6038 2N6039

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector–Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 80\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— —	100 100	$\mu\text{A}$
Collector–Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$	— — — —	100 100 500 500	$\mu\text{A}$
Collector–Cutoff Current ( $V_{CB} = 60\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	— —	0.5 0.5	mAdc
Emitter–Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	2.0	mAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	$h_{FE}$	500 750 100	— 15,000 —	—
Collector–Emitter Saturation Voltage ( $I_C = 2.0\text{ Adc}$ , $I_B = 8.0\text{ mAdc}$ ) ( $I_C = 4.0\text{ Adc}$ , $I_B = 40\text{ mAdc}$ )	$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 4.0\text{ Adc}$ , $I_B = 40\text{ mAdc}$ )	$V_{BE(sat)}$	—	4.0	Vdc
Base–Emitter On Voltage ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	$V_{BE(on)}$	—	2.8	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Small–Signal Current–Gain ( $I_C = 0.75\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$ h_{fe} $	25	—	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	— —	200 100	pF

\*Indicates JEDEC Registered Data.

2N6035 2N6036 2N6038 2N6039

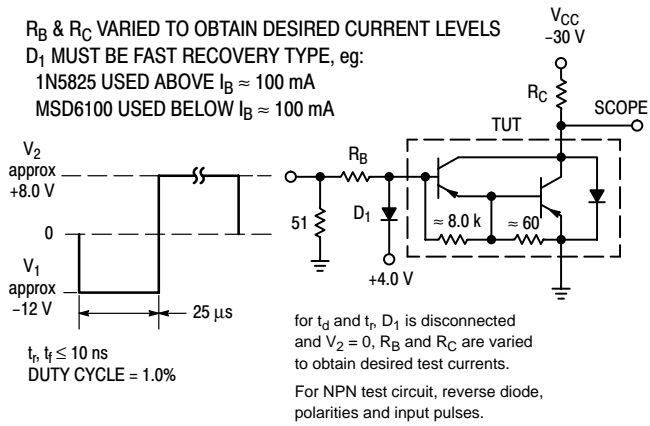


Figure 2. Switching Times Test Circuit

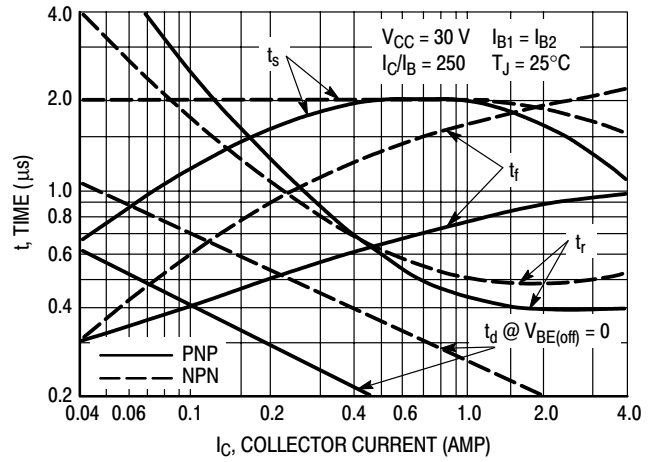


Figure 3. Switching Times

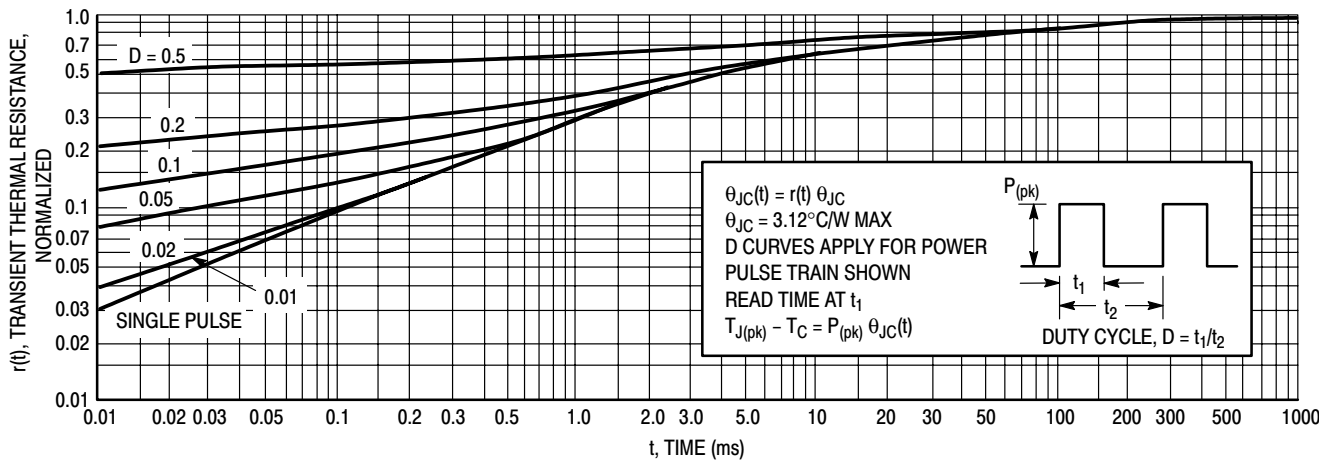


Figure 4. Thermal Response



ACTIVE-REGION SAFE-OPERATING AREA

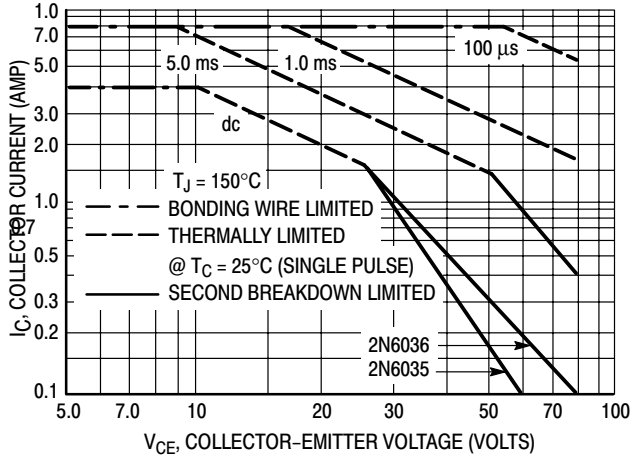


Figure 5. 2N6035, 2N6036

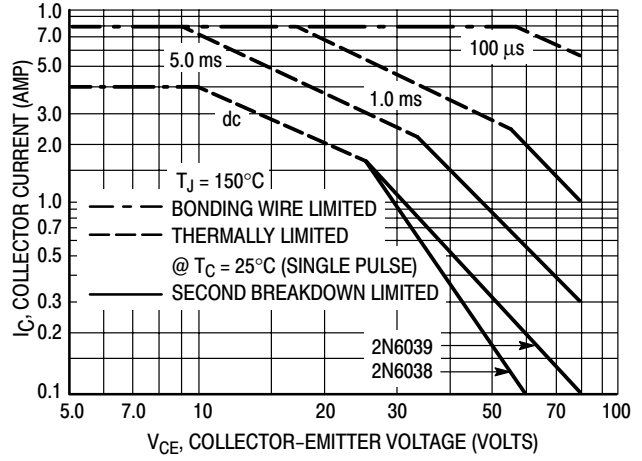


Figure 6. 2N6038, 2N6039

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

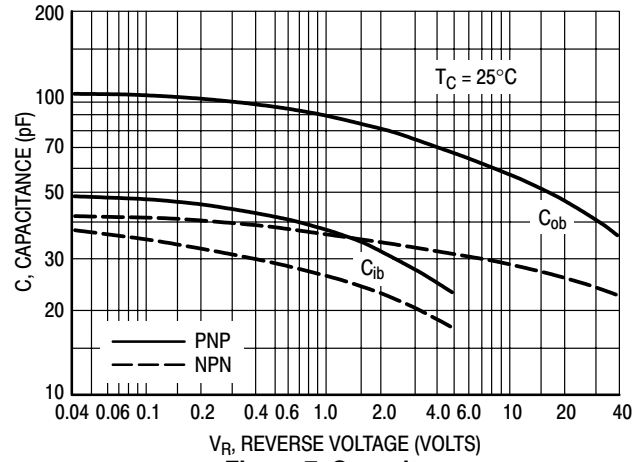


Figure 7. Capacitance

2N6035 2N6036 2N6038 2N6039

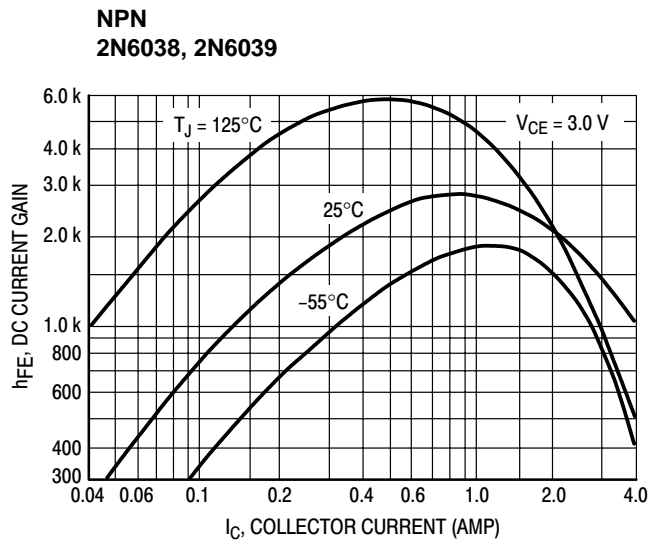
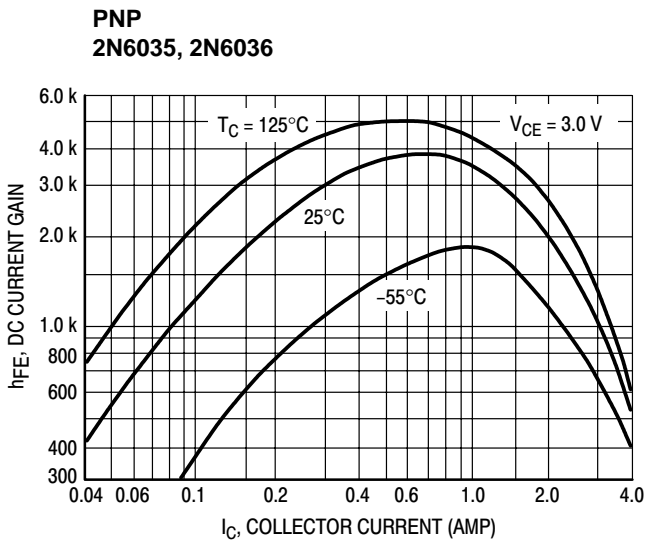


Figure 8. DC Current Gain

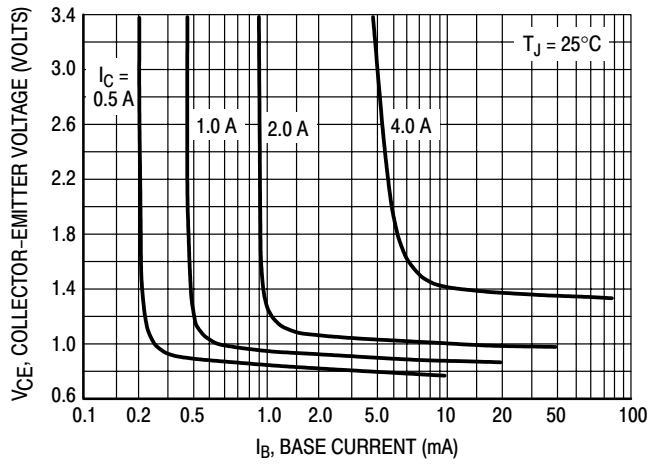
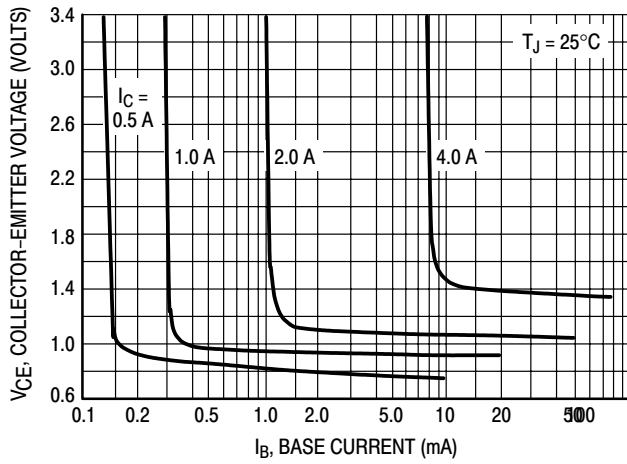


Figure 9. Collector Saturation Region

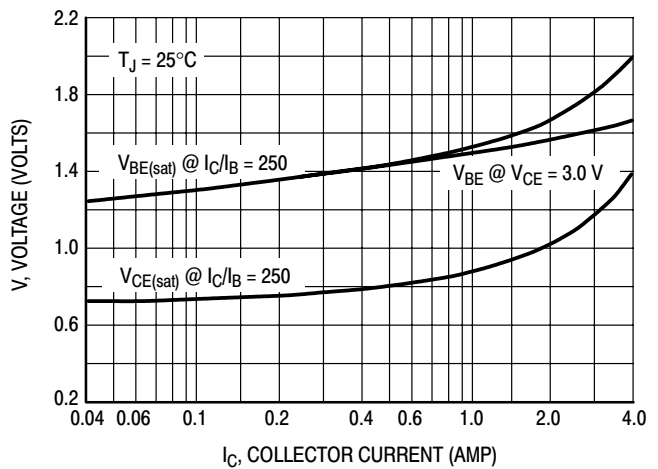
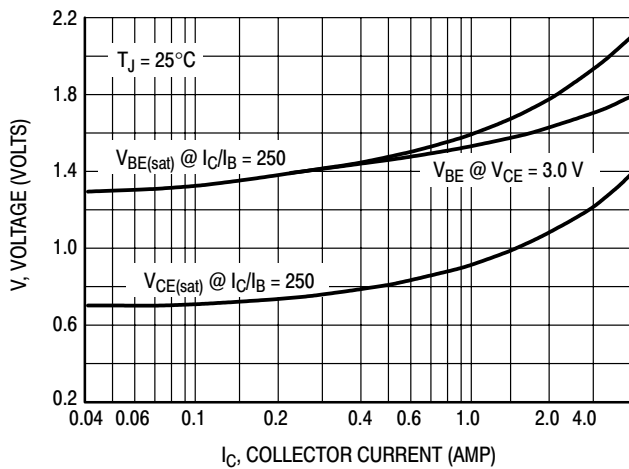


Figure 10. "On" Voltages

# Plastic Medium-Power Complementary Silicon Transistors

...designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –  
 $h_{FE} = 2500$  (Typ) @  $I_C = 4.0$  Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc –  
 $V_{CE(sus)} = 60$  Vdc (Min) – 2N6040, 2N6043  
 $= 100$  Vdc (Min) – 2N6042, 2N6045
- Low Collector-Emitter Saturation Voltage –  
 $V_{CE(sat)} = 2.0$  Vdc (Max) @  $I_C = 4.0$  Adc – 2N6043,44  
 $= 2.0$  Vdc (Max) @  $I_C = 3.0$  Adc – 2N6042, 2N6045
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

## MAXIMUM RATINGS (1)

Rating	Symbol	2N6040 2N6043	2N6042 2N6045	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	100	Vdc
Collector-Base Voltage	$V_{CB}$	60	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current – Continuous Peak	$I_C$	8.0 16		Adc
Base Current	$I_B$	120		mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	75 0.60		Watts W/ $^\circ\text{C}$
Operating and Storage Junction, Temperature Range	$T_J, T_{stg}$	-65 to +150		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	1.67	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	57	$^\circ\text{C}/\text{W}$

(1) Indicates JEDEC Registered Data.

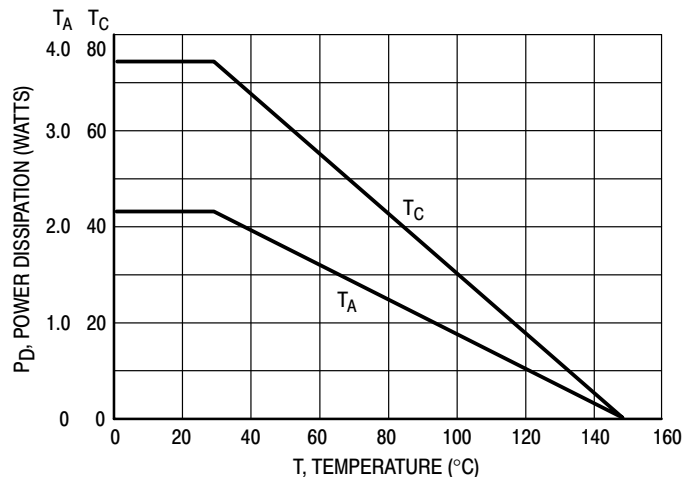


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**PNP**  
**2N6040**  
**2N6042**  
**2N6043\***  
**NPN**  
**2N6045\***

\*ON Semiconductor Preferred Device

**DARLINGTON**  
**8 AMPERE**  
**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**60-100 VOLTS**  
**75 WATTS**

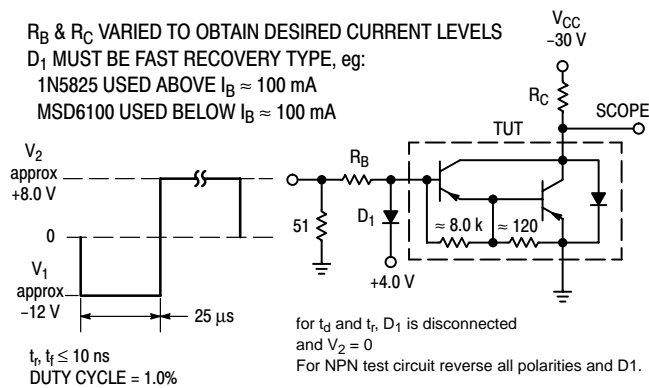
**CASE 221A-09**  
**TO-220AB**

# 2N6040 2N6042 2N6043 2N6045

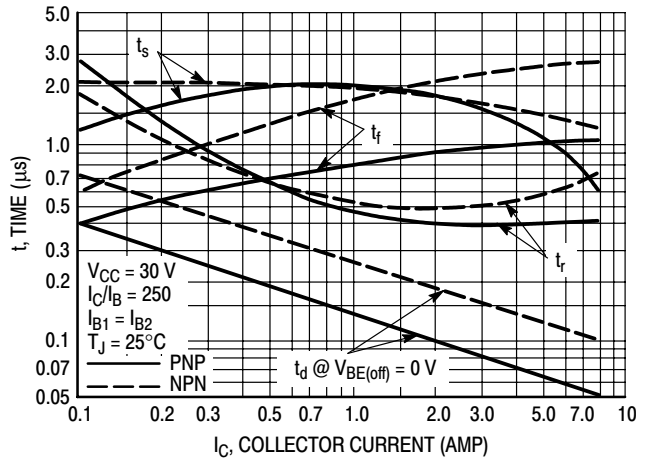
**\*ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Sustaining Voltage ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	60 100	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 100\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— —	20 20	$\mu\text{A}$
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 100\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) ( $V_{CE} = 100\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	— — — — —	20 20 200 200 200	$\mu\text{A}$
Collector Cutoff Current ( $V_{CB} = 60\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	20	$\mu\text{A}$
( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )		—	20	
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	2.0	mAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 8.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	1000 1000 100	20,000 20,000 —	—
Collector-Emitter Saturation Voltage ( $I_C = 4.0\text{ Adc}$ , $I_B = 16\text{ mAdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $I_B = 12\text{ mAdc}$ ) ( $I_C = 8.0\text{ Adc}$ , $I_B = 80\text{ Adc}$ )	$V_{CE(sat)}$	— — —	2.0 2.0 4.0	Vdc
Base-Emitter Saturation Voltage ( $I_C = 8.0\text{ Adc}$ , $I_B = 80\text{ mAdc}$ )	$V_{BE(sat)}$	—	4.5	Vdc
Base-Emitter On Voltage ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	2.8	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Small Signal Current Gain ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$ h_{fe} $	4.0	—	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	—	300 200	pF
Small-Signal Current Gain ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	300	—	—

\*Indicates JEDEC Registered Data.



**Figure 2. Switching Times Equivalent Circuit**



**Figure 3. Switching Times**

2N6040 2N6042 2N6043 2N6045

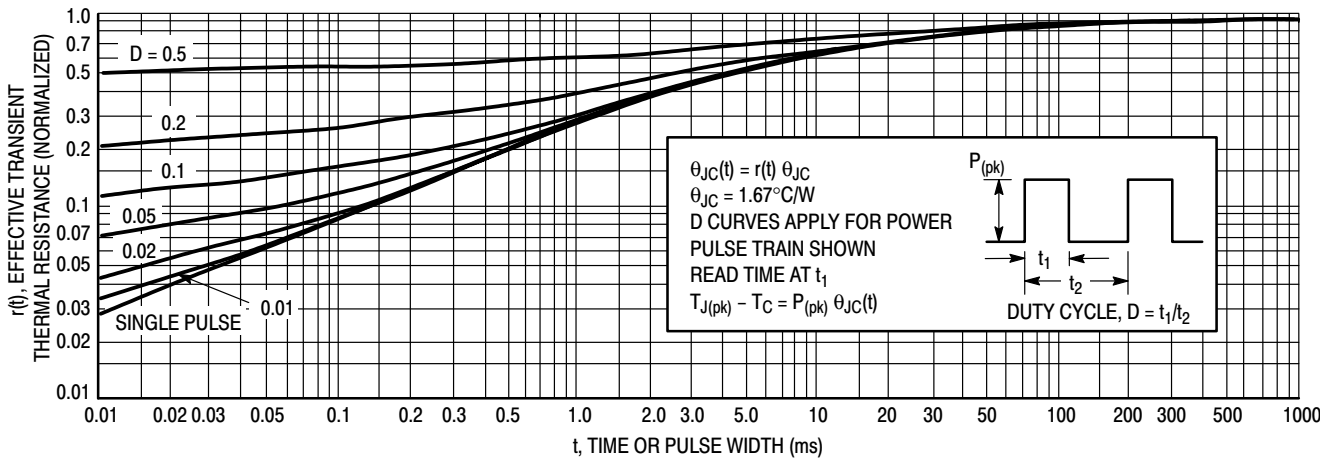


Figure 4. Thermal Response

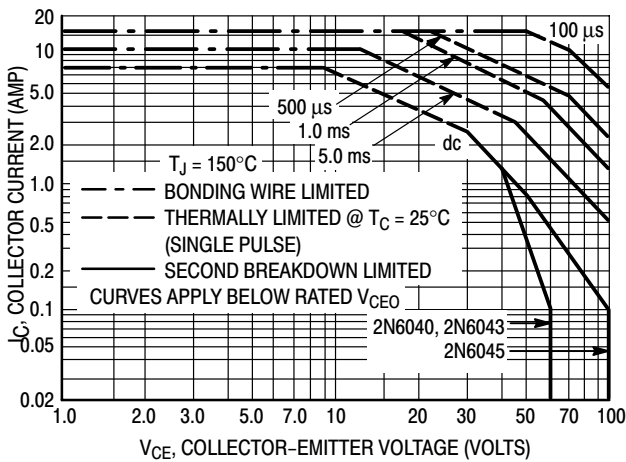


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

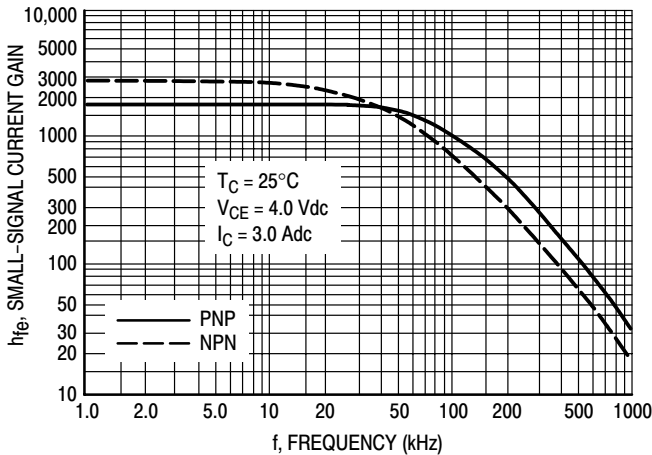


Figure 6. Small-Signal Current Gain

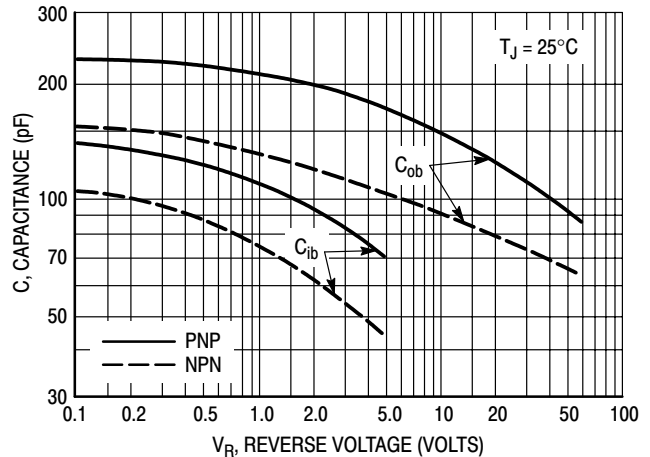


Figure 7. Capacitance

2N6040 2N6042 2N6043 2N6045

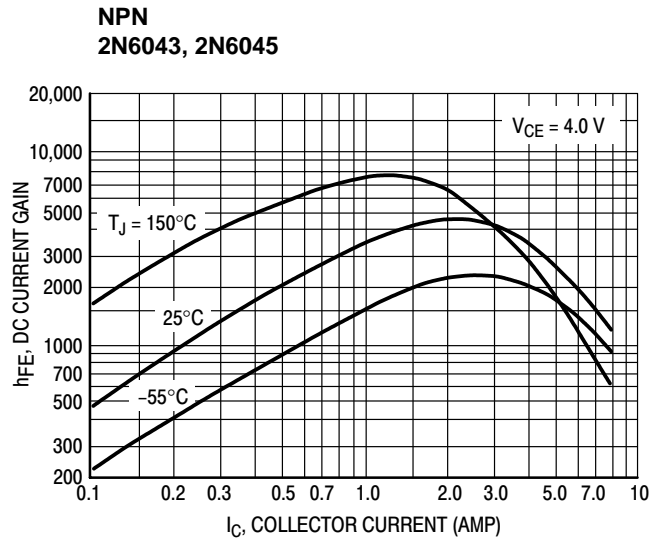
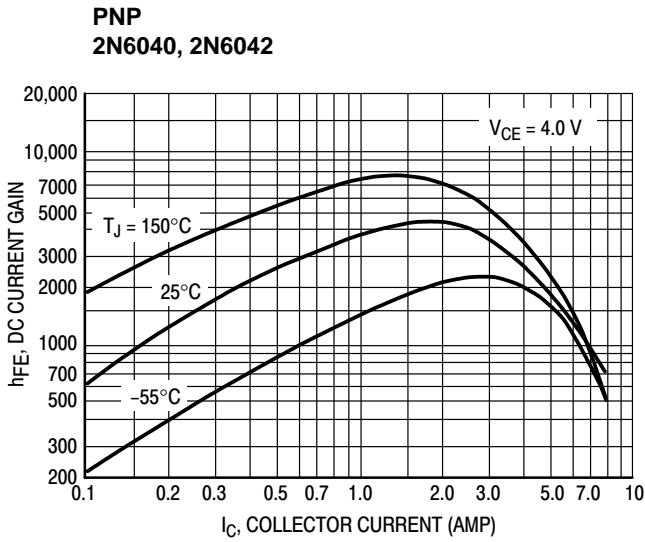


Figure 8. DC Current Gain

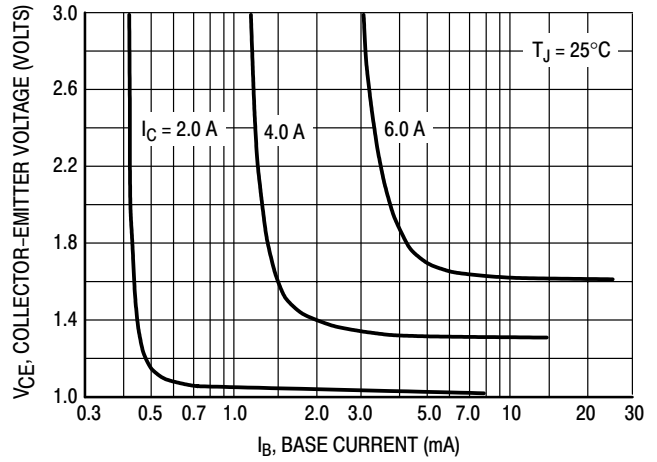
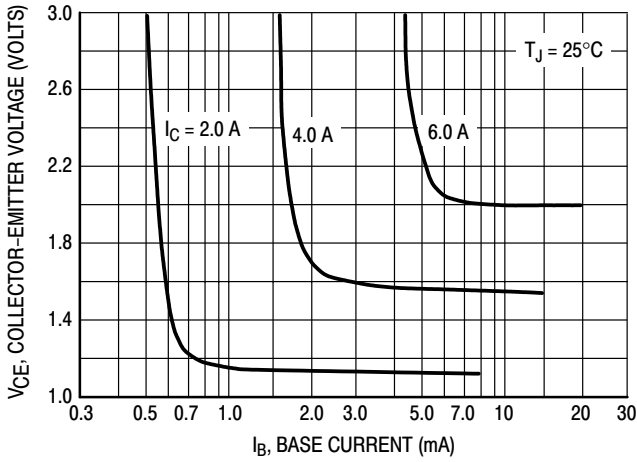


Figure 9. Collector Saturation Region

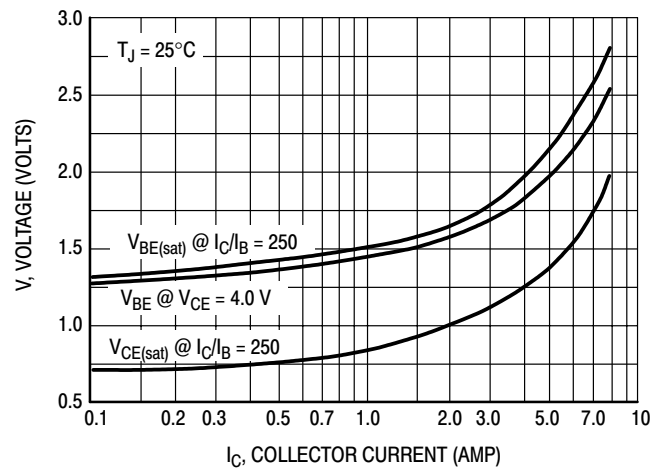
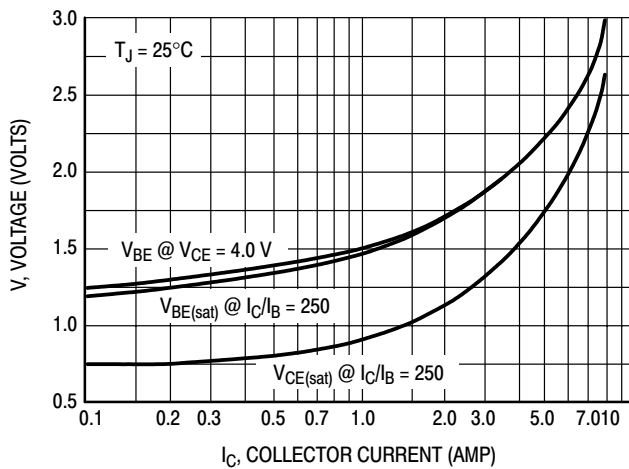


Figure 10. "On" Voltages

# Darlington Complementary Silicon Power Transistors

... designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain —  
 $h_{FE} = 3500$  (Typ) @  $I_C = 5.0$  Adc
- Collector–Emitter Sustaining Voltage — @ 100 mA  
 $V_{CEO(sus)} = 80$  Vdc (Min) — 2N6058  
 100 Vdc (Min) — 2N6052, 2N6059
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

## MAXIMUM RATINGS (1)

Rating	Symbol	2N6058	2N6052 2N6059	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	100	Vdc
Collector–Base Voltage	$V_{CB}$	80	100	Vdc
Emitter–Base voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous Peak	$I_C$	12 20		Adc
Base Current	$I_B$	0.2		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	150	0.857	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +200 $^\circ\text{C}$		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Rating	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

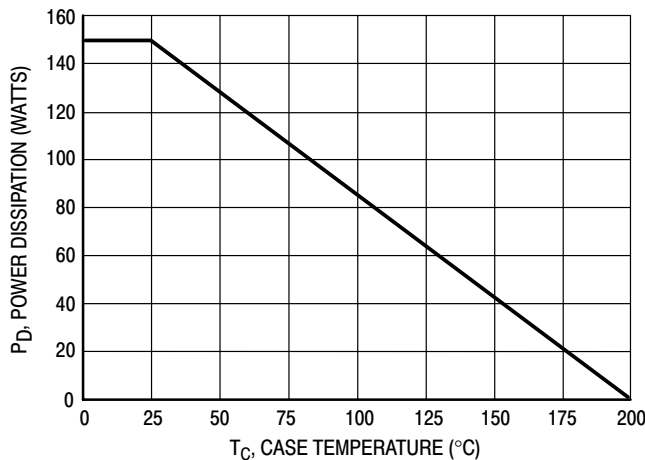


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**PNP**  
**2N6052\***  
**NPN**  
**2N6058**  
**2N6059\***

\*ON Semiconductor Preferred Device

**DARLINGTON**  
**12 AMPERE**  
**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**80–100 VOLTS**  
**150 WATTS**

**CASE 1–07**  
**TO–204AA**  
**(TO–3)**

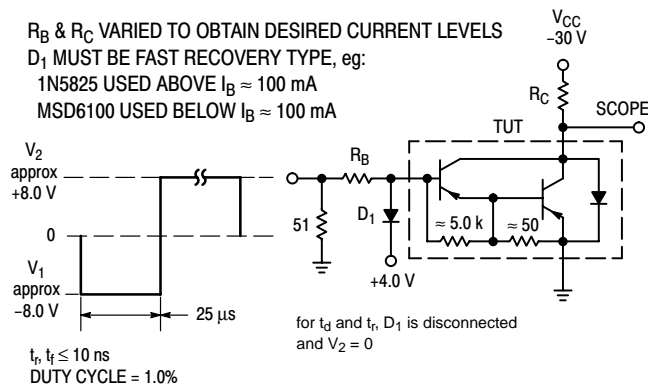
# 2N6052

\*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (2) ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	80 100	—	Vdc
	2N6058 2N6052, 2N6059			
Collector Cutoff Current ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	1.0 1.0	mAdc
	2N6058 2N6052, 2N6059			
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	—	0.5 5.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	2.0	mAdc
<b>ON CHARACTERISTICS (2)</b>				
DC Current Gain ( $I_C = 6.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 12\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	$h_{FE}$	750 100	18,000 —	—
Collector–Emitter Saturation Voltage ( $I_C = 6.0\text{ Adc}$ , $I_B = 24\text{ mAdc}$ ) ( $I_C = 12\text{ Adc}$ , $I_B = 120\text{ mAdc}$ )	$V_{CE(sat)}$	—	2.0 3.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 12\text{ Adc}$ , $I_B = 120\text{ mAdc}$ )	$V_{BE(sat)}$	—	4.0	Vdc
Base–Emitter On Voltage ( $I_C = 6.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	$V_{BE(on)}$	—	2.8	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Magnitude of Common Emitter Small–Signal Short Circuit Forward Current Transfer Ratio ( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$ h_{fe} $	4.0	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	—	500 300	pF
	2N6052 2N6058/2N6059			
Small–Signal Current Gain ( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	300	—	—

\*Indicates JEDEC Registered Data.

(2) Pulse test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

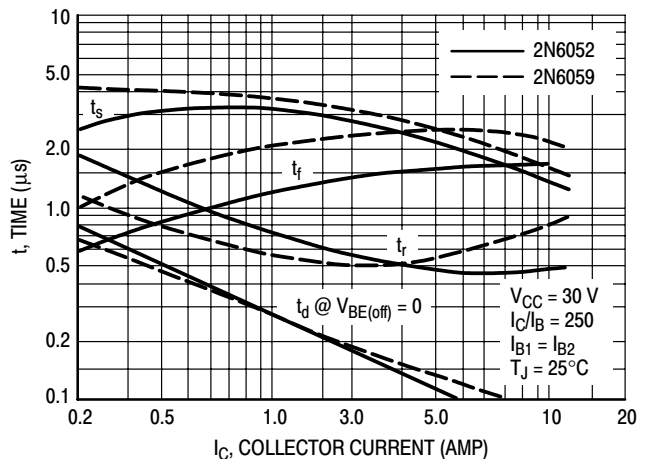
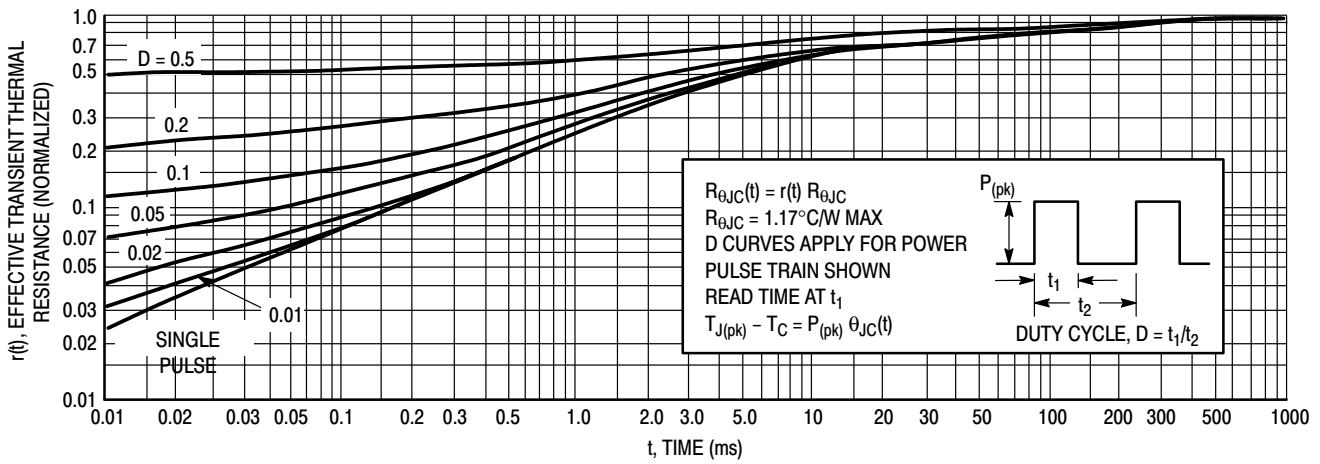


Figure 3. Switching Times

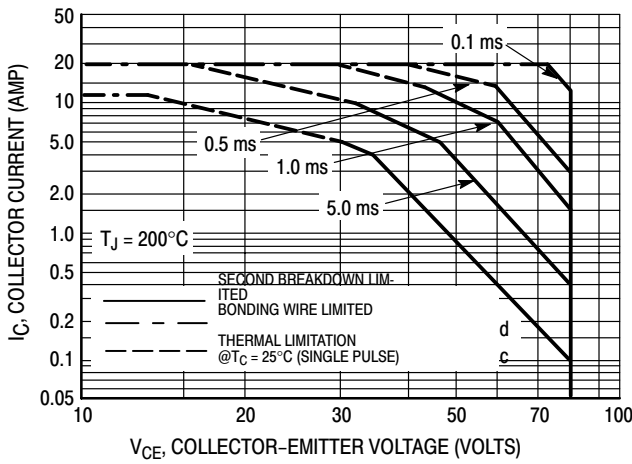


## 2N6052

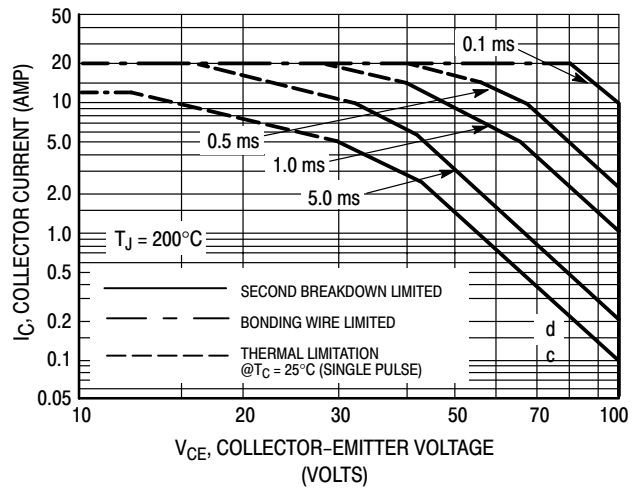


**Figure 4. Thermal Response**

### ACTIVE-REGION SAFE OPERATING AREA



**Figure 5. 2N6058**



**Figure 6. 2N6052, 2N6059**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6, and 7 is based on  $T_{J(pk)} = 200^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown

pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^{\circ}\text{C}$ ;  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# 2N6052

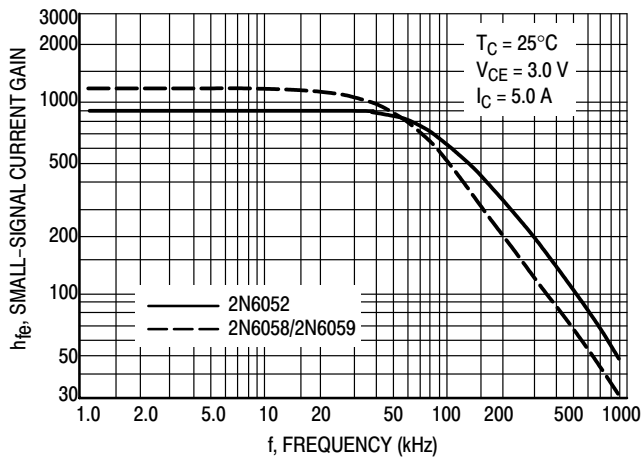


Figure 7. Small-Signal Current Gain

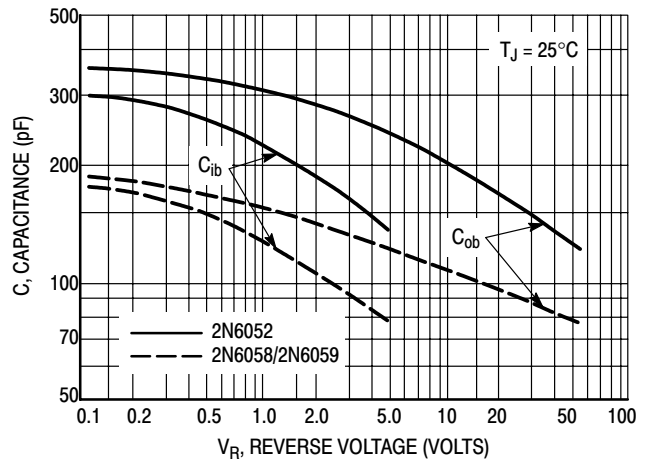


Figure 8. Capacitance

# 2N6052

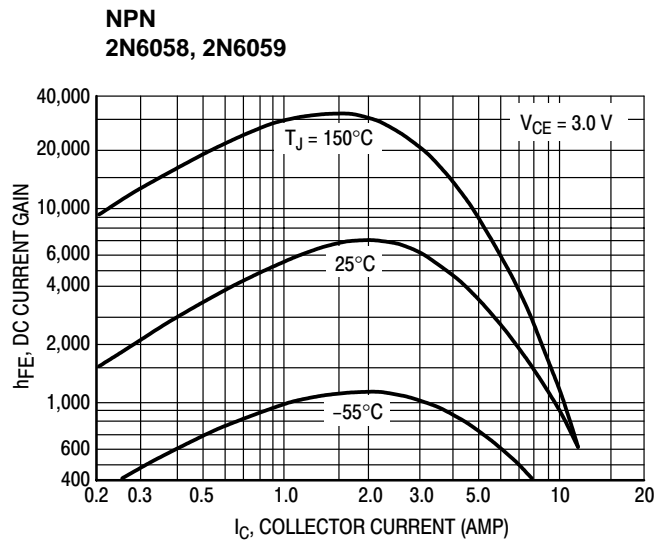
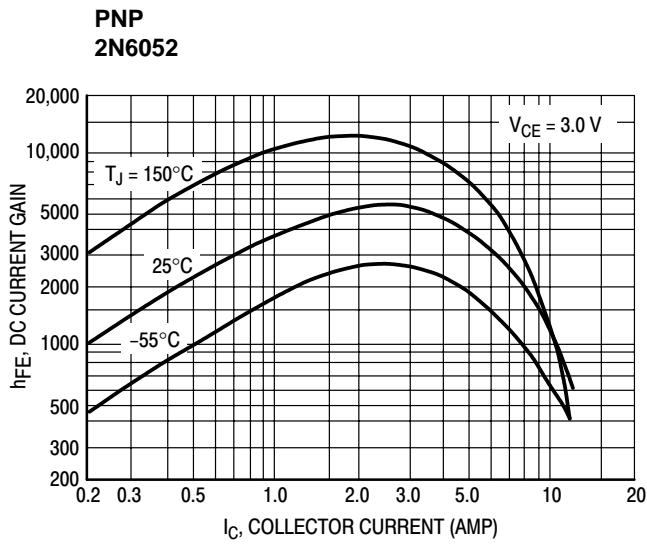


Figure 9. DC Current Gain

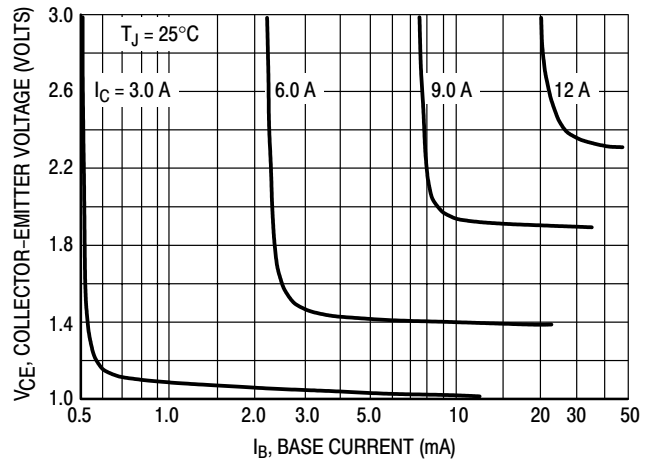
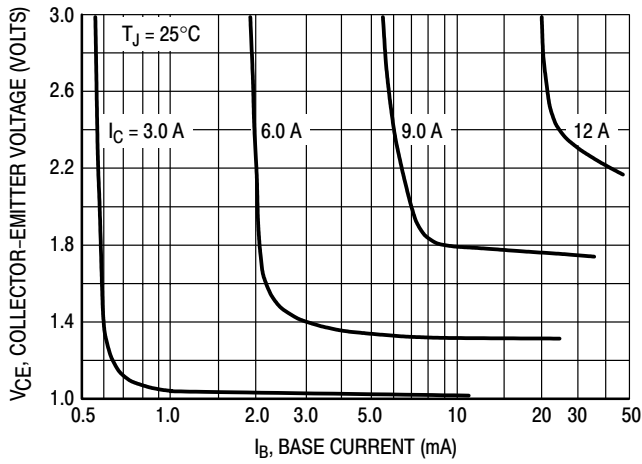


Figure 10. Collector Saturation Region

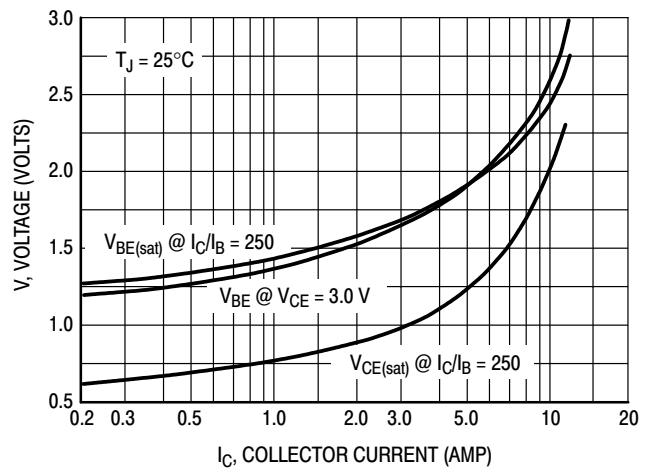
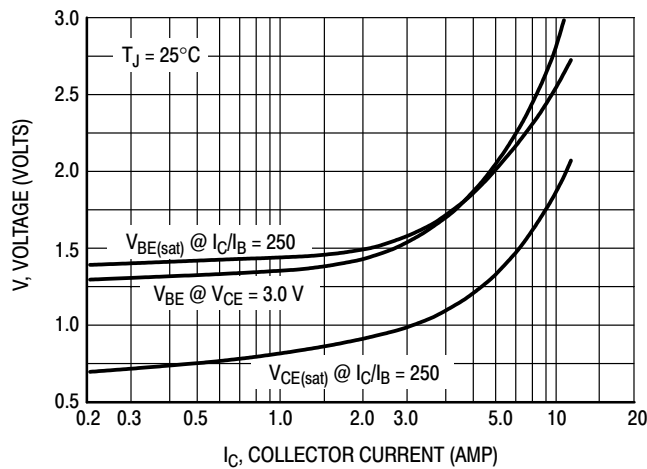


Figure 11. "On" Voltages

## Complementary Silicon Plastic Power Transistors

... designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 7.0 Amperes  
 $h_{FE} = 30-150 @ I_C$   
 = 3.0 Adc — 2N6111, 2N6288  
 = 2.3 (Min) @  $I_C = 7.0$  Adc — All Devices
- Collector-Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 30$  Vdc (Min) — 2N6111, 2N6288  
 = 50 Vdc (Min) — 2N6109  
 = 70 Vdc (Min) — 2N6107, 2N6292
- High Current Gain — Bandwidth Product  
 $f_T = 4.0$  MHz (Min) @  $I_C = 500$  mAdc — 2N6288, 90, 92  
 = 10 MHz (Min) @  $I_C = 500$  mAdc — 2N6107, 09, 11
- TO-220AB Compact Package

### \*MAXIMUM RATINGS

Rating	Symbol	2N6111 2N6288	2N6109	2N6107 2N6292	Unit
Collector-Emitter Voltage	$V_{CEO}$	30	50	70	Vdc
Collector-Base Voltage	$V_{CB}$	40	60	80	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous Peak	$I_C$	7.0 10			Adc
Base Current	$I_B$	3.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.32			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150			$^\circ\text{C}$

### THERMAL CHARACTERISTICS

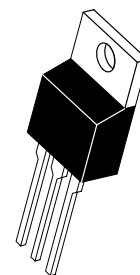
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	$^\circ\text{C/W}$

\*Indicates JEDEC Registered Data.

**PNP**  
**2N6107**  
**2N6109\***  
**2N6111**  
**NPN**  
**2N6288**  
**2N6292\***

\*ON Semiconductor Preferred Device

**7 AMPERE**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**30-50-70 VOLTS**  
**40 WATTS**



**CASE 221A-09**  
**TO-220AB**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

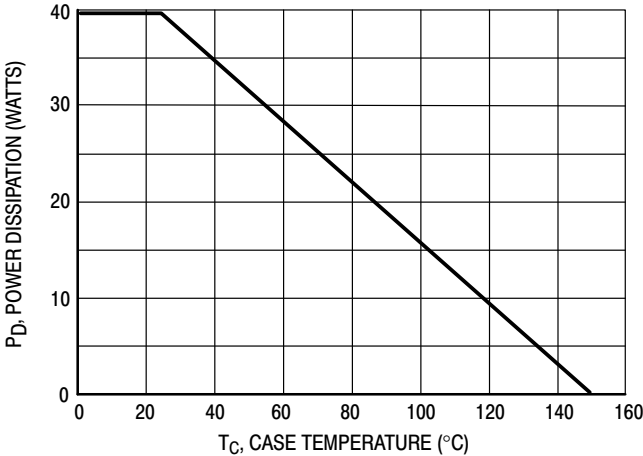


Figure 1. Power Derating

## 2N6107 2N6109 2N6111 2N6288 2N6292

\*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	$V_{CE(sus)}$	30 50 70	— — —	Vdc
				2N6111, 2N6288 2N6109 2N6107, 2N6292
Collector Cutoff Current ( $V_{CE} = 20\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— — —	1.0 1.0 1.0	mAdc
				2N6111, 2N6288 2N6109 2N6107, 2N6292
Collector Cutoff Current ( $V_{CE} = 40\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 30\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) ( $V_{CE} = 50\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) ( $V_{CE} = 70\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	— — — — — —	100 100 100 2.0 2.0 2.0	$\mu\text{Adc}$   mAdc
				2N6111, 2N6288 2N6109 2N6107, 2N6292 2N6111, 2N6288 2N6109 2N6107, 2N6292
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc

### ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 2.5\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 7.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	30 30 30 2.3	150 150 150 —	—
				2N6107, 2N6292 2N6109 2N6111, 2N6288 All Devices
Collector–Emitter Saturation Voltage ( $I_C = 7.0\text{ Adc}$ , $I_B = 3.0\text{ Adc}$ )	$V_{CE(sat)}$	—	3.5	Vdc
Base–Emitter On Voltage ( $I_C = 7.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	3.0	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product (2) ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	4.0 10	— —	MHz
				2N6288, 92 2N6107, 09, 11
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	$C_{ob}$	—	250	pF
Small–Signal Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 50\text{ kHz}$ )	$h_{fe}$	20	—	—

\*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

(2)  $f_T = |h_{fe}| \cdot f_{test}$ .

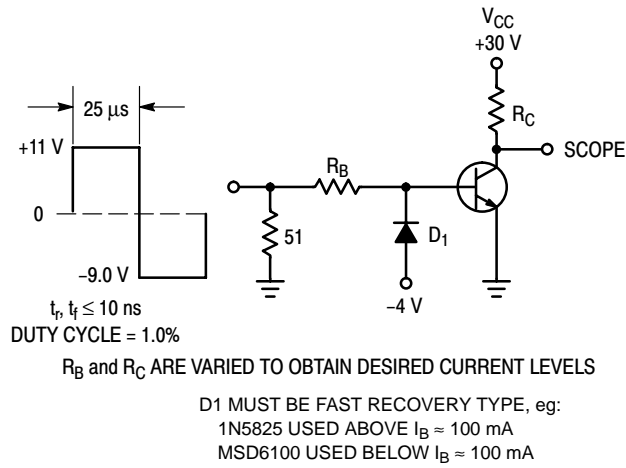


Figure 2. Switching Time Test Circuit

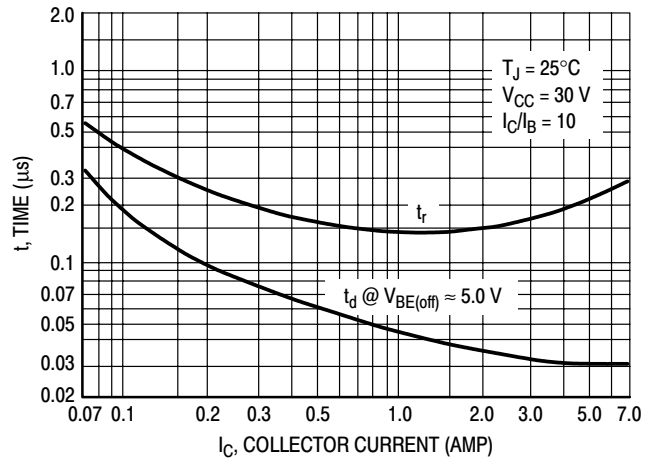


Figure 3. Turn-On Time

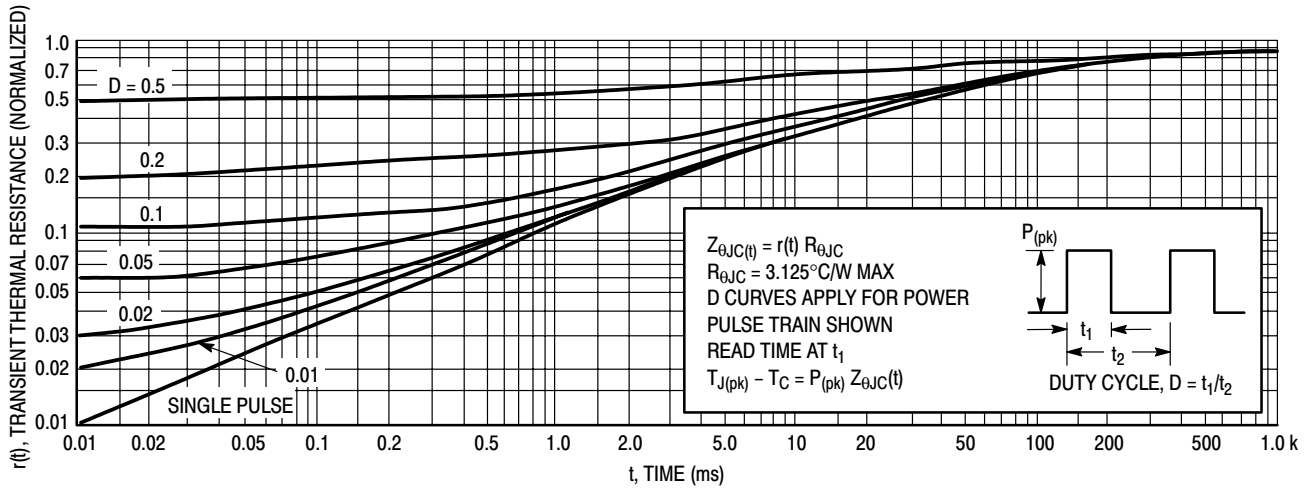


Figure 4. Thermal Response

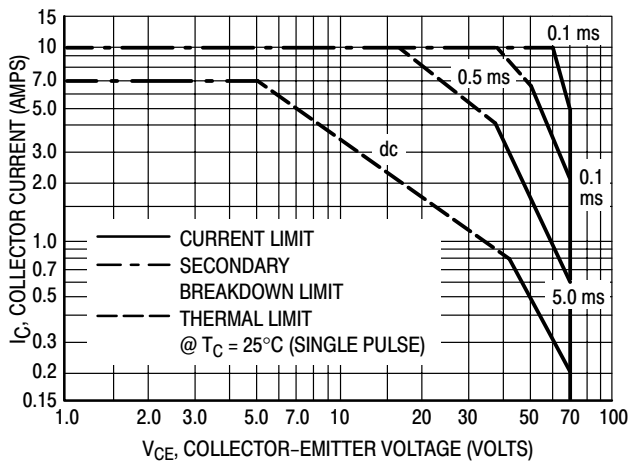


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

2N6107 2N6109 2N6111 2N6288 2N6292

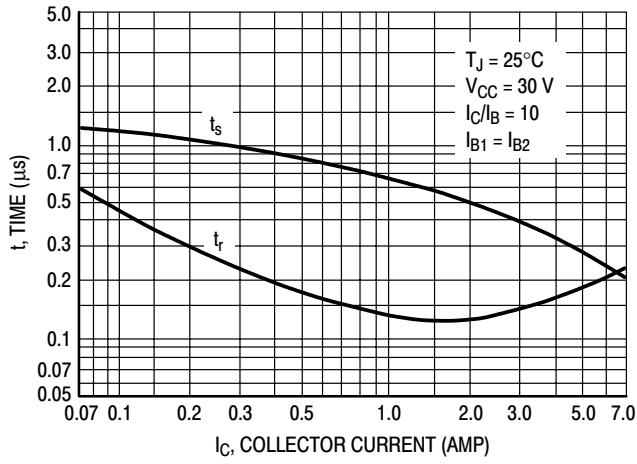


Figure 6. Turn-Off Time

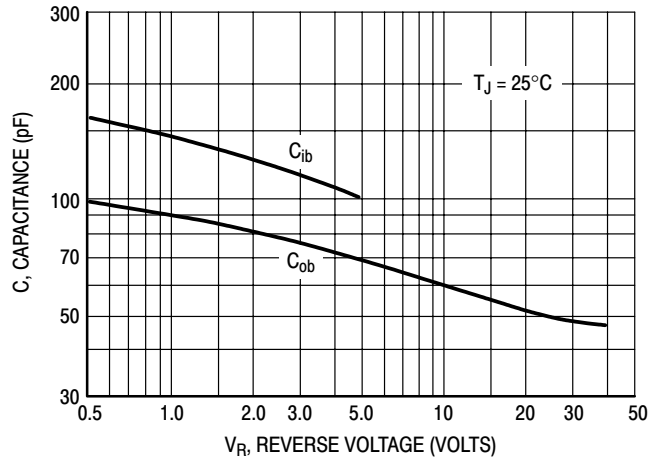


Figure 7. Capacitance



# Darlington Complementary Silicon Power Transistors

... designed for general-purpose amplifier and low-frequency switching applications.

- High DC Current Gain @  $I_C = 10 \text{ Adc}$  –  
 $h_{FE} = 2400 \text{ (Typ)} - 2N6284$   
 $= 4000 \text{ (Typ)} - 2N6287$
- Collector–Emitter Sustaining Voltage –  
 $V_{CEO(sus)} = 100 \text{ Vdc (Min)}$
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

**\*MAXIMUM RATINGS**

Rating	Symbol	2N6283 2N6286	2N6284 2N6287	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	100	Vdc
Collector–Base Voltage	$V_{CB}$	80	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current – Continuous Peak	$I_C$	20 40		Adc
Base Current	$I_B$	0.5		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	160 0.915		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +200		$^\circ\text{C}$

**\*THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.09	$^\circ\text{C/W}$

\*Indicates JEDEC Registered Data.

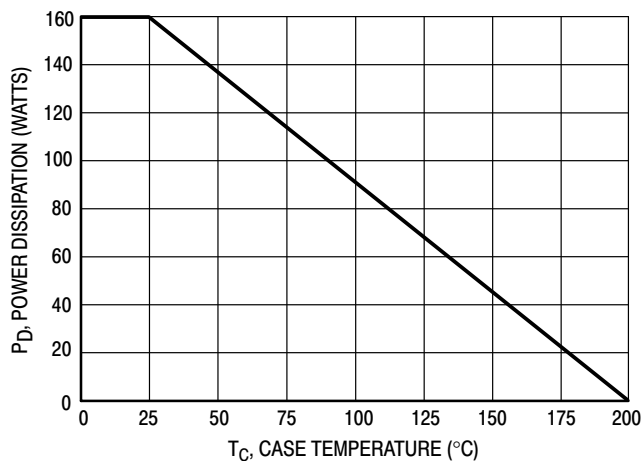


Figure 1. Power Derating

**NPN**  
**2N6283**  
  
**2N6284**  
**PNP**  
**2N6286**  
  
**2N6287**

**DARLINGTON**  
**20 AMPERE**  
**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**100 VOLTS**  
**160 WATTS**

**CASE 1–07**  
**TO–204AA**  
**(TO–3)**

## 2N6283 2N6284 2N6286 2N6287

\*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage ( $I_C = 0.1 \text{ Adc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	<b>80</b> 100	– –	Vdc
Collector Cutoff Current ( $V_{CE} = 40 \text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 50 \text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	– –	1.0 1.0	mAdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CB}$ , $V_{BE(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CB}$ , $V_{BE(off)} = 1.5 \text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	– –	0.5 5.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	2.0	mAdc
<b>ON CHARACTERISTICS (1)</b>				
DC Current Gain ( $I_C = 10 \text{ Adc}$ , $V_{CE} = 3.0 \text{ Vdc}$ ) ( $I_C = 20 \text{ Adc}$ , $V_{CE} = 3.0 \text{ Vdc}$ )	$h_{FE}$	750 100	18,000 –	–
Collector–Emitter Saturation Voltage ( $I_C = 10 \text{ Adc}$ , $I_B = 40 \text{ mAdc}$ ) ( $I_C = 20 \text{ Adc}$ , $I_B = 200 \text{ mAdc}$ )	$V_{CE(sat)}$	– –	2.0 3.0	Vdc
Base–Emitter On Voltage ( $I_C = 10 \text{ Adc}$ , $V_{CE} = 3.0 \text{ Vdc}$ )	$V_{BE(on)}$	–	2.8	Vdc
Base–Emitter Saturation Voltage ( $I_C = 20 \text{ Adc}$ , $I_B = 200 \text{ mAdc}$ )	$V_{BE(sat)}$	–	4.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Magnitude of Common Emitter Small–Signal Short–Circuit Forward Current Transfer Ratio ( $I_C = 10 \text{ Adc}$ , $V_{CE} = 3.0 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	$ h_{fe} $	4.0	–	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 0.1 \text{ MHz}$ )	$C_{ob}$	– –	400 600	pF
Small–Signal Current Gain ( $I_C = 10 \text{ Adc}$ , $V_{CE} = 3.0 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ )	$h_{fe}$	300	–	–

\*Indicates JEDEC Registered Data.

(1) Pulse test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 2%

2N6283 2N6284 2N6286 2N6287

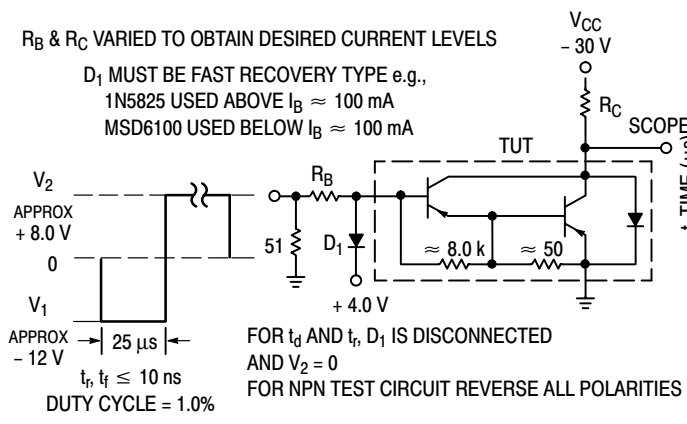


Figure 2. Switching Times Test Circuit

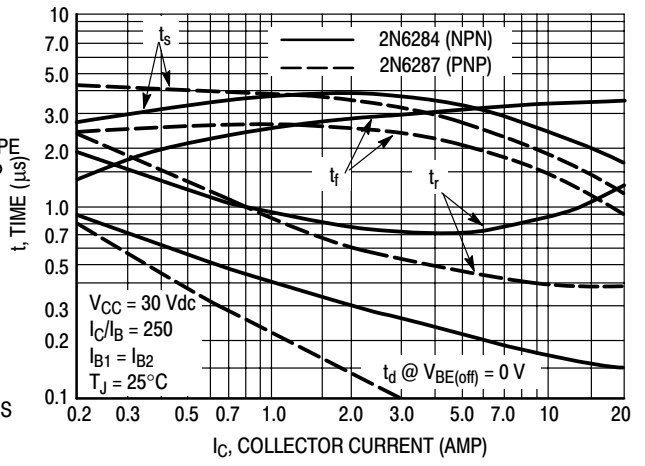


Figure 3. Switching Times

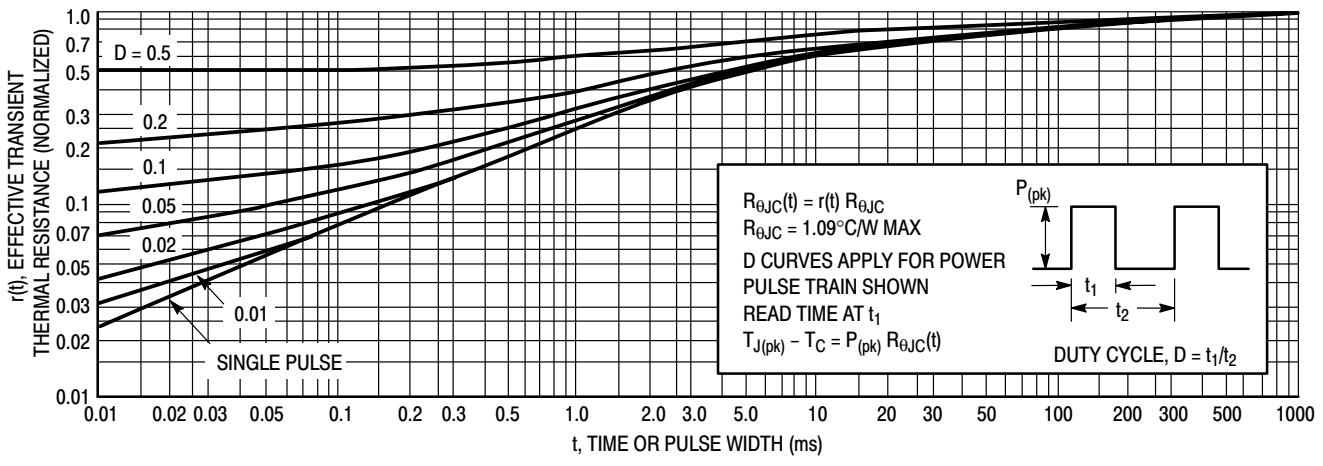


Figure 4. Thermal Response

ACTIVE-REGION SAFE OPERATING AREA

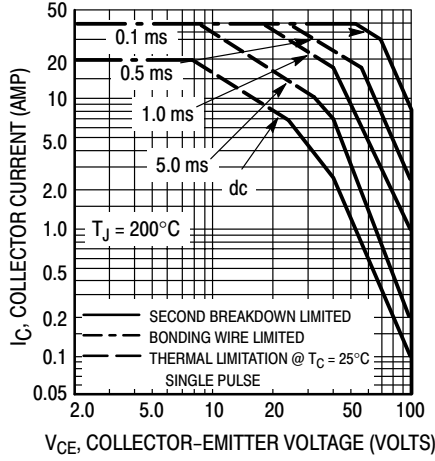


Figure 5. 2N6284, 2N6287

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 200^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

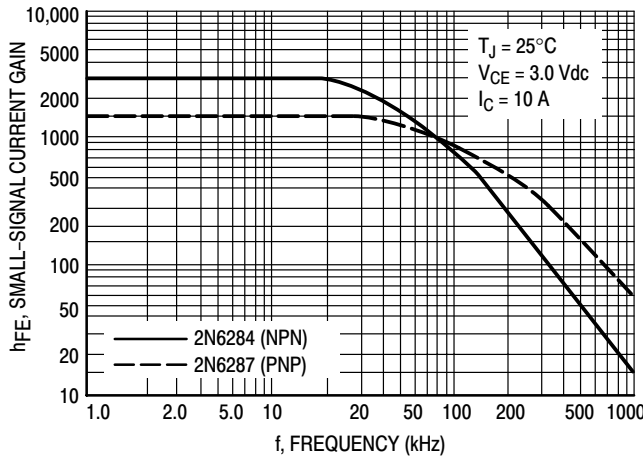


Figure 6. Small-Signal Current Gain

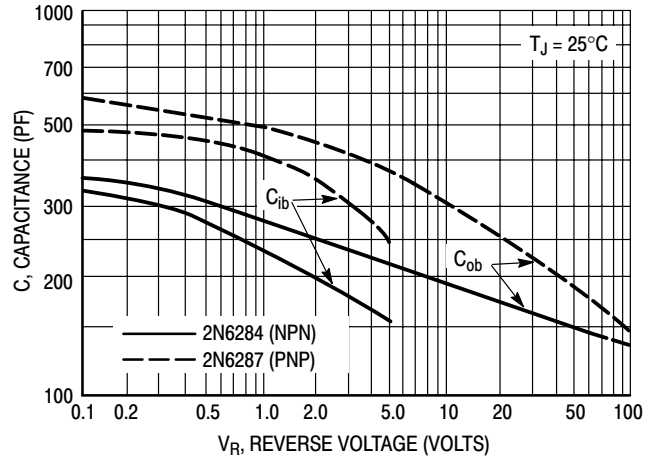
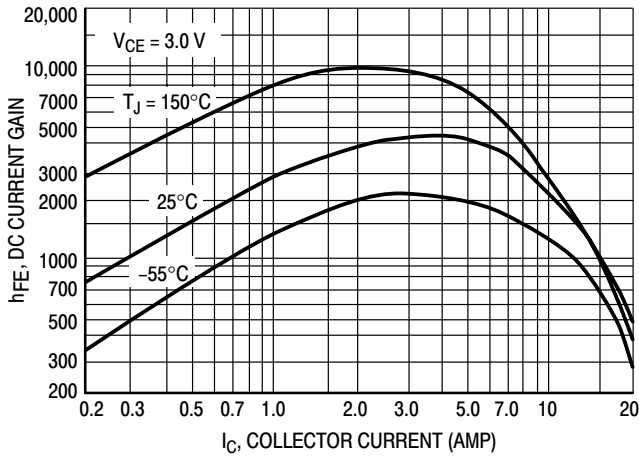


Figure 7. Capacitance

2N6283 2N6284 2N6286 2N6287

NPN  
2N6284



PNP  
2N6287

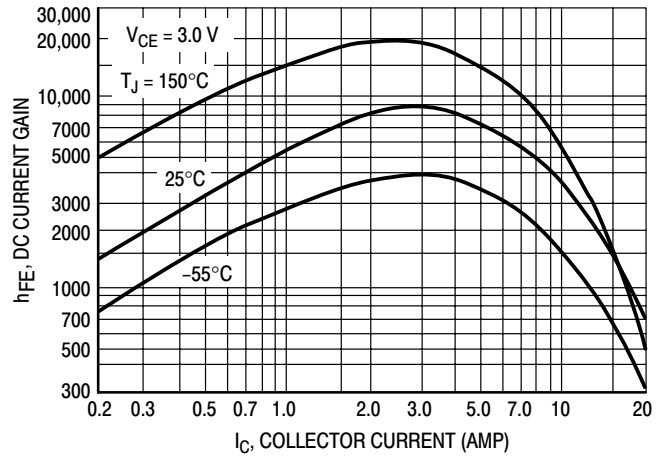


Figure 8. DC Current Gain

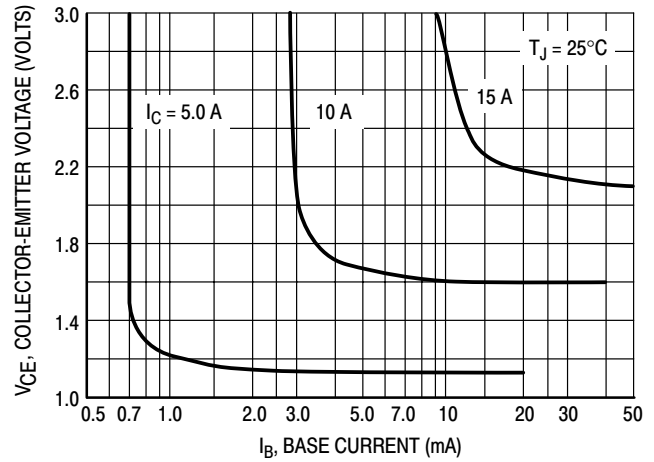
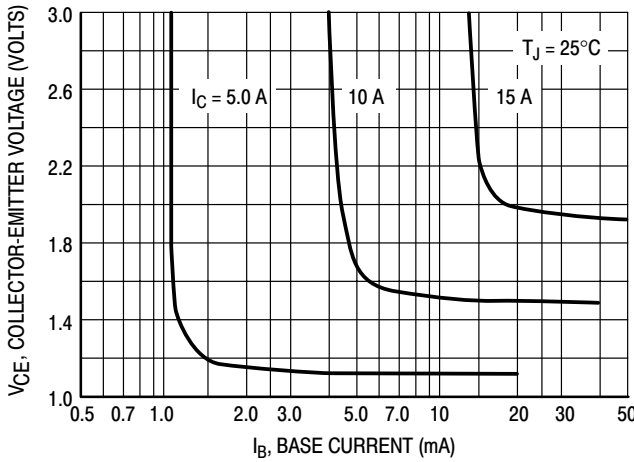


Figure 9. Collector Saturation Region

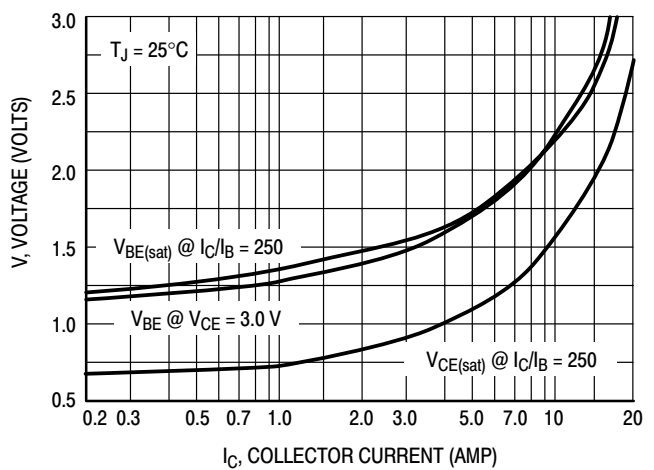
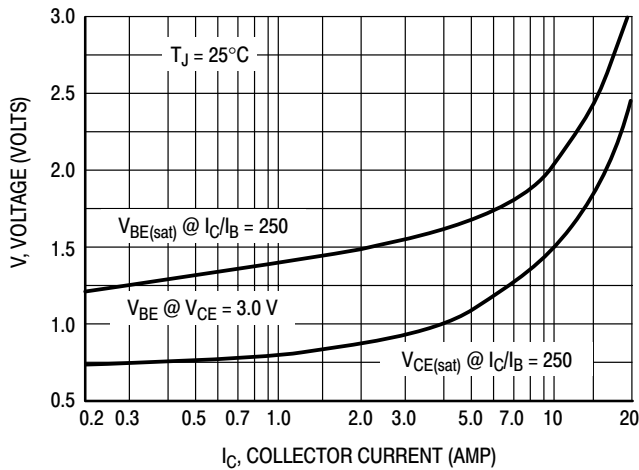


Figure 10. "On" Voltages

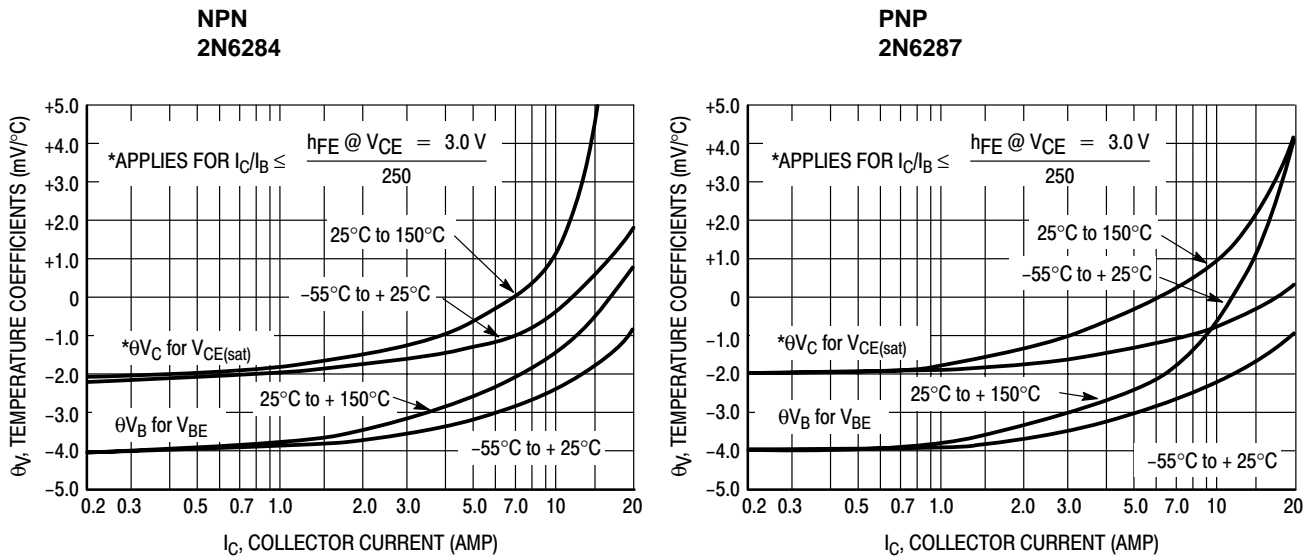


Figure 11. Temperature Coefficients

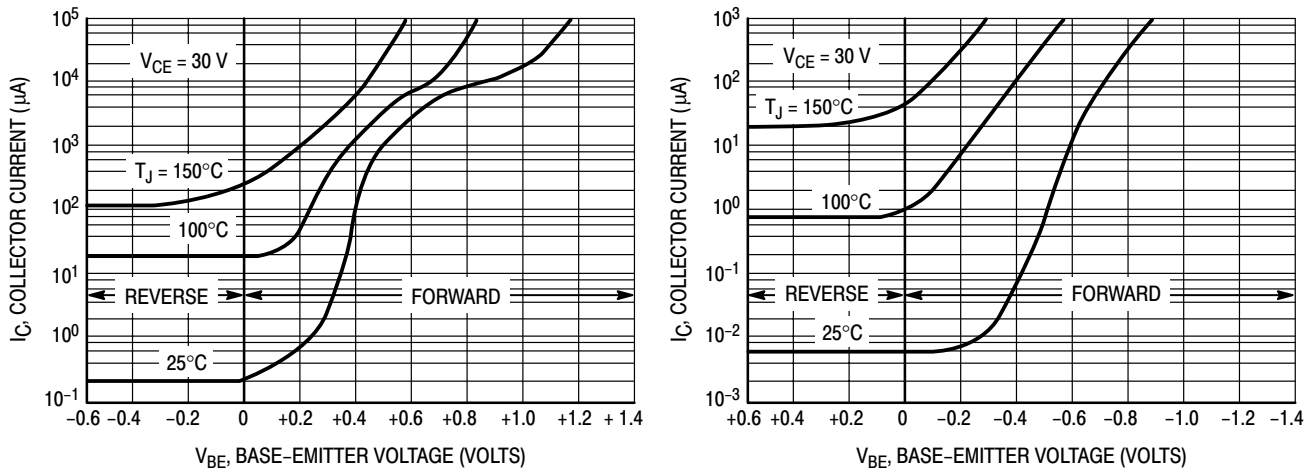


Figure 12. Collector Cut-Off Region

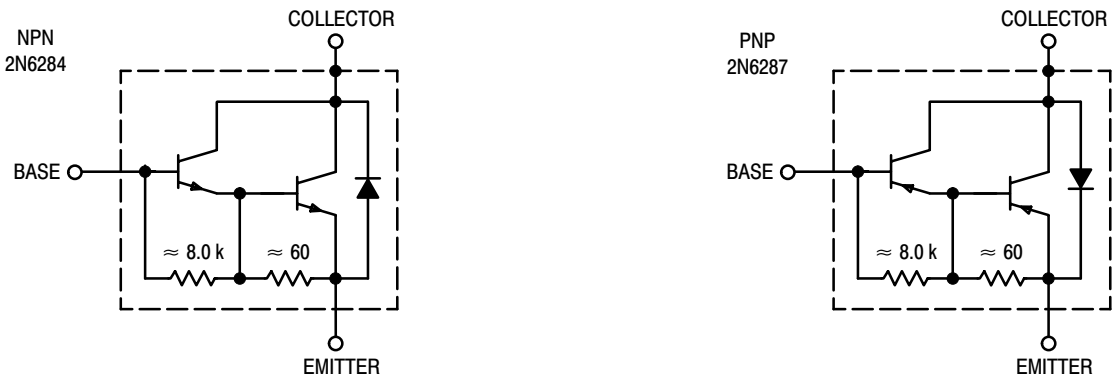


Figure 13. Darlington Schematic

# High-Power NPN Silicon Transistors

... designed for use in industrial–military power amplifier and switching circuit applications.

- High Collector–Emitter Sustaining Voltage –  
 $V_{CEO(sus)} = 100 \text{ Vdc (Min) – 2N6338}$   
 $= 150 \text{ Vdc (Min) – 2N6341}$
- High DC Current Gain –  
 $h_{FE} = 30 - 120 @ I_C = 10 \text{ Adc}$   
 $= 12 \text{ (Min) @ } I_C = 25 \text{ Adc}$
- Low Collector–Emitter Saturation Voltage –  
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) @ } I_C = 10 \text{ Adc}$
- Fast Switching Times @  $I_C = 10 \text{ Adc}$   
 $t_r = 0.3 \text{ ms (Max)}$   
 $t_s = 1.0 \text{ ms (Max)}$   
 $t_f = 0.25 \text{ ms (Max)}$

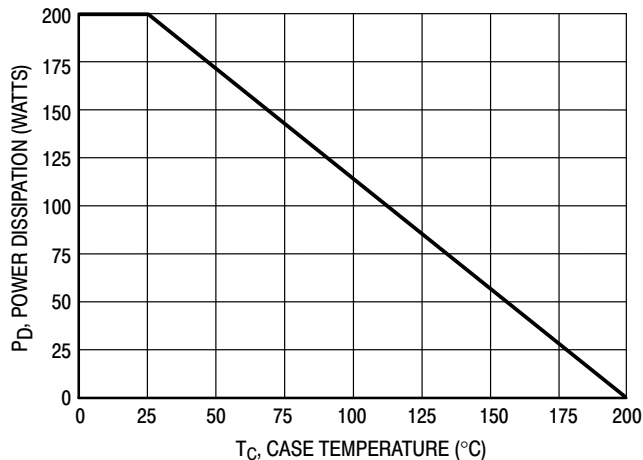
**\*MAXIMUM RATINGS**

Rating	Symbol	2N6338	2N6341	Unit
Collector–Base Voltage	$V_{CB}$	120	180	Vdc
Collector–Emitter Voltage	$V_{CEO}$	100	150	Vdc
Emitter–Base Voltage	$V_{EB}$	6.0		Vdc
Collector Current	$I_C$			Adc
Continuous		25		
Peak		50		
Base Current	$I_B$	10		Adc
Total Device Dissipation	$P_D$			Watts
@ $T_C = 25^\circ\text{C}$		200		$W/^\circ\text{C}$
Derate above $25^\circ\text{C}$		1.14		
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +200		$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.875	$^\circ\text{C/W}$

\*Indicates JEDEC Registered Data.



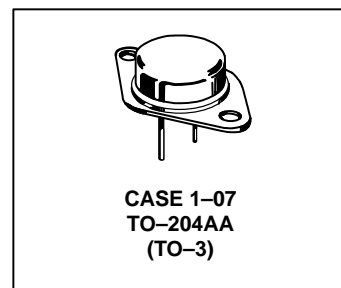
**Figure 1. Power Derating**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**2N6338**  
**2N6341\***

\*ON Semiconductor Preferred Device

**25 AMPERE**  
**POWER TRANSISTORS**  
**NPN SILICON**  
**100, 120, 140, 150 VOLTS**  
**200 WATTS**



# 2N6338 2N6341

\*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 50 \text{ mAdc}$ , $I_B = 0$ )	2N6338 2N6341 $V_{CEO(sus)}$	100 150	– –	Vdc
Collector Cutoff Current ( $V_{CE} = 50 \text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 75 \text{ Vdc}$ , $I_B = 0$ )	2N6338 2N6341 $I_{CEO}$	– –	50 50	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB(off)} = 1.5 \text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	– –	10 1.0	$\mu\text{Adc}$ mAdc
Collector Cutoff Current ( $V_{CB} = \text{Rated } V_{CB}$ , $I_E = 0$ )	$I_{CBO}$	–	10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 6.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	100	$\mu\text{Adc}$

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 0.5 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ ) ( $I_C = 10 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ ) ( $I_C = 25 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ )	$h_{FE}$	50 30 12	– 120 –	–
Collector Emitter Saturation Voltage ( $I_C = 10 \text{ Adc}$ , $I_B = 1.0 \text{ Adc}$ ) ( $I_C = 25 \text{ Adc}$ , $I_B = 2.5 \text{ Adc}$ )	$V_{CE(sat)}$	– –	1.0 1.8	Vdc
Base–Emitter Saturation Voltage ( $I_C = 10 \text{ Adc}$ , $I_B = 1.0 \text{ Adc}$ ) ( $I_C = 25 \text{ Adc}$ , $I_B = 2.5 \text{ Adc}$ )	$V_{BE(sat)}$	– –	1.8 2.5	Vdc
Base–Emitter On Voltage ( $I_C = 10 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ )	$V_{BE(on)}$	–	1.8	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product (2) ( $I_C = 1.0 \text{ Adc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f_{test} = 10 \text{ MHz}$ )	$f_T$	40	–	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 0.1 \text{ MHz}$ )	$C_{ob}$	–	300	pF

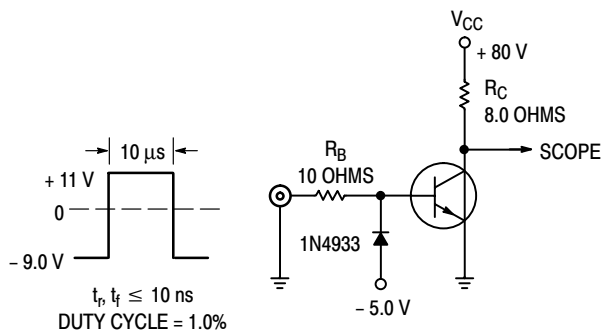
## SWITCHING CHARACTERISTICS

Rise Time ( $V_{CC} \approx 80 \text{ Vdc}$ , $I_C = 10 \text{ Adc}$ , $I_{B1} = 1.0 \text{ Adc}$ , $V_{BE(off)} = 6.0 \text{ Vdc}$ )	$t_r$	–	0.3	$\mu\text{s}$
Storage Time ( $V_{CC} \approx 80 \text{ Vdc}$ , $I_C = 10 \text{ Adc}$ , $I_{B1} = I_{B2} = 1.0 \text{ Adc}$ )	$t_s$	–	1.0	$\mu\text{s}$
Fall Time ( $V_{CC} \approx 80 \text{ Vdc}$ , $I_C = 10 \text{ Adc}$ , $I_{B1} = I_{B2} = 1.0 \text{ Adc}$ )	$t_f$	–	0.25	$\mu\text{s}$

\*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

(2)  $f_T = |h_{fe}| \cdot f_{test}$ .



NOTE: For information on Figures 3 and 6,  $R_B$  and  $R_C$  were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

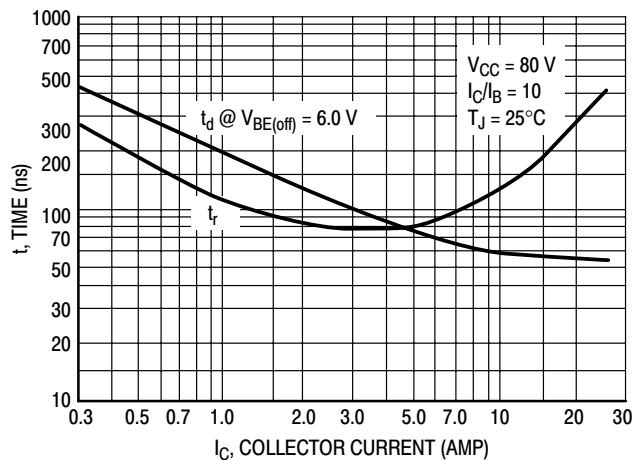


Figure 3. Turn–On Time



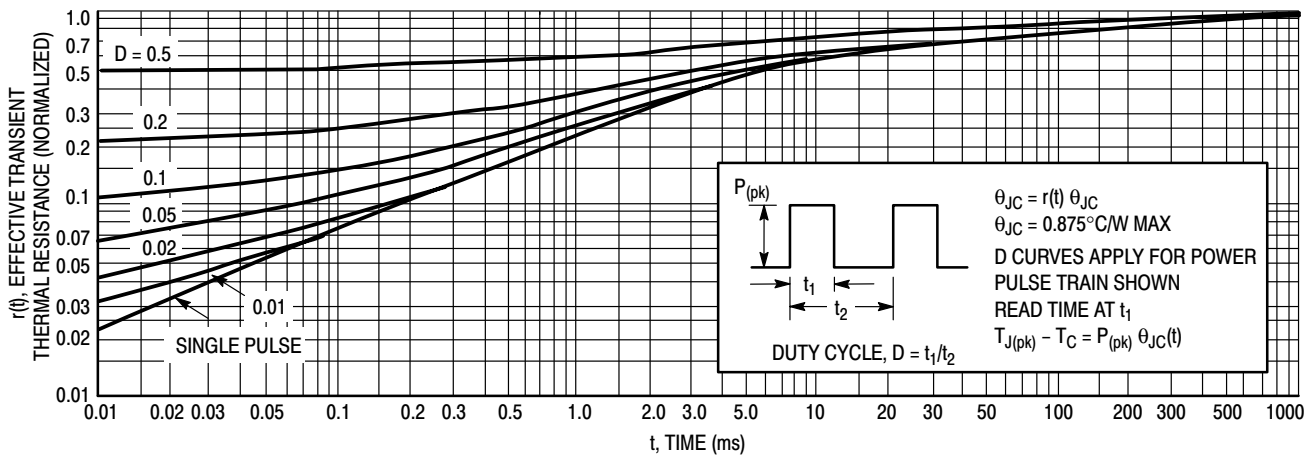


Figure 4. Thermal Response

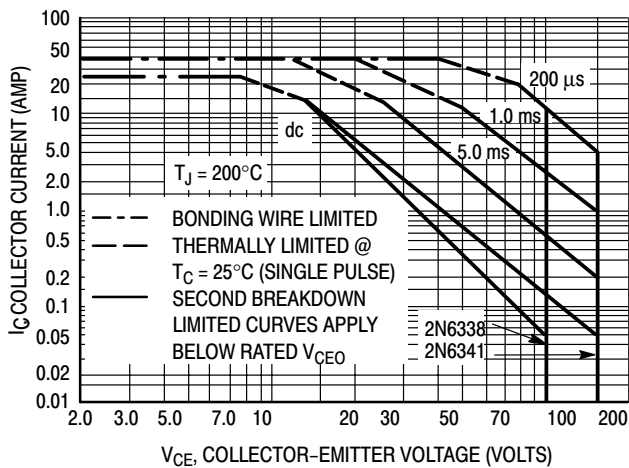


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

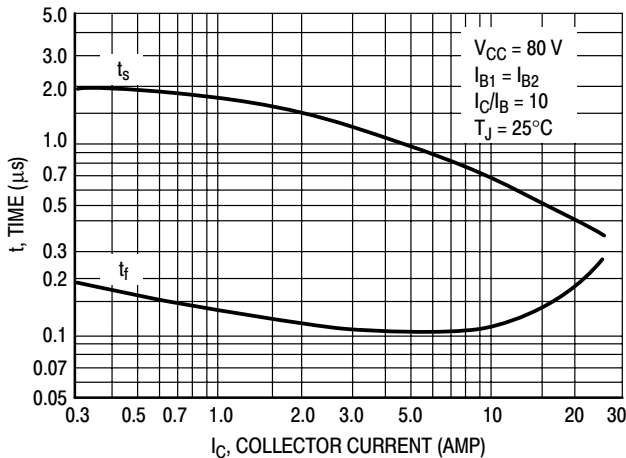


Figure 6. Turn-Off Time

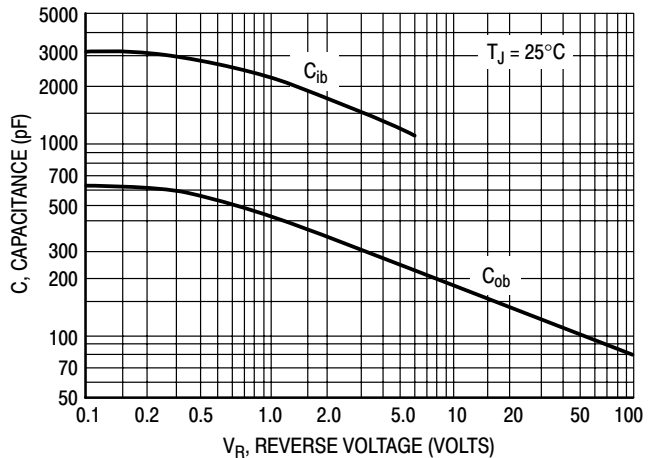


Figure 7. Capacitance

# Plastic Medium-Power Silicon Transistors

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —  
 $h_{FE} = 2500$  (Typ) @  $I_C$   
 $= 4.0$  Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc  
 $V_{CE(sus)} = 60$  Vdc (Min) — 2N6387  
 $= 80$  Vdc (Min) — 2N6388
- Low Collector-Emitter Saturation Voltage —  
 $V_{CE(sat)} = 2.0$  Vdc (Max) @  $I_C$   
 $= 5.0$  Adc — 2N6387, 2N6388
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package

**\*MAXIMUM RATINGS**

Rating	Symbol	2N6387	2N6388	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	80	Vdc
Collector-Base Voltage	$V_{CB}$	60	80	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous	$I_C$	10	10	Adc
Peak		15	15	
Base Current	$I_B$	250		mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	65		Watts W/ $^\circ\text{C}$
		0.52		
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0		Watts W/ $^\circ\text{C}$
		0.016		
Operating and Storage Junction, Temperature Range	$T_J, T_{stg}$	-65 to +150		$^\circ\text{C}$

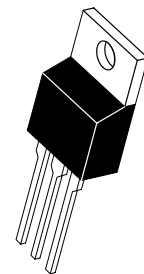
**THERMAL CHARACTERISTICS**

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

**2N6387**  
**2N6388\***

\*ON Semiconductor Preferred Device

**DARLINGTON**  
**8 AND 10 AMPERE**  
**NPN SILICON**  
**POWER TRANSISTORS**  
**60-80 VOLTS**  
**65 WATTS**



**CASE 221A-09**  
**TO-220AB**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# 2N6387 2N6388

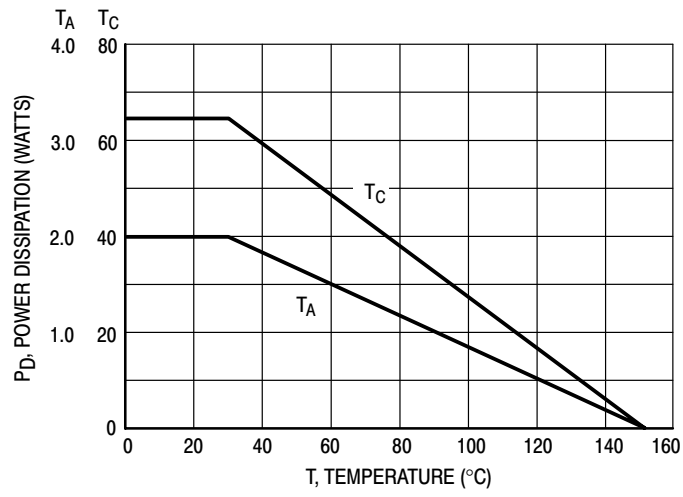


Figure 1. Power Derating

## 2N6387 2N6388

**\*ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (1) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	2N6387 2N6388	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 80\text{ Vdc}$ , $I_B = 0$ )	2N6387 2N6388	$I_{CEO}$	— —	1.0 1.0	mAdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	2N6387 2N6388 2N6387 2N6388	$I_{CEX}$	— — — —	300 300 3.0 3.0	$\mu\text{Adc}$  mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	5.0	mAdc

### ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	2N6387, 2N6388 2N6387, 2N6388	$h_{FE}$	1000 100	20,000 —	—
Collector–Emitter Saturation Voltage ( $I_C = 5.0\text{ Adc}$ , $I_B = 0.01\text{ Adc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )	2N6387, 2N6388 2N6387, 2N6388	$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base–Emitter On Voltage ( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 10\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	2N6387, 2N6388 2N6387, 2N6388	$V_{BE(on)}$	— —	2.8 4.5	Vdc

### DYNAMIC CHARACTERISTICS

Small–Signal Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$ h_{fe} $	20	—	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	$C_{ob}$	—	200	$\mu\text{F}$
Small–Signal Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	1000	—	—

\*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

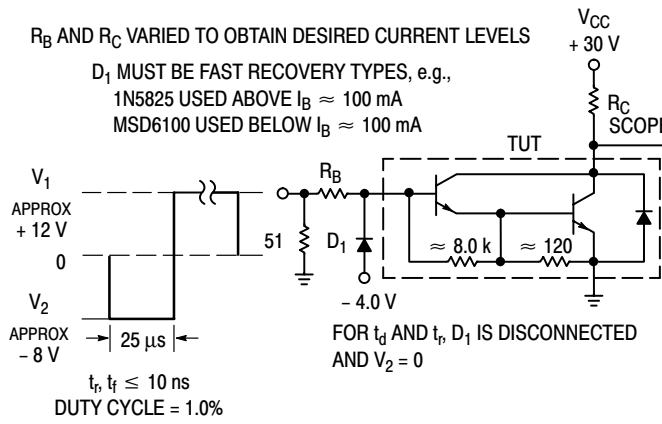


Figure 2. Switching Times Test Circuit

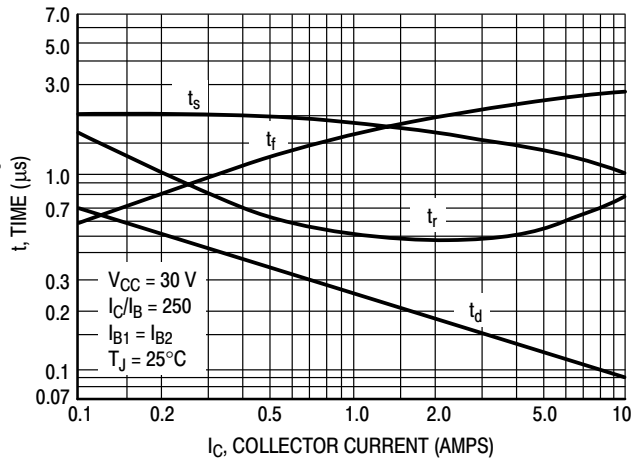


Figure 3. Switching Times

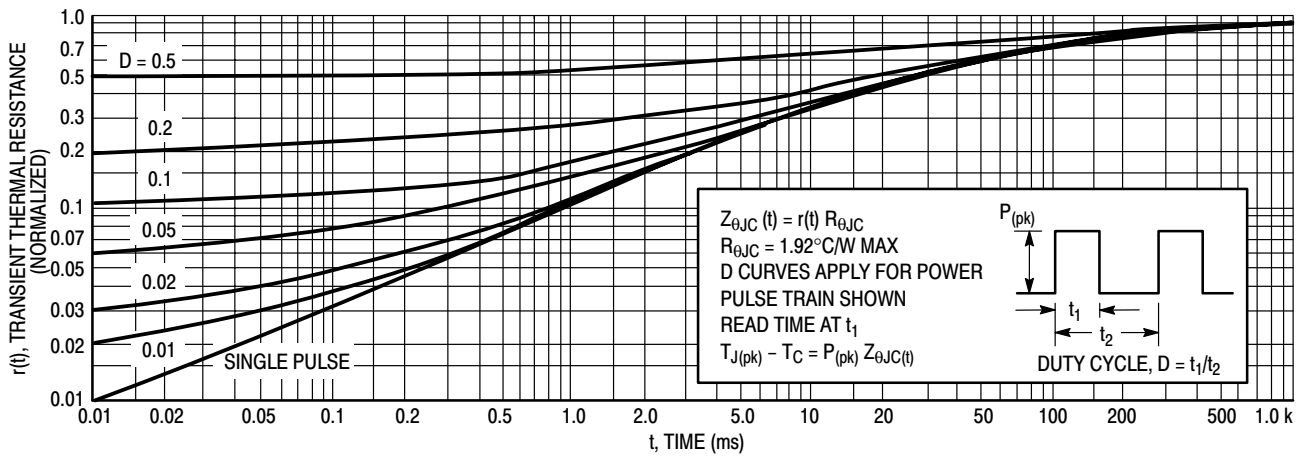


Figure 4. Thermal Response

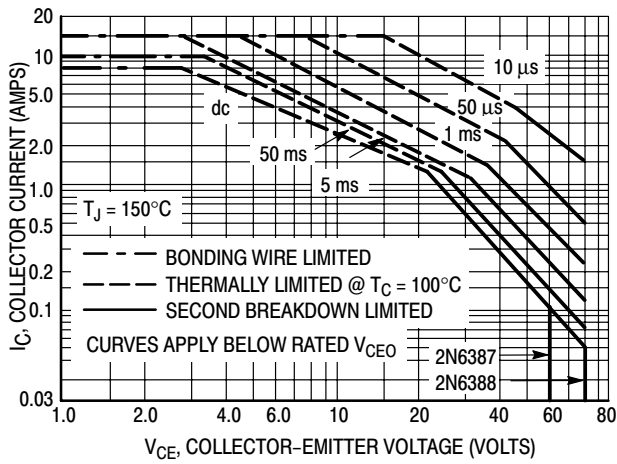


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

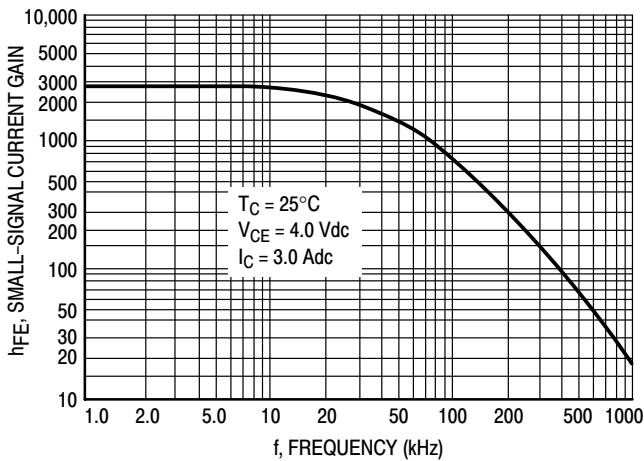


Figure 6. Small-Signal Current Gain

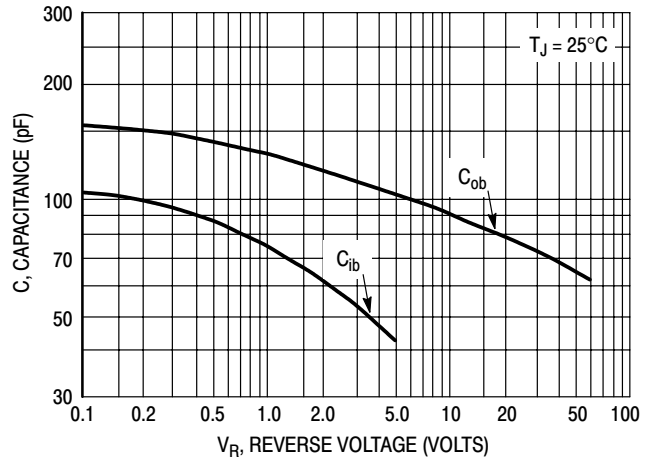


Figure 7. Capacitance

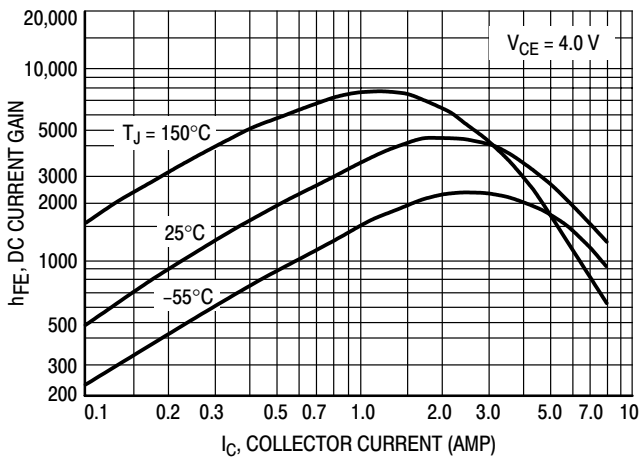


Figure 8. DC Current Gain

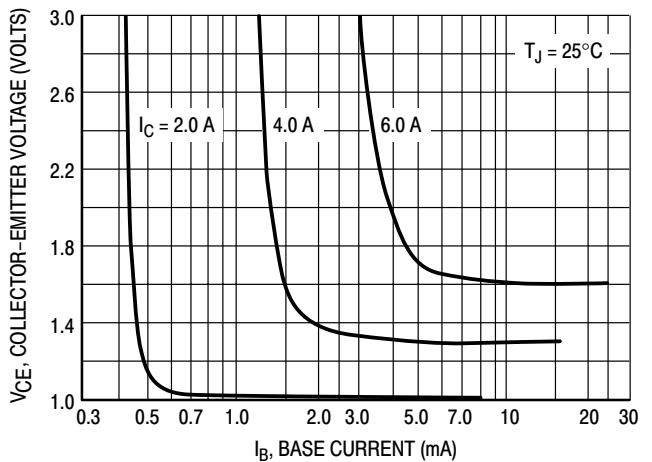


Figure 9. Collector Saturation Region

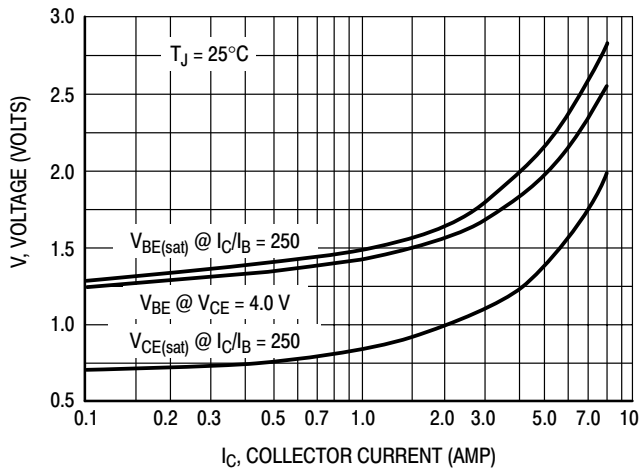


Figure 10. "On" Voltages

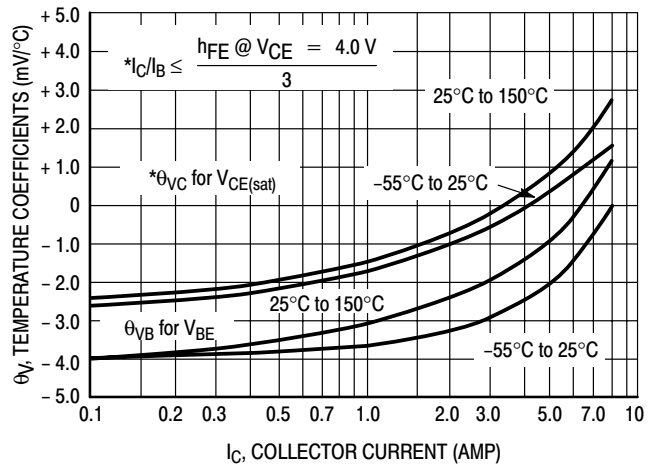


Figure 11. Temperature Coefficients

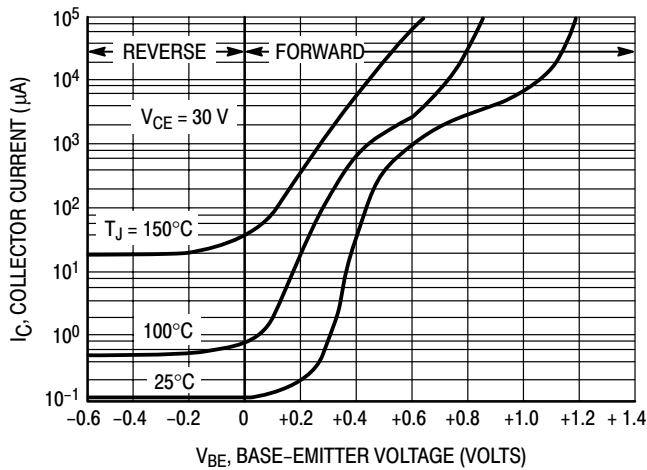


Figure 12. Collector Cut-Off Region

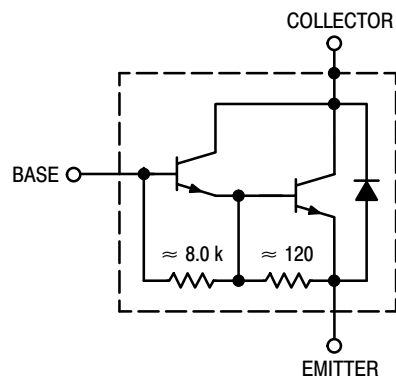


Figure 13. Darlington Schematic

# Complementary Silicon Plastic Power Transistors

... designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 15 Amperes —  
 $h_{FE} = 20-150 @ I_C = 5.0 \text{ Adc}$   
 $= 5.0 (\text{Min}) @ I_C = 15 \text{ Adc}$
- Collector-Emitter Sustaining Voltage —  
 $V_{CEO(\text{sus})} = 60 \text{ Vdc (Min) - 2N6487, 2N6490}$   
 $= 80 \text{ Vdc (Min) - 2N6488, 2N6491}$
- High Current Gain — Bandwidth Product  
 $f_T = 5.0 \text{ MHz (Min) @ } I_C = 1.0 \text{ Adc}$
- TO-220AB Compact Package

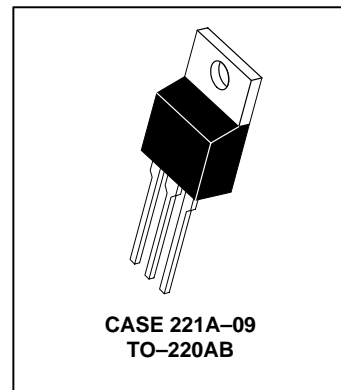
**NPN**  
**2N6487**  
  
**2N6488\***  
**PNP**  
**2N6490**  
  
**2N6491\***

\*ON Semiconductor Preferred Device

**15 AMPERE**  
**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**60-80 VOLTS**  
**75 WATTS**

## MAXIMUM RATINGS (1)

Rating	Symbol	2N6487 2N6490	2N6488 2N6491	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	80	Vdc
Collector-Base Voltage	$V_{CB}$	70	90	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous	$I_C$	15		Adc
Base Current	$I_B$	5.0		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	75		Watts
		0.6		W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.8		Watts
		0.014		W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150		$^\circ\text{C}$



## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.



2N6487 2N6488 2N6490 2N6491

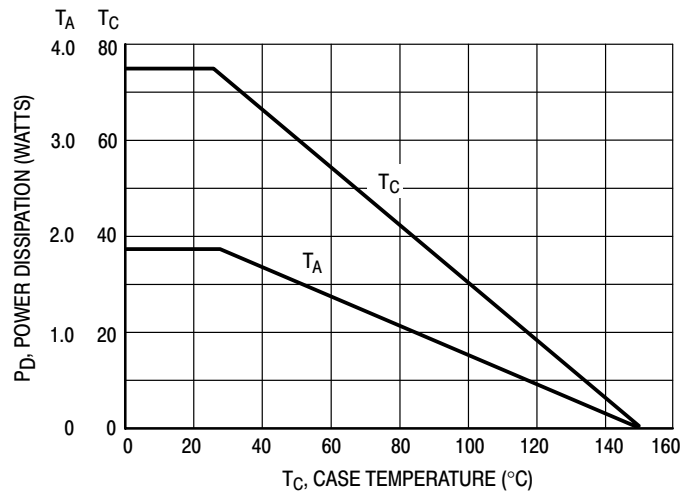


Figure 1. Power Derating

## 2N6487 2N6488 2N6490 2N6491

\*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (1) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	2N6487, 2N6490 2N6488, 2N6491	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector–Emitter Sustaining Voltage (1) ( $I_C = 200\text{ mAdc}$ , $V_{BE} = 1.5\text{ Vdc}$ )	2N6487, 2N6490 2N6488, 2N6491	$V_{CEX}$	70 90	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ )	2N6487, 2N6490 2N6488, 2N6491	$I_{CEO}$	— —	1.0 1.0	mAdc
Collector Cutoff Current ( $V_{CE} = 65\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 85\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	2N6487, 2N6490 2N6488, 2N6491 2N6487, 2N6490 2N6488, 2N6491	$I_{CEX}$	— — — —	500 500 5.0 5.0	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	1.0	mAdc
<b>ON CHARACTERISTICS</b>					
DC Current Gain ( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 15\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )		$h_{FE}$	20 5.0	150 —	—
Collector–Emitter Saturation Voltage ( $I_C = 5.0\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ ) ( $I_C = 15\text{ Adc}$ , $I_B = 5.0\text{ Adc}$ )		$V_{CE(sat)}$	— —	1.3 3.5	Vdc
Base–Emitter On Voltage ( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 15\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )		$V_{BE(on)}$	— —	1.3 3.5	Vdc
<b>DYNAMIC CHARACTERISTICS</b>					
Current–Gain — Bandwidth Product (2) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )		$f_T$	5.0	—	MHz
Small–Signal Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )		$h_{fe}$	25	—	—

\*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

(2)  $f_T = |h_{fe}| \cdot f_{test}$ .

2N6487 2N6488 2N6490 2N6491

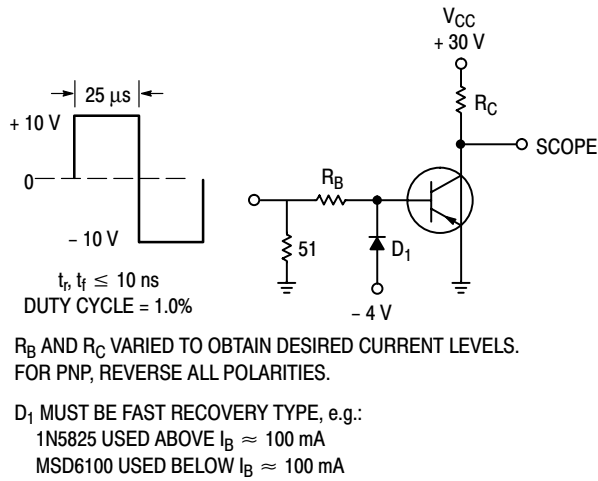


Figure 2. Switching Time Test Circuit

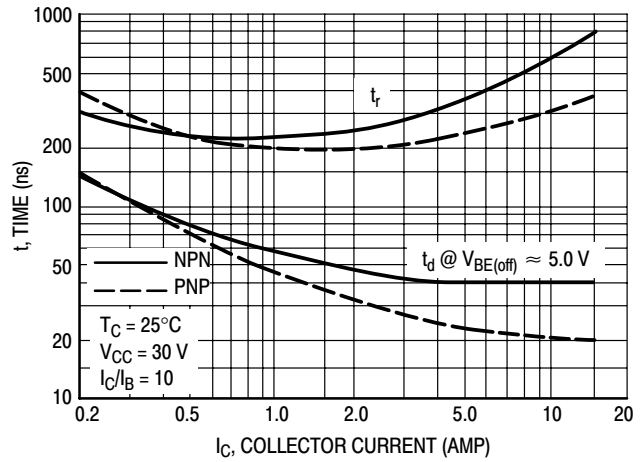


Figure 3. Turn-On Time

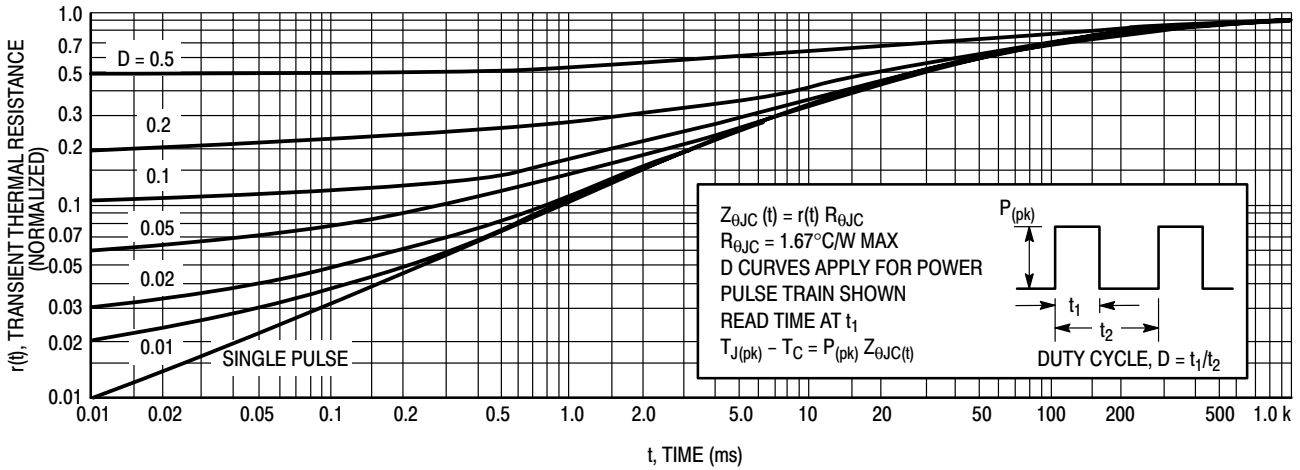


Figure 4. Thermal Response

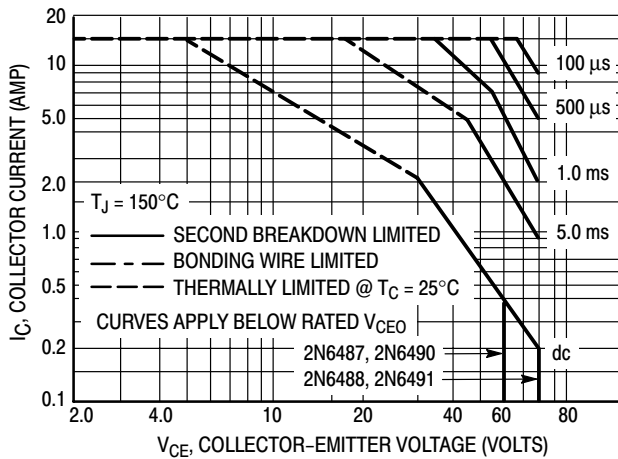


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistors average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

2N6487 2N6488 2N6490 2N6491

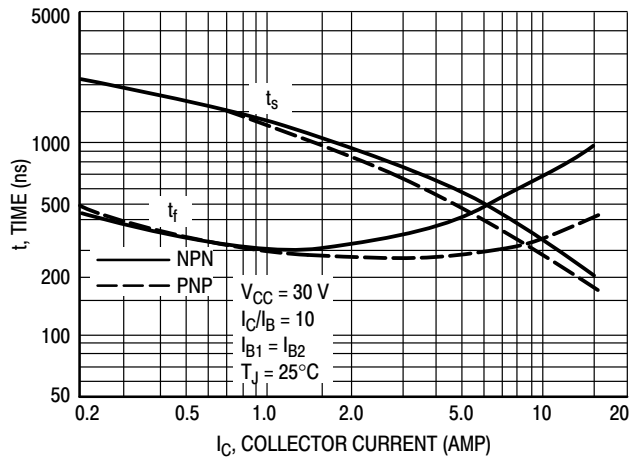


Figure 6. Turn-Off Time

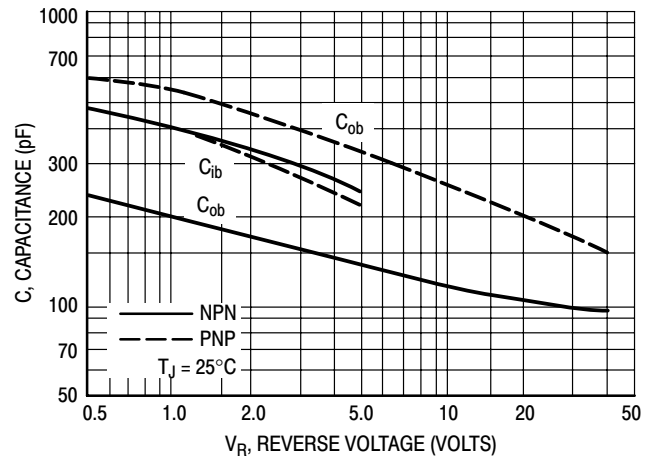


Figure 7. Capacitances

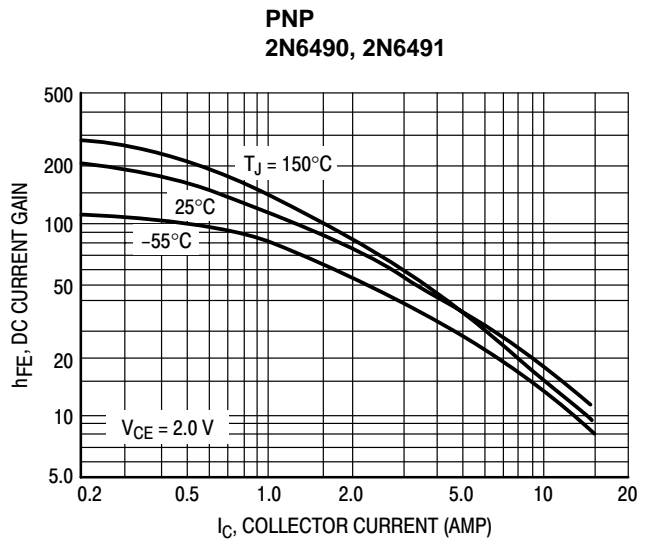
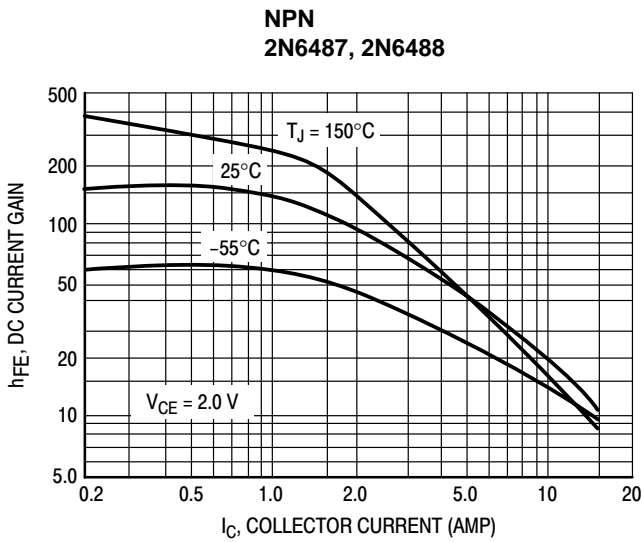


Figure 8. DC Current Gain

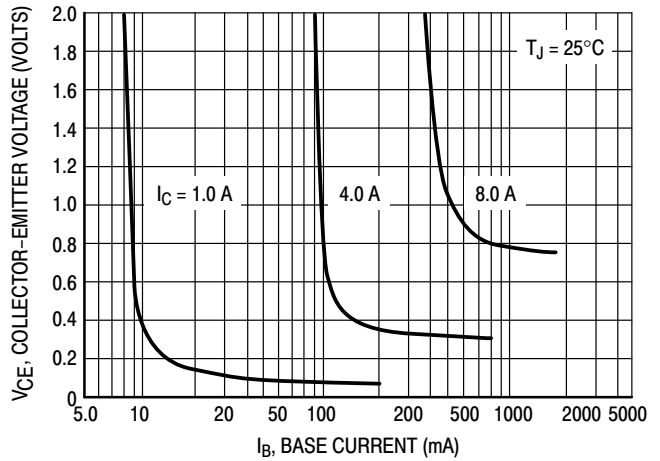
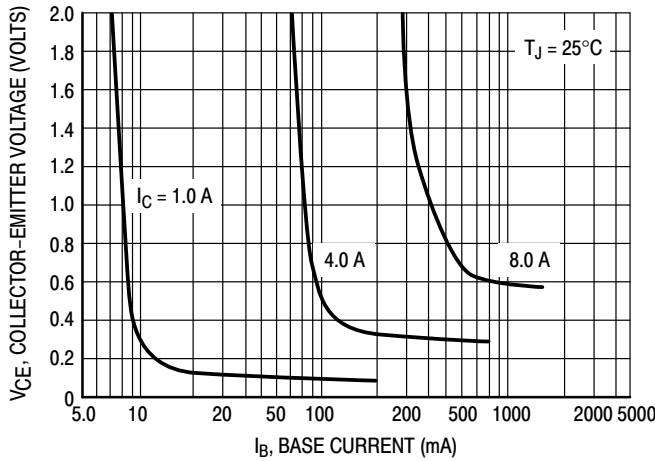


Figure 9. Collector Saturation Region

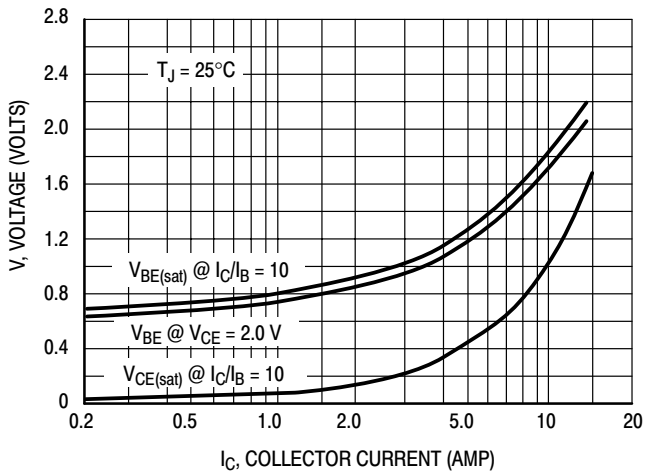
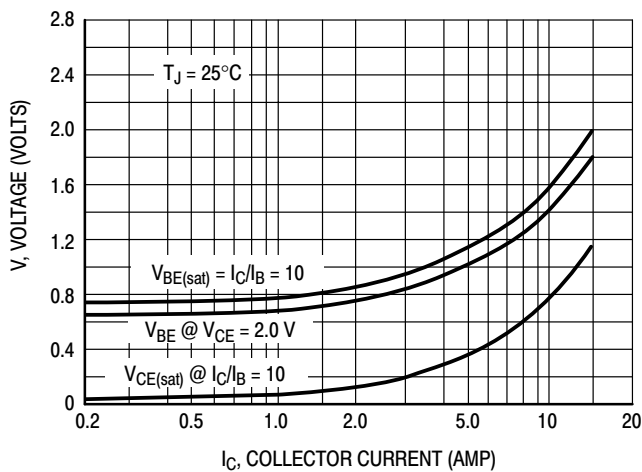


Figure 10. "On" Voltages

## High Voltage NPN Silicon Power Transistors

... designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications.

- High Collector–Emitter Sustaining Voltage –  
 $V_{CEO(sus)} = 250 \text{ Vdc (Min)}$
- Excellent DC Current Gain  
 $h_{FE} = 10\text{--}75 @ I_C = 2.5 \text{ Adc}$
- Low Collector–Emitter Saturation Voltage @  $I_C = 2.5 \text{ Adc}$  –  
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max)}$

### MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	Vdc
Collector–Base Voltage	$V_{CB}$	350	Vdc
Emitter–Base Voltage	$V_{EB}$	6.0	Vdc
Collector Current – Continuous – Peak	$I_C$	5.0 10	A dc
Base Current	$I_B$	2.0	A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	80 0.64	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

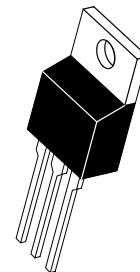
### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

# 2N6497

**5 AMPERE  
POWER TRANSISTORS  
NPN SILICON  
250 VOLT  
80 WATTS**



**CASE 221A–09  
TO–220AB**

# 2N6497

## \*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (1) ( $I_C = 25 \text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	250	–	–	Vdc
Collector Cutoff Current ( $V_{CE} = 350 \text{ Vdc}$ , $V_{BE(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 175 \text{ Vdc}$ , $V_{BE(off)} = 1.5 \text{ Vdc}$ , $T_C = 100^\circ\text{C}$ )	$I_{CEX}$	–	–	1.0 10	mAdc
Emitter Cutoff Current ( $V_{BE} = 6.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	–	1.0	mAdc

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 2.5 \text{ Adc}$ , $V_{CE} = 10 \text{ Vdc}$ ) ( $I_C = 5.0 \text{ Adc}$ , $V_{CE} = 10 \text{ Vdc}$ )	$h_{FE}$	10 3.0	– –	75 –	–
Collector–Emitter Saturation Voltage ( $I_C = 2.5 \text{ Adc}$ , $I_B = 500 \text{ mAdc}$ ) ( $I_C = 5.0 \text{ Adc}$ , $I_B = 2.0 \text{ Adc}$ )	$V_{CE(sat)}$	– –	– –	1.0 5.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 2.5 \text{ Adc}$ , $I_B = 500 \text{ mAdc}$ ) ( $I_C = 5.0 \text{ Adc}$ , $I_B = 2.0 \text{ Adc}$ )	$V_{BE(sat)}$	– –	– –	1.5 2.5	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product ( $I_C = 250 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	$f_T$	5.0	–	–	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 100 \text{ kHz}$ )	$C_{ob}$	–	–	150	pF

## SWITCHING CHARACTERISTICS

Rise Time ( $V_{CC} = 125 \text{ Vdc}$ , $I_C = 2.5 \text{ Adc}$ , $I_{B1} = 0.5 \text{ Adc}$ )	$t_r$	–	0.4	1.0	$\mu\text{s}$
Storage Time ( $V_{CC} = 125 \text{ Vdc}$ , $I_C = 2.5 \text{ Adc}$ , $V_{BE} = 5.0 \text{ Vdc}$ , $I_{B1} = I_{B2} = 0.5 \text{ Adc}$ )	$t_s$	–	1.4	2.5	$\mu\text{s}$
Fall Time ( $V_{CC} = 125 \text{ Vdc}$ , $I_C = 2.5 \text{ Adc}$ , $I_{B1} = I_{B2} = 0.5 \text{ Adc}$ )	$t_f$	–	0.45	1.0	$\mu\text{s}$

\*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

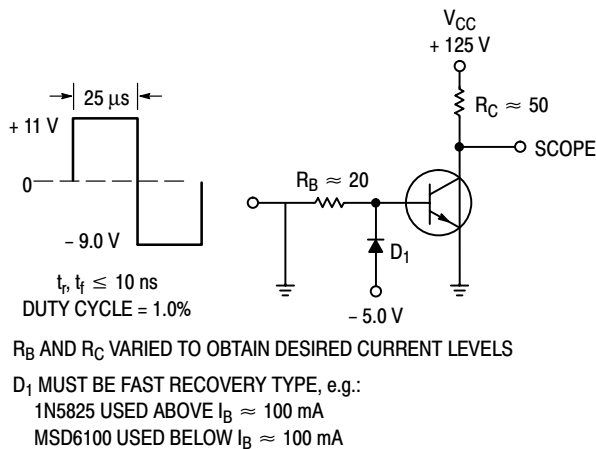


Figure 11. Switching Time Test Circuit

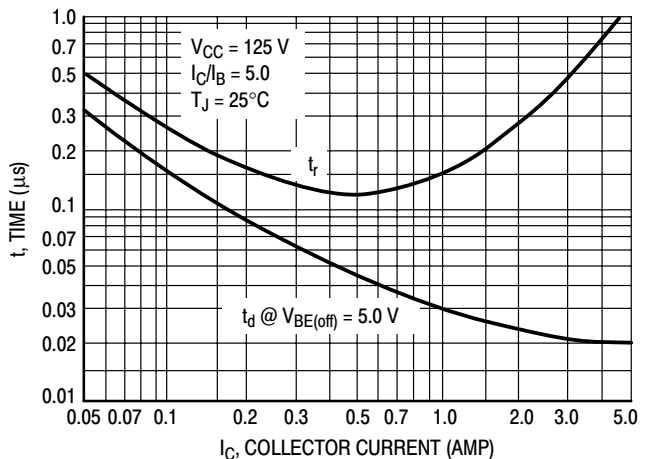


Figure 12. Turn–On Time

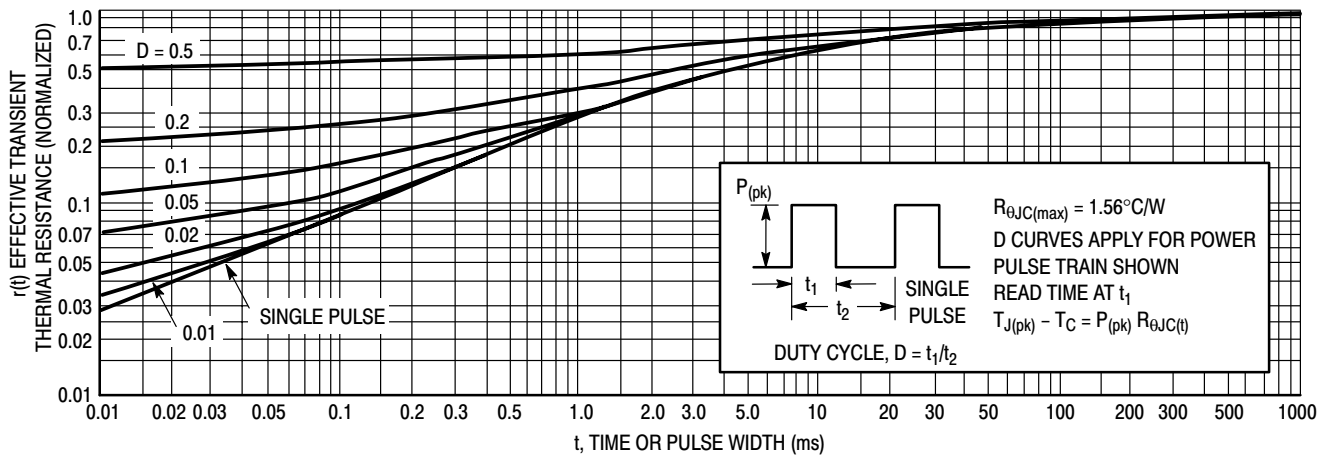


Figure 13. Thermal Response

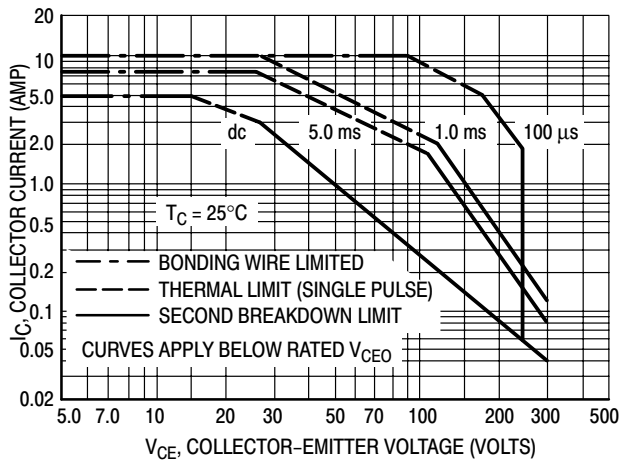


Figure 14. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 14 is based on  $T_C = 25^\circ C$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ C$ .  $T_{J(pk)}$  may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltage shown on Figure 14 may be found at any case temperature by using the appropriate curve on Figure 16.

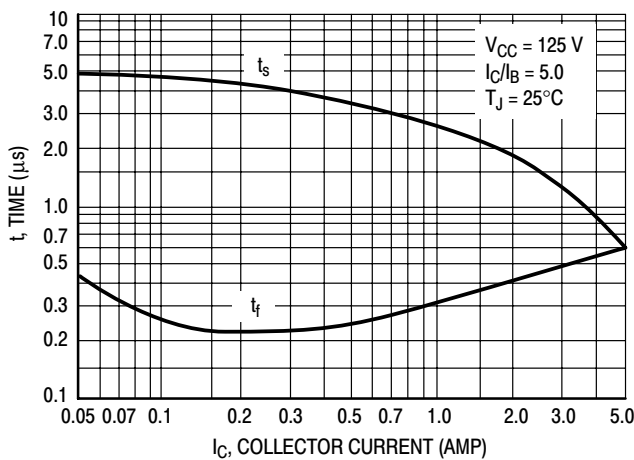


Figure 15. Turn-Off Time

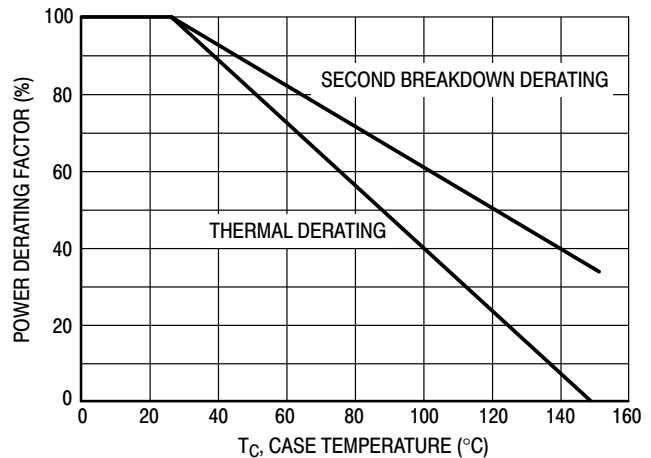


Figure 16. Power Derating



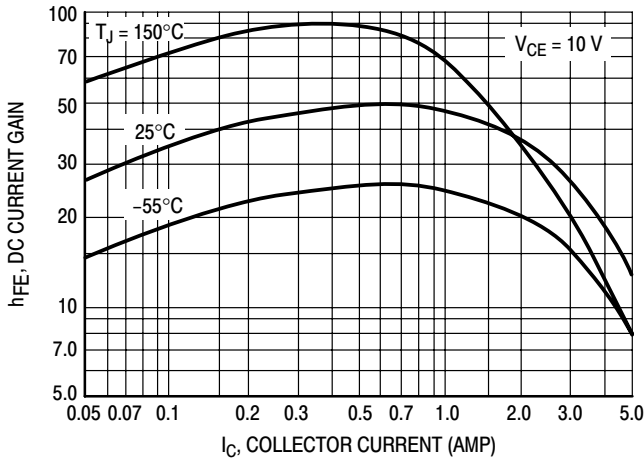


Figure 17. DC Current Gain

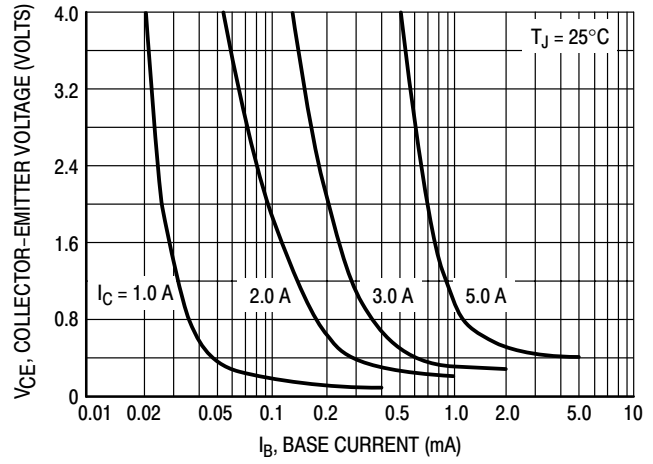


Figure 18. Collector Saturation Region

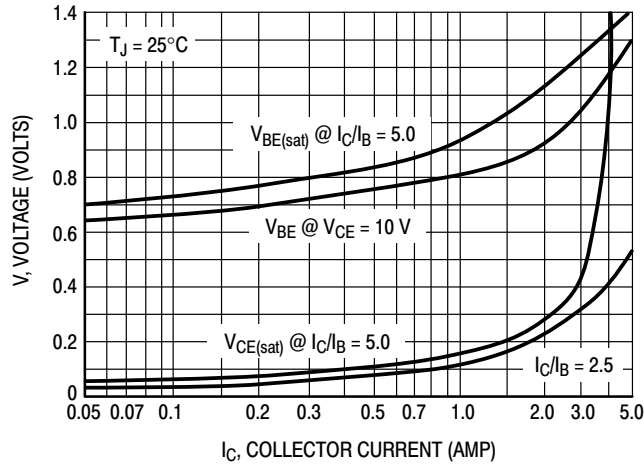


Figure 19. "On" Voltages

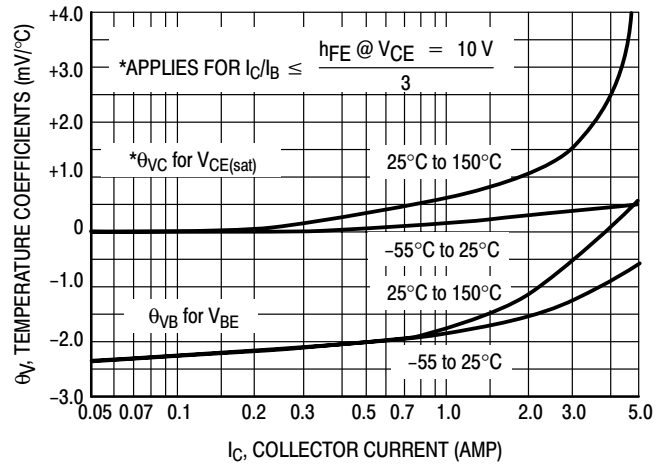


Figure 20. Temperature Coefficients

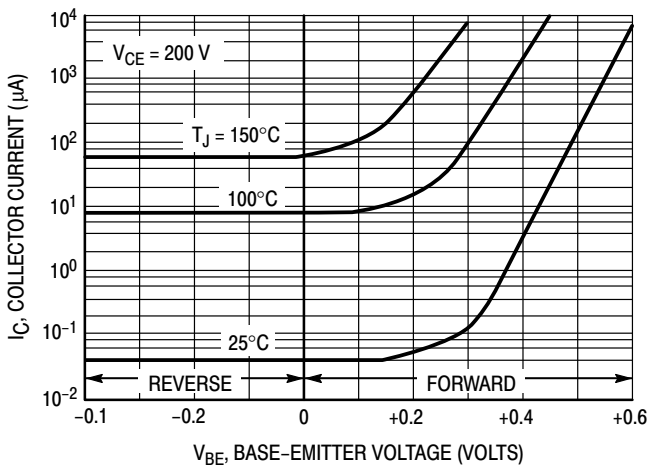


Figure 21. Collector Cutoff Region

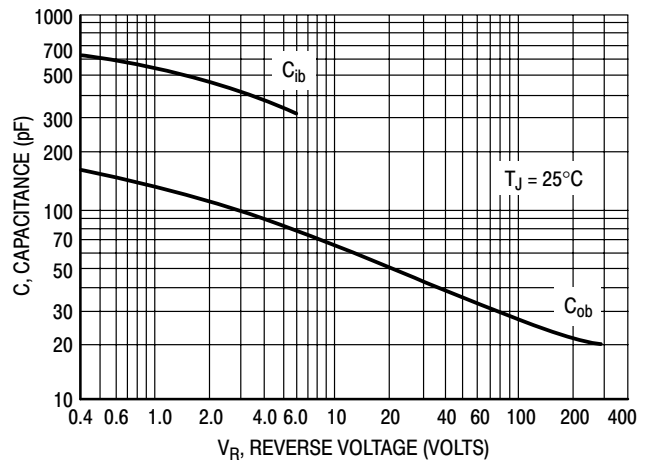


Figure 22. Capacitance

# Darlington Silicon Power Transistors

... designed for general-purpose amplifier and low speed switching applications.

- High DC Current Gain —  
 $h_{FE} = 3500$  (Typ) @  $I_C = 4$  Adc
- Collector–Emitter Sustaining Voltage — @ 200 mAdc  
 $V_{CEO(sus)} = 60$  Vdc (Min) — 2N6667  
 $= 80$  Vdc (Min) — 2N6668
- Low Collector–Emitter Saturation Voltage —  
 $V_{CE(sat)} = 2$  Vdc (Max) @  $I_C = 5$  Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package
- Complementary to 2N6387, 2N6388

**2N6667**  
**2N6668**

**PNP SILICON**  
**DARLINGTON**  
**POWER TRANSISTORS**  
**10 AMPERES**  
**60–80 VOLTS**  
**65 WATTS**

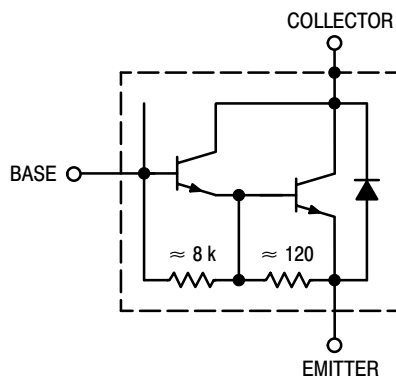
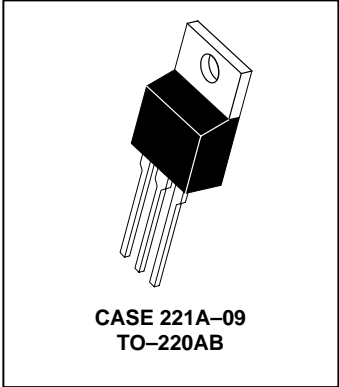


Figure 1. Darlington Schematic

**MAXIMUM RATINGS (1)**

Rating	Symbol	2N6667	2N6668	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	80	Vdc
Collector–Base Voltage	$V_{CB}$	60	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5		Vdc
Collector Current — Continuous — Peak	$I_C$	10 15		Adc
Base Current	$I_B$	250		mAdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	65 0.52		watts $W/^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2 0.016		Watts $W/^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C}$

(1) Indicates JEDEC Registered Data.

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^{\circ}C/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^{\circ}C/W$

**\*ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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**OFF CHARACTERISTICS**

Collector–Emitter Sustaining Voltage (2) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	2N6667 2N6668	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 80\text{ Vdc}$ , $I_B = 0$ )	2N6667 2N6668	$I_{CEO}$	— —	1 1	mAdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^{\circ}C$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^{\circ}C$ )	2N6667 2N6668 2N6667 2N6668	$I_{CEX}$	— — — —	300 300 3 3	$\mu\text{Adc}$  mAdc
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	5	mAdc

**ON CHARACTERISTICS (1)**

DC Current Gain ( $I_C = 5\text{ Adc}$ , $V_{CE} = 3\text{ Vdc}$ ) ( $I_C = 10\text{ Adc}$ , $V_{CE} = 3\text{ Vdc}$ )		$h_{FE}$	1000 100	20000 —	—
Collector–Emitter Saturation Voltage ( $I_C = 5\text{ Adc}$ , $I_B = 0.01\text{ Adc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )		$V_{CE(sat)}$	— —	2 3	Vdc
Base–Emitter Saturation Voltage ( $I_C = 5\text{ Adc}$ , $I_B = 0.01\text{ Adc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )		$V_{BE(sat)}$	— —	2.8 4.5	Vdc

**DYNAMIC CHARACTERISTICS**

Current Gain — Bandwidth Product ( $I_C = 1\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )		$ h_{fe} $	20	—	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1\text{ MHz}$ )		$C_{ob}$	—	200	pF
Small–Signal Current Gain ( $I_C = 1\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ , $f = 1\text{ kHz}$ )		$h_{fe}$	1000	—	—

\*Indicates JEDEC Registered Data

(2) Pulse Test: Pulse Width  $\leq 300\ \mu s$ , Duty Cycle  $\leq 2\%$ .

$R_B$  &  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS

$D_1$ , MUST BE FAST RECOVERY TYPES e.g.,

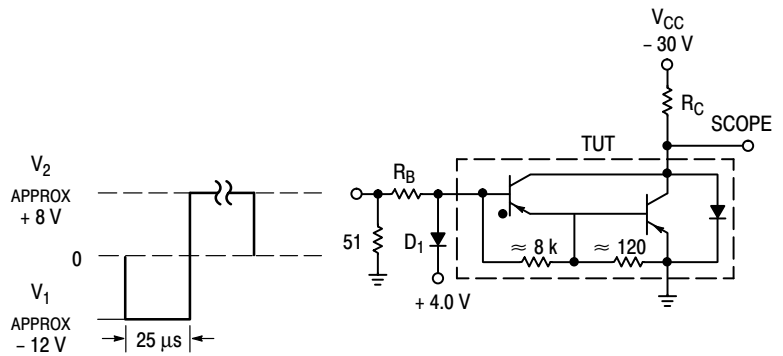
1N5825 USED ABOVE  $I_B \approx 100\text{ mA}$

MSD6100 USED BELOW  $I_B \approx 100\text{ mA}$

FOR  $t_d$  AND  $t_r$ ,  $D_1$  IS DISCONNECTED AND  $V_2 = 0$

$t_f$ ,  $t_r \leq 10\text{ ns}$

DUTY CYCLE = 1.0%



**Figure 2. Switching Times Test Circuit**

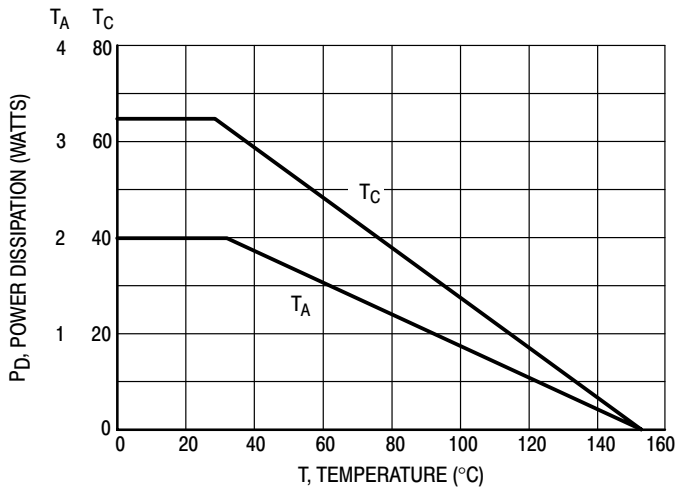


Figure 3. Power Derating

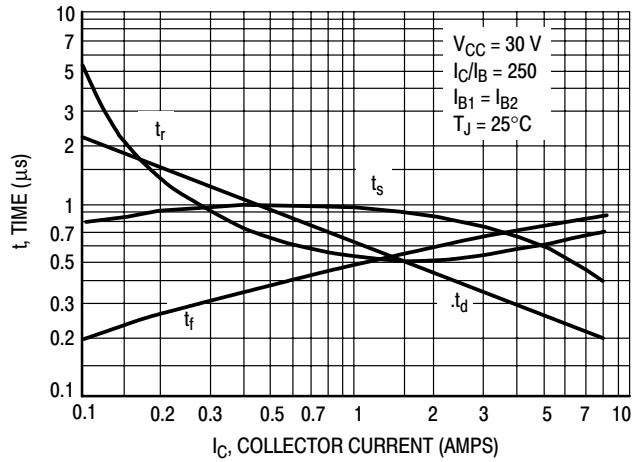


Figure 4. Typical Switching Times

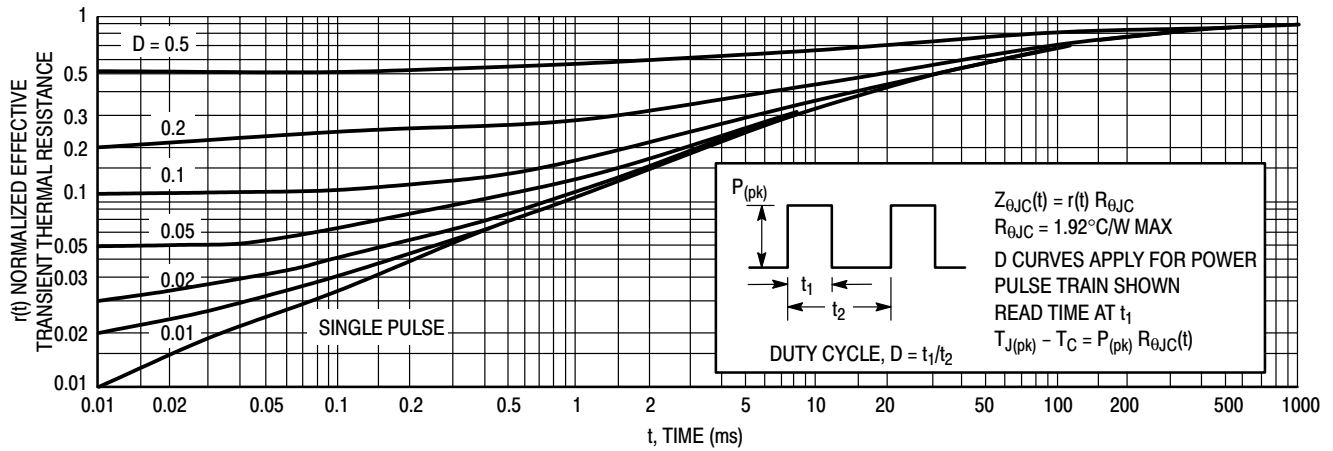


Figure 5. Thermal Response

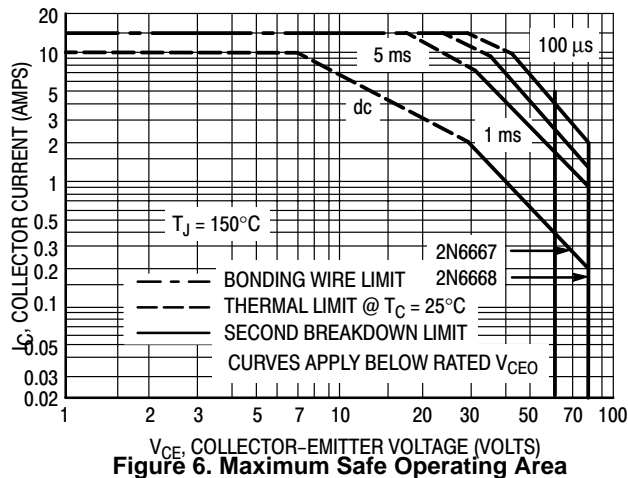


Figure 6. Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

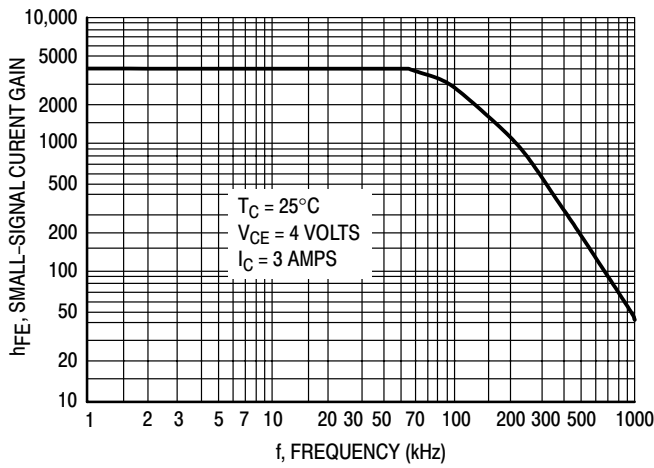


Figure 7. Typical Small-Signal Current Gain

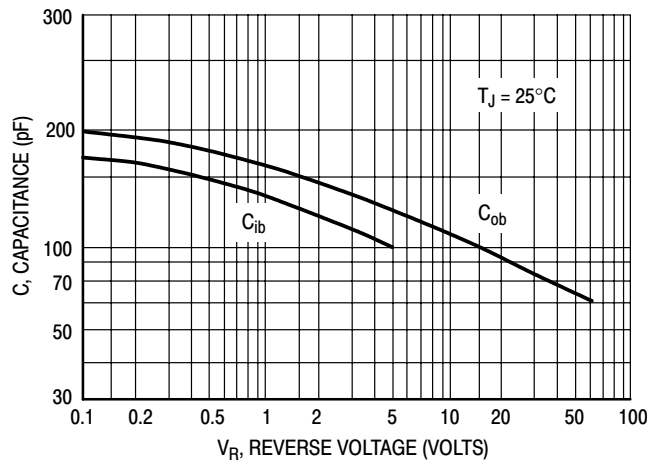


Figure 8. Typical Capacitance

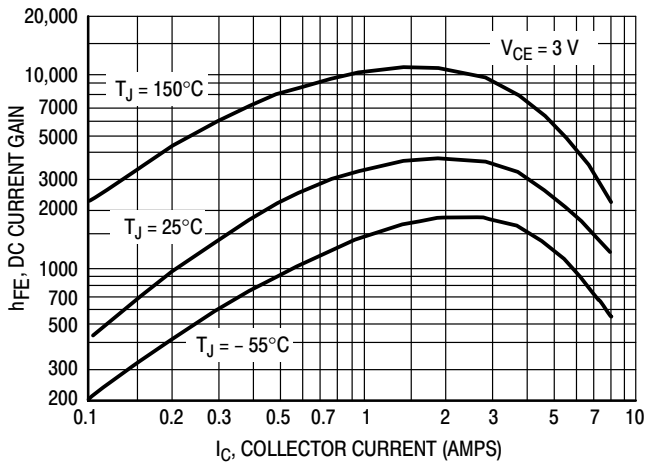


Figure 9. Typical DC Current Gain

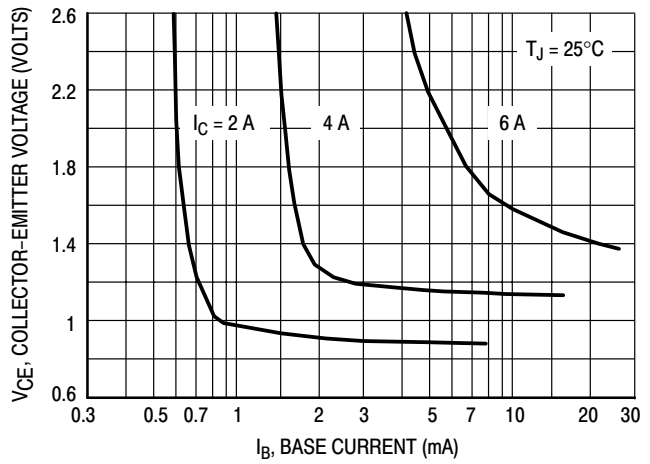


Figure 10. Typical Collector Saturation Region

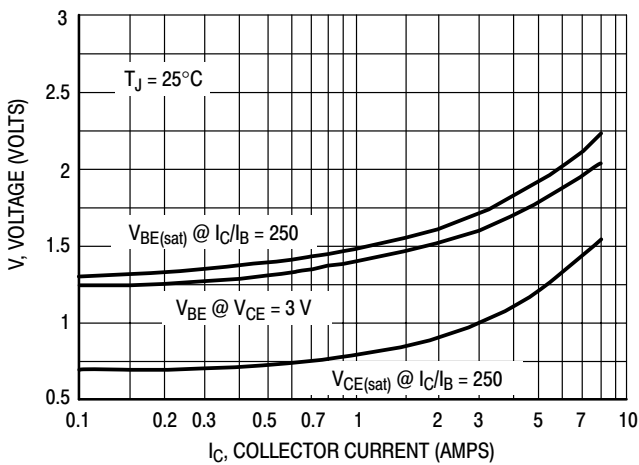


Figure 11. Typical "On" Voltages

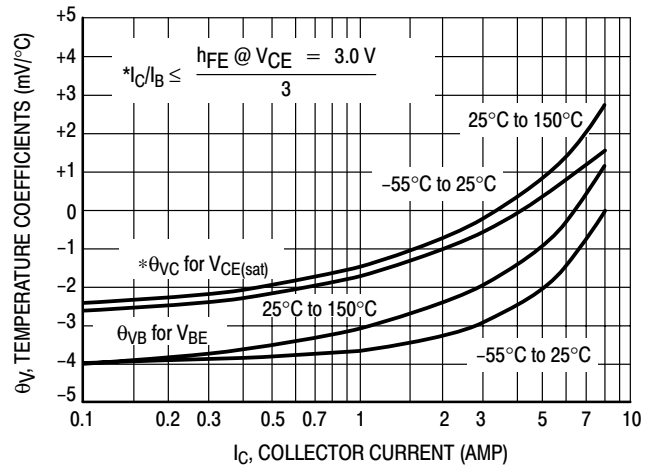


Figure 12. Typical Temperature Coefficients

# 2N6667 2N6668

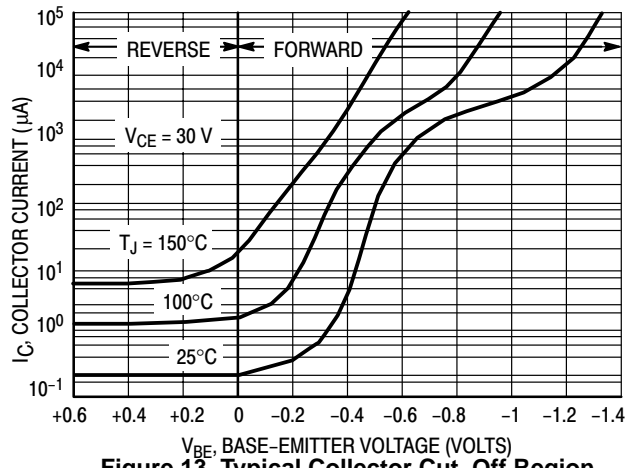


Figure 13. Typical Collector Cut-Off Region

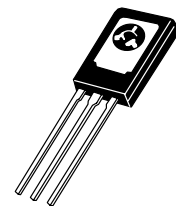
## Plastic Medium Power Silicon NPN Transistor

...designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain —  
 $h_{FE} = 40$  (Min) @  $I_C = 0.15$  Adc
- BD 135, 137, 139 are complementary with BD 136, 138, 140

**BD135**  
**BD137**  
**BD139**

**1.5 AMPERE**  
**POWER TRANSISTORS**  
**NPN SILICON**  
**45, 60, 80 VOLTS**  
**10 WATTS**



**CASE 77-09**  
**TO-225AA TYPE**

### MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	BD 135 BD 137 BD 139	45 60 80	Vdc
Collector-Base Voltage	$V_{CBO}$	BD 135 BD 137 BD 139	45 60 100	Vdc
Emitter-Base Voltage	$V_{EBO}$		5	Vdc
Collector Current	$I_C$		1.5	Adc
Base Current	$I_B$		0.5	Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$		1.25 10	Watts mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$		12.5 100	Watt mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$		-55 to +150	$^\circ\text{C}$

# BD135 BD137 BD139

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	10	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	100	$^{\circ}\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector–Emitter Sustaining Voltage* ( $I_C = 0.03 \text{ A dc}$ , $I_B = 0$ )	$BV_{CEO}^*$	BD 135 BD 137 BD 139	45 60 80	— — —	Vdc
Collector Cutoff Current ( $V_{CB} = 30 \text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 30 \text{ Vdc}$ , $I_E = 0$ , $T_C = 125^{\circ}\text{C}$ )	$I_{CBO}$		— —	0.1 10	$\mu\text{A dc}$
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$		—	10	$\mu\text{A dc}$
DC Current Gain ( $I_C = 0.005 \text{ A}$ , $V_{CE} = 2 \text{ V}$ ) ( $I_C = 0.15 \text{ A}$ , $V_{CE} = 2 \text{ V}$ ) ( $I_C = 0.5 \text{ A}$ , $V_{CE} = 2 \text{ V}$ )	$h_{FE}^*$		25 40 25	— 250 —	—
Collector–Emitter Saturation Voltage* ( $I_C = 0.5 \text{ A dc}$ , $I_B = 0.05 \text{ A dc}$ )	$V_{CE(sat)}^*$		—	0.5	Vdc
Base–Emitter On Voltage* ( $I_C = 0.5 \text{ A dc}$ , $V_{CE} = 2.0 \text{ Vdc}$ )	$V_{BE(on)}^*$		—	1	Vdc

\*Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

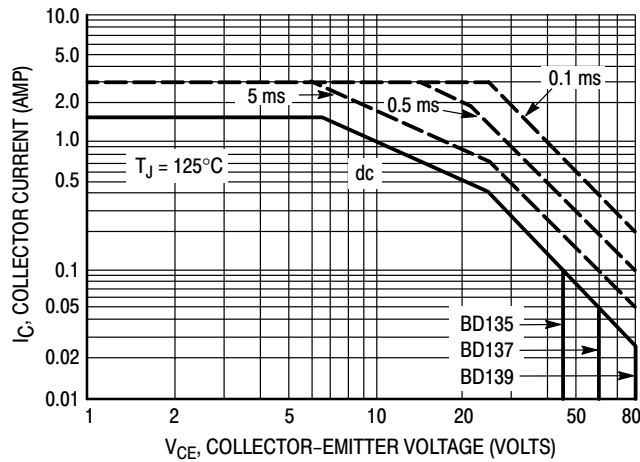


Figure 1. Active–Region Safe Operating Area



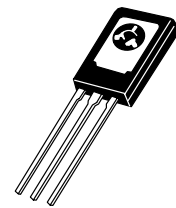
# Plastic Medium Power Silicon PNP Transistor

...designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain —  $h_{FE} = 40$  (Min) @  $I_C = 0.15$  Adc
- BD 136, 138, 140 are complementary with BD 135, 137, 139

**BD136**  
**BD138**  
**BD140**  
**BD140-10**

**1.5 AMPERE**  
**POWER TRANSISTORS**  
**PNP SILICON**  
**45, 60, 80 VOLTS**  
**10 WATTS**



**CASE 77-09**  
**TO-225AA TYPE**

## MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	BD 136 BD 138 BD 140	45 60 80	Vdc
Collector-Base Voltage	$V_{CBO}$	BD 136 BD 138 BD 140	45 60 100	Vdc
Emitter-Base Voltage	$V_{EBO}$		5	Vdc
Collector Current	$I_C$		1.5	Adc
Base Current	$I_B$		0.5	Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$		1.25 10	Watts mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$		12.5 100	Watt mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$		-55 to +150	$^\circ\text{C}$

# BD136 BD138 BD140 BD140-10

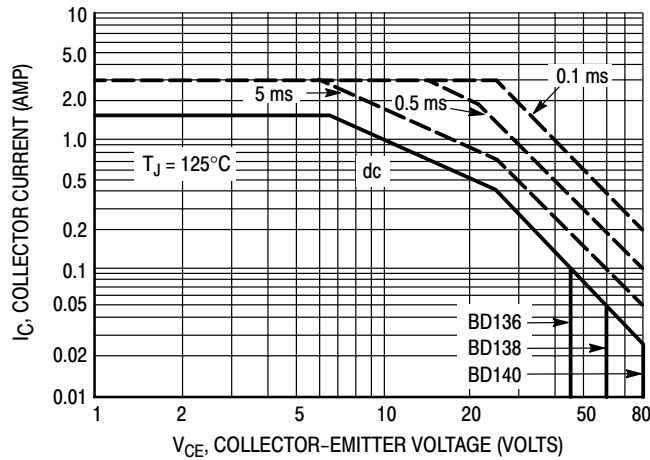
## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	10	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	100	$^{\circ}\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector–Emitter Sustaining Voltage* ( $I_C = 0.03 \text{ A dc}$ , $I_B = 0$ )	$BV_{CEO}$	BD 136 BD 138 BD 140	45 60 80	—	Vdc
Collector Cutoff Current ( $V_{CB} = 30 \text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 30 \text{ Vdc}$ , $I_E = 0$ , $T_C = 125^{\circ}\text{C}$ )	$I_{CBO}$		—	0.1 10	$\mu\text{A dc}$
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$		—	10	$\mu\text{A dc}$
DC Current Gain ( $I_C = 0.005 \text{ A}$ , $V_{CE} = 2 \text{ V}$ )  ( $I_C = 0.15 \text{ A}$ , $V_{CE} = 2 \text{ V}$ )  ( $I_C = 0.5 \text{ A}$ , $V_{CE} = 2 \text{ V}$ )	$h_{FE}^*$	ALL  BD140–10	25 40 63 25	— 250 160 —	—
Collector–Emitter Saturation Voltage* ( $I_C = 0.5 \text{ A dc}$ , $I_B = 0.05 \text{ A dc}$ )	$V_{CE(sat)}^*$		—	0.5	Vdc
Base–Emitter On Voltage* ( $I_C = 0.5 \text{ A dc}$ , $V_{CE} = 2.0 \text{ Vdc}$ )	$V_{BE(on)}^*$		—	1	Vdc

\*Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



**Figure 1. Active–Region Safe Operating Area**

# Plastic Medium Power NPN Silicon Transistor

... designed for power output stages for television, radio, phonograph and other consumer product applications.

- Suitable for Transformerless, Line-Operated Equipment
- Thermopad™ Construction Provides High Power Dissipation Rating for High Reliability

## BD159

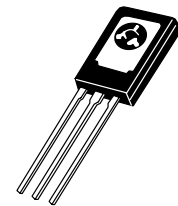
**0.5 AMPERE  
POWER TRANSISTOR  
NPN SILICON  
350 VOLTS  
20 WATTS**

### MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	$V_{CEO}$	350	Vdc
Collector–Base Voltage	$V_{CB}$	375	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous Peak	$I_C$	0.5 1.0	Adc
Base Current	$I_B$	0.25	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	6.25	$^\circ\text{C}/\text{W}$



**CASE 77-09  
TO-225AA TYPE**

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 1.0 \text{ mAdc}, I_B = 0$ )	$BV_{CEO}$	350	—	Vdc
Collector Cutoff Current (At rated voltage)	$I_{CBO}$	—	100	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = 5.0 \text{ Vdc}, I_C = 0$ )	$I_{EBO}$	—	100	$\mu\text{Adc}$

### ON CHARACTERISTICS

DC Current Gain ( $I_C = 50 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$ )	$h_{FE}$	30	240	—
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# BD159

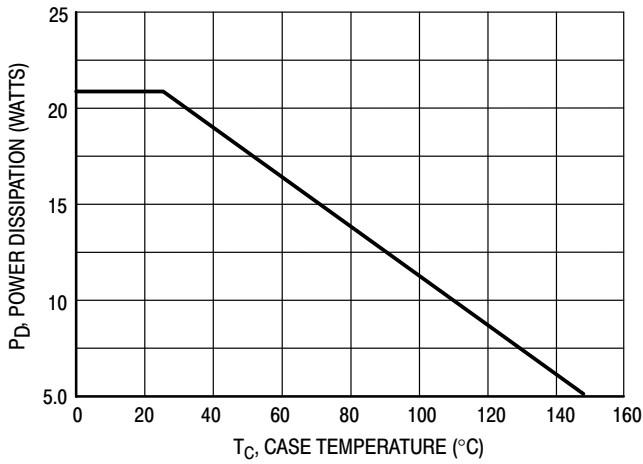


Figure 2. Power-Temperature Derating Curve

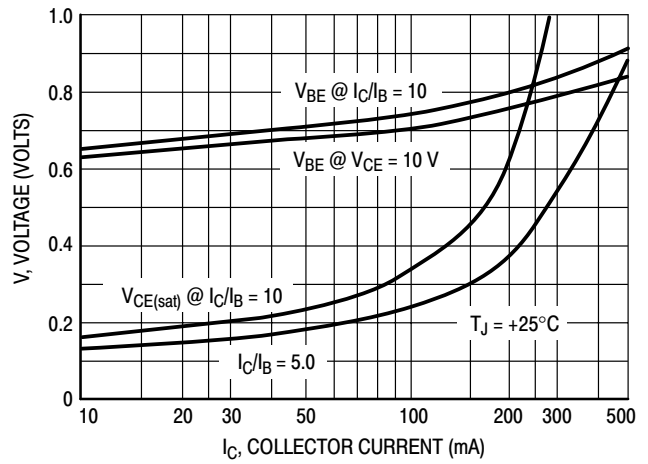


Figure 3. "On" Voltages

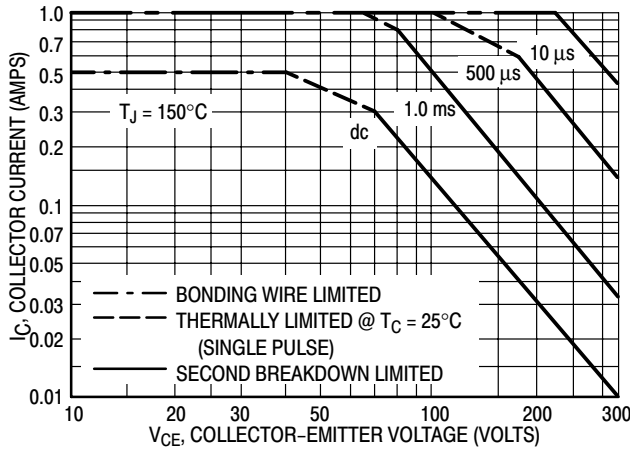


Figure 4. DC Safe Operating Area

The Safe Operating Area Curves indicate  $I_C - V_{CE}$  limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below, the maximum  $T_J$ , power-temperature derating must be observed for both steady state and pulse power conditions.

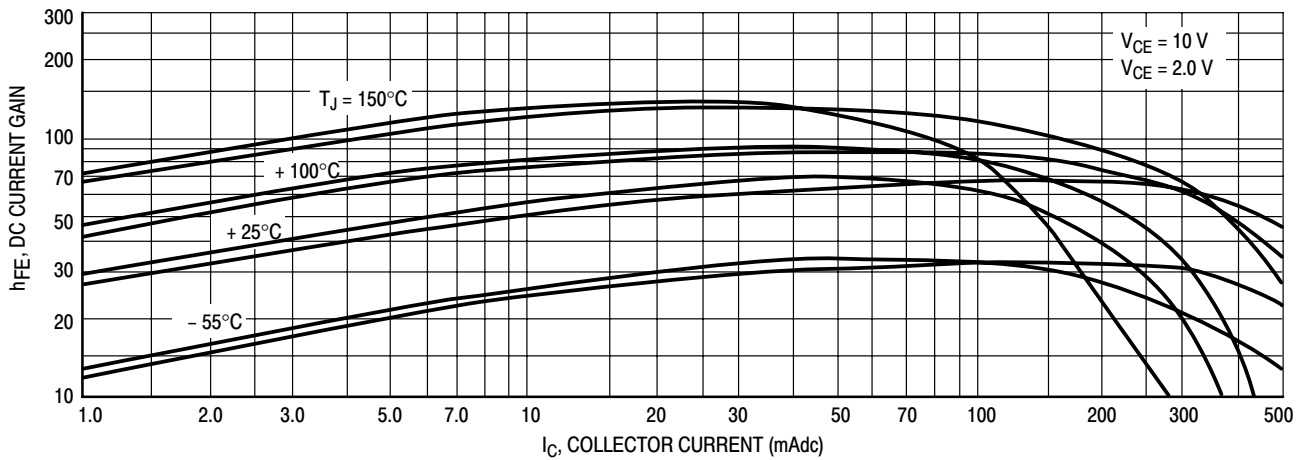


Figure 5. Current Gain

# Plastic Medium Power Silicon NPN Transistor

... designed for use in 5.0 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain —  $h_{FE} = 40$  (Min) @  $I_C = 0.15$  Adc
- BD179 is complementary with BD180

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Collector–Base Voltage	$V_{CBO}$	80	Vdc
Emitter–Base Voltage	$V_{EBO}$	5.0	Vdc
Collector Current	$I_C$	3.0	Adc
Base Current	$I_B$	1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	30 240	Watts mw/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	4.16	$^\circ\text{C/W}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

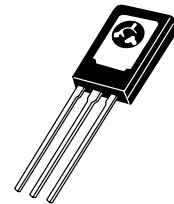
Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* ( $I_C = 0.1$ Adc, $I_B = 0$ )	$V_{(BR)CEO}$	80	—	Vdc
Collector Cutoff Current ( $V_{CB} = 80$ Vdc, $I_E = 0$ )	$I_{CBO}$	—	0.1	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0$ Vdc, $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc
DC Current Gain ( $I_C = 0.15$ A, $V_{CE} = 2.0$ V)      BD179–10 ( $I_C = 1.0$ A, $V_{CE} = 2.0$ V)      ALL	$h_{FE}$	63 15	160 —	
Collector–Emitter Saturation Voltage* ( $I_C = 1.0$ Adc, $I_B = 0.1$ Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter On Voltage* ( $I_C = 1.0$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Current–Gain – Bandwidth Product ( $I_C = 250$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	$f_T$	3.0	—	MHz

\*Pulse Test: Pulse Width  $\leq 300$  As, Duty Cycle  $\leq 2.0\%$ .

**BD179**  
**BD179-10**

**3.0 AMPERES**  
**POWER TRANSISTORS**  
**NPN SILICON**  
**80 VOLTS**  
**30 WATTS**

\*ON Semiconductor Preferred Device



**CASE 77–09**  
**TO–225AA TYPE**

The Safe Operating Area Curves indicate  $I_C - V_{CE}$  limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum  $T_J$ , power-temperature derating must be observed for both steady state and pulse power conditions.

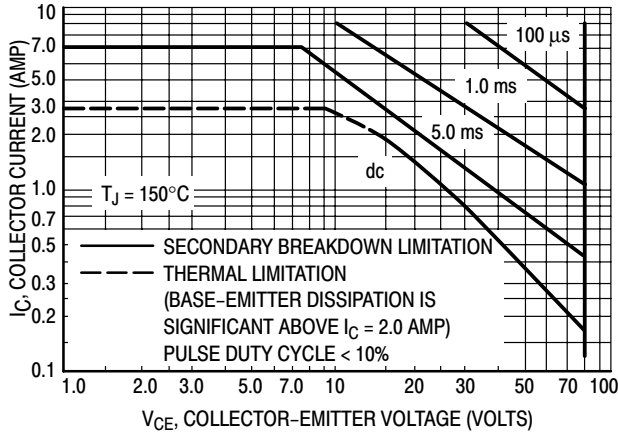


Figure 1. Active Region Safe Operating Area

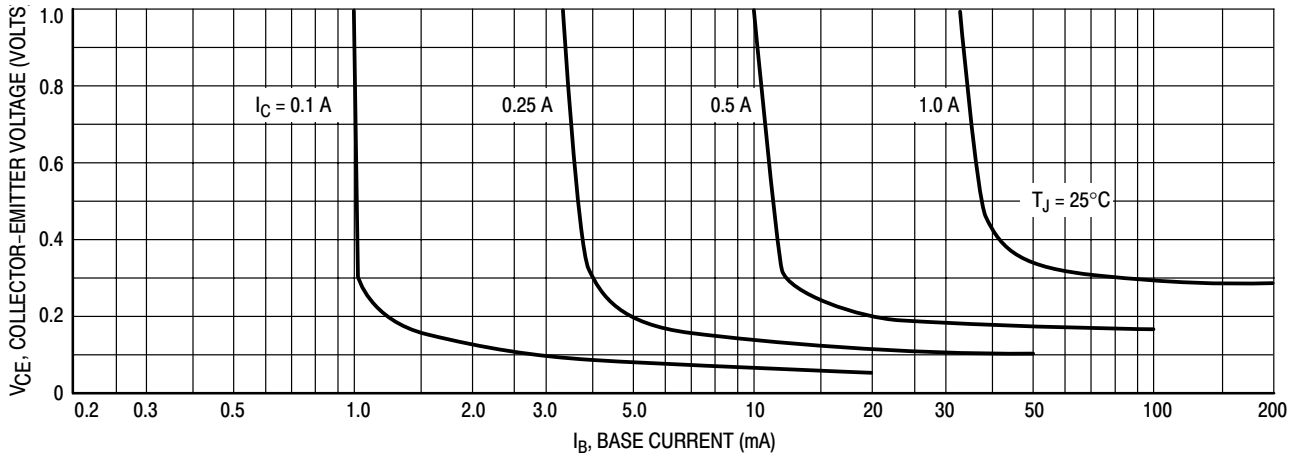


Figure 2. Collector Saturation Region

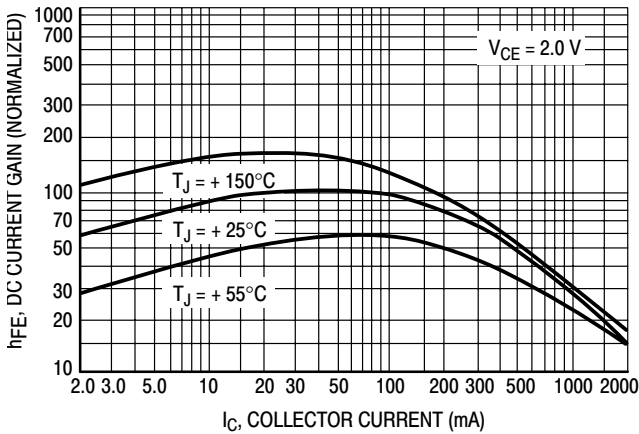


Figure 3. Current Gain

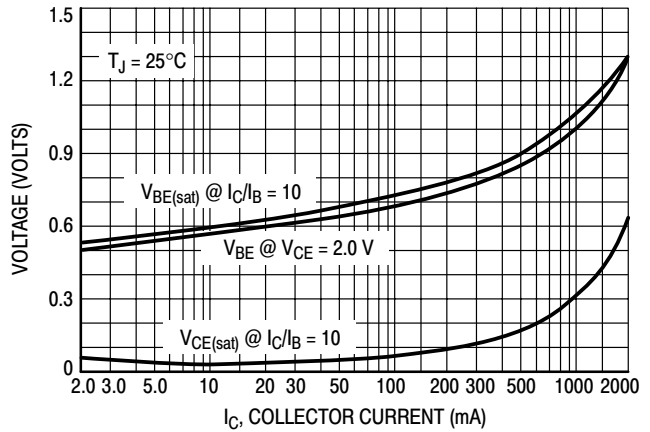


Figure 4. "On" Voltages

# BD179 BD179-10

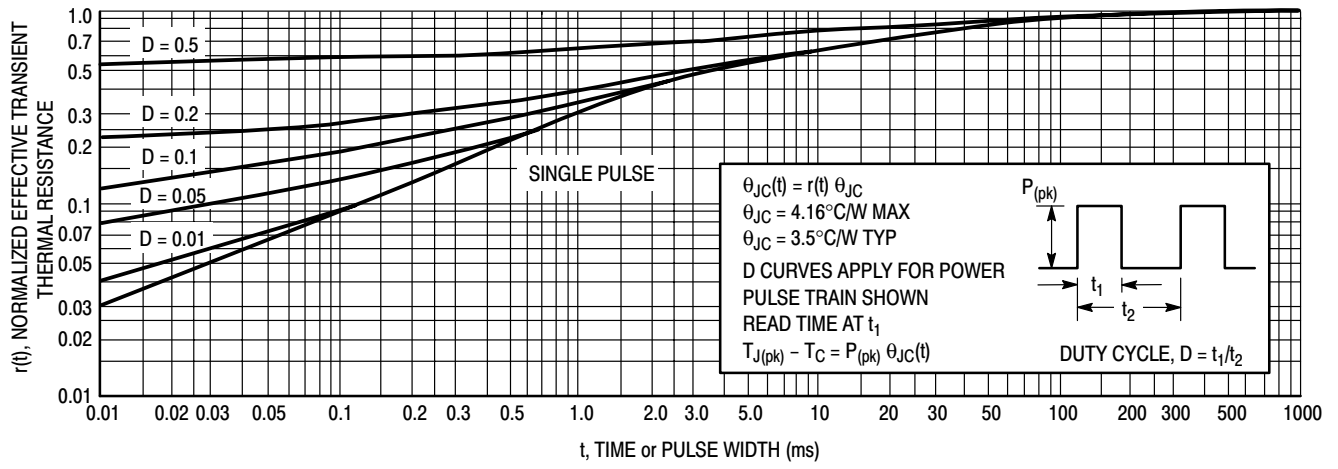


Figure 5. Thermal Response

# Plastic Medium Power Silicon PNP Transistor

... designed for use in 5.0 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain —  $h_{FE} = 40$  (Min) @  $I_C = 0.15$  Adc
- BD180 is complementary with BD179

## MAXIMUM RATINGS

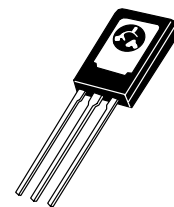
Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Collector–Base Voltage	$V_{CBO}$	80	Vdc
Emitter–Base Voltage	$V_{EBO}$	5.0	Vdc
Collector Current	$I_C$	3.0	Adc
Base Current	$I_B$	1.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	30 240	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	4.16	$^\circ\text{C/W}$

# BD180

3.0 AMPERES  
POWER TRANSISTOR  
PNP SILICON  
80 VOLTS  
30 WATTS



CASE 77-09  
TO-225AA TYPE

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* ( $I_C = 0.1$ Adc, $I_B = 0$ )	$V_{(BR)CEO}$	80	—	Vdc
Collector Cutoff Current ( $V_{CB} = 45$ Vdc, $I_E = 0$ ) ( $V_{CB} = 80$ Vdc, $I_E = 0$ )	$I_{CBO}$	— —	— 1.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0$ Vdc, $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc
DC Current Gain ( $I_C = 0.15$ A, $V_{CE} = 2.0$ V) ( $I_C = 1.0$ A, $V_{CE} = 2.0$ V)	$h_{FE}$	40 15	250 —	—
Collector–Emitter Saturation Voltage* ( $I_C = 1.0$ Adc, $I_B = 0.1$ Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter On Voltage* ( $I_C = 1.0$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Current–Gain — Bandwidth Product ( $I_C = 250$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	$f_T$	3.0	—	MHz

\*Pulse Test: Pulse Width  $\leq 300$   $\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



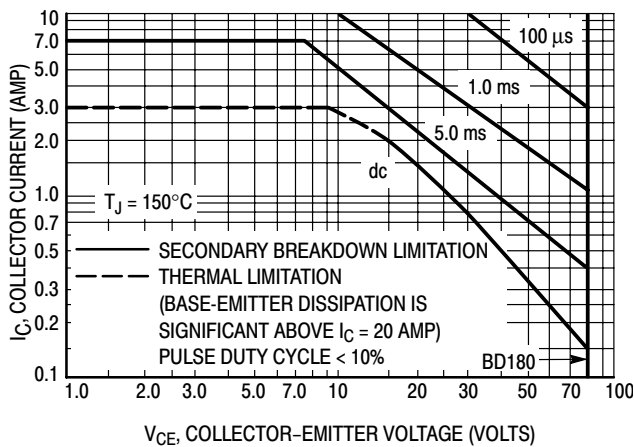


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate  $I_C - V_{CE}$  limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum  $T_J$ , power-temperature derating must be observed for both steady state and pulse power conditions.

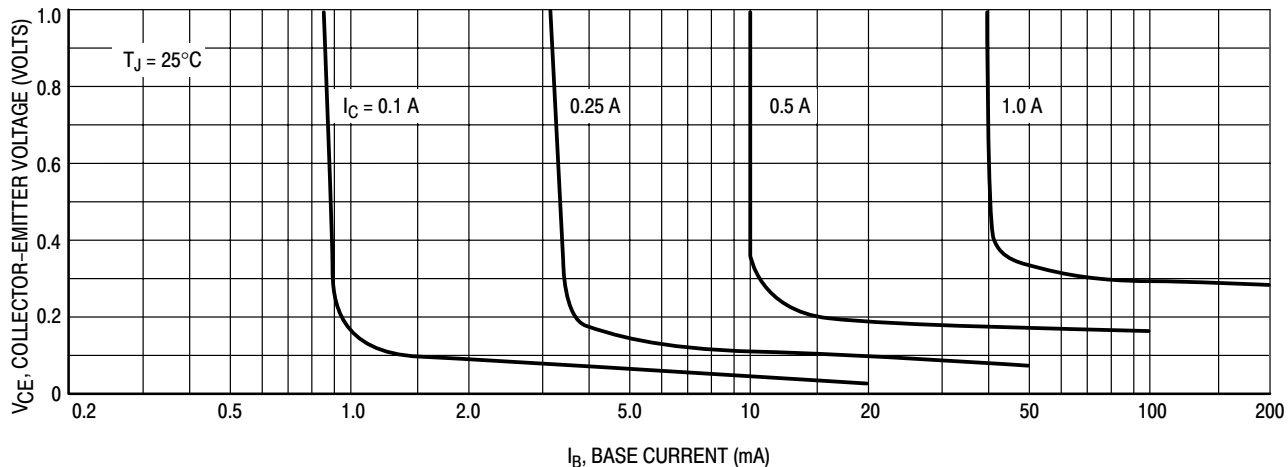


Figure 2. Collector Saturation Region

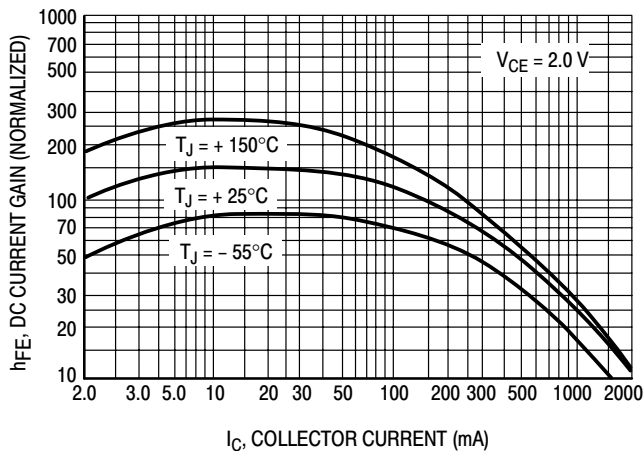


Figure 3. Current Gain

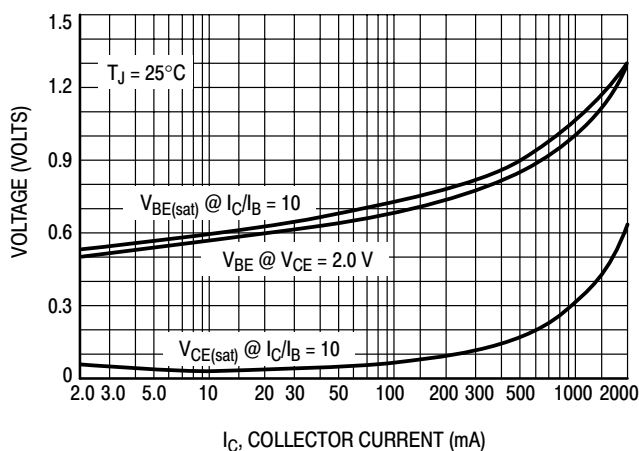


Figure 4. "On" Voltages

# BD180

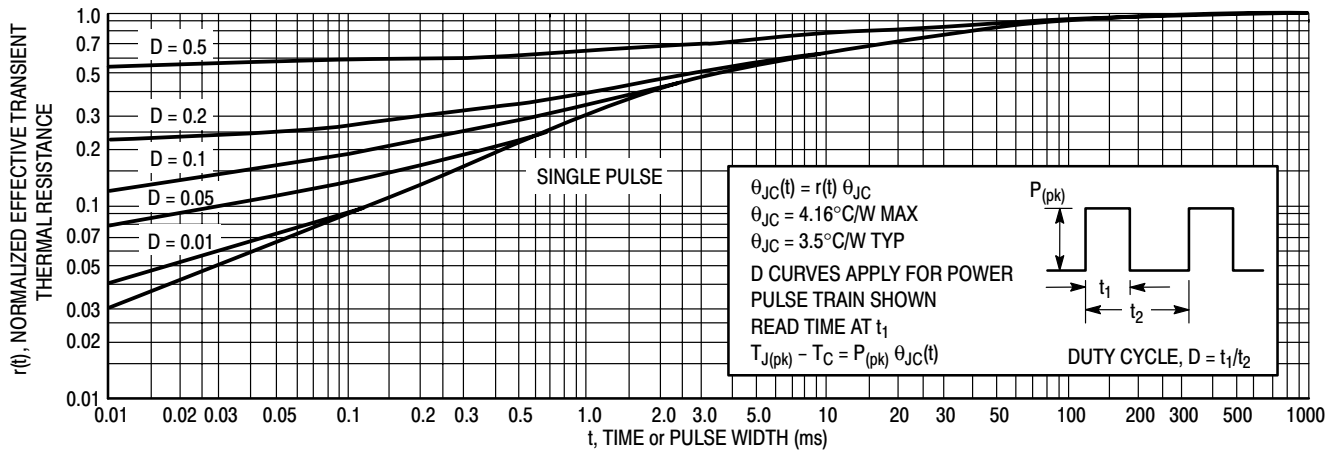


Figure 5. Thermal Response

# Plastic Medium Power Silicon NPN Transistor

... designed for use in 5.0 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain —  
 $h_{FE} = 40$  (Min) @  $I_C = 0.15$  Adc

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Collector–Base Voltage	$V_{CBO}$	100	Vdc
Emitter–Base Voltage	$V_{EBO}$	5.0	Vdc
Collector Current	$I_C$	2.0	Adc
Base Current	$I_B$	1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	25	Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	5.0	$^\circ\text{C/W}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

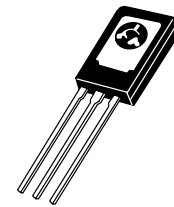
Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* ( $I_C = 0.1$ Adc, $I_B = 0$ )	$V_{(BR)CEO}$	80	—	Vdc
Collector Cutoff Current ( $V_{CB} = 100$ Vdc, $I_E = 0$ )	$I_{CBO}$	—	0.1	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0$ Vdc, $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc
DC Current Gain ( $I_C = 0.15$ A, $V_{CE} = 2.0$ V) ( $I_C = 1.0$ A, $V_{CE} = 2.0$ V)	$h_{FE1}$ $h_{FE2}$	40 25	— —	
Collector–Emitter Saturation Voltage* ( $I_C = 1.0$ Adc, $I_B = 0.1$ Adc)	$V_{CE(sat)}$	—	0.6	Vdc
Base–Emitter On Voltage* ( $I_C = 1.0$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Current–Gain — Bandwidth Product ( $I_C = 250$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	$f_T$	3.0	—	MHz

\*Pulse Test: Pulse Width  $\leq 300$   $\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

**NPN  
BD237  
PNP  
BD238**

\*ON Semiconductor Preferred Device

**2.0 AMPERES  
POWER TRANSISTORS  
NPN SILICON  
80 VOLTS  
25 WATTS**



**CASE 77-09  
TO-225AA TYPE**

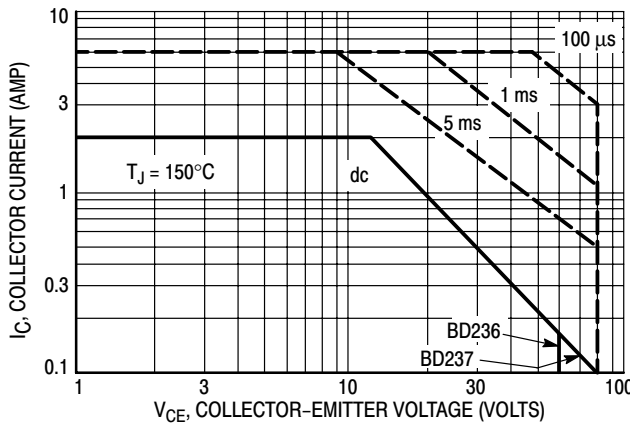


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate  $I_C - V_{CE}$  limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum  $T_J$ , power-temperature derating must be observed for both steady state and pulse power conditions.

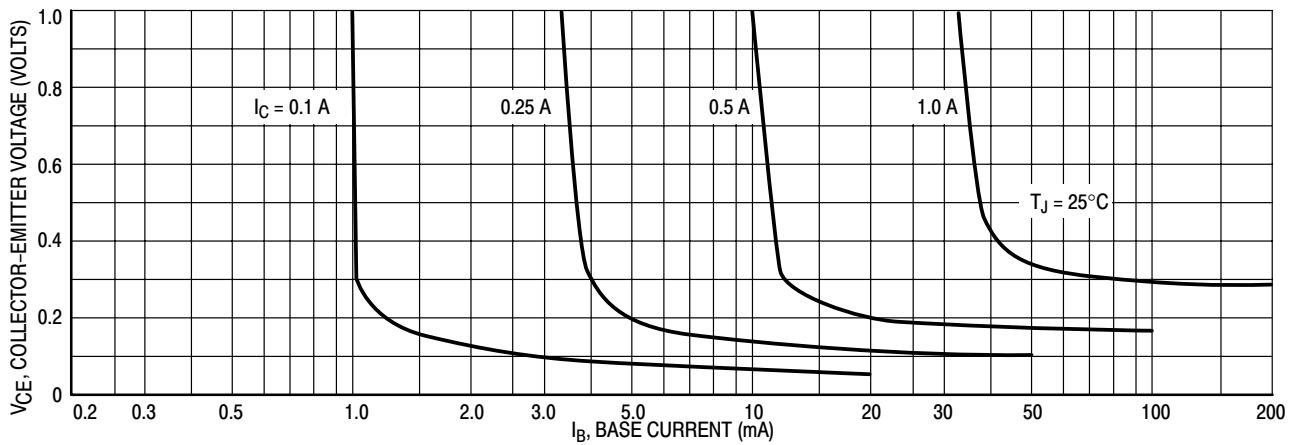


Figure 2. Collector Saturation Region

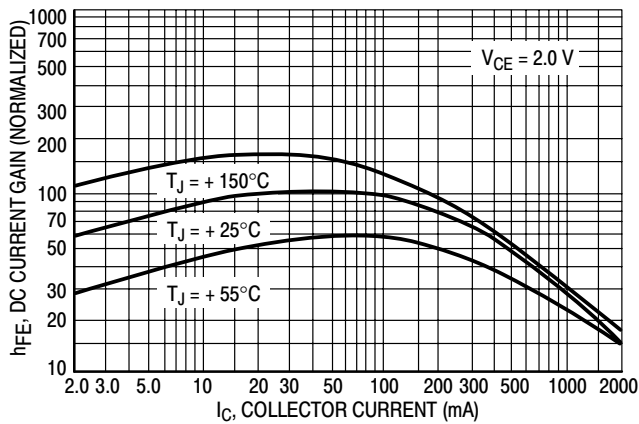


Figure 3. Current Gain

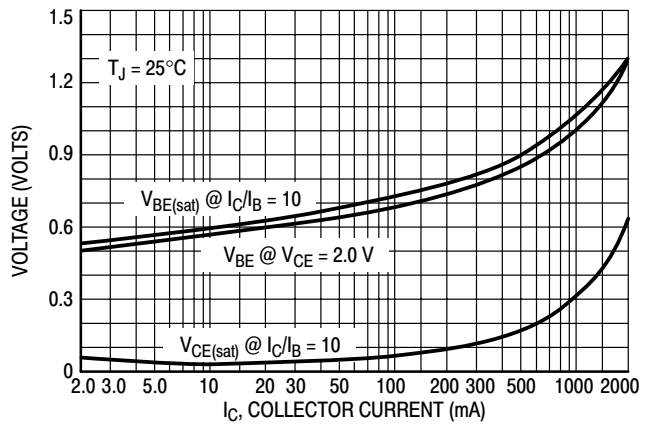
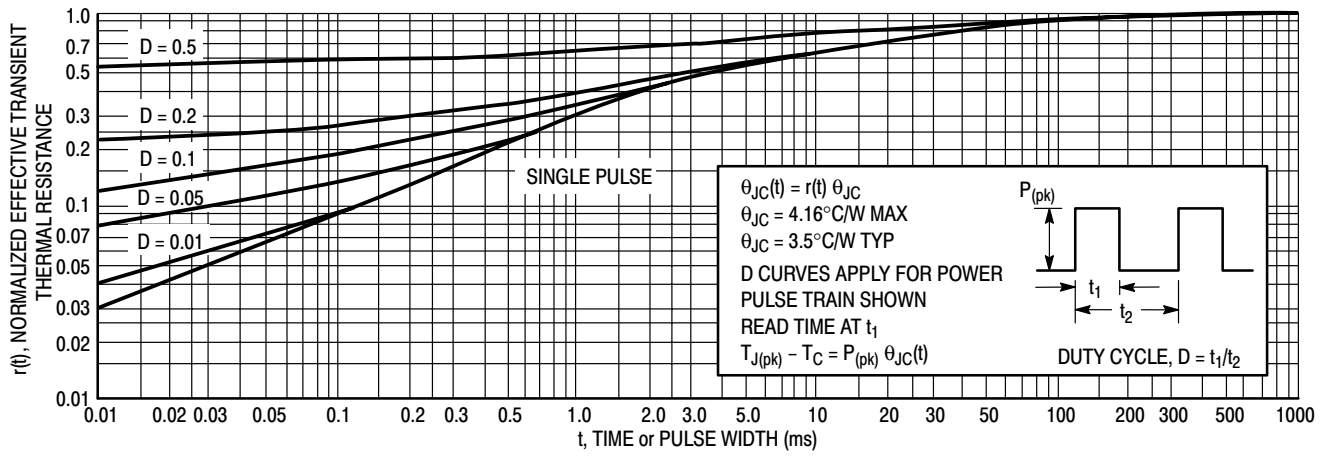


Figure 4. "On" Voltages

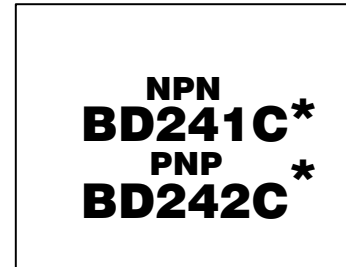
# BD238



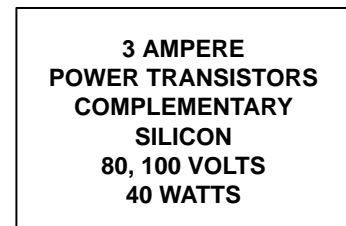
# Complementary Silicon Plastic Power Transistors

... designed for use in general purpose amplifier and switching applications.

- Collector–Emitter Saturation Voltage —  
 $V_{CE} = 1.2 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- Collector–Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 100 \text{ Vdc (Min.) BD241C, BD242C}$
- High Current Gain — Bandwidth Product  
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 500 \text{ mAdc}$
- Compact TO–220 AB Package

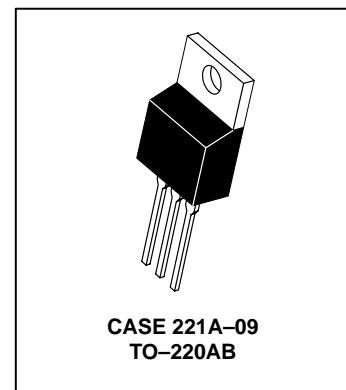


\*ON Semiconductor Preferred Device



## MAXIMUM RATINGS

Rating	Symbol	BD241C BD242C	Unit
Collector–Emitter Voltage	$V_{CEO}$	100	Vdc
Collector–Emitter Voltage	$V_{CES}$	115	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous Peak	$I_C$	3.0 5.0	Adc Adc
Base Current	$I_B$	1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.32	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$



## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	$^\circ\text{C/W}$

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

## BD241C BD242C

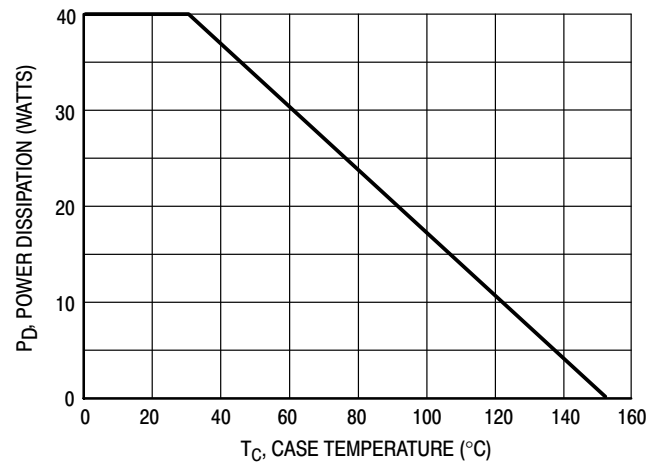


Figure 1. Power Derating

# BD241C BD242C

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage <sup>1</sup> ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	BD241C, BD242C $V_{CEO}$	100		Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	BD241C, BD242C $I_{CEO}$		0.3	mAdc
Collector Cutoff Current ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB} = 0$ )	BD241C, BD242C $I_{CES}$		200	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$		1.0	mAdc
<b>ON CHARACTERISTICS<sup>1</sup></b>				
DC Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	25 10		
Collector–Emitter Saturation Voltage ( $I_C = 3.0\text{ Adc}$ , $I_B = 600\text{ Adc}$ )	$V_{CE(sat)}$		1.2	Vdc
Base–Emitter On Voltage ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$		1.8	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current Gain – Bandwidth Product <sup>2</sup> ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )	$f_T$	3.0		MHz
Small–Signal Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ kHz}$ )	$h_{fe}$	20		

<sup>1</sup> Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

<sup>2</sup>  $f_T = |h_{fe}| \cdot f_{test}$ .

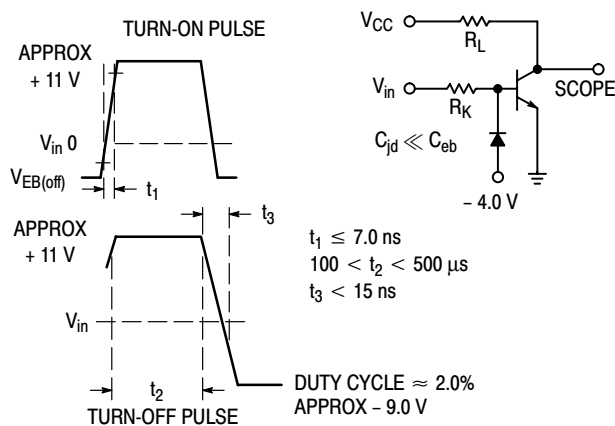


Figure 2. Switching Time Equivalent Circuit

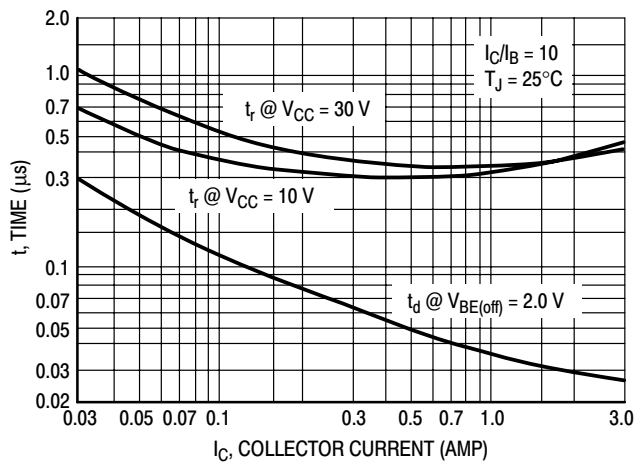


Figure 3. Turn–On Time



# BD241C BD242C

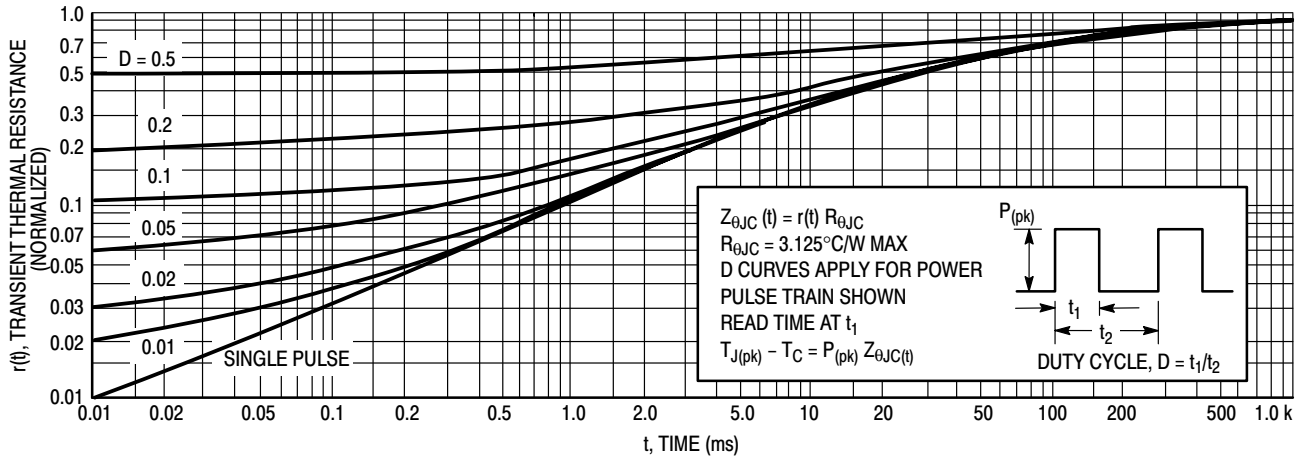


Figure 4. Thermal Response

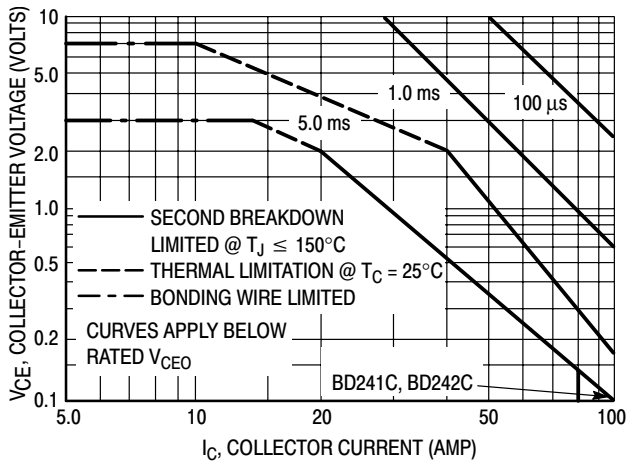


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ}C$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}C$ ,  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

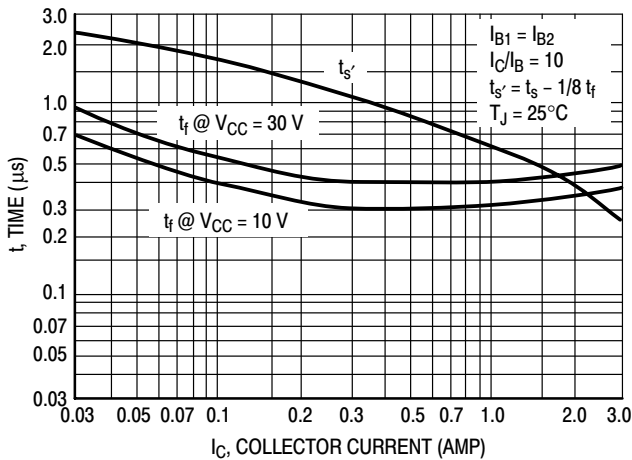


Figure 6. Turn-Off Time

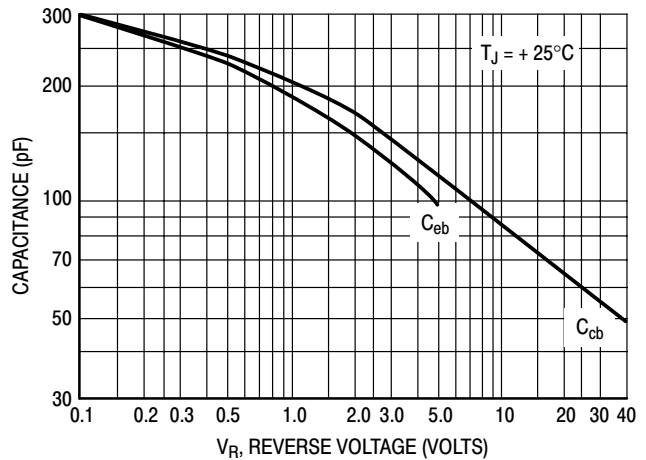
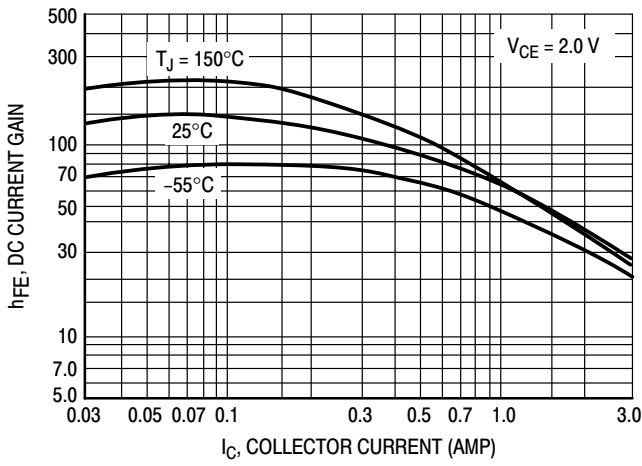
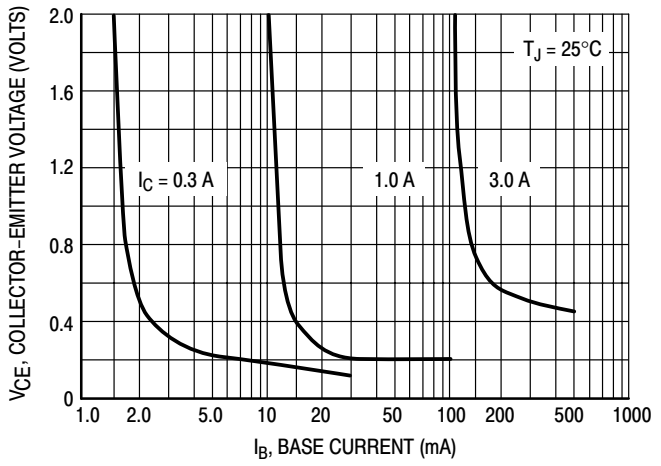


Figure 7. Capacitance

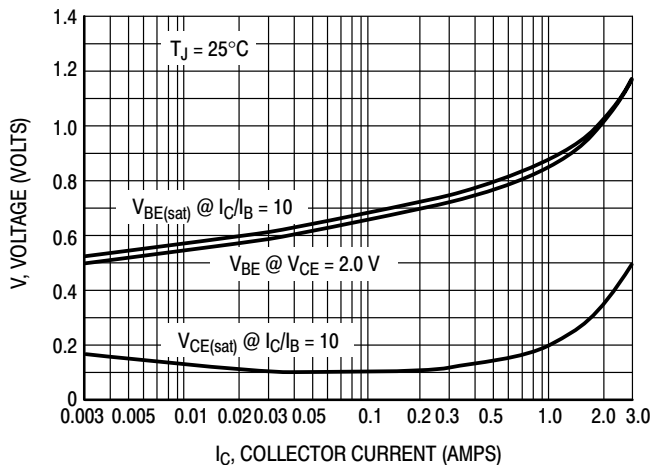
# BD241C BD242C



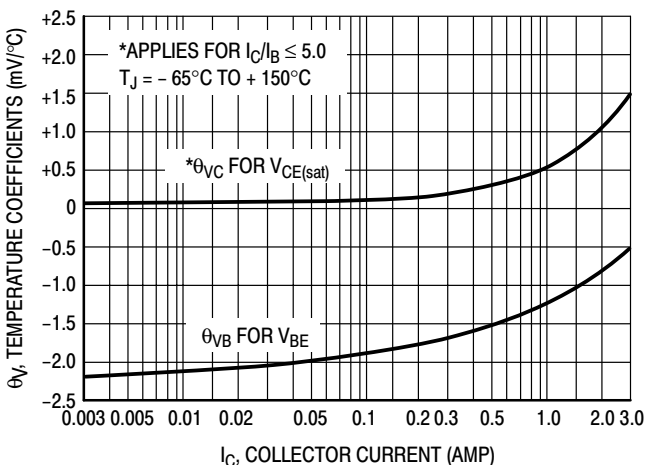
**Figure 8. DC Current Gain**



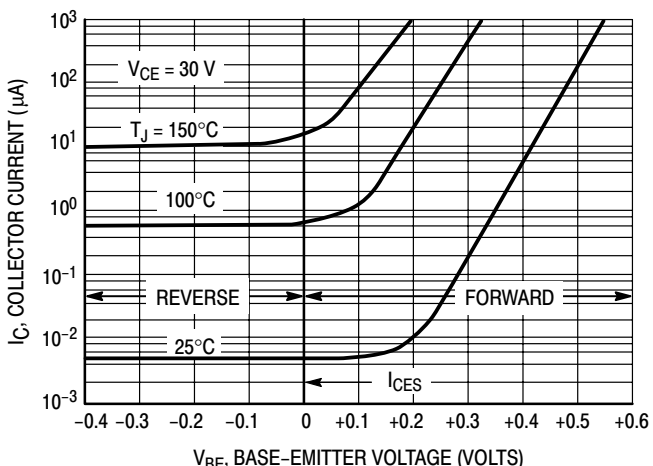
**Figure 9. Collector Saturation Region**



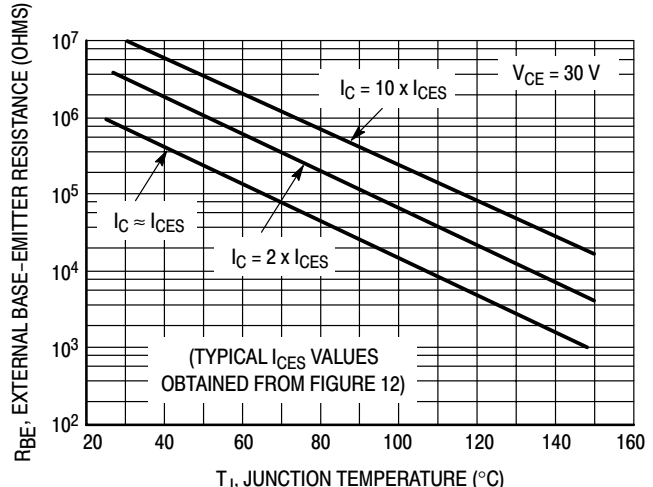
**Figure 10. "On" Voltages**



**Figure 11. Temperature Coefficients**



**Figure 12. Collector Cut-Off Region**



**Figure 13. Effects of Base-Emitter Resistance**

# Complementary Silicon Plastic Power Transistors

... designed for use in general purpose amplifier and switching applications.

- Collector – Emitter Saturation Voltage —  
 $V_{CE(sat)} = 1.5 \text{ Vdc (Max) @ } I_C = 6.0 \text{ Adc}$
- Collector Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 80 \text{ Vdc (Min) — BD243B, BD244B}$   
 $= 100 \text{ Vdc (Min) — BD243C, BD244C}$
- High Current Gain Bandwidth Product  
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 500 \text{ mA}$
- Compact TO–220 AB Package

## MAXIMUM RATINGS

Rating	Symbol	BD243B BD244B	BD243C BD244C	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	100	Vdc
Collector–Base Voltage	$V_{CB}$	80	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous Peak	$I_C$	6 10		A
Base Current	$I_B$	2.0		A
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	65 0.52		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C/W}$

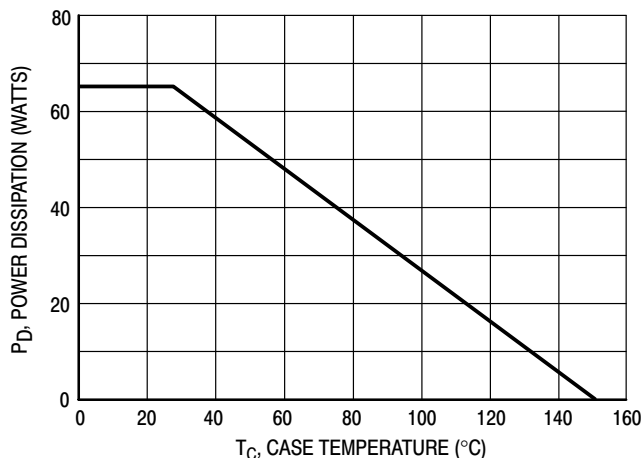
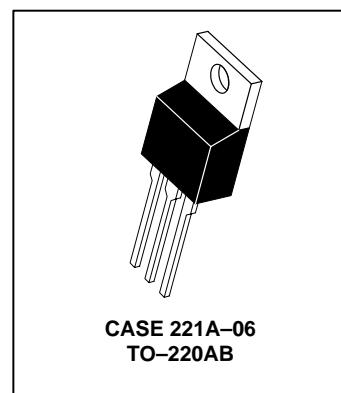


Figure 1. Power Derating

**NPN**  
**BD243B**  
  
**BD243C\***  
**PNP**  
**BD244B**  
  
**BD244C\***

\*ON Semiconductor Preferred Device

**6 AMPERE**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**80–100 VOLTS**  
**65 WATTS**



# BD243B BD243C BD244B BD244C

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	80 100	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	0.7	mAdc
Collector Cutoff Current ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB} = 0$ ) ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB} = 0$ )	$I_{CES}$	— —	400 400	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc

### ON CHARACTERISTICS (1)

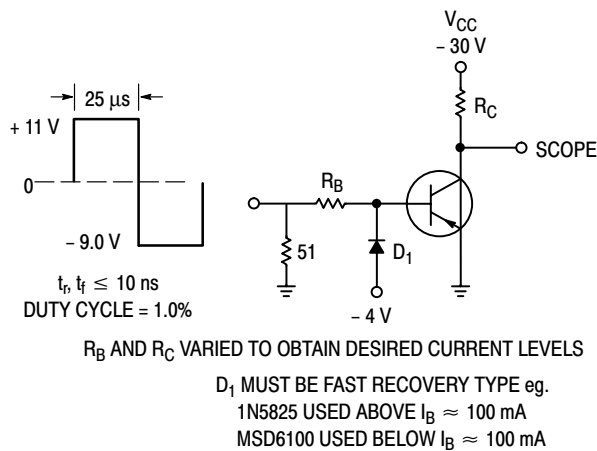
DC Current Gain ( $I_C = 0.3\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	30 15	— —	—
Collector–Emitter Saturation Voltage ( $I_C = 6.0\text{ Adc}$ , $I_B = 1.0\text{ Adc}$ )	$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter On Voltage ( $I_C = 6.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	2.0	Vdc

### DYNAMIC CHARACTERISTICS

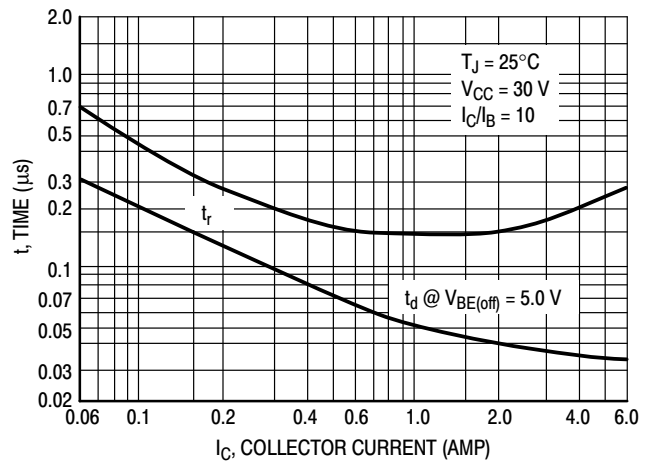
Current–Gain — Bandwidth Product (2) ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	3.0	—	MHz
Small–Signal Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	20	—	—

(1) Pulse Test: Pulsewidth  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

(2)  $f_T = h_{fe} \cdot f_{test}$



**Figure 2. Switching Time Test Circuit**



**Figure 3. Turn–On Time**

BD243B BD243C BD244B BD244C

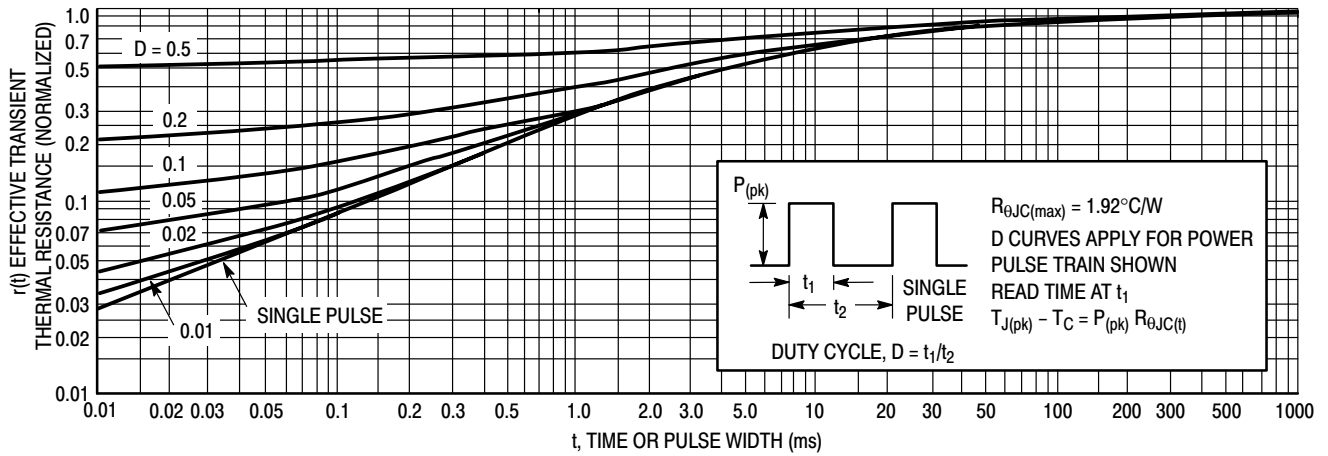


Figure 4. Thermal Response

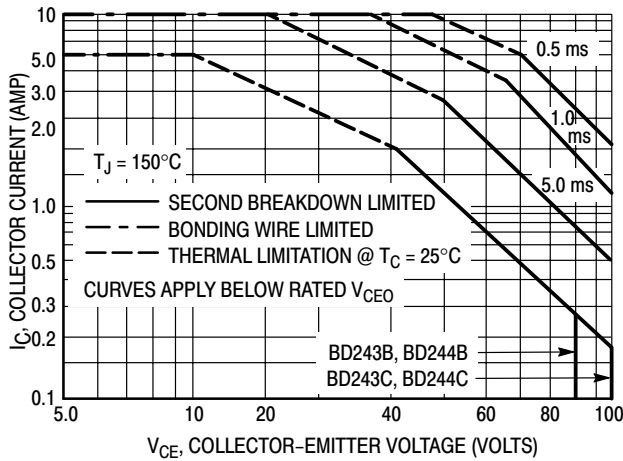


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

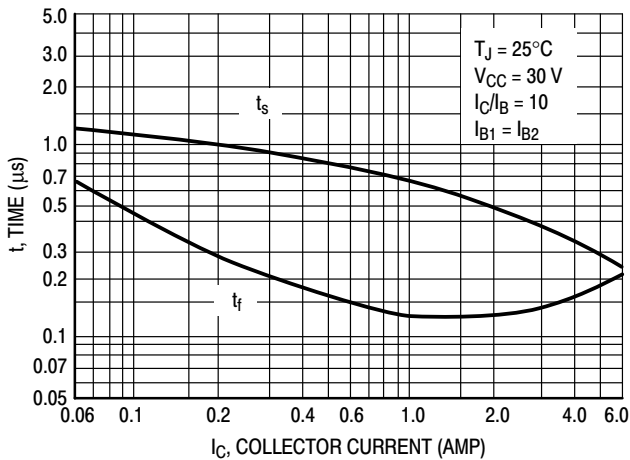


Figure 6. Turn-Off Time

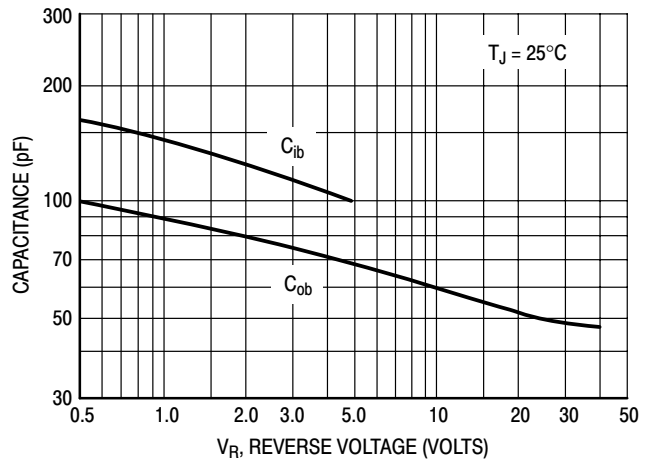


Figure 7. Capacitance

BD243B BD243C BD244B BD244C

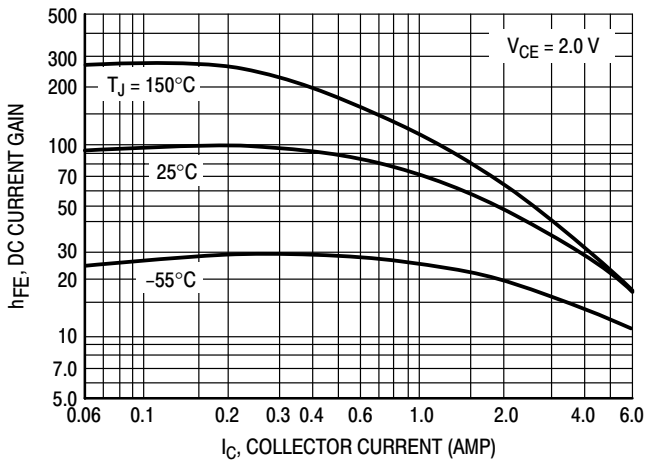


Figure 8. DC Current Gain

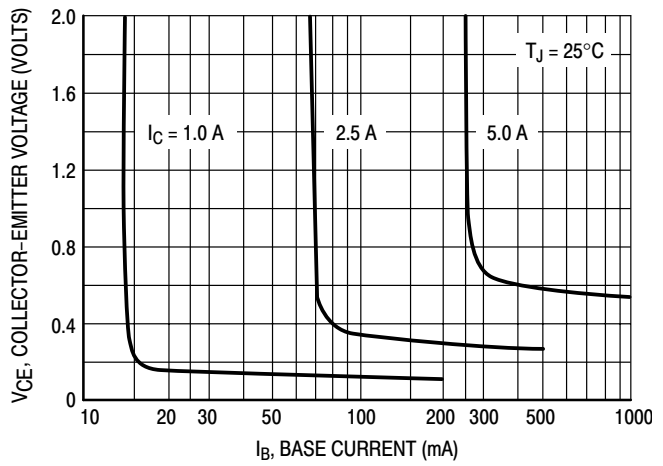


Figure 9. Collector Saturation Region

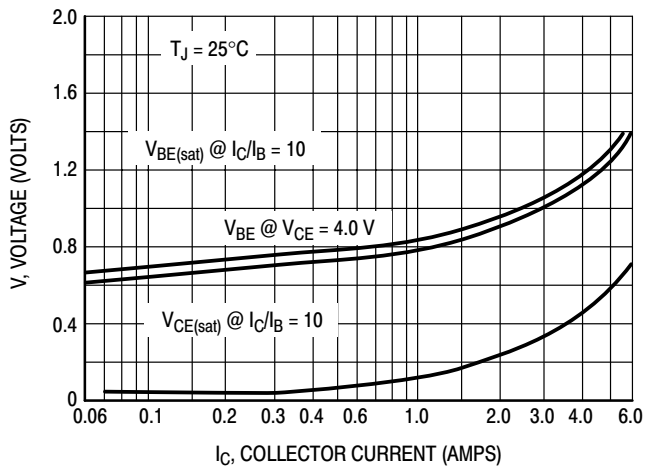


Figure 10. "On" Voltages

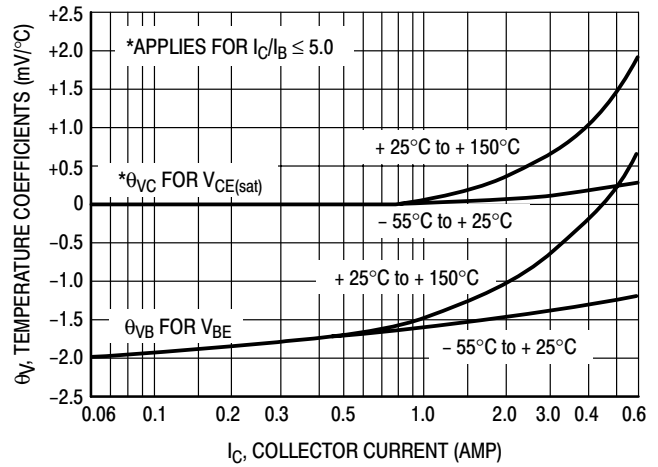


Figure 11. Temperature Coefficients

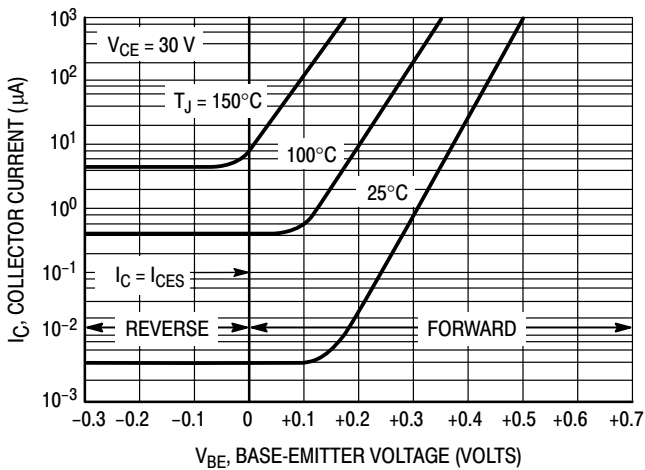


Figure 12. Collector Cut-Off Region

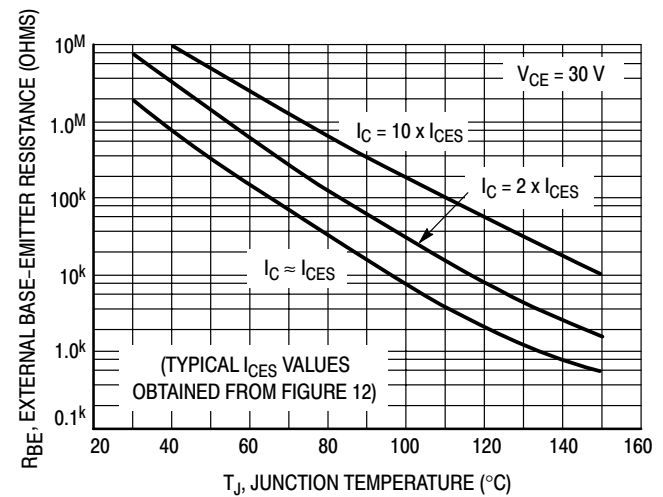


Figure 13. Effects of Base-Emitter Resistance

# Plastic Medium Power Silicon NPN Transistor

... for amplifier and switching applications. Complementary types are BD438 and BD442.

**BD437  
BD439  
BD441**

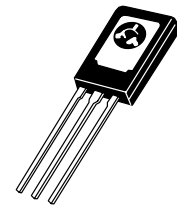
**4.0 AMPERES  
POWER TRANSISTORS  
NPN SILICON**

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	BD437 BD439 BD441	$V_{CEO}$ 45 60 80	Vdc
Collector–Base Voltage	BD437 BD439 BD441	$V_{CBO}$ 45 60 80	Vdc
Emitter–Base Voltage		$V_{EBO}$ 5.0	Vdc
Collector Current		$I_C$ 4.0	Adc
Base Current		$I_B$ 1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$		$P_D$ 36 288	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range		$T_J, T_{stg}$ –55 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	3.5	$^\circ\text{C}/\text{W}$



**CASE 77–09  
TO–225AA TYPE**

# BD437 BD439 BD441

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector–Emitter Breakdown Voltage ( $I_C = 100\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$ BD437 BD439 BD441	45 60 80	– – –	– – –	Vdc
Collector–Base Breakdown Voltage ( $I_C = 100\ \mu\text{A}$ , $I_B = 0$ )	$V_{(BR)CBO}$ BD437 BD439 BD441	45 60 80	– – –	– – –	Vdc
Emitter–Base Breakdown Voltage ( $I_E = 100\ \mu\text{A}$ , $I_C = 0$ )	$V_{(BR)EBO}$	5.0	–	–	Vdc
Collector Cutoff Current ( $V_{CB} = 45\text{ V}$ , $I_E = 0$ ) ( $V_{CB} = 60\text{ V}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ V}$ , $I_E = 0$ )	$I_{CBO}$ BD437 BD439 BD441	– – –	– – –	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ( $V_{EB} = 5.0\text{ V}$ )	$I_{EBO}$	–	–	1.0	mAdc
DC Current Gain ( $I_C = 10\text{ mA}$ , $V_{CE} = 5.0\text{ V}$ )	$h_{FE}$ BD437 BD439 BD441	30 20 15	– – –	– – –	
DC Current Gain ( $I_C = 500\text{ mA}$ , $V_{CE} = 1.0\text{ V}$ )	$h_{FE}$ BD437 BD439, BD441	85 40	– –	375 475	
DC Current Gain ( $I_C = 2.0\text{ A}$ , $V_{CE} = 1.0\text{ V}$ )	$h_{FE}$ BD437 BD439 BD441	40 25 15	– – –	– – –	
Collector Saturation Voltage ( $I_C = 3.0\text{ A}$ , $I_B = 0.3\text{ A}$ )	$V_{CE(sat)}$ BD437, BD439, BD441	–	–	0.8	Vdc
Base–Emitter On Voltage ( $I_C = 2.0\text{ A}$ , $V_{CE} = 1.0\text{ V}$ )	$V_{BE(on)}$	–	–	1.1	Vdc
Current–Gain – Bandwidth Product ( $V_{CE} = 1.0\text{ V}$ , $I_C = 250\text{ mA}$ , $f = 1.0\text{ MHz}$ )	$f_T$	3.0	–	–	MHz



# BD437 BD439 BD441

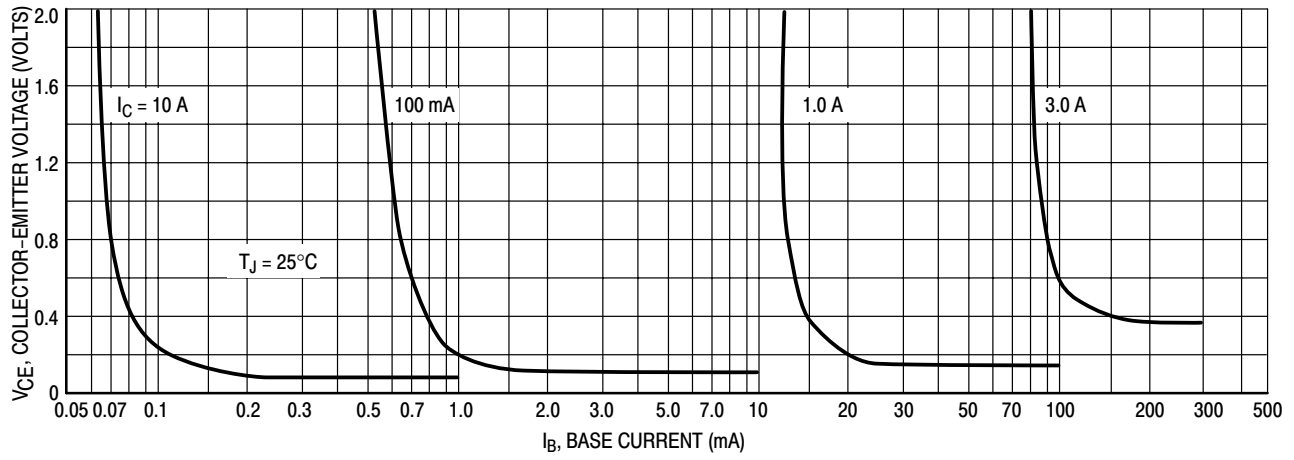


Figure 1. Collector Saturation Region

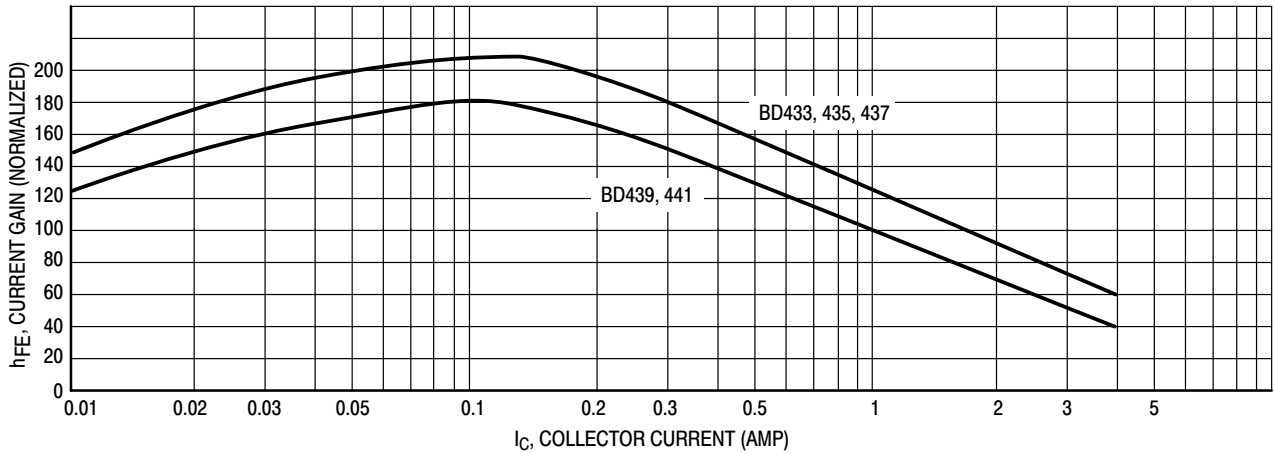


Figure 2. Current Gain

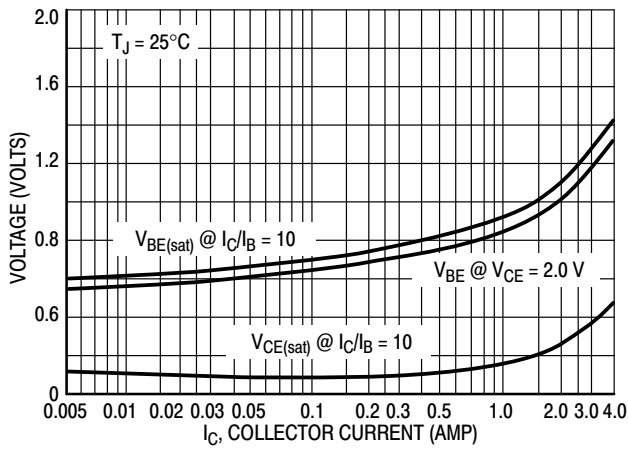


Figure 3. "On" Voltage

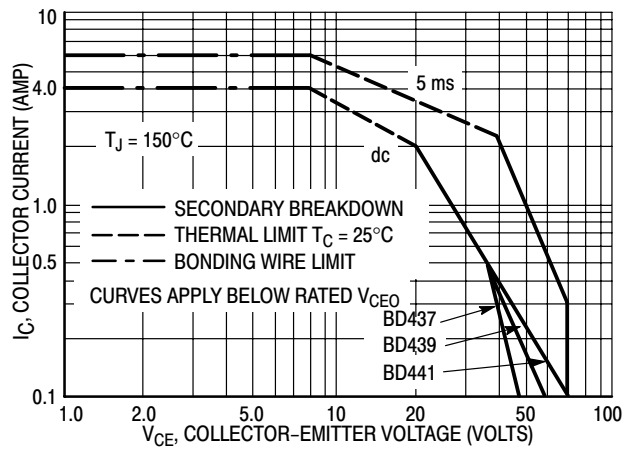


Figure 4. Active Region Safe Operating Area

# Plastic Medium Power Silicon PNP Transistor

... for amplifier and switching applications. Complementary types are BD437 and BD441.

**BD438**  
**BD440**  
**BD442**

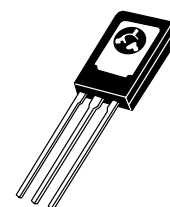
**4.0 AMPERES**  
**POWER TRANSISTORS**  
**PNP SILICON**

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	BD438 BD440 BD442	$V_{CEO}$ 45 60 80	Vdc
Collector–Base Voltage	BD438 BD440 BD442	$V_{CBO}$ 45 60 80	Vdc
Emitter–Base Voltage		$V_{EBO}$ 5.0	Vdc
Collector Current		$I_C$ 4.0	Adc
Base Current		$I_B$ 1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$		$P_D$ 36 288	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range		$T_J, T_{stg}$ –55 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	3.5	$^\circ\text{C}/\text{W}$



**CASE 77–09**  
**TO–225AA TYPE**

## BD438 BD440 BD442

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector–Emitter Breakdown Voltage ( $I_C = 100\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	45 60 80	— — —	— — —	Vdc
Collector–Base Breakdown Voltage ( $I_C = 100\ \mu\text{A}$ , $I_B = 0$ )	$V_{(BR)CBO}$	45 60 80	— — —	— — —	Vdc
Emitter–Base Breakdown Voltage ( $I_E = 100\ \mu\text{A}$ , $I_C = 0$ )	$V_{(BR)EBO}$	5.0	—	—	Vdc
Collector Cutoff Current ( $V_{CB} = 45\text{ V}$ , $I_E = 0$ ) ( $V_{CB} = 60\text{ V}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ V}$ , $I_E = 0$ )	$I_{CBO}$	— — —	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ( $V_{EB} = 5.0\text{ V}$ )	$I_{EBO}$	—	—	1.0	mAdc
DC Current Gain ( $I_C = 10\text{ mA}$ , $V_{CE} = 5.0\text{ V}$ )	$h_{FE}$	30 20 15	— — —	— — —	
DC Current Gain ( $I_C = 500\text{ mA}$ , $V_{CE} = 1.0\text{ V}$ )	$h_{FE}$	85 40 40	— — —	375 475 475	
DC Current Gain ( $I_C = 2.0\text{ A}$ , $V_{CE} = 1.0\text{ V}$ )	$h_{FE}$	40 25 15	— — —	— — —	
Collector Saturation Voltage ( $I_C = 3.0\text{ A}$ , $I_B = 0.3\text{ A}$ )	$V_{CE(sat)}$	— — —	— — —	0.7 0.8 0.8	Vdc
Base–Emitter On Voltage ( $I_C = 2.0\text{ A}$ , $V_{CE} = 1.0\text{ V}$ )	$V_{BE(ON)}$	— —	— —	1.1 1.5	Vdc
Current–Gain — Bandwidth Product ( $V_{CE} = 1.0\text{ V}$ , $I_C = 250\text{ mA}$ , $f = 1.0\text{ MHz}$ )	$f_T$	3.0	—	—	MHz

# BD438 BD440 BD442

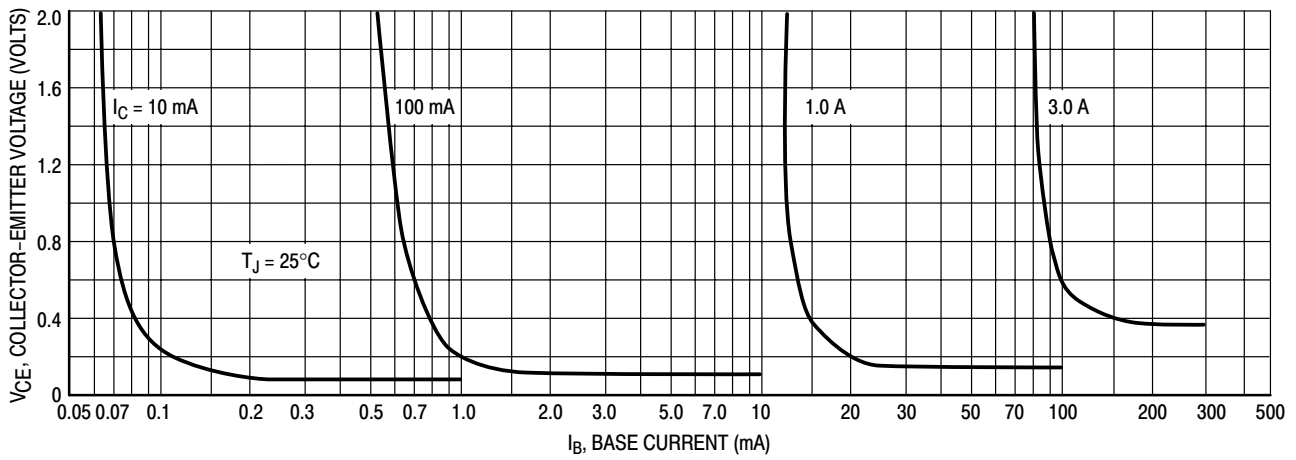


Figure 1. Collector Saturation Region

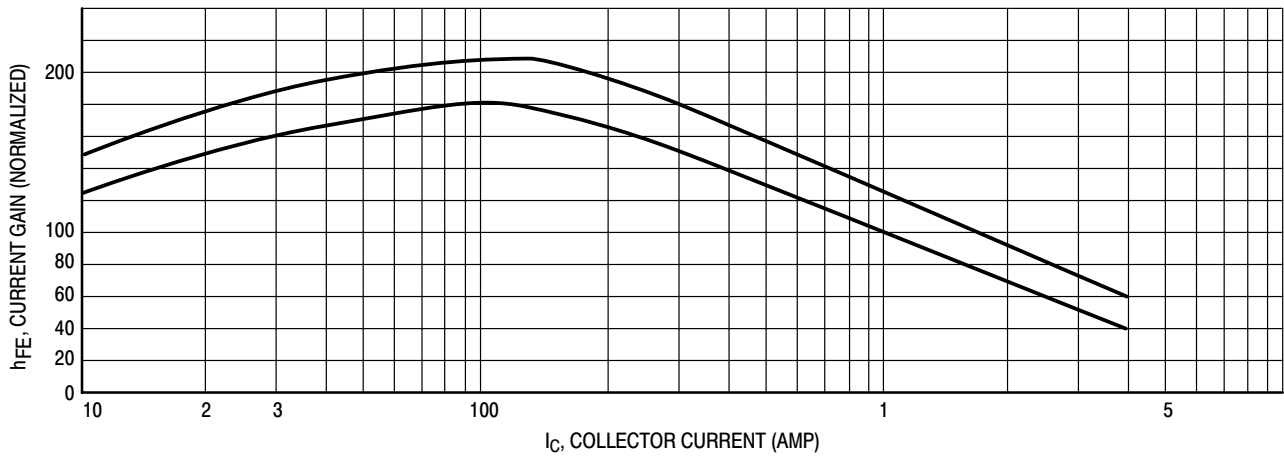


Figure 2. Current Gain

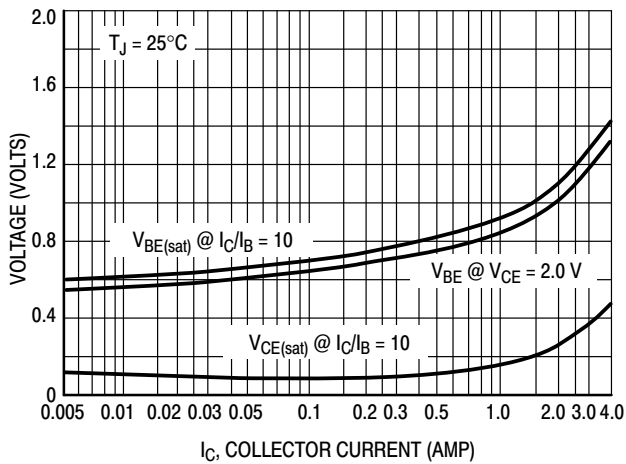


Figure 3. "On" Voltage

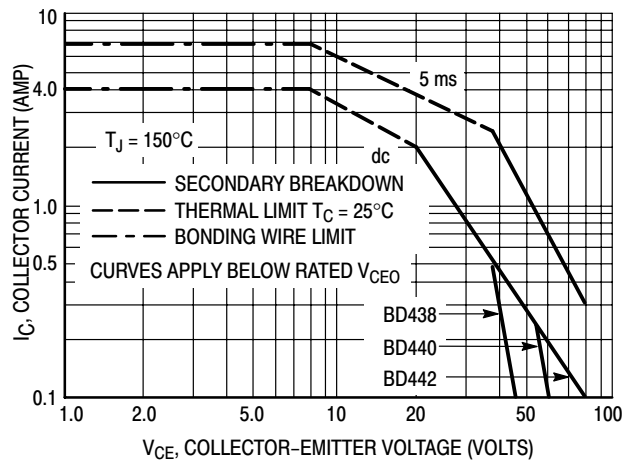


Figure 4. Active Region Safe Operating Area

# Plastic Medium-Power Silicon NPN Darlington

... for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain —  
 $h_{FE} = 750$  (Min) @  $I_C$   
 $= 1.5$  and  $2.0$  Adc
- Monolithic Construction
- BD675, 675A, 677, 677A, 679, 679A, 681 are complementary with BD676, 676A, 678, 678A, 680, 680A, 682
- BD 677, 677A, 679, 679A are equivalent to MJE 800, 801, 802, 803

## MAXIMUM RATINGS

Rating	Symbol	BD675 BD675 A	BD677 BD677 A	BD679 BD679 A	BD68 1	Unit
Collector–Emitter Voltage	$V_{CEO}$	45	60	80	100	Vdc
Collector–Base Voltage	$V_{CB}$	45	60	80	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0				Vdc
Collector Current	$I_C$	4.0				Adc
Base Current	$I_B$	0.1				Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.32				Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperating Range	$T_J, T_{stg}$	-55 to +150				$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	3.13	$^\circ\text{C}/\text{W}$

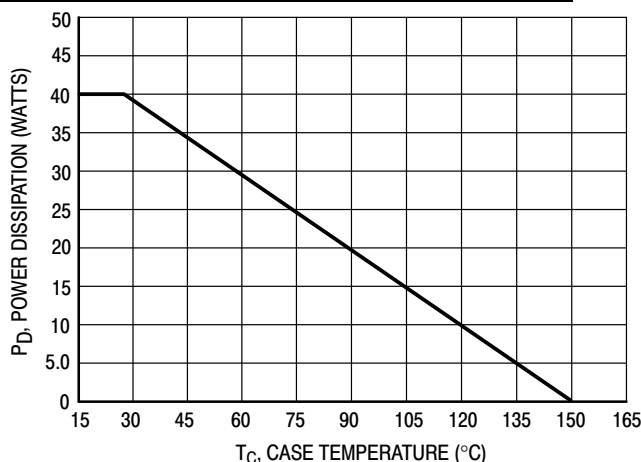


Figure 1. Power Temperature Derating

**BD675**  
**BD675A**  
**BD677**  
**BD677A**  
**BD679**  
**BD679A**  
**BD681\***

\*ON Semiconductor Preferred Device

**4.0 AMPERE**  
**DARLINGTON**  
**POWER TRANSISTORS**  
**NPN SILICON**  
**60, 80, 100 VOLTS**  
**40 WATTS**

**CASE 77-09**  
**TO-225AA TYPE**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# BD675 BD675A BD677 BD677A BD679 BD679A BD681

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Breakdown Voltage <sup>(1)</sup> ( $I_C = 50\text{ mAdc}$ , $I_B = 0$ )	BD675, 675A BD677, 677A BD679, 679A BD681	$BV_{CEO}$	45 60 80 100	— — — —	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Half Rated } BV_{CEO}$ , $I_B = 0$ )		$I_{CEO}$	—	500	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CB} = \text{Rated } BV_{CEO}$ , $I_E = 0$ ) ( $V_{CB} = \text{Rated } BV_{CEO}$ , $I_E = 0$ , $T_C = 100^\circ\text{C}$ )		$I_{CBO}$	— —	0.2 2.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	2.0	mAdc

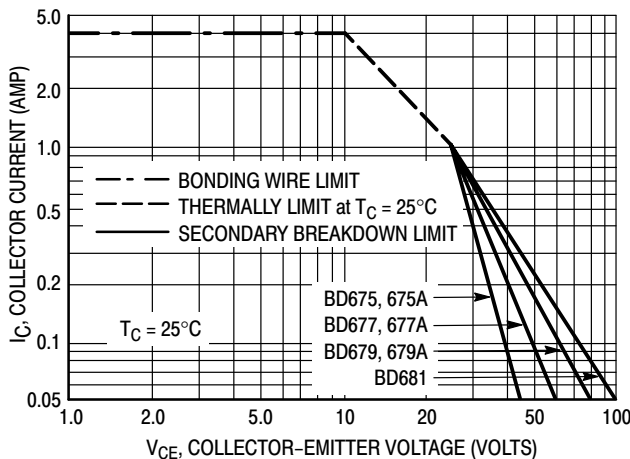
## ON CHARACTERISTICS

DC Current Gain <sup>(1)</sup> ( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	BD675, 677, 679, 681 BD675A, 677A, 679A	$h_{FE}$	750 750	— —	—
Collector–Emitter Saturation Voltage <sup>(1)</sup> ( $I_C = 1.5\text{ Adc}$ , $I_B = 30\text{ mAdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $I_B = 40\text{ mAdc}$ )	BD677, 679, 681 BD675A, 677A, 679A	$V_{CE(\text{sat})}$	— —	2.5 2.8	Vdc
Base–Emitter On Voltage <sup>(1)</sup> ( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	BD677, 679, 681 BD675A, 677A, 679A	$V_{BE(\text{on})}$	— —	2.5 2.5	Vdc

## DYNAMIC CHARACTERISTICS

Small Signal Current Gain ( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$h_{fe}$	1.0	—	—
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(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



**Figure 2. DC Safe Operating Area**

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

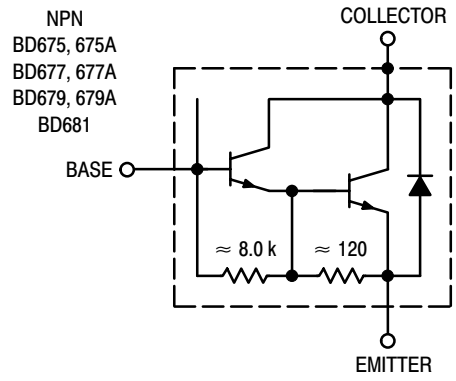


Figure 3. Darlington Circuit Schematic

# BD676, BD676A, BD678, BD678A, BD680, BD680A, BD682

## Plastic Medium-Power Silicon PNP Darlington

...for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain –  
 $h_{FE} = 750$  (Min) @  $I_C = 1.5$  and  $2.0$  Adc
- Monolithic Construction
- BD676, 676A, 678, 678A, 680, 680A, 682 are complementary with  
BD675, 675A, 677, 677A, 679, 679A, 681
- BD 678, 678A, 680, 680A are equivalent to MJE 700, 701, 702, 703

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage BD676, BD676A BD678, BD678A BD680, BD680A BD682	$V_{CEO}$	45 60 80 100	Vdc
Collector-Base Voltage BD676, BD676A BD678, BD678A BD680, BD680A BD682	$V_{CB}$	45 60 80 100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current	$I_C$	4.0	Adc
Base Current	$I_B$	0.1	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.32	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

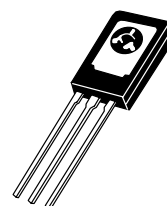
Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Case	$R_{\theta JC}$	3.13	$^\circ\text{C}/\text{W}$



ON Semiconductor™

<http://onsemi.com>

**4.0 AMPERE  
DARLINGTON  
POWER TRANSISTORS  
PNP SILICON  
45, 60, 80, 100 VOLTS  
40 WATTS**



TO-225AA  
CASE 77  
STYLE 1

### MARKING DIAGRAM



Y = Year  
WW = Work Week  
BD6xxx = Specific Device Code  
xxx = 76, 76A, 78, 78A, 80, 80A or 82

### ORDERING INFORMATION

Device	Package	Shipping
BD676	TO-225AA	500 Units/Box
BD676A	TO-225AA	500 Units/Box
BD678	TO-225AA	500 Units/Box
BD678A	TO-225AA	500 Units/Box
BD680	TO-225AA	500 Units/Box
BD680A	TO-225AA	500 Units/Box
BD682	TO-225AA	500 Units/Box



# BD676, BD676A, BD678, BD678A, BD680, BD680A, BD682

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Breakdown Voltage (Note 1.) ( $I_C = 50\text{ mAdc}$ , $I_B = 0$ )	BD676, 676A BD678, 678A BD680, 680A BD682	$BV_{CEO}$	45 60 80 100	– – – –	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Half Rated } V_{CEO}$ , $I_B = 0$ )		$I_{CEO}$	–	500	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CB} = \text{Rated } BV_{CEO}$ , $I_E = 0$ ) ( $V_{CB} = \text{Rated } BV_{CEO}$ , $I_E = 0$ , $T_C = 100^\circ\text{C}$ )		$I_{CBO}$	– –	0.2 2.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	–	2.0	mAdc

## ON CHARACTERISTICS

DC Current Gain (Note 1.) ( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	BD676, 678, 680, 682 BD676A, 678A, 680A	$h_{FE}$	750 750	– –	
Collector–Emitter Saturation Voltage (Note 1.) ( $I_C = 1.5\text{ Adc}$ , $I_B = 30\text{ mAdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $I_B = 40\text{ mAdc}$ )	BD678, 680, 682 BD676A, 678A, 680A	$V_{CE(sat)}$	– –	2.5 2.8	Vdc
Base–Emitter On Voltage (Note 1.) ( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	BD678, 680, 682 BD676A, 678A, 680A	$V_{BE(on)}$	– –	2.5 2.5	Vdc

## DYNAMIC CHARACTERISTICS

Small–Signal Current Gain ( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$h_{fe}$	1.0	–	–
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1. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

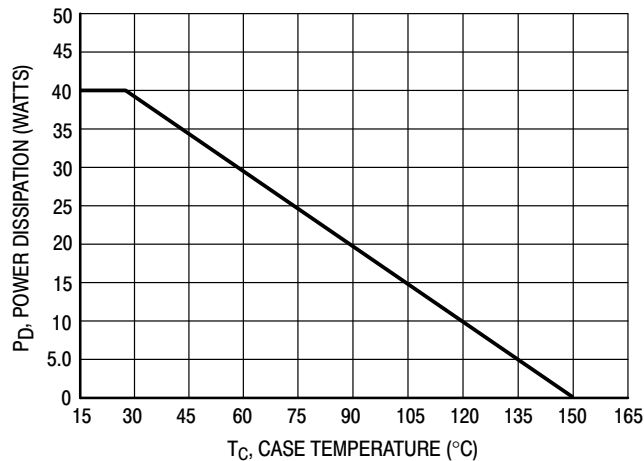
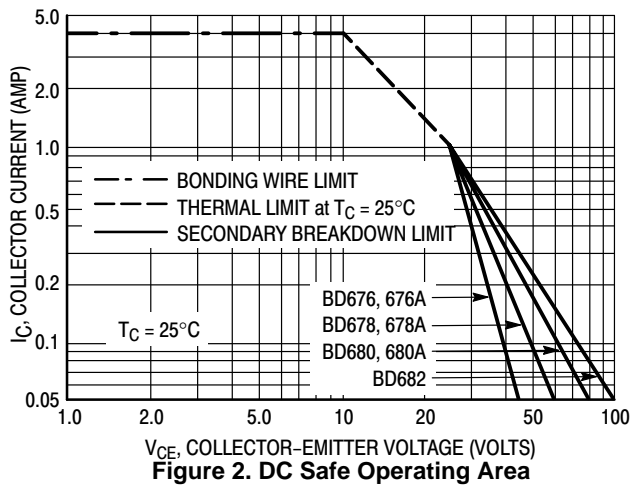


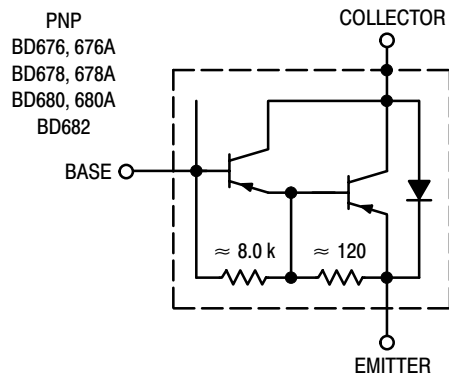
Figure 1. Power Temperature Derating

## BD676, BD676A, BD678, BD678A, BD680, BD680A, BD682



There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.



# Complementary Plastic Silicon Power Transistors

... designed for lower power audio amplifier and low current, high-speed switching applications.

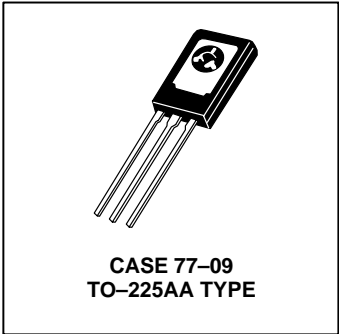
- Low Collector–Emitter Sustaining Voltage —  $V_{CEO(sus)}$  60 Vdc (Min) — BD787, BD788
- High Current–Gain — Bandwidth Product —  $f_T = 50$  MHz (Min) @  $I_C = 100$  mAdc
- Collector–Emitter Saturation Voltage Specified at 0.5, 1.0, 2.0 and 4.0 Adc

**NPN  
BD787  
PNP  
BD788**

**4 AMPERE  
POWER TRANSISTORS  
COMPLEMENTARY  
SILICON  
60 VOLTS  
15 WATTS**

## MAXIMUM RATINGS

Rating	Symbol	BD787 BD788	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	Vdc
Collector–Base Voltage	$V_{CBO}$	80	Vdc
Emitter–Base Voltage	$V_{EBO}$	6.0	Vdc
Collector Current — Continuous — Peak	$I_C$	4.0 8.0	Adc Adc
Base Current	$I_B$	1.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	15 0.12	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$



## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	$^\circ\text{C}/\text{W}$

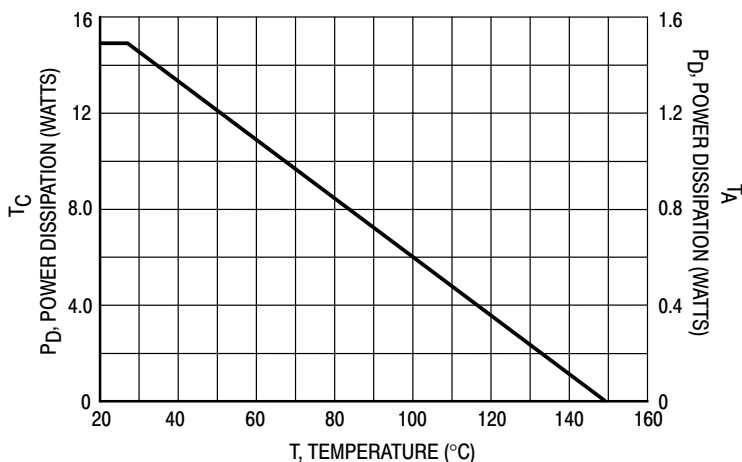


Figure 1. Power Derating

# BD787 BD788

**\*ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 10\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current ( $V_{CE} = 20\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	100	$\mu\text{A dc}$
Collector Cutoff Current ( $V_{CE} = 80\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 40\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$	— —	1.0 0.1	$\mu\text{A dc}$ mA dc
Emitter Cutoff Current ( $V_{EB} = 6.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	$\mu\text{A dc}$
<b>ON CHARACTERISTICS(1)</b>				
DC Current Gain ( $I_C = 200\text{ mA dc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 1.0\text{ A dc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 2.0\text{ A dc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 4.0\text{ A dc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	$h_{FE}$	40 25 20 5.0	250 — — —	—
Collector–Emitter Saturation Voltage ( $I_C = 500\text{ mA dc}$ , $I_B = 50\text{ mA dc}$ ) ( $I_C = 1.0\text{ A dc}$ , $I_B = 100\text{ mA dc}$ ) ( $I_C = 2.0\text{ A dc}$ , $I_B = 200\text{ mA dc}$ ) ( $I_C = 4.0\text{ A dc}$ , $I_B = 800\text{ mA dc}$ )	$V_{CE(sat)}$	— — — —	0.4 0.6 0.8 2.5	Vdc
Base–Emitter Saturation Voltage ( $I_C = 2.0\text{ A dc}$ , $I_B = 200\text{ mA dc}$ )	$V_{BE(sat)}$	—	2.0	Vdc
Base–Emitter On Voltage ( $I_C = 2.0\text{ A dc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	$V_{BE(on)}$	—	1.8	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain — Bandwidth Product ( $I_C = 100\text{ mA dc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 10\text{ MHz}$ )	$f_T$	50	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_C = 0$ ) ( $f = 0.1\text{ MHz}$ )	$C_{ob}$	— —	50 70	pF
Small–Signal Current Gain ( $I_C = 200\text{ mA dc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	10	—	—

\*Indicates JEDEC Registered Data

(1) Pulse Test; Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

# BD787 BD788

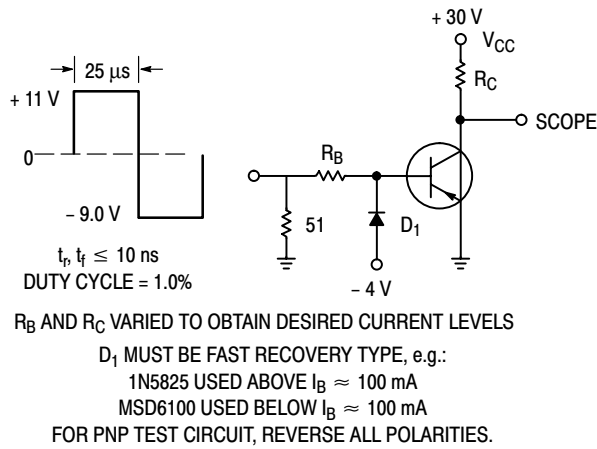


Figure 2. Switching Time Test Circuit

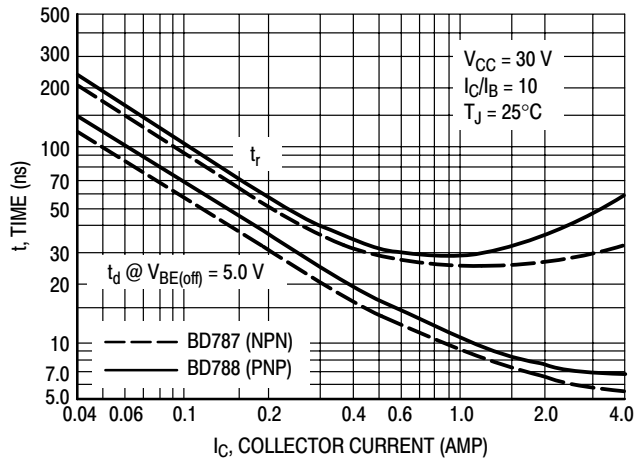


Figure 3. Turn-On Time

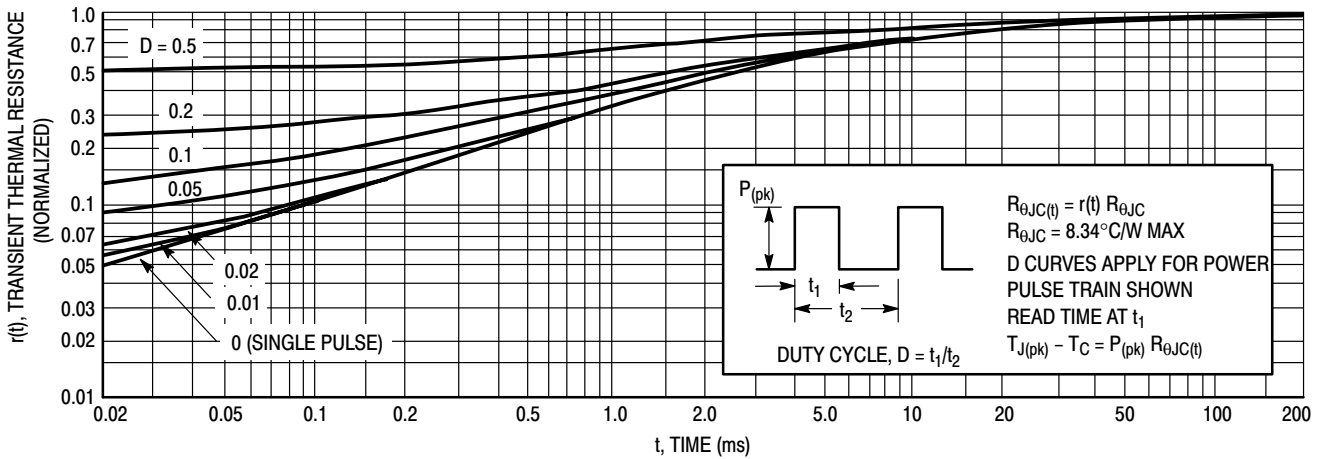


Figure 4. Thermal Response

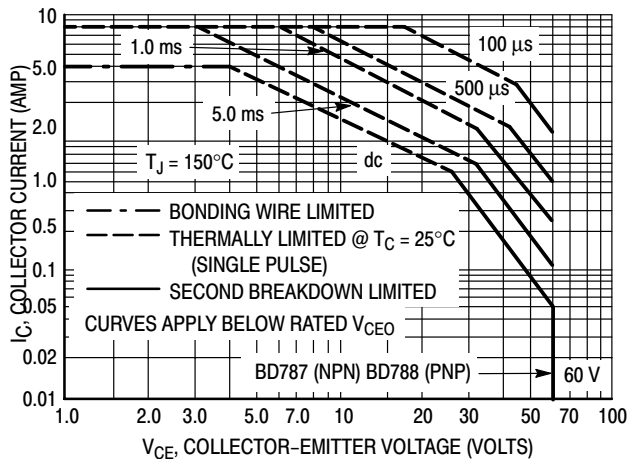


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ ,  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# BD787 BD788

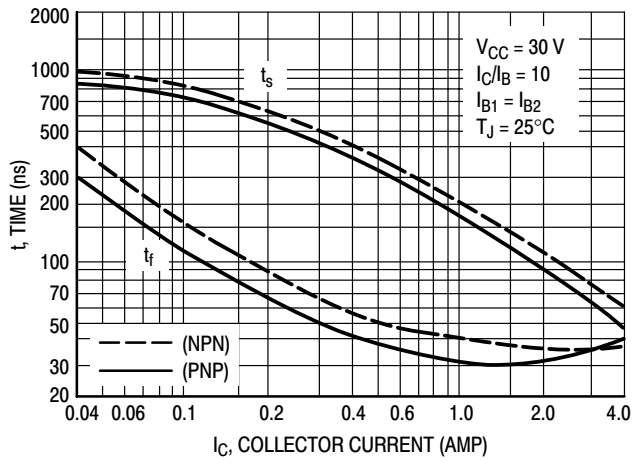


Figure 6. Turn-Off Time

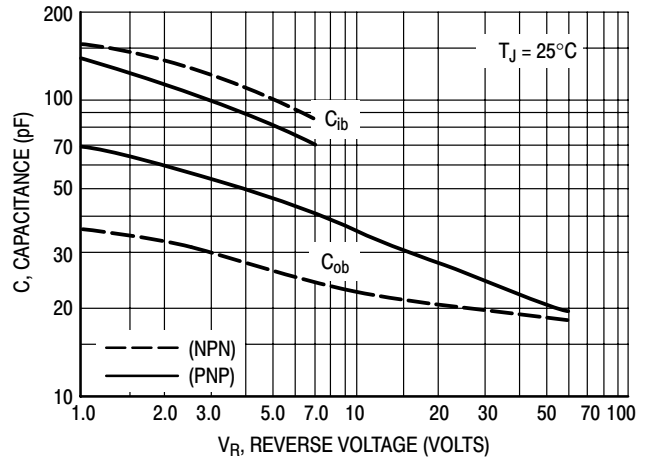


Figure 7. Capacitance

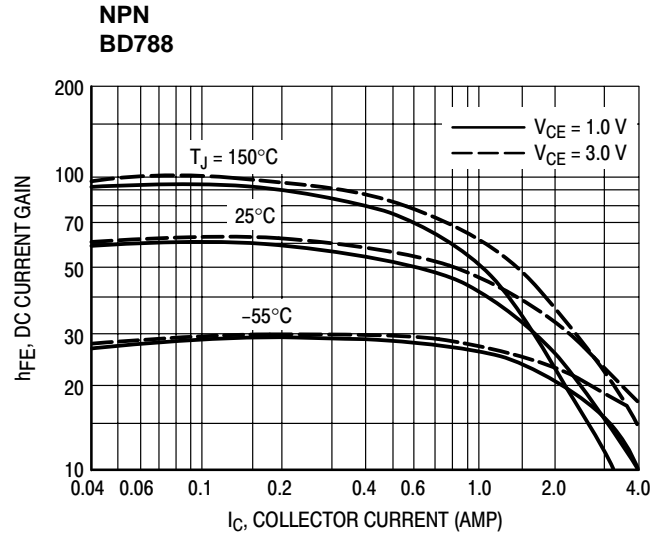
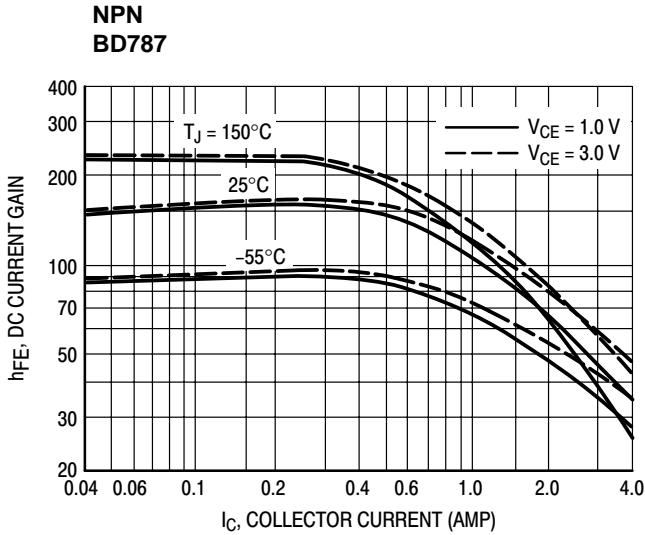


Figure 8. DC Current Gain

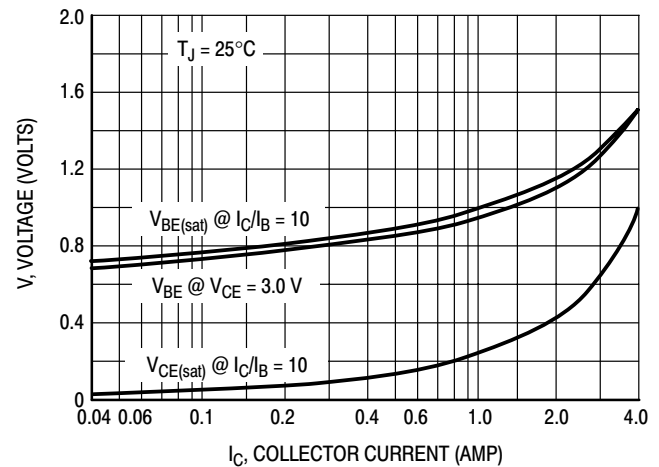
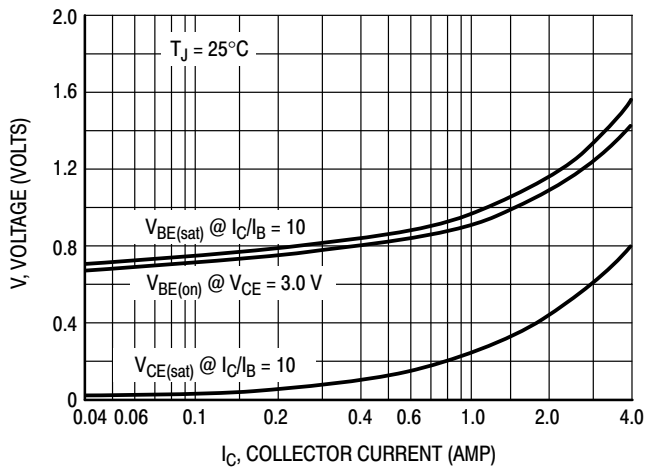


Figure 9. "On" Voltages

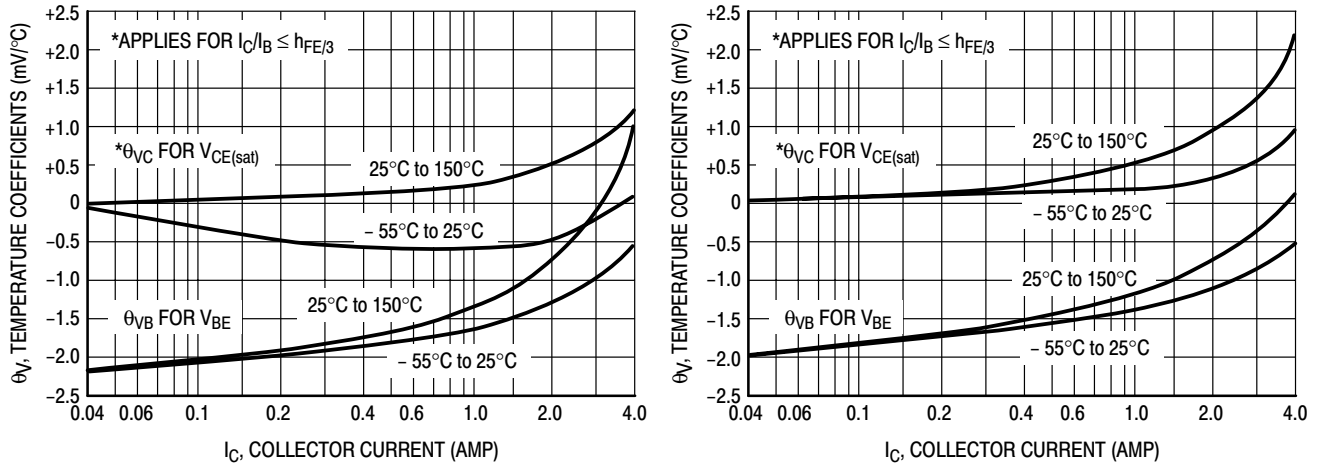


Figure 10. Temperature Coefficients

# Plastic High Power Silicon Transistor

... designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain —  
 $h_{FE} = 30 \text{ (Min) @ } I_C = 2.0 \text{ A dc}$

## MAXIMUM RATINGS

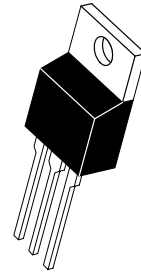
Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Collector–Base Voltage	$V_{CBO}$	80	Vdc
Emitter–Base Voltage	$V_{EBO}$	5.0	Vdc
Collector Current	$I_C$	10	A dc
Base Current	$I_B$	6.0	A dc
Total Device Dissipation $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	90 720	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	1.39	$^\circ\text{C/W}$

**NPN**  
**BD809**  
**PNP**  
**BD810**

**10 AMPERE**  
**POWER TRANSISTORS**  
**PNP SILICON**  
**60, 80 VOLTS**  
**90 WATTS**



**CASE 221A-09**  
**TO-220AB**

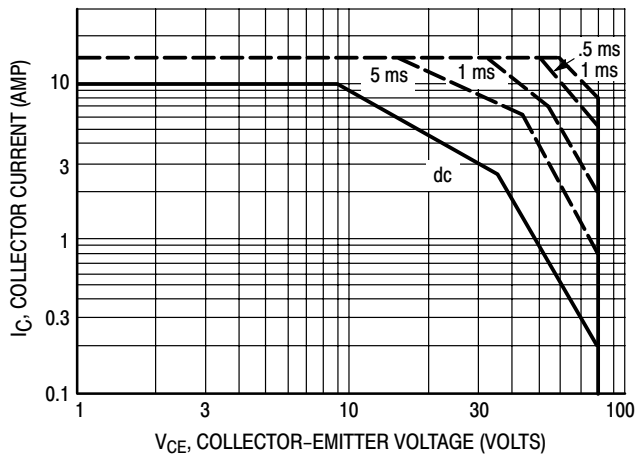


# BD809 BD810

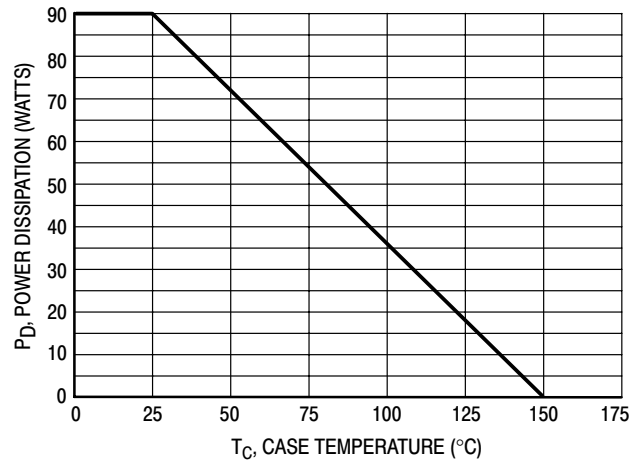
## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* ( $I_C = 0.1 \text{ Adc}$ , $I_B = 0$ )	$BV_{CEO}$	80	—	Vdc
Collector Cutoff Current ( $V_{CB} = 80 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	1.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	2.0	mAdc
DC Current Gain ( $I_C = 2.0 \text{ A}$ , $V_{CE} = 2.0 \text{ V}$ ) ( $I_C = 4.0 \text{ A}$ , $V_{CE} = 2.0 \text{ V}$ )	$h_{FE}$	30 15	—	
Collector–Emitter Saturation Voltage* ( $I_C = 3.0 \text{ Adc}$ , $I_B = 0.3 \text{ Adc}$ )	$V_{CE(sat)}$	—	1.1	Vdc
Base–Emitter On Voltage* ( $I_C = 4.0 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ )	$V_{BE(on)}$	—	1.6	Vdc
Current–Gain Bandwidth Product ( $I_C = 1.0 \text{ Adc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	$f_T$	1.5	—	MHz

\*Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



**Figure 1. Active Region DC Safe Operating Area**  
(see Note 1)



**Figure 2. Power–Temperature Derating Curve**

# BD809 BD810

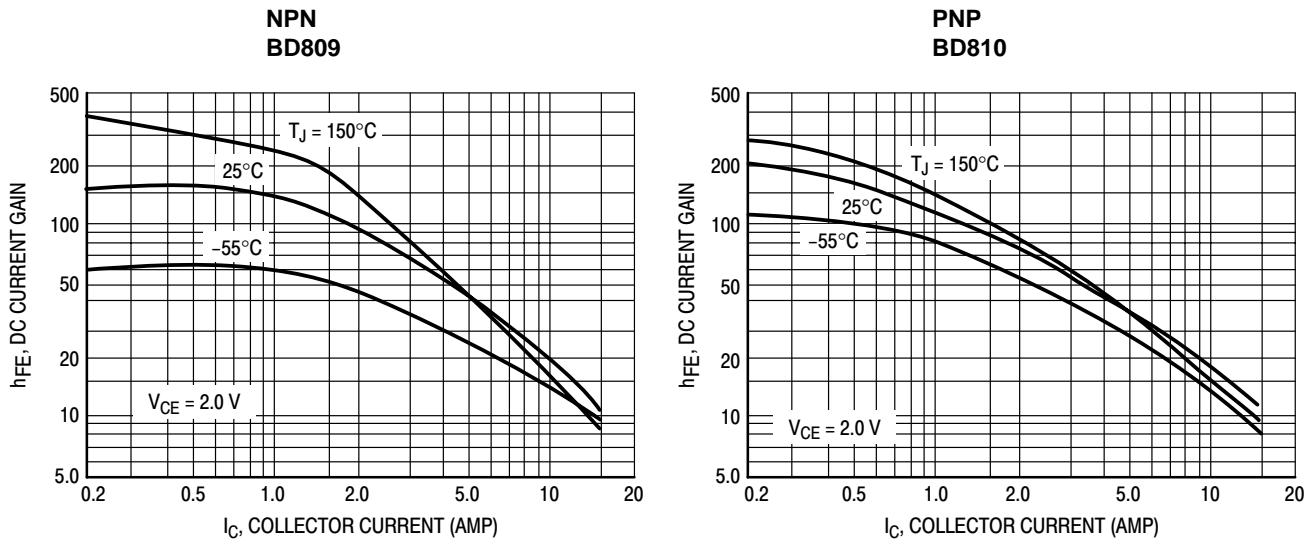


Figure 3. DC Current Gain

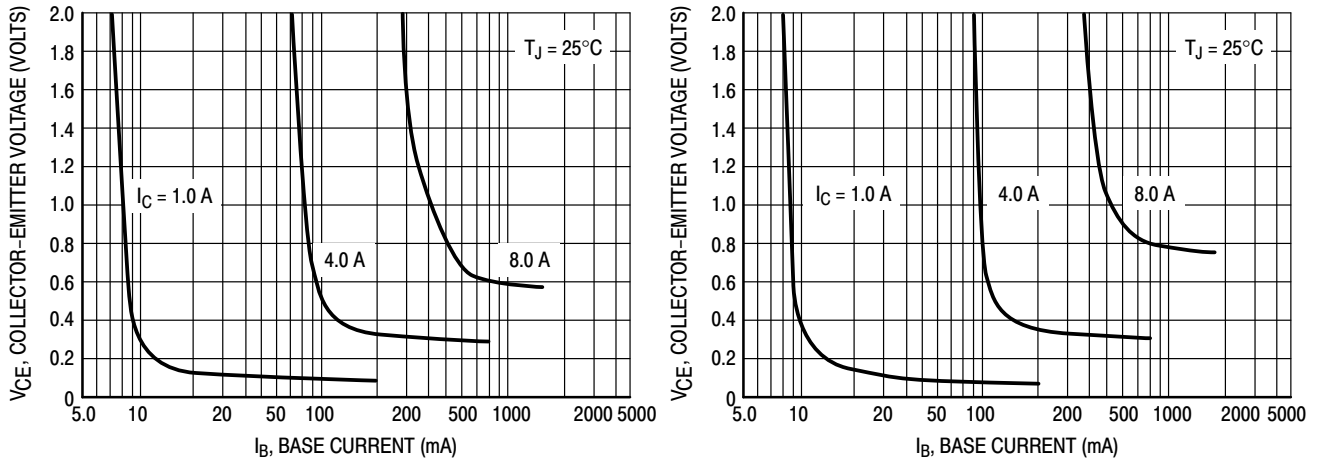


Figure 4. Collector Saturation Region

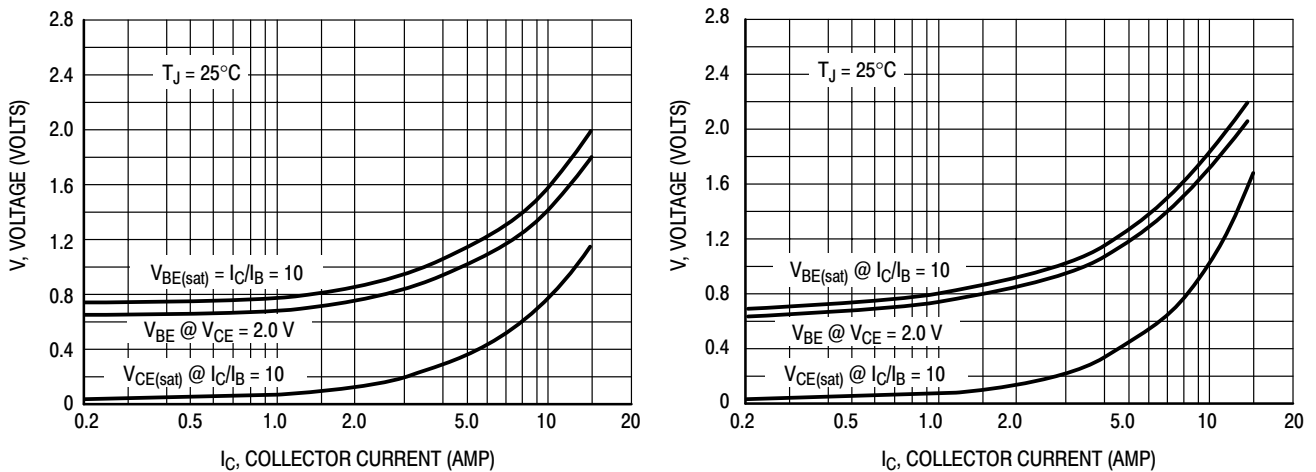
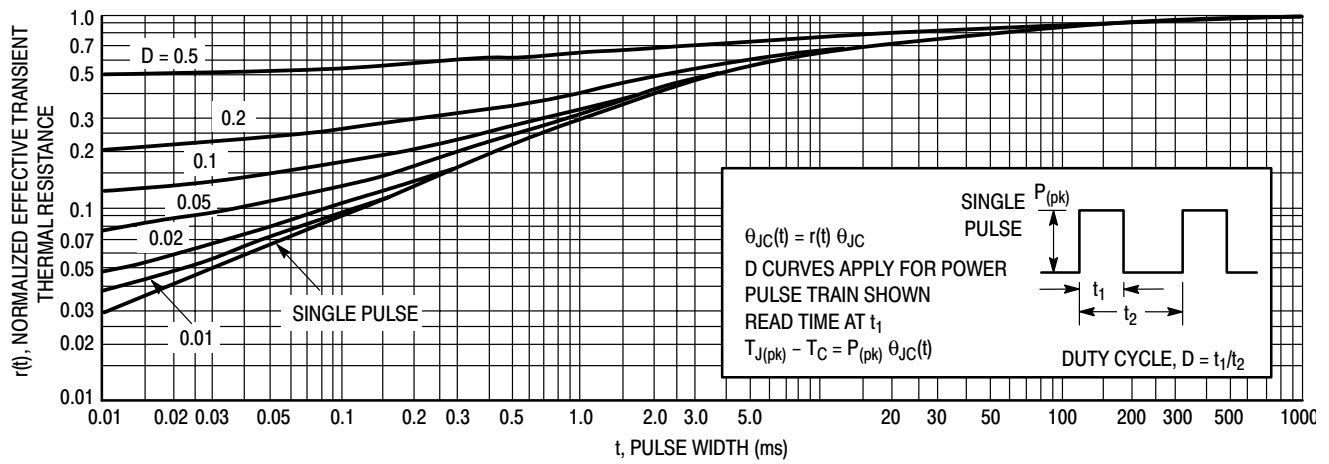


Figure 5. "On" Voltages

# BD809 BD810



**Figure 6. Thermal Response**

**Note 1:**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# Complementary Silicon Plastic Power Darlington

... for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain  
HFE = 1000 (min.) @ 5 Adc
- Monolithic Construction with Built-in Base Emitter Shunt Resistors

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous — Peak	$I_C$	10 20	A <sub>dc</sub>
Base Current	$I_B$	0.5	A <sub>dc</sub>
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	125 1.0	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	1.0	$^\circ\text{C}/\text{W}$

**NPN  
BDV65B  
PNP  
BDV64B**

**DARLINGTONS  
10 AMPERES  
COMPLEMENTARY  
SILICON  
POWER TRANSISTORS  
60-80-100-120 VOLTS  
125 WATTS**

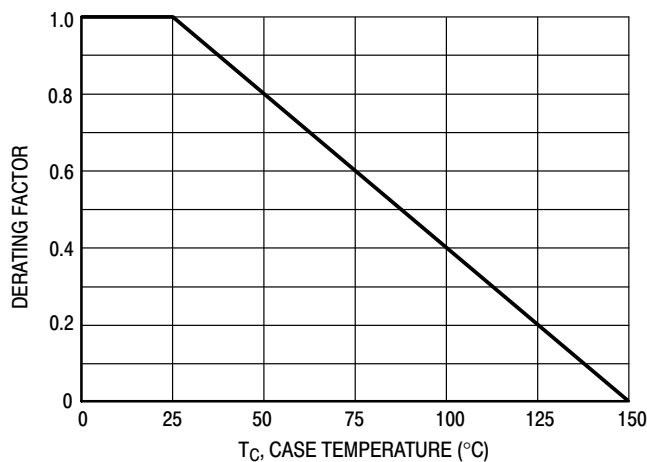
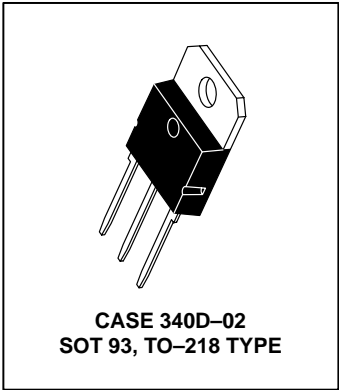
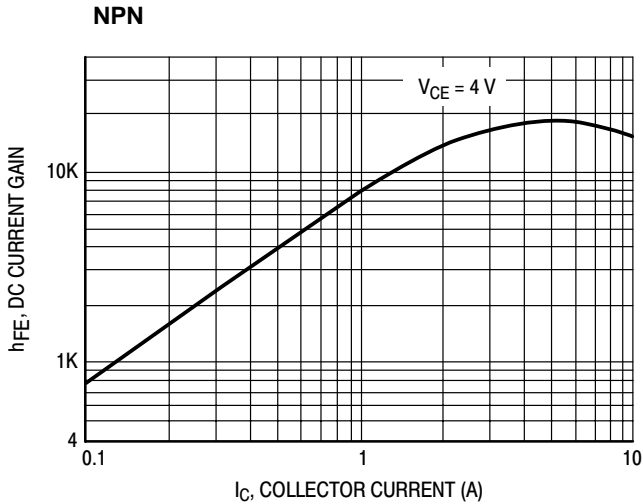


Figure 1. Power Derating

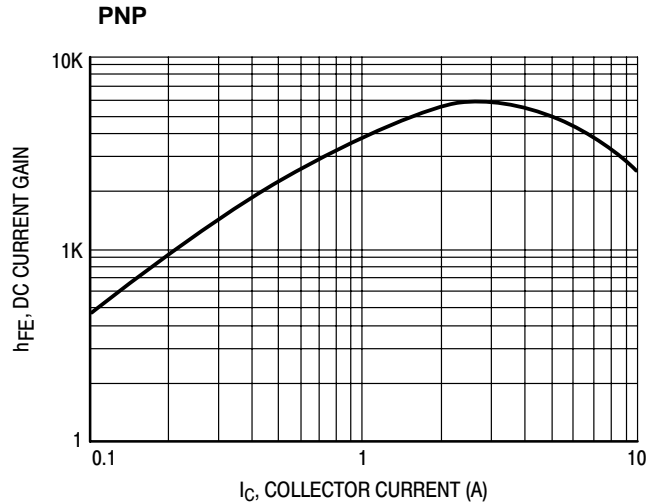
# BDV65B BDV64B

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30 \text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current ( $V_{CE} = 50 \text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	1.0	mAdc
Collector Cutoff Current ( $V_{CB} = 100 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	0.4	mAdc
Collector Cutoff Current ( $V_{CB} = 50 \text{ Vdc}$ , $I_E = 0$ , $T_C = 150^\circ\text{C}$ )	$I_{CBO}$	—	2.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	5.0	mAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = 5.0 \text{ Adc}$ , $V_{CE} = 4.0 \text{ Vdc}$ )	$h_{FE}$	1000	—	—
Collector–Emitter Saturation Voltage ( $I_C = 5.0 \text{ Adc}$ , $I_B = 0.02 \text{ Adc}$ )	$V_{CE(sat)}$	—	2.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 5.0 \text{ Adc}$ , $V_{CE} = 4.0 \text{ Vdc}$ )	$V_{BE(on)}$	—	2.5	Vdc



**Figure 2. DC Current Gain**



**Figure 3. DC Current Gain**

# BDV65B BDV64B

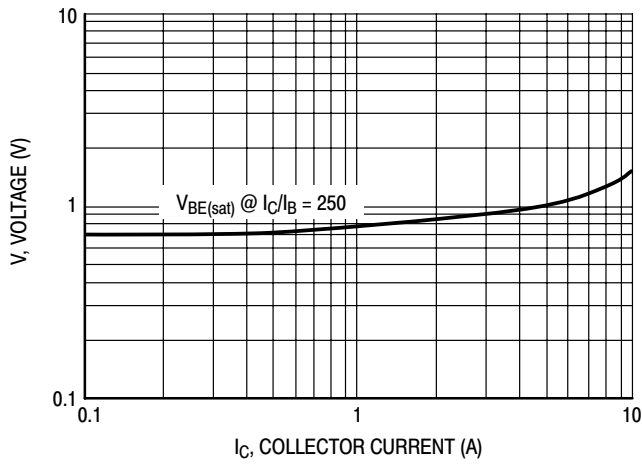


Figure 4. "On" Voltages

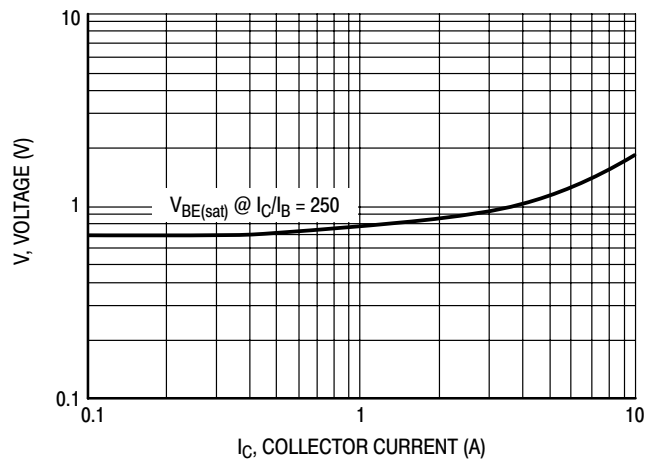


Figure 5. "On" Voltages

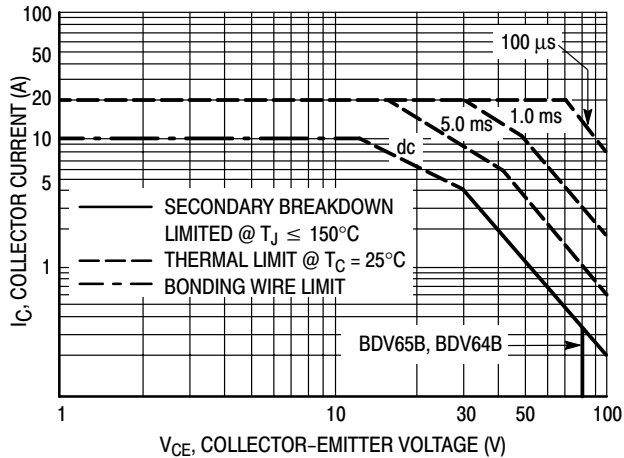


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ,  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

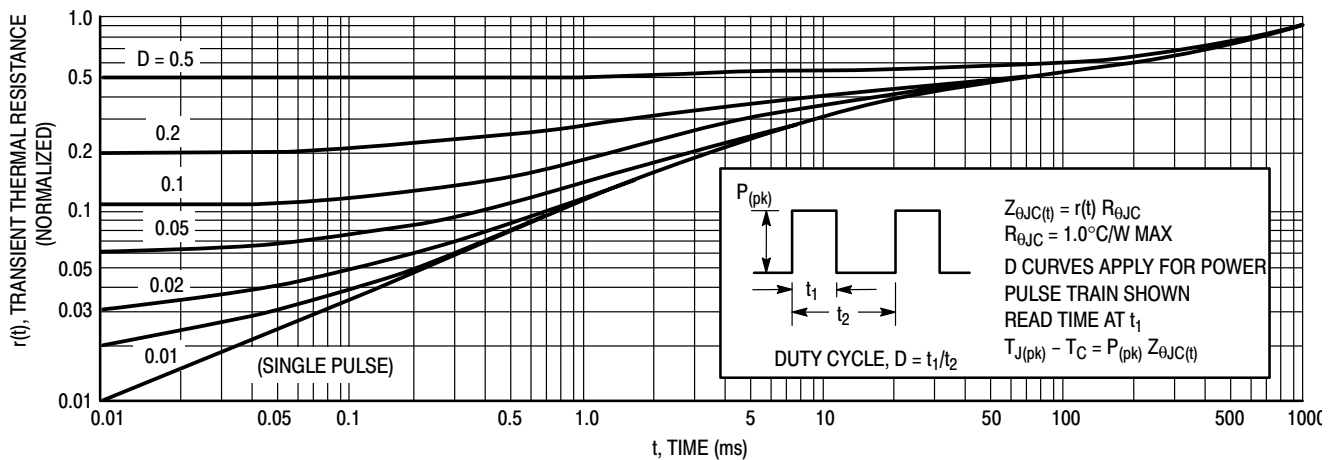


Figure 7. Thermal Response

# Darlington Complementary Silicon Power Transistors

...designed for general purpose and low speed switching applications.

- High DC Current Gain –  $h_{FE} = 2500$  (typ.) @  $I_C = 5.0$  Adc.
- Collector Emitter Sustaining Voltage @ 30 mAdc:
  - $V_{CEO(sus)} = 80$  Vdc (min.) — BDW46
  - 100 Vdc (min.) — BDW42/BDW47
- Low Collector Emitter Saturation Voltage
  - $V_{CE(sat)} = 2.0$  Vdc (max.) @  $I_C = 5.0$  Adc
  - 3.0 Vdc (max.) @  $I_C = 10.0$  Adc
- Monolithic Construction with Built-In Base Emitter Shunt resistors
- TO-220AB Compact Package

## MAXIMUM RATINGS

Rating	Symbol	BDW46	BDW42 BDW47	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	100	Vdc
Collector–Base Voltage	$V_{CB}$	80	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous	$I_C$	15		Adc
Base Current	$I_B$	0.5		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	85 0.68		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–55 to +150		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.47	$^\circ\text{C/W}$

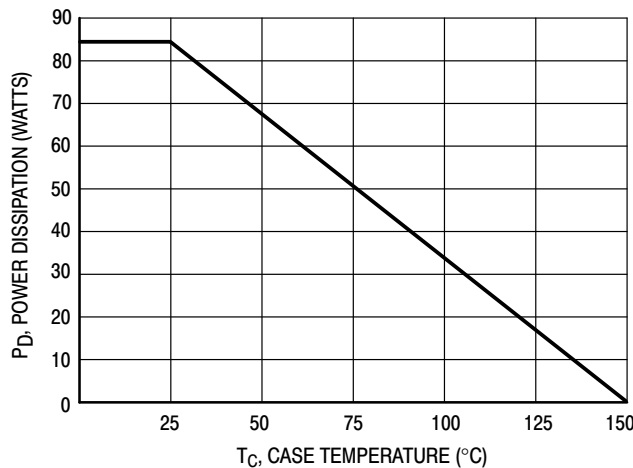
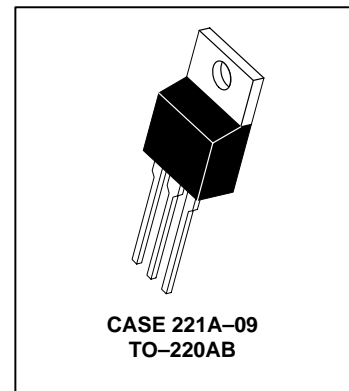


Figure 1. Power Temperature Derating Curve

**NPN**  
**BDW42\***  
**PNP**  
**BDW46**  
  
**BDW47\***

\*ON Semiconductor Preferred Device

**DARLINGTON**  
**15 AMPERE**  
**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**80–100 VOLTS**  
**85 WATTS**



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# BDW42 BDW46 BDW47

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector Emitter Sustaining Voltage (1) (I <sub>C</sub> = 30 mA, I <sub>B</sub> = 0)	BDW46 BDW42/BDW47	V <sub>CEO(sus)</sub>	80 100	— —	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 40 Vdc, I <sub>B</sub> = 0) (V <sub>CE</sub> = 50 Vdc, I <sub>B</sub> = 0)	BDW46 BDW42/BDW47	I <sub>CEO</sub>	— —	2.0 2.0	mA
Collector Cutoff Current (V <sub>CB</sub> = 80 Vdc, I <sub>E</sub> = 0) (V <sub>CB</sub> = 100 Vdc, I <sub>E</sub> = 0)	BDW41/BDW46 BDW42/BDW47	I <sub>CBO</sub>	— —	1.0 1.0	mA
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)		I <sub>EBO</sub>	—	2.0	mA
<b>ON CHARACTERISTICS (1)</b>					
DC Current Gain (I <sub>C</sub> = 5.0 mA, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 10 mA, V <sub>CE</sub> = 4.0 Vdc)		h <sub>FE</sub>	1000 250	— —	
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 5.0 mA, I <sub>B</sub> = 10 mA) (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 50 mA)		V <sub>CE(sat)</sub>	— —	2.0 3.0	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 10 mA, V <sub>CE</sub> = 4.0 Vdc)		V <sub>BE(on)</sub>	—	3.0	Vdc
<b>SECOND BREAKDOWN (2)</b>					
Second Breakdown Collector Current with Base Forward Biased BDW42 BDW46/BDW47	V <sub>CE</sub> = 28.4 Vdc V <sub>CE</sub> = 40 Vdc V <sub>CE</sub> = 22.5 Vdc V <sub>CE</sub> = 36 Vdc	I <sub>S/b</sub>	3.0 1.2 3.8 1.2	— — — —	mA
<b>DYNAMIC CHARACTERISTICS</b>					
Magnitude of common emitter small signal short circuit current transfer ratio (I <sub>C</sub> = 3.0 mA, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 MHz)		f <sub>T</sub>	4.0	—	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	BDW42 BDW46/BDW47	C <sub>ob</sub>	— —	200 300	pF
Small–Signal Current Gain (I <sub>C</sub> = 3.0 mA, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 kHz)		h <sub>fe</sub>	300	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

(2) Pulse Test non repetitive: Pulse Width = 250 ms.



# BDW42 BDW46 BDW47

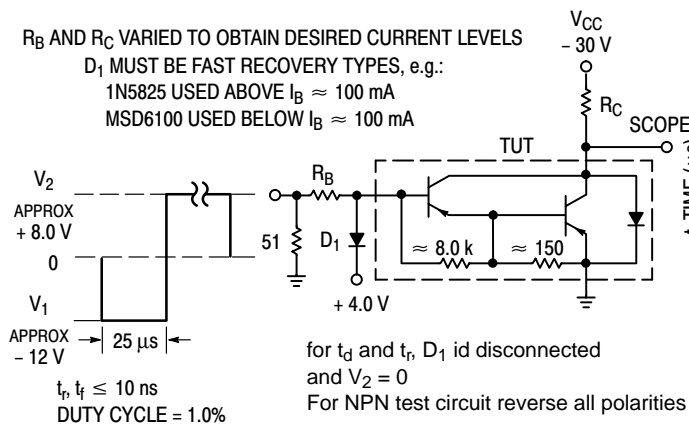


Figure 2. Switching Times Test Circuit

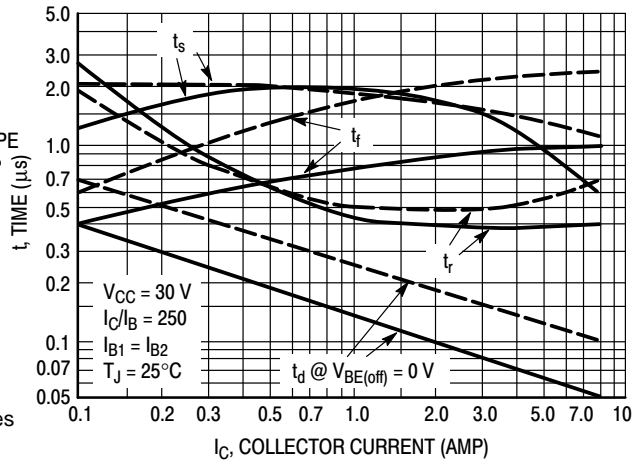


Figure 3. Switching Times

# BDW42 BDW46 BDW47

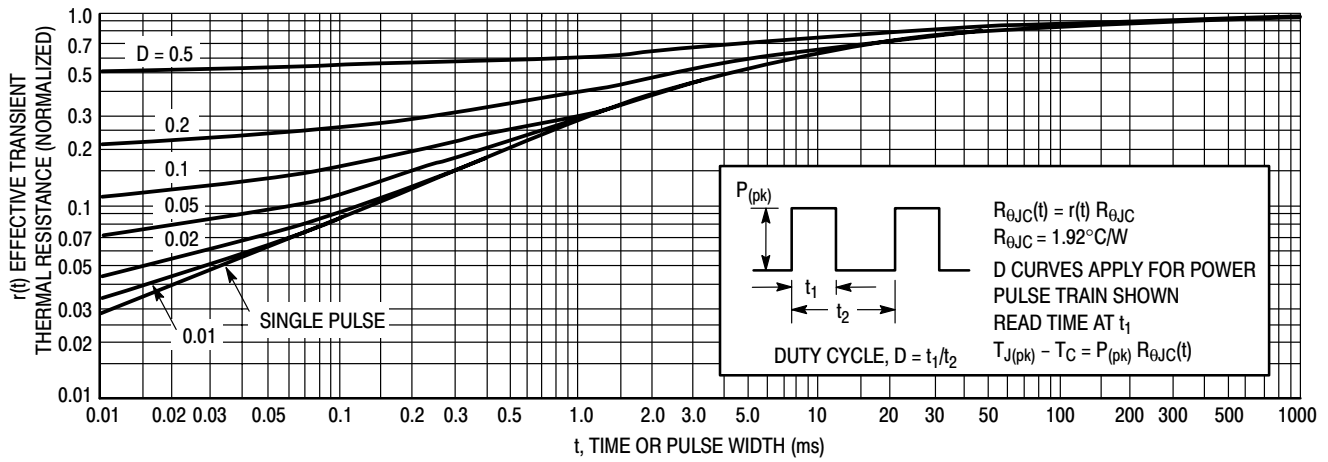


Figure 4. Thermal Response

## ACTIVE-REGION SAFE OPERATING AREA

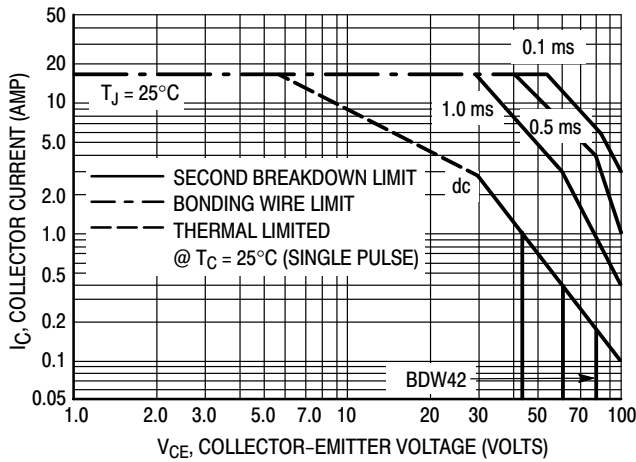


Figure 5. BDW42

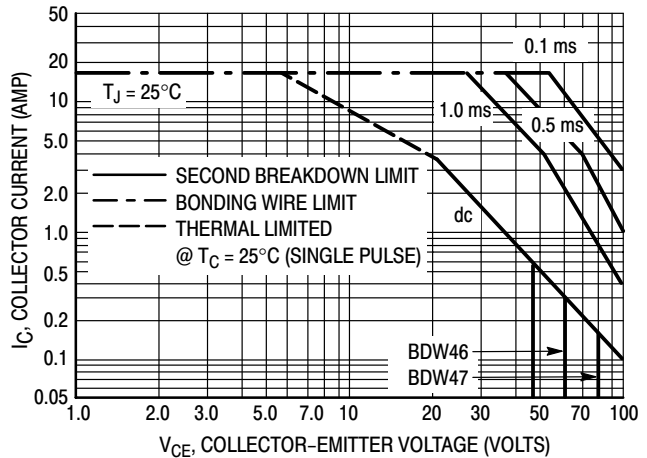


Figure 6. BDW46 and BDW47

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 5 and 6 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions.

Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

\*Linear extrapolation

# BDW42 BDW46 BDW47

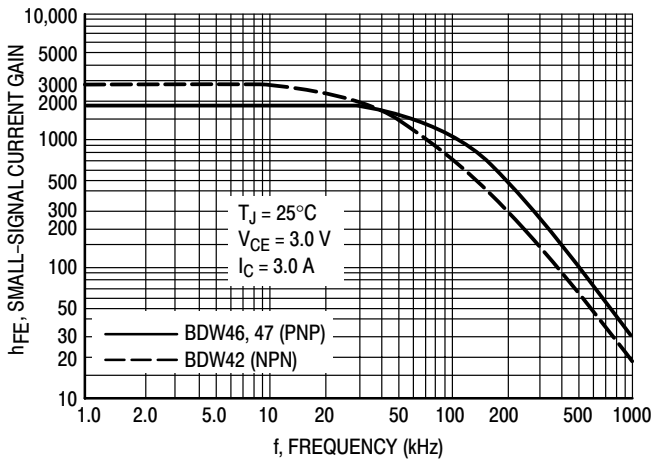


Figure 7. Small-Signal Current Gain

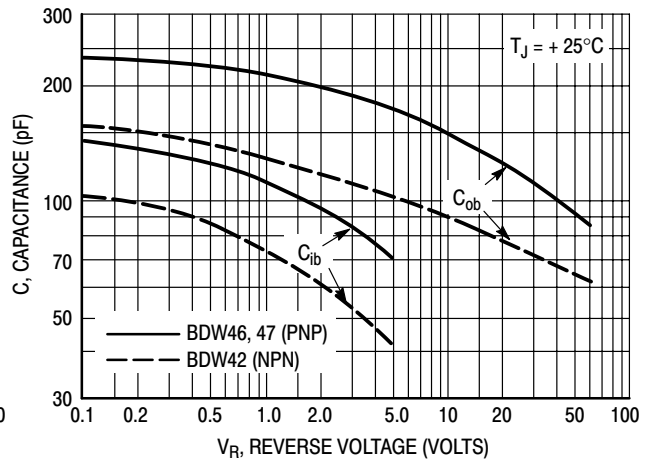
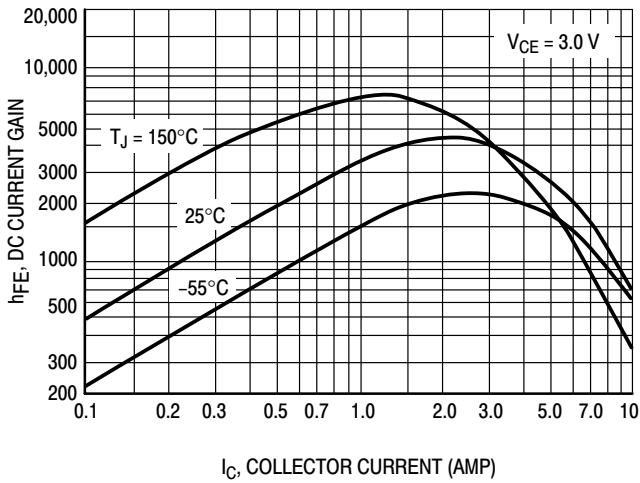


Figure 8. Capacitance

## BDW40, 41, 42 (NPN)



## BDW45, 46, 47 (PNP)

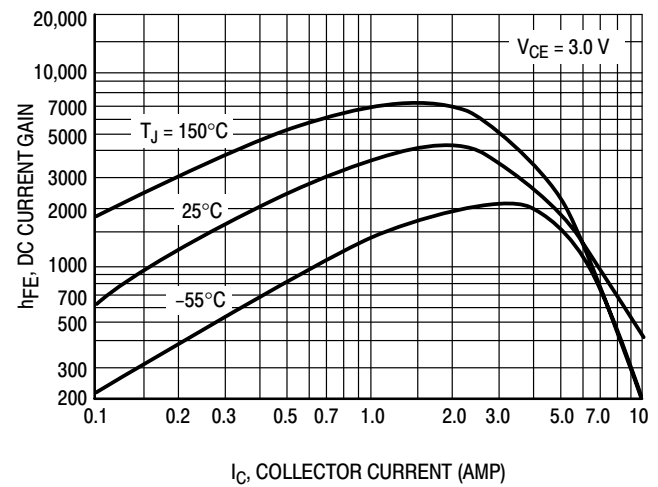


Figure 9. DC Current Gain

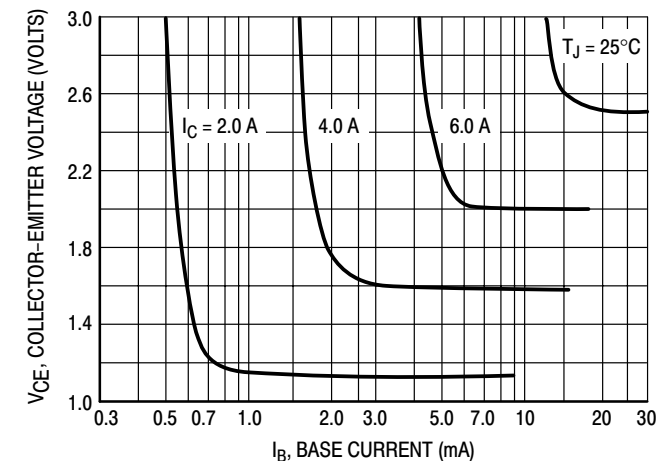
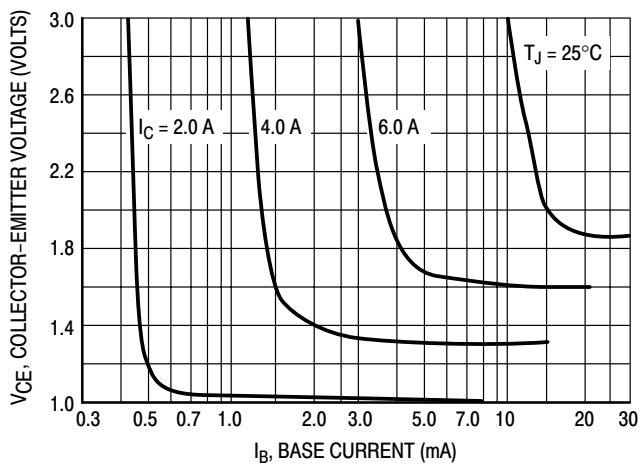
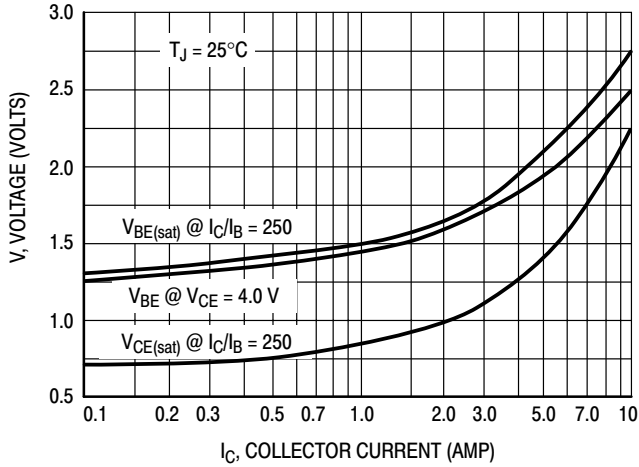


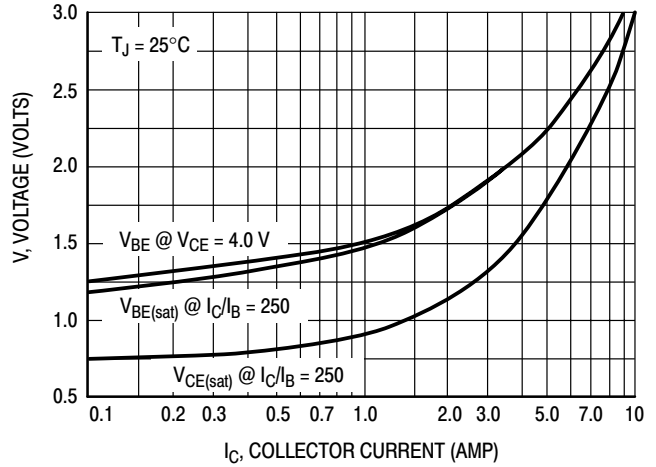
Figure 10. Collector Saturation Region

# BDW42 BDW46 BDW47

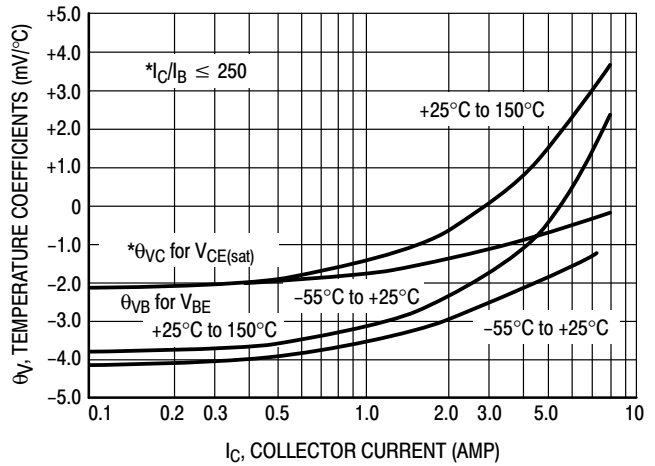
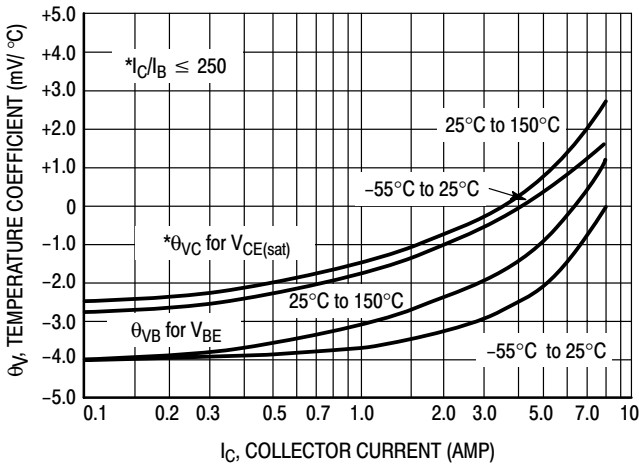
**BDW40, 41, 42 (NPN)**



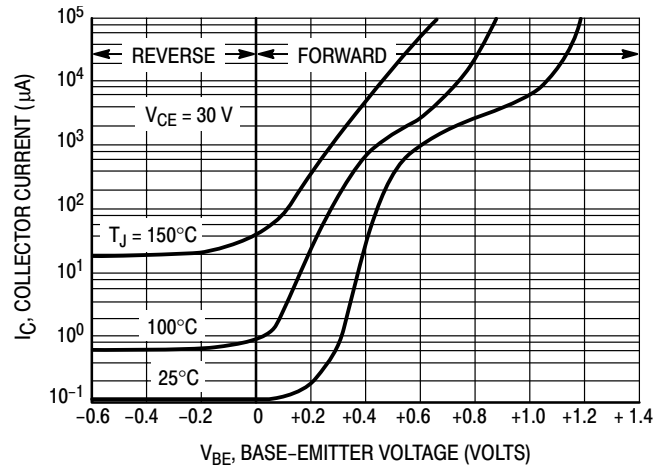
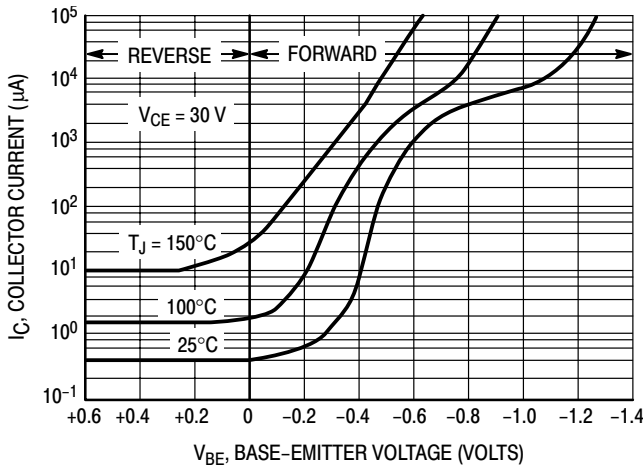
**BDW45, 46, 47 (PNP)**



**Figure 11. "On" Voltages**



**Figure 12. Temperature Coefficients**



**Figure 13. Collector Cut-Off Region**

# BDW42 BDW46 BDW47

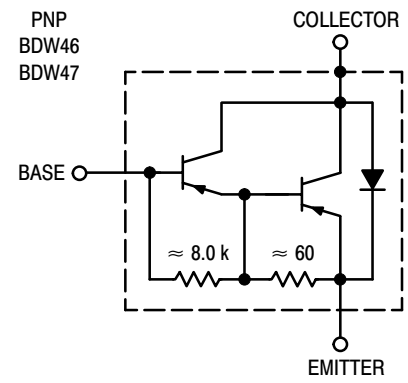
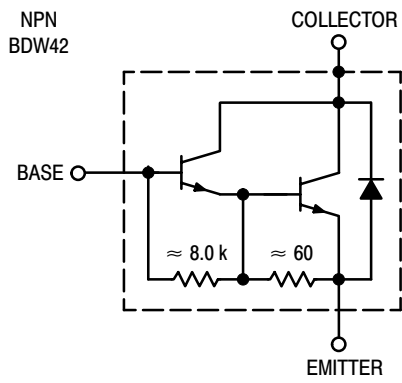


Figure 14. Darlington Schematic

# Darlington Complementary Silicon Power Transistors

... designed for general purpose and low speed switching applications.

- High DC Current Gain —  
 $h_{FE} = 2500$  (typ.) at  $I_C = 4.0$
- Collector–Emitter Sustaining Voltage at 100 mAdc  
 $V_{CE(sus)} = 80$  Vdc (min.) — BDX33B, 34B  
 $100$  Vdc (min.) — BDX33C, 34C
- Low Collector–Emitter Saturation Voltage  
 $V_{CE(sat)} = 2.5$  Vdc (max.) at  $I_C = 3.0$  Adc — BDX33B, 33C/34B, 34C
- Monolithic Construction with Build–In Base–Emitter Shunt resistors
- TO–220AB Compact Package

## MAXIMUM RATINGS

Rating	Symbol	BDX33B BDX34B	BDX33C BDX34C	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	100	Vdc
Collector–Base Voltage	$V_{CB}$	80	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous Peak	$I_C$	10 15		Adc
Base Current	$I_B$	0.25		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	70 0.56		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C}$

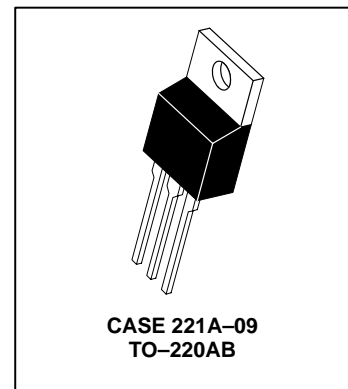
## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.78	$^\circ\text{C/W}$

**NPN**  
**BDX33B**  
**BDX33C\***  
**PNP**  
**BDX34B**  
**BDX34C\***

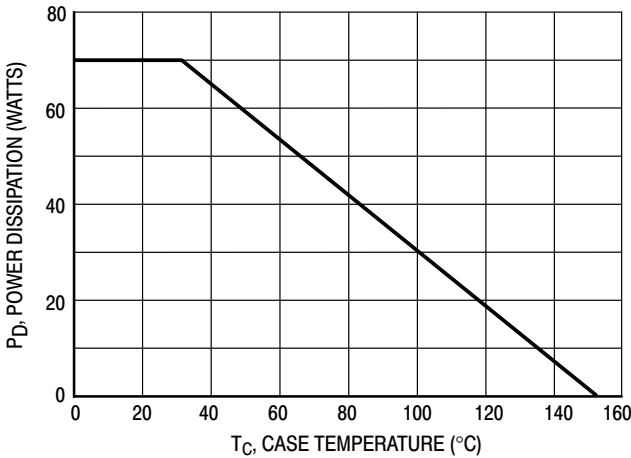
\*ON Semiconductor Preferred Device

**DARLINGTON**  
**10 AMPERE**  
**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**80–100 VOLTS**  
**70 WATTS**



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**BDX33B BDX33C BDX34B BDX34C**



**Figure 1. Power Derating**

# BDX33B BDX33C BDX34B BDX34C

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

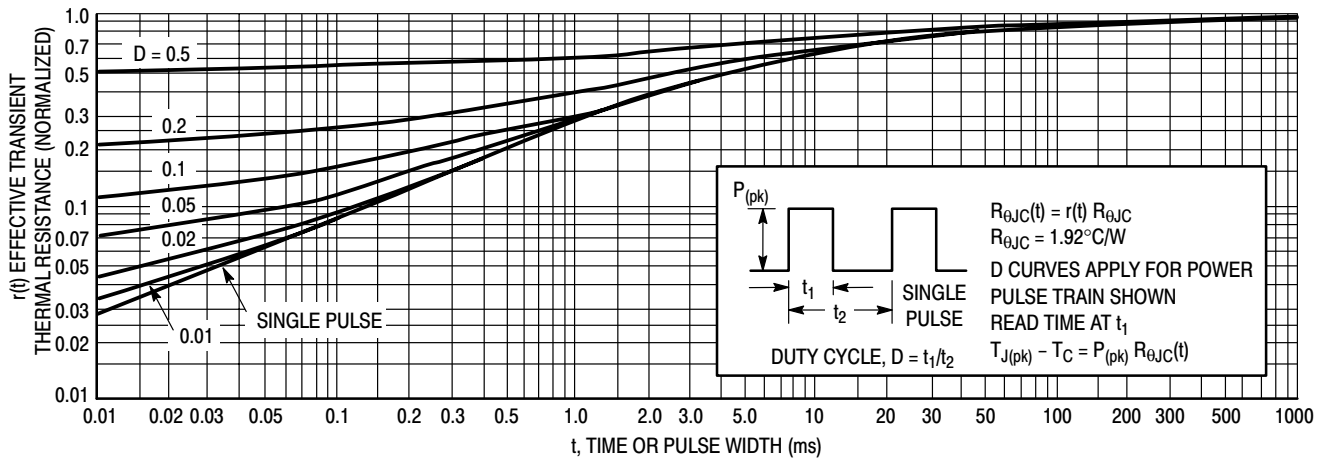
Characteristic		Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage <sup>1</sup> ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	BDX33B/BDX34B BDX33C/BDX34C	$V_{CEO(sus)}$	80 100	— —	Vdc
Collector–Emitter Sustaining Voltage <sup>1</sup> ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ , $R_{BE} = 100$ )	BDX33B/BDX34B BDX33C/BDX33C	$V_{CER(sus)}$	80 100	— —	Vdc
Collector–Emitter Sustaining Voltage <sup>1</sup> ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ , $V_{BE} = 1.5\text{ Vdc}$ )	BDX33B/BDX34B BDX33C/BDX34C	$V_{CEX(sus)}$	80 100	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 1/2$ rated $V_{CEO}$ , $I_B = 0$ )	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	$I_{CEO}$	— —	0.5 10	mAdc
Collector Cutoff Current ( $V_{CB} =$ rated $V_{CBO}$ , $I_E = 0$ )	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	$I_{CBO}$	— —	1.0 5.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	10	mAdc
<b>ON CHARACTERISTICS</b>					
DC Current Gain <sup>1</sup> ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	BDX33B, 33C/34B, 34C	$h_{FE}$	750	—	—
Collector–Emitter Saturation Voltage ( $I_C = 3.0\text{ Adc}$ , $I_B = 6.0\text{ mAdc}$ )	BDX33B, 33C/34B, 34C	$V_{CE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	BDX33B, 33C/34B, 34C	$V_{BE(on)}$	—	2.5	Vdc
Diode Forward Voltage ( $I_C = 8.0\text{ Adc}$ )		$V_F$	—	4.0	Vdc

<sup>1</sup> Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

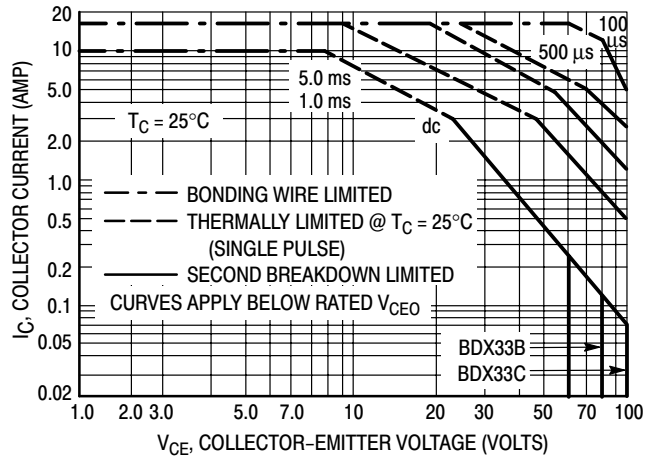
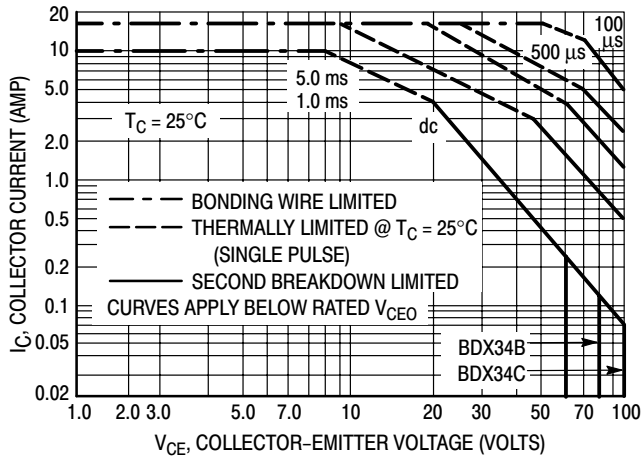
<sup>2</sup> Pulse Test non repetitive: Pulse Width = 0.25 s.



**BDX33B BDX33C BDX34B BDX34C**



**Figure 1. Thermal Response**

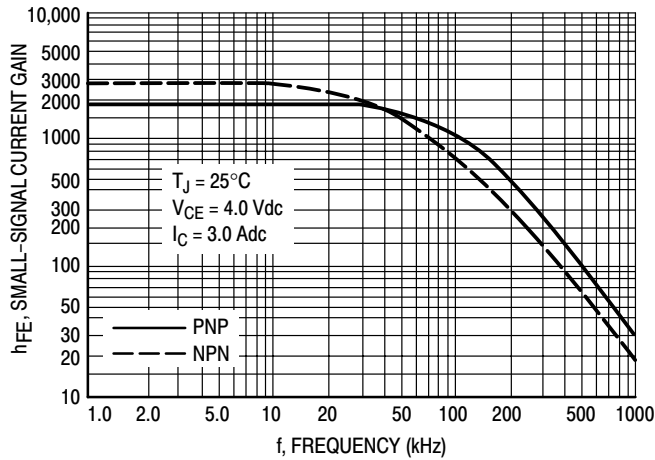


**Figure 2. Active-Region Safe Operating Area**

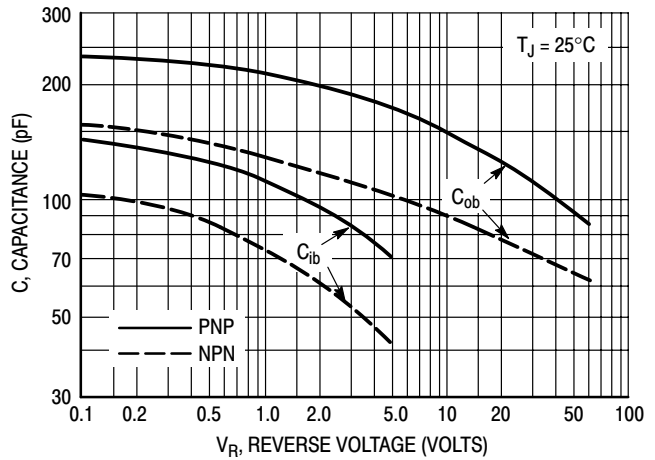
## BDX33B BDX33C BDX34B BDX34C

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 3 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on

conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} = 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 3. Small-Signal Current Gain**

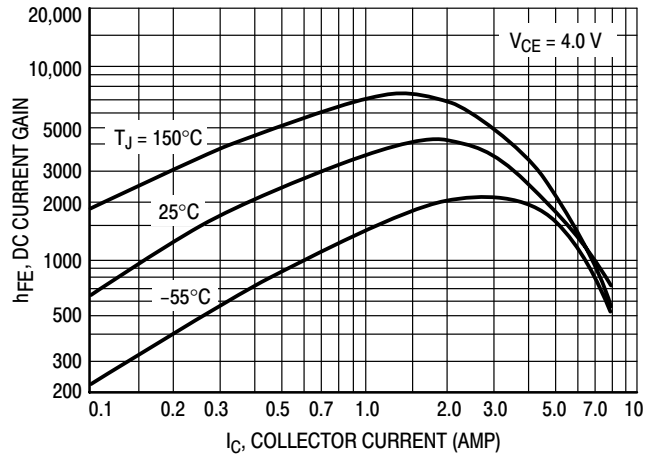
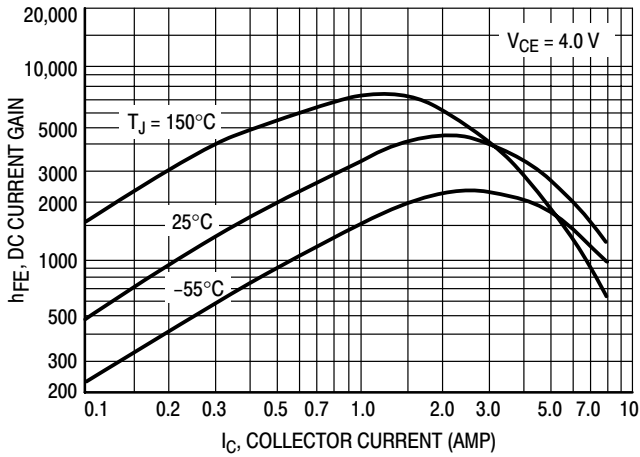


**Figure 4. Capacitance**

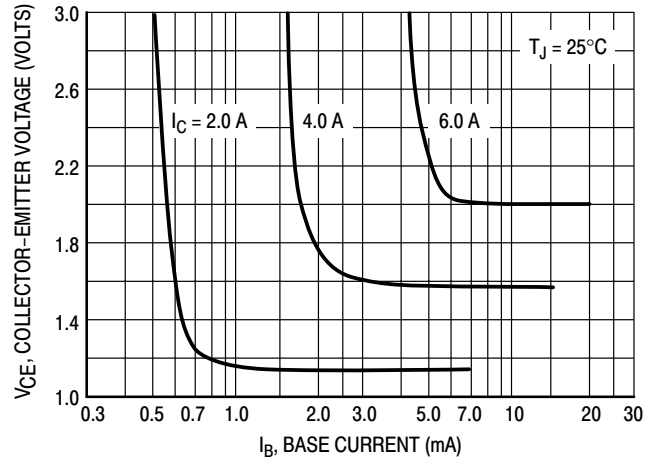
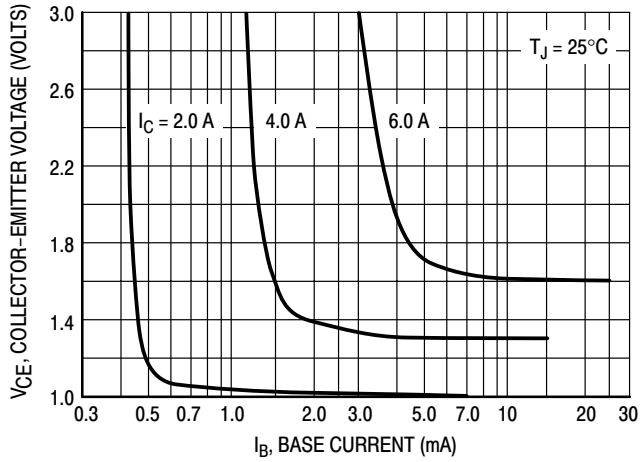
# BDX33B BDX33C BDX34B BDX34C

**NPN**  
**BDX33B, 33C**

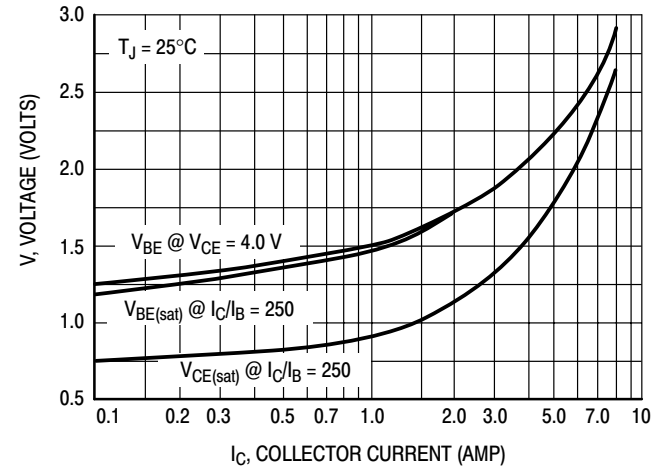
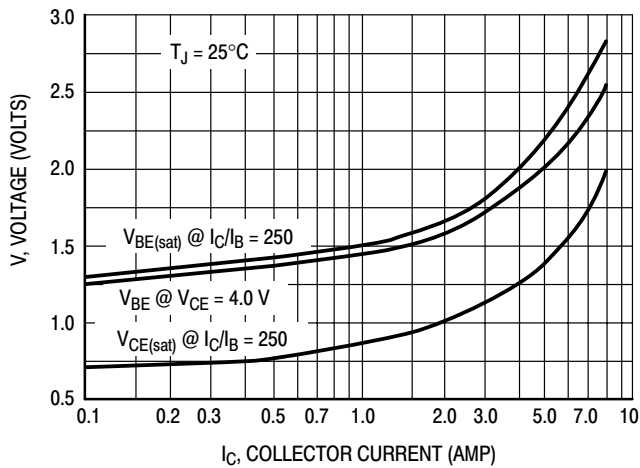
**PNP**  
**BDX34B, 34C**



**Figure 5. DC Current Gain**



**Figure 6. Collector Saturation Region**



**Figure 7. "On" Voltages**

# Plastic Medium-Power Complementary Silicon Transistors

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —  
 $h_{FE} = 2500$  (Typ) @  $I_C = 4.0$  Adc
- Collector Emitter Sustaining Voltage — @ 100 mAdc  
 $V_{CEO(sus)} = 80$  Vdc (Min) — BDX53B, 54B  
 $= 100$  Vdc (Min) — BDX53C, 54C
- Low Collector-Emitter Saturation Voltage —  
 $V_{CE(sat)} = 2.0$  Vdc (Max) @  $I_C = 3.0$  Adc  
 $= 4.0$  Vdc (Max) @  $I_C = 5.0$  Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package

## MAXIMUM RATINGS

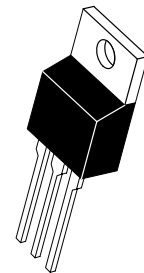
Rating	Symbol	BDX53B BDX54B	BDX53C BDX54C	Unit
Collector-Emitter Voltage	$V_{CEO}$	80	100	Vdc
Collector-Base Voltage	$V_{CB}$	80	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous Peak	$I_C$	8.0 12		Adc
Base Current	$I_B$	0.2		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	60 0.48		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	70	$^\circ\text{C/W}$

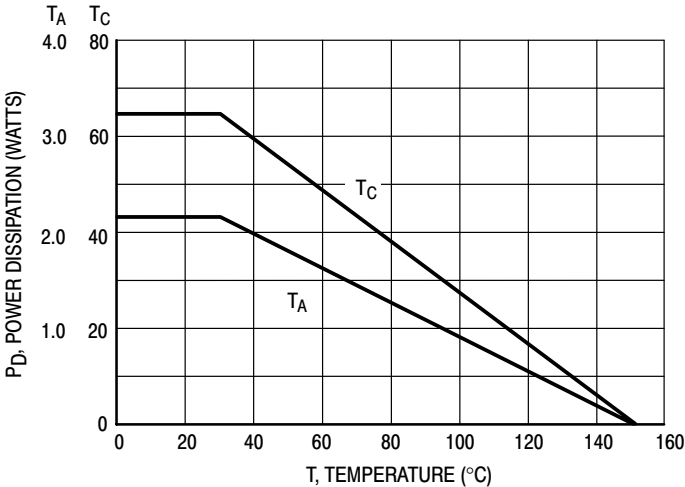
**NPN**  
**BDX53B**  
**BDX53C**  
**PNP**  
**BDX54B**  
**BDX54C**

**DARLINGTON**  
**8 AMPERE**  
**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**80-100 VOLTS**  
**65 WATTS**



**CASE 221A-09**  
**TO-220AB**

**BDX53B BDX53C BDX54B BDX54C**



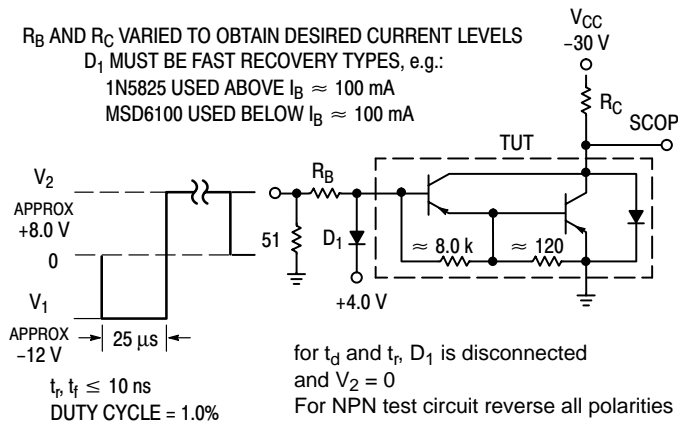
**Figure 1. Power Derating**

# BDX53B BDX53C BDX54B BDX54C

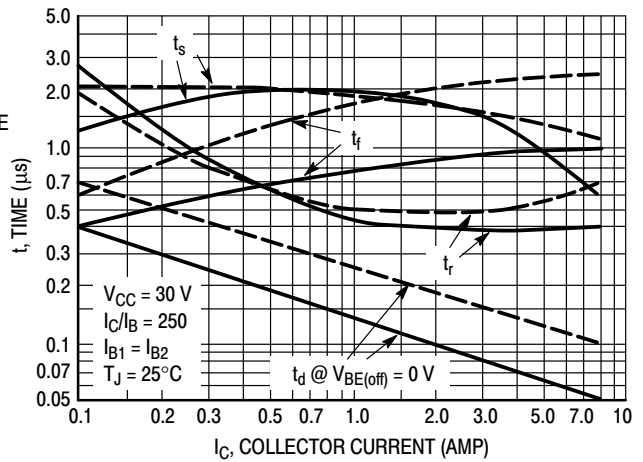
## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (1) ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	BDX53B, BDX54B BDX53C, BDX54C	$V_{CEO(sus)}$	80 100	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )	BDX53B, BDX54B BDX53C, BDX54C	$I_{CEO}$	— —	0.5 0.5	mAdc
Collector Cutoff Current ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	BDX53B, BDX54B BDX53C, BDX54C	$I_{CBO}$	— —	0.2 0.2	mAdc
<b>ON CHARACTERISTICS (1)</b>					
DC Current Gain ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )		$h_{FE}$	750	—	—
Collector–Emitter Saturation Voltage ( $I_C = 3.0\text{ Adc}$ , $I_B = 12\text{ mAdc}$ )		$V_{CE(sat)}$	— —	2.0 4.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 3.0\text{ Adc}$ , $I_C = 12\text{ mA}$ )		$V_{BE(sat)}$	—	2.5	Vdc
<b>DYNAMIC CHARACTERISTICS</b>					
Small–Signal Current Gain ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )		$h_{fe}$	4.0	—	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	BDX53B, 53C BDX54B, 54C	$C_{ob}$	— —	300 200	pF

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

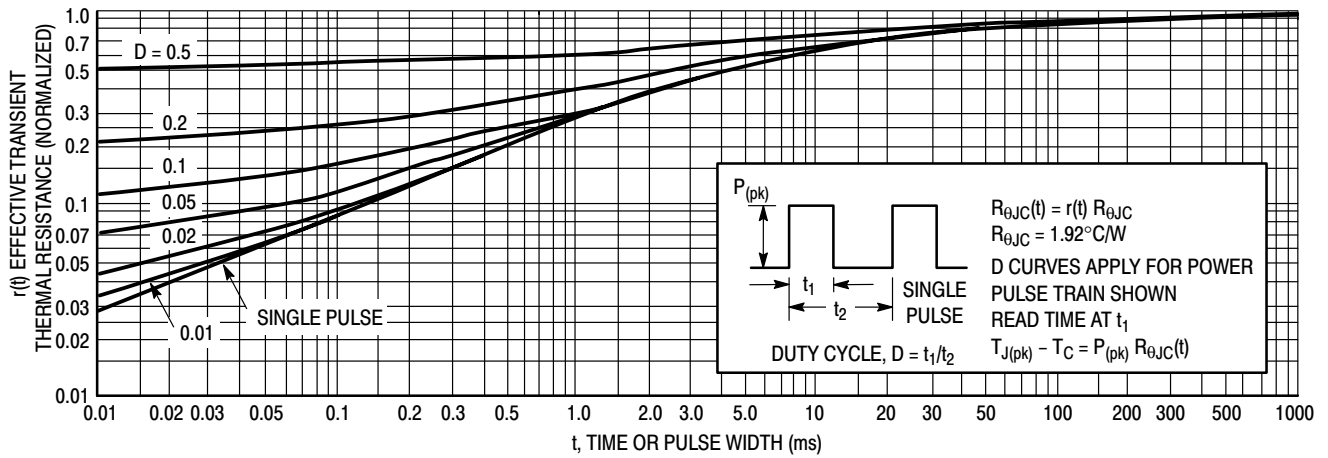


**Figure 2. Switching Time Test Circuit**

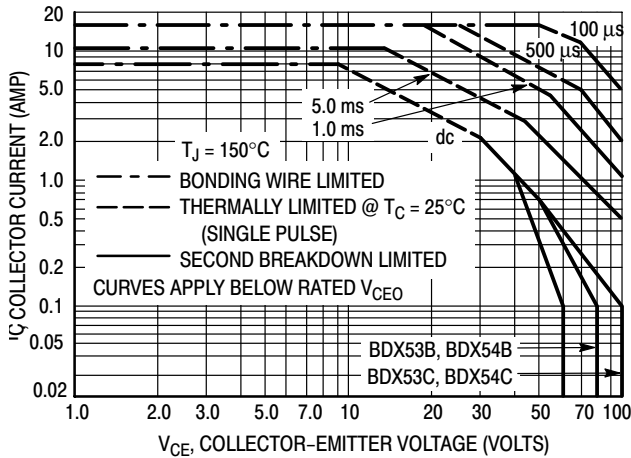


**Figure 3. Switching Times**

# BDX53B BDX53C BDX54B BDX54C



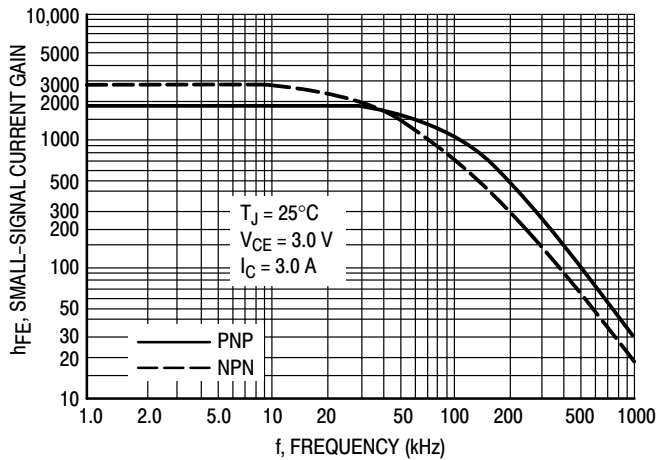
**Figure 4. Thermal Response**



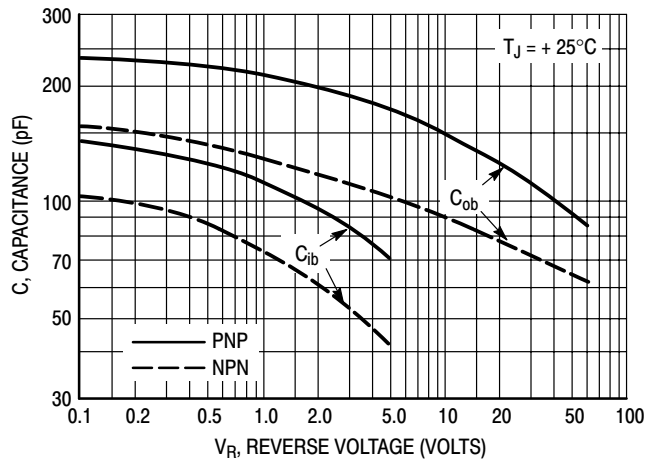
**Figure 5. Active-Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 6. Small-Signal Current Gain**

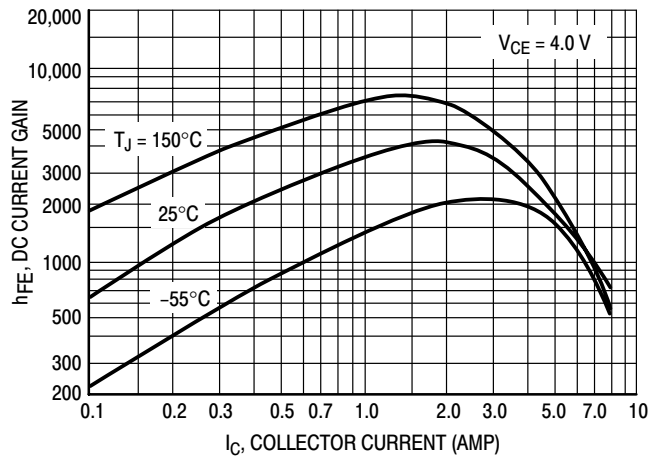
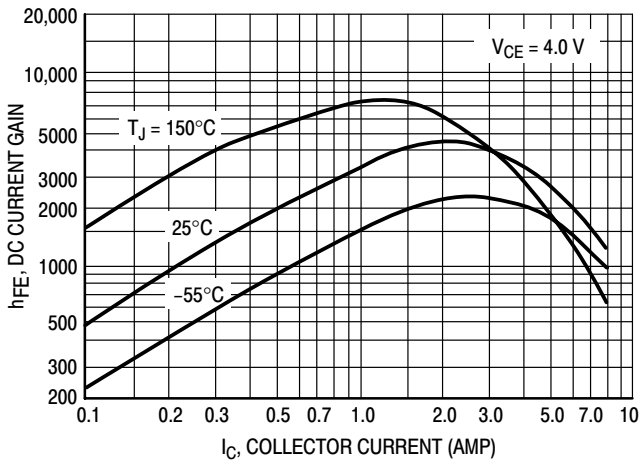


**Figure 7. Capacitance**

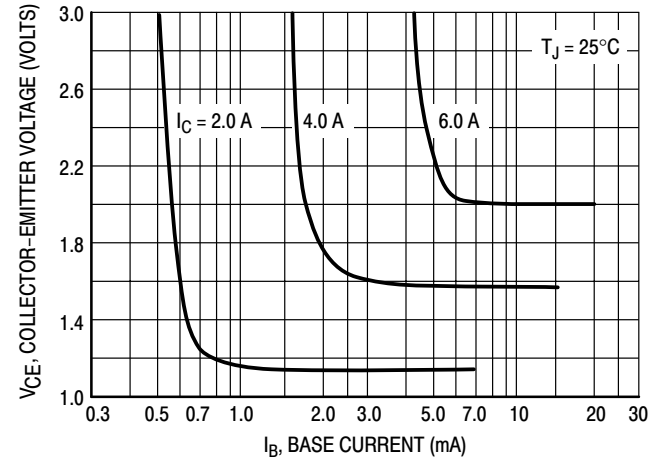
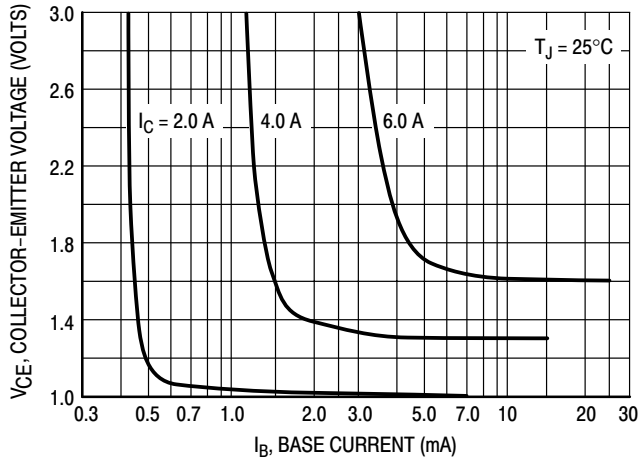
# BDX53B BDX53C BDX54B BDX54C

**NPN**  
**BDX53B, 53C**

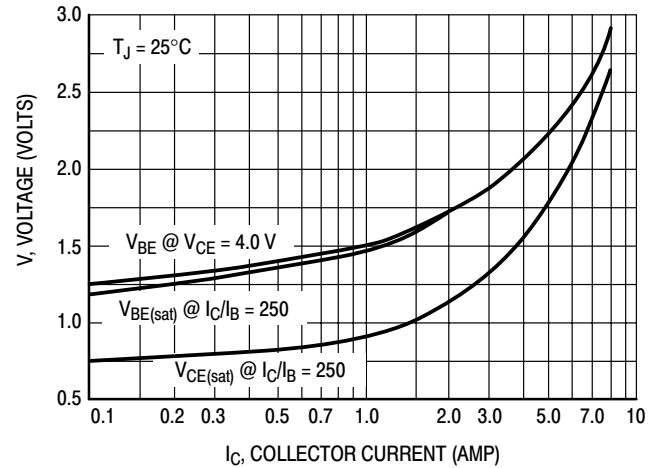
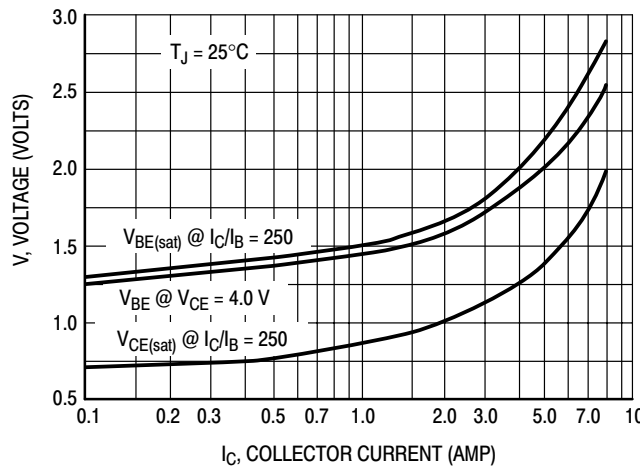
**PNP**  
**BDX54B, 54C**



**Figure 8. DC Current Gain**



**Figure 9. Collector Saturation Region**



**Figure 10. "On" Voltages**



# BDX53B BDX53C BDX54B BDX54C

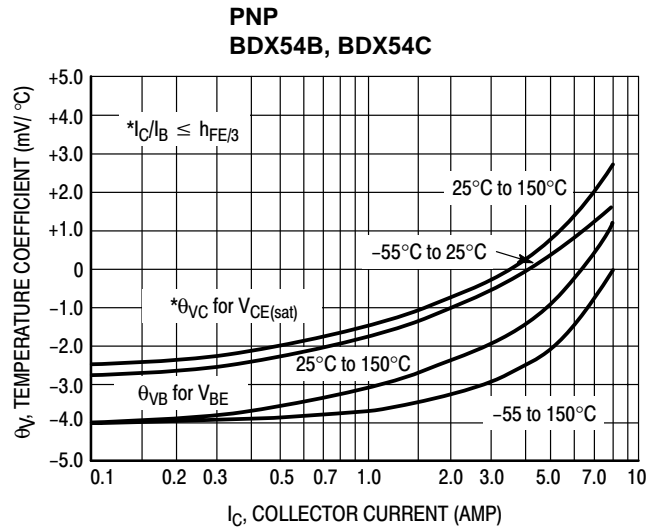
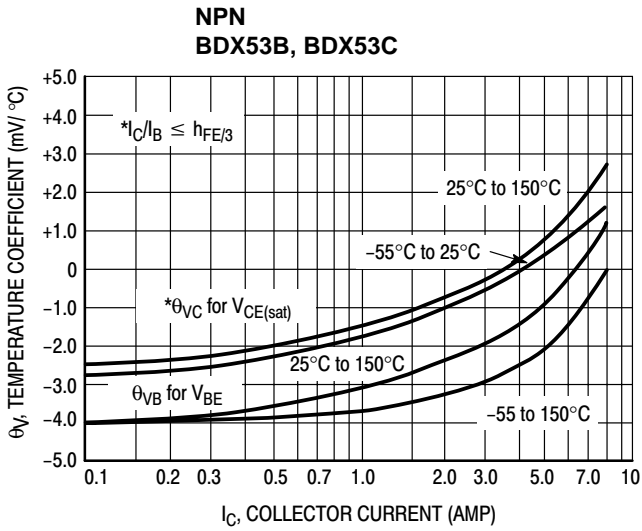


Figure 11. Temperature Coefficients

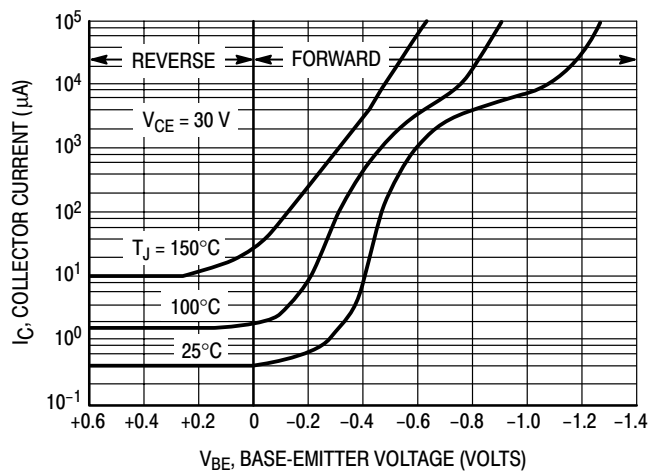
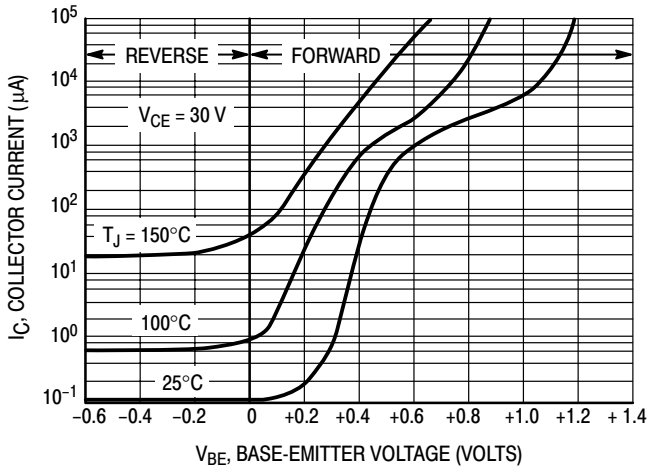


Figure 12. Collector Cut-Off Region

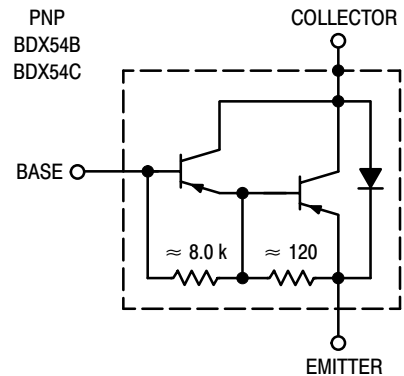
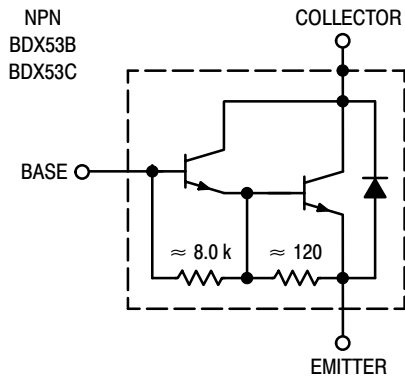
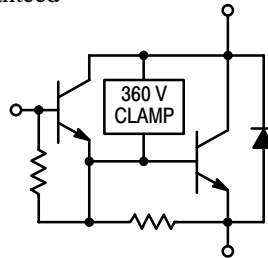


Figure 13. Darlington Schematic

# NPN Silicon Power Darlington High Voltage Autoprotected

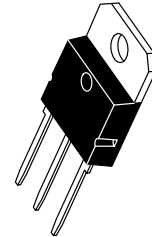
The BU323Z is a planar, monolithic, high-voltage power Darlington with a built-in active zener clamping circuit. This device is specifically designed for unclamped, inductive applications such as Electronic Ignition, Switching Regulators and Motor Control, and exhibit the following main features:

- Integrated High-Voltage Active Clamp
- Tight Clamping Voltage Window (350 V to 450 V) Guaranteed Over the -40°C to +125°C Temperature Range
- Clamping Energy Capability 100% Tested in a Live Ignition Circuit
- High DC Current Gain/Low Saturation Voltages Specified Over Full Temperature Range
- Design Guarantees Operation in SOA at All Times
- Offered in Plastic SOT-93/TO-218 Type or TO-220 Packages



**BU323Z**

**AUTOPROTECTED  
DARLINGTON  
10 AMPERES  
360-450 VOLTS CLAMP  
150 WATTS**



**CASE 340D-02  
SOT-93/TO-218 TYPE**

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	350	Vdc
Collector-Emitter Voltage	$V_{EBO}$	6.0	Vdc
Collector Current — Continuous — Peak	$I_C$ $I_{CM}$	10 20	Adc
Base Current — Continuous — Peak	$I_B$ $I_{BM}$	3.0 6.0	Adc
Total Power Dissipation Derate above 25°C	$P_D$	150 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +175	°C

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	260	°C

# BU323Z

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS (1)</b>					
Collector–Emitter Clamping Voltage ( $I_C = 7.0\text{ A}$ ) ( $T_C = -40^\circ\text{C}$ to $+125^\circ\text{C}$ )	$V_{\text{CLAMP}}$	350	—	450	Vdc
Collector–Emitter Cutoff Current ( $V_{\text{CE}} = 200\text{ V}$ , $I_B = 0$ )	$I_{\text{CEO}}$	—	—	100	$\mu\text{A}$ dc
Emitter–Base Leakage Current ( $V_{\text{EB}} = 6.0\text{ Vdc}$ , $I_C = 0$ )	$I_{\text{EBO}}$	—	—	50	$\text{mA}$ dc

## ON CHARACTERISTICS (1)

Base–Emitter Saturation Voltage ( $I_C = 8.0\text{ Adc}$ , $I_B = 100\text{ mA}$ dc) ( $I_C = 10\text{ Adc}$ , $I_B = 0.25\text{ Adc}$ )	$V_{\text{BE(sat)}}$	— —	— —	2.2 2.5	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 7.0\text{ Adc}$ , $I_B = 70\text{ mA}$ dc)  ( $I_C = 8.0\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )  ( $I_C = 10\text{ Adc}$ , $I_B = 0.25\text{ Adc}$ )	$V_{\text{CE(sat)}}$	— — — —	— — — —	1.6 1.8 1.8 2.1 1.7	Vdc
Base–Emitter On Voltage ( $I_C = 5.0\text{ Adc}$ , $V_{\text{CE}} = 2.0\text{ Vdc}$ ) ( $I_C = 8.0\text{ Adc}$ , $V_{\text{CE}} = 2.0\text{ Vdc}$ )	$V_{\text{BE(on)}}$	1.1 1.3	— —	2.1 2.3	Vdc
Diode Forward Voltage Drop ( $I_F = 10\text{ Adc}$ )	$V_F$	—	—	2.5	Vdc
DC Current Gain ( $I_C = 6.5\text{ Adc}$ , $V_{\text{CE}} = 1.5\text{ Vdc}$ ) ( $I_C = 5.0\text{ Adc}$ , $V_{\text{CE}} = 4.6\text{ Vdc}$ )	$h_{\text{FE}}$	150 500	— —	— 3400	—

## DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 0.2\text{ Adc}$ , $V_{\text{CE}} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	—	—	2.0	MHz
Output Capacitance ( $V_{\text{CB}} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	$C_{\text{ob}}$	—	—	200	pF
Input Capacitance ( $V_{\text{EB}} = 6.0\text{ V}$ )	$C_{\text{ib}}$	—	—	550	pF

## CLAMPING ENERGY (see notes)

Repetitive Non–Destructive Energy Dissipated at turn–off: ( $I_C = 7.0\text{ A}$ , $L = 8.0\text{ mH}$ , $R_{\text{BE}} = 100\ \Omega$ ) (see Figures 2 and 4)	$W_{\text{CLAMP}}$	200	—	—	mJ
---	--------------------	-----	---	---	----

## SWITCHING CHARACTERISTICS: Inductive Load ( $L = 10\text{ mH}$ )

Fall Time	$(I_C = 6.5\text{ A}$ , $I_{\text{B1}} = 45\text{ mA}$ , $V_{\text{BE(off)}} = 0$ , $R_{\text{BE(off)}} = 0$ , $V_{\text{CC}} = 14\text{ V}$ , $V_Z = 300\text{ V}$ )	$t_{\text{fi}}$	—	625	—	ns
Storage Time		$t_{\text{si}}$	—	10	30	$\mu\text{s}$
Cross–over Time		$t_c$	—	1.7	—	$\mu\text{s}$

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle = 2.0%.

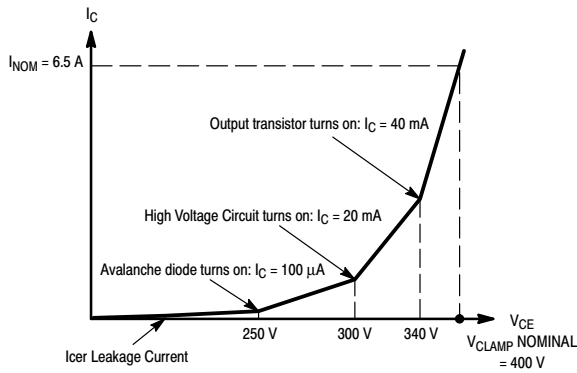


Figure 1.  $I_C = f(V_{CE})$  Curve Shape

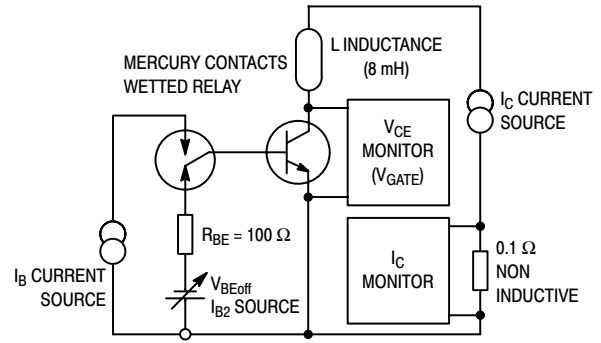


Figure 2. Basic Energy Test Circuit

By design, the BU323Z has a built-in avalanche diode and a special high voltage driving circuit. During an auto-protect cycle, the transistor is turned on again as soon as a voltage, determined by the zener threshold and the network, is reached. This prevents the transistor from going into a Reverse Bias Operating limit condition. Therefore, the device will have an extended safe operating area and will always appear to be in “FBSOA.” Because of the built-in zener and associated network, the  $I_C = f(V_{CE})$  curve exhibits an unfamiliar shape compared to standard products as shown in Figure 1.

The bias parameters,  $V_{CLAMP}$ ,  $I_{B1}$ ,  $V_{BE(off)}$ ,  $I_{B2}$ ,  $I_C$ , and the inductance, are applied according to the Device Under Test (DUT) specifications.  $V_{CE}$  and  $I_C$  are monitored by the test system while making sure the load line remains within the limits as described in Figure 4.

Note: All BU323Z ignition devices are 100% energy tested, per the test circuit and criteria described in Figures 2 and 4, to the minimum guaranteed repetitive energy, as specified in the device parameter section. The device can sustain this energy on a repetitive basis without degrading any of the specified electrical characteristics of the devices. The units under test are kept functional during the complete test sequence for the test conditions described:

$I_{C(peak)} = 7.0 \text{ A}$ ,  $I_{CH} = 5.0 \text{ A}$ ,  $I_{CL} = 100 \text{ mA}$ ,  $I_B = 100 \text{ mA}$ ,  $R_{BE} = 100 \text{ } \Omega$ ,  $V_{gate} = 280 \text{ V}$ ,  $L = 8.0 \text{ mH}$

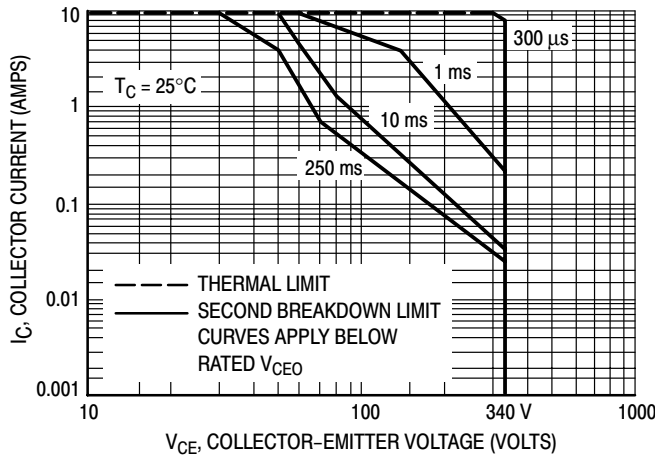
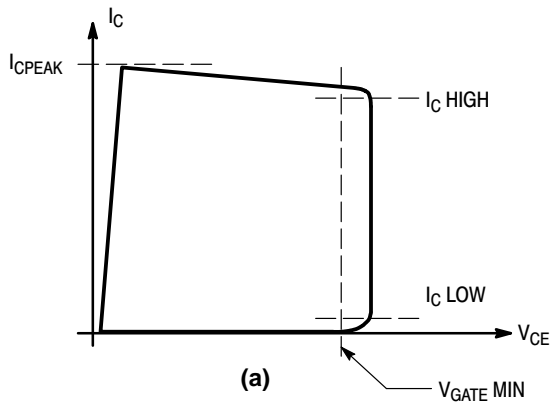
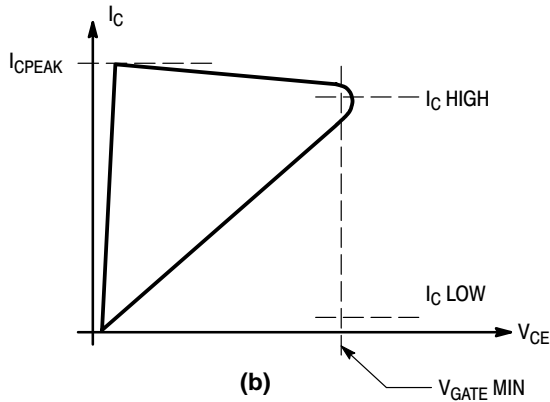


Figure 3. Forward Bias Safe Operating Area

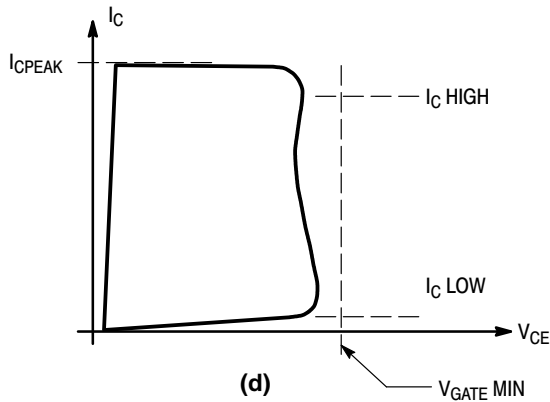
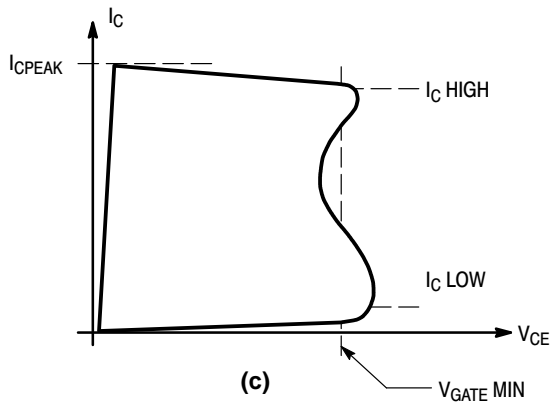


The shaded area represents the amount of energy the device can sustain, under given DC biases ( $I_C/I_B/V_{BE(off)}/R_{BE}$ ), without an external clamp; see the test schematic diagram, Figure 2.

The transistor **PASSES** the Energy test if, for the inductive load and  $I_{CPEAK}/I_B/V_{BE(off)}$  biases, the  $V_{CE}$  remains outside the shaded area and greater than the  $V_{GATE}$  minimum limit, Figure 4a.



The transistor **FAILS** if the  $V_{CE}$  is less than the  $V_{GATE}$  (minimum limit) at any point along the  $V_{CE}/I_C$  curve as shown on Figures 4b, and 4c. This assures that hot spots and uncontrolled avalanche are not being generated in the die, and the transistor is not damaged, thus enabling the sustained energy level required.



The transistor **FAILS** if its Collector/Emitter breakdown voltage is less than the  $V_{GATE}$  value, Figure 4d.

Figure 4. Energy Test Criteria for BU323Z

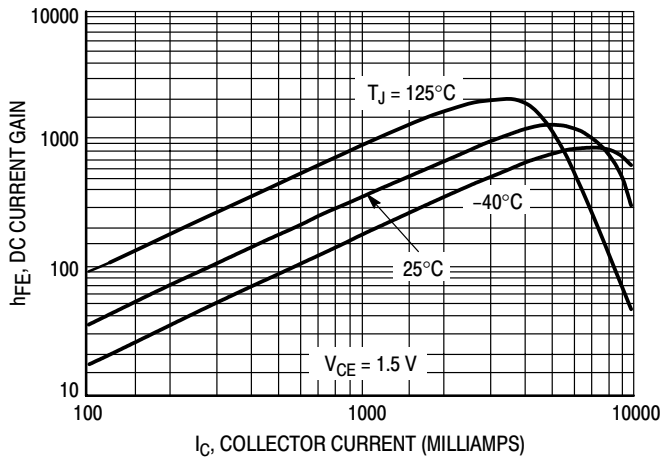


Figure 5. DC Current Gain

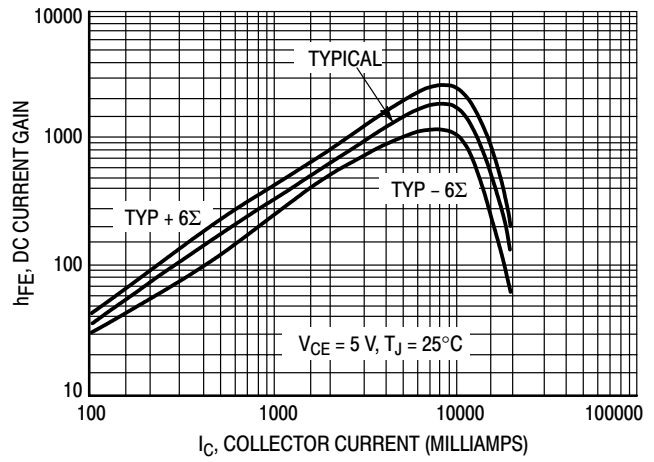


Figure 6. DC Current Gain

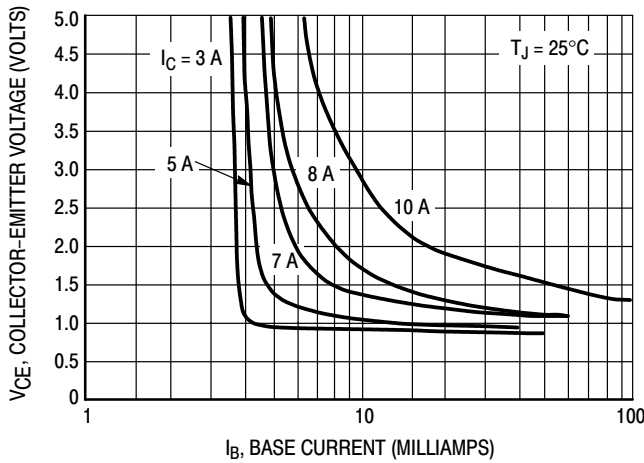


Figure 7. Collector Saturation Region

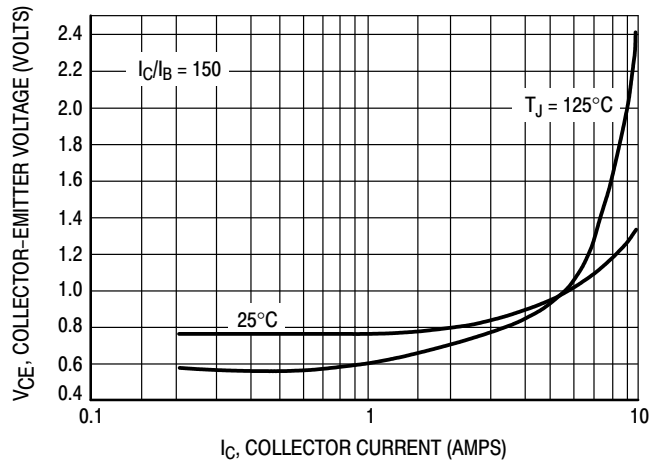


Figure 8. Collector–Emitter Saturation Voltage

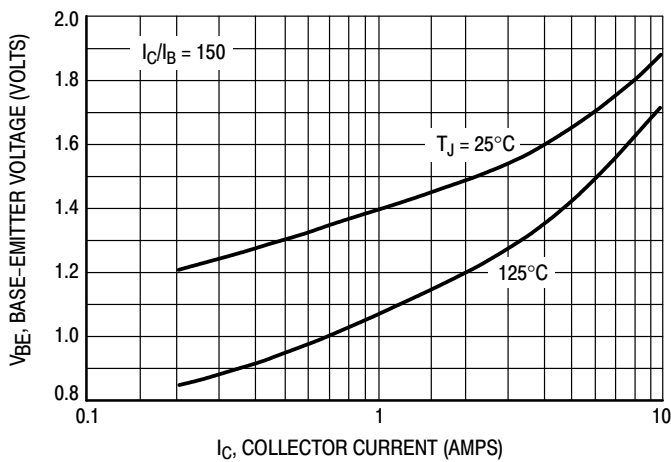


Figure 9. Base–Emitter Saturation Voltage

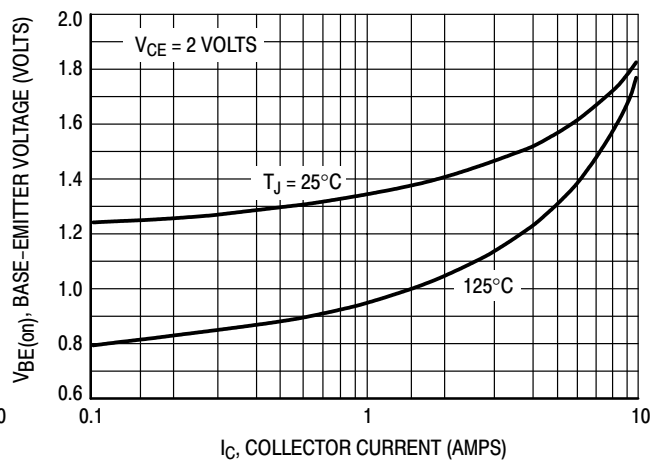


Figure 10. Base–Emitter "ON" Voltages

## NPN Power Transistors

These devices are high voltage, high speed transistors for horizontal deflection output stages of TV's and CRT's.

- High Voltage:  $V_{CEV} = 330$  or  $400$  V
- Fast Switching Speed:  $t_f = 750$  ns (max)
- Low Saturation Voltage:  $V_{CE(sat)} = 1$  V (max) @ 5 A
- Packaged in Compact JEDEC TO-220AB

### MAXIMUM RATINGS

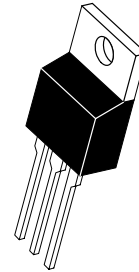
Rating	Symbol	BU406	BU407	Unit
Collector-Emitter Voltage	$V_{CEO}$	200	150	Vdc
Collector-Emitter Voltage	$V_{CEV}$	400	330	Vdc
Collector-Base Voltage	$V_{CBO}$	400	330	Vdc
Emitter Base Voltage	$V_{EBO}$	6		Vdc
Collector Current — Continuous	$I_C$	7		Adc
Peak Repetitive		10		
Peak (10 ms)		15		
Base Current	$I_B$	4		Adc
Total Device Dissipation, $T_C = 25^\circ\text{C}$ Derate above $T_C = 25^\circ\text{C}$	$P_D$	60 0.48		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to 150		$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	$^\circ\text{C}/\text{W}$
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	$^\circ\text{C}$

**BU406**  
**BU407**

**7 AMPERES**  
**NPN SILICON**  
**POWER TRANSISTORS**  
**60 WATTS**  
**150 and 200 VOLTS**



**CASE 221A-09**  
**TO-220AB**

# BU406 BU407

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage <sup>(1)</sup> ( $I_C = 100\text{ mA}$ , $I_B = 0$ )	BU406 BU407	$V_{CEO(sus)}$	200 150	— —	— —	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEV}$ , $V_{BE} = 0$ ) ( $V_{CE} = \text{Rated } V_{CEO} + 50\text{ Vdc}$ , $V_{BE} = 0$ ) ( $V_{CE} = \text{Rated } V_{CEO} + 50\text{ Vdc}$ , $V_{BE} = 0$ , $T_C = 150^\circ\text{C}$ )		$I_{CES}$	— — —	— — —	5 0.1 1	mAdc
Emitter Cutoff Current ( $V_{EB} = 6\text{ Vdc}$ , $I_C = 0$ )	BU406, BU407	$I_{EBO}$	—	—	1	mAdc

### ON CHARACTERISTICS (1)

Collector–Emitter Saturation Voltage ( $I_C = 5\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ )	$V_{CE(sat)}$	—	—	1	Vdc
Base–Emitter Saturation Voltage ( $I_C = 5\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ )	$V_{BE(sat)}$	—	—	1.2	Vdc
Forward Diode Voltage ( $I_{EC} = 5\text{ Adc}$ ) "D" only	$V_{EC}$	—	—	2	Volts

### DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 20\text{ MHz}$ )	$f_T$	10	—	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1\text{ MHz}$ )	$C_{ob}$	—	80	—	pF

### SWITCHING CHARACTERISTICS

Inductive Load Crossover Time ( $V_{CC} = 40\text{ Vdc}$ , $I_C = 5\text{ Adc}$ , $I_{B1} = I_{B2} = 0.5\text{ Adc}$ , $L = 150\text{ }\mu\text{H}$ )	$t_c$	—	—	0.75	$\mu\text{s}$
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(1) Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 1\%$ .

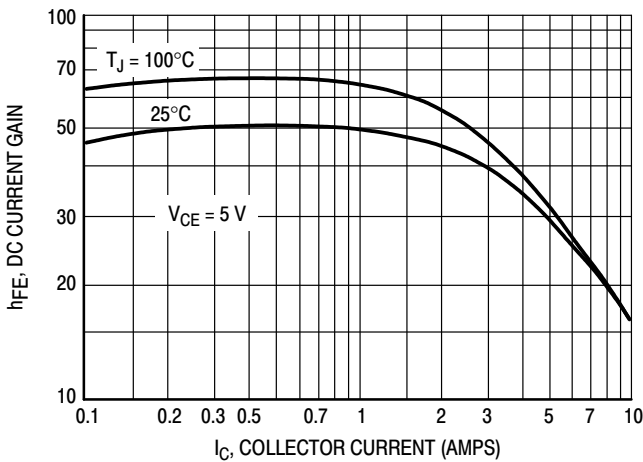


Figure 11. DC Current Gain

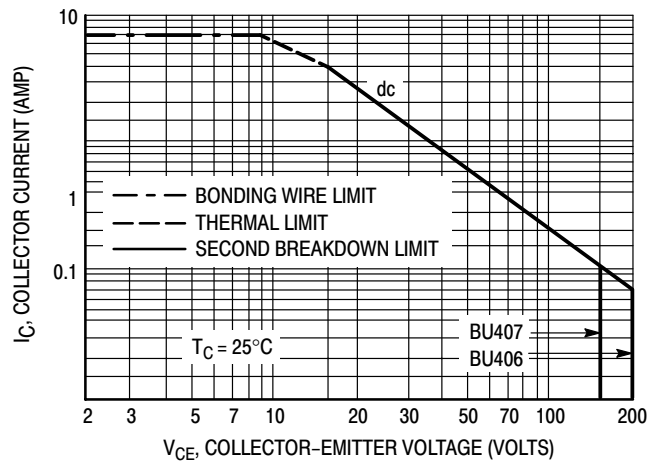


Figure 12. Maximum Rated Forward Bias Safe Operating Area



# High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

The BUD44D2 is state-of-art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread ( $\pm 150$  ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an  $h_{FE}$  window.

**Main features:**

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @  $I_C = 100$  mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector-Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic  $V_{CE(sat)}$
- Six Sigma Process Providing Tight and Reproducible Parameter Spreads
- It's characteristics make it also suitable for PFC application.

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	400	Vdc
Collector-Base Breakdown Voltage	$V_{CBO}$	700	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	700	Vdc
Emitter-Base Voltage	$V_{EBO}$	12	Vdc
Collector Current — Continuous	$I_C$	2	Adc
— Peak (1)	$I_{CM}$	5	
Base Current — Continuous	$I_B$	1	Adc
— Peak (1)	$I_{BM}$	2	
*Total Device Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	25	Watt
*Derate above $25^\circ\text{C}$		0.2	W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150	$^\circ\text{C}$

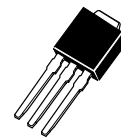
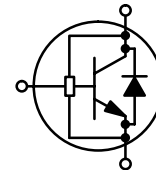
**THERMAL CHARACTERISTICS**

Thermal Resistance			$^\circ\text{C/W}$
— Junction to Case	$R_{\theta JC}$	5	
— Junction to Ambient	$R_{\theta JA}$	71.4	
Maximum Lead Temperature for Soldering Purposes: 1/8" from case for 5 seconds	$T_L$	260	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq 10\%$ .

## BUD44D2

POWER TRANSISTORS  
2 AMPERES  
700 VOLTS  
25 WATTS

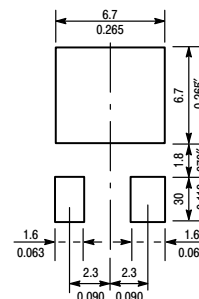


CASE 369-07



CASE 369A-13

**MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS**



# BUD44D2

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CE(sus)}$	400	470		Vdc
Collector–Base Breakdown Voltage ( $I_{CBO} = 1\text{ mA}$ )	$V_{CBO}$	700	920		Vdc
Emitter–Base Breakdown Voltage ( $I_{EBO} = 1\text{ mA}$ )	$V_{EBO}$	12	14.5		Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ $I_{CEO}$			50 500	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )  ( $V_{CE} = 500\text{ V}$ , $V_{EB} = 0$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ $I_{CES}$			50 500 100	$\mu\text{Adc}$
Emitter–Cutoff Current ( $V_{EB} = 10\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$			100	$\mu\text{Adc}$

## ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 0.4\text{ Adc}$ , $I_B = 40\text{ mAdc}$ )  ( $I_C = 1\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{BE(sat)}$		0.78 0.65	0.9 0.8	Vdc
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.87 0.76	1 0.9	
Collector–Emitter Saturation Voltage ( $I_C = 0.4\text{ Adc}$ , $I_B = 20\text{ mAdc}$ )  ( $I_C = 0.4\text{ Adc}$ , $I_B = 40\text{ mAdc}$ )  ( $I_C = 1\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(sat)}$		0.45 0.67	0.65 1	Vdc
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.25 0.27	0.4 0.5	
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.28 0.35	0.5 0.6	
DC Current Gain ( $I_C = 0.4\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )  ( $I_C = 1\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )  ( $I_C = 2\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$h_{FE}$	20 18	32 26		—
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		10 7	14 9.5		
	@ $T_C = 25^\circ\text{C}$		8	11		

## DIODE CHARACTERISTICS

Forward Diode Voltage ( $I_{EC} = 0.2\text{ Adc}$ )  ( $I_{EC} = 0.2\text{ Adc}$ )  ( $I_{EC} = 0.4\text{ Adc}$ )  ( $I_{EC} = 1\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$	$V_{EC}$		0.8	1	V
	@ $T_C = 125^\circ\text{C}$			0.6		
	@ $T_C = 25^\circ\text{C}$			0.9	1.2	
	@ $T_C = 25^\circ\text{C}$			1.1	1.5	
Forward Recovery Time (see Figure 22 bis) ( $I_F = 0.2\text{ Adc}$ , $di/dt = 10\text{ A}/\mu\text{s}$ )  ( $I_F = 0.4\text{ Adc}$ , $di/dt = 10\text{ A}/\mu\text{s}$ )  ( $I_F = 1\text{ Adc}$ , $di/dt = 10\text{ A}/\mu\text{s}$ )	@ $T_C = 25^\circ\text{C}$	$T_{fr}$		415		ns
	@ $T_C = 25^\circ\text{C}$			390		
	@ $T_C = 25^\circ\text{C}$			340		

# BUD44D2

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 1 $\mu\text{s}$ and 3 $\mu\text{s}$ respectively after rising $I_{B1}$ reaches 90% of final $I_{B1}$	$I_C = 0.4\text{ A}$ $I_{B1} = 40\text{ mA}$ $V_{CC} = 300\text{ V}$	@ 1 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(dsat)}$		3.3 6.8		V
		@ 3 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.5 1.3		
	$I_C = 1\text{ A}$ $I_{B1} = 0.2\text{ A}$ $V_{CC} = 300\text{ V}$	@ 1 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			4.4 12.8		
		@ 3 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.5 1.8		

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$f_T$		13		MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1\text{ MHz}$ )	$C_{ob}$		50	75	pF
Input Capacitance ( $V_{EB} = 8\text{ Vdc}$ )	$C_{ib}$		240	500	pF

### SWITCHING CHARACTERISTICS: Resistive Load (D.C. $\leq 10\%$ , Pulse Width = 40 $\mu\text{s}$ )

Turn-on Time	$I_C = 1\text{ Adc}$ , $I_{B1} = 0.2\text{ Adc}$ $I_{B2} = 0.5\text{ Adc}$ $V_{CC} = 300\text{ Vdc}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_{on}$		90 105	150	ns
Turn-off Time		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_{off}$		1.1 1.5	1.25	$\mu\text{s}$
Turn-on Time	$I_C = 0.5\text{ Adc}$ , $I_{B1} = 50\text{ mAdc}$ $I_{B2} = 250\text{ mAdc}$ $V_{CC} = 300\text{ Vdc}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_{on}$	400	600	600	ns
Turn-off Time		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_{off}$	750	1300	1000	ns

## BUD44D2

Characteristic	Symbol	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS: Inductive Load</b> ( $V_{\text{clamp}} = 300 \text{ V}$ , $V_{\text{CC}} = 15 \text{ V}$ , $L = 200 \mu\text{H}$ )					
Fall Time	$I_C = 0.4 \text{ Adc}$ $I_{B1} = 40 \text{ mAdc}$ $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_f$	110 105	150 ns
Storage Time		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_s$	0.55 0.7	0.75 $\mu\text{s}$
Crossover Time		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_c$	85 80	150 ns
Fall Time	$I_C = 1 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_f$	100 90	150 ns
Storage Time		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_s$	1.05 1.45	1.5 $\mu\text{s}$
Crossover Time		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_c$	100 100	175 ns
Fall Time	$I_C = 0.8 \text{ Adc}$ $I_{B1} = 160 \text{ mAdc}$ $I_{B2} = 160 \text{ mAdc}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_f$	110 180	150 ns
Storage Time		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_s$	2.05 2.8	2.35 $\mu\text{s}$
Crossover Time		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_c$	180 400	300 ns
Fall Time	$I_C = 0.4 \text{ Adc}$ $I_{B1} = 40 \text{ mAdc}$ $I_{B2} = 40 \text{ mAdc}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_f$	150 175	225 ns
Storage Time		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_s$	1.65 2.2	1.95 $\mu\text{s}$
Crossover Time		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$t_c$	150 330	250 ns

TYPICAL STATIC CHARACTERISTICS

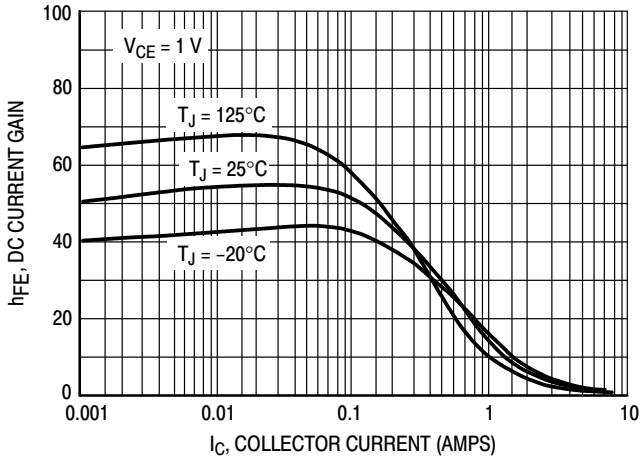


Figure 13. DC Current Gain @ 1 Volt

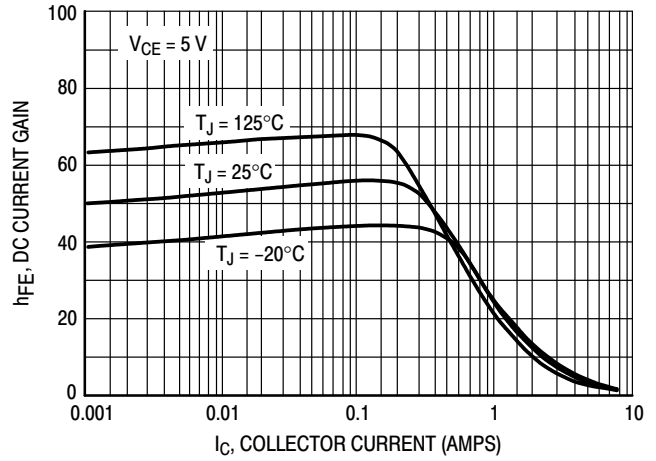


Figure 14. DC Current Gain @ 5 Volt

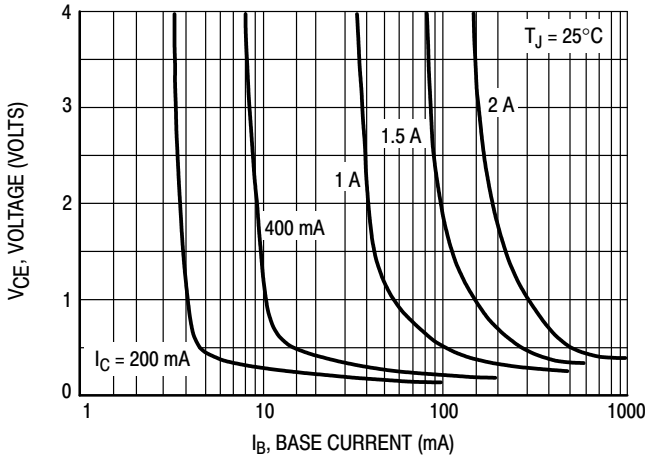


Figure 15. Collector Saturation Region

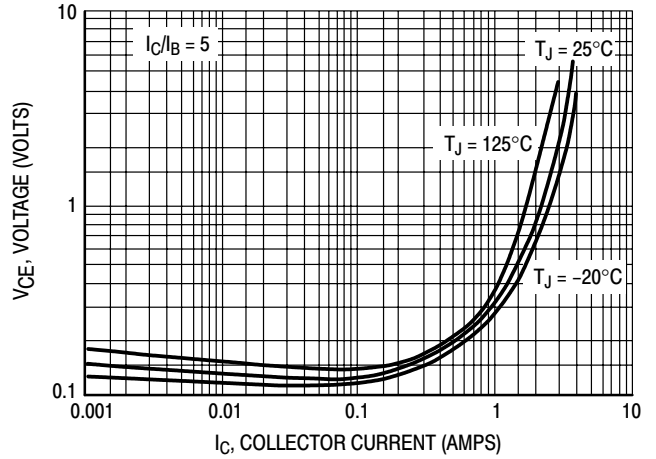


Figure 16. Collector-Emitter Saturation Voltage

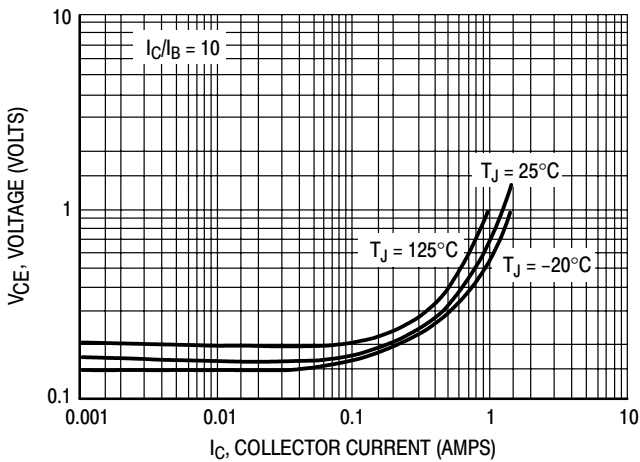


Figure 17. Collector-Emitter Saturation Voltage

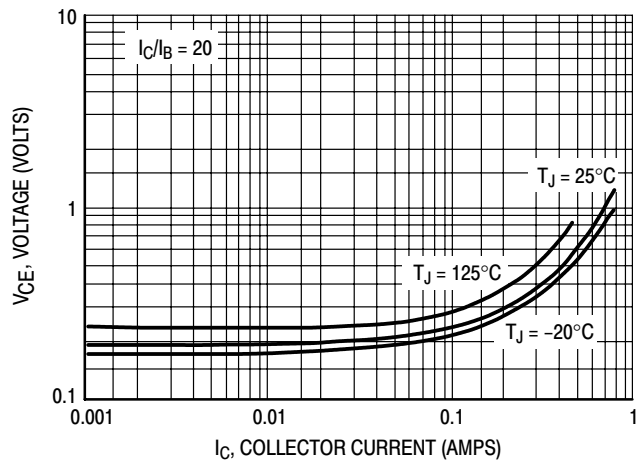


Figure 18. Collector-Emitter Saturation Voltage

# BUD44D2

## TYPICAL STATIC CHARACTERISTICS

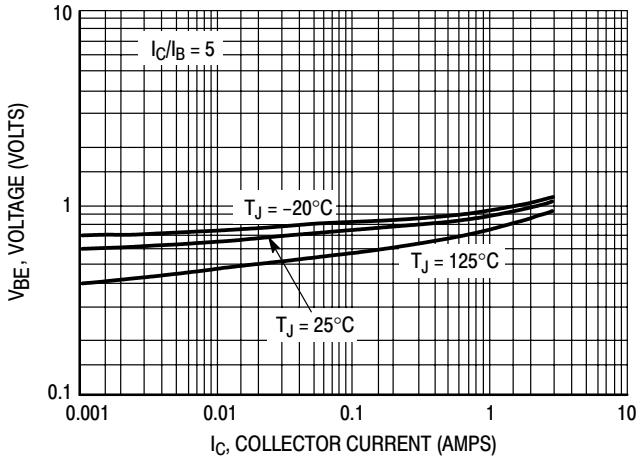


Figure 7A. Base-Emitter Saturation Region

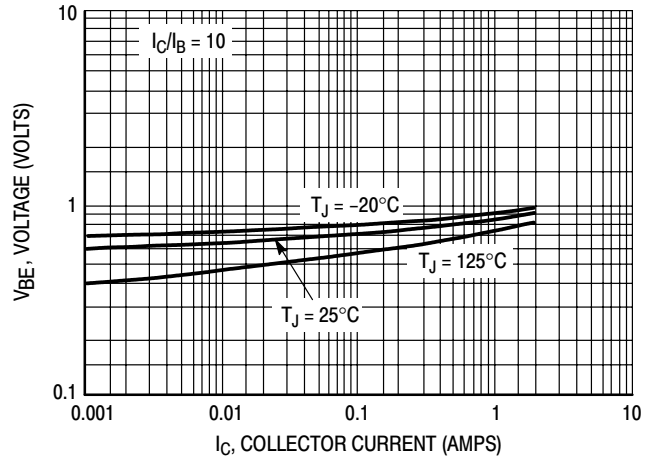


Figure 7B. Base-Emitter Saturation Region

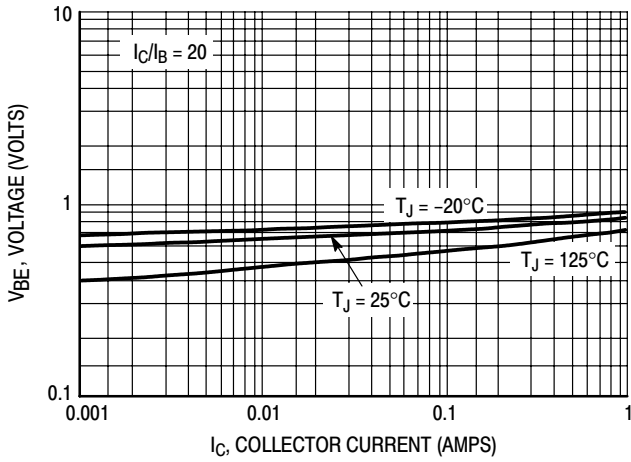


Figure 7C. Base-Emitter Saturation Region

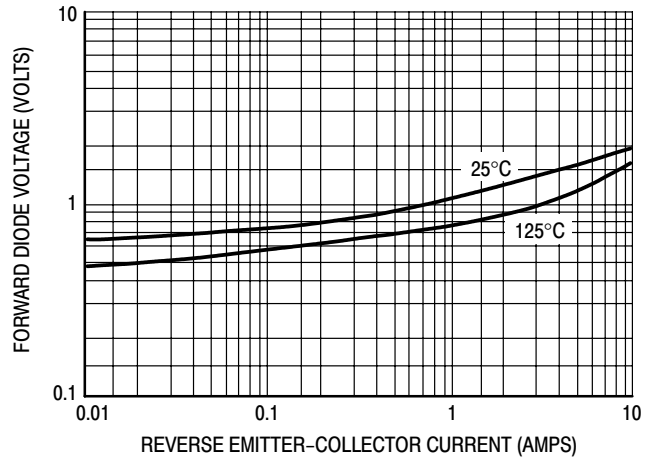


Figure 8. Forward Diode Voltage

TYPICAL SWITCHING CHARACTERISTICS

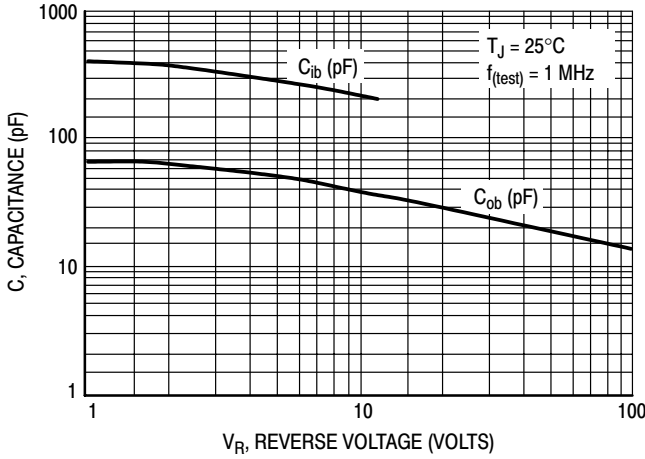


Figure 9. Capacitance

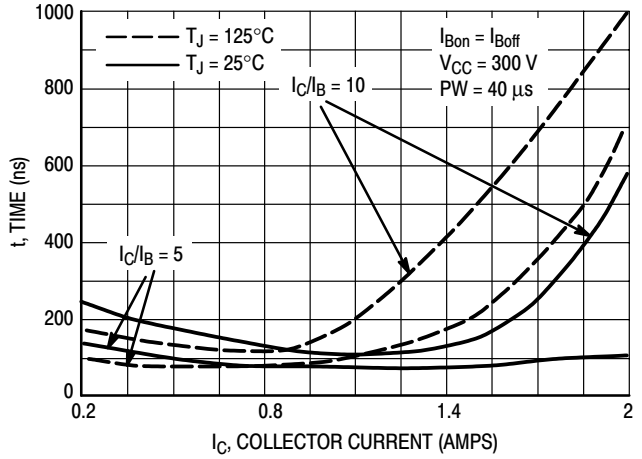


Figure 10. Resistive Switch Time,  $t_{on}$

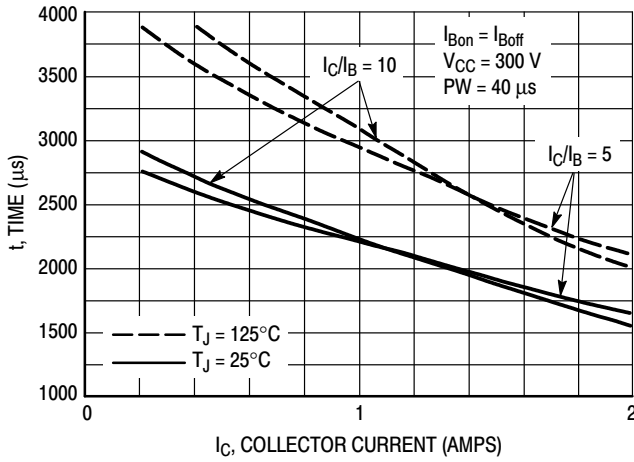


Figure 11. Resistive Switch Time,  $t_{off}$

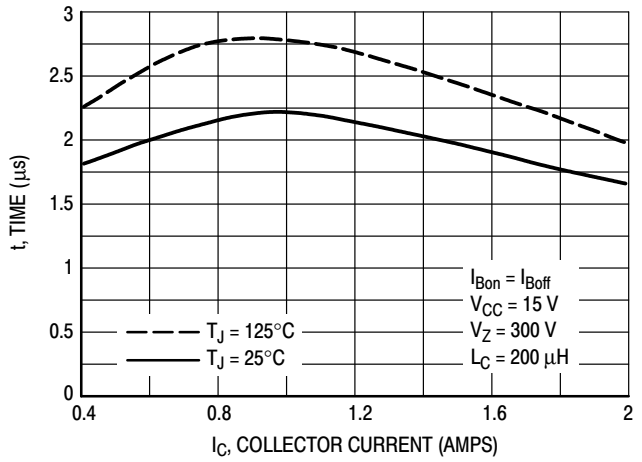


Figure 12. Inductive Storage Time,  $t_{si}$  @  $I_C/I_B = 5$

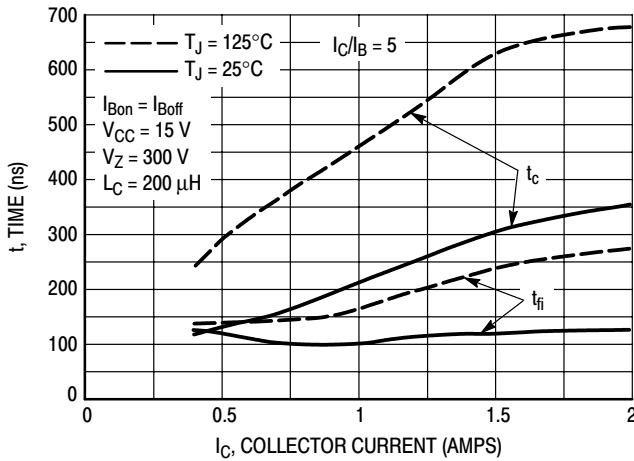


Figure 13. Inductive Switching,  $t_c$  &  $t_{rf}$  @  $I_C/I_B = 5$

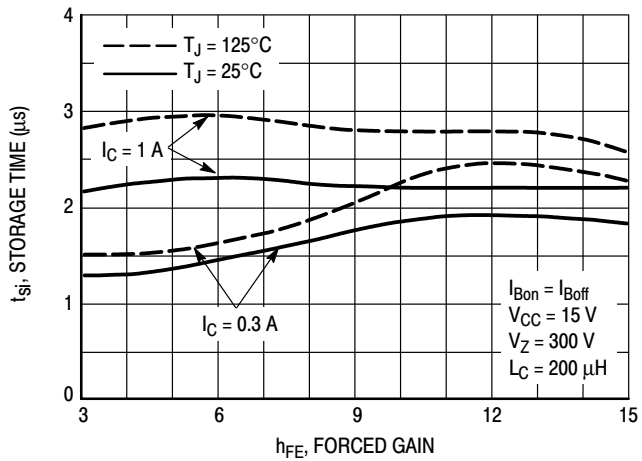


Figure 14. Inductive Storage Time

TYPICAL SWITCHING CHARACTERISTICS

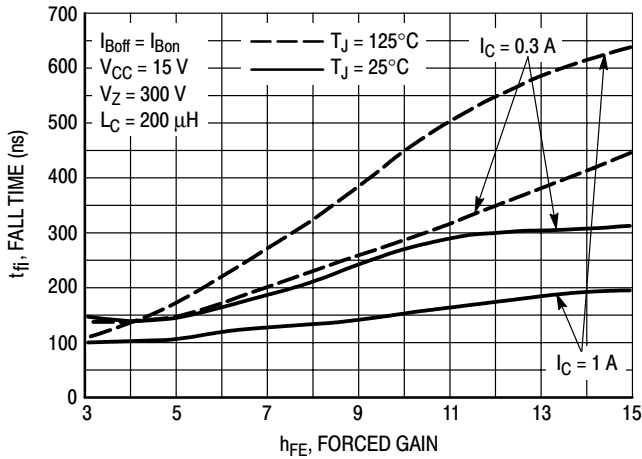


Figure 15. Inductive Fall Time

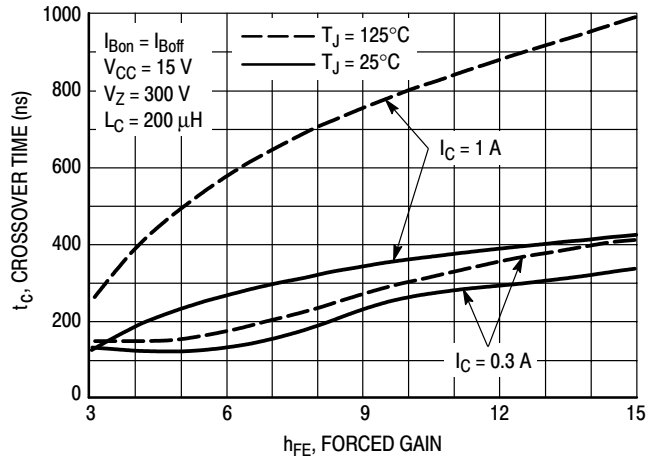


Figure 16. Inductive Crossover Time

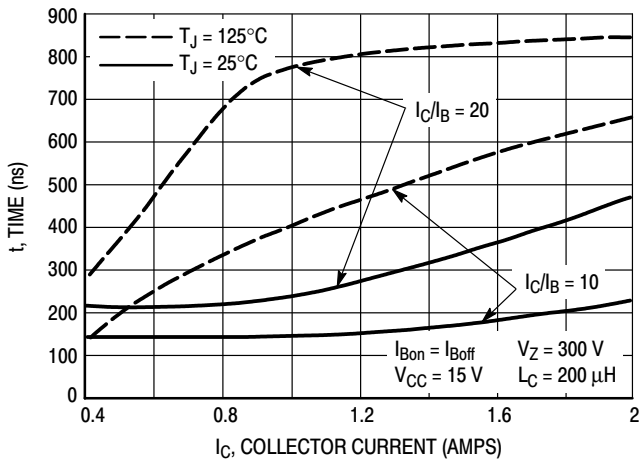


Figure 17. Inductive Switching,  $t_{fi}$

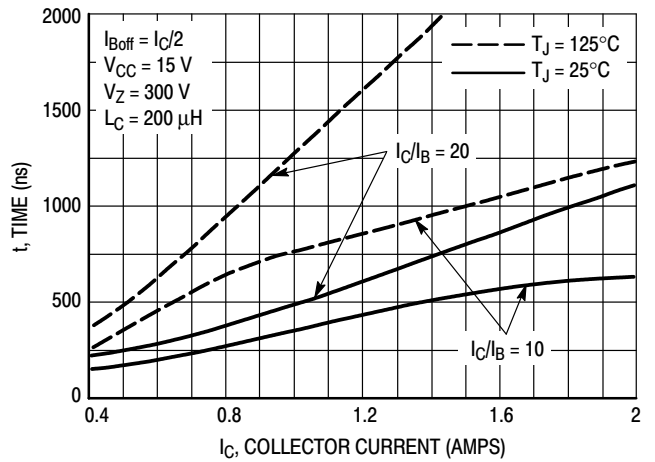


Figure 18. Inductive Switching,  $t_c$

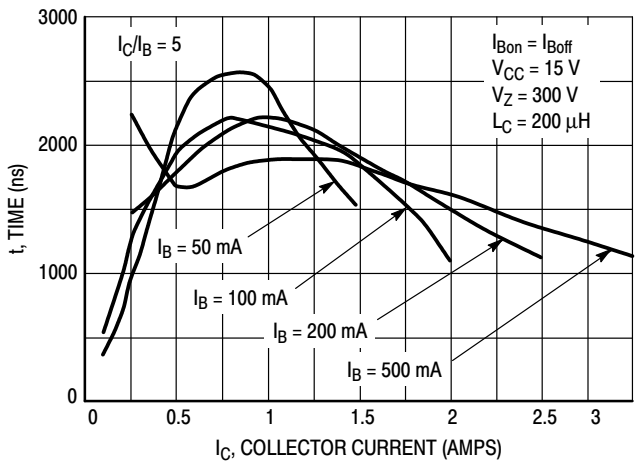


Figure 19. Inductive Storage Time,  $t_{si}$

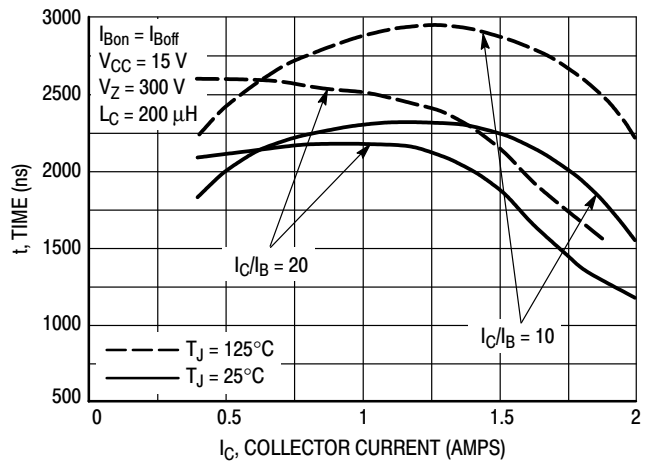


Figure 20. Inductive Storage Time,  $t_{si}$



# BUD44D2

## TYPICAL SWITCHING CHARACTERISTICS

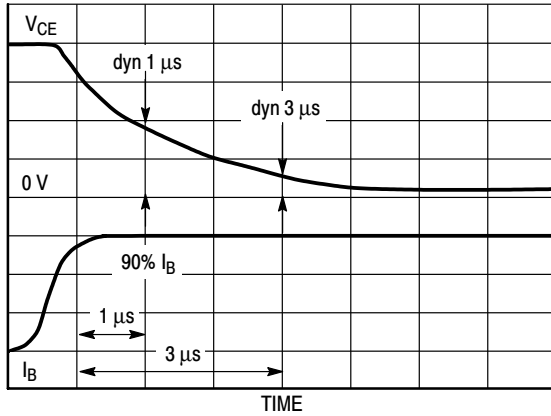


Figure 21. Dynamic Saturation Voltage Measurements

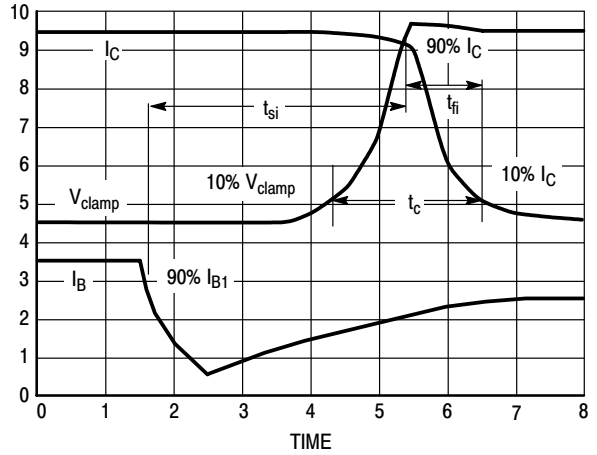


Figure 22. Inductive Switching Measurements

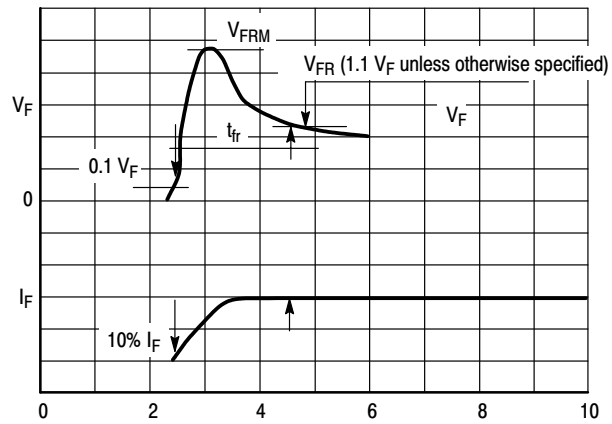
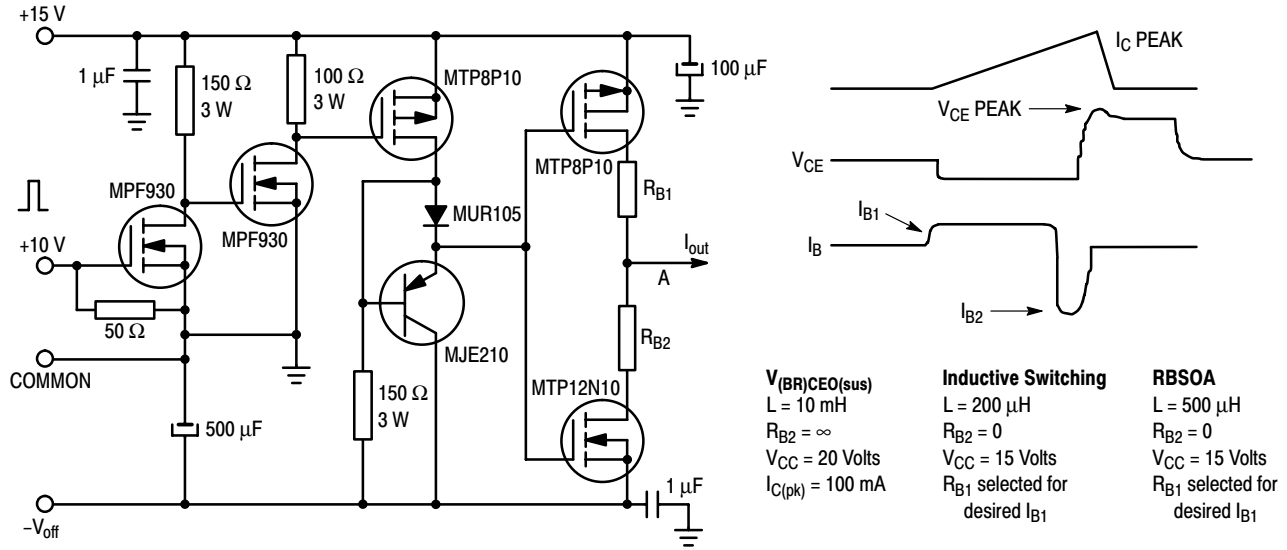


Figure 22 bis.  $t_{fr}$  Measurements

# BUD44D2

## TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



## TYPICAL STATIC CHARACTERISTICS

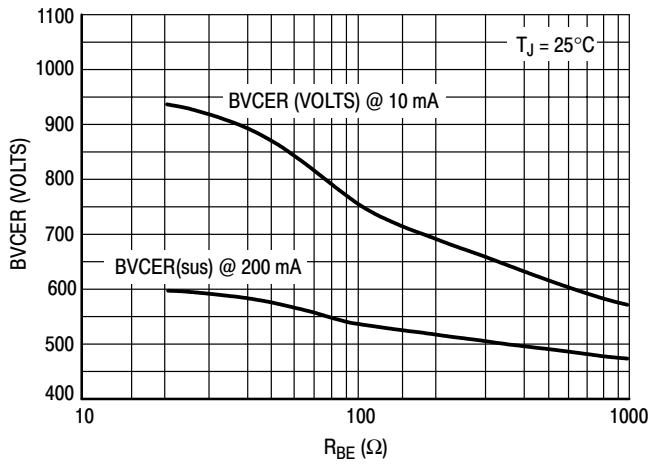


Figure 23. BV<sub>CEr</sub>

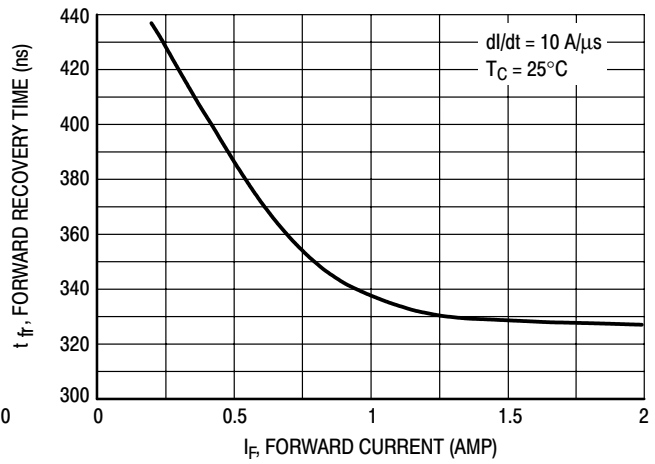


Figure 24. Forward Recovery Time t<sub>fr</sub>

## SWITCHMODE™ NPN Silicon Planar Power Transistor

The BUH100 has an application specific state-of-art die designed for use in 100 Watts Halogen electronic transformers.

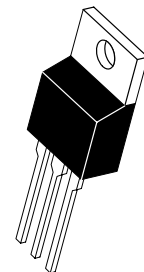
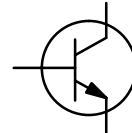
This power transistor is specifically designed to sustain the large inrush current during either the start-up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:  
High and Flat DC Current Gain  $h_{FE}$   
Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions

# BUH100

POWER TRANSISTOR  
10 AMPERES  
700 VOLTS  
100 WATTS



CASE 221A-09  
TO-220AB

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	400	Vdc
Collector-Base Breakdown Voltage	$V_{CBO}$	700	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	700	Vdc
Emitter-Base Voltage	$V_{EBO}$	10	Vdc
Collector Current — Continuous — Peak (1)	$I_C$ $I_{CM}$	10 20	Adc
Base Current — Continuous — Peak (1)	$I_B$ $I_{BM}$	4 10	Adc
*Total Device Dissipation @ $T_C = 25^\circ\text{C}$ *Derate above $25^\circ\text{C}$	$P_D$	100 0.8	Watt W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from case for 5 seconds	$T_L$	260	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq$  10%.

# BUH100

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	400	460		Vdc
Collector–Base Breakdown Voltage ( $I_{CBO} = 1\text{ mA}$ )	$V_{CBO}$	700	860		Vdc
Emitter–Base Breakdown Voltage ( $I_{EBO} = 1\text{ mA}$ )	$V_{EBO}$	10	12.5		Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$			100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$I_{CES}$		100 1000	$\mu\text{Adc}$
Collector Base Current ( $V_{CB} = \text{Rated } V_{CBO}$ , $V_{EB} = 0$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$I_{CBO}$		100 1000	$\mu\text{Adc}$
Emitter–Cutoff Current ( $V_{EB} = 9\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$			100	$\mu\text{Adc}$

## ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 5\text{ Adc}$ , $I_B = 1\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$	$V_{BE(sat)}$		1	1.1	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 5\text{ Adc}$ , $I_B = 1\text{ Adc}$ )  ( $I_C = 7\text{ Adc}$ , $I_B = 1.5\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(sat)}$		0.37 0.37	0.6 0.6	Vdc
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.5 0.6	0.75 1.5	Vdc
DC Current Gain ( $I_C = 1\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )  ( $I_C = 5\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )  ( $I_C = 7\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )  ( $I_C = 10\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$h_{FE}$	15 16	24 28		—
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		10 10	15 14.5		—
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		8 7	12 10.5		—
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		6 4	9.5 8		—

## DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 3 $\mu\text{s}$ after rising $I_{B1}$ reaches 90% of final $I_{B1}$ (See Figure 19)	$I_C = 5\text{ Adc}$ , $I_{B1} = 1\text{ Adc}$ $V_{CC} = 300\text{ V}$	@ $T_C = 25^\circ\text{C}$	$V_{CE(dsat)}$		1.1		V
		@ $T_C = 125^\circ\text{C}$			2.1		V
	$I_C = 7.5\text{ Adc}$ , $I_{B1} = 1.5\text{ Adc}$ $V_{CC} = 300\text{ V}$	@ $T_C = 25^\circ\text{C}$			1.7		V
		@ $T_C = 125^\circ\text{C}$			5		V

## DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$f_T$		23		MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1\text{ MHz}$ )	$C_{ob}$		100	150	pF
Input Capacitance ( $V_{EB} = 8\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$C_{ib}$		1300	1750	pF

# BUH100

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)

Turn-on Time	I <sub>C</sub> = 1 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.2 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C	t <sub>on</sub>		130	200	ns
Turn-off Time		@ T <sub>C</sub> = 125°C			140		
Turn-on Time	I <sub>C</sub> = 1 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.4 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C	t <sub>on</sub>		140	200	ns
Turn-off Time		@ T <sub>C</sub> = 125°C			150		
Turn-on Time	I <sub>C</sub> = 5 Adc, I <sub>B1</sub> = 1 Adc I <sub>B2</sub> = 1 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C	t <sub>on</sub>		250	500	ns
Turn-off Time		@ T <sub>C</sub> = 125°C			800		
Turn-on Time	I <sub>C</sub> = 7.5 Adc, I <sub>B1</sub> = 1.5 Adc I <sub>B2</sub> = 1.5 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C	t <sub>on</sub>		500	700	ns
Turn-off Time		@ T <sub>C</sub> = 125°C			900		
Turn-on Time	I <sub>C</sub> = 1 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.2 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C	t <sub>off</sub>		6.8	8	μs
Turn-off Time		@ T <sub>C</sub> = 125°C			8.5		
Turn-on Time	I <sub>C</sub> = 1 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.4 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C	t <sub>off</sub>		3.4	4	μs
Turn-off Time		@ T <sub>C</sub> = 125°C			4.3		
Turn-on Time	I <sub>C</sub> = 5 Adc, I <sub>B1</sub> = 1 Adc I <sub>B2</sub> = 1 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C	t <sub>off</sub>		2.9	3.5	μs
Turn-off Time		@ T <sub>C</sub> = 125°C			3.6		
Turn-on Time	I <sub>C</sub> = 7.5 Adc, I <sub>B1</sub> = 1.5 Adc I <sub>B2</sub> = 1.5 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C	t <sub>off</sub>		2.1	2.5	μs
Turn-off Time		@ T <sub>C</sub> = 125°C			2.5		

### SWITCHING CHARACTERISTICS: Inductive Load (V<sub>clamp</sub> = 300 V, V<sub>CC</sub> = 15 V, L = 200 μH)

Fall Time	I <sub>C</sub> = 1 Adc I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.2 Adc	@ T <sub>C</sub> = 25°C	t <sub>fi</sub>		150	250	ns
Storage Time		@ T <sub>C</sub> = 125°C			180		
Crossover Time		@ T <sub>C</sub> = 25°C	t <sub>si</sub>		5.1	6	μs
Fall Time	I <sub>C</sub> = 1 Adc I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.5 Adc	@ T <sub>C</sub> = 125°C			5.8		
Storage Time		@ T <sub>C</sub> = 25°C	t <sub>c</sub>		230	325	ns
Crossover Time		@ T <sub>C</sub> = 125°C			300		
Fall Time	I <sub>C</sub> = 1 Adc I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.5 Adc	@ T <sub>C</sub> = 25°C	t <sub>fi</sub>		150	250	ns
Storage Time		@ T <sub>C</sub> = 125°C			170		
Crossover Time		@ T <sub>C</sub> = 25°C	t <sub>si</sub>		2.5	3	μs
Fall Time	I <sub>C</sub> = 5 Adc I <sub>B1</sub> = 1 Adc I <sub>B2</sub> = 1 Adc	@ T <sub>C</sub> = 125°C			2.8		
Storage Time		@ T <sub>C</sub> = 25°C	t <sub>c</sub>		260	350	ns
Crossover Time		@ T <sub>C</sub> = 125°C			300		
Fall Time	I <sub>C</sub> = 5 Adc I <sub>B1</sub> = 1 Adc I <sub>B2</sub> = 1 Adc	@ T <sub>C</sub> = 25°C	t <sub>fi</sub>		100	150	ns
Storage Time		@ T <sub>C</sub> = 125°C			140		
Crossover Time		@ T <sub>C</sub> = 25°C	t <sub>si</sub>		2.9	3.5	μs
Fall Time	I <sub>C</sub> = 7.5 Adc I <sub>B1</sub> = 1.5 Adc I <sub>B2</sub> = 1.5 Adc	@ T <sub>C</sub> = 125°C			4.6		
Storage Time		@ T <sub>C</sub> = 25°C	t <sub>c</sub>		220	300	ns
Crossover Time		@ T <sub>C</sub> = 125°C			450		
Fall Time	I <sub>C</sub> = 7.5 Adc I <sub>B1</sub> = 1.5 Adc I <sub>B2</sub> = 1.5 Adc	@ T <sub>C</sub> = 25°C	t <sub>fi</sub>		100	150	ns
Storage Time		@ T <sub>C</sub> = 125°C			150		
Crossover Time		@ T <sub>C</sub> = 25°C	t <sub>si</sub>		2	2.5	μs
Fall Time	I <sub>C</sub> = 7.5 Adc I <sub>B1</sub> = 1.5 Adc I <sub>B2</sub> = 1.5 Adc	@ T <sub>C</sub> = 125°C			2.5		
Storage Time		@ T <sub>C</sub> = 25°C	t <sub>c</sub>		250	350	ns
Crossover Time		@ T <sub>C</sub> = 125°C			475		

TYPICAL STATIC CHARACTERISTICS

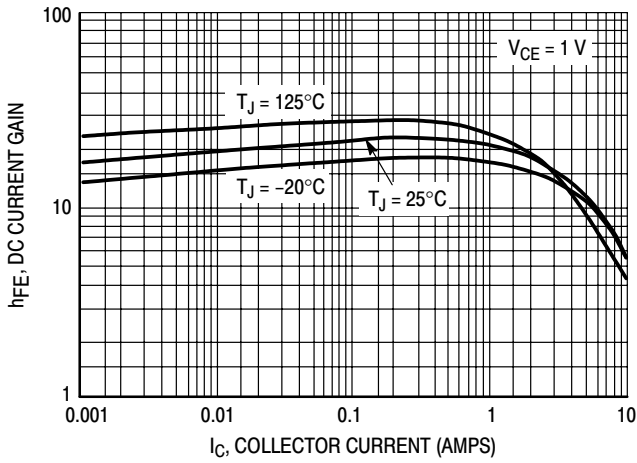


Figure 19. DC Current Gain @ 1 Volt

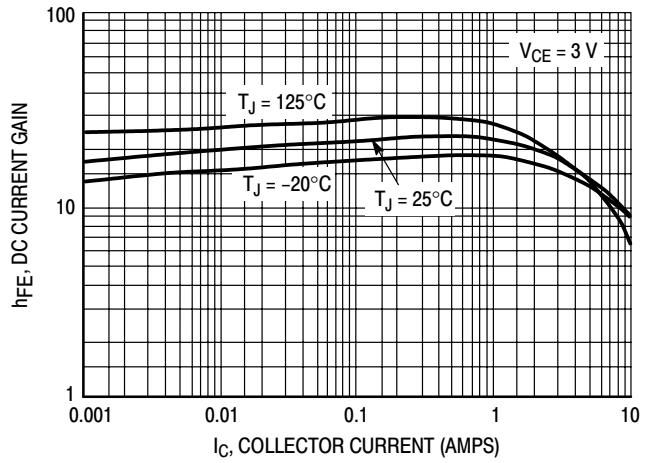


Figure 20. DC Current Gain @ 3 Volt

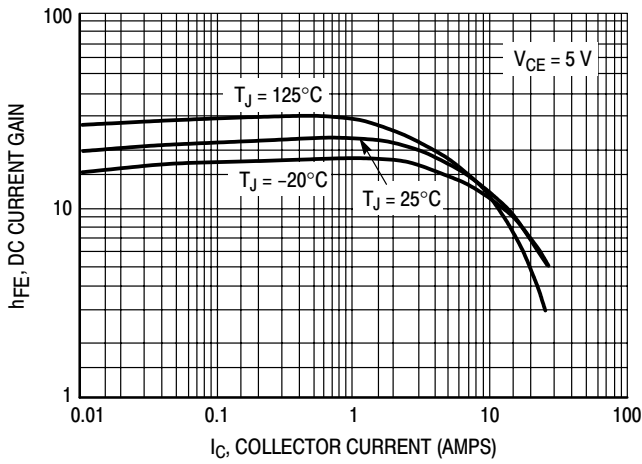


Figure 21. DC Current Gain @ 5 Volt

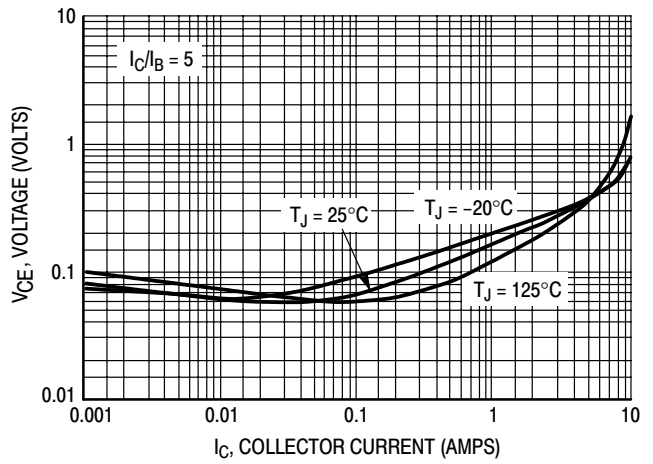


Figure 22. Collector-Emitter Saturation Voltage

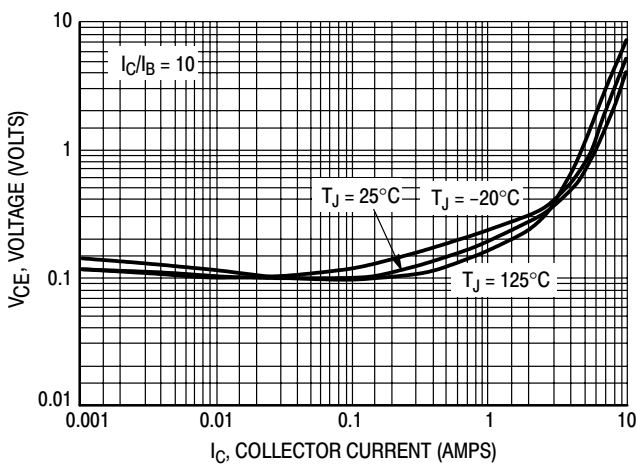


Figure 23. Collector-Emitter Saturation Voltage

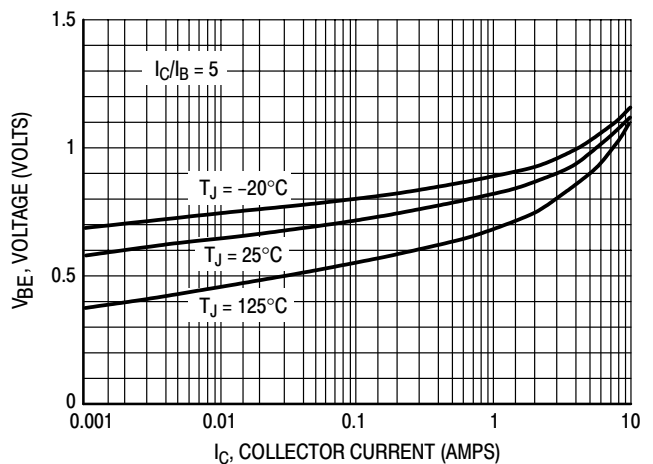


Figure 24. Base-Emitter Saturation Region

TYPICAL STATIC CHARACTERISTICS

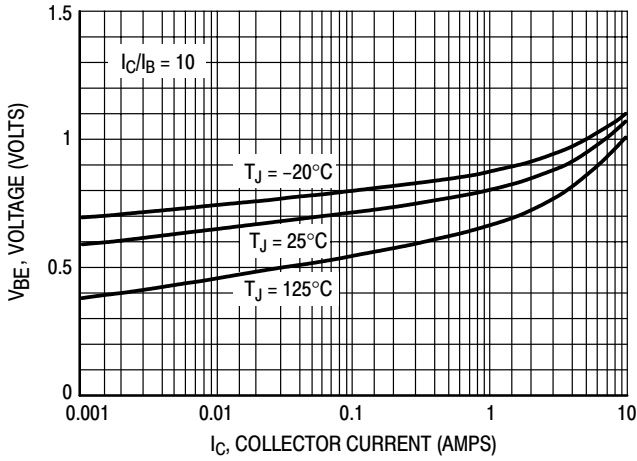


Figure 25. Base-Emitter Saturation Region

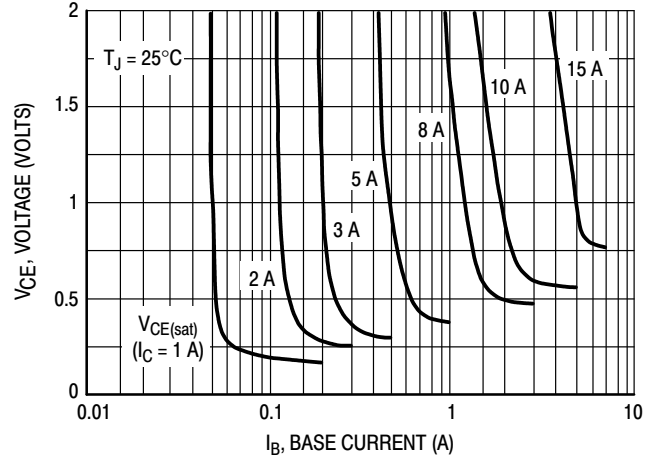


Figure 26. Collector Saturation Region

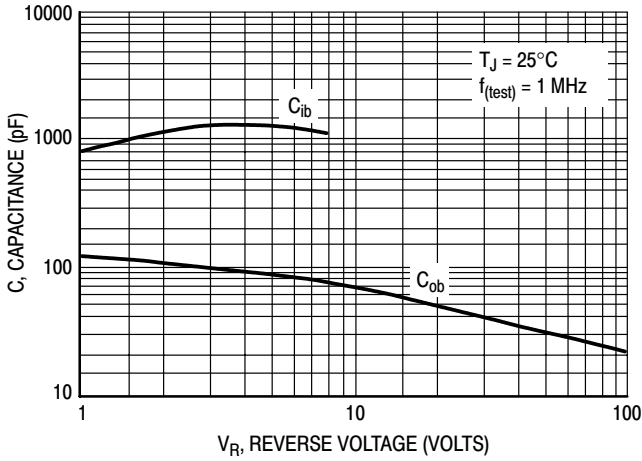


Figure 27. Capacitance

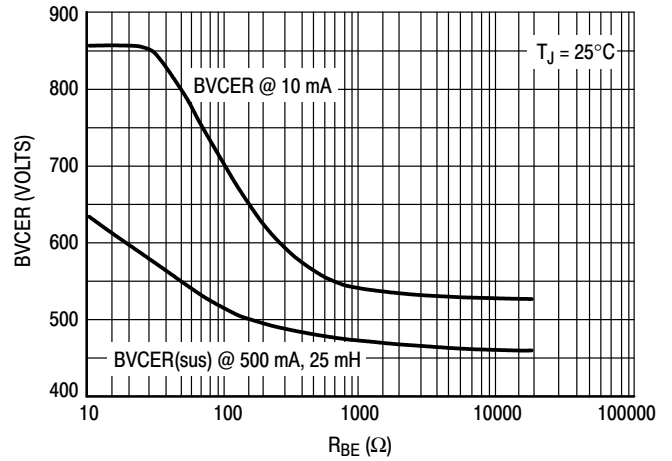


Figure 28. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

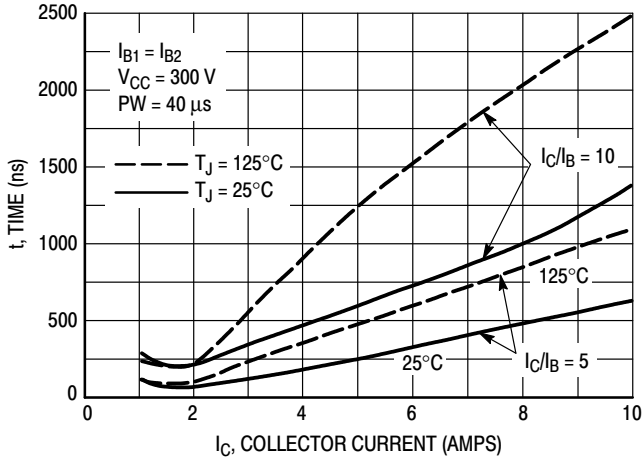


Figure 29. Resistive Switching Time,  $t_{on}$

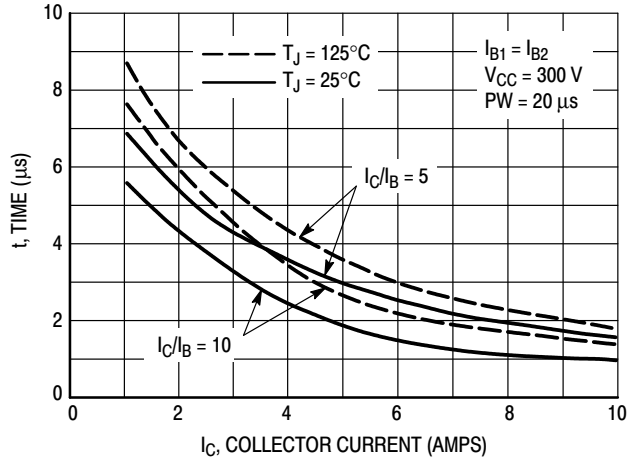


Figure 30. Resistive Switch Time,  $t_{off}$

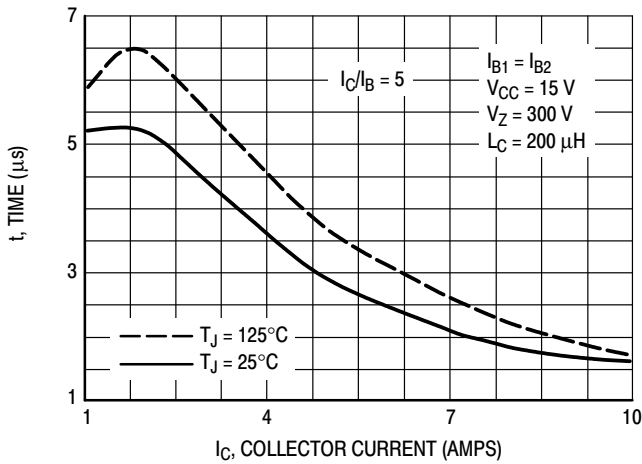


Figure 31. Inductive Storage Time,  $t_{si}$

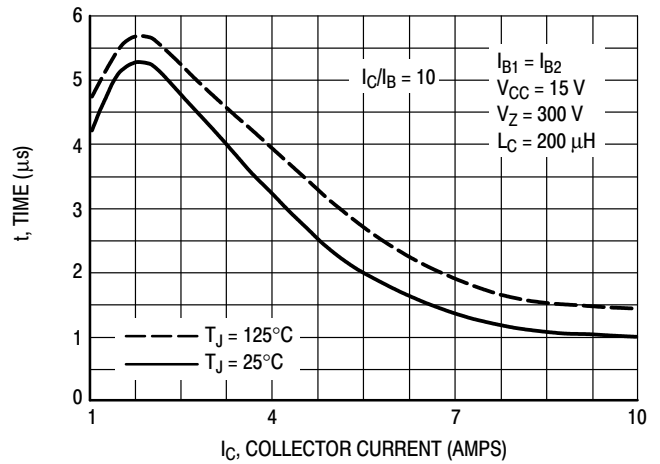


Figure 13 Bis. Inductive Storage Time,  $t_{si}$

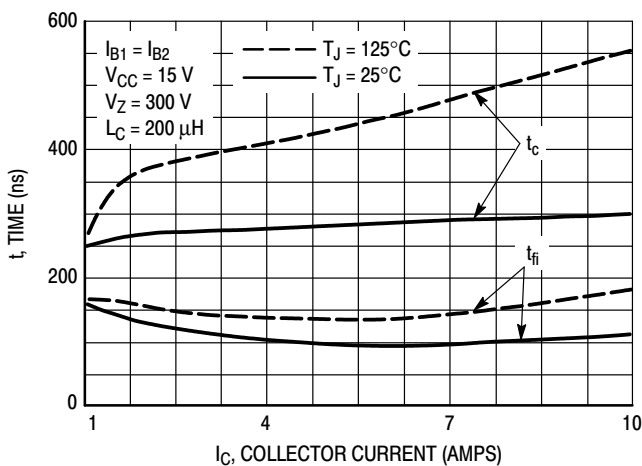


Figure 32. Inductive Storage Time,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 5$

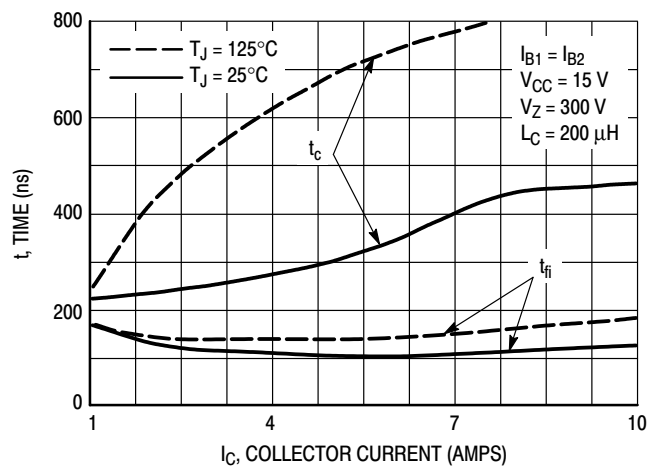


Figure 33. Inductive Storage Time,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 10$



TYPICAL SWITCHING CHARACTERISTICS

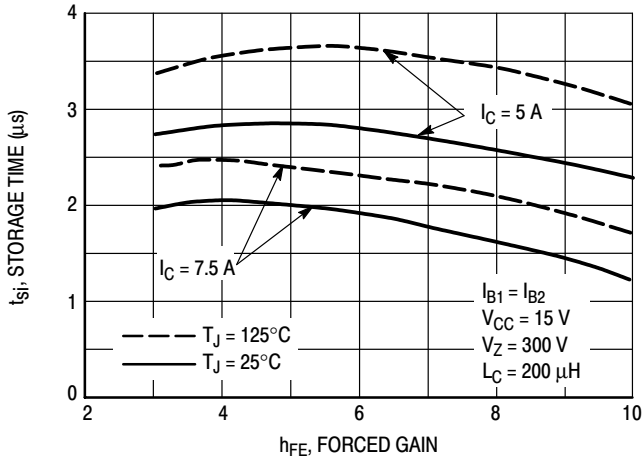


Figure 34. Inductive Storage Time

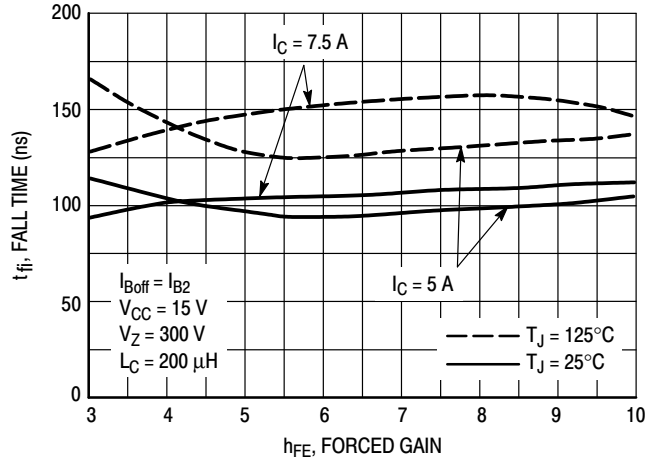


Figure 35. Inductive Fall Time

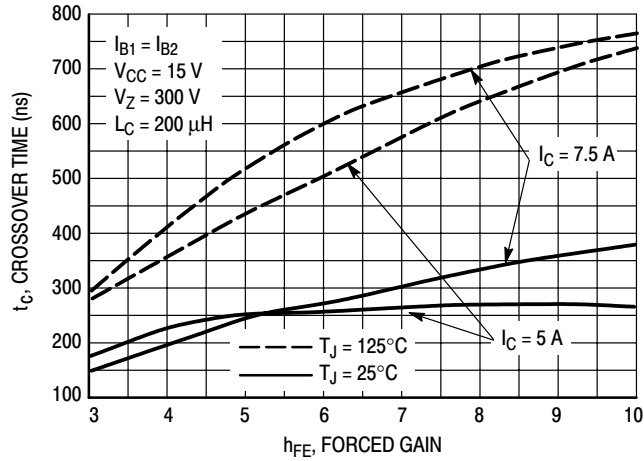


Figure 36. Inductive Crossover Time,  $t_c$

TYPICAL SWITCHING CHARACTERISTICS

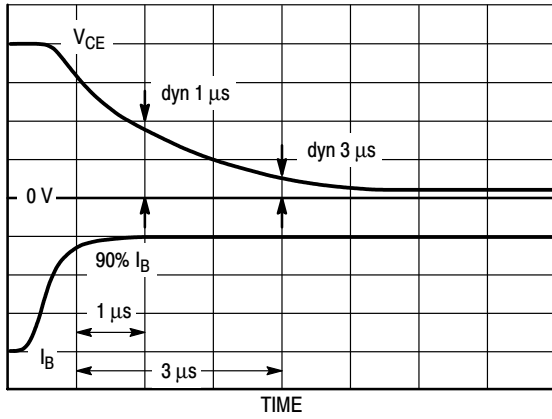


Figure 37. Dynamic Saturation Voltage Measurements

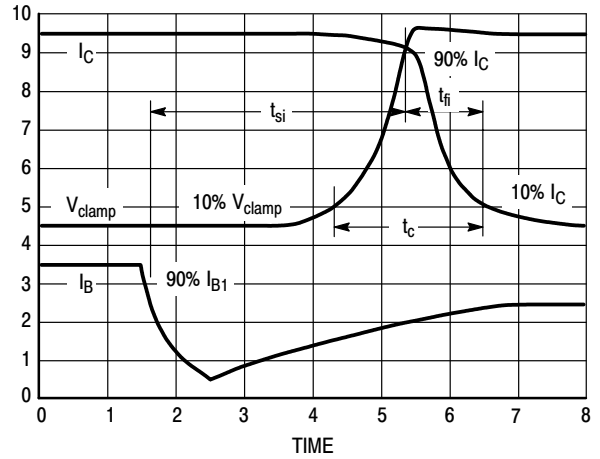
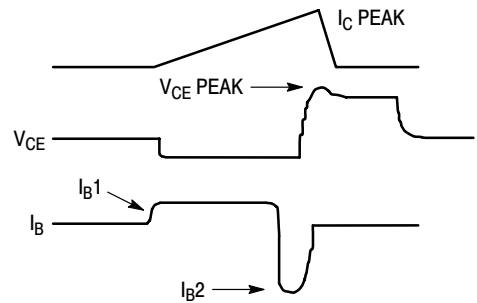
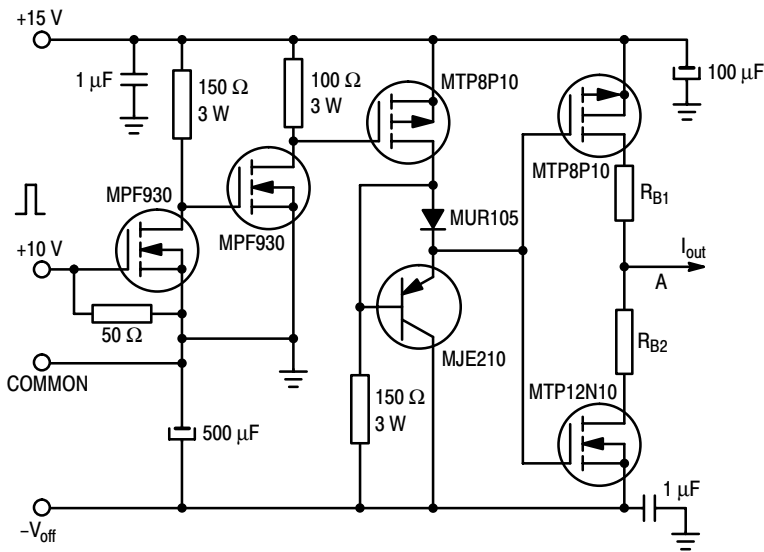


Figure 38. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit



$V_{(BR)CEO(sus)}$   
 $L = 10 \text{ mH}$   
 $R_{B2} = \infty$   
 $V_{CC} = 20 \text{ Volts}$   
 $I_{C(pk)} = 100 \text{ mA}$

**Inductive Switching**  
 $L = 200 \mu\text{H}$   
 $R_{B2} = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $R_{B1}$  selected for desired  $I_{B1}$

**RBSOA**  
 $L = 500 \mu\text{H}$   
 $R_{B2} = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $R_{B1}$  selected for desired  $I_{B1}$

TYPICAL THERMAL RESPONSE

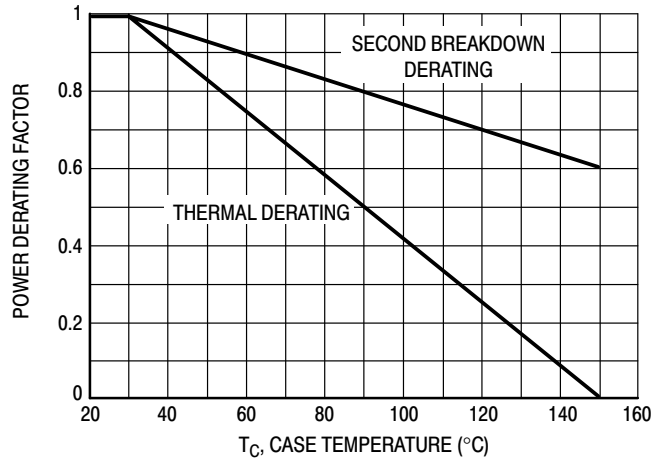


Figure 39. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 22 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 22 may be found at any case temperature by using the appropriate curve on Figure 21.

$T_{J(pk)}$  may be calculated from the data in Figure 24. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 23). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

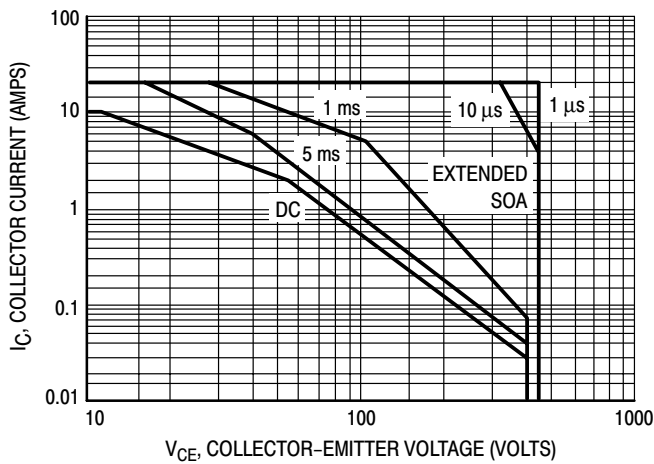


Figure 40. Forward Bias Safe Operating Area

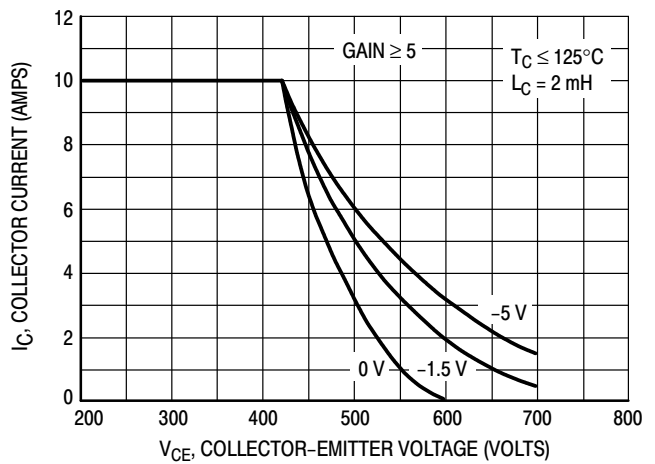


Figure 41. Reverse Bias Safe Operating Area

# BUH100

## TYPICAL THERMAL RESPONSE

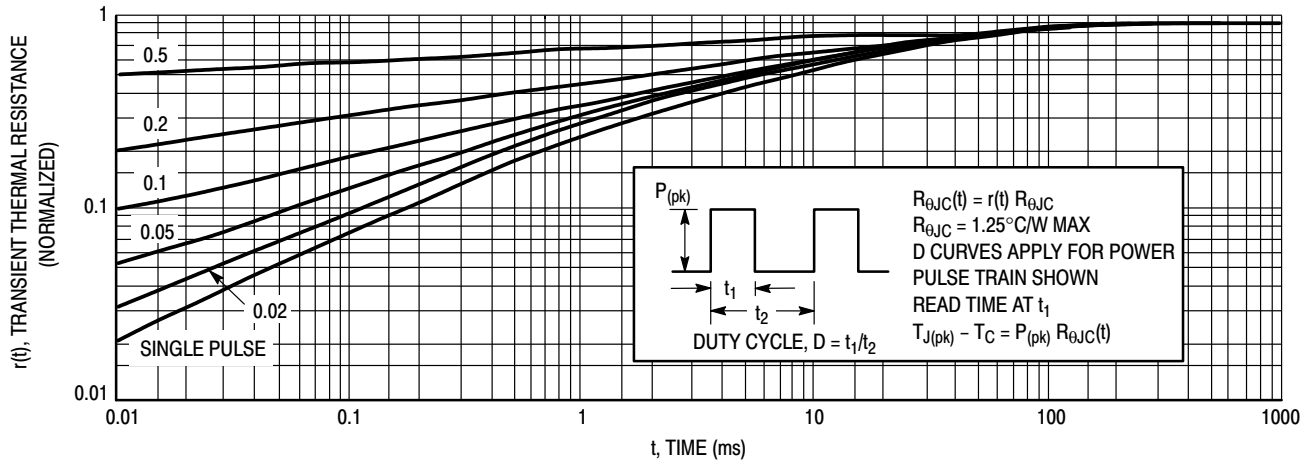


Figure 42. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for BUH100

## SWITCHMODE™ NPN Silicon Planar Power Transistor

The BUH150 has an application specific state-of-art die designed for use in 150 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the start-up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:  
High and Flat DC Current Gain  $h_{FE}$   
Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	400	Vdc
Collector-Base Breakdown Voltage	$V_{CBO}$	700	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	700	Vdc
Emitter-Base Voltage	$V_{EBO}$	10	Vdc
Collector Current — Continuous — Peak (1)	$I_C$ $I_{CM}$	15 25	Adc
Base Current — Continuous — Peak (1)	$I_B$ $I_{BM}$	6 12	Adc
*Total Device Dissipation @ $T_C = 25^\circ\text{C}$ *Derate above $25^\circ\text{C}$	$P_D$	150 1.2	Watt W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150	$^\circ\text{C}$

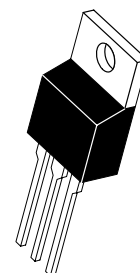
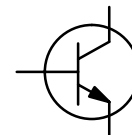
### THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.85 62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from case for 5 seconds	$T_L$	260	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq 10\%$ .

# BUH150

POWER TRANSISTOR  
15 AMPERES  
700 VOLTS  
150 WATTS



CASE 221A-09  
TO-220AB

# BUH150

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	400	460		Vdc
Collector–Base Breakdown Voltage ( $I_{CBO} = 1\text{ mA}$ )	$V_{CBO}$	700	860		Vdc
Emitter–Base Breakdown Voltage ( $I_{EBO} = 1\text{ mA}$ )	$V_{EBO}$	10	12.3		Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$			100	$\mu\text{A}$ dc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )	$I_{CES}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		100 1000	$\mu\text{A}$ dc
Collector Base Current ( $V_{CB} = \text{Rated } V_{CBO}$ , $V_{EB} = 0$ )	$I_{CBO}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		100 1000	$\mu\text{A}$ dc
Emitter–Cutoff Current ( $V_{EB} = 9\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$			100	$\mu\text{A}$ dc

### ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 10\text{ Adc}$ , $I_B = 2\text{ Adc}$ )	$V_{BE(sat)}$		1	1.25	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 2\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )	$V_{CE(sat)}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	0.16 0.15	0.4 0.4	Vdc
( $I_C = 10\text{ Adc}$ , $I_B = 2\text{ Adc}$ )		@ $T_C = 25^\circ\text{C}$	0.45	1	Vdc
( $I_C = 20\text{ Adc}$ , $I_B = 4\text{ Adc}$ )		@ $T_C = 25^\circ\text{C}$	2	5	Vdc
DC Current Gain ( $I_C = 20\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$h_{FE}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	4 2.5	7 4.5	—
( $I_C = 10\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	8 6	12 10	—
( $I_C = 2\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	12 14	20 22	—
( $I_C = 100\text{ mAdc}$ , $V_{CE} = 5\text{ Vdc}$ )		@ $T_C = 25^\circ\text{C}$	10	20	—

### DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 3 $\mu\text{s}$ after rising $I_{B1}$ reaches 90% of final $I_{B1}$ (see Figure 19)	$I_C = 5\text{ Adc}$ , $I_{B1} = 1\text{ Adc}$ $V_{CC} = 300\text{ V}$	@ $T_C = 25^\circ\text{C}$	$V_{CE(dsat)}$	1.5	V
		@ $T_C = 125^\circ\text{C}$		2.8	V
	$I_C = 10\text{ Adc}$ , $I_{B1} = 2\text{ Adc}$ $V_{CC} = 300\text{ V}$	@ $T_C = 25^\circ\text{C}$		2.4	V
		@ $T_C = 125^\circ\text{C}$		5	V

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$f_T$		23		MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1\text{ MHz}$ )	$C_{ob}$		100	150	pF
Input Capacitance ( $V_{EB} = 8\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$C_{ib}$		1300	1750	pF

# BUH150

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### SWITCHING CHARACTERISTICS: Resistive Load (D.C. $\leq 10\%$ , Pulse Width = 40 $\mu\text{s}$ )

Turn-on Time	$I_C = 2 \text{ Adc}$ , $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.2 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$		200	300	ns
Storage Time		@ $T_C = 25^\circ\text{C}$	$t_s$		5.3	6.5	$\mu\text{s}$
Fall Time		@ $T_C = 25^\circ\text{C}$	$t_f$		240	350	ns
Turn-off Time		@ $T_C = 25^\circ\text{C}$	$t_{off}$		5.6	7	$\mu\text{s}$
Turn-on Time	$I_C = 2 \text{ Adc}$ , $I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 0.4 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$		100	200	ns
Storage Time		@ $T_C = 25^\circ\text{C}$	$t_s$		6.1	7.5	$\mu\text{s}$
Fall Time		@ $T_C = 25^\circ\text{C}$	$t_f$		320	500	ns
Turn-off Time		@ $T_C = 25^\circ\text{C}$	$t_{off}$		6.5	8	$\mu\text{s}$
Turn-on Time	$I_C = 5 \text{ Adc}$ , $I_{B1} = 0.5 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$		450	650	ns
Turn-off Time		@ $T_C = 125^\circ\text{C}$	$t_{off}$		2.5	3	$\mu\text{s}$
		@ $T_C = 25^\circ\text{C}$			3.9		
Turn-on Time	$I_C = 10 \text{ Adc}$ , $I_{B1} = 2 \text{ Adc}$ $I_{B2} = 2 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$		500	700	ns
Turn-off Time		@ $T_C = 125^\circ\text{C}$	$t_{off}$		2.25	2.75	$\mu\text{s}$
		@ $T_C = 25^\circ\text{C}$			2.75		

### SWITCHING CHARACTERISTICS: Inductive Load ( $V_{clamp} = 300 \text{ V}$ , $V_{CC} = 15 \text{ V}$ , $L = 200 \mu\text{H}$ )

Fall Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_{fi}$		110	250	ns
		@ $T_C = 125^\circ\text{C}$				160	
Storage Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_{si}$		6.5	8	$\mu\text{s}$
		@ $T_C = 125^\circ\text{C}$				8	
Crossover Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_c$		235	350	ns
		@ $T_C = 125^\circ\text{C}$				240	
Fall Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 0.4 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_{fi}$		110	250	ns
		@ $T_C = 125^\circ\text{C}$				170	
Storage Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 0.4 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_{si}$		6	7.5	$\mu\text{s}$
		@ $T_C = 125^\circ\text{C}$				7.8	
Crossover Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 0.4 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_c$		250	350	ns
		@ $T_C = 125^\circ\text{C}$				270	
Fall Time	$I_C = 5 \text{ Adc}$ $I_{B1} = 0.5 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_{fi}$		110	150	ns
		@ $T_C = 125^\circ\text{C}$				140	
Storage Time	$I_C = 5 \text{ Adc}$ $I_{B1} = 0.5 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_{si}$		3.25	3.75	$\mu\text{s}$
		@ $T_C = 125^\circ\text{C}$				4.6	
Crossover Time	$I_C = 5 \text{ Adc}$ $I_{B1} = 0.5 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_c$		275	350	ns
		@ $T_C = 125^\circ\text{C}$				450	
Fall Time	$I_C = 10 \text{ Adc}$ $I_{B1} = 2 \text{ Adc}$ $I_{B2} = 2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_{fi}$		110	175	ns
		@ $T_C = 125^\circ\text{C}$				160	
Storage Time	$I_C = 10 \text{ Adc}$ $I_{B1} = 2 \text{ Adc}$ $I_{B2} = 2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_{si}$		2.3	2.75	$\mu\text{s}$
		@ $T_C = 125^\circ\text{C}$				2.8	
Crossover Time	$I_C = 10 \text{ Adc}$ $I_{B1} = 2 \text{ Adc}$ $I_{B2} = 2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_c$		250	350	ns
		@ $T_C = 125^\circ\text{C}$				475	

TYPICAL STATIC CHARACTERISTICS

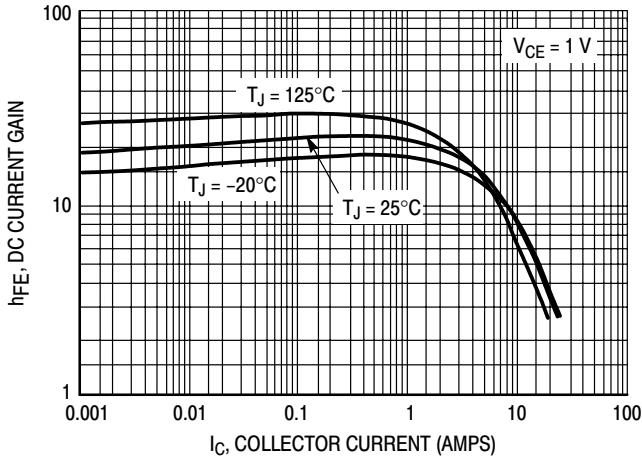


Figure 43. DC Current Gain @ 1 Volt

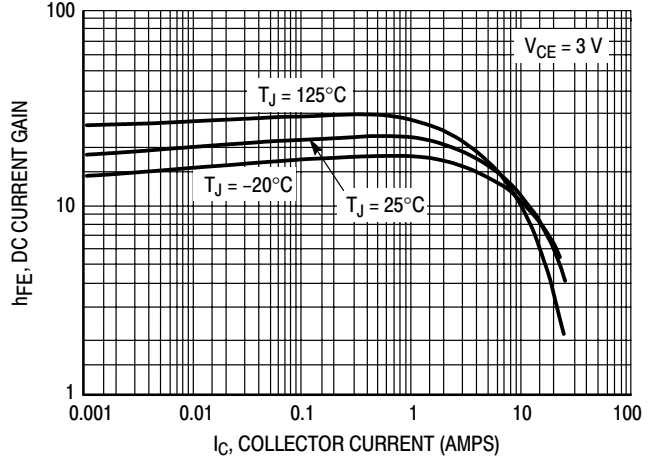


Figure 44. DC Current Gain @ 3 Volt

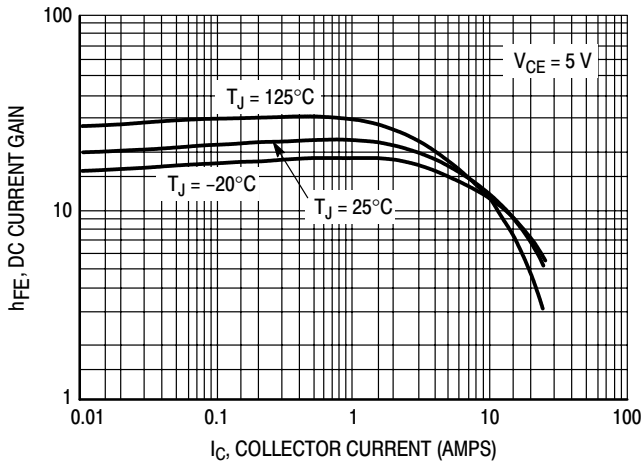


Figure 45. DC Current Gain @ 5 Volt

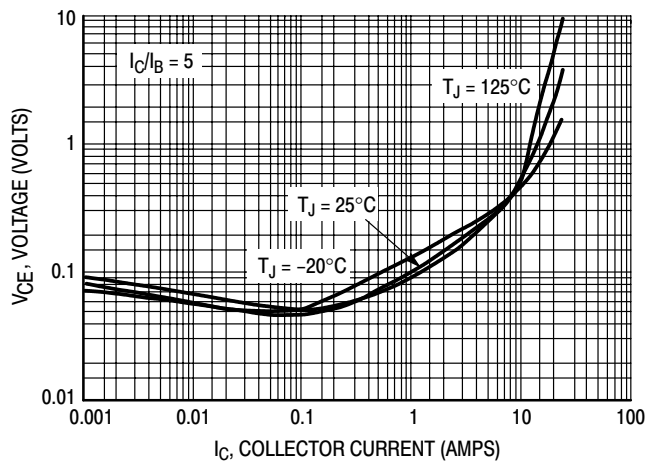


Figure 46. Collector-Emitter Saturation Voltage

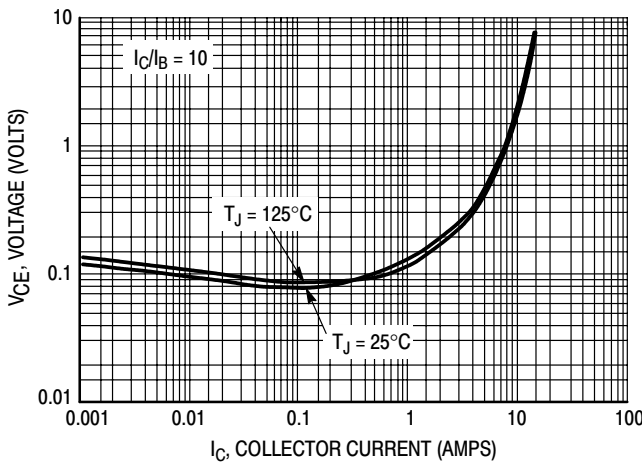


Figure 47. Collector-Emitter Saturation Voltage

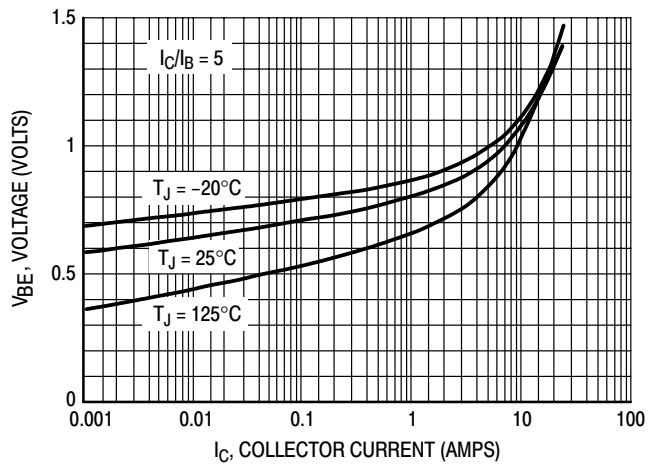


Figure 48. Base-Emitter Saturation Region



TYPICAL STATIC CHARACTERISTICS

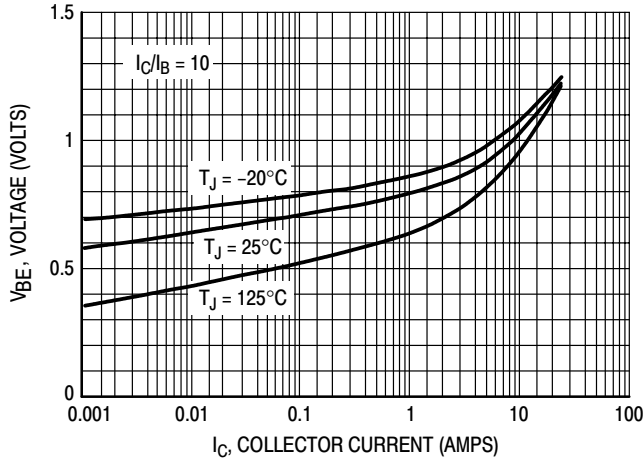


Figure 49. Base-Emitter Saturation Region

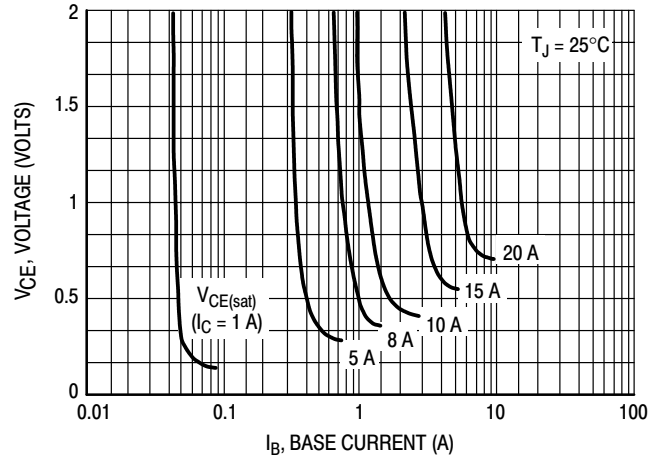


Figure 50. Collector Saturation Region

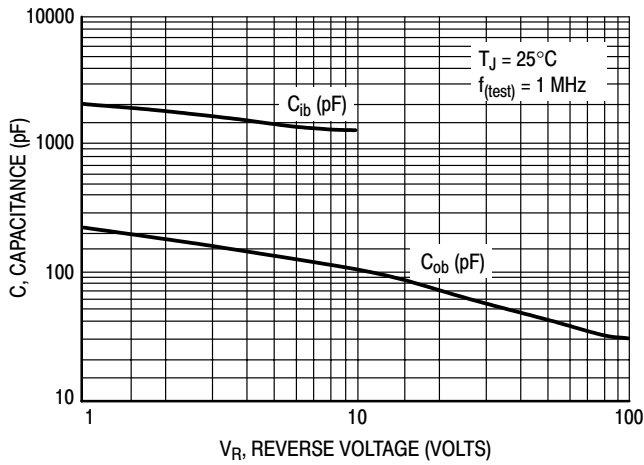


Figure 51. Capacitance

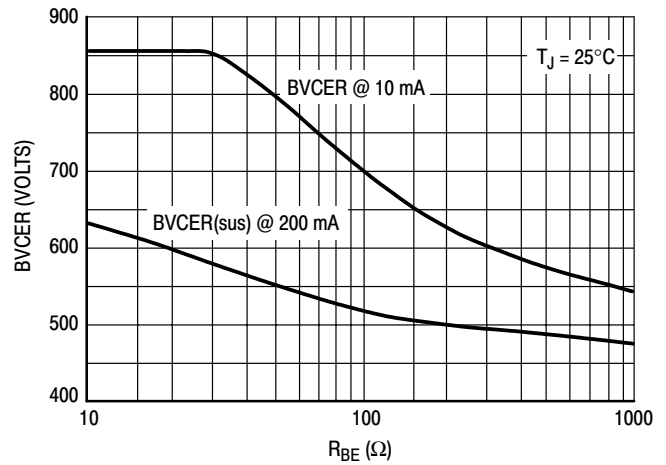


Figure 52. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

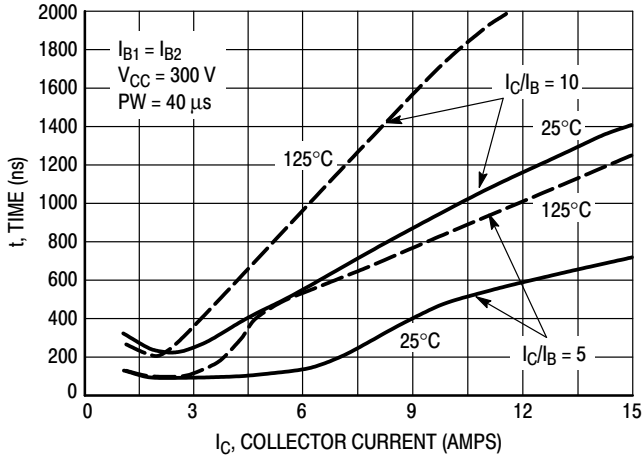


Figure 53. Resistive Switching,  $t_{on}$

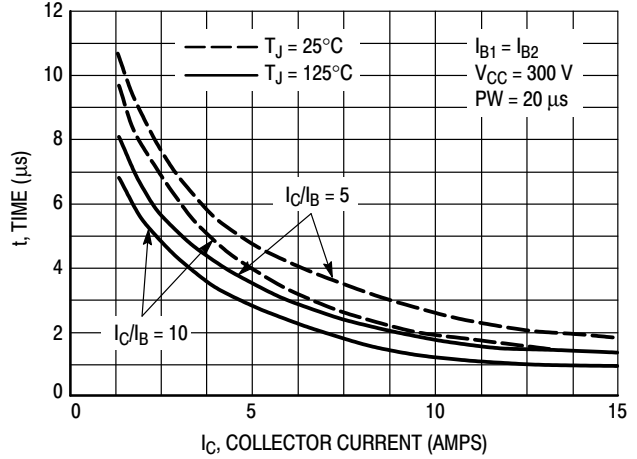


Figure 54. Resistive Switch Time,  $t_{off}$

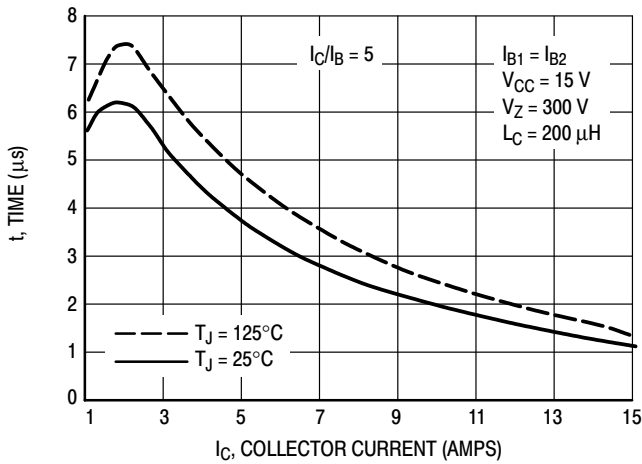


Figure 55. Inductive Storage Time,  $t_{si}$

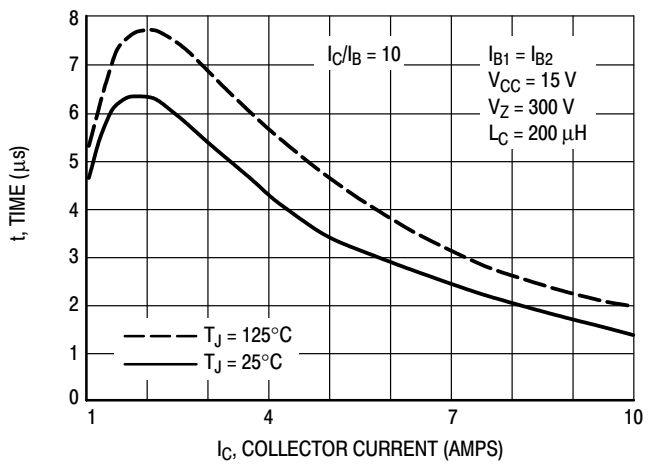


Figure 13 Bis. Inductive Storage Time,  $t_{si}$

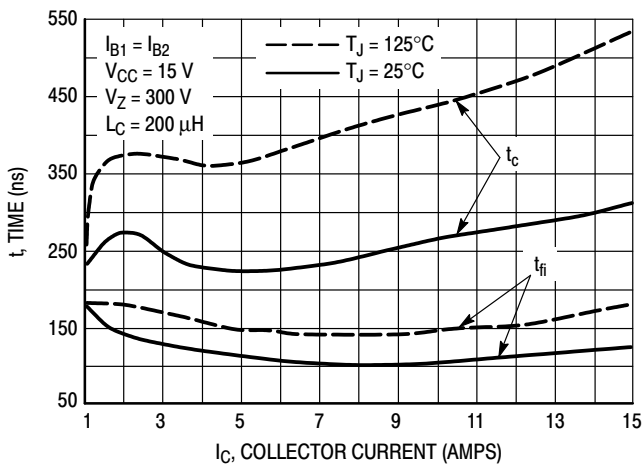


Figure 56. Inductive Storage Time,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 5$

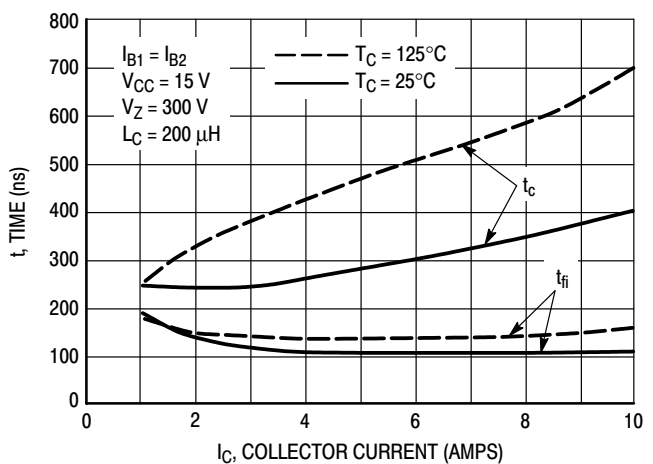


Figure 57. Inductive Storage Time,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS

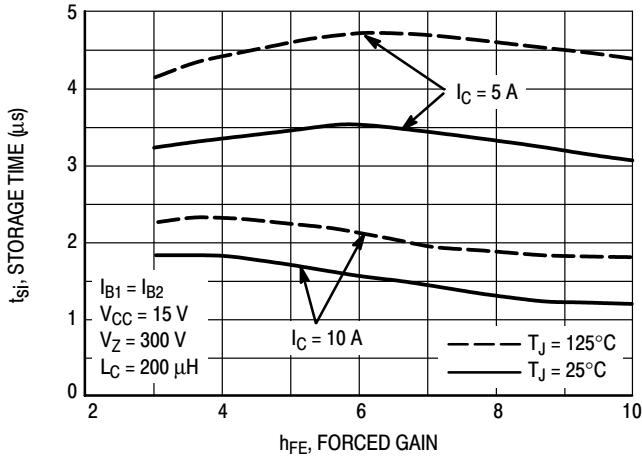


Figure 58. Inductive Storage Time

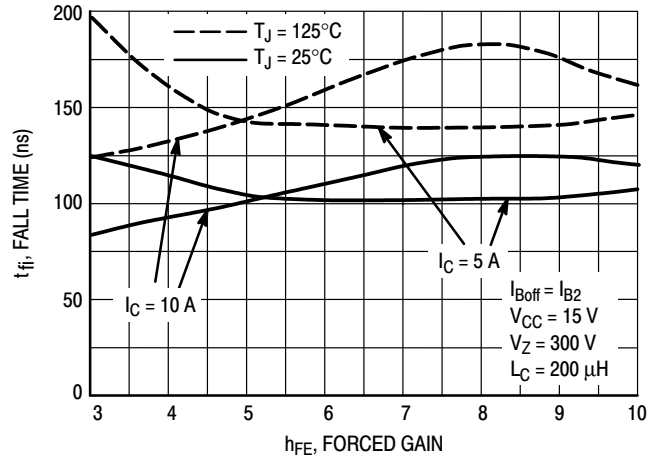


Figure 59. Inductive Fall Time

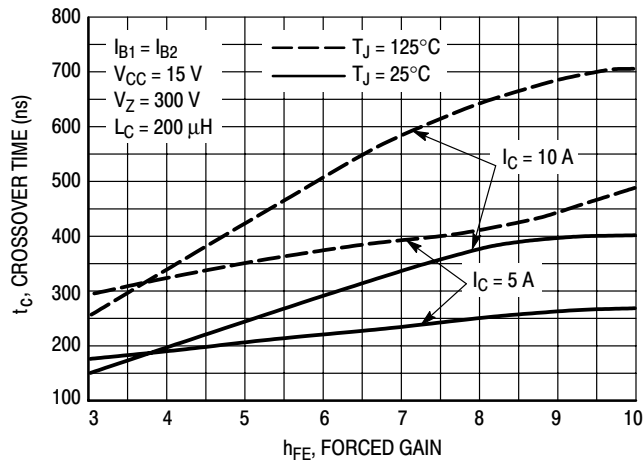


Figure 60. Inductive Crossover Time

TYPICAL SWITCHING CHARACTERISTICS

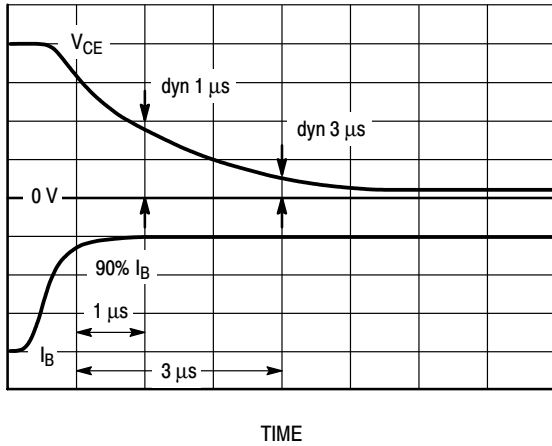


Figure 61. Dynamic Saturation Voltage Measurements

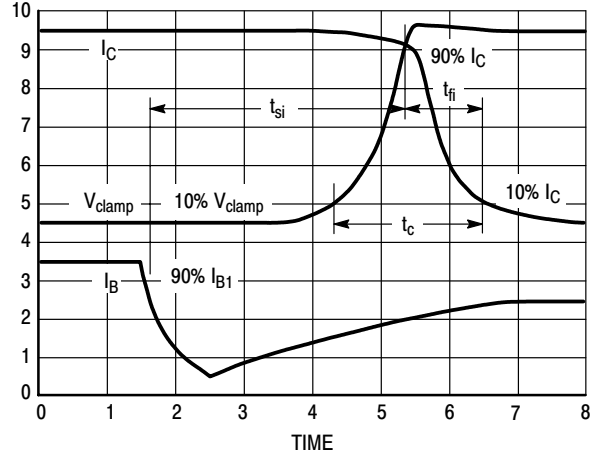
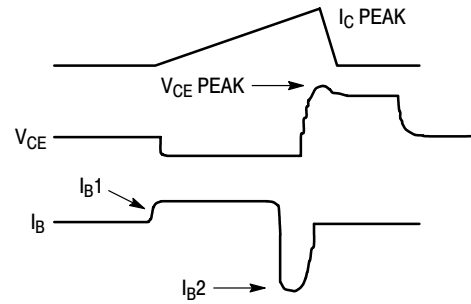
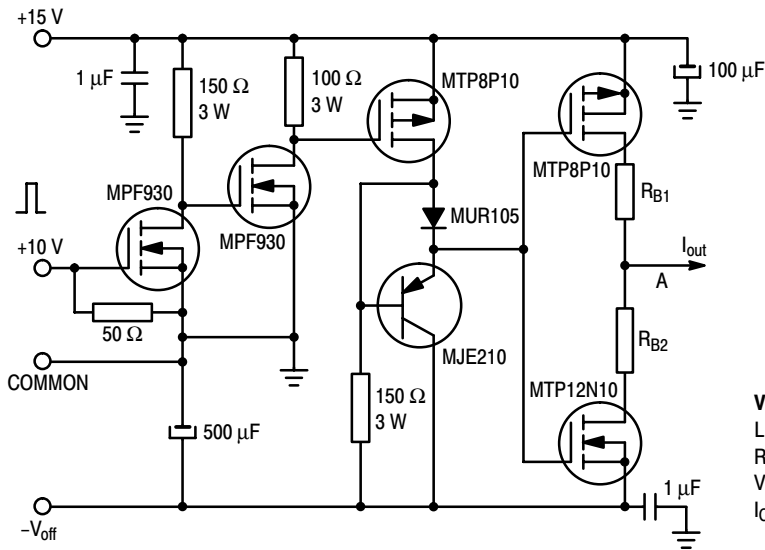


Figure 62. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit



$V_{(BR)CEO(sus)}$   
 $L = 10 \text{ mH}$   
 $R_{B2} = \infty$   
 $V_{CC} = 20 \text{ Volts}$   
 $I_{C(pk)} = 100 \text{ mA}$

**Inductive Switching**  
 $L = 200 \mu\text{H}$   
 $R_{B2} = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $R_{B1}$  selected for desired  $I_{B1}$

**RBSOA**  
 $L = 500 \mu\text{H}$   
 $R_{B2} = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $R_{B1}$  selected for desired  $I_{B1}$

TYPICAL THERMAL RESPONSE

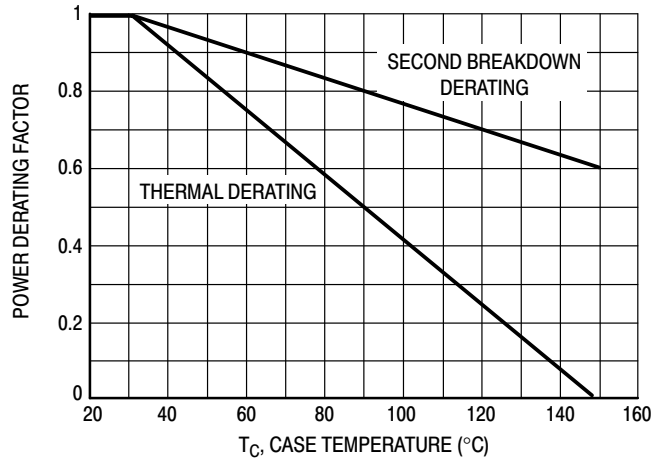


Figure 63. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 64 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 64 may be found at any case temperature by using the appropriate curve on Figure 63.

$T_{J(pk)}$  may be calculated from the data in Figure 66. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 65). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

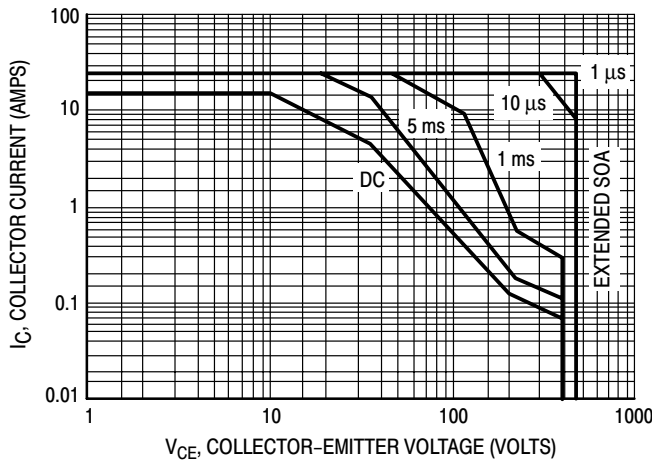


Figure 64. Forward Bias Safe Operating Area

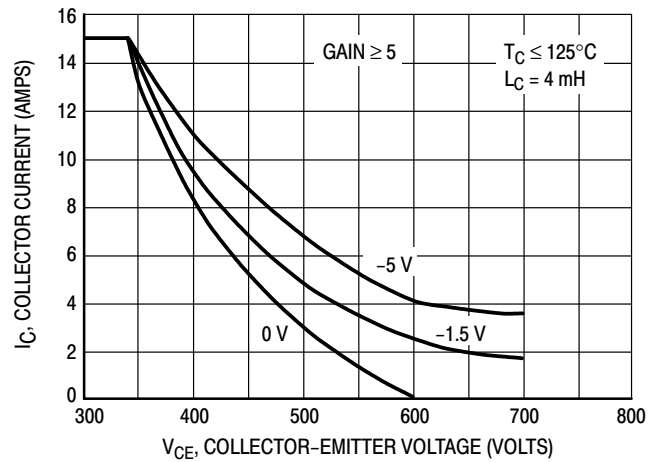


Figure 65. Reverse Bias Safe Operating Area

# BUH150

## TYPICAL THERMAL RESPONSE

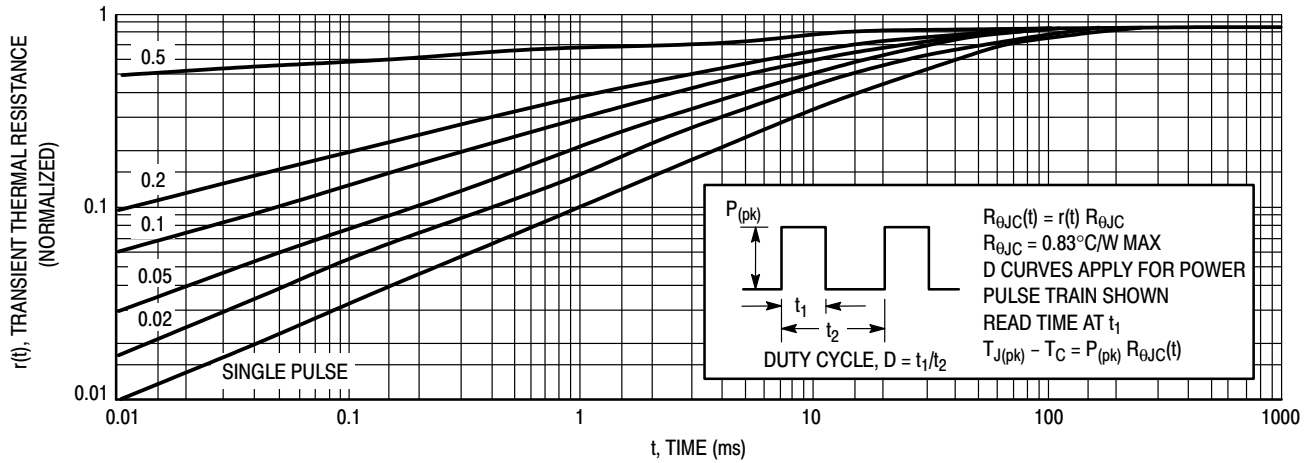


Figure 66. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for BUH150

## SWITCHMODE™ NPN Silicon Planar Power Transistor

The BUH50 has an application specific state-of-art die designed for use in 50 Watts HALOGEN electronic transformers and SWITCHMODE applications.

This high voltage/high speed transistor exhibits the following main feature:

- Improved Efficiency Due to Low Base Drive Requirements:  
High and Flat DC Current Gain  $h_{FE}$   
Fast Switching
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions
- Specified Dynamic Saturation Data
- Full Characterization at 125°C

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	$V_{CEO}$	500	Vdc
Collector–Base Breakdown Voltage	$V_{CBO}$	800	Vdc
Collector–Emitter Breakdown Voltage	$V_{CES}$	800	Vdc
Emitter–Base Voltage	$V_{EBO}$	9	Vdc
Collector Current — Continuous — Peak (1)	$I_C$ $I_{CM}$	4 8	Adc
Base Current — Continuous — Peak (1)	$I_B$ $I_{BM}$	2 4	Adc
*Total Device Dissipation @ $T_C = 25^\circ\text{C}$ *Derate above 25°C	$P_D$	50 0.4	Watt W/°C
Operating and Storage Temperature	$T_J, T_{stg}$	–65 to 150	°C

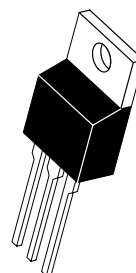
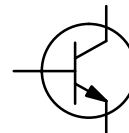
### THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from case for 5 seconds	$T_L$	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

# BUH50

POWER TRANSISTOR  
4 AMPERES  
800 VOLTS  
50 WATTS



CASE 221A-09  
TO-220AB

# BUH50

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	500			Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$			100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )	$I_{CES}$			100 1000	$\mu\text{Adc}$
Emitter–Cutoff Current ( $V_{EB} = 9\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$			100	$\mu\text{Adc}$

### ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 1\text{ Adc}$ , $I_B = 0.33\text{ Adc}$ ) ( $I_C = 2\text{ Adc}$ , $I_B = 0.66\text{ Adc}$ ) $25^\circ\text{C}$ ( $I_C = 2\text{ Adc}$ , $I_B = 0.66\text{ Adc}$ ) $100^\circ\text{C}$	$V_{BE(sat)}$		0.86 0.94 0.85	1.2 1.6 1.5	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 1\text{ Adc}$ , $I_B = 0.33\text{ Adc}$ )  ( $I_C = 2\text{ Adc}$ , $I_B = 0.66\text{ Adc}$ )  ( $I_C = 3\text{ Adc}$ , $I_B = 1\text{ Adc}$ )	$V_{CE(sat)}$	@ $T_C = 25^\circ\text{C}$  @ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$  @ $T_C = 25^\circ\text{C}$	0.2  0.32 0.29  0.5	0.5  0.6 0.7  1	Vdc
DC Current Gain ( $I_C = 1\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )  ( $I_C = 2\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$h_{FE}$	@ $T_C = 25^\circ\text{C}$  @ $T_C = 25^\circ\text{C}$	7  5	13  10	—  —

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$f_T$	4			MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1\text{ MHz}$ )	$C_{ob}$		50	100	pF
Input Capacitance ( $V_{EB} = 8\text{ Vdc}$ )	$C_{ib}$		850	1200	pF

### DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined $1\text{ }\mu\text{s}$ and $3\text{ }\mu\text{s}$ respectively after rising $I_{B1}$ reaches 90% of final $I_{B1}$	$I_C = 1\text{ A}$ $I_{B1} = 0.33\text{ A}$ $V_{CC} = 300\text{ V}$	@ $1\text{ }\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(dsat)}$	1.75 5		V
		@ $3\text{ }\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		0.3 0.5		V
	$I_C = 2\text{ A}$ $I_{B1} = 0.66\text{ A}$ $V_{CC} = 300\text{ V}$	@ $1\text{ }\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(dsat)}$	6 14		V
		@ $3\text{ }\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		0.75 4		V



# BUH50

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### SWITCHING CHARACTERISTICS: Resistive Load ( $D.C. \leq 10\%$ , Pulse Width = 20 $\mu\text{s}$ )

Turn-on Time	$I_C = 2 \text{ Adc}$ , $I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 0.4 \text{ Adc}$ $V_{CC} = 125 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$	95	250	ns
Turn-off Time		@ $T_C = 25^\circ\text{C}$	$t_{off}$	2.5	3.5	$\mu\text{s}$
Turn-on Time	$I_C = 2 \text{ Adc}$ , $I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 1 \text{ Adc}$ $V_{CC} = 125 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$	110	250	ns
Turn-off Time		@ $T_C = 25^\circ\text{C}$	$t_{off}$	0.95	2	$\mu\text{s}$
Turn-on Time	$I_C = 1 \text{ Adc}$ , $I_{B1} = 0.3 \text{ Adc}$ $I_{B2} = 0.3 \text{ Adc}$ $V_{CC} = 125 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$	100	200	ns
Turn-off Time		@ $T_C = 25^\circ\text{C}$	$t_{off}$	2.9	3.5	$\mu\text{s}$

### SWITCHING CHARACTERISTICS: Inductive Load ( $V_{clamp} = 300 \text{ V}$ , $V_{CC} = 15 \text{ V}$ , $L = 200 \mu\text{H}$ )

Fall Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 1 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_f$	80	150	ns
		@ $T_C = 125^\circ\text{C}$		95		
Storage Time		@ $T_C = 25^\circ\text{C}$	$t_s$	1.2	2.5	$\mu\text{s}$
	@ $T_C = 125^\circ\text{C}$	$t_s$	1.7			
Crossover Time		@ $T_C = 25^\circ\text{C}$	$t_c$	150	300	ns
	@ $T_C = 125^\circ\text{C}$	$t_c$		180		
Fall Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 0.66 \text{ Adc}$ $I_{B2} = 1 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_f$	90	150	ns
		@ $T_C = 125^\circ\text{C}$		$t_f$		
Storage Time		@ $T_C = 25^\circ\text{C}$	$t_s$	1.7	2.75	$\mu\text{s}$
	@ $T_C = 125^\circ\text{C}$	$t_s$	2.5			
Crossover Time		@ $T_C = 25^\circ\text{C}$	$t_c$	190	350	ns
	@ $T_C = 125^\circ\text{C}$	$t_c$		220		

## TYPICAL STATIC CHARACTERISTICS

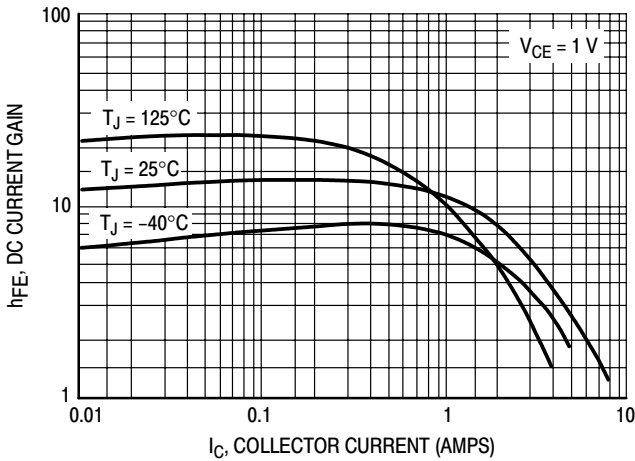


Figure 67. DC Current Gain @ 1 Volt

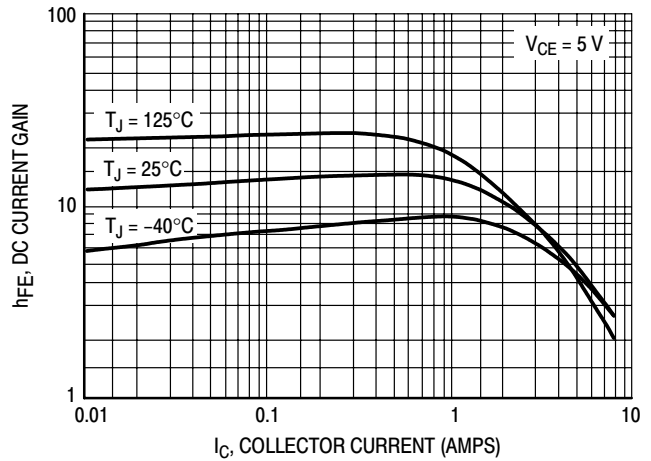


Figure 68. DC Current Gain @ 5 Volt

TYPICAL STATIC CHARACTERISTICS

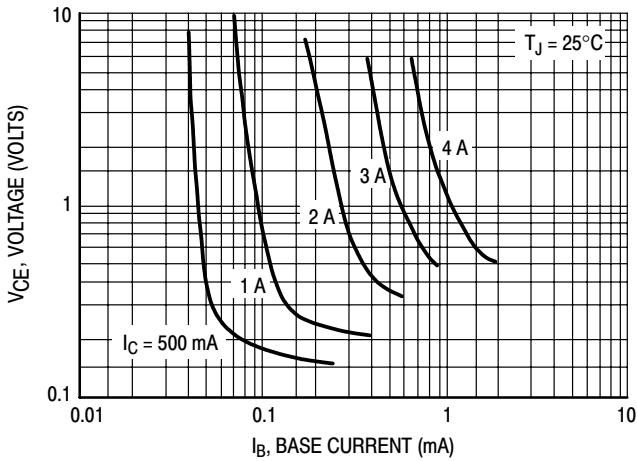


Figure 69. Collector Saturation Region

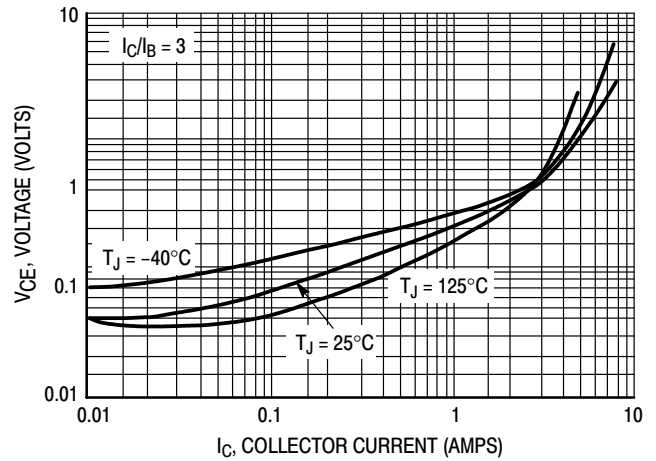


Figure 70. Collector-Emitter Saturation Voltage

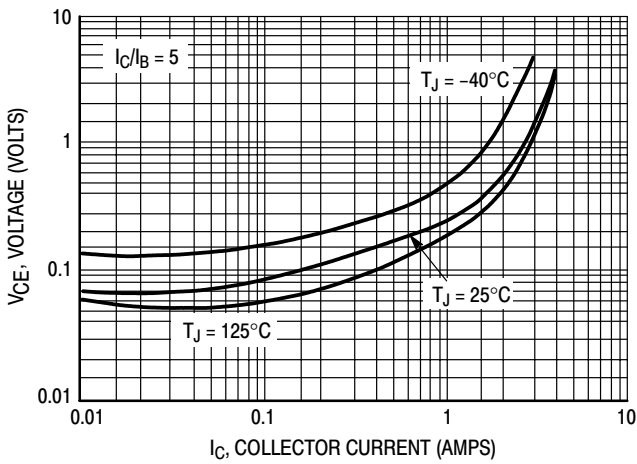


Figure 71. Collector-Emitter Saturation Voltage

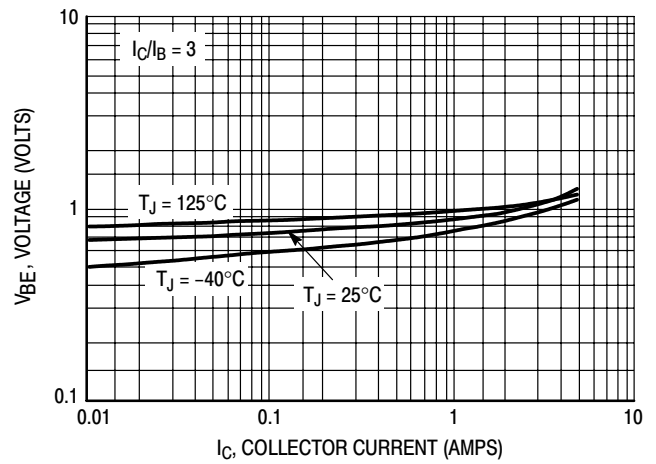


Figure 72. Base-Emitter Saturation Region

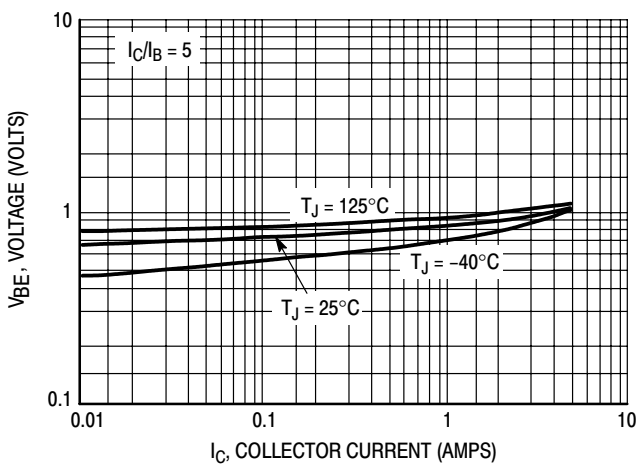


Figure 73. Base-Emitter Saturation Region

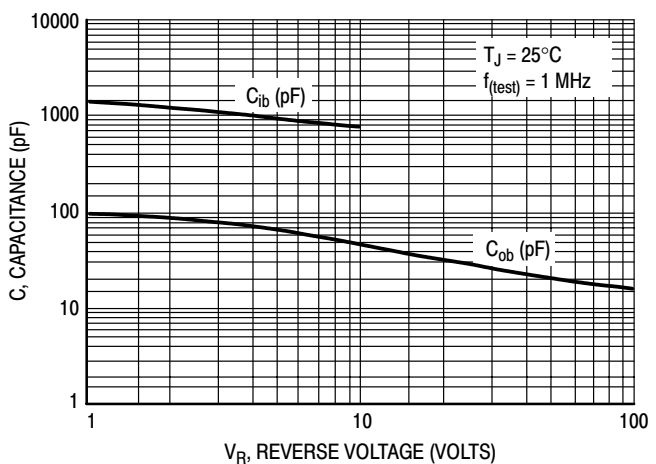


Figure 74. Capacitance

TYPICAL SWITCHING CHARACTERISTICS

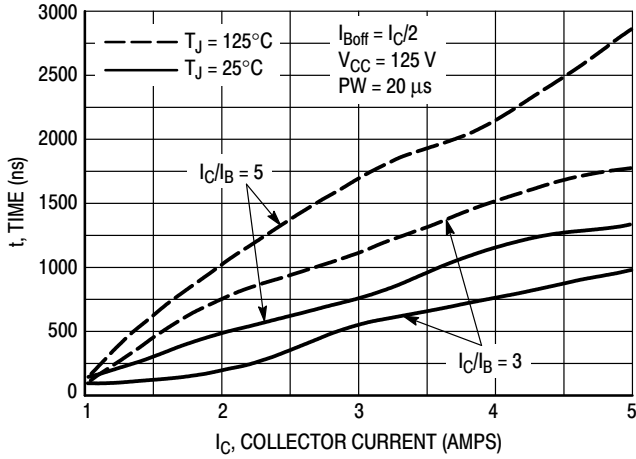


Figure 75. Resistive Switching,  $t_{on}$

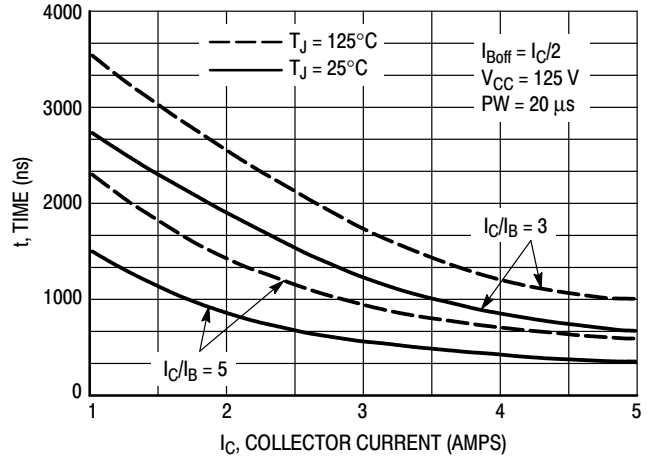


Figure 76. Resistive Switch Time,  $t_{off}$

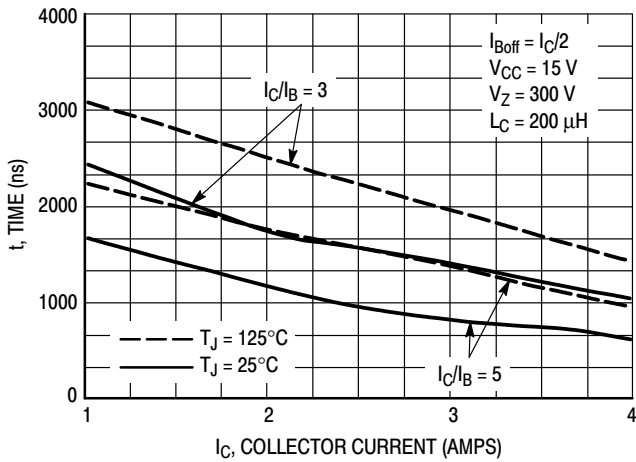


Figure 77. Inductive Storage Time,  $t_{si}$

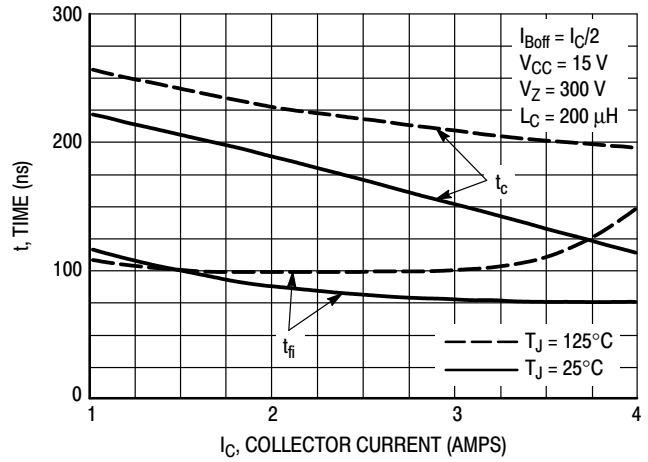


Figure 78. Inductive Storage Time,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 3$

TYPICAL CHARACTERISTICS

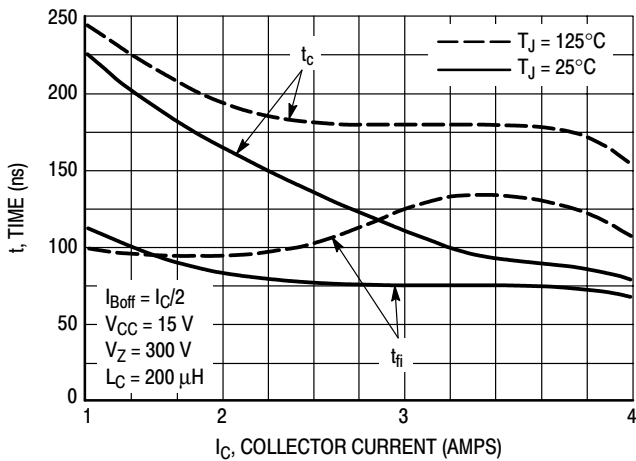


Figure 79. Inductive Switching,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 5$

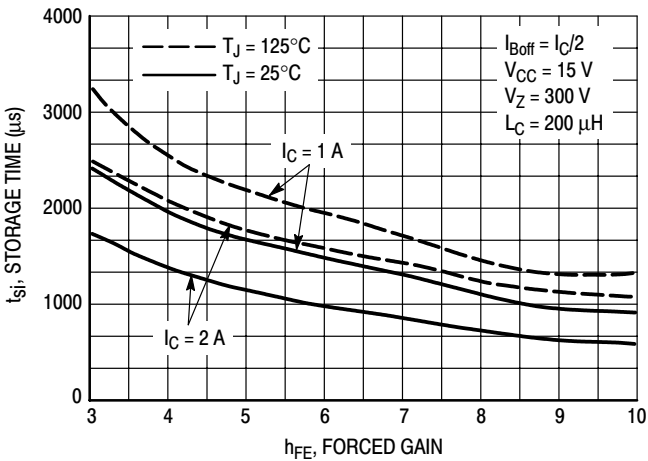


Figure 80. Inductive Storage Time

# BUH50

## TYPICAL CHARACTERISTICS

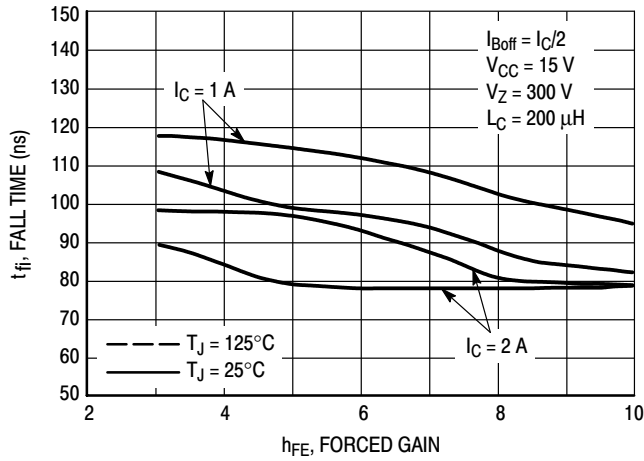


Figure 81. Inductive Fall Time

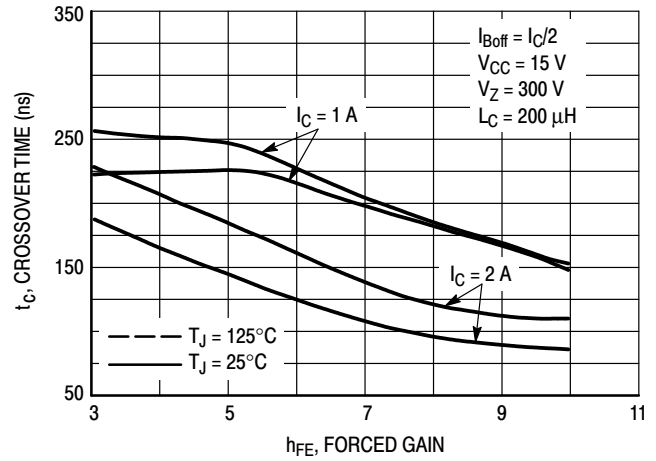


Figure 82. Inductive Crossover Time

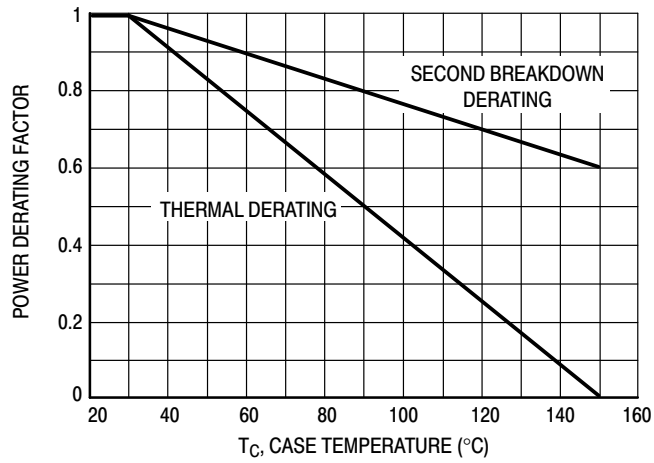


Figure 83. Forward Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 86 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 86 may be found at any case temperature by using the appropriate curve on Figure 83.

$T_{J(pk)}$  may be calculated from the data in Figure 88. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 87). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL CHARACTERISTICS

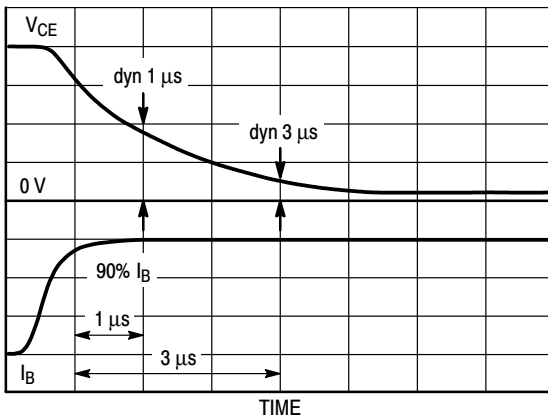


Figure 84. Dynamic Saturation Voltage

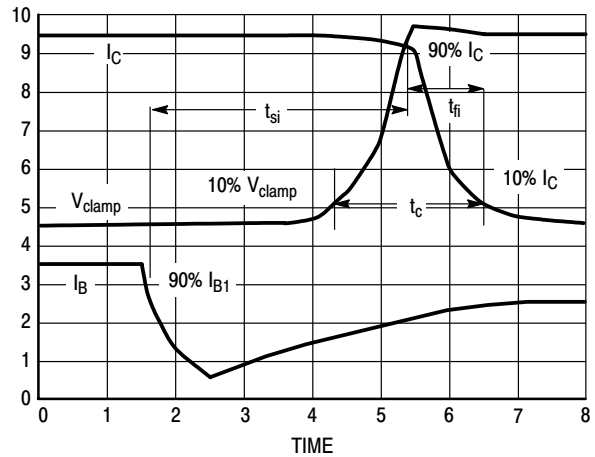


Figure 85. Inductive Switching Measurements

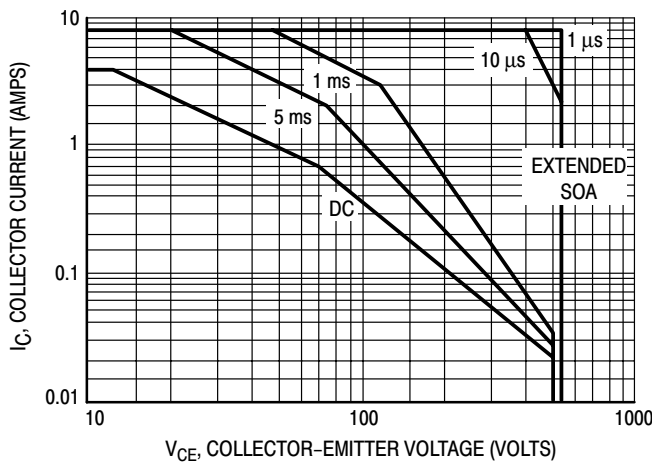


Figure 86. Forward Bias Safe Operating Area

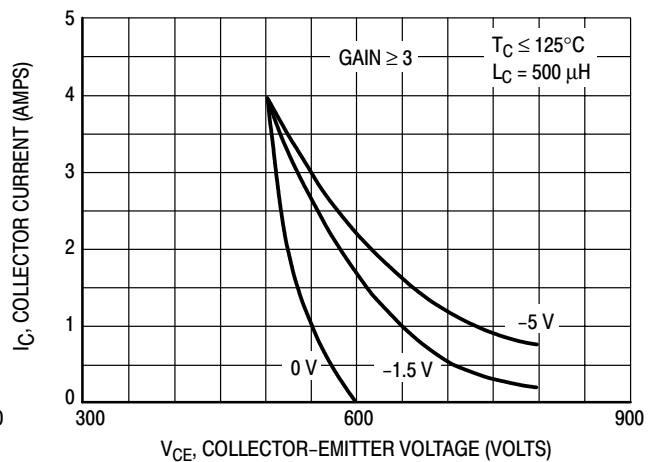
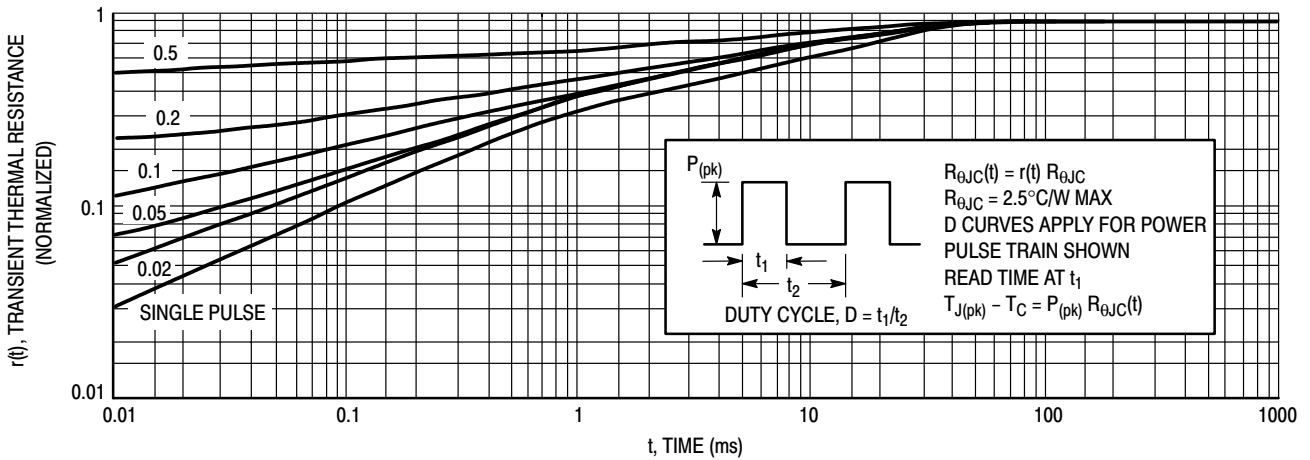
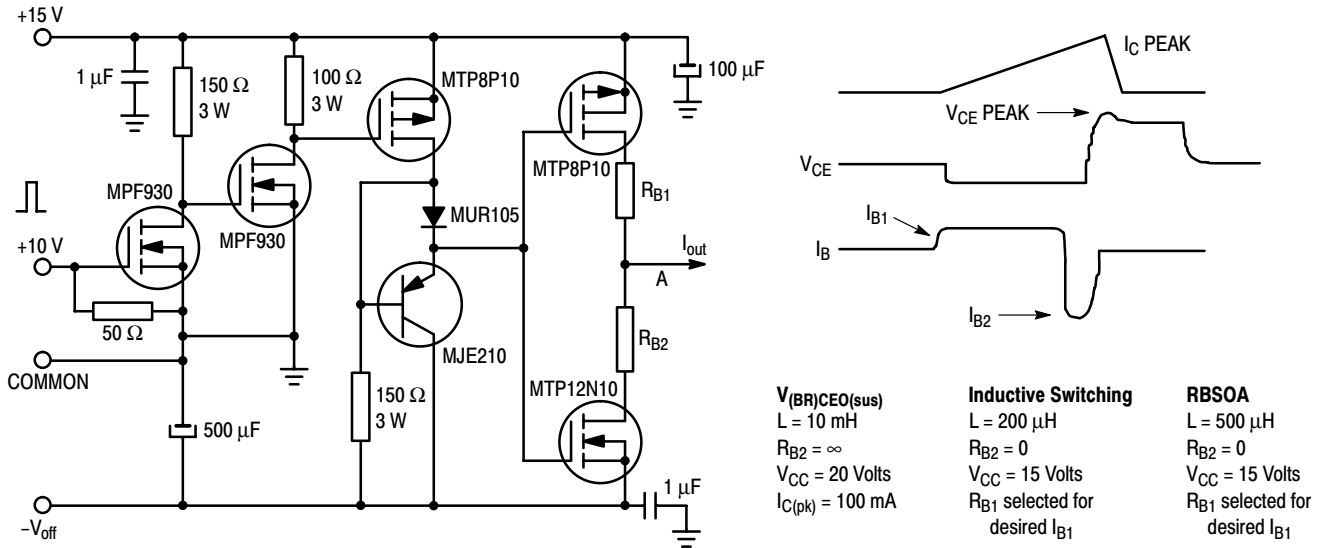


Figure 87. Reverse Bias Safe Operating Area

# BUH50

## TYPICAL CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



## SWITCHMODE™ NPN Silicon Planar Power Transistor

The BUH51 has an application specific state-of-art die designed for use in 50 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the start-up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:  
High and Flat DC Current Gain  $h_{FE}$   
Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- ON Semiconductor Six Sigma Philosophy Providing Tight and Reproducible Parametric Distributions

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	500	Vdc
Collector-Base Breakdown Voltage	$V_{CBO}$	800	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	800	Vdc
Emitter-Base Voltage	$V_{EBO}$	10	Vdc
Collector Current — Continuous — Peak (1)	$I_C$ $I_{CM}$	3 8	Adc
Base Current — Continuous — Peak (1)	$I_B$ $I_{BM}$	2 4	Adc
*Total Device Dissipation @ $T_C = 25^\circ\text{C}$ *Derate above $25^\circ\text{C}$	$P_D$	50 0.4	Watt W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150	$^\circ\text{C}$

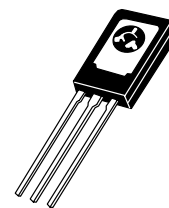
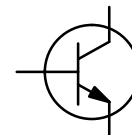
### THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 100	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from case for 5 seconds	$T_L$	260	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq 10\%$ .

## BUH51

POWER TRANSISTOR  
3 AMPERES  
800 VOLTS  
50 WATTS



CASE 77-09  
TO-225AA TYPE

# BUH51

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	500	550		Vdc
Collector–Base Breakdown Voltage ( $I_{CBO} = 1\text{ mA}$ )	$V_{CBO}$	800	950		Vdc
Emitter–Base Breakdown Voltage ( $I_{EBO} = 1\text{ mA}$ )	$V_{EBO}$	10	12.5		Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$			100	$\mu\text{A}$ dc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ $I_{CES}$			100 1000	$\mu\text{A}$ dc
Collector Base Current ( $V_{CB} = \text{Rated } V_{CBO}$ , $V_{EB} = 0$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ $I_{CBO}$			100 1000	$\mu\text{A}$ dc
Emitter–Cutoff Current ( $V_{EB} = 9\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$			100	$\mu\text{A}$ dc

### ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 1\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{BE(sat)}$		0.92 0.8	1.1	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 1\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(sat)}$		0.3 0.32	0.5 0.6	Vdc
DC Current Gain ( $I_C = 1\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$h_{FE}$	8 6	10 8		—
( $I_C = 2\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		5 4	7.5 6.2		—
( $I_C = 0.8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		10 8	14 13		—
( $I_C = 10\text{ mA}$ dc, $V_{CE} = 5\text{ Vdc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		14 18	20 25		—

### DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 3 $\mu\text{s}$ after rising $I_{B1}$ reaches 90% of final $I_{B1}$	$I_C = 1\text{ Adc}$ , $I_{B1} = 0.2\text{ Adc}$ $V_{CC} = 300\text{ V}$	@ $T_C = 25^\circ\text{C}$	$V_{CE(dsat)}$		1.7	V
		@ $T_C = 125^\circ\text{C}$			6	V
	$I_C = 2\text{ Adc}$ , $I_{B1} = 0.4\text{ Adc}$ $V_{CC} = 300\text{ V}$	@ $T_C = 25^\circ\text{C}$			5.1	V
		@ $T_C = 125^\circ\text{C}$			15	V

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$f_T$		23		MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1\text{ MHz}$ )	$C_{ob}$		34	100	pF
Input Capacitance ( $V_{EB} = 8\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$C_{ib}$		200	500	pF



# BUH51

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### SWITCHING CHARACTERISTICS: Resistive Load ( $D.C. \leq 10\%$ , Pulse Width = 40 $\mu\text{s}$ )

Turn-on Time	$I_C = 1 \text{ Adc}, I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.2 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$	110	150	ns
Turn-off Time		@ $T_C = 125^\circ\text{C}$		125		
Turn-on Time	$I_C = 2 \text{ Adc}, I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 0.4 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$	700	1000	ns
Turn-off Time		@ $T_C = 125^\circ\text{C}$		1250		
		@ $T_C = 25^\circ\text{C}$	$t_{off}$	3.5	4	$\mu\text{s}$
		@ $T_C = 125^\circ\text{C}$		4.1		
		@ $T_C = 25^\circ\text{C}$	$t_{on}$	1.75	2	$\mu\text{s}$
		@ $T_C = 125^\circ\text{C}$		2.1		

### SWITCHING CHARACTERISTICS: Inductive Load ( $V_{clamp} = 300 \text{ V}, V_{CC} = 15 \text{ V}, L = 200 \mu\text{H}$ )

Fall Time	$I_C = 1 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_{fi}$	200	300	ns
Storage Time		@ $T_C = 125^\circ\text{C}$		320		
		@ $T_C = 25^\circ\text{C}$	$t_{si}$	3.4	3.75	$\mu\text{s}$
		@ $T_C = 125^\circ\text{C}$		4		
Crossover Time		@ $T_C = 25^\circ\text{C}$	$t_c$	350	500	ns
		@ $T_C = 125^\circ\text{C}$		640		
Fall Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 0.4 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_{fi}$	140	200	ns
Storage Time		@ $T_C = 125^\circ\text{C}$		300		
		@ $T_C = 25^\circ\text{C}$	$t_{si}$	2.3	2.75	$\mu\text{s}$
		@ $T_C = 125^\circ\text{C}$		2.8		
Crossover Time		@ $T_C = 25^\circ\text{C}$	$t_c$	400	600	ns
		@ $T_C = 125^\circ\text{C}$		725		

## TYPICAL STATIC CHARACTERISTICS

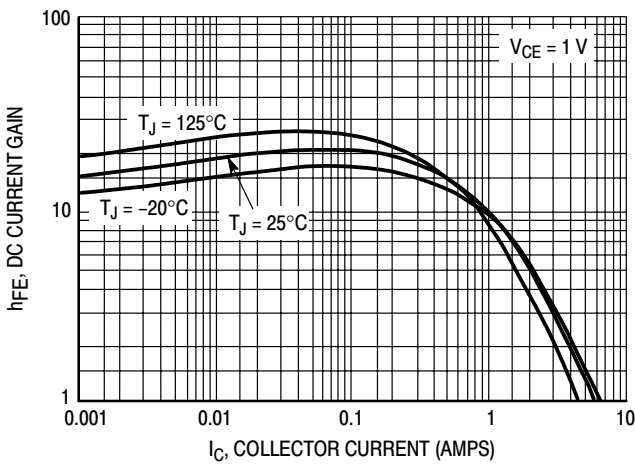


Figure 89. DC Current Gain @ 1 Volt

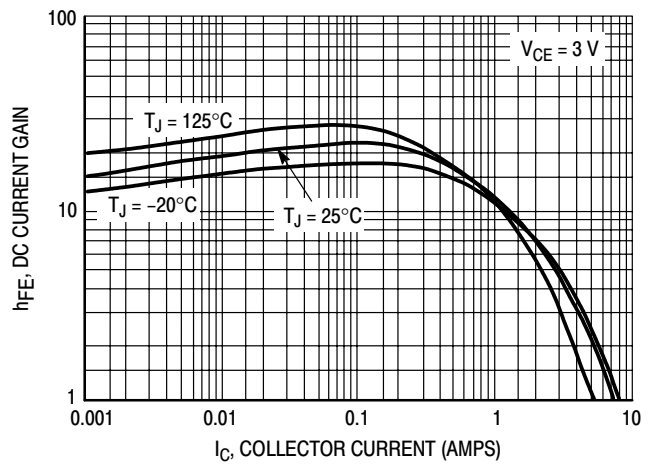


Figure 90. DC Current Gain @ 3 Volt

TYPICAL STATIC CHARACTERISTICS

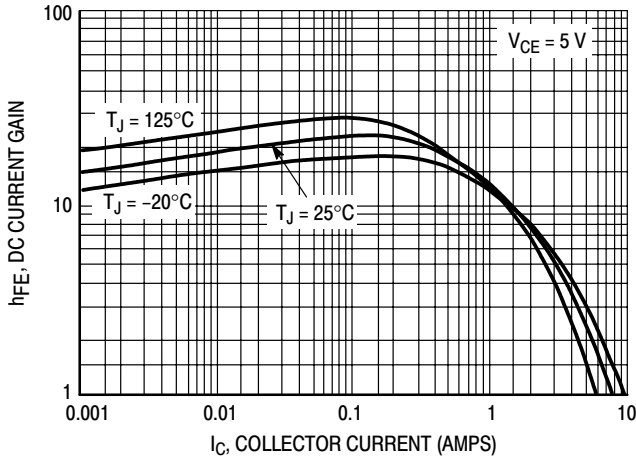


Figure 91. DC Current Gain @ 5 Volt

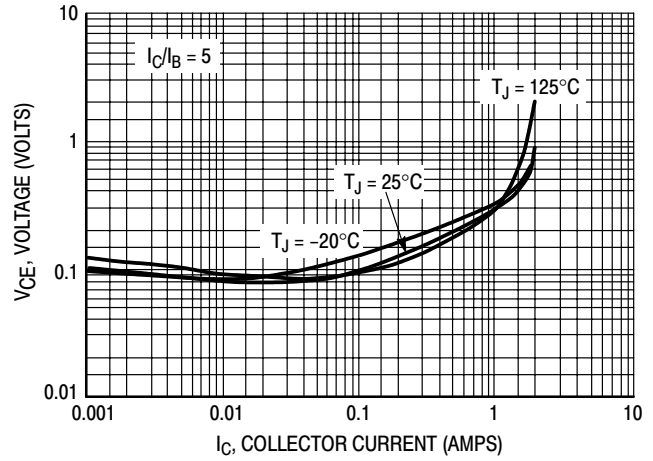


Figure 92. Collector-Emitter Saturation Voltage

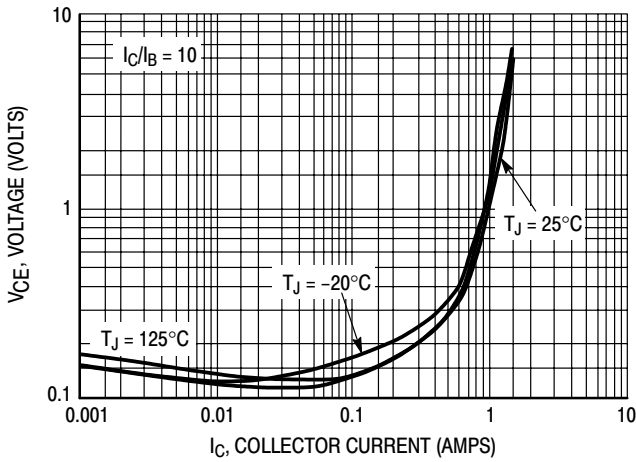


Figure 93. Collector-Emitter Saturation Voltage

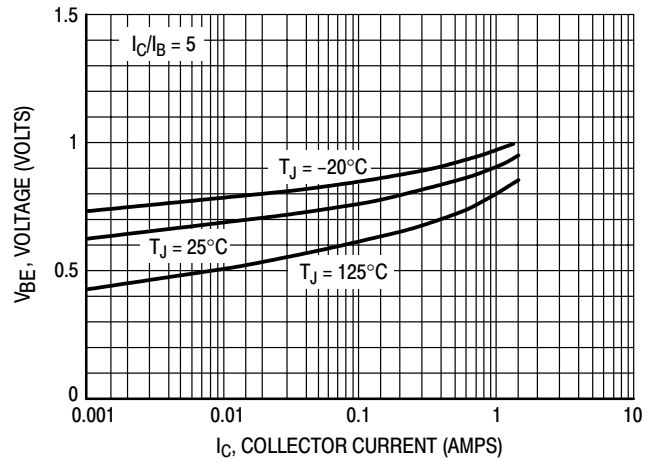


Figure 94. Base-Emitter Saturation Region

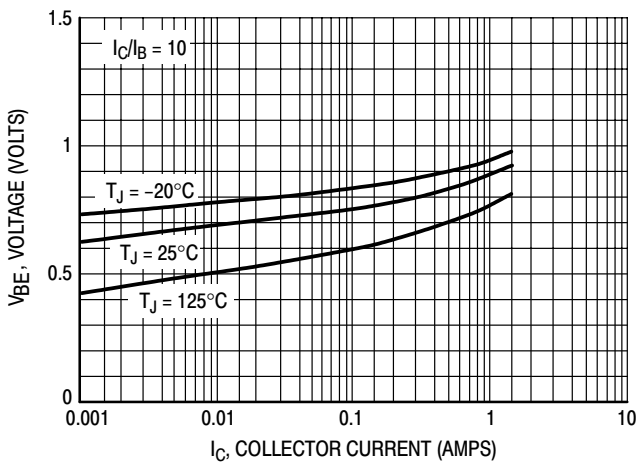


Figure 95. Base-Emitter Saturation Region

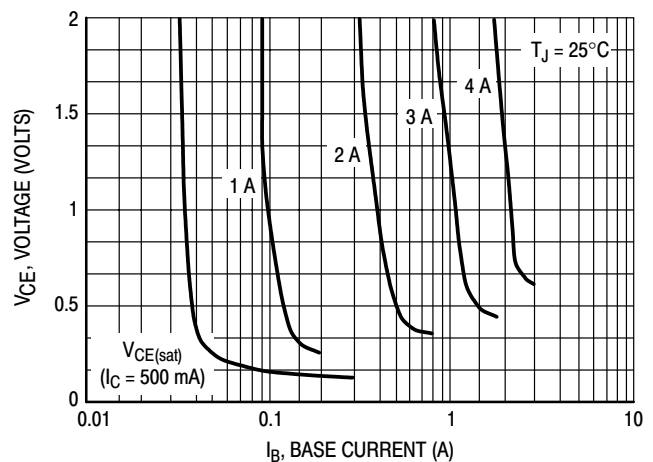


Figure 96. Collector Saturation Region

TYPICAL STATIC CHARACTERISTICS

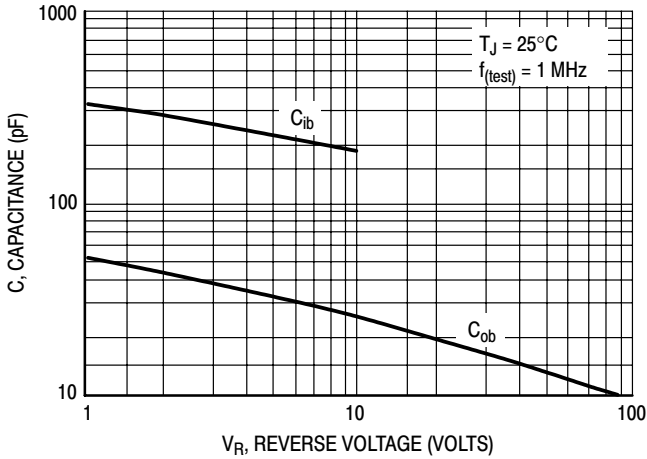


Figure 97. Capacitance

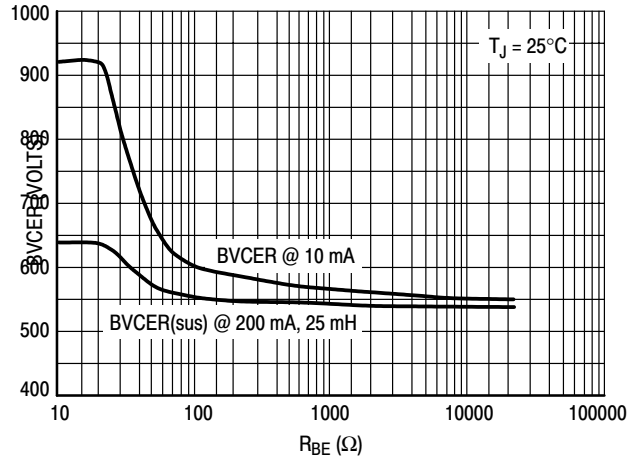


Figure 98. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

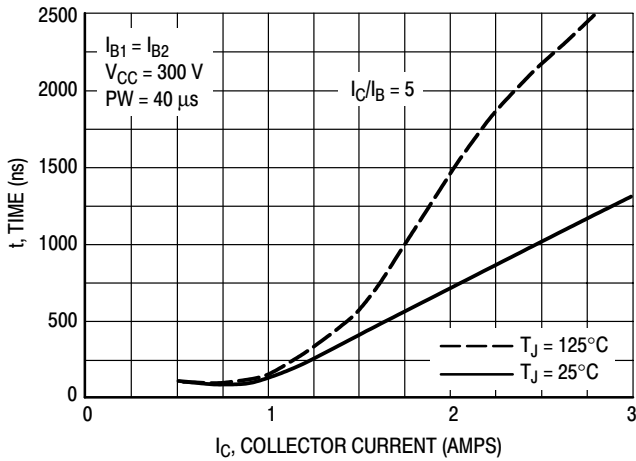


Figure 99. Resistive Switching,  $t_{on}$

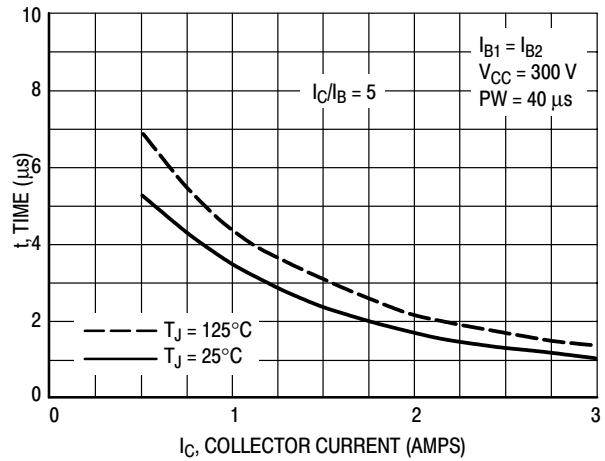


Figure 100. Resistive Switch Time,  $t_{off}$

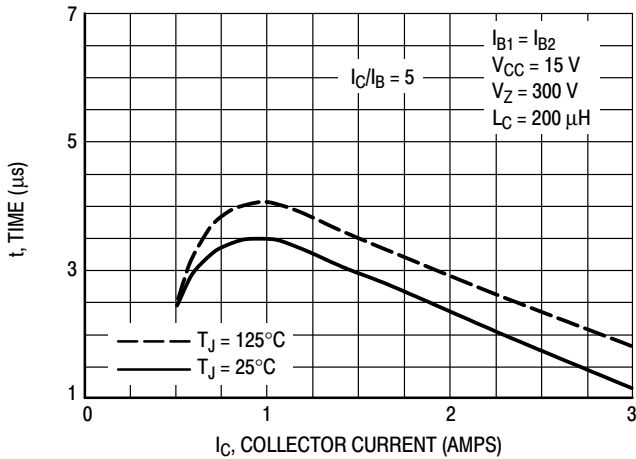


Figure 101. Inductive Storage Time,  $t_{si}$

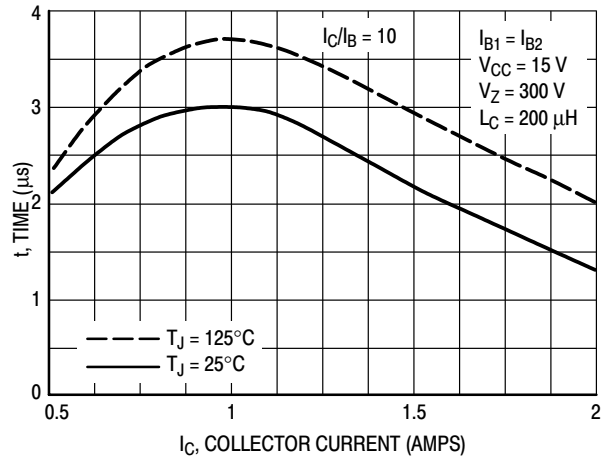


Figure 13 Bis. Inductive Storage Time,  $t_{si}$

TYPICAL SWITCHING CHARACTERISTICS

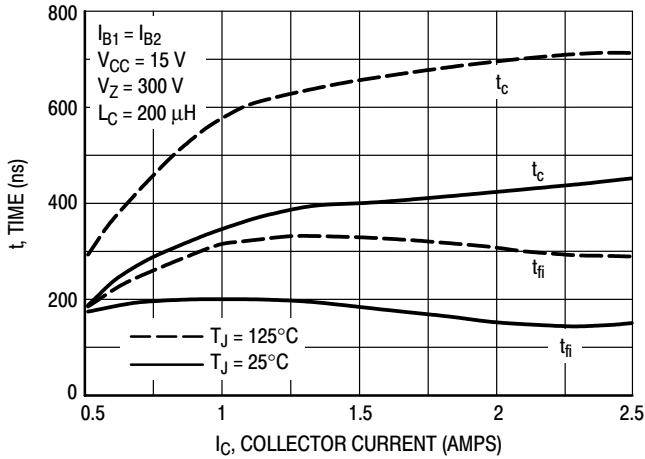


Figure 102. Inductive Storage Time,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 5$

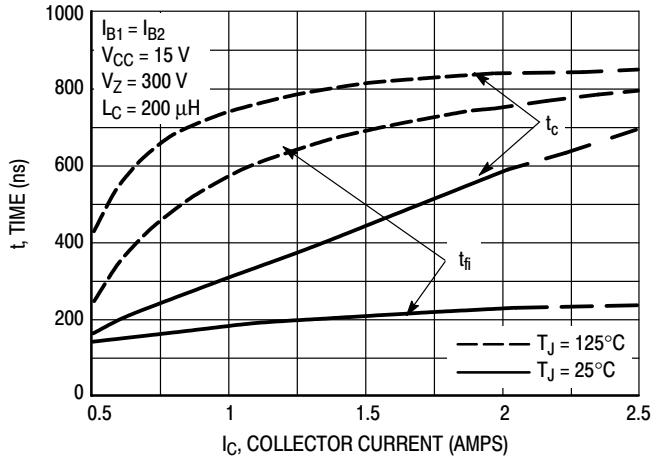


Figure 103. Inductive Storage Time,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 10$

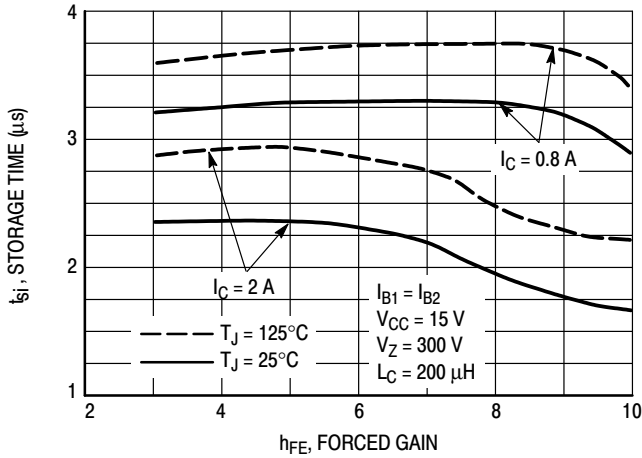


Figure 104. Inductive Storage Time

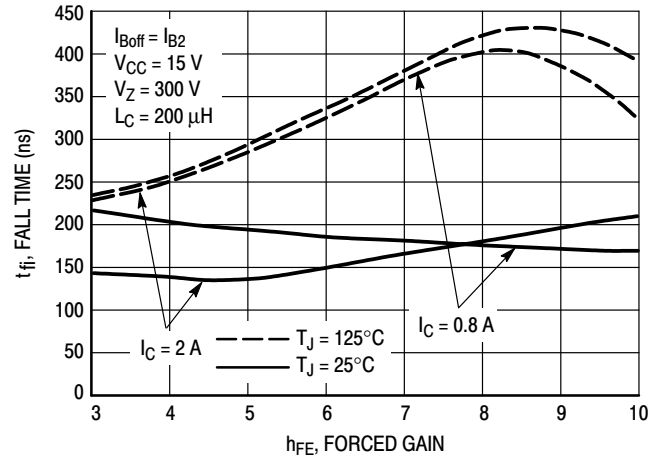


Figure 105. Inductive Fall Time

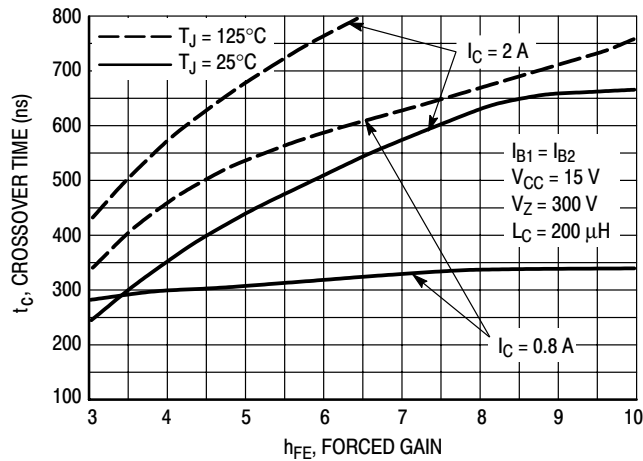


Figure 106. Inductive Crossover Time

TYPICAL SWITCHING CHARACTERISTICS

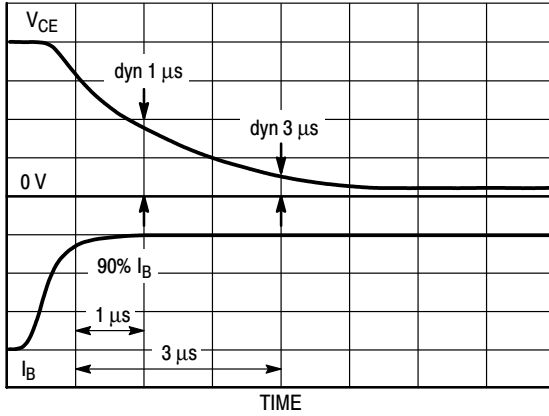


Figure 107. Dynamic Saturation Voltage Measurements

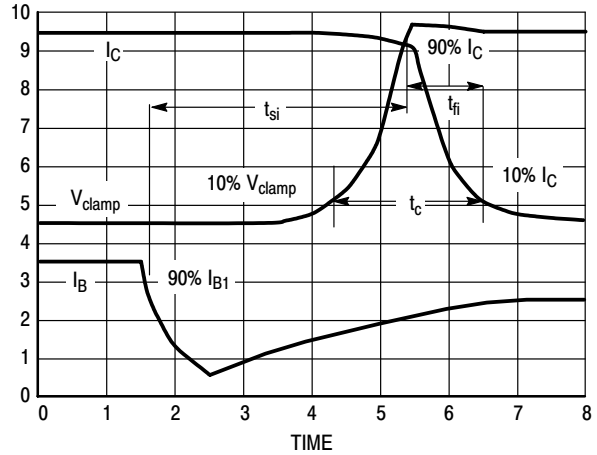
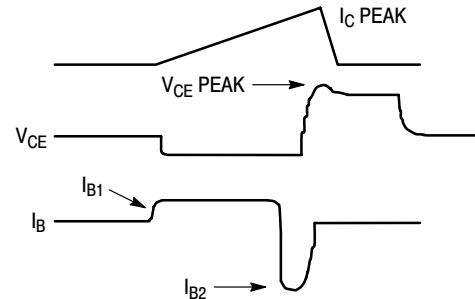
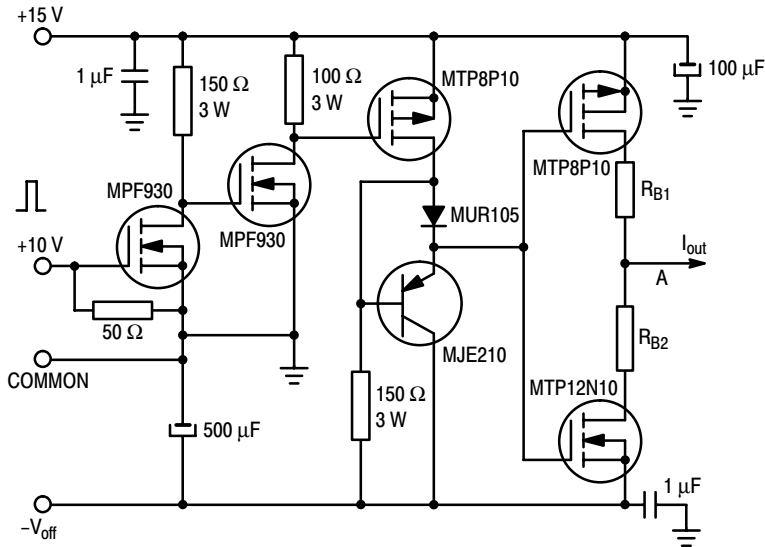


Figure 108. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit



$V_{(BR)CEO(sus)}$   
 $L = 10 \text{ mH}$   
 $R_{B2} = \infty$   
 $V_{CC} = 20 \text{ Volts}$   
 $I_{C(pk)} = 100 \text{ mA}$

**Inductive Switching**  
 $L = 200 \mu\text{H}$   
 $R_{B2} = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $R_{B1}$  selected for desired  $I_{B1}$

**RBSOA**  
 $L = 500 \mu\text{H}$   
 $R_{B2} = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $R_{B1}$  selected for desired  $I_{B1}$

TYPICAL THERMAL RESPONSE

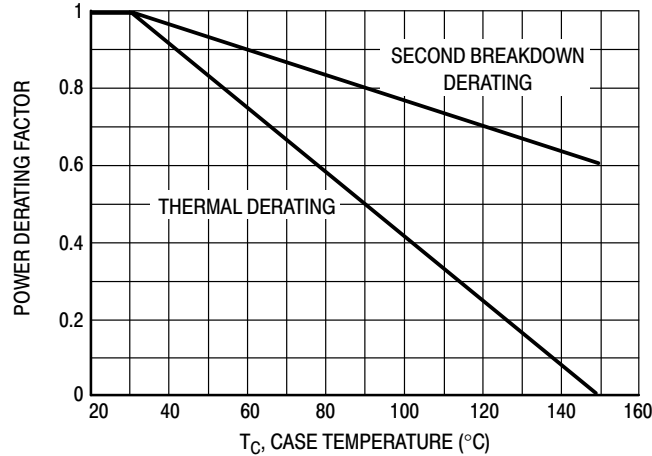


Figure 109. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 110 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 110 may be found at any case temperature by using the appropriate curve on Figure 109.

$T_{J(pk)}$  may be calculated from the data in Figure 112. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 111). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

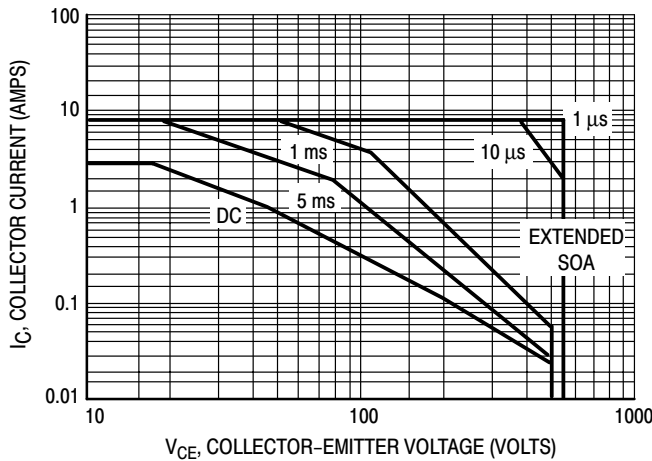


Figure 110. Forward Bias Safe Operating Area

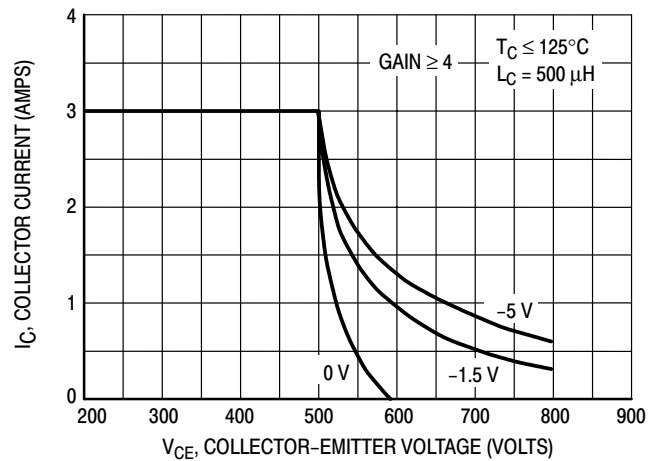


Figure 111. Reverse Bias Safe Operating Area

# BUH51

## TYPICAL THERMAL RESPONSE

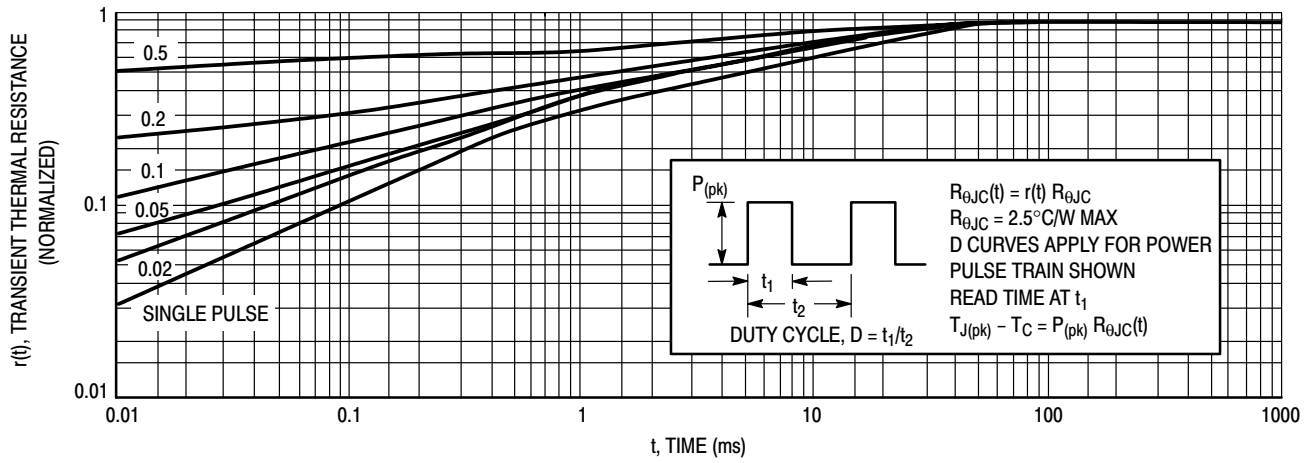


Figure 112. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for BUH51

# SWITCHMODE™

## NPN Bipolar Power Transistor

### For Switching Power Supply Applications

The BUL146/BUL146F have an applications specific state-of-the-art die designed for use in fluorescent electric lamp ballasts to 130 Watts and in Switchmode Power supplies for all types of electronic equipment. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain
  - Fast Switching
  - No Coil Required in Base Circuit for Turn-Off (No Current Tail)
- Full Characterization at 125°C
- Two Packages Choices: Standard TO220 or Isolated TO220
- Parametric Distributions are Tight and Consistent Lot-to-Lot
- BUL146F, Case 221D, is UL Recognized to 3500 V<sub>RMS</sub>: File # E69369

#### MAXIMUM RATINGS

Rating	Sym- bol	BUL146	BUL146F	Unit
Collector-Emitter Sustaining Voltage	V <sub>CEO</sub>	400		Vdc
Collector-Emitter Breakdown Voltage	V <sub>CES</sub>	700		Vdc
Emitter-Base Voltage	V <sub>EBO</sub>	9.0		Vdc
Collector Current – Continuous – Peak(1)	I <sub>C</sub> I <sub>CM</sub>	6.0 15		Adc
Base Current – Continuous – Peak(1)	I <sub>B</sub> I <sub>BM</sub>	4.0 8.0		Adc
RMS Isolation Voltage: (2) (for 1 sec, R.H. ≤ 30%, T <sub>C</sub> = 25° C)	V <sub>ISOL1</sub> V <sub>ISOL2</sub> V <sub>ISOL3</sub>	– – –	4500 3500 1500	Volts
Total Device Dissipation Derate above 25°C (T <sub>C</sub> = 25°C)	P <sub>D</sub>	100 0.8	40 0.32	Watts W/°C
Operating and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	– 65 to 150		°C

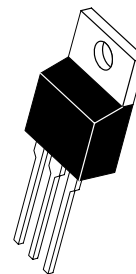
#### THERMAL CHARACTERISTICS

Rating	Sym- bol	BUL146	BUL146F	Unit
Thermal Resistance – Junction to Case – Junction to Ambient	R <sub>θJC</sub> R <sub>θJA</sub>	1.25 62.5	3.125 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T <sub>L</sub>	260		°C

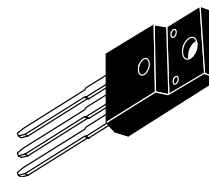
## BUL146

## BUL146F

**POWER TRANSISTOR**  
**6.0 AMPERES**  
**700 VOLTS**  
**40 and 100 WATTS**



**BUL146**  
**CASE 221A-09**  
**TO-220AB**



**CASE 221D-02**  
**ISOLATED TO-220 TYPE**  
**BUL146F**



# BUL146 BUL146F

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 100 mA, L = 25 mH)	V <sub>CEO(sus)</sub>	400	–	–	Vdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEO</sub> , I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	100	μAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CES</sub> , V <sub>EB</sub> = 0)	I <sub>CES</sub>	–	–	100	μAdc
		(T <sub>C</sub> = 125°C)	–	500	
(V <sub>CE</sub> = 500 V, V <sub>EB</sub> = 0)		–	–	100	
Emitter Cutoff Current (V <sub>EB</sub> = 9.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

## ELECTRICAL CHARACTERISTICS – (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### ON CHARACTERISTICS

Base–Emitter Saturation Voltage (I <sub>C</sub> = 1.3 Adc, I <sub>B</sub> = 0.13 Adc)	V <sub>BE(sat)</sub>	–	0.82	1.1	Vdc	
		–	0.93	1.25		
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 1.3 Adc, I <sub>B</sub> = 0.13 Adc)	V <sub>CE(sat)</sub>	–	0.22	0.5	Vdc	
		(T <sub>C</sub> = 125°C)	–	0.20		0.5
		(I <sub>C</sub> = 3.0 Adc, I <sub>B</sub> = 0.6 Adc)	–	0.30		0.7
			(T <sub>C</sub> = 125°C)	–		0.30
DC Current Gain (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 5.0 Vdc)	h <sub>FE</sub>	(T <sub>C</sub> = 125°C)	14	–	34	–
		–	–	30	–	
		(I <sub>C</sub> = 1.3 Adc, V <sub>CE</sub> = 1.0 Vdc)	12	20	–	
		(T <sub>C</sub> = 125°C)	12	20	–	
		(I <sub>C</sub> = 3.0 Adc, V <sub>CE</sub> = 1.0 Vdc)	8.0	13	–	
		(T <sub>C</sub> = 125°C)	7.0	12	–	
(I <sub>C</sub> = 10 mAdc, V <sub>CE</sub> = 5.0 Vdc)	10	20	–			

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1.0 MHz)	f <sub>T</sub>	–	14	–	MHz			
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1.0 MHz)	C <sub>OB</sub>	–	95	150	pF			
Input Capacitance (V <sub>EB</sub> = 8.0 V)	C <sub>IB</sub>	–	1000	1500	pF			
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I <sub>B1</sub> reaches 90% of final I <sub>B1</sub> (see Figure 18)	(I <sub>C</sub> = 1.3 Adc, I <sub>B1</sub> = 300 mAdc, V <sub>CC</sub> = 300 V)	1.0 μs	(T <sub>C</sub> = 125°C)	–	2.5	–	V	
		3.0 μs	(T <sub>C</sub> = 125°C)	–	6.5	–		
		(I <sub>C</sub> = 3.0 Adc, I <sub>B1</sub> = 0.6 Adc, V <sub>CC</sub> = 300 V)	1.0 μs	(T <sub>C</sub> = 125°C)	–	0.6		–
			3.0 μs	(T <sub>C</sub> = 125°C)	–	2.5		–
		V <sub>CE(dsat)</sub>	–	–	–	3.0		–
			–	–	–	7.0		–
		–	–	–	0.75	–		
		–	–	–	1.4	–		

## BUL146 BUL146F

### SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn-On Time	(I <sub>C</sub> = 1.3 Adc, I <sub>B1</sub> = 0.13 Adc I <sub>B2</sub> = 0.65 Adc, V <sub>CC</sub> = 300 V)	(T <sub>C</sub> = 125°C)	t <sub>on</sub>	–	100	200	ns
Turn-Off Time			t <sub>off</sub>	–	90	–	–
Turn-On Time	(I <sub>C</sub> = 3.0 Adc, I <sub>B1</sub> = 0.6 Adc I <sub>B1</sub> = 1.5 Adc, V <sub>CC</sub> = 300 V)	(T <sub>C</sub> = 125°C)	t <sub>on</sub>	–	90	150	ns
Turn-Off Time			t <sub>off</sub>	–	100	–	–
		(T <sub>C</sub> = 125°C)			1.7	2.5	μs
					2.1	–	

### SWITCHING CHARACTERISTICS: Inductive Load (V<sub>clamp</sub> = 300 V, V<sub>CC</sub> = 15 V, L = 200 μH)

Fall Time	(I <sub>C</sub> = 1.3 Adc, I <sub>B1</sub> = 0.13 Adc I <sub>B2</sub> = 0.65 Adc)	(T <sub>C</sub> = 125°C)	t <sub>fi</sub>	–	115	200	ns
Storage Time			t <sub>si</sub>	–	120	–	–
Crossover Time			t <sub>c</sub>	–	1.35	2.5	μs
		(T <sub>C</sub> = 125°C)			1.75	–	
		(T <sub>C</sub> = 125°C)			200	350	ns
					210	–	
Fall Time	(I <sub>C</sub> = 3.0 Adc, I <sub>B1</sub> = 0.6 Adc I <sub>B2</sub> = 1.5 Adc)	(T <sub>C</sub> = 125°C)	t <sub>fi</sub>	–	85	150	ns
Storage Time			t <sub>si</sub>	–	100	–	–
Crossover Time			t <sub>c</sub>	–	1.75	2.5	μs
		(T <sub>C</sub> = 125°C)			2.25	–	
		(T <sub>C</sub> = 125°C)			175	300	ns
					200	–	
Fall Time	(I <sub>C</sub> = 3.0 Adc, I <sub>B1</sub> = 0.6 Adc I <sub>B2</sub> = 0.6 Adc)	(T <sub>C</sub> = 125°C)	t <sub>fi</sub>	80	–	180	ns
Storage Time			t <sub>si</sub>	–	210	–	–
Crossover Time			t <sub>c</sub>	–	2.6	–	3.8
		(T <sub>C</sub> = 125°C)			–	–	
		(T <sub>C</sub> = 125°C)			4.5	–	
		(T <sub>C</sub> = 125°C)			230	350	ns
					400	–	

TYPICAL STATIC CHARACTERISTICS

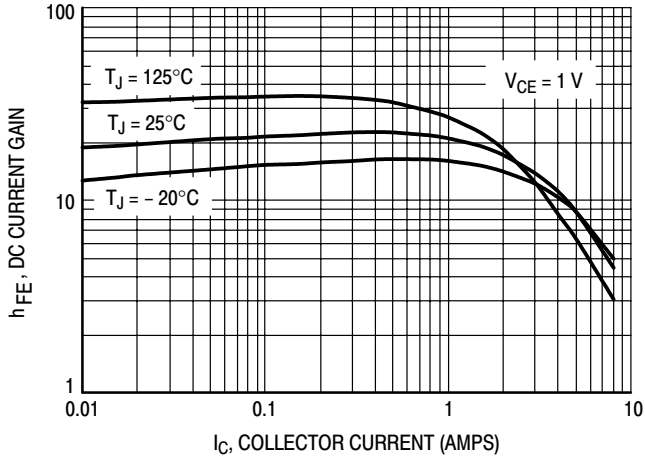


Figure 1. DC Current Gain @ 1 Volt

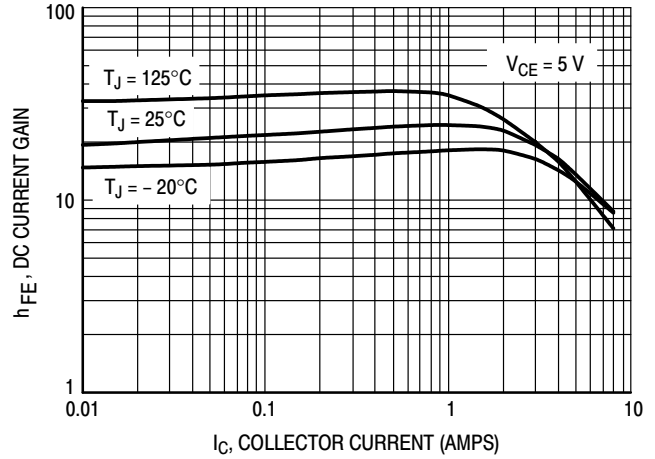


Figure 2. DC Current Gain @ 5 Volts

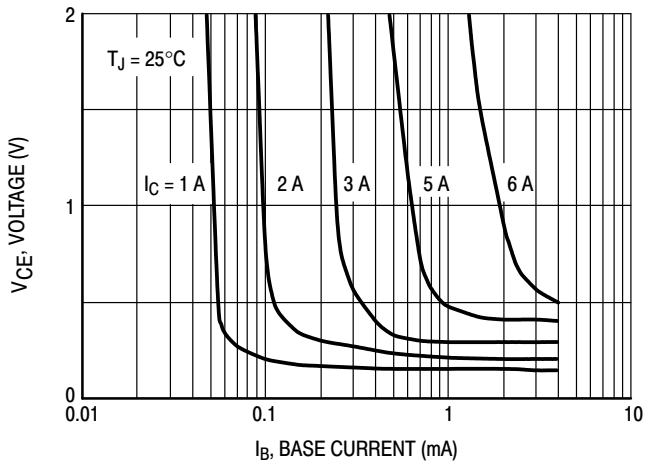


Figure 3. Collector Saturation Region

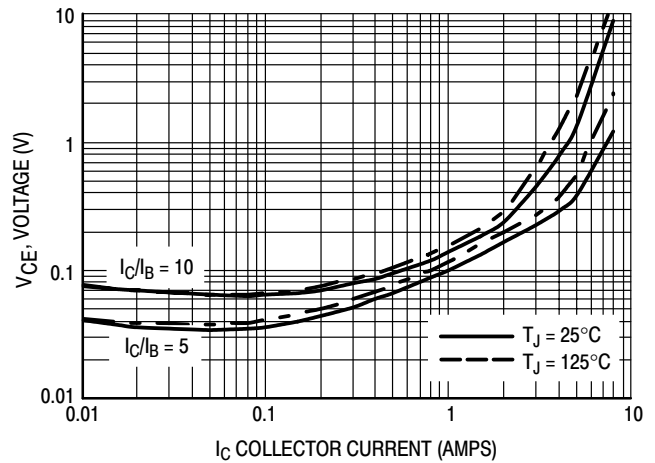


Figure 4. Collector-Emitter Saturation Voltage

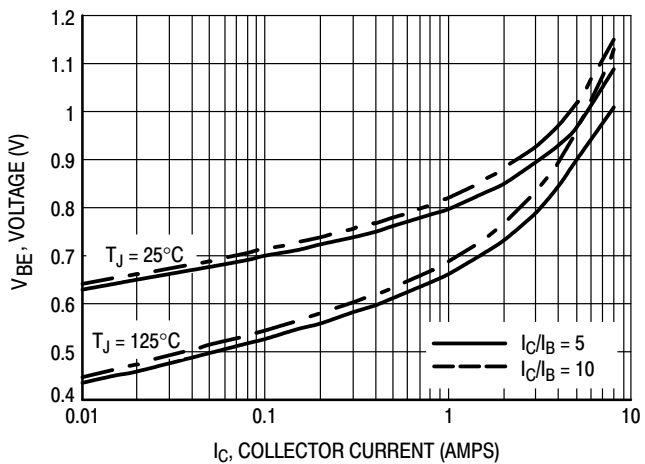


Figure 5. Base-Emitter Saturation Region

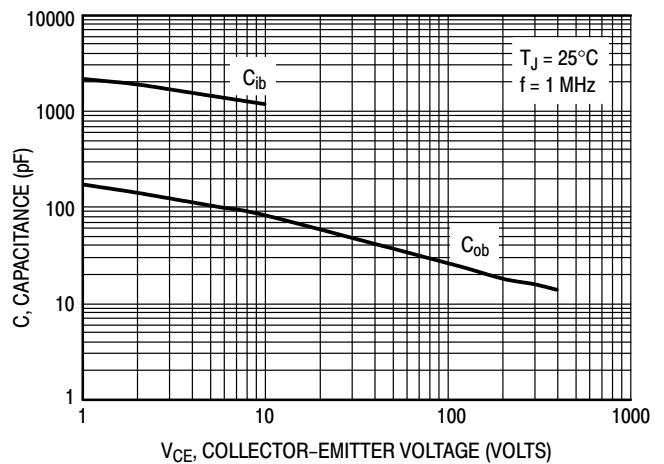


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

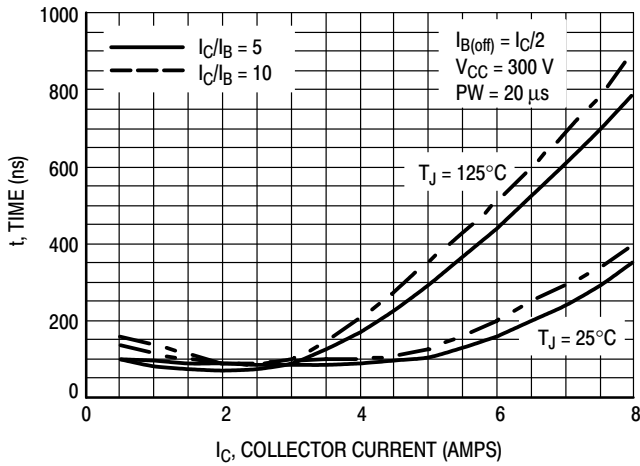


Figure 7. Resistive Switching,  $t_{on}$

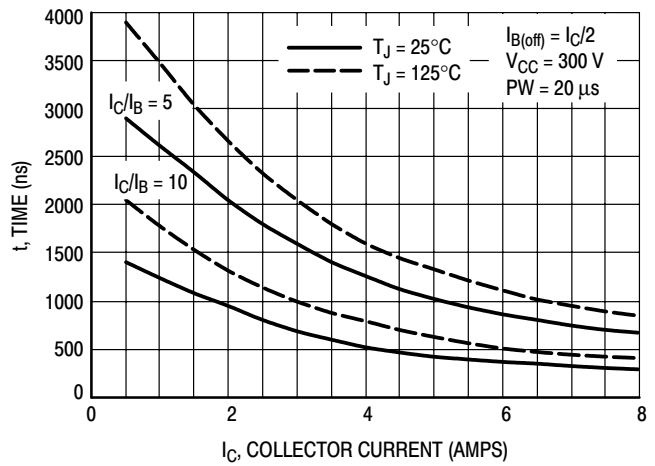


Figure 8. Resistive Switching,  $t_{off}$

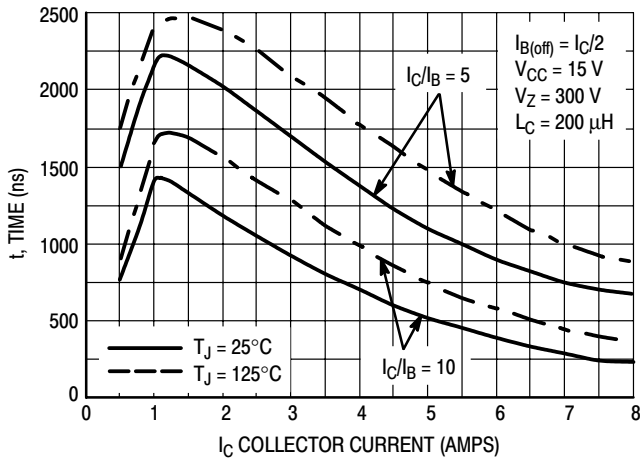


Figure 9. Inductive Storage Time,  $t_{si}$

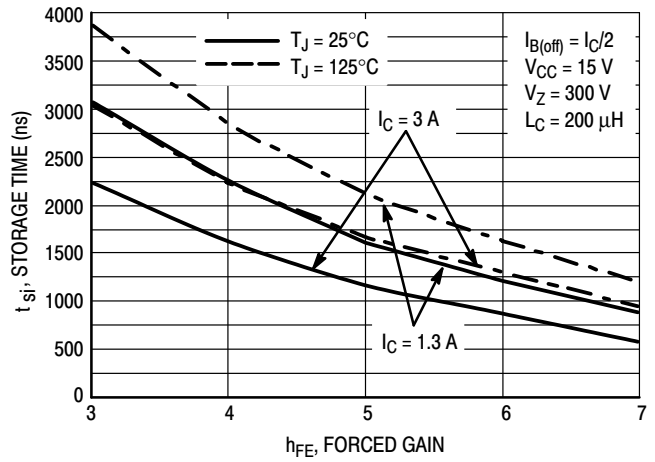


Figure 10. Inductive Storage Time,  $t_{si}(h_{FE})$

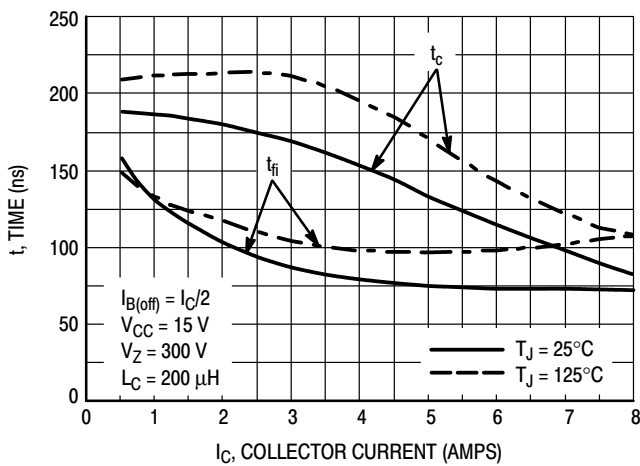


Figure 11. Inductive Switching,  $t_c$  and  $t_{fi}$   
 $I_C/I_B = 5$

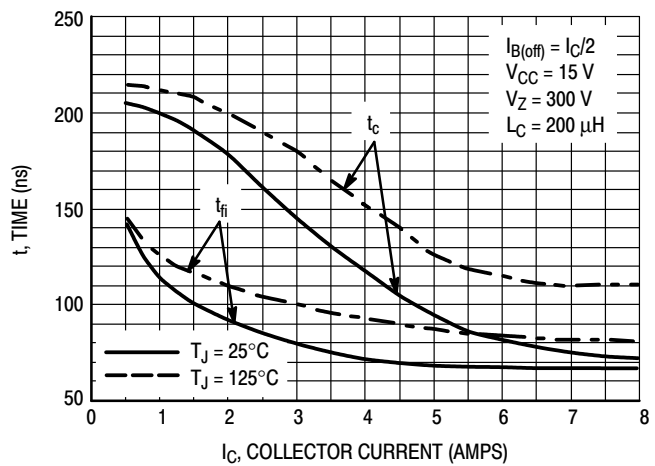


Figure 12. Inductive Switching,  $t_c$  and  $t_{fi}$   
 $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

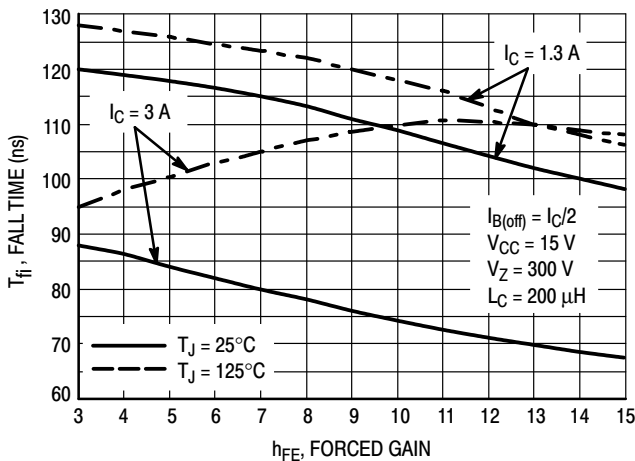


Figure 13. Inductive Fall Time

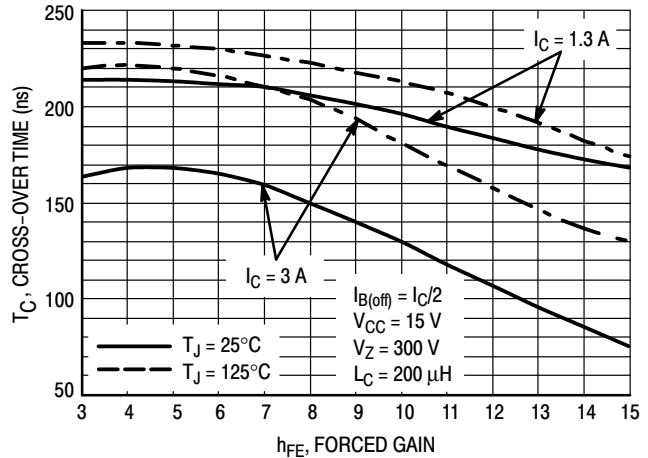


Figure 14. Inductive Cross-Over Time

GUARANTEED SAFE OPERATING AREA INFORMATION

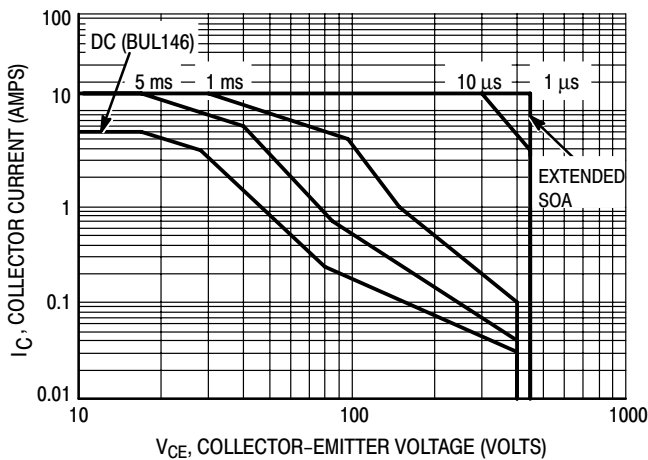


Figure 15. Forward Bias Safe Operating Area

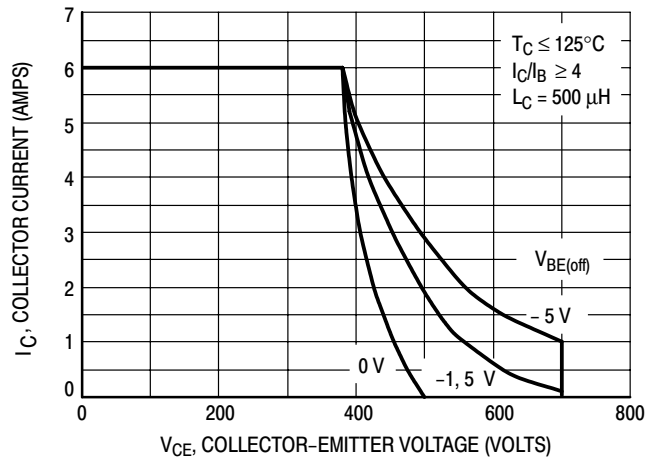


Figure 16. Reverse Bias Switching Safe Operating Area

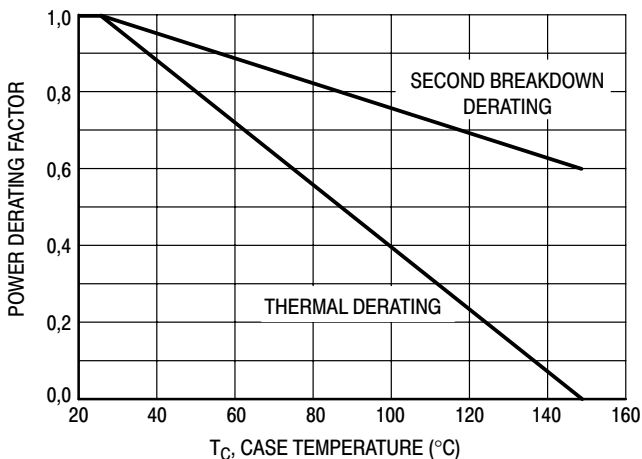


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.  $T_{J(pk)}$  may be calculated from the data in Figure 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse-biased. The safe level is specified as a reverse-biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

# BUL146 BUL146F

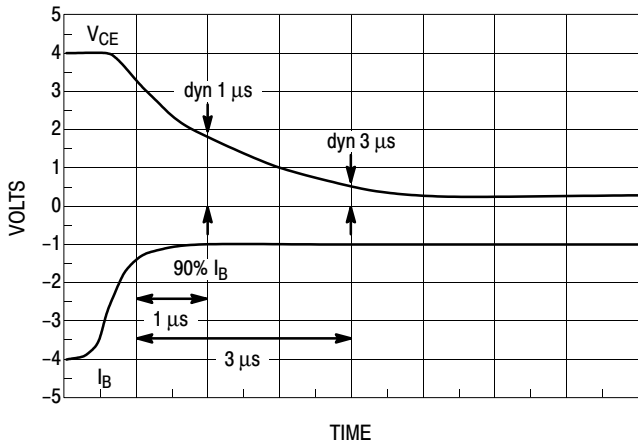


Figure 18. Dynamic Saturation Voltage Measurements

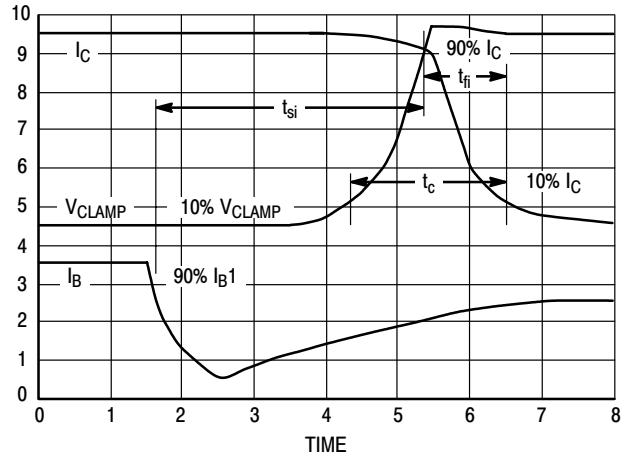
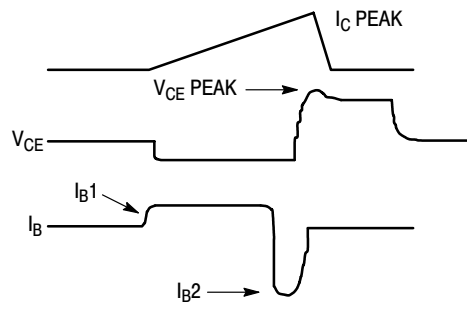
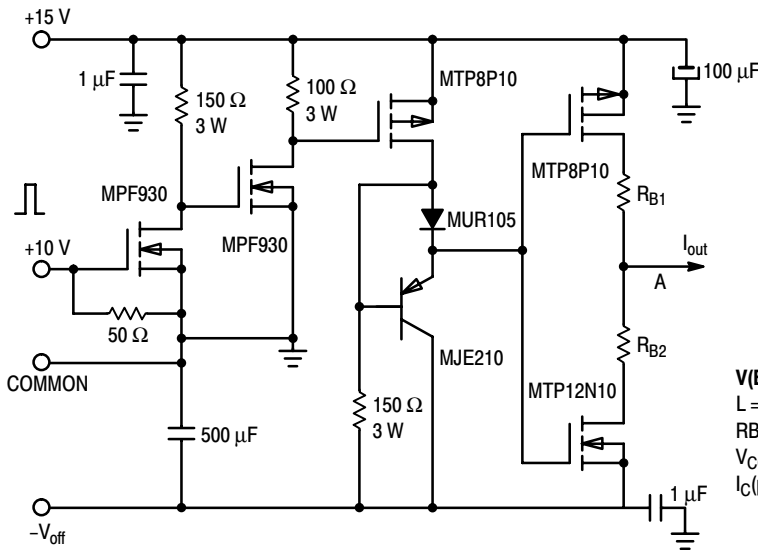


Figure 19. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
VCC = 20 VOLTS	VCC = 15 VOLTS	VCC = 15 VOLTS
IC(pk) = 100 mA	RB1 SELECTED FOR DESIRED IB1	RB1 SELECTED FOR DESIRED IB1

Table 1. Inductive Load Switching Drive Circuit

## TYPICAL THERMAL RESPONSE

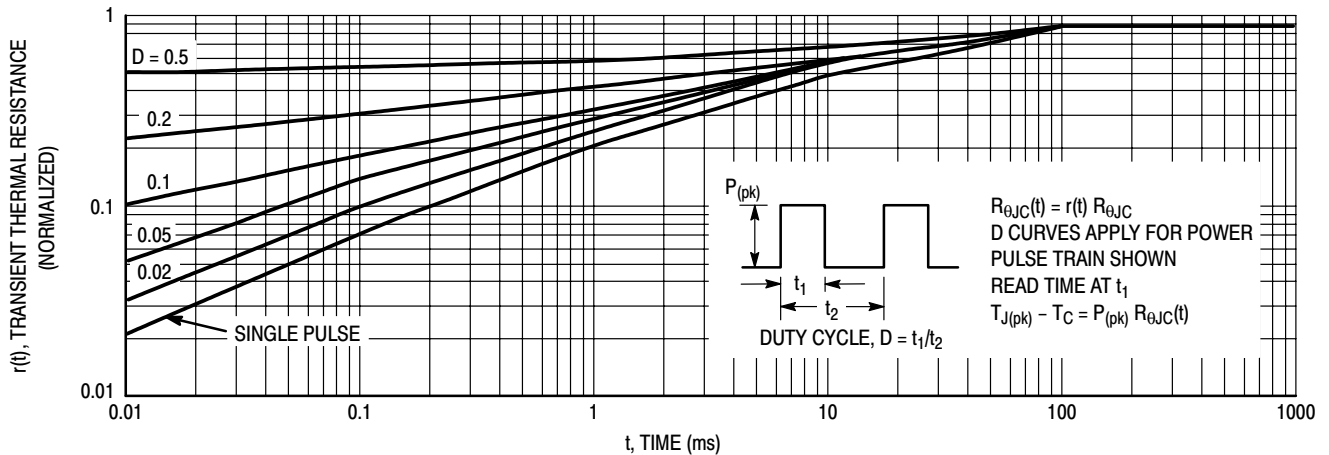


Figure 20. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for BUL146

# BUL146 BUL146F

## TYPICAL THERMAL RESPONSE

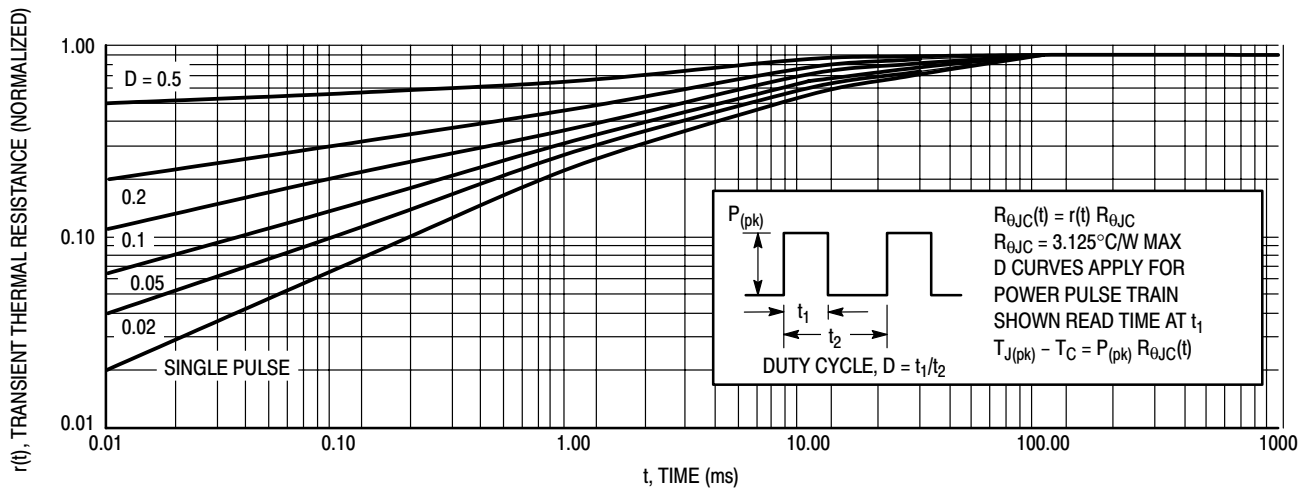


Figure 21. Typical Thermal Response for BUL146F

TEST CONDITIONS FOR ISOLATION TESTS\*

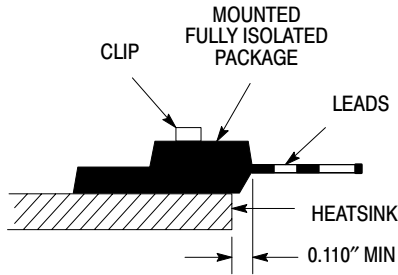


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

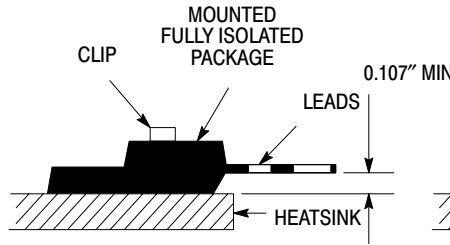


Figure 22b. Clip Mounting Position for Isolation Test Number 2

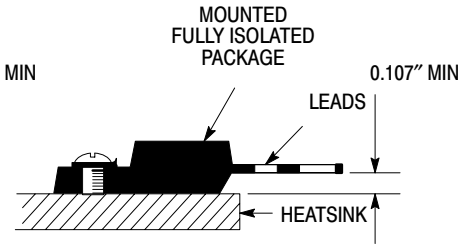


Figure 22c. Screw Mounting Position for Isolation Test Number 3

\*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION\*\*

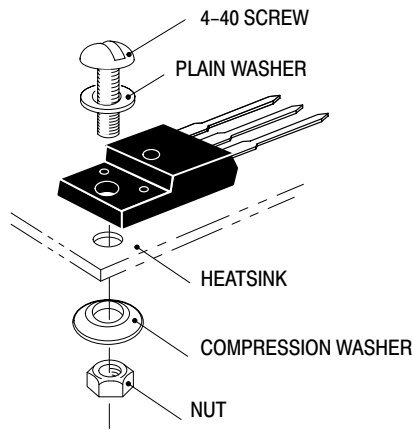


Figure 23a. Screw-Mounted

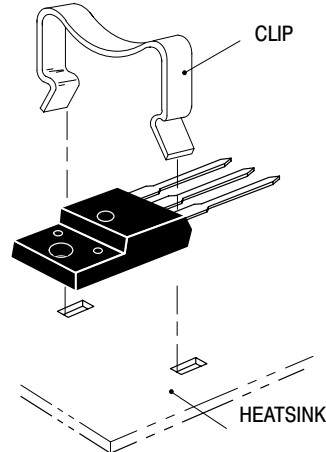


Figure 23b. Clip-Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.



# SWITCHMODE™

## NPN Bipolar Power Transistor

### For Switching Power Supply Applications

The BUL147 have an applications specific state-of-the-art die designed for use in electric fluorescent lamp ballasts to 180 Watts and in Switchmode Power supplies for all types of electronic equipment. These high-voltage/high-speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain
  - Fast Switching
  - No Coil Required in Base Circuit for Turn-Off (No Current Tail)
- Parametric Distributions are Tight and Consistent Lot-to-Lot
- Two Package Choices: Standard TO-220 or Isolated TO-220B

#### MAXIMUM RATINGS

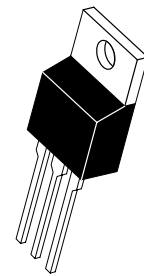
Rating	Symbol	BUL147	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	400	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	700	Vdc
Emitter-Base Voltage	$V_{EBO}$	9.0	Vdc
Collector Current — Continuous	$I_C$	8.0	Adc
— Peak(1)	$I_{CM}$	16	
Base Current — Continuous	$I_B$	4.0	Adc
— Peak(1)	$I_{BM}$	8.0	
Total Device Dissipation Derate above 25°C	$P_D$	125 1.0	Watts W/°C
Operating and Storage Temperature	$T_J, T_{stg}$	- 65 to 150	°C

#### THERMAL CHARACTERISTICS

Rating	Symbol	BUL44	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.0	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	260	°C

# BUL147

**POWER TRANSISTOR**  
**8.0 AMPERES**  
**700 VOLTS**  
**45 and 125 WATTS**



**BUL147**  
**CASE 221A-09**  
**TO-220AB**

# BUL147

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 100 mA, L = 25 mH)	V <sub>CEO(sus)</sub>	400	—	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEO</sub> , I <sub>B</sub> = 0)	I <sub>CEO</sub>	—	—	100	μAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CES</sub> , V <sub>EB</sub> = 0)	I <sub>CES</sub>	—	—	100	μAdc
(T <sub>C</sub> = 125°C)		—	—	500	
(V <sub>CE</sub> = 500 V, V <sub>EB</sub> = 0)	(T <sub>C</sub> = 125°C)	—	—	100	
Emitter Cutoff Current (V <sub>EB</sub> = 9.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	—	100	μAdc

### ON CHARACTERISTICS

Base–Emitter Saturation Voltage (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 0.2 Adc)	V <sub>BE(sat)</sub>	—	0.82	1.1	Vdc
(I <sub>C</sub> = 4.5 Adc, I <sub>B</sub> = 0.9 Adc)		—	0.92	1.25	
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 0.2 Adc)	V <sub>CE(sat)</sub>	—	0.25	0.5	Vdc
(T <sub>C</sub> = 125°C)		—	0.3	0.5	
(I <sub>C</sub> = 4.5 Adc, I <sub>B</sub> = 0.9 Adc)		—	0.35	0.7	
(T <sub>C</sub> = 125°C)		—	0.35	0.8	
DC Current Gain (I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 5.0 Vdc)	h <sub>FE</sub>	14	—	34	—
(T <sub>C</sub> = 125°C)		—	30	—	
(I <sub>C</sub> = 4.5 Adc, V <sub>CE</sub> = 1.0 Vdc)		8.0	12	—	
(T <sub>C</sub> = 125°C)		7.0	11	—	
(I <sub>C</sub> = 2.0 Adc, V <sub>CE</sub> = 1.0 Vdc) (T <sub>C</sub> = 25°C to 125°C)		10	18	—	
(I <sub>C</sub> = 10 mAdc, V <sub>CE</sub> = 5.0 Vdc)	10	20	—		

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1.0 MHz)	f <sub>T</sub>	—	14	—	MHz			
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1.0 MHz)	C <sub>ob</sub>	—	100	175	pF			
Input Capacitance (V <sub>EB</sub> = 8.0 V)	C <sub>ib</sub>	—	1750	2500	pF			
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I <sub>B1</sub> reaches 90% of final I <sub>B1</sub> (see Figure 18)	(I <sub>C</sub> = 2.0 Adc I <sub>B1</sub> = 200 mAdc V <sub>CC</sub> = 300 V)	1.0 μs (T <sub>C</sub> = 125°C)	V <sub>CE(dsat)</sub>	—	3.0	—	Volts	
		3.0 μs (T <sub>C</sub> = 125°C)		—	5.5	—		
		(I <sub>C</sub> = 5.0 Adc I <sub>B1</sub> = 0.9 Adc V <sub>CC</sub> = 300 V)		1.0 μs (T <sub>C</sub> = 125°C)	—	0.8		—
				3.0 μs (T <sub>C</sub> = 125°C)	—	1.4		—
				—	3.3	—		
				—	8.5	—		
				—	0.4	—		
				—	1.0	—		

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

# BUL147

## SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn-On Time	(I <sub>C</sub> = 2.0 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 1.0 Adc, V <sub>CC</sub> = 300 V)	(T <sub>C</sub> = 125°C)	t <sub>on</sub>	—	200	350	ns
Turn-Off Time			t <sub>off</sub>	—	190	—	—
Turn-On Time	(I <sub>C</sub> = 4.5 Adc, I <sub>B1</sub> = 0.9 Adc I <sub>B1</sub> = 2.25 Adc, V <sub>CC</sub> = 300 V)	(T <sub>C</sub> = 125°C)	t <sub>on</sub>	—	85	150	ns
Turn-Off Time			t <sub>off</sub>	—	100	—	—
		(T <sub>C</sub> = 125°C)			1.5	2.5	μs
					2.0	—	

## SWITCHING CHARACTERISTICS: Inductive Load (V<sub>clamp</sub> = 300 V, V<sub>CC</sub> = 15 V, L = 200 μH)

Fall Time	(I <sub>C</sub> = 2.0 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 1.0 Adc)	(T <sub>C</sub> = 125°C)	t <sub>fi</sub>	—	100	180	ns
Storage Time			t <sub>si</sub>	—	120	—	—
Crossover Time			t <sub>c</sub>	—	1.3	2.5	μs
		(T <sub>C</sub> = 125°C)			1.9	—	
Fall Time	(I <sub>C</sub> = 4.5 Adc, I <sub>B1</sub> = 0.9 Adc I <sub>B2</sub> = 2.25 Adc)	(T <sub>C</sub> = 125°C)	t <sub>fi</sub>	—	80	150	ns
Storage Time			t <sub>si</sub>	—	100	—	—
Crossover Time			t <sub>c</sub>	—	1.6	3.2	μs
		(T <sub>C</sub> = 125°C)			2.1	—	
Fall Time	(I <sub>C</sub> = 4.5 Adc, I <sub>B1</sub> = 0.9 Adc I <sub>B2</sub> = 0.9 Adc)	(T <sub>C</sub> = 125°C)	t <sub>fi</sub>	60	—	180	ns
Storage Time			t <sub>si</sub>	—	150	—	—
Crossover Time			t <sub>c</sub>	—	2.6	—	3.8
		(T <sub>C</sub> = 125°C)			4.3	—	
		(T <sub>C</sub> = 125°C)			200	350	ns
					330	—	

TYPICAL STATIC CHARACTERISTICS

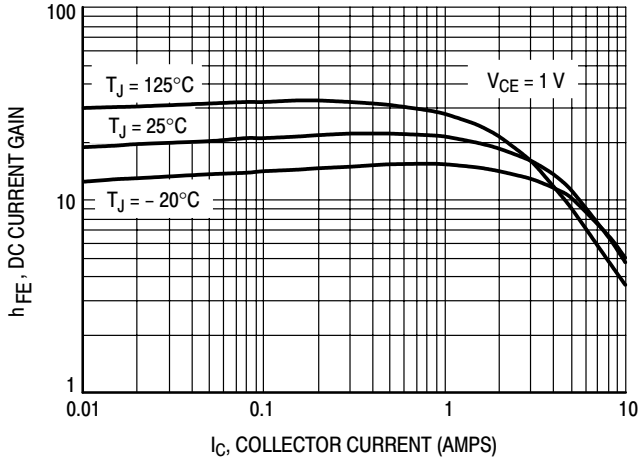


Figure 1. DC Current Gain @ 1 Volt

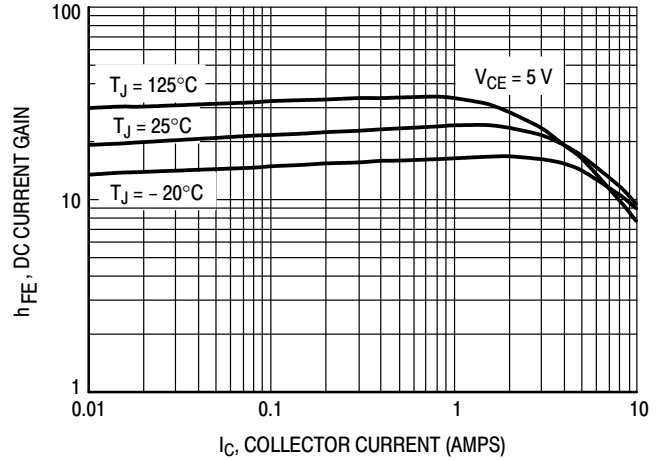


Figure 2. DC Current Gain @ 5 Volts

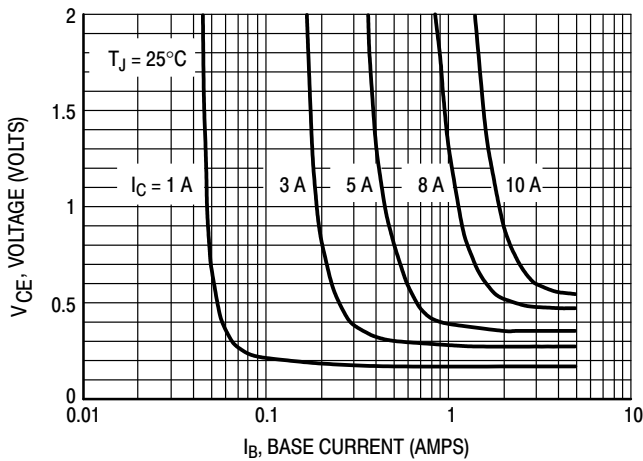


Figure 3. Collector Saturation Region

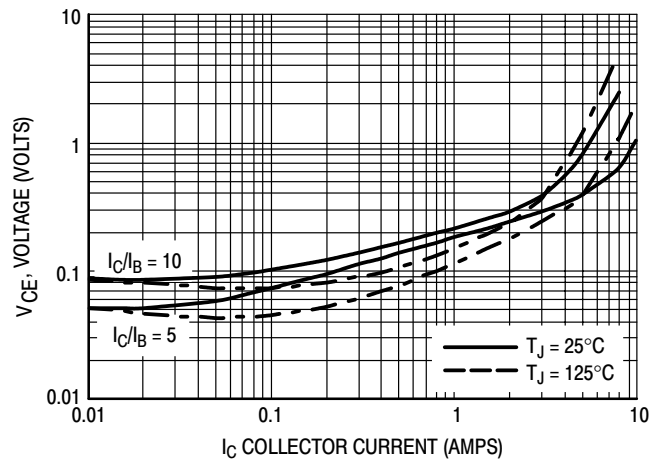


Figure 4. Collector-Emitter Saturation Voltage

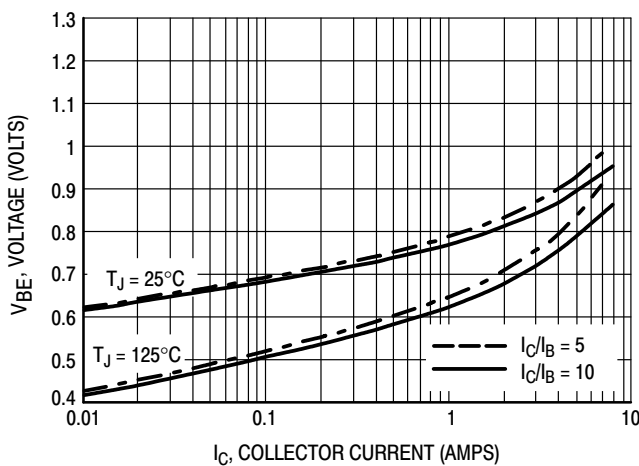


Figure 5. Base-Emitter Saturation Region

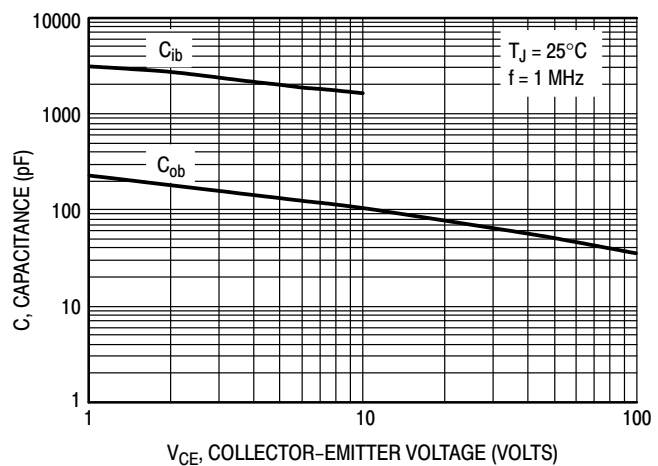


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

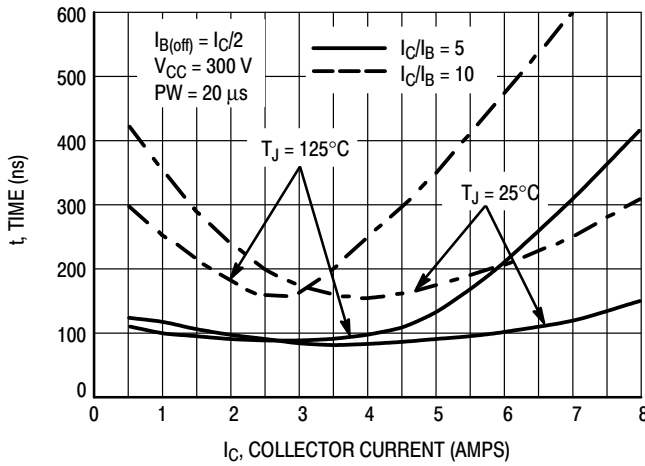


Figure 7. Resistive Switching,  $t_{on}$

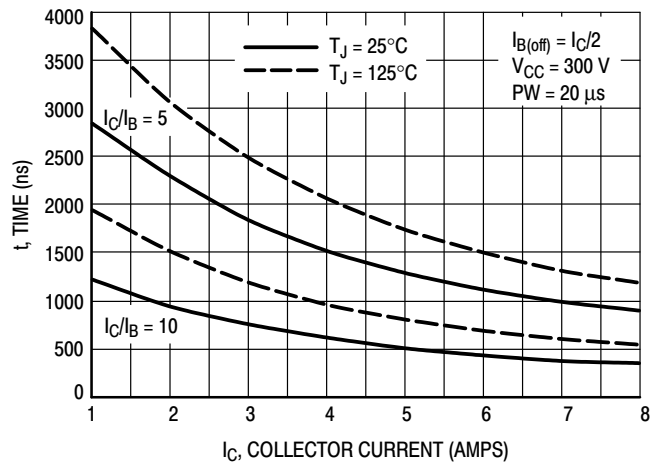


Figure 8. Resistive Switching,  $t_{off}$

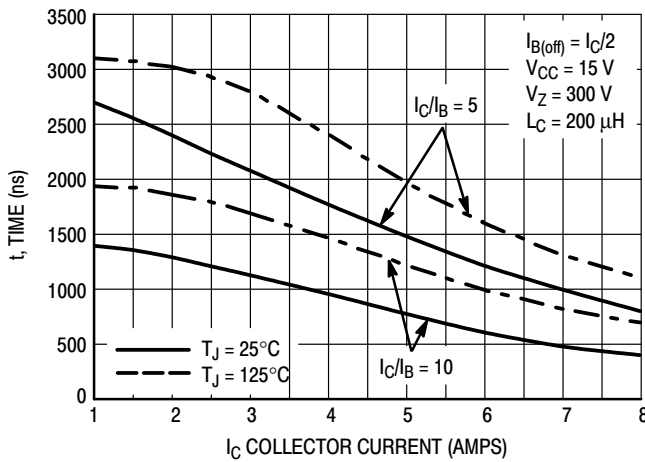


Figure 9. Inductive Storage Time,  $t_{si}$

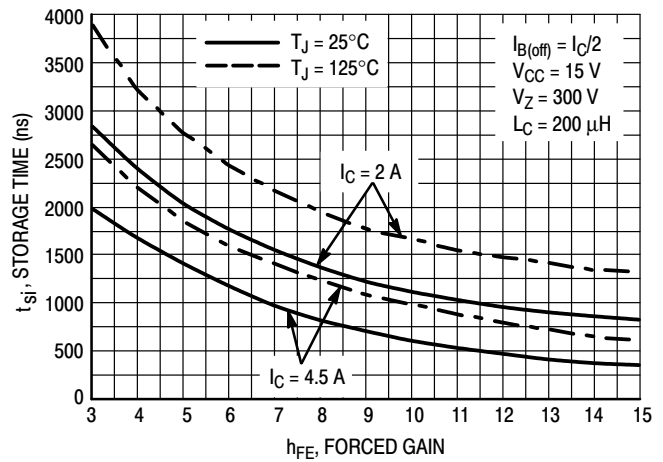


Figure 10. Inductive Storage Time,  $t_{si}(h_{FE})$

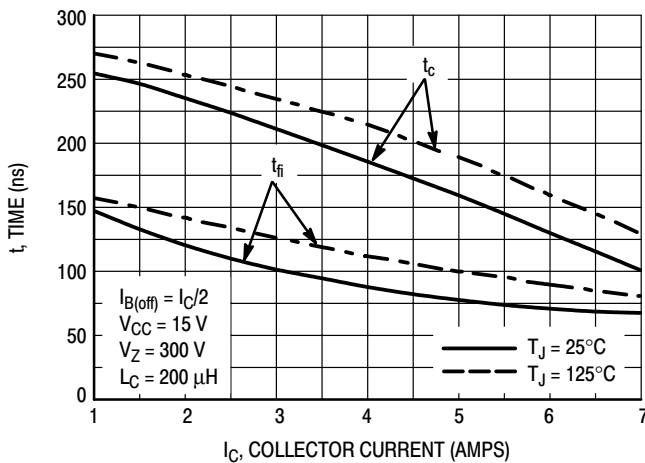


Figure 11. Inductive Switching,  $t_c$  and  $t_{fi}$   
 $I_C/I_B = 5$

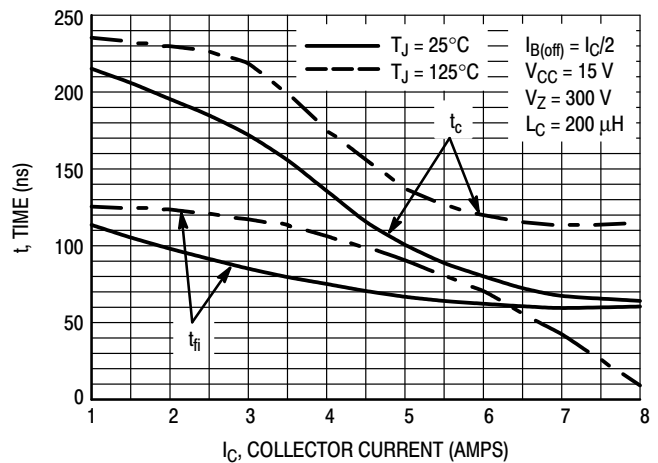


Figure 12. Inductive Switching,  $t_c$  and  $t_{fi}$   
 $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

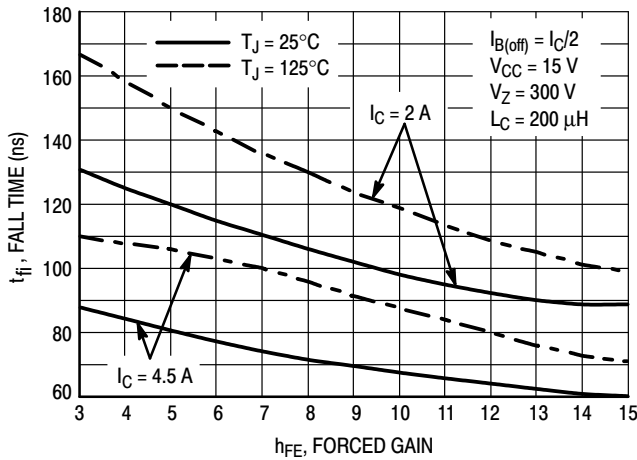


Figure 13. Inductive Fall Time

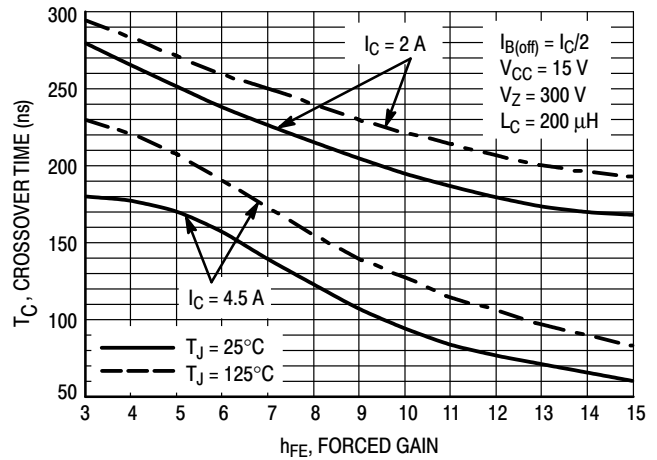


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

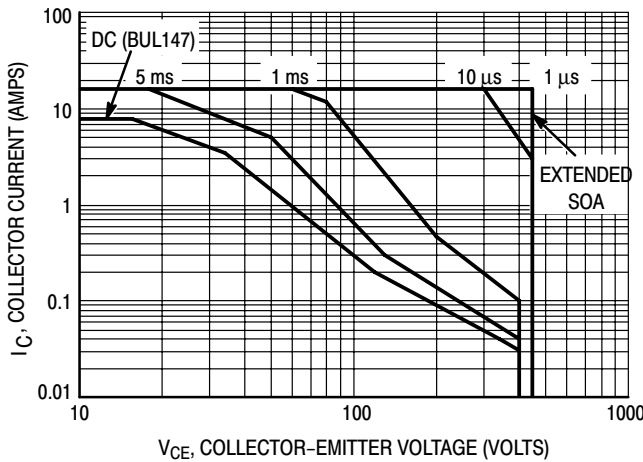


Figure 15. Forward Bias Safe Operating Area

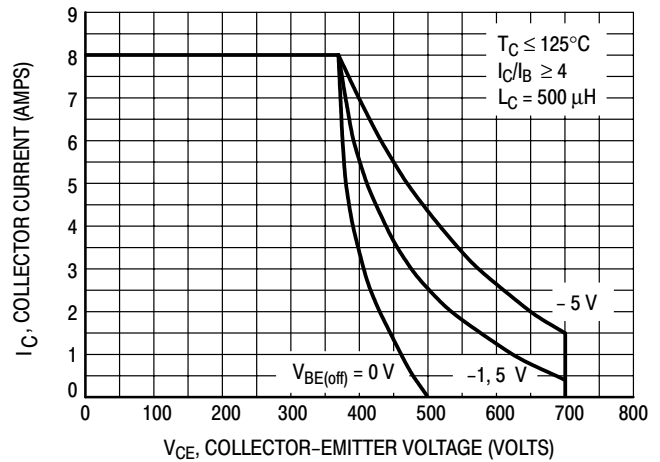


Figure 16. Reverse Bias Switching Safe Operating Area

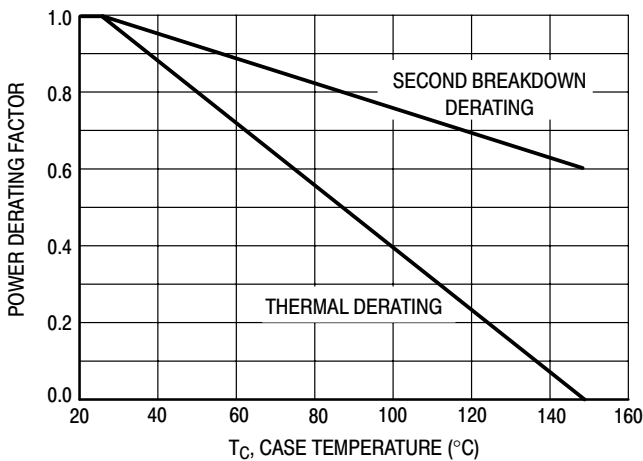


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.  $T_{J(pk)}$  may be calculated from the data in Figure 20 and NO TAG. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse-biased. The safe level is specified as a reverse-biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

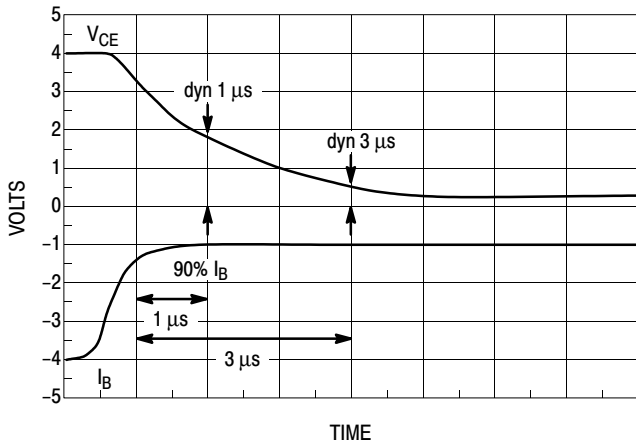


Figure 18. Dynamic Saturation Voltage Measurements

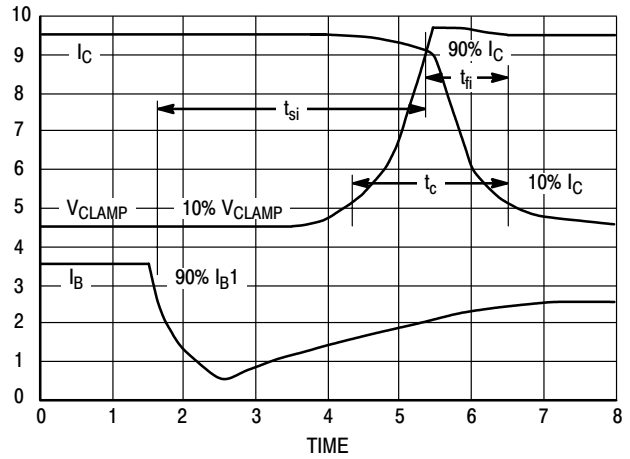
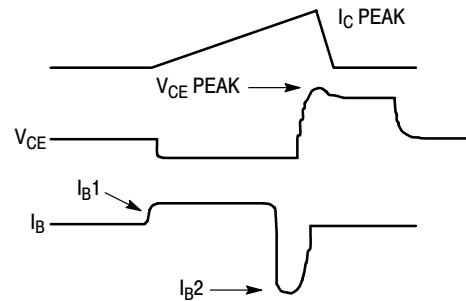
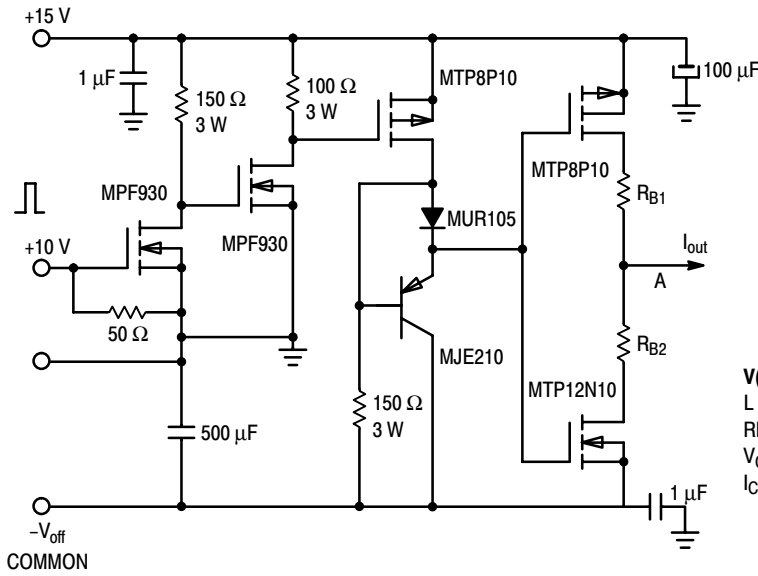


Figure 19. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V <sub>CC</sub> = 20 VOLTS	V <sub>CC</sub> = 15 VOLTS	V <sub>CC</sub> = 15 VOLTS
I <sub>C(pk)</sub> = 100 mA	RB1 SELECTED FOR DESIRED I <sub>B1</sub>	RB1 SELECTED FOR DESIRED I <sub>B1</sub>

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

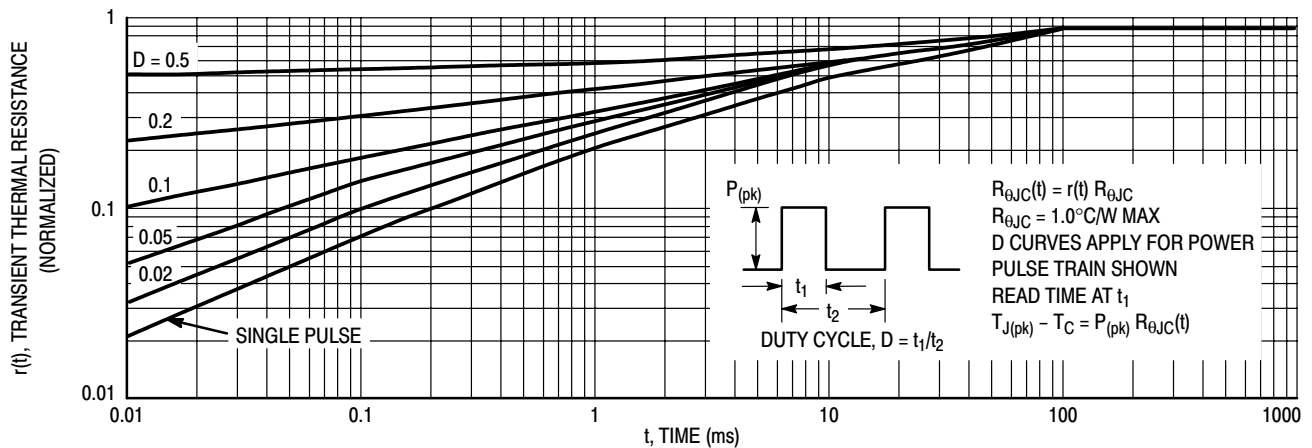


Figure 20. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for BUL147

# SWITCHMODE™

## NPN Bipolar Power Transistor

### For Switching Power Supply Applications

The BUL44 have an applications specific state-of-the-art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain  $h_{FE}$
  - Fast Switching
  - No Coil Required in Base Circuit for Turn-Off (No Current Tail)
- Full Characterization at 125°C
- Tight Parametric Distributions are Consistent Lot-to-Lot

#### MAXIMUM RATINGS

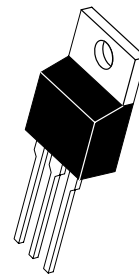
Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	400	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	700	Vdc
Emitter-Base Voltage	$V_{EBO}$	9.0	Vdc
Collector Current — Continuous	$I_C$	2.0	Adc
— Peak(1)	$I_{CM}$	5.0	
Base Current — Continuous	$I_B$	1.0	Adc
— Peak(1)	$I_{BM}$	2.0	
Total Device Dissipation Derate above 25°C	$P_D$	50 0.4	Watts W/°C
Operating and Storage Temperature	$T_J, T_{stg}$	- 65 to 150	°C

#### THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	2.5	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	260	°C

# BUL44

**POWER TRANSISTOR**  
**2.0 AMPERES**  
**700 VOLTS**  
**40 and 100 WATTS**



**BUL44**  
**CASE 221A-06**  
**TO-220AB**



# BUL44

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 100 mA, L = 25 mH)	V <sub>CEO(sus)</sub>	400	—	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEO</sub> , I <sub>B</sub> = 0)	I <sub>CEO</sub>	—	—	100	μAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CES</sub> , V <sub>EB</sub> = 0)	I <sub>CES</sub>	—	—	100	μAdc
(T <sub>C</sub> = 125°C)		—	—	500	
(V <sub>CE</sub> = 500 V, V <sub>EB</sub> = 0)		—	—	100	
(T <sub>C</sub> = 125°C)		—	—	100	
Emitter Cutoff Current (V <sub>EB</sub> = 9.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	—	100	μAdc

## ON CHARACTERISTICS

Base–Emitter Saturation Voltage (I <sub>C</sub> = 0.4 Adc, I <sub>B</sub> = 40 mAdc)	V <sub>BE(sat)</sub>	—	0.85	1.1	Vdc
(I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.2 Adc)		—	0.92	1.25	
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 0.4 Adc, I <sub>B</sub> = 40 mAdc)	V <sub>CE(sat)</sub>	—	0.20	0.5	Vdc
(I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.2 Adc)		—	0.20	0.5	
(T <sub>C</sub> = 125°C)		—	0.25	0.6	
(T <sub>C</sub> = 125°C)		—	0.25	0.6	
DC Current Gain (I <sub>C</sub> = 0.2 Adc, V <sub>CE</sub> = 5.0 Vdc)	h <sub>FE</sub>	14	—	34	—
(I <sub>C</sub> = 0.4 Adc, V <sub>CE</sub> = 1.0 Vdc)		—	32	—	
(I <sub>C</sub> = 0.4 Adc, V <sub>CE</sub> = 1.0 Vdc)		12	20	—	
(I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 1.0 Vdc)		12	20	—	
(I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 1.0 Vdc)		8.0	14	—	
(I <sub>C</sub> = 10 mAdc, V <sub>CE</sub> = 5.0 Vdc)		7.0	13	—	
		10	22	—	

## DYNAMIC CHARACTERISTICS

Current Gain Bandwidth (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1.0 MHz)	f <sub>T</sub>	—	13	—	MHz		
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1.0 MHz)	C <sub>OB</sub>	—	38	60	pF		
Input Capacitance (V <sub>EB</sub> = 8.0 V)	C <sub>IB</sub>	—	380	600	pF		
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I <sub>B1</sub> reaches 90% of final I <sub>B1</sub>	V <sub>CE(dsat)</sub>	(I <sub>C</sub> = 0.4 Adc, I <sub>B1</sub> = 40 mAdc, V <sub>CC</sub> = 300 V)	1.0 μs (T <sub>C</sub> = 125°C)	—	2.5	—	Vdc
			3.0 μs (T <sub>C</sub> = 125°C)	—	2.7	—	
		(I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = 0.2 Adc, V <sub>CC</sub> = 300 V)	1.0 μs (T <sub>C</sub> = 125°C)	—	1.3	—	
			3.0 μs (T <sub>C</sub> = 125°C)	—	1.15	—	
			1.0 μs (T <sub>C</sub> = 125°C)	—	3.2	—	
			3.0 μs (T <sub>C</sub> = 125°C)	—	7.5	—	
			1.25	—			
			1.6	—			

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

(continued)

# BUL44

## SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn-On Time	(I <sub>C</sub> = 0.4 Adc, I <sub>B1</sub> = 40 mAdc I <sub>B2</sub> = 0.2 Adc, V <sub>CC</sub> = 300 V) (T <sub>C</sub> = 125°C)	t <sub>on</sub>	—	40	100	ns
Turn-Off Time		t <sub>off</sub>	—	40	—	—
Turn-On Time	(I <sub>C</sub> = 0.4 Adc, I <sub>B1</sub> = 40 mAdc I <sub>B2</sub> = 0.2 Adc, V <sub>CC</sub> = 300 V) (T <sub>C</sub> = 125°C)	t <sub>on</sub>	—	1.5	2.5	μs
Turn-Off Time		t <sub>off</sub>	—	2.0	—	—
Turn-On Time	(I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B1</sub> = 0.5 Adc, V <sub>CC</sub> = 300 V) (T <sub>C</sub> = 125°C)	t <sub>on</sub>	—	85	150	ns
Turn-Off Time		t <sub>off</sub>	—	85	—	—
Turn-On Time	(I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.5 Adc, V <sub>CC</sub> = 300 V) (T <sub>C</sub> = 125°C)	t <sub>on</sub>	—	1.75	2.5	μs
Turn-Off Time		t <sub>off</sub>	—	2.10	—	—

## SWITCHING CHARACTERISTICS: Inductive Load (V<sub>clamp</sub> = 300 V, V<sub>CC</sub> = 15 V, L = 200 μH)

Fall Time	(I <sub>C</sub> = 0.4 Adc, I <sub>B1</sub> = 40 mAdc I <sub>B2</sub> = 0.2 Adc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	—	125	200	ns
Storage Time		t <sub>si</sub>	—	120	—	—
Crossover Time		t <sub>c</sub>	—	0.7	1.25	μs
Fall Time	(I <sub>C</sub> = 0.4 Adc, I <sub>B1</sub> = 40 mAdc I <sub>B2</sub> = 0.2 Adc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	—	0.8	—	—
Storage Time		t <sub>si</sub>	—	110	200	ns
Crossover Time		t <sub>c</sub>	—	110	—	—
Fall Time	(I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.5 Adc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	—	110	175	ns
Storage Time		t <sub>si</sub>	—	120	—	—
Crossover Time		t <sub>c</sub>	—	1.7	2.75	μs
Fall Time	(I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.5 Adc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	—	2.25	—	—
Storage Time		t <sub>si</sub>	—	180	300	ns
Crossover Time		t <sub>c</sub>	—	210	—	—
Fall Time	(I <sub>C</sub> = 0.8 Adc, I <sub>B1</sub> = 160 mAdc I <sub>B2</sub> = 160 mAdc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	70	—	170	ns
Storage Time		t <sub>si</sub>	—	180	—	—
Crossover Time		t <sub>c</sub>	2.6	—	3.8	μs
Fall Time	(I <sub>C</sub> = 0.8 Adc, I <sub>B1</sub> = 160 mAdc I <sub>B2</sub> = 160 mAdc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	—	4.2	—	—
Storage Time		t <sub>si</sub>	—	190	300	ns
Crossover Time		t <sub>c</sub>	—	350	—	—

TYPICAL STATIC CHARACTERISTICS

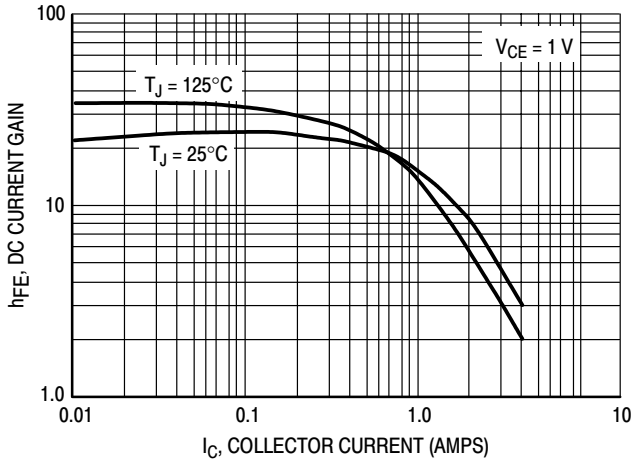


Figure 21. DC Current Gain at 1 Volt

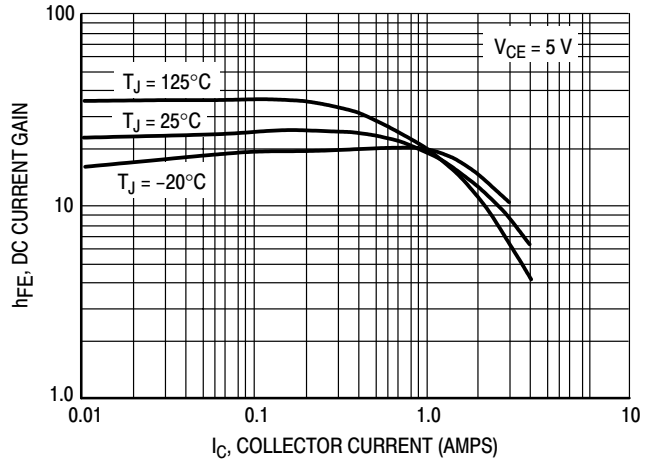


Figure 22. DC Current Gain at 5 Volts

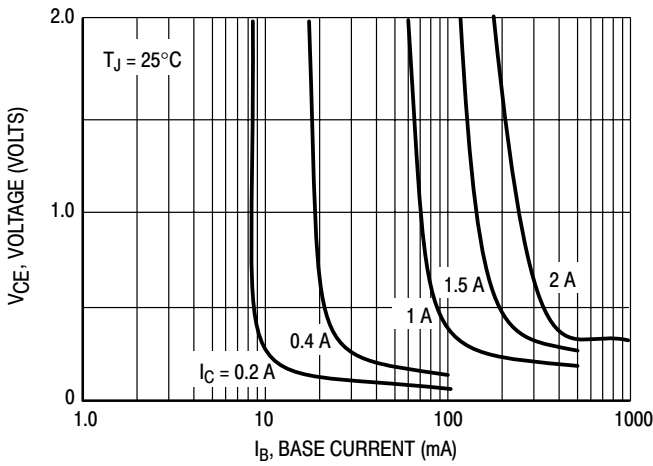


Figure 23. Collector Saturation Region

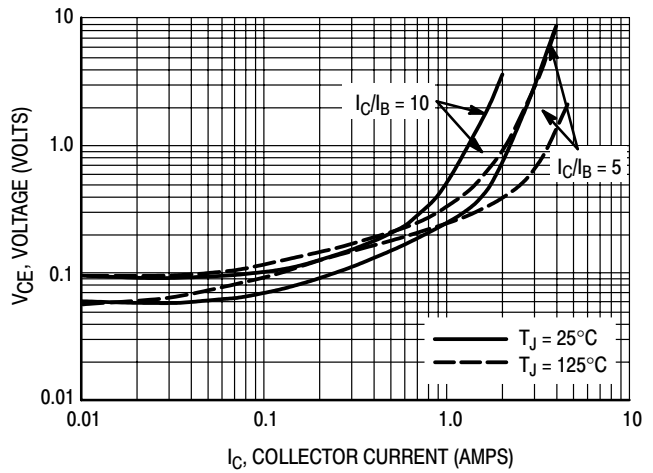


Figure 24. Collector-Emitter Saturation Voltage

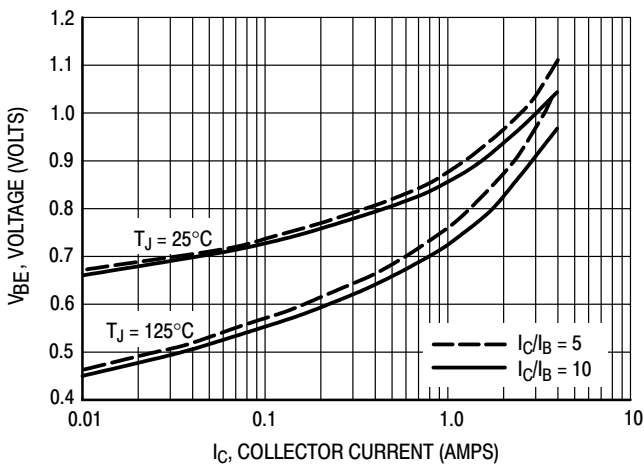


Figure 25. Base-Emitter Saturation Region

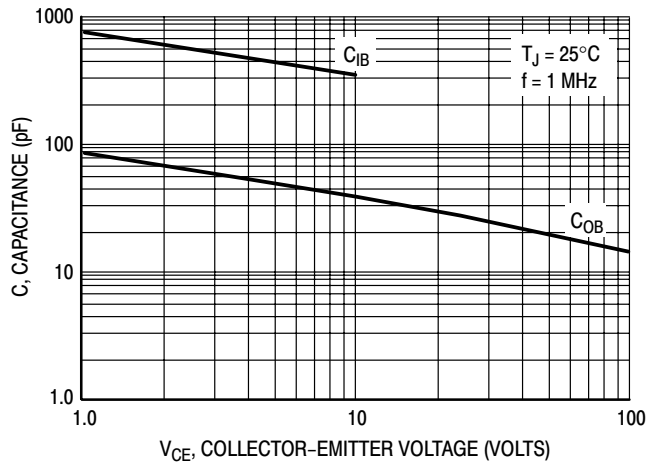


Figure 26. Capacitance

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

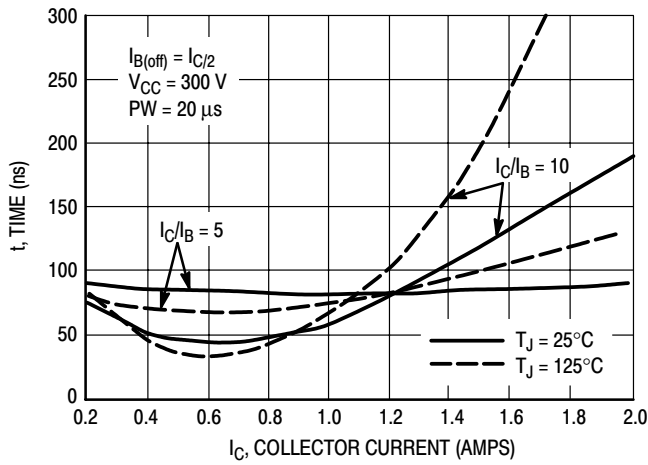


Figure 27. Resistive Switching,  $t_{on}$

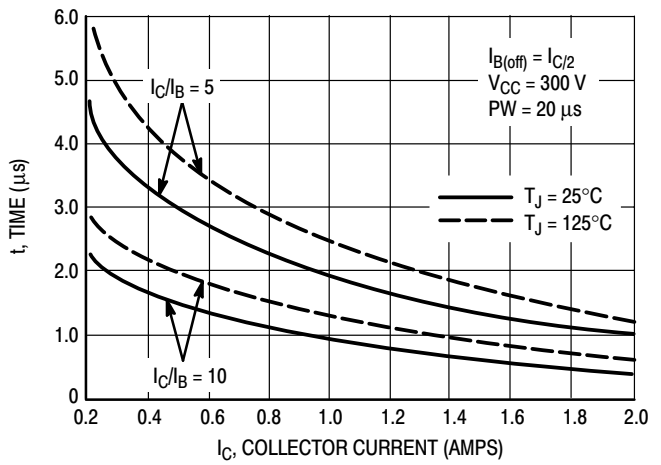


Figure 28. Resistive Switching,  $t_{off}$

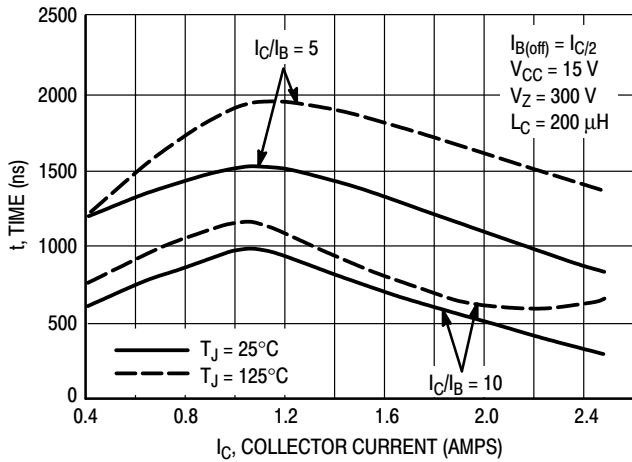


Figure 29. Inductive Storage Time,  $t_{si}$

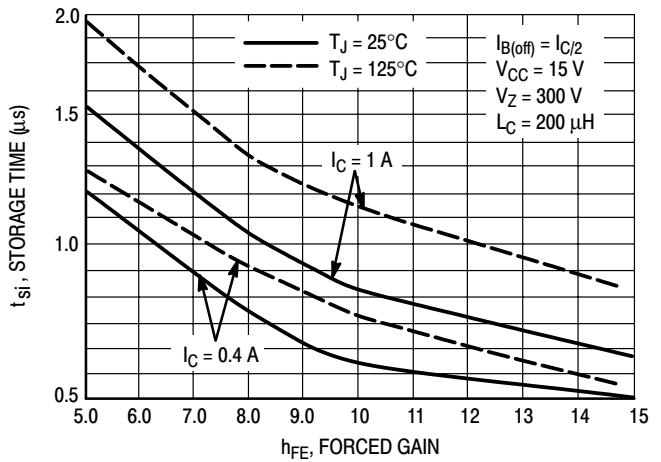


Figure 30. Inductive Storage Time

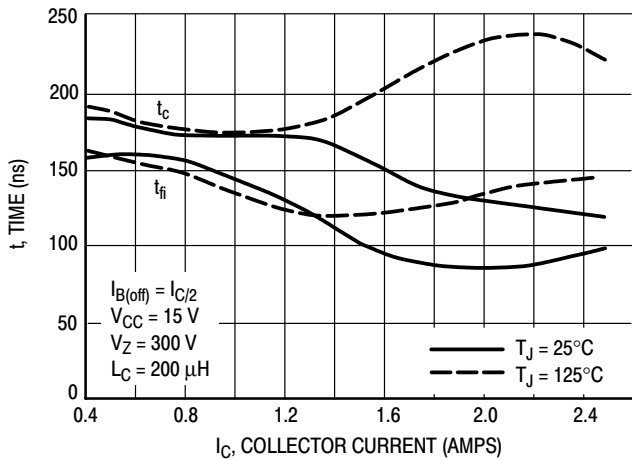


Figure 31. Inductive Switching,  $t_c$  and  $t_{fi}$   $I_C/I_B = 5$

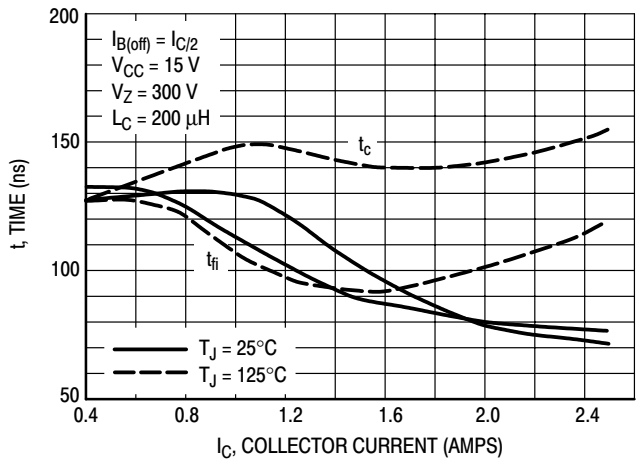


Figure 32. Inductive Switching,  $t_c$  and  $t_{fi}$   $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

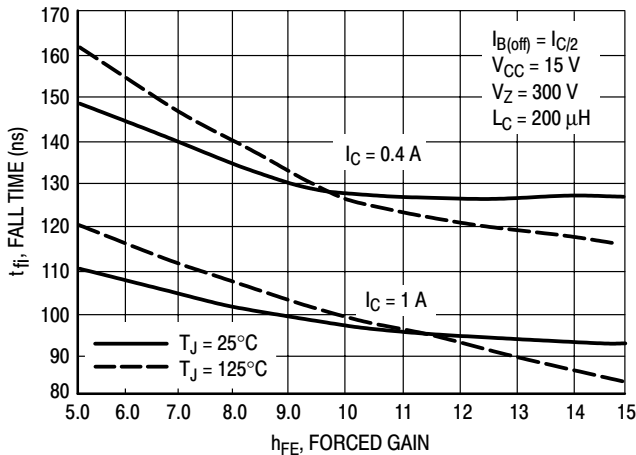


Figure 33. Inductive Fall Time

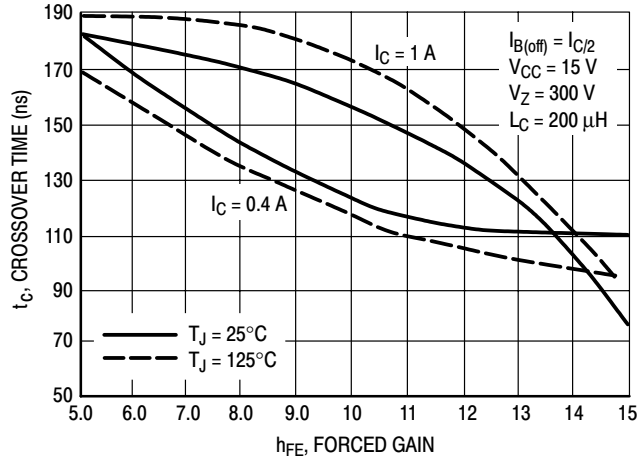


Figure 34. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

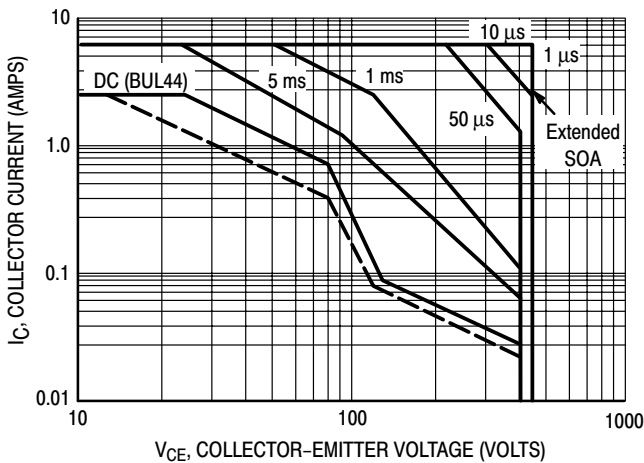


Figure 35. Forward Bias Safe Operating Area

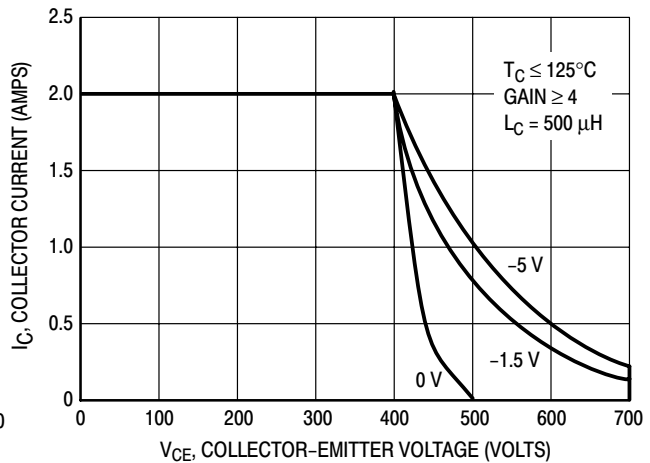


Figure 36. Reverse Bias Switching Safe Operating Area

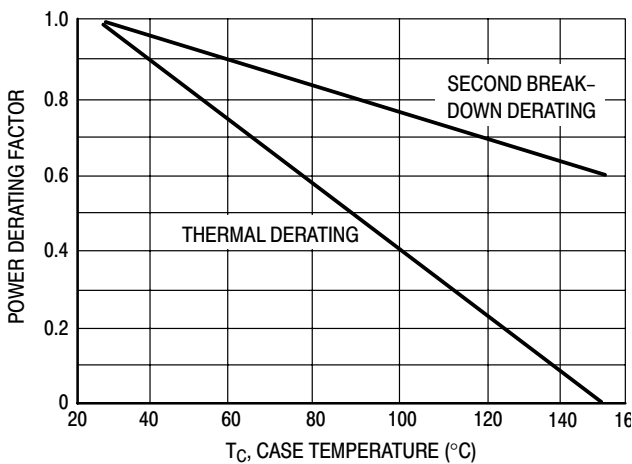


Figure 37. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$

limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 35 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(PK)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on figure 35 may be found at any case temperature by using the appropriate curve on figure 37.  $T_{J(PK)}$  may be calculated from the data in figure 40. At any case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse-biased. The safe level is specified as a reverse-biased safe operating area (Figure 36). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

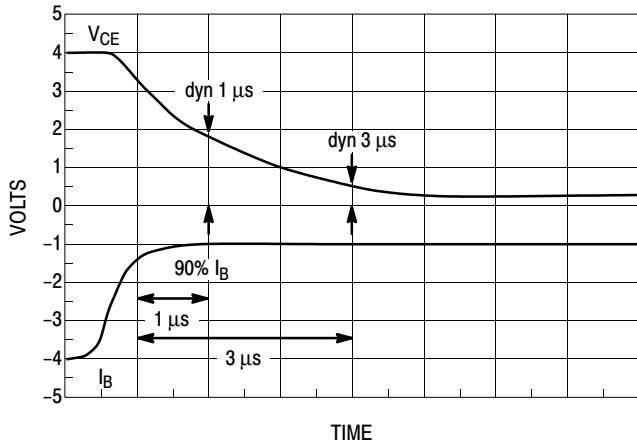


Figure 38. Dynamic Saturation Voltage Measurements

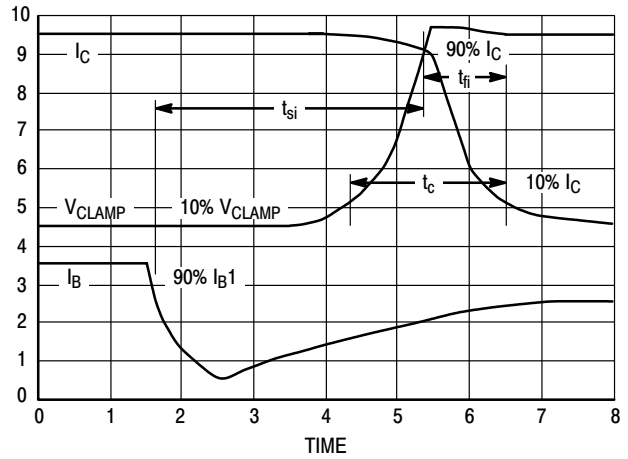
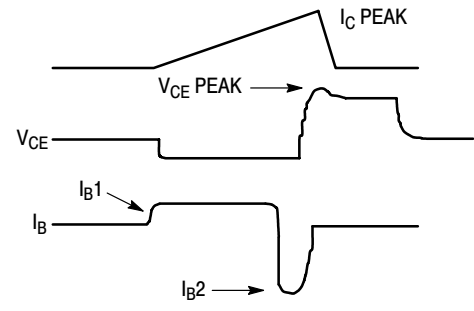
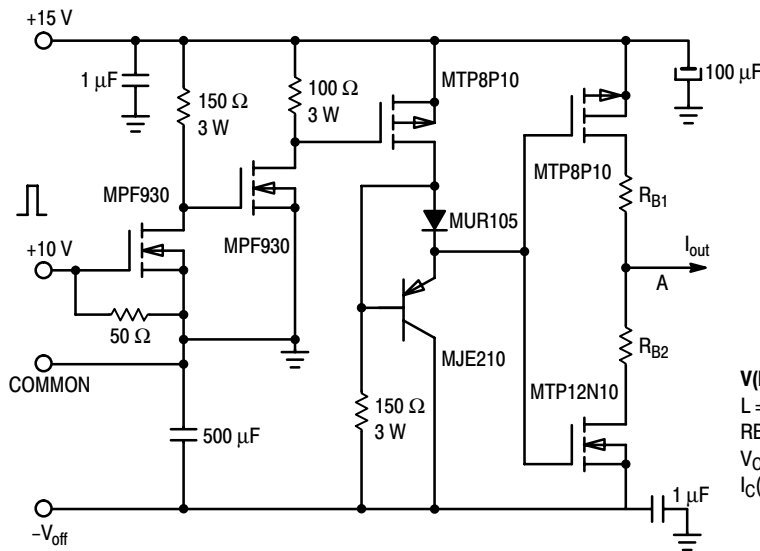


Figure 39. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
VCC = 20 VOLTS	VCC = 15 VOLTS	VCC = 15 VOLTS
IC(pk) = 100 mA	RB1 SELECTED FOR DESIRED IB1	RB1 SELECTED FOR DESIRED IB1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

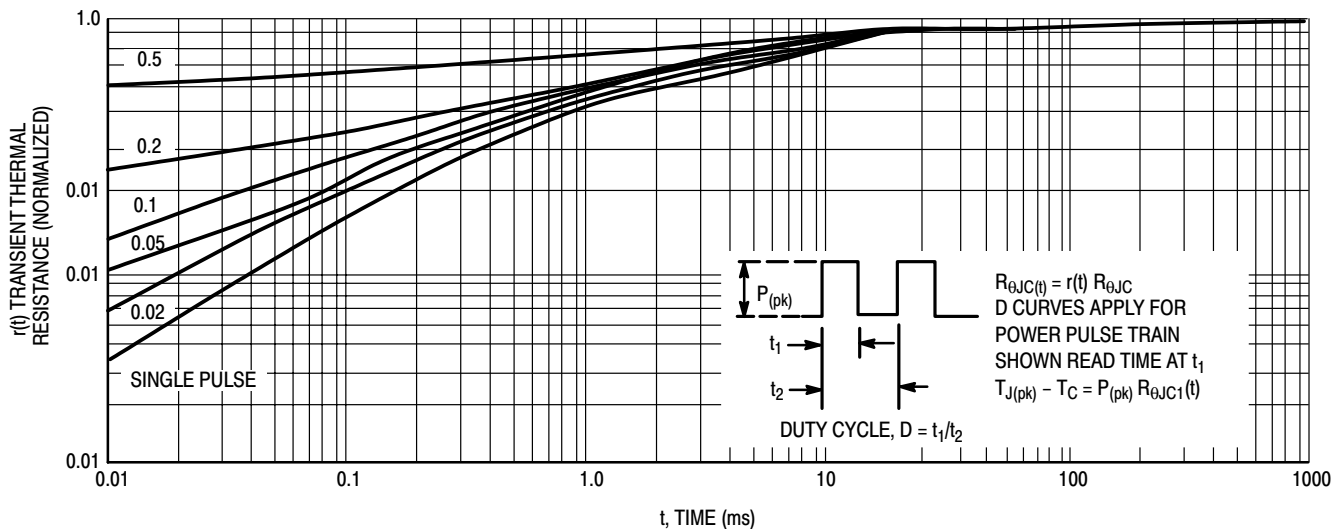


Figure 40. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for BUL44

# High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

The BUL45D2 is state-of-art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread ( $\pm 150$  ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an  $h_{FE}$  window.

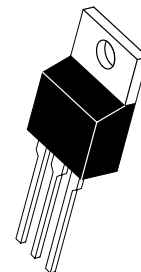
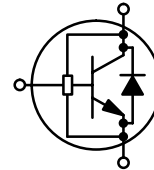
## Main features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @  $I_C = 100$  mA
- Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread
- Integrated Collector-Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic  $V_{CE(sat)}$
- "6 Sigma" Process Providing Tight and Reproducible Parameter Spreads

It's characteristics make it also suitable for PFC application.

## BUL45D2

POWER TRANSISTORS  
5 AMPERES  
700 VOLTS  
75 WATTS



CASE 221A-09  
TO-220AB

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	400	Vdc
Collector-Base Breakdown Voltage	$V_{CBO}$	700	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	700	Vdc
Emitter-Base Voltage	$V_{EBO}$	12	Vdc
Collector Current — Continuous — Peak (1)	$I_C$ $I_{CM}$	5 10	Adc
Base Current — Continuous — Peak (1)	$I_B$ $I_{BM}$	2 4	Adc
*Total Device Dissipation @ $T_C = 25^\circ\text{C}$ *Derate above $25^\circ\text{C}$	$P_D$	75 0.6	Watt W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from case for 5 seconds	$T_L$	260	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq 10\%$ .

# BUL45D2

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	400	450		Vdc
Collector–Base Breakdown Voltage ( $I_{CBO} = 1\text{ mA}$ )	$V_{CBO}$	700	910		Vdc
Emitter–Base Breakdown Voltage ( $I_{EBO} = 1\text{ mA}$ )	$V_{EBO}$	12	14.1		Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$			100	$\mu\text{A}$ dc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )  ( $V_{CE} = 500\text{ V}$ , $V_{EB} = 0$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$I_{CES}$		100 500 100	$\mu\text{A}$ dc
Emitter–Cutoff Current ( $V_{EB} = 10\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$			100	$\mu\text{A}$ dc

## ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 0.8\text{ Adc}$ , $I_B = 80\text{ mA}$ dc)	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{BE(sat)}$		0.8 0.7	1 0.9	Vdc	
	( $I_C = 2\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		0.89 0.79		1 0.9
Collector–Emitter Saturation Voltage ( $I_C = 0.8\text{ Adc}$ , $I_B = 80\text{ mA}$ dc)	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(sat)}$		0.28 0.32	0.4 0.5	Vdc	
	( $I_C = 2\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		0.32 0.38		0.5 0.6
	( $I_C = 0.8\text{ Adc}$ , $I_B = 40\text{ mA}$ dc)		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		0.46 0.62		0.75 1
DC Current Gain ( $I_C = 0.8\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$h_{FE}$	22 20	34 29		—	
	( $I_C = 2\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	10 7	14 9.5		

## DIODE CHARACTERISTICS

Forward Diode Voltage ( $I_{EC} = 1\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{EC}$		1.04 0.7	1.5	V
	( $I_{EC} = 2\text{ Adc}$ )		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		1.2 1.6	
	( $I_{EC} = 0.4\text{ Adc}$ )		@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		0.85 0.62	
Forward Recovery Time (see Figure 27) ( $I_F = 1\text{ Adc}$ , $di/dt = 10\text{ A}/\mu\text{s}$ )	@ $T_C = 25^\circ\text{C}$	$T_{fr}$		330		ns
	( $I_F = 2\text{ Adc}$ , $di/dt = 10\text{ A}/\mu\text{s}$ )		@ $T_C = 25^\circ\text{C}$		360	
	( $I_F = 0.4\text{ Adc}$ , $di/dt = 10\text{ A}/\mu\text{s}$ )		@ $T_C = 25^\circ\text{C}$		320	



# BUL45D2

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>DYNAMIC CHARACTERISTICS</b>					
Current Gain Bandwidth (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1 MHz)	f <sub>T</sub>		13		MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1 MHz)	C <sub>ob</sub>		50	75	pF
Input Capacitance (V <sub>EB</sub> = 8 Vdc)	C <sub>ib</sub>		340	500	pF

## DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I <sub>B1</sub> reaches 90% of final I <sub>B1</sub>	I <sub>C</sub> = 1 A I <sub>B1</sub> = 100 mA V <sub>CC</sub> = 300 V	@ 1 μs	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	V <sub>CE(dsat)</sub>		3.7 9.4		V
		@ 3 μs	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C			0.35 2.7		V
	I <sub>C</sub> = 2 A I <sub>B1</sub> = 0.8 A V <sub>CC</sub> = 300 V	@ 1 μs	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C			3.9 12		V
		@ 3 μs	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C			0.4 1.5		V

## SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn-on Time	I <sub>C</sub> = 2 Adc, I <sub>B1</sub> = 0.4 Adc I <sub>B2</sub> = 1 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>on</sub>		90 105	150	ns
Turn-off Time		@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>off</sub>		1.15 1.5	1.3	μs
Turn-on Time	I <sub>C</sub> = 2 Adc, I <sub>B1</sub> = 0.4 Adc I <sub>B2</sub> = 0.4 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>on</sub>		90 110	150	ns
Turn-off Time		@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>off</sub>	2.1	3.1	2.4	μs

## SWITCHING CHARACTERISTICS: Inductive Load (V<sub>clamp</sub> = 300 V, V<sub>CC</sub> = 15 V, L = 200 μH)

Fall Time	I <sub>C</sub> = 1 Adc I <sub>B1</sub> = 100 mA I <sub>B2</sub> = 500 mA	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>f</sub>		90 93	150	ns
Storage Time		@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>s</sub>		0.72 1.05	0.9	μs
Crossover Time		@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>c</sub>		95 95	150	ns
Fall Time	I <sub>C</sub> = 2 Adc I <sub>B1</sub> = 0.4 Adc I <sub>B2</sub> = 0.4 Adc	@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>f</sub>		80 105	150	ns
Storage Time		@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>s</sub>	1.95	2.9	2.25	μs
Crossover Time		@ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 125°C	t <sub>c</sub>		225 450	300	ns

TYPICAL STATIC CHARACTERISTICS

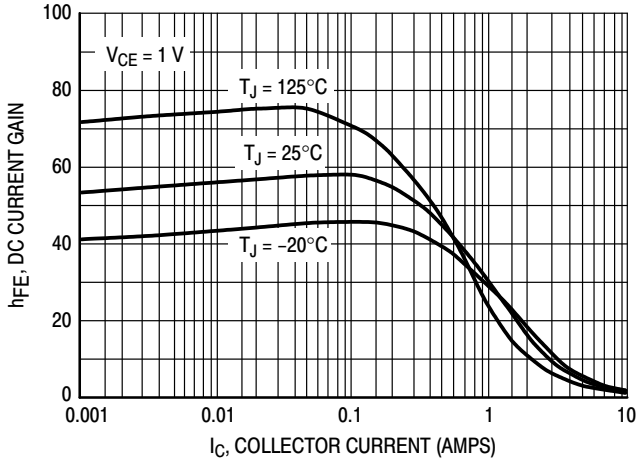


Figure 41. DC Current Gain @ 1 Volt

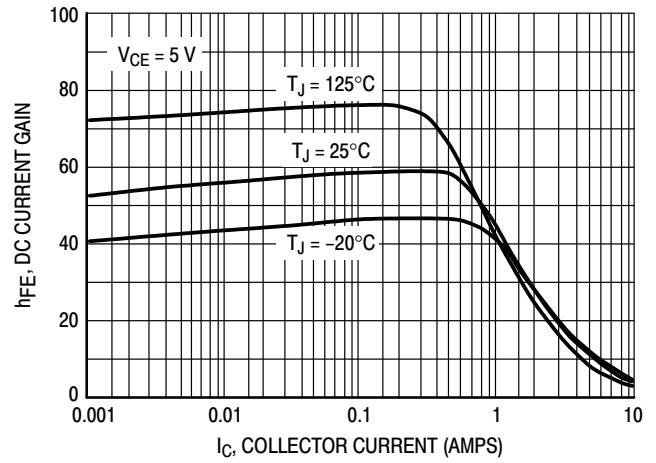


Figure 42. DC Current Gain @ 5 Volt

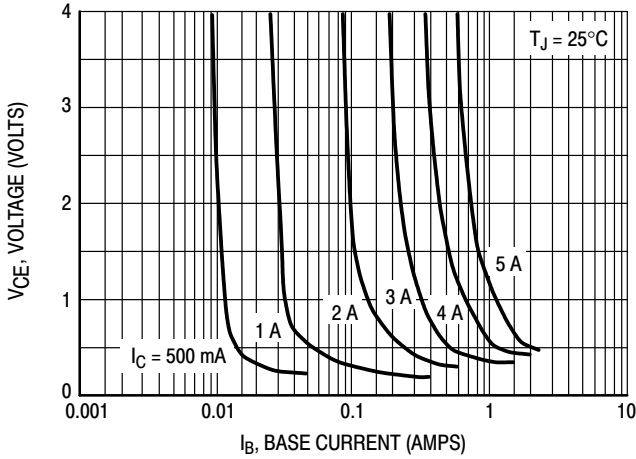


Figure 43. Collector Saturation Region

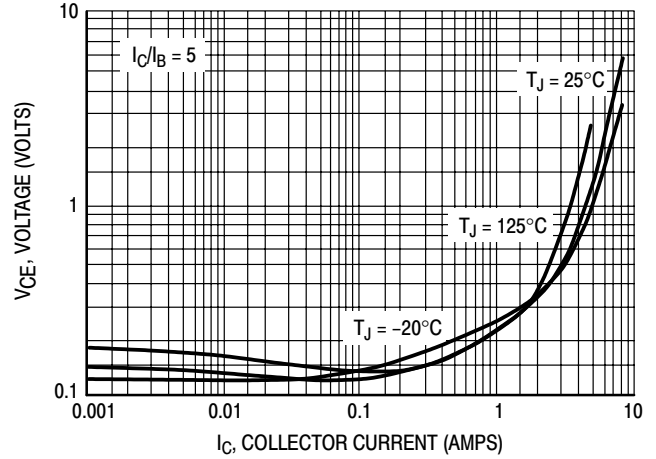


Figure 44. Collector-Emitter Saturation Voltage

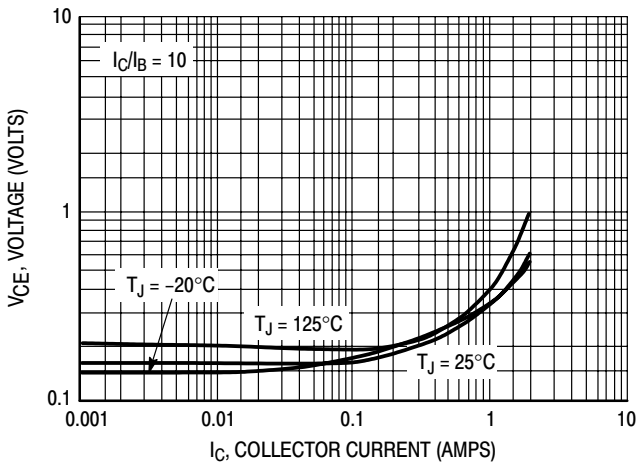


Figure 45. Collector-Emitter Saturation Voltage

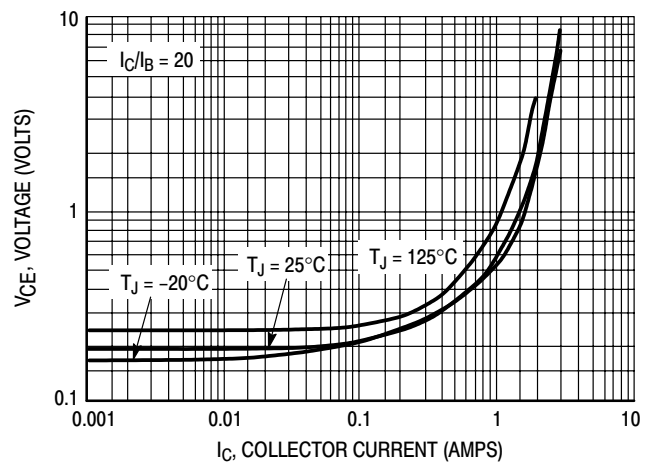


Figure 46. Collector-Emitter Saturation Voltage

# BUL45D2

## TYPICAL STATIC CHARACTERISTICS

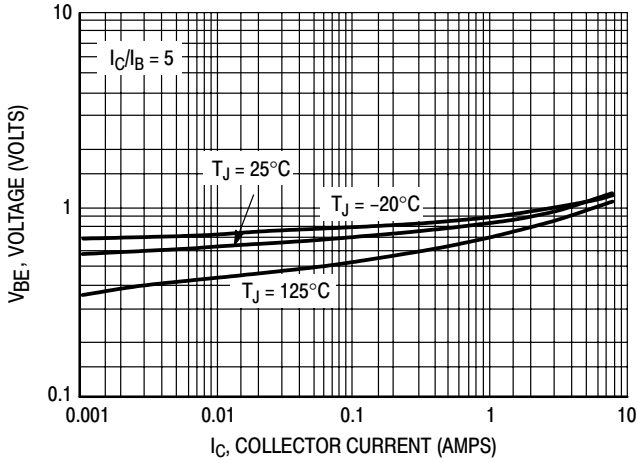


Figure 47. Base-Emitter Saturation Region

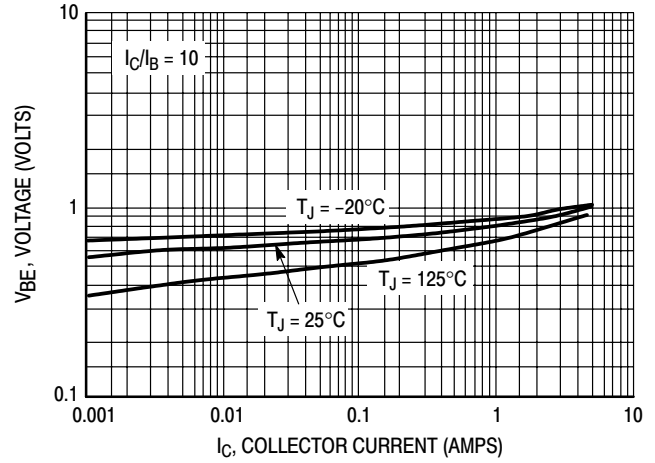


Figure 48. Base-Emitter Saturation Region

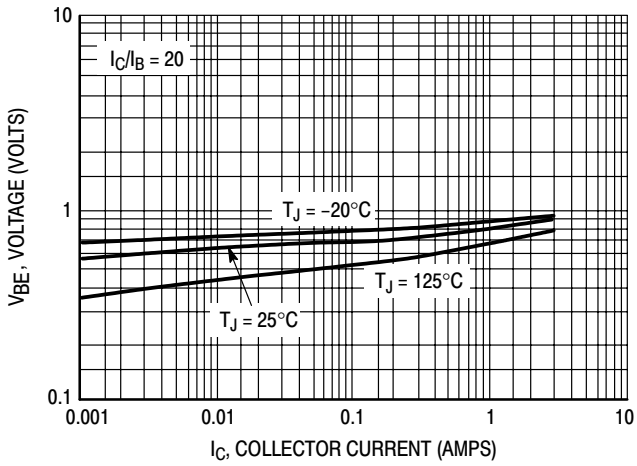


Figure 49. Base-Emitter Saturation Region

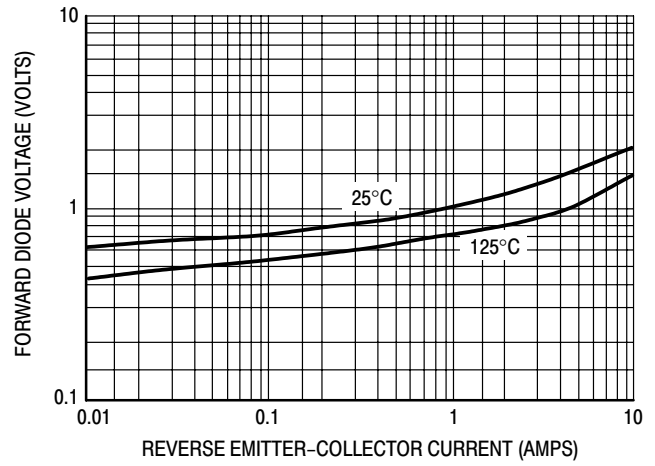


Figure 50. Forward Diode Voltage

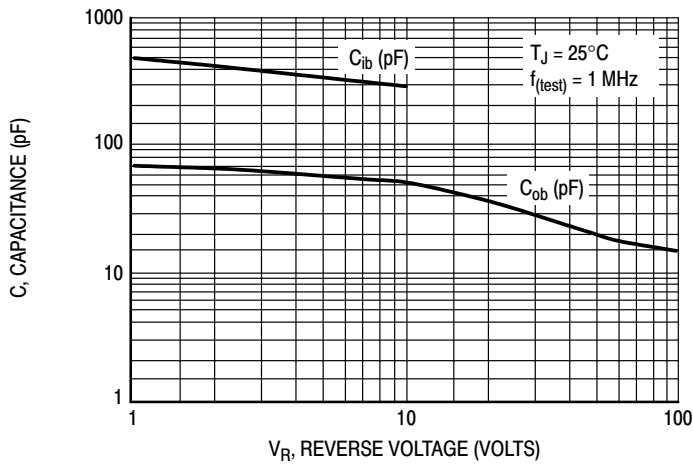


Figure 51. Capacitance

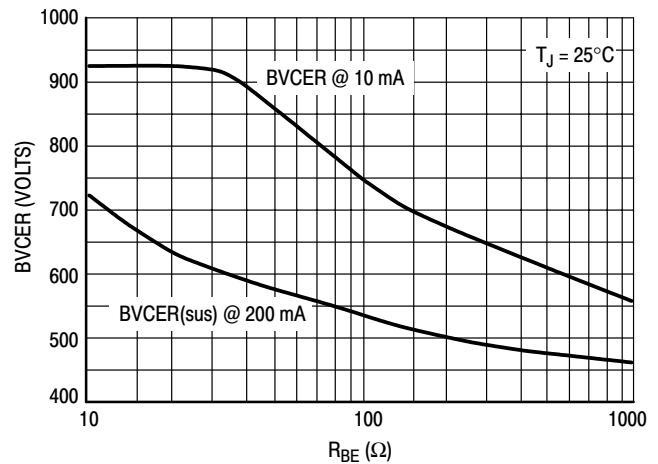


Figure 52. BVCEr = f(ICER)

TYPICAL SWITCHING CHARACTERISTICS

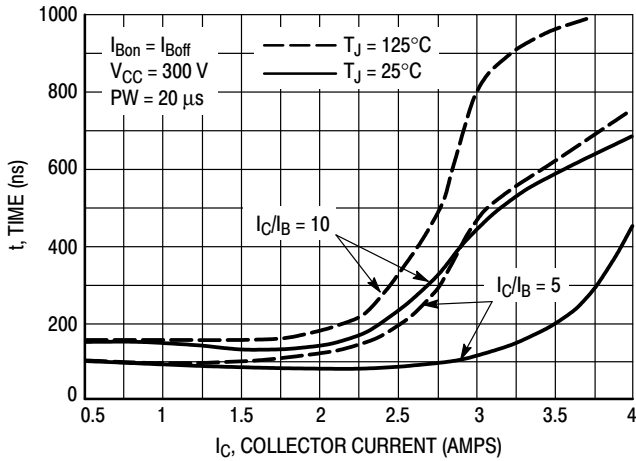


Figure 53. Resistive Switch Time,  $t_{on}$

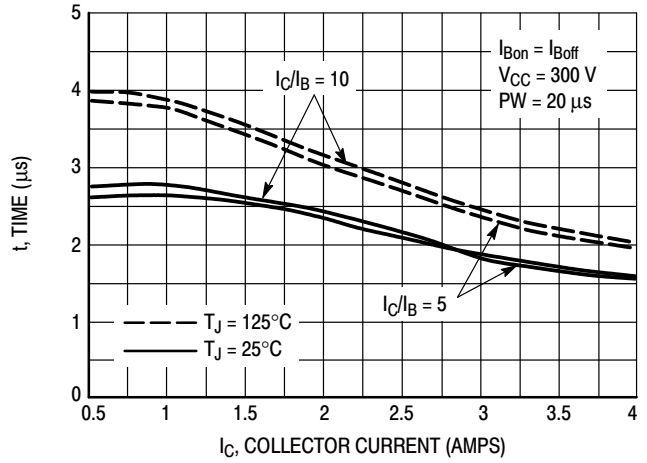


Figure 54. Resistive Switch Time,  $t_{off}$

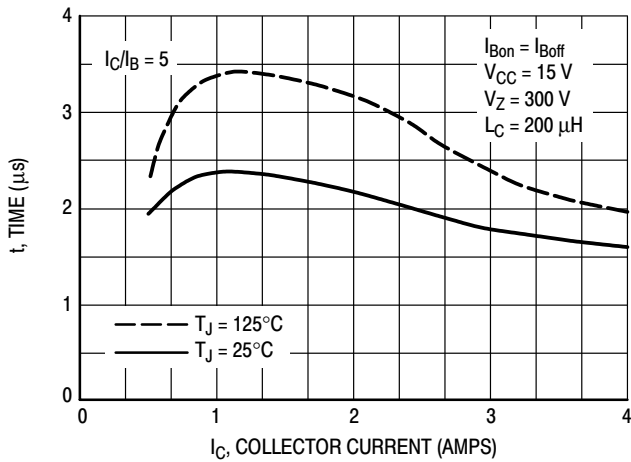


Figure 55. Inductive Storage Time,  $t_{si}$  @  $I_C/I_B = 5$

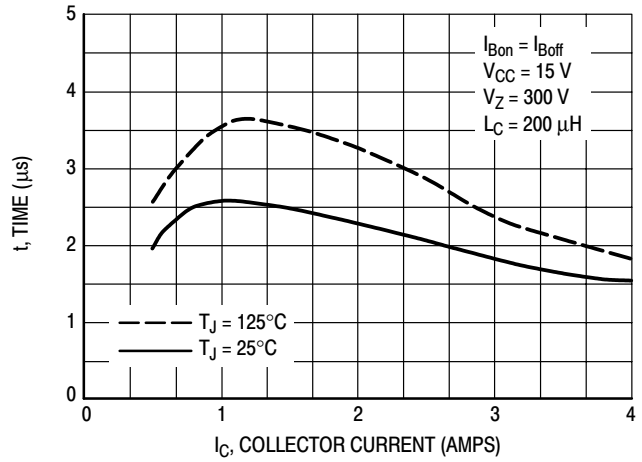


Figure 56. Inductive Storage Time,  $t_{si}$  @  $I_C/I_B = 10$

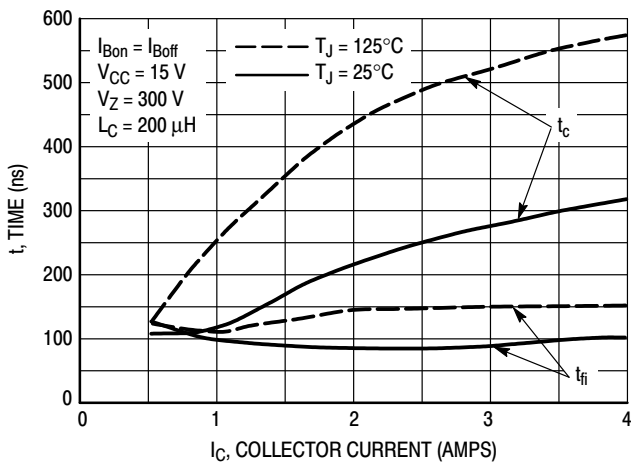


Figure 57. Inductive Switching,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 5$

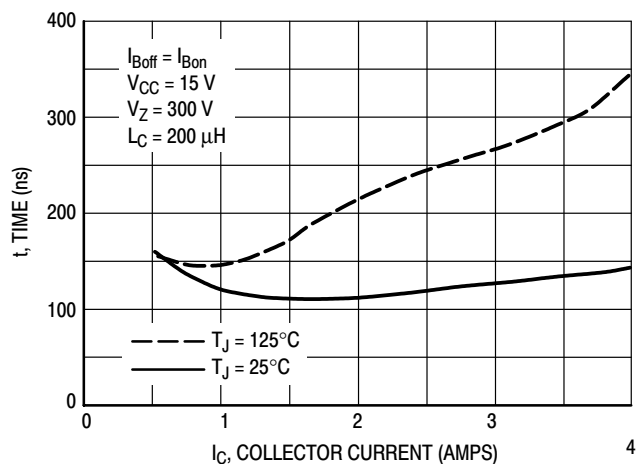


Figure 58. Inductive Switching,  $t_{fi}$  @  $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS

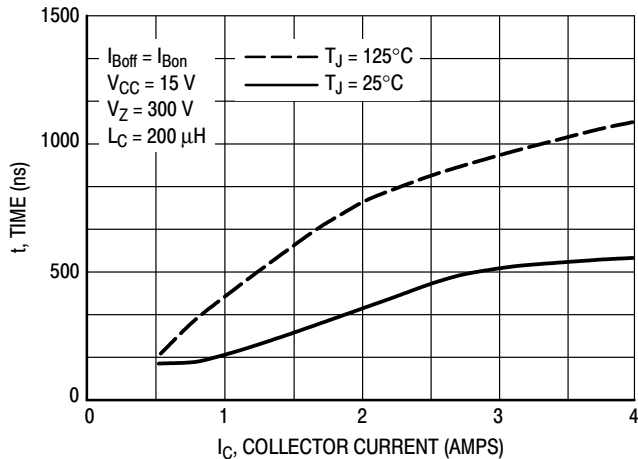


Figure 59. Inductive Switching,  $t_c$  @  $I_C/I_B = 10$

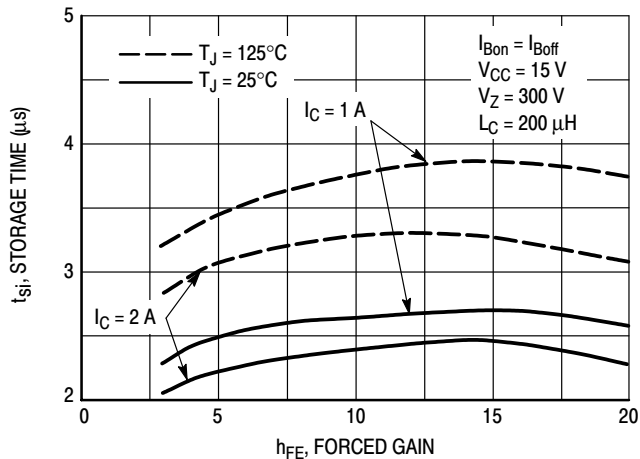


Figure 60. Inductive Storage Time

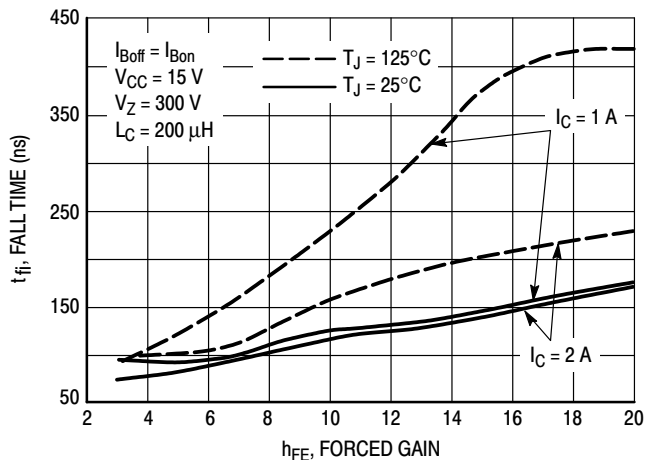


Figure 61. Inductive Fall Time

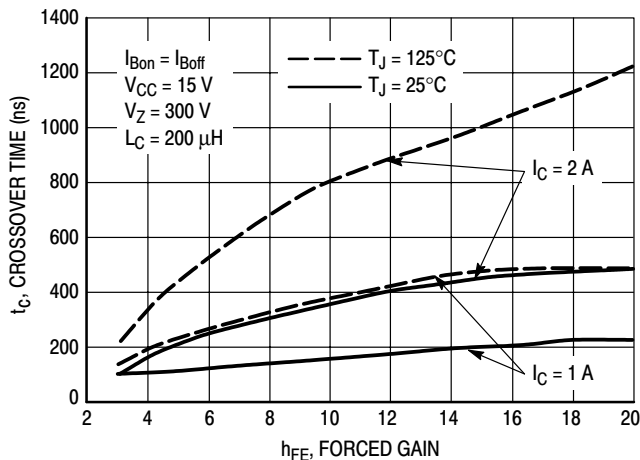


Figure 62. Inductive Crossover Time

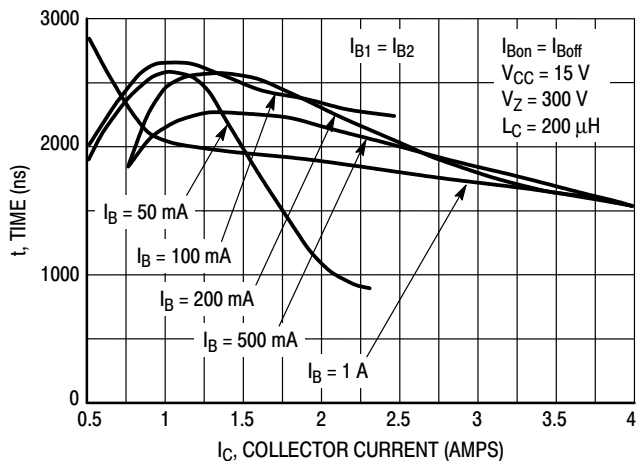


Figure 63. Inductive Storage Time,  $t_{si}$

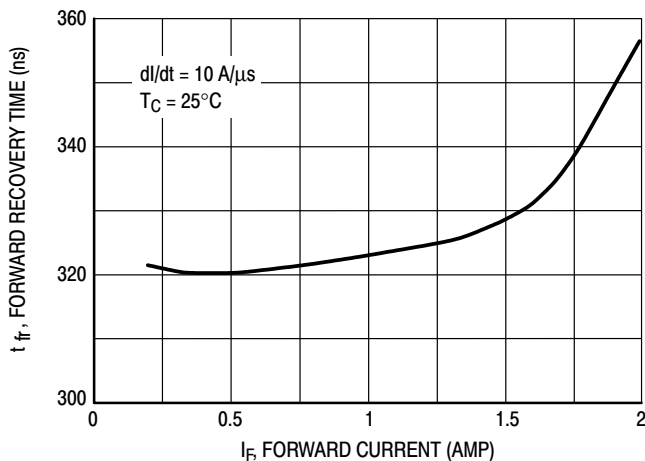


Figure 64. Forward Recovery Time  $t_{fr}$

TYPICAL SWITCHING CHARACTERISTICS

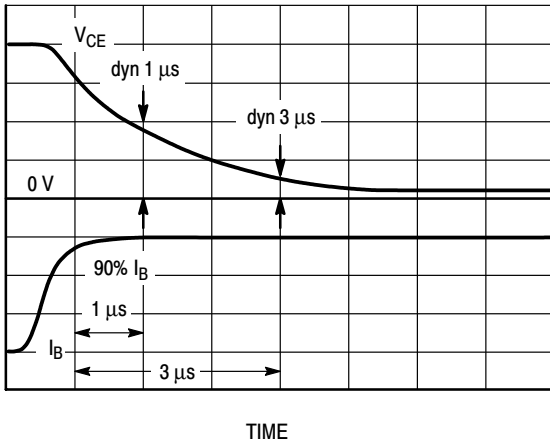


Figure 65. Dynamic Saturation Voltage Measurements

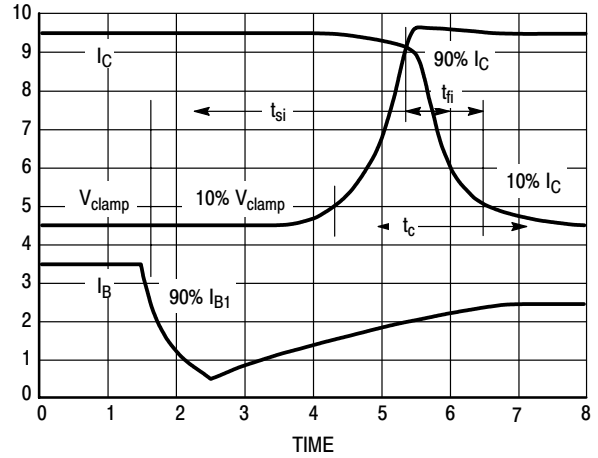


Figure 66. Inductive Switching Measurements

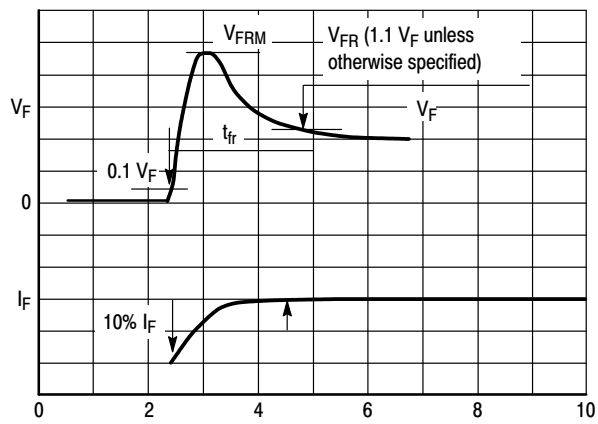
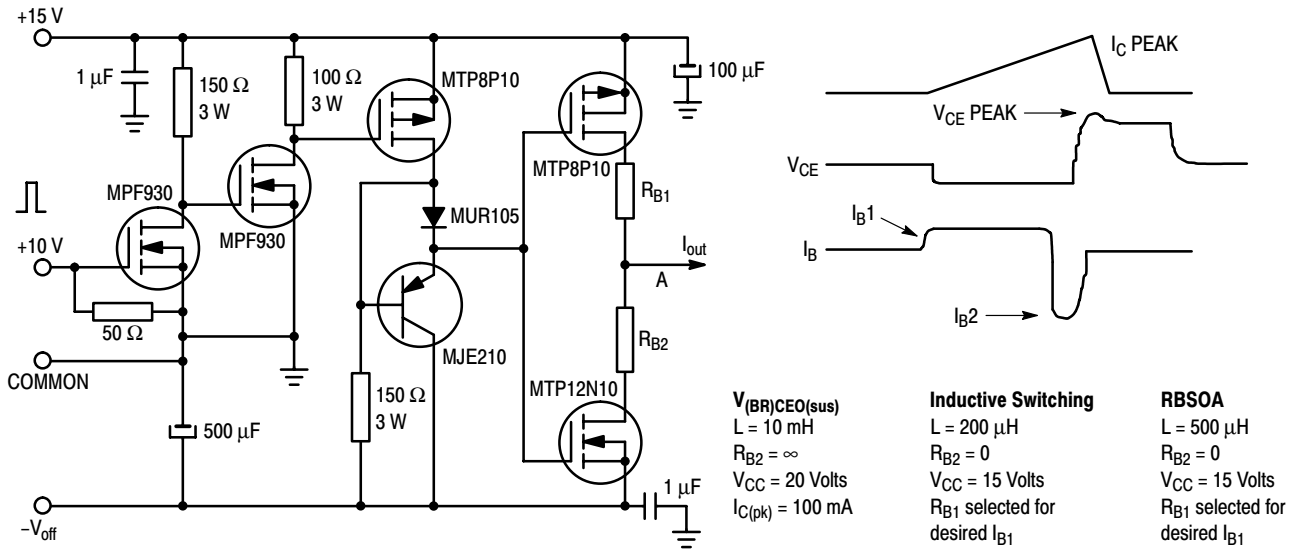


Figure 67.  $t_{fr}$  Measurements

# BUL45D2

## TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



## TYPICAL CHARACTERISTICS

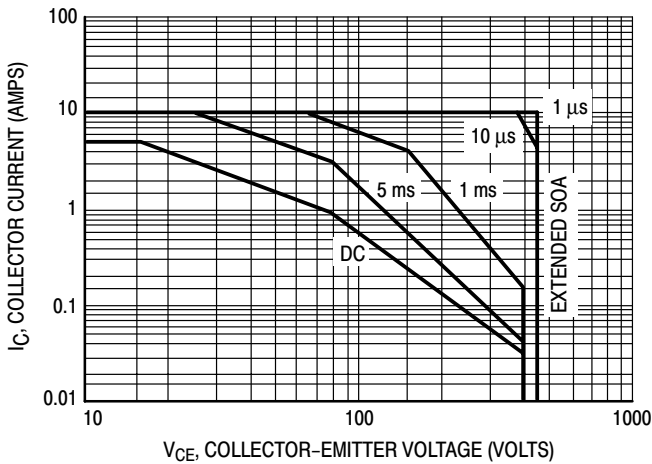


Figure 68. Forward Bias Safe Operating Area

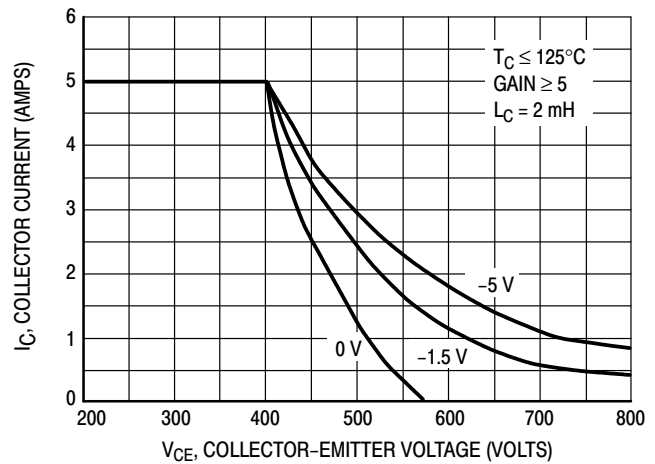


Figure 69. Reverse Bias Safe Operating Area

# BUL45D2

## TYPICAL CHARACTERISTICS

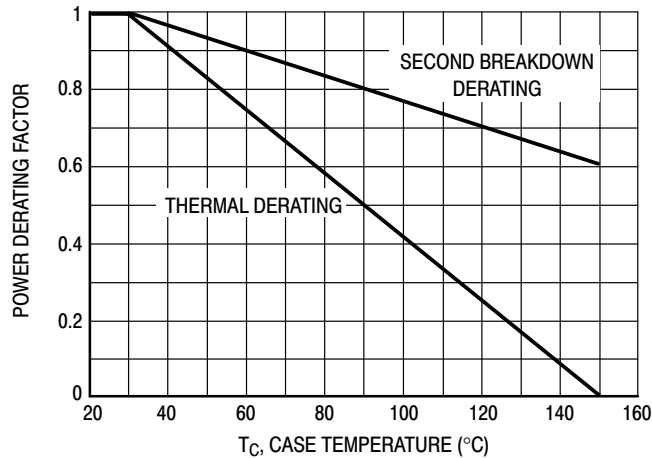


Figure 70. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C-V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 68 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 68 may be found at any case temperature by using the appropriate curve on Figure 70.

$T_{J(pk)}$  may be calculated from the data in Figure 71. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 69). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

## TYPICAL THERMAL RESPONSE

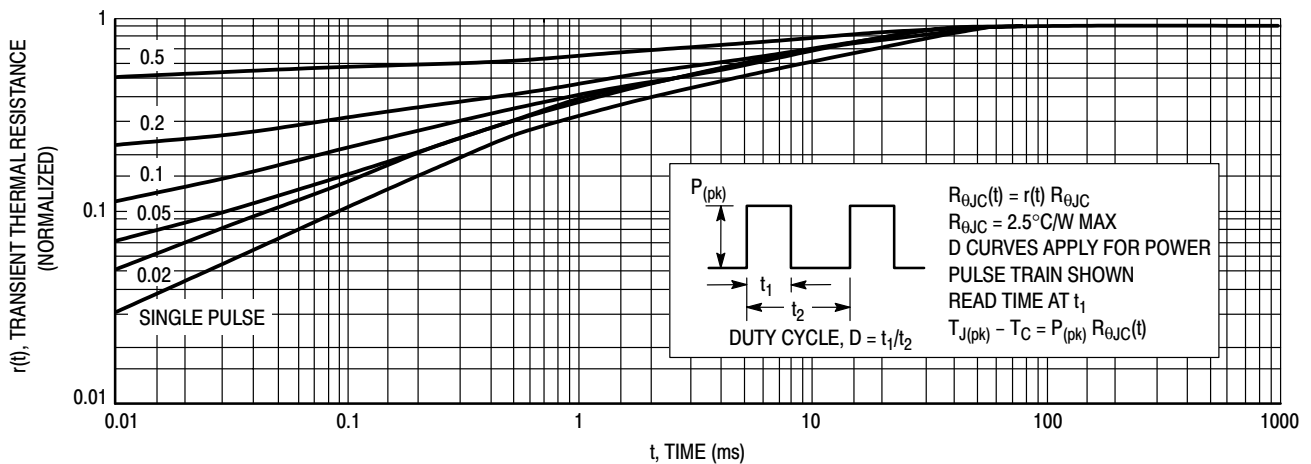


Figure 71. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for BUL45D2



# NPN Silicon Power Transistor

## High Voltage SWITCHMODE™ Series

Designed for use in electronic ballast (light ballast) and in Switchmode Power supplies up to 50 Watts. Main features include:

- Improved Efficiency Due to:
  - Low Base Drive Requirements (High and Flat DC Current Gain  $h_{FE}$ )
  - Low Power Losses (On-State and Switching Operations)
  - Fast Switching:  $t_{fi} = 100$  ns (typ) and  $t_{si} = 3.2$   $\mu$ s (typ)
  - @  $I_C = 2.0$  A,  $I_{B1} = I_{B2} = 0.4$  A
- Full Characterization at 125°C
- Tight Parametric Distributions Consistent Lot-to-Lot

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	$V_{CEO}$	400	Vdc
Collector–Emitter Breakdown Voltage	$V_{CES}$	700	Vdc
Emitter–Base Voltage	$V_{EBO}$	9.0	Vdc
Collector Current — Continuous	$I_C$	5.0	Adc
— Peak(1)	$I_{CM}$	10	
Base Current	$I_B$	2.0	Adc
Total Device Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_D$	75	Watts
Derate above 25°C		0.6	W/°C
Operating and Storage Temperature	$T_J, T_{stg}$	– 65 to 150	°C

### THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.65	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

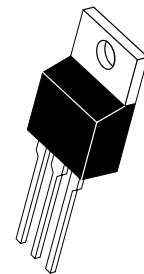
### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100$ mA, $L = 25$ mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}, I_B = 0$ )	$I_{CEO}$	—	—	100	$\mu$ Adc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}, V_{EB} = 0$ )	$I_{CES}$	—	—	10	$\mu$ Adc
				100	
Emitter Cutoff Current ( $V_{EB} = 9.0$ Vdc, $I_C = 0$ )	$I_{EBO}$	—	—	100	$\mu$ Adc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle  $\leq$  10%.

# BUL45

**POWER TRANSISTOR**  
**5.0 AMPERES**  
**700 VOLTS**  
**35 and 75 WATTS**



**BUL45**  
**CASE 221A-06**  
**TO-220AB**

# BUL45

## ELECTRICAL CHARACTERISTICS — continued (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b>					
Base–Emitter Saturation Voltage (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.2 Adc) (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 0.4 Adc)	V <sub>BE(sat)</sub>	— —	0.84 0.89	1.2 1.25	Vdc
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.2 Adc)  (T <sub>C</sub> = 125°C)	V <sub>CE(sat)</sub>	— —	0.175 0.150	0.25 —	Vdc
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 0.4 Adc)  (T <sub>C</sub> = 125°C)	V <sub>CE(sat)</sub>	— —	0.25 0.275	0.4 —	Vdc
DC Current Gain (I <sub>C</sub> = 0.3 Adc, V <sub>CE</sub> = 5.0 Vdc)  (I <sub>C</sub> = 2.0 Adc, V <sub>CE</sub> = 1.0 Vdc)  (I <sub>C</sub> = 10 mAdc, V <sub>CE</sub> = 5.0 Vdc)  (T <sub>C</sub> = 125°C)	h <sub>FE</sub>	14 — 7.0 5.0 10	— 32 14 12 22	34 — — — —	—

## DYNAMIC CHARACTERISTICS

Current Gain Bandwidth (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1.0 MHz)				f <sub>T</sub>	—	12	—	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1.0 MHz)				C <sub>ob</sub>	—	50	75	pF
Input Capacitance (V <sub>EB</sub> = 8.0 Vdc)				C <sub>ib</sub>	—	920	1200	pF
Dynamic Saturation Voltage:  Determined 1.0 μs and 3.0 μs respectively after rising I <sub>B1</sub> reaches 90% of final I <sub>B1</sub> (see Figure 18)	(I <sub>C</sub> = 1.0 Adc I <sub>B1</sub> = 100 mAdc V <sub>CC</sub> = 300 V)	1.0 μs	(T <sub>C</sub> = 125°C)	V <sub>CE</sub> (Dyn sat)	—	1.75	—	Vdc
		3.0 μs	(T <sub>C</sub> = 125°C)		—	0.5 1.0	— —	
	(I <sub>C</sub> = 2.0 Adc I <sub>B1</sub> = 400 mAdc V <sub>CC</sub> = 300 V)	1.0 μs	(T <sub>C</sub> = 125°C)		—	1.85 6.0	— —	
		3.0 μs	(T <sub>C</sub> = 125°C)		—	0.5 1.0	— —	

# BUL45

## SWITCHING CHARACTERISTICS: Resistive Load

Turn-On Time	(I <sub>C</sub> = 2.0 Adc, I <sub>B1</sub> = I <sub>B2</sub> = 0.4 Adc Pulse Width = 20 μs, Duty Cycle < 20% V <sub>CC</sub> = 300 V) (T <sub>C</sub> = 125°C)	t <sub>on</sub>	— —	75 120	110 —	ns
Turn-Off Time		t <sub>off</sub>	— —	2.8 3.5	3.5 —	μs

## SWITCHING CHARACTERISTICS: Inductive Load (V<sub>CC</sub> = 15 Vdc, L<sub>C</sub> = 200 μH, V<sub>clamp</sub> = 300 Vdc)

Fall Time	(I <sub>C</sub> = 2.0 Adc, I <sub>B1</sub> = 0.4 Adc I <sub>B2</sub> = 0.4 Adc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	70 —	— 200	170 —	ns
Storage Time		t <sub>si</sub>	2.6 —	— 4.2	3.8 —	μs
Crossover Time		t <sub>c</sub>	— —	230 400	350 —	ns
Fall Time	(I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = 100 mAdc I <sub>B2</sub> = 0.5 Adc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	— —	110 100	150 —	ns
Storage Time		t <sub>si</sub>	— —	1.1 1.5	1.7 —	μs
Crossover Time		t <sub>c</sub>	— —	170 170	250 —	ns
Fall Time	(I <sub>C</sub> = 2.0 Adc, I <sub>B1</sub> = 250 mAdc I <sub>B2</sub> = 2.0 Adc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	—	80	120	ns
Storage Time		t <sub>si</sub>	—	0.6	0.9	μs
Crossover Time		t <sub>c</sub>	—	175	300	ns

TYPICAL STATIC CHARACTERISTICS

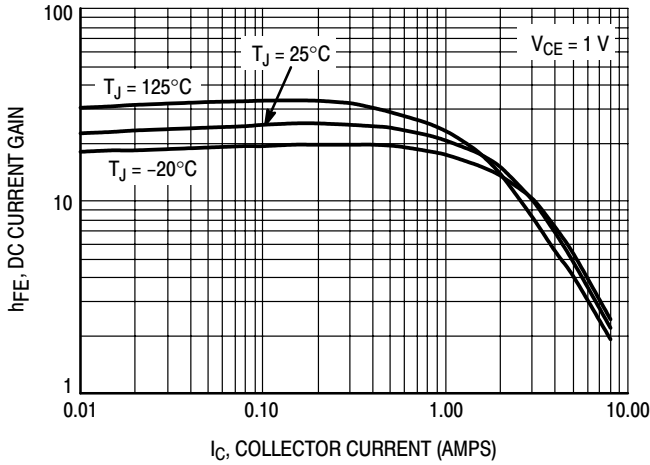


Figure 1. DC Current Gain @ 1 Volt

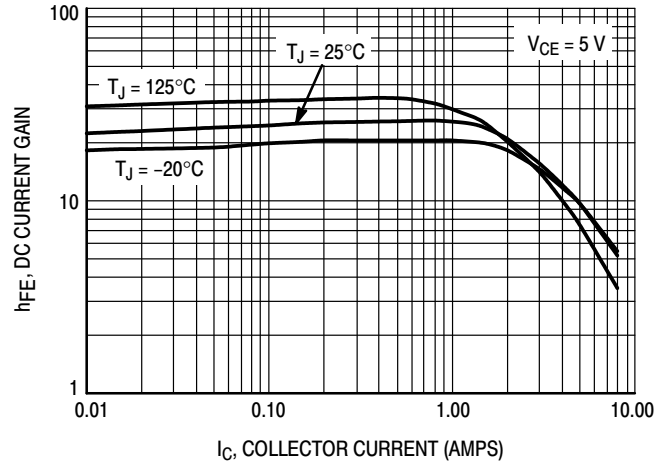


Figure 2. DC Current Gain at @ 5 Volts

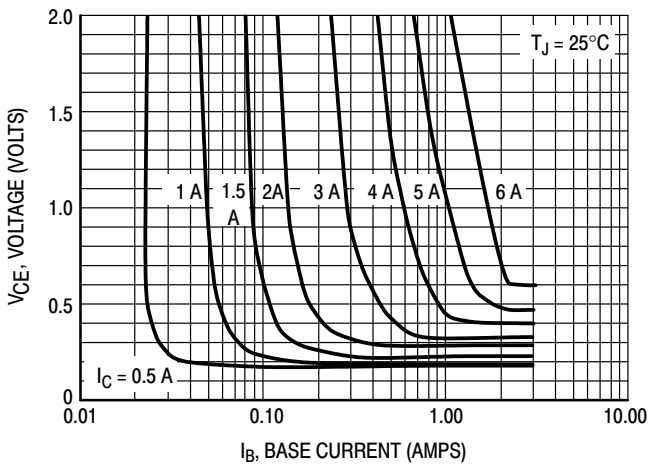


Figure 3. Collector-Emitter Saturation Region

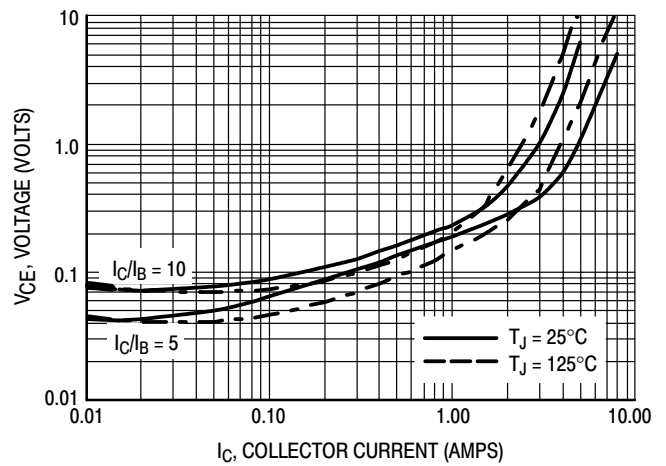


Figure 4. Collector-Emitter Saturation Voltage

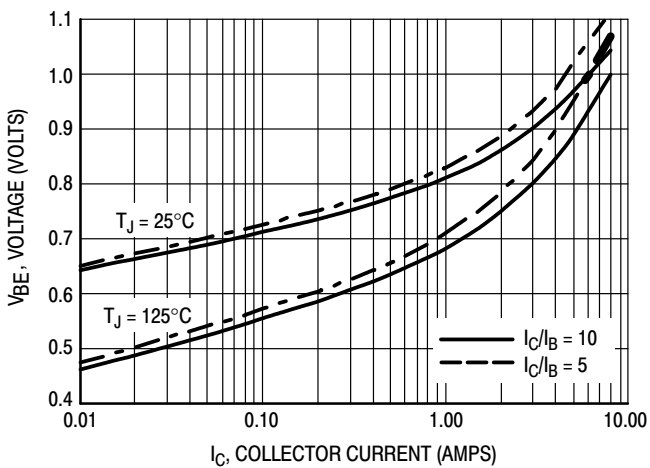


Figure 5. Base-Emitter Saturation Region

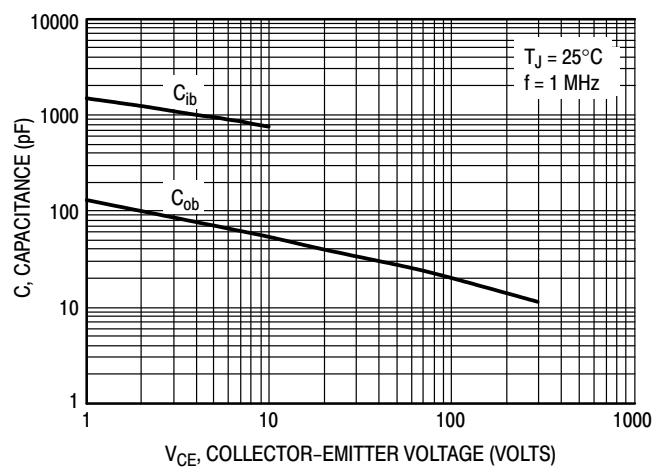


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

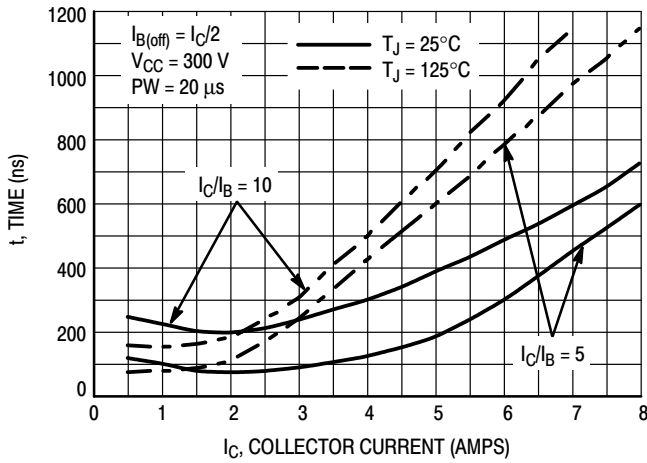


Figure 7. Resistive Switching,  $t_{on}$

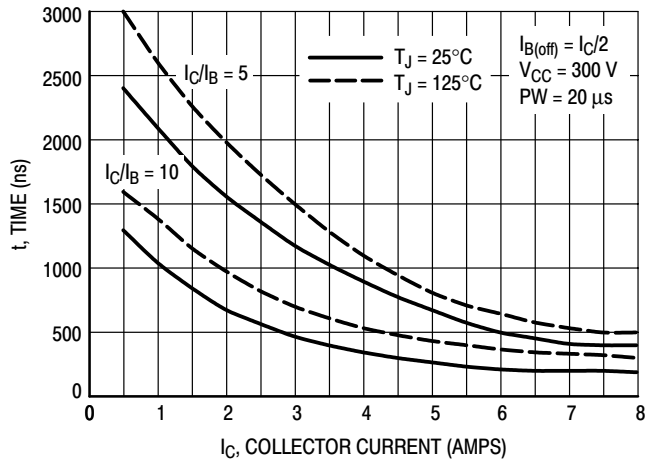


Figure 8. Resistive Switching,  $t_{off}$

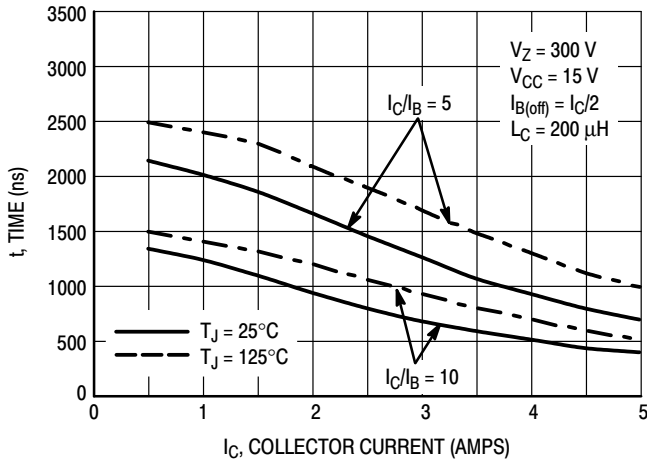


Figure 9. Inductive Storage Time,  $t_{si}$

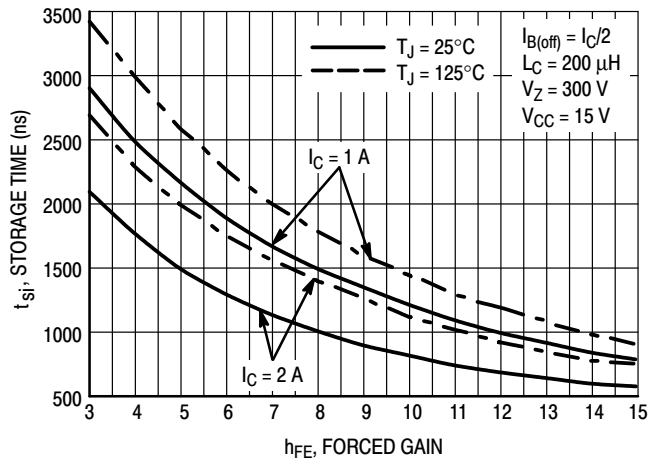


Figure 10. Inductive Storage Time,  $t_{si}(h_{FE})$

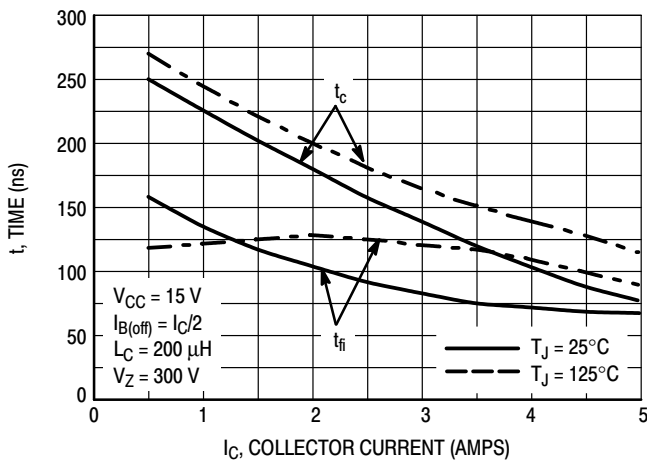


Figure 11. Inductive Switching,  $t_c$  &  $t_{fi}$ ,  $I_C/I_B = 5$

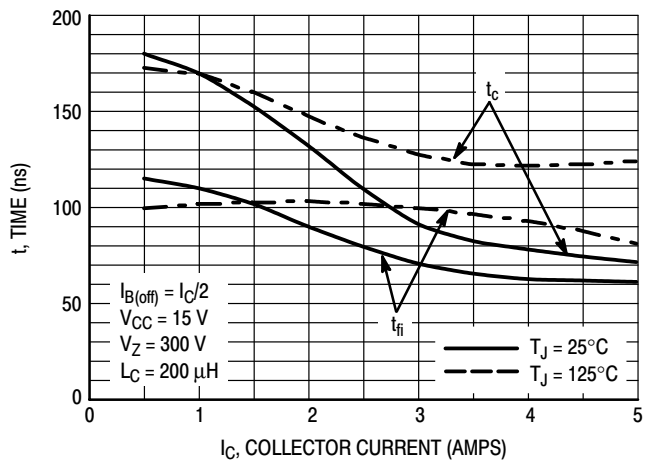


Figure 12. Inductive Switching,  $t_c$  &  $t_{fi}$ ,  $I_C/I_B = 10$

**TYPICAL SWITCHING CHARACTERISTICS**  
( $I_{B2} = I_C/2$  for all switching)

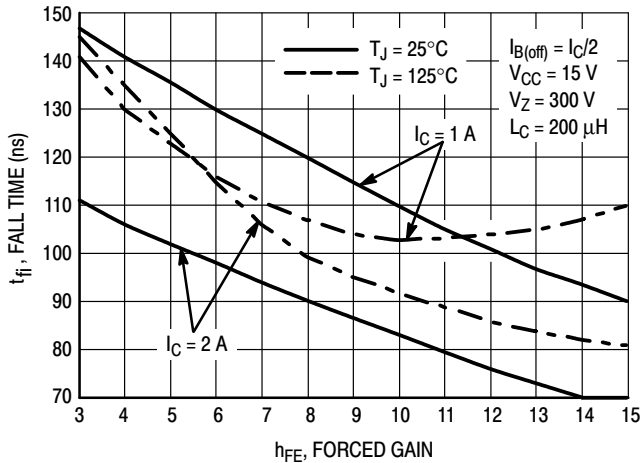


Figure 13. Inductive Fall Time,  $t_{fi}(h_{FE})$

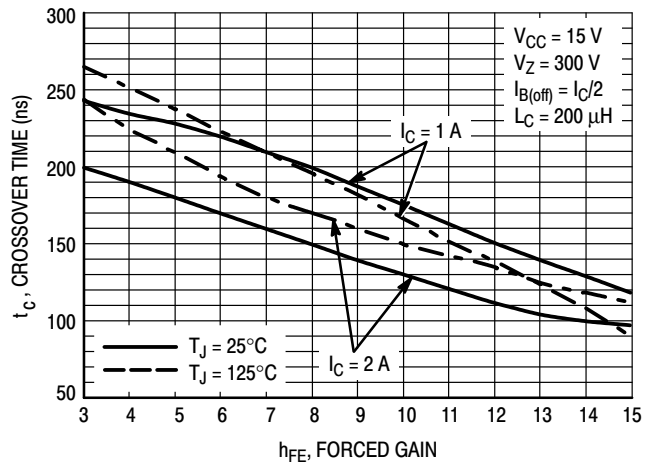


Figure 14. Crossover Time

**GUARANTEED SAFE OPERATING AREA INFORMATION**

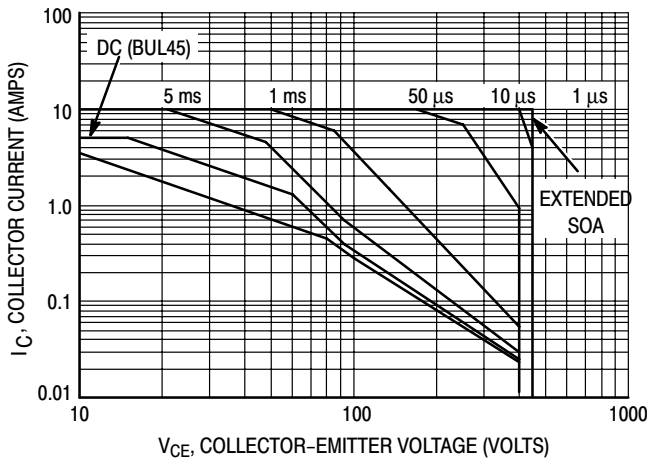


Figure 15. Forward Bias Safe Operating Area

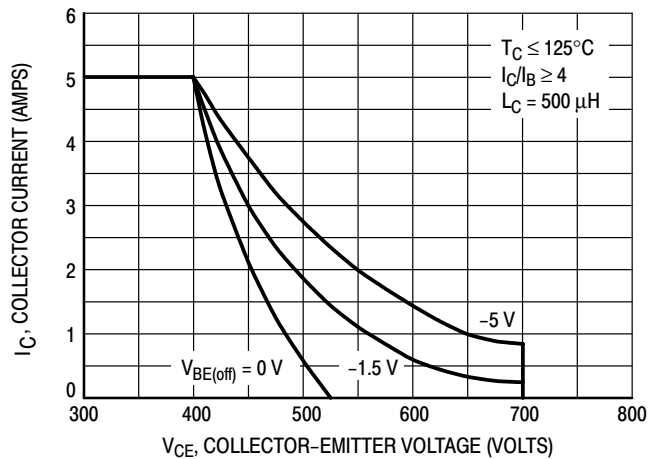


Figure 16. Reverse Bias Switching Safe Operating Area

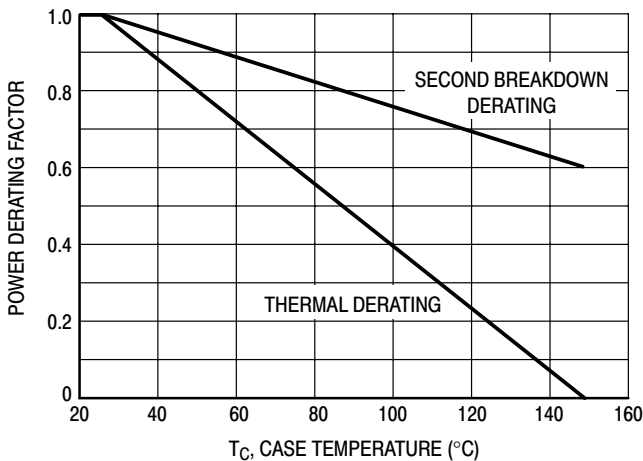


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.  $T_{J(pk)}$  may be calculated from the data in Figures 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse-biased. The safe level is specified as a reverse-biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

# BUL45

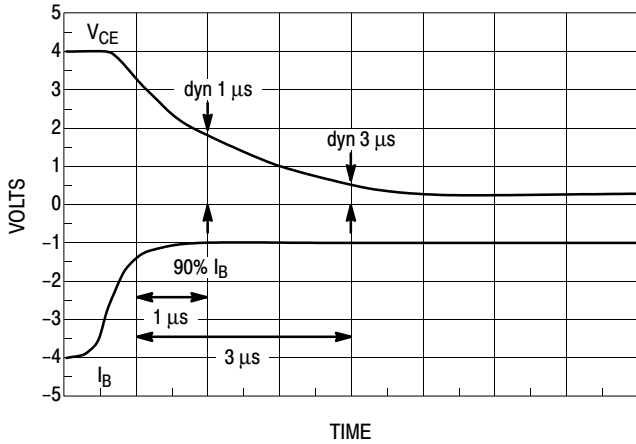


Figure 18. Dynamic Saturation Voltage Measurements

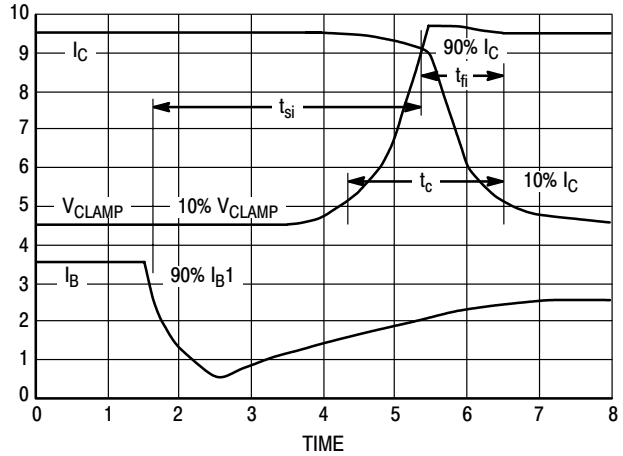
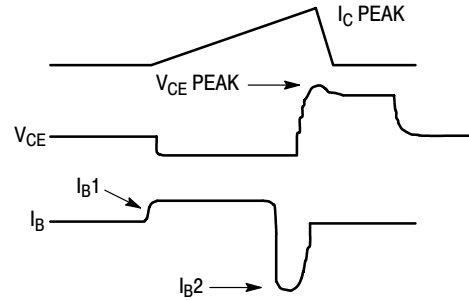
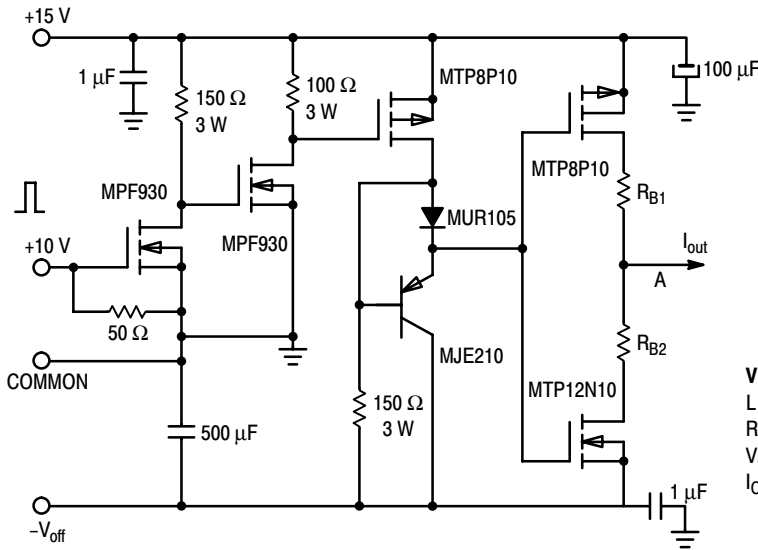


Figure 19. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
VCC = 20 VOLTS	VCC = 15 VOLTS	VCC = 15 VOLTS
IC(pk) = 100 mA	RB1 SELECTED FOR DESIRED IB1	RB1 SELECTED FOR DESIRED IB1

Table 1. Inductive Load Switching Drive Circuit

## TYPICAL THERMAL RESPONSE

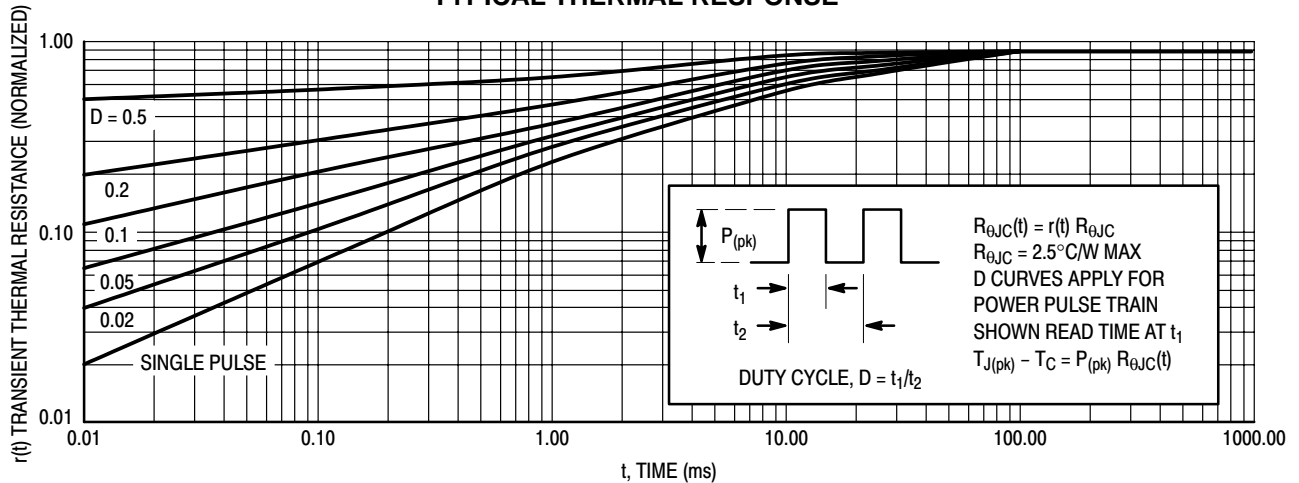
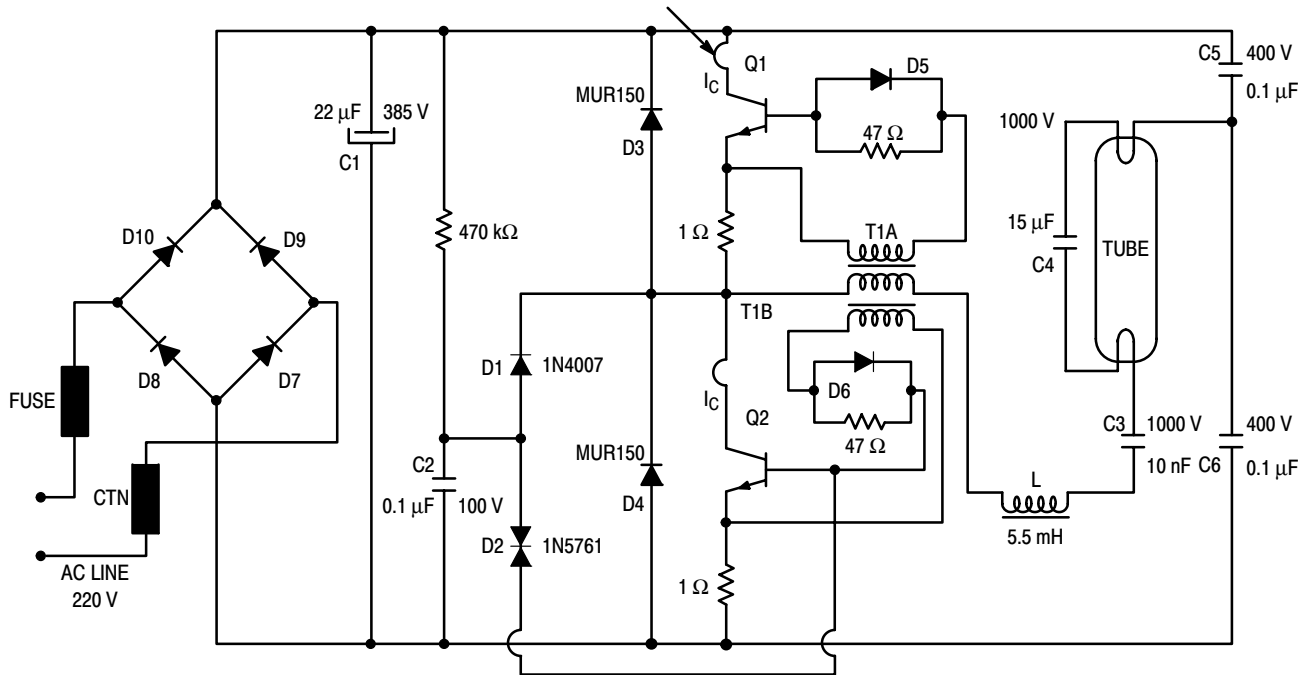


Figure 20. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for BUL45

## BUL45

The BUL45 Bipolar Power Transistors were specially designed for use in electronic lamp ballasts. A circuit designed by ON Semiconductor applications was built to

demonstrate how well these devices operate. The circuit and detailed component list are provided below.



### Components Lists

Q1 = Q2 = BUL45 Transistor  
 D1 = 1N4007 Rectifier  
 D2 = 1N5761 Rectifier  
 D3 = D4 = MUR150  
 D5 = D6 = MUR105  
 D7 = D8 = D9 = D10 = 1N400  
 CTN = 47 Ω @ 25°C  
 L = RM10 core, A1 = 400, B51 (LCC) 75 turns,  
 wire  $\varnothing$  = 0.6 mm  
 T1 = FT10 toroid, T4A (LCC)  
 Primary: 4 turns  
 Secondaries: T1A: 4 turns  
 T1B: 4 turns

All resistors are 1/4 Watt,  $\pm 5\%$

R1 = 470 kΩ  
 R2 = R3 = 47 Ω  
 R4 = R5 = 1 Ω (these resistors are optional, and  
 might be replaced by a short circuit)  
 C1 = 22 μF/385 V  
 C2 = 0.1 μF  
 C3 = 10 nF/1000 V  
 C4 = 15 nF/1000 V  
 C5 = C6 = 0.1 μF/400 V

### NOTES:

1. Since this design does not include the line input filter, it cannot be used "as-is" in a practical industrial circuit.
2. The windings are given for a 55 Watt load. For proper operation they must be re-calculated with any other loads.

Figure 21. Application Example



# SWITCHMODE™ Series NPN Silicon Power Transistor

... designed for high speed, high current, high power applications.

- High DC current gain:  
 $h_{FE} \text{ min} = 20 \text{ at } I_C = 25 \text{ A}$   
 $= 10 \text{ at } I_C = 50 \text{ A}$
- Low  $V_{CE(sat)}$ :  
 $V_{CE(sat)} \text{ max.} = 0.6 \text{ V at } I_C = 25 \text{ A}$   
 $= 0.9 \text{ V at } I_C = 50 \text{ A}$
- Very fast switching times:  
 $T_F = 0.25 \mu\text{s at } I_C = 50 \text{ A}$

### MAXIMUM RATINGS

Rating	Symbol	BUV20	BUV60	Unit
Collector–Emititer Voltage	$V_{CEO(sus)}$	125		Vdc
Collector–Base Voltage	$V_{CBO}$	160	260	Vdc
Emitter–Base Voltage	$V_{EBO}$	7		Vdc
Collector–Emitter Voltage ( $V_{BE} = -1.5 \text{ V}$ )	$V_{CEX}$	160	260	Vdc
Collector–Emitter voltage ( $R_{BE} = 100 \Omega$ )	$V_{CER}$	150	260	Vdc
Collector–Current — Continuous — Peak ( $PW \leq 10 \text{ ms}$ )	$I_C$	50		Adc
	$I_{CM}$	60		Apk
Base–Current continuous	$I_B$	10		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	250		Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to 200		$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	BUV20	BUV60	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.7		$^\circ\text{C/W}$

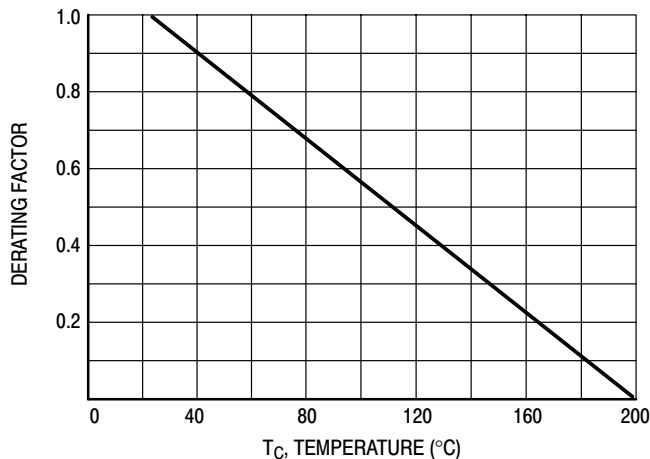
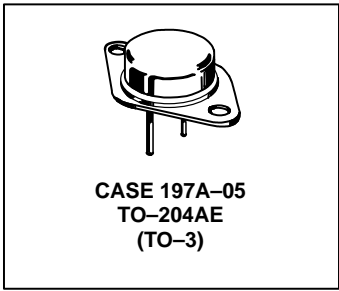


Figure 1. Power Derating

**BUV20**  
**BUV60**

**50 AMPERES**  
**NPN SILICON**  
**POWER**  
**METAL TRANSISTOR**  
**125 VOLTS**  
**250 WATTS**



# BUV20 BUV60

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS<sup>1</sup>

Collector–Emitter Sustaining Voltage ( $I_C = 200\text{ mA}$ , $I_B = 0$ , $L = 25\text{ mH}$ )	BUV20, BUV60	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Bias ( $V_{CE} = 140\text{ V}$ , $V_{BE} = -1.5\text{ V}$ ) ( $V_{CE} = 140\text{ V}$ , $V_{BE} = -1.5\text{ V}$ , $T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 260\text{ V}$ , $V_{BE} = -1.5\text{ V}$ )	BUV20 BUV20 BUV60	$I_{CEX}$		3.0 12	mAdc
Collector–Emitter Cutoff Current ( $V_{CE} = 100\text{ V}$ )	BUV20	$I_{CEO}$		3.0	mAdc
Emitter–Base Reverse Voltage ( $I_E = 50\text{ mA}$ )	BUV20, BUV60	$V_{EBO}$	7		V
Emitter–Cutoff Current ( $V_{EB} = 5\text{ V}$ )	BUV20, BUV60	$I_{EBO}$		1.0	mAdc

### SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ( $V_{CE} = 20\text{ V}$ , $t = 1\text{ s}$ ) ( $V_{CE} = 40\text{ V}$ , $t = 1\text{ s}$ )		$I_{S/b}$	12 1.5		A
---	--	-----------	-----------	--	---

### ON CHARACTERISTICS<sup>1</sup>

DC Current Gain ( $I_C = 25\text{ A}$ , $V_{CE} = 2\text{ V}$ ) ( $I_C = 50\text{ A}$ , $V_{CE} = 4\text{ V}$ )	BUV20 BUV20	$h_{FE}$	20 10	60 –	
Collector–Emitter Saturation Voltage ( $I_C = 25\text{ A}$ , $I_B = 2.5\text{ A}$ ) ( $I_C = 50\text{ A}$ , $I_B = 5\text{ A}$ )	BUV20 BUV20	$V_{CE(sat)}$		0.6 1.2	Vdc
Base–Emitter Saturation Voltage ( $I_C = 50\text{ A}$ , $I_B = 5\text{ A}$ )	BUV20	$V_{BE(sat)}$		2.0	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 25\text{ A}$ , $I_B = 1.25\text{ A}$ ) ( $I_C = 50\text{ A}$ , $I_B = 5\text{ A}$ ) ( $I_C = 60\text{ A}$ , $I_B = 7.5\text{ A}$ )	BUV60 BUV60 BUV60	$V_{CE(sat)}$		0.9 0.9 1.2	Vdc
Base–Emitter Saturation Voltage ( $I_C = 50\text{ A}$ , $I_B = 5\text{ A}$ ) ( $I_C = 60\text{ A}$ , $I_B = 7.5\text{ A}$ )	BUV60 BUV60	$V_{BE(sat)}$		1.6 1.8	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ( $V_{CE} = 15\text{ V}$ , $I_C = 2\text{ A}$ , $f = 4\text{ MHz}$ )		$f_T$	8.0		MHz
--	--	-------	-----	--	-----

### SWITCHING CHARACTERISTICS (Resistive Load)

Turn–on Time	$(I_C = 50\text{ A}$ , $I_{B1} = I_{B2} = 5\text{ A}$ , $V_{CC} = 30\text{ V}$ , $R_C = 0.6\ \Omega$ )	$t_{on}$		1.5	$\mu\text{s}$
Storage Time		$t_s$		1.2	
Fall Time		$t_f$		0.25	

<sup>1</sup> Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

# BUV20 BUV60

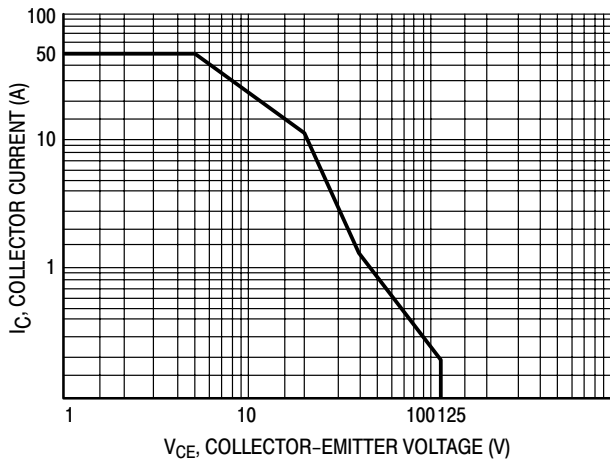


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_C = 25^\circ\text{C}$ .  $T_{J(pk)}$  is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

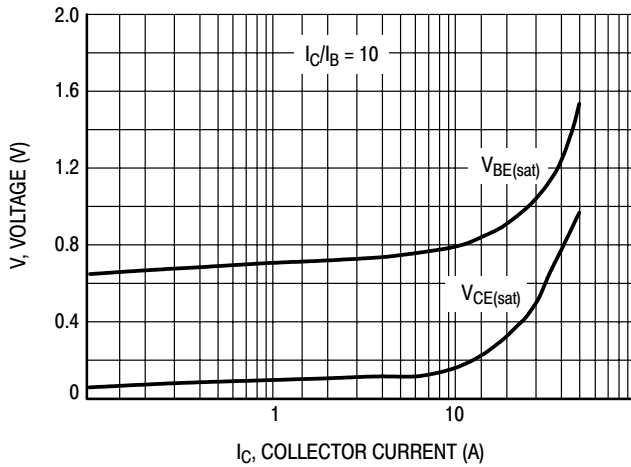


Figure 3. "On" Voltages

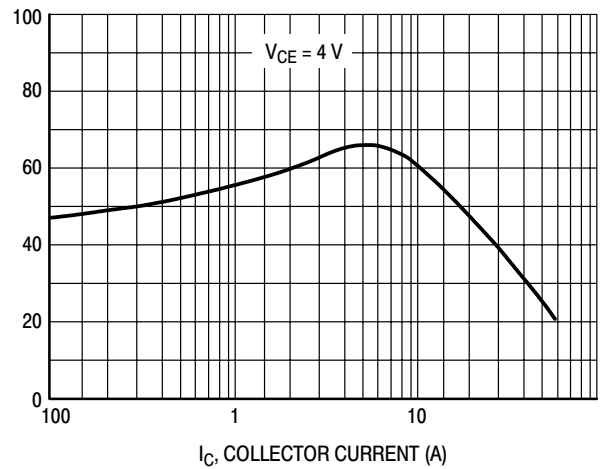


Figure 4. DC Current Gain

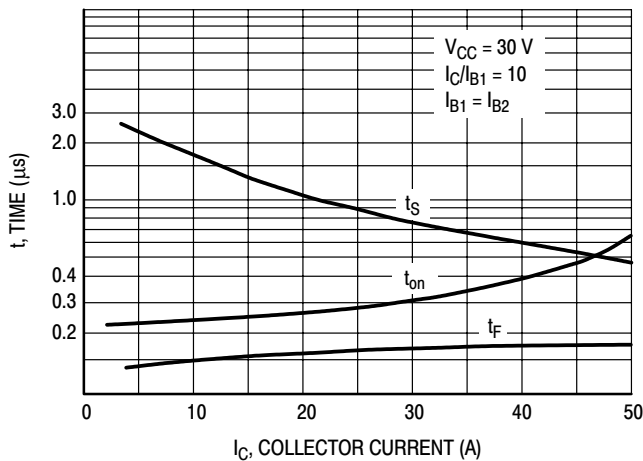


Figure 5. Resistive Switching Performance

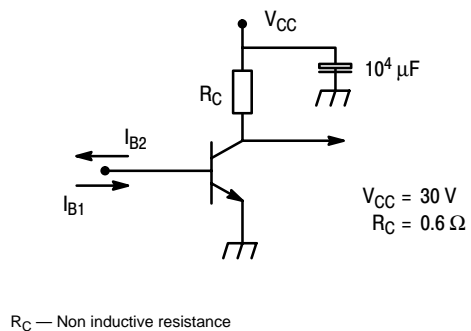


Figure 6. Switching Times Test Circuit

# SWITCHMODE™ Series NPN Silicon Power Transistor

... designed for high speed, high current, high power applications.

- High DC current gain:  
 $h_{FE} \text{ min.} = 20 \text{ at } I_C = 12 \text{ A}$
- Low  $V_{CE(sat)}$ ,  $V_{CE(sat)}$   
 $\text{max.} = 0.6 \text{ V at } I_C = 8 \text{ A}$
- Very fast switching times:  
 $TF \text{ max.} = 0.4 \mu\text{s at } I_C = 25 \text{ A}$

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector–Base Voltage	$V_{CBO}$	250	Vdc
Emitter–Base Voltage	$V_{EBO}$	7	Vdc
Collector–Emitter Voltage ( $V_{BE} = -1.5 \text{ V}$ )	$V_{CEX}$	250	Vdc
Collector–Emitter Voltage ( $R_{BE} = 100 \Omega$ )	$V_{CER}$	240	Vdc
Collector–Current — Continuous	$I_C$	40	Adc
— Peak ( $PW \leq 10 \text{ ms}$ )	$I_{CM}$	50	Apk
Base–Current continuous	$I_B$	8	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	250	Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to 200	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.7	$^\circ\text{C/W}$

**BUV21**

**40 AMPERES  
NPN SILICON  
POWER  
METAL TRANSISTOR  
200 VOLTS  
250 WATTS**

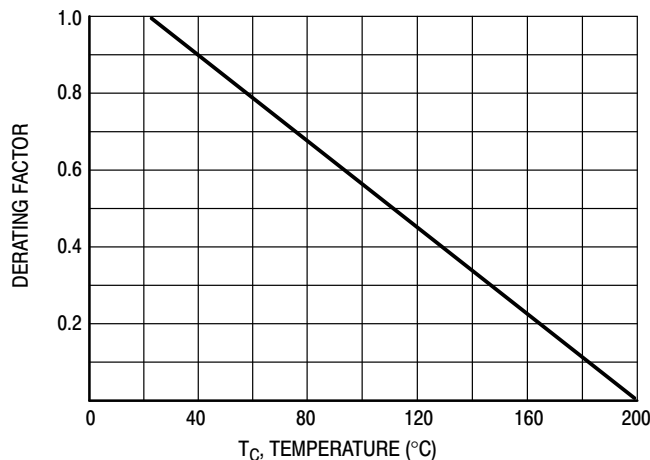
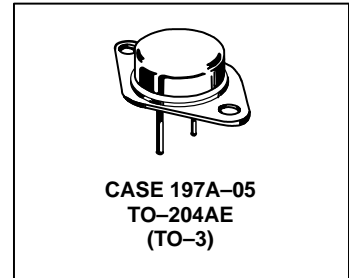


Figure 1. Power Derating

# BUV21

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS<sup>1</sup>

Collector–Emitter Sustaining Voltage ( $I_C = 200\text{ mA}$ , $I_B = 0$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias: ( $V_{CE} = 250\text{ V}$ , $V_{BE} = -1.5\text{ V}$ ) ( $V_{CE} = 250\text{ V}$ , $V_{BE} = -1.5\text{ V}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$		3.0 12.0	mAdc
Collector–Emitter Cutoff Current ( $V_{CE} = 160\text{ V}$ )	$I_{CEO}$		3.0	mAdc
Emitter–Base Reverse Voltage ( $I_E = 50\text{ mA}$ )	$V_{EBO}$	7		V
Emitter–Cutoff Current ( $V_{EB} = 5\text{ V}$ )	$I_{EBO}$		1.0	mAdc

### SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ( $V_{CE} = 20\text{ V}$ , $t = 1\text{ s}$ ) ( $V_{CE} = 140\text{ V}$ , $t = 1\text{ s}$ )	$I_{S/b}$	12 0.15		Adc
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### ON CHARACTERISTICS<sup>1</sup>

DC Current Gain ( $I_C = 12\text{ A}$ , $V_{CE} = 2\text{ V}$ ) ( $I_C = 25\text{ A}$ , $V_{CE} = 4\text{ V}$ )	$h_{FE}$	20 10	60	
Collector–Emitter Saturation Voltage ( $I_C = 12\text{ A}$ , $I_B = 1.2\text{ A}$ ) ( $I_C = 25\text{ A}$ , $I_B = 3\text{ A}$ )	$V_{CE(sat)}$		0.6 1.5	Vdc
Base–Emitter Saturation Voltage ( $I_C = 25\text{ A}$ , $I_B = 3\text{ A}$ )	$V_{BE(sat)}$		1.5	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ( $V_{CE} = 15\text{ V}$ , $I_C = 2\text{ A}$ , $f = 4\text{ MHz}$ )	$f_T$	8.0		MHz
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### SWITCHING CHARACTERISTICS (Resistive Load)

Turn-on Time	$(I_C = 25\text{ A}$ , $I_{B1} = I_{B2} = 3\text{ A}$ , $V_{CC} = 100\text{ V}$ , $R_C = 4\ \Omega$ )	$t_{on}$	1.0	$\mu\text{s}$
Storage Time		$t_s$	1.8	
Fall Time		$t_f$	0.4	

<sup>1</sup> Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

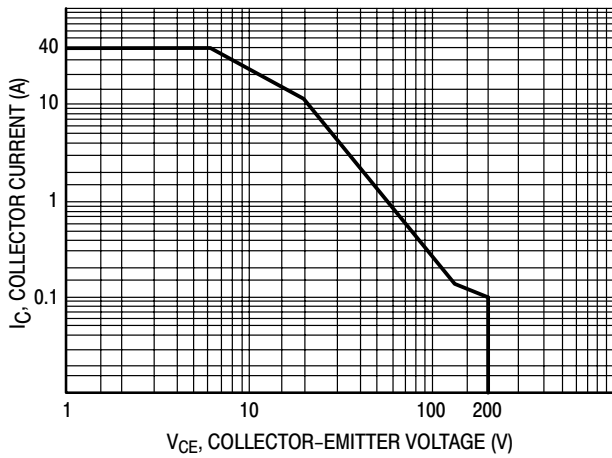


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_C = 25^\circ C$ ,  $T_{J(pk)}$  is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

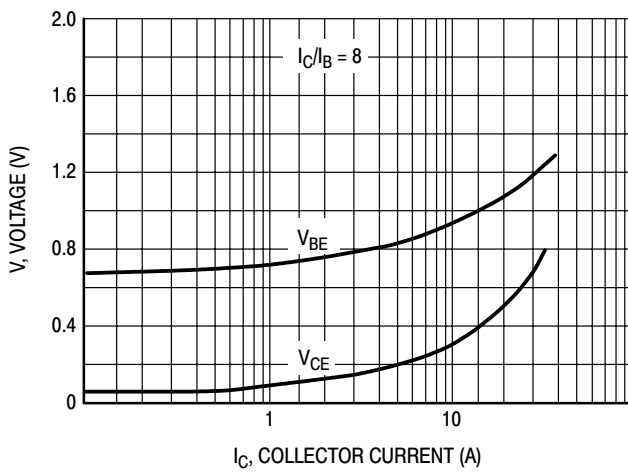


Figure 3. "On" Voltages

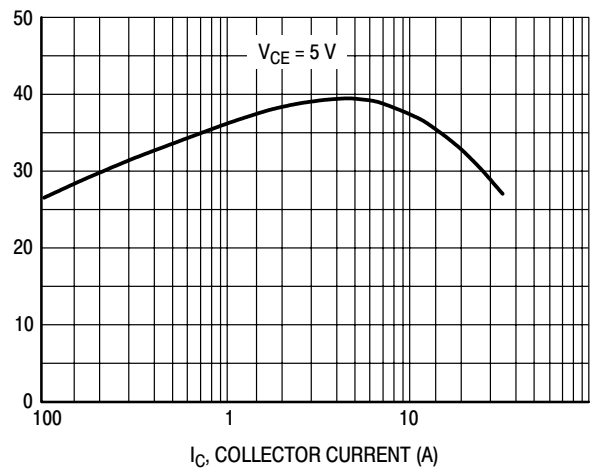


Figure 4. DC Current Gain

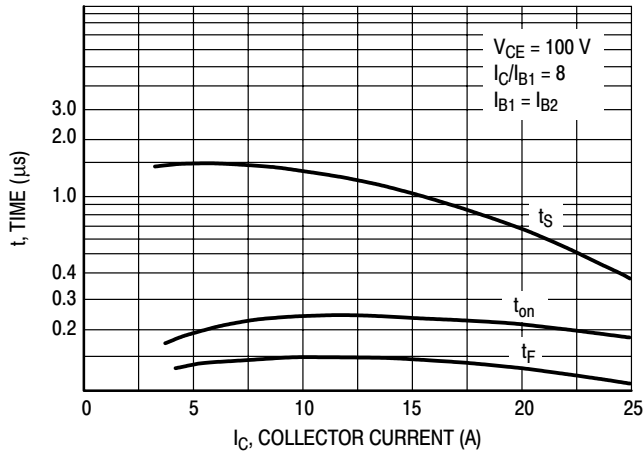


Figure 5. Resistive Switching Performance

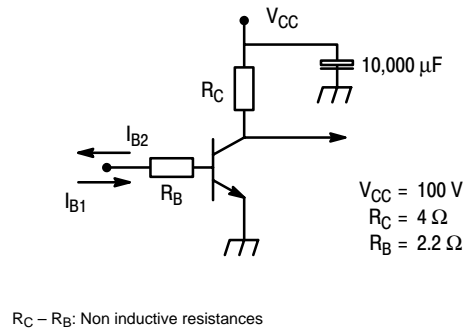


Figure 6. Switching Times Test Circuit

# SWITCHMODE™ Series NPN Silicon Power Transistor

... designed for high current, high speed, high power applications.

- High DC current gain:  
HFE min. = 20 at  $I_C = 10\text{ A}$
- Low  $V_{CE(sat)}$ :  $V_{CE(sat)}$   
max. = 1.0 V at  $I_C = 10\text{ A}$
- Very fast switching times:  
 $T_F$  max. = 0.35  $\mu\text{s}$  at  $I_C = 20\text{ A}$

### MAXIMUM RATINGS

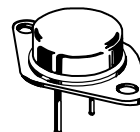
Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector–Base Voltage	$V_{CBO}$	300	Vdc
Emitter–Base Voltage	$V_{EBO}$	7	Vdc
Collector–Emitter Voltage ( $V_{BE} = -1.5\text{ V}$ )	$V_{CEX}$	300	Vdc
Collector–Emitter Voltage ( $R_{BE} = 100\ \Omega$ )	$V_{CER}$	290	Vdc
Collector–Current — Continuous	$I_C$	40	Adc
— Peak ( $p_w \leq 10\text{ ms}$ )	$I_{CM}$	50	Apk
Base–Current continuous	$I_B$	8	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	250	Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to 200	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.7	$^\circ\text{C/W}$

**BUV22**

**40 AMPERES  
NPN SILICON  
POWER  
METAL TRANSISTOR  
250 VOLTS  
250 WATTS**



**CASE 197A-05  
TO-204AE  
(TO-3)**

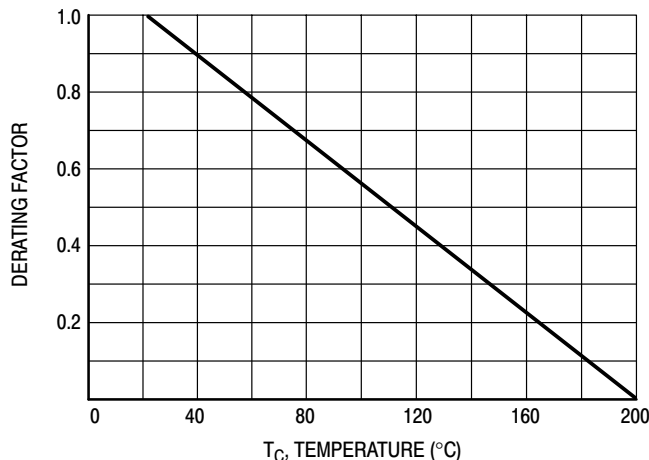


Figure 1. Power Derating

# BUV22

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS<sup>1</sup>

Collector–Emitter Sustaining Voltage ( $I_C = 200\text{ mA}$ , $I_B = 0$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Bias ( $V_{CE} = 300\text{ V}$ , $V_{BE} = -1.5\text{ V}$ ) ( $V_{CE} = 300\text{ V}$ , $V_{BE} = -1.5\text{ V}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$		3.0 12.0	mAdc
Collector–Emitter Cutoff Current ( $V_{CE} = 200\text{ V}$ )	$I_{CEO}$		3.0	mAdc
Emitter–Base Reverse Voltage ( $I_E = 50\text{ mA}$ )	$V_{EBO}$	7		V
Emitter–Cutoff Current ( $V_{EB} = 5\text{ V}$ )	$I_{EBO}$		1.0	mAdc

### SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ( $V_{CE} = 20\text{ V}$ , $t = 1\text{ s}$ ) ( $V_{CE} = 140\text{ V}$ , $t = 1\text{ s}$ )	$I_{S/b}$	12 0.15		Adc
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### ON CHARACTERISTICS<sup>1</sup>

DC Current Gain ( $I_C = 10\text{ A}$ , $V_{CE} = 4\text{ V}$ ) ( $I_C = 20\text{ A}$ , $V_{CE} = 4\text{ V}$ )	$h_{FE}$	20 10	60	
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ A}$ , $I_B = 1\text{ A}$ ) ( $I_C = 20\text{ A}$ , $I_B = 2.5\text{ A}$ )	$V_{CE(sat)}$		1.0 1.5	Vdc
Base–Emitter Saturation Voltage ( $I_C = 40\text{ A}$ , $I_B = 4\text{ A}$ )	$V_{BE(sat)}$		1.5	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ( $V_{CE} = 15\text{ V}$ , $I_C = 2\text{ A}$ , $f = 4\text{ MHz}$ )	$f_T$	8.0		MHz
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### SWITCHING CHARACTERISTICS (Resistive Load)

Turn–on Time	$(I_C = 20\text{ A}$ , $I_{B1} = I_{B2} = 2.5\text{ A}$ , $V_{CC} = 100\text{ V}$ , $R_C = 5\ \Omega$ )	$t_{on}$	0.8	$\mu\text{s}$
Storage Time		$t_s$	2.0	
Fall Time		$t_f$	0.35	

<sup>1</sup>Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .



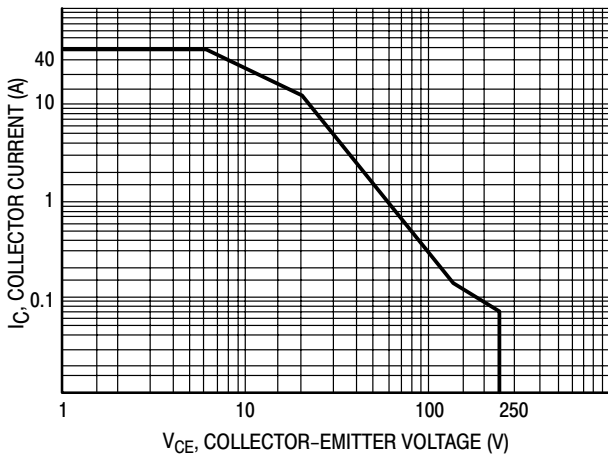


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

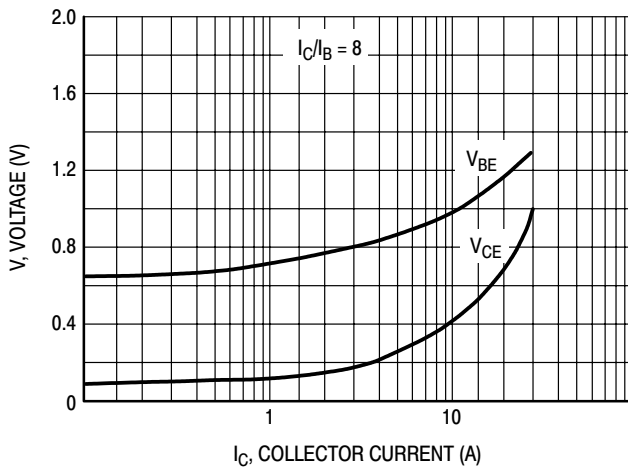


Figure 3. "On" Voltages

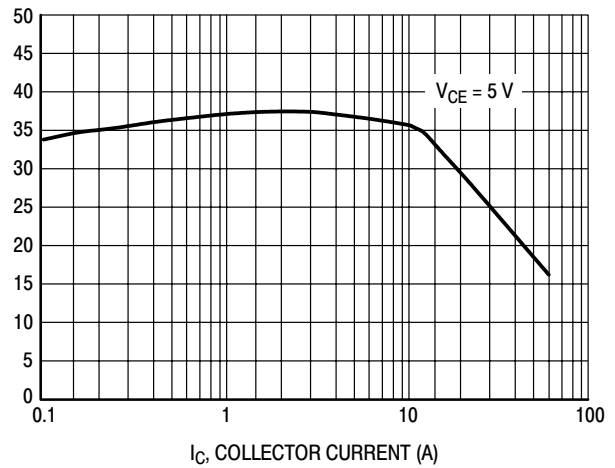


Figure 4. DC Current Gain

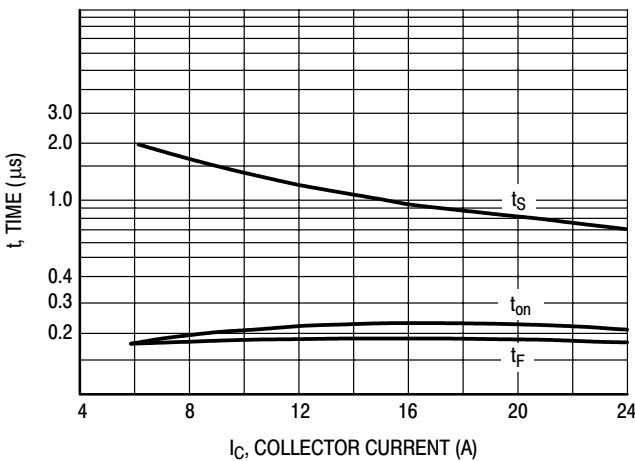
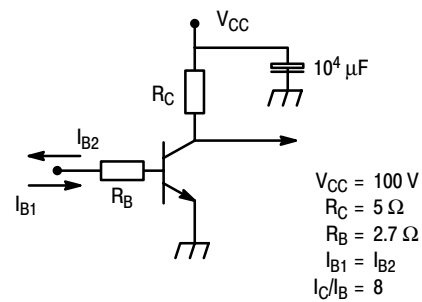


Figure 5. Resistive Switching Performance



$R_C - R_B$ : Non inductive resistances

$V_{CC} = 100\text{ V}$   
 $R_C = 5\ \Omega$   
 $R_B = 2.7\ \Omega$   
 $I_{B1} = I_{B2}$   
 $I_C/I_B = 8$

Figure 6. Switching Times Test Circuit

# SWITCHMODE™ NPN Silicon Power Transistors

The BUX85 is designed for high voltage, high speed power switching applications like converters, inverters, switching regulators, motor control systems.

## Specifications Features:

- $V_{CEO(sus)}$  450 V
- $V_{CES(sus)}$  1000 V
- Fall time = 0.3  $\mu$ s (typ) at  $I_C = 1.0$  A
- $V_{CE(sat)}$  = 1.0 V (max) at  $I_C = 1.0$  A,  $I_B = 0.2$  A

## MAXIMUM RATINGS

Rating	Symbol	BUX84	BUX85	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector–Emitter Voltage	$V_{CES}$	800	1000	Vdc
Emitter Base Voltage	$V_{EBO}$	5		Vdc
Collector Current — Continuous — Peak (1)	$I_C$ $I_{CM}$	2 3.0		Adc
Base Current — Continuous — Peak (1)	$I_B$ $I_{BM}$	0.75 1.0		Adc
Reverse Base Current — Peak	$I_{BM}$	1		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	50 400		Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C}$

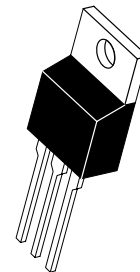
## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	$T_L$	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq 10\%$ .

## BUX85

2 AMPERES  
POWER TRANSISTOR  
NPN SILICON  
450 VOLTS  
50 WATTS



CASE 221A–09  
TO–220AB

# BUX85

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS (1)

Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ ) See fig. 1	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current ( $V_{CES} = \text{Rated Value}$ ) ( $V_{CES} = \text{Rated Value}$ , $T_C = 125^\circ\text{C}$ )	$I_{CES}$	—	—	0.2 1.5	mAdc
Emitter Cutoff Current ( $V_{EB} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	1	mAdc

### ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 0.1\text{ Adc}$ , $V_{CE} = 5\text{ V}$ )	$h_{FE}$	30	50	—	—
Collector–Emitter Saturation Voltage ( $I_C = 0.3\text{ Adc}$ , $I_B = 30\text{ mAdc}$ ) ( $I_C = 1\text{ Adc}$ , $I_B = 200\text{ mAdc}$ )	$V_{CE(sat)}$	—	—	0.8 1	Vdc
Base–Emitter Saturation Voltage ( $I_C = 1\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	$V_{BE(sat)}$	—	—	1.1	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$f_T$	4	—	—	MHz
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### SWITCHING CHARACTERISTICS

Turn–on Time	$V_{CC} = 250\text{ Vdc}$ , $I_C = 1\text{ A}$ $I_{B1} = 0.2\text{ A}$ , $I_{B2} = 0.4\text{ A}$ See fig. 2	$t_{on}$	—	0.3	0.5	$\mu\text{s}$
Storage Time		$t_s$	—	2	3.5	$\mu\text{s}$
Fall Time		$t_f$	—	0.3	—	$\mu\text{s}$
Fall Time	Same above cond. at $T_C = 95^\circ\text{C}$	$t_f$	—	—	1.4	$\mu\text{s}$

(1) Pulse Test:  $PW = 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

# BUX85

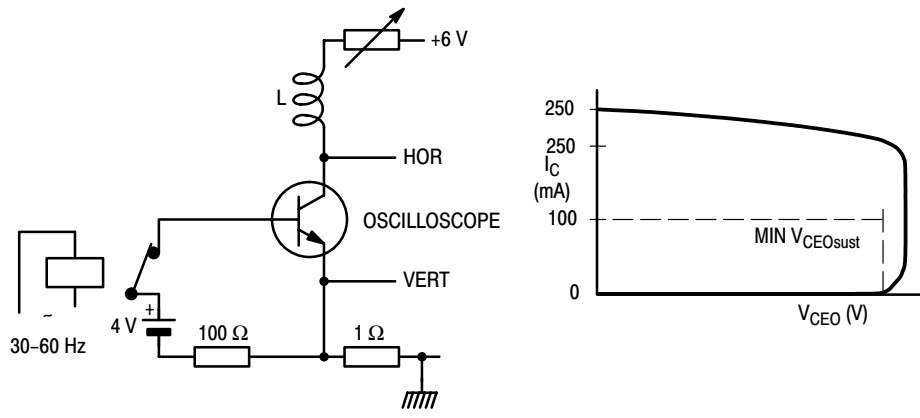


Figure 1. Test Circuit for  $V_{CEOsust}$

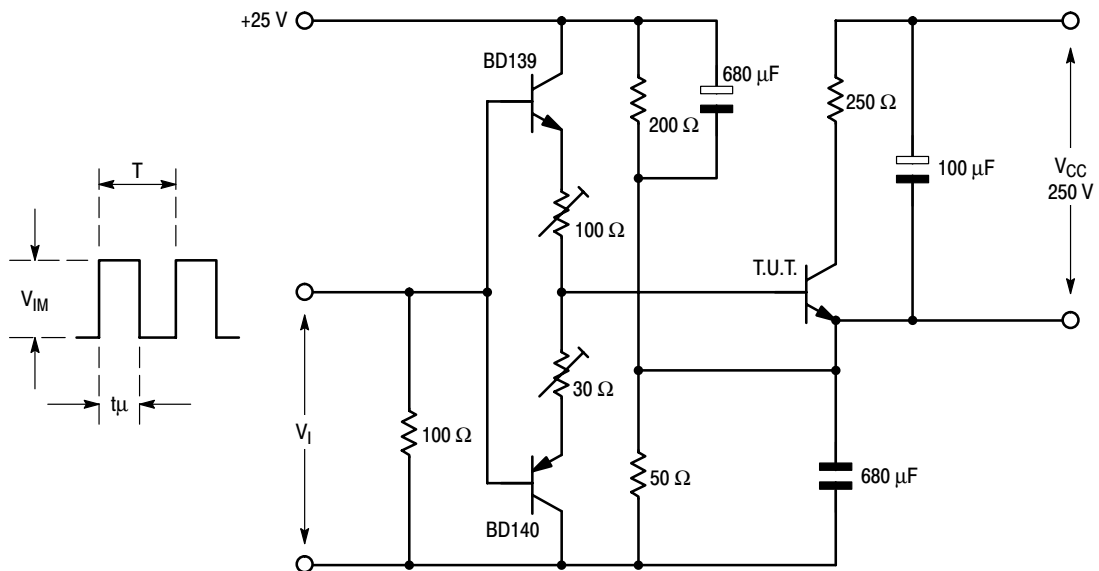
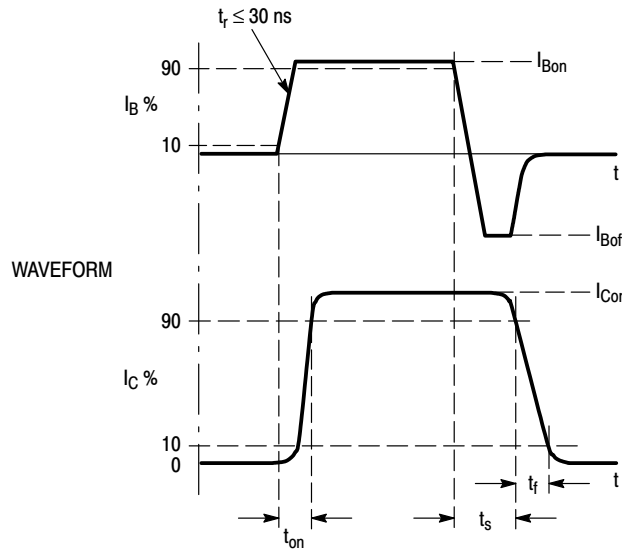


Figure 2. Switching Times/Test Circuit

# Complementary Silicon Power Transistors

... for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector–Emitter Saturation Voltage  
 $V_{CE(sat)} = 1.0 \text{ V (Max) @ } 8.0 \text{ A}$
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

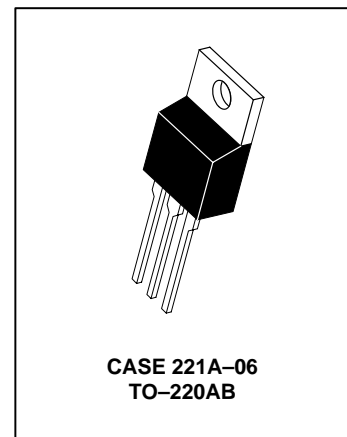
**NPN  
D44H Series\***  
**PNP  
D45H Series\***

\*ON Semiconductor Preferred Device

**10 AMPERE  
COMPLEMENTARY  
SILICON  
POWER TRANSISTORS  
60, 80 VOLTS**

## MAXIMUM RATINGS

Rating	Symbol	D44H or D45H		Unit
		8	10, 11	
Collector–Emitter Voltage	$V_{CEO}$	60	80	Vdc
Emitter Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous — Peak (1)	$I_C$	10 20		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_A = 25^\circ\text{C}$	$P_D$	50 1.67		Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–55 to 150		$^\circ\text{C}$



## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	$^\circ\text{C}$

(1) Pulse Width  $\leq 6.0 \text{ ms}$ , Duty Cycle  $\leq 50\%$ .

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DC Current Gain ( $V_{CE} = 1.0 \text{ Vdc}$ , $I_C = 2.0 \text{ Adc}$ )	D44H10 D45H10	35	—	—
	D44H8,11 D44H8,11	60	—	
( $V_{CE} = 1.0 \text{ Vdc}$ , $I_C = 4.0 \text{ Adc}$ )	D44H10 D45H10	20	—	—
	D44H8,11 D45H8,11	40	—	

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

## D44H Series D45H Series

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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#### OFF CHARACTERISTICS

Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}, V_{BE} = 0$ )	$I_{CES}$	—	—	10	$\mu\text{A}$
Emitter Cutoff Current ( $V_{EB} = 5.0 \text{ Vdc}$ )	$I_{EBO}$	—	—	100	$\mu\text{A}$

#### ON CHARACTERISTICS

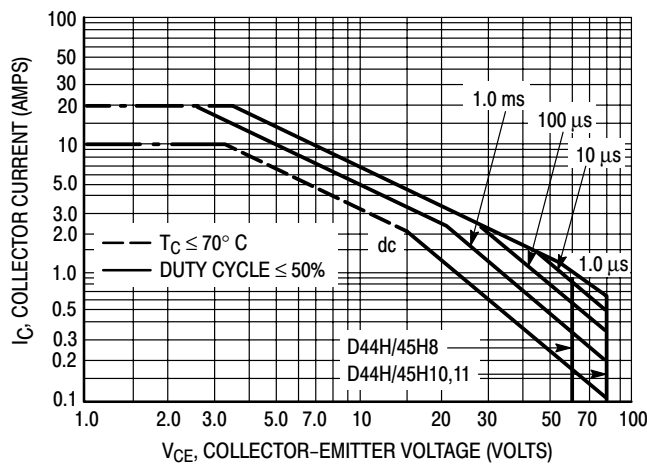
Collector-Emitter Saturation Voltage ( $I_C = 8.0 \text{ Adc}, I_B = 0.4 \text{ Adc}$ ) ( $I_C = 8.0 \text{ Adc}, I_B = 0.8 \text{ Adc}$ )		$V_{CE(\text{sat})}$	—	—	1.0	Vdc
	D44H/D45H8,11 D44H/D45H10				1.0	
Base-Emitter Saturation Voltage ( $I_C = 8.0 \text{ Adc}, I_B = 0.8 \text{ Adc}$ )		$V_{BE(\text{sat})}$	—	—	1.5	Vdc

#### DYNAMIC CHARACTERISTICS

Collector Capacitance ( $V_{CB} = 10 \text{ Vdc}, f_{\text{test}} = 1.0 \text{ MHz}$ )		$C_{cb}$	—	130	—	pF
	D44H Series D45H Series			230	—	
Gain Bandwidth Product ( $I_C = 0.5 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 20 \text{ MHz}$ )		$f_T$	—	50	—	MHz
	D44H Series D45H Series			40	—	

#### SWITCHING TIMES

Delay and Rise Times ( $I_C = 5.0 \text{ Adc}, I_{B1} = 0.5 \text{ Adc}$ )		$t_d + t_r$	—	300	—	ns
	D44H Series D45H Series			135	—	
Storage Time ( $I_C = 5.0 \text{ Adc}, I_{B1} = I_{B2} = 0.5 \text{ Adc}$ )		$t_s$	—	500	—	ns
	D44H Series D45H Series			500	—	
Fall Time ( $I_C = 5.0 \text{ Adc}, I_{B1} = 102 = 0.5 \text{ Adc}$ )		$t_f$	—	140	—	ns
	D44H Series D45H Series			100	—	



**Figure 1. Maximum Rated Forward Bias Safe Operating Area**

# Complementary Silicon Power Transistors

These complementary silicon power transistors are designed for high-speed switching applications, such as switching regulators and high frequency inverters. The devices are also well-suited for drivers for high power switching circuits.

- Fast Switching —  
 $t_f = 90 \text{ ns (Max)}$
- Key Parameters Specified @ 100°C
- Low Collector-Emitter Saturation Voltage —  
 $V_{CE(sat)} = 1.0 \text{ V (Max) @ 8.0 A}$
- Complementary Pairs Simplify Circuit Designs

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	80	Vdc
Collector-Emitter Voltage	$V_{CEV}$	100	Vdc
Emitter Base Voltage	$V_{EB}$	7.0	Vdc
Collector Current — Continuous	$I_C$	15	Adc
— Peak (1)	$I_{CM}$	20	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	83	Watts
Derate above 25°C		0.67	W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to 150	°C

## THERMAL CHARACTERISTICS

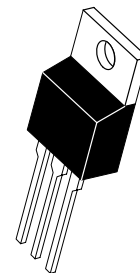
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	°C

(2) Pulse Width  $\leq 6.0 \text{ ms}$ , Duty Cycle  $\leq 50\%$ .

NOTE: All polarities are shown for NPN transistors. For PNP transistors, reverse polarities.

**NPN  
D44VH  
PNP  
D45VH**

**15 AMPERE  
COMPLEMENTARY  
SILICON  
POWER TRANSISTORS  
80 VOLTS  
83 WATTS**



**CASE 221A-09  
TO-220AB**

# D44VH D45VH

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (2) (I <sub>C</sub> = 25 mA, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	80	—	—	Vdc
Collector–Emitter Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEV</sub> , V <sub>BE(off)</sub> = 4.0 Vdc) (V <sub>CE</sub> = Rated V <sub>CEV</sub> , V <sub>BE(off)</sub> = 4.0 Vdc, T <sub>C</sub> = 100°C)	I <sub>CEV</sub>	—	—	10 100	μA
Emitter Base Cutoff Current (V <sub>EB</sub> = 7.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	—	10	μA

### ON CHARACTERISTICS (2)

DC Current Gain (I <sub>C</sub> = 2.0 A, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 4.0 A, V <sub>CE</sub> = 1.0 Vdc)	h <sub>FE</sub>	35 20	— —	— —	—
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 8.0 A, I <sub>B</sub> = 0.4 A) D44VH10 (I <sub>C</sub> = 8.0 A, I <sub>B</sub> = 0.8 A) D45VH10 (I <sub>C</sub> = 15 A, I <sub>B</sub> = 3.0 A, T <sub>C</sub> = 100°C) D44VH10 D45VH10	V <sub>CE(sat)</sub>	— — — —	— — — —	0.4 1.0 0.8 1.5	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 8.0 A, I <sub>B</sub> = 0.4 A) D44VH10 (I <sub>C</sub> = 8.0 A, I <sub>B</sub> = 0.8 A) D45VH10 (I <sub>C</sub> = 8.0 A, I <sub>B</sub> = 0.4 A, T <sub>C</sub> = 100°C) D44VH10 (I <sub>C</sub> = 8.0 A, I <sub>B</sub> = 0.8 A, T <sub>C</sub> = 100°C) D45VH10	V <sub>BE(sat)</sub>	— — — —	— — — —	1.2 1.0 1.1 1.5	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth Product (I <sub>C</sub> = 0.1 A, V <sub>CE</sub> = 10 Vdc, f = 20 MHz)	f <sub>T</sub>	—	50	—	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>C</sub> = 0, f <sub>test</sub> = 1.0 MHz) D44VH10 D45VH10	C <sub>ob</sub>	— —	120 275	— —	pF

### SWITCHING CHARACTERISTICS

Delay Time	(V <sub>CC</sub> = 20 Vdc, I <sub>C</sub> = 8.0 A, I <sub>B1</sub> = I <sub>B2</sub> = 0.8 A)	t <sub>d</sub>	—	—	50	ns
Rise Time		t <sub>r</sub>	—	—	250	
Storage Time		t <sub>s</sub>	—	—	700	
Fall Time		t <sub>f</sub>	—	—	90	

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



# Complementary Silicon Power Transistor

... for general purpose driver or medium power output stages in CW or switching applications.

- Low Collector–Emitter Saturation Voltage — 0.5 V (Max)
- High  $f_t$  for Good Frequency Response
- Low Leakage Current

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Collector–Emitter Voltage	$V_{CES}$	90	Vdc
Emitter Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous Peak (1)	$I_C$	4.0 6.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_A = 25^\circ\text{C}$	$P_D$	30 1.67	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–55 to 150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.2	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	$^\circ\text{C}$

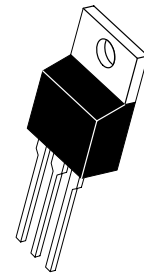
(1) Pulse Width  $\leq$  6.0 ms, Duty Cycle  $\leq$  50%.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DC Current Gain	$h_{FE}$			—
( $V_{CE} = 1.0$ Vdc, $I_C = 0.2$ Adc)		40	120	
( $V_{CE} = 1.0$ Vdc, $I_C = 1.0$ Adc)		20	—	
( $V_{CE} = 1.0$ Vdc, $I_C = 2.0$ Adc)		20	—	

**PNP  
D45C  
NPN  
D44C**

**4.0 AMPERE  
COMPLEMENTARY  
SILICON  
POWER TRANSISTORS  
80 VOLTS**



**CASE 221A-09  
TO-220AB**

# NPN

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}, V_{BE} = 0$ )	$I_{CES}$	—	—	0.1	$\mu\text{A}$
Emitter Cutoff Current ( $V_{EB} = 5.0 \text{ Vdc}$ )	$I_{EBO}$	—	—	10	$\mu\text{A}$

### ON CHARACTERISTICS

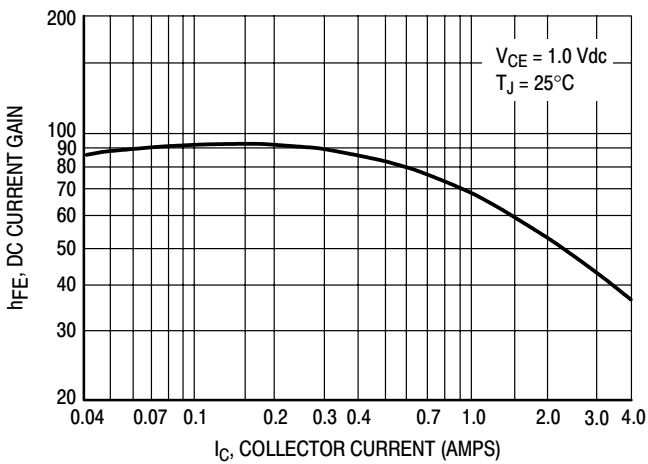
Collector–Emitter Saturation Voltage ( $I_C = 1.0 \text{ Adc}, I_B = 50 \text{ mAdc}$ )	$V_{CE(\text{sat})}$	—	0.135	0.5	Vdc
Base–Emitter Saturation Voltage ( $I_C = 1.0 \text{ Adc}, I_B = 100 \text{ mAdc}$ )	$V_{BE(\text{sat})}$	—	0.85	1.3	Vdc

### DYNAMIC CHARACTERISTICS

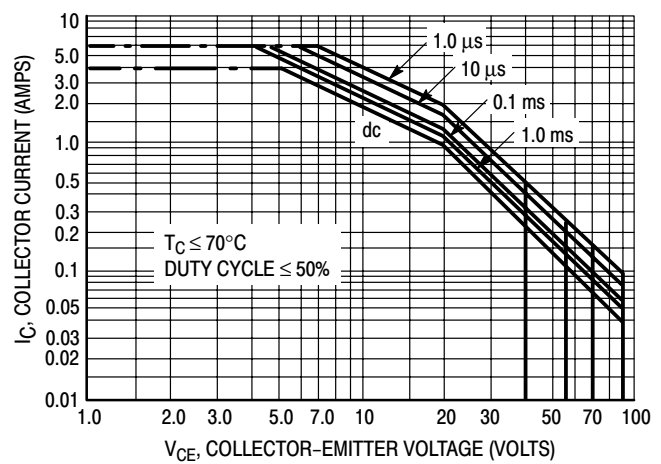
Collector Capacitance ( $V_{CB} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$ )	$C_{cb}$	—	125	—	$\mu\text{F}$
Gain Bandwidth Product ( $I_C = 20 \text{ mA}, V_{CE} = 4.0 \text{ Vdc}, f = 20 \text{ MHz}$ )	$f_T$	—	40	—	MHz

### SWITCHING TIMES

Delay and Rise Times ( $I_C = 1.0 \text{ Adc}, I_{B1} = 0.1 \text{ Adc}$ )	$t_d + t_r$	—	50	75	ns
Storage Time ( $I_C = 1.0 \text{ Adc}, I_{B1} = I_{B2} = 0.1 \text{ Adc}$ )	$t_s$	—	350	550	ns
Fall Time ( $I_C = 1.0 \text{ Adc}, I_{B1} = I_{B2} = 0.1 \text{ Adc}$ )	$t_f$	—	50	75	ns



**Figure 2. Typical DC Current Gain**



**Figure 3. Maximum Rated Forward Bias Safe Operating Area**

# High-Current Complementary Silicon Transistors

... for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain —  
 $h_{FE} = 1000$  (Min) @  $I_C = 20$  Adc
- Monolithic Construction with Built-in Base Emitter Shunt Resistor
- Junction Temperature to +200°C

## MAXIMUM RATINGS

Rating	Symbol	MJ11012	MJ11015 MJ11016	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	120	Vdc
Collector–Base Voltage	$V_{CB}$	60	120	Vdc
Emitter–Base Voltage	$V_{EB}$	5		Vdc
Collector Current	$I_C$	30		Adc
Base Current	$I_B$	1		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	$P_D$	200	1.15	Watts W/°C
Operating Storage Junction Temperature Range	$T_J, T_{stg}$	–55 to +200		°C

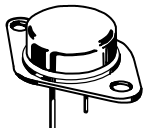
## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.87	°C/W
Maximum Lead Temperature for Soldering Purposes for $\leq 10$ Seconds.	$T_L$	275	°C

**PNP**  
**MJ11015**  
**NPN**  
**MJ11012**  
**MJ11016\***

\*ON Semiconductor Preferred Device

**30 AMPERE**  
**DARLINGTON**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**60–120 VOLTS**  
**200 WATTS**



**CASE 1–07**  
**TO–204AA**  
**(TO–3)**

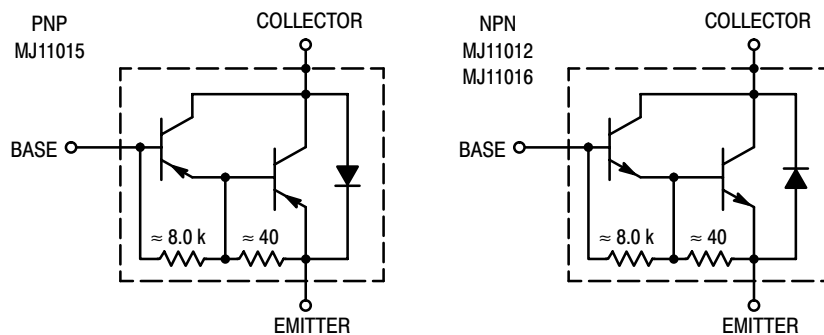


Figure 1. Darlington Circuit Schematic

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJ11015 MJ11012 MJ11016

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Breakdown Voltage(1) (I <sub>C</sub> = 100 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	60 120	— —	Vdc
	MJ11012 MJ11015, MJ11016			
Collector–Emitter Leakage Current (V <sub>CE</sub> = 60 Vdc, R <sub>BE</sub> = 1k ohm)	I <sub>CER</sub>	—	1	mA
(V <sub>CE</sub> = 120 Vdc, R <sub>BE</sub> = 1k ohm)	MJ11015, MJ11016	—	1	
(V <sub>CE</sub> = 60 Vdc, R <sub>BE</sub> = 1k ohm, T <sub>C</sub> = 150°C)	MJ11012	—	5	
(V <sub>CE</sub> = 120 Vdc, R <sub>BE</sub> = 1k ohm, T <sub>C</sub> = 150°C)	MJ11015, MJ11016	—	5	
Emitter Cutoff Current (V <sub>BE</sub> = 5 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	5	mA
Collector–Emitter Leakage Current (V <sub>CE</sub> = 50 Vdc, I <sub>B</sub> = 0)	I <sub>CEO</sub>	—	1	mA
<b>ON CHARACTERISTICS(1)</b>				
DC Current Gain (I <sub>C</sub> = 20 A, V <sub>CE</sub> = 5 Vdc)	h <sub>FE</sub>	1000	—	—
(I <sub>C</sub> = 30 A, V <sub>CE</sub> = 5 Vdc)		200	—	
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 20 A, I <sub>B</sub> = 200 mA)	V <sub>CE(sat)</sub>	—	3	Vdc
(I <sub>C</sub> = 30 A, I <sub>B</sub> = 300 mA)		—	4	
Base–Emitter Saturation Voltage (I <sub>C</sub> = 20 A, I <sub>B</sub> = 200 mA)	V <sub>BE(sat)</sub>	—	3.5	Vdc
(I <sub>C</sub> = 30 A, I <sub>B</sub> = 300 mA)		—	5	
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain Bandwidth Product (I <sub>C</sub> = 10 A, V <sub>CE</sub> = 3 Vdc, f = 1 MHz)	h <sub>fe</sub>	4	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

# MJ11015 MJ11012 MJ11016

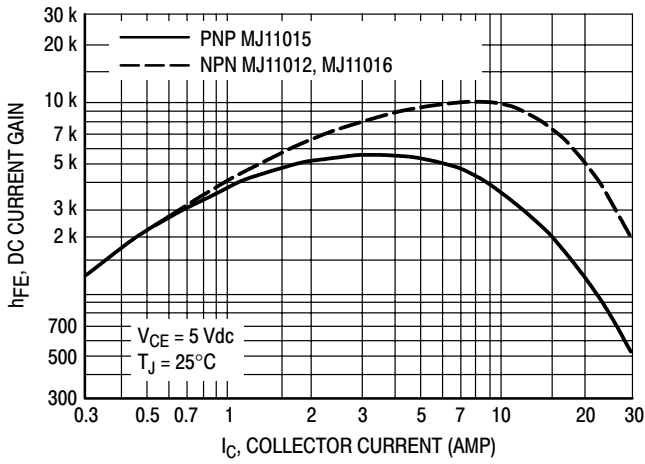


Figure 2. DC Current Gain (1)

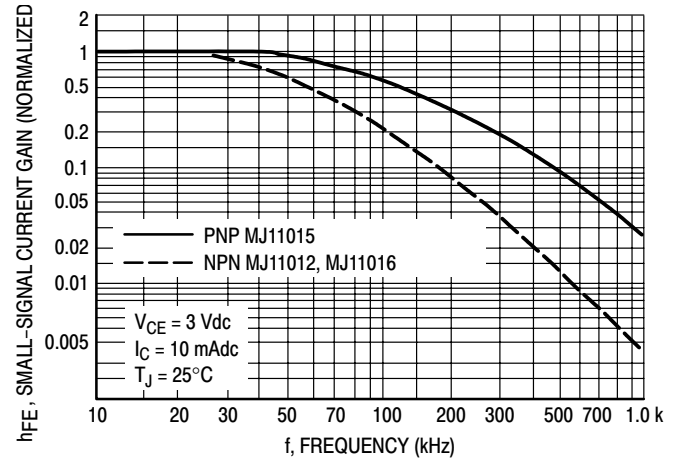


Figure 3. Small-Signal Current Gain

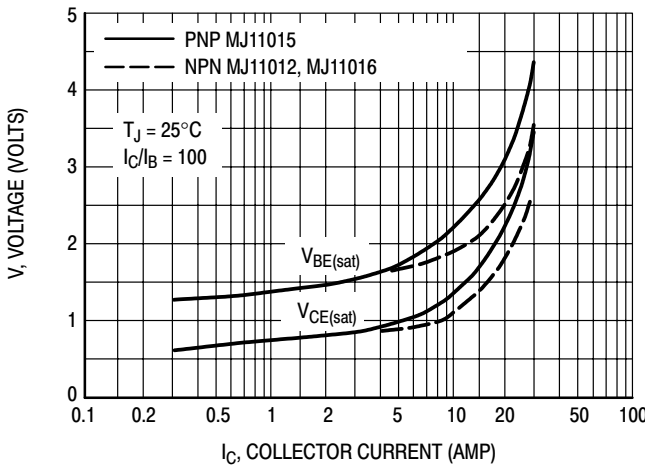


Figure 4. "On" Voltages (1)

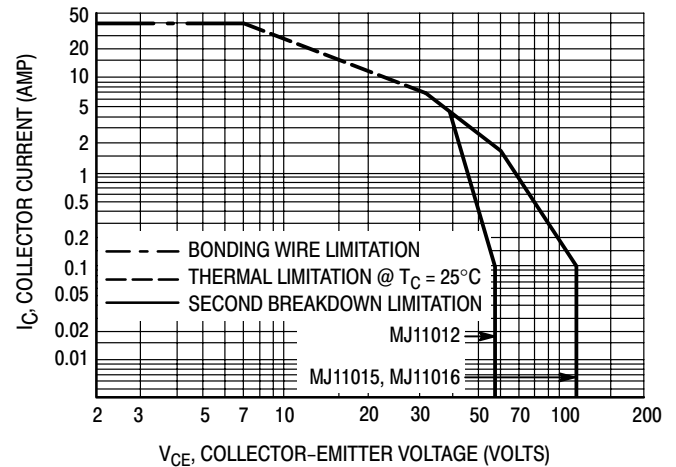


Figure 5. Active Region DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operations e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

# Complementary Darlington Silicon Power Transistors

... designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High dc Current Gain @ 10 Adc —  
 $h_{FE} = 400 \text{ Min (All Types)}$
- Collector–Emitter Sustaining Voltage  
 $V_{CEO(sus)} = 250 \text{ Vdc (Min) – MJ11022, 21}$
- Low Collector–Emitter Saturation  
 $V_{CE(sat)} = 1.0 \text{ V (Typ) @ } I_C = 5.0 \text{ A}$   
 $= 1.8 \text{ V (Typ) @ } I_C = 10 \text{ A}$
- Monolithic Construction
- 100% SOA Tested @  
 $V_{CE} = 44 \text{ V,}$   
 $I_C = 4.0 \text{ A,}$   
 $t = 250 \text{ ms.}$

## MAXIMUM RATINGS

Rating	Symbol	MJ11022 MJ11021	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	Vdc
Collector–Base Voltage	$V_{CB}$	250	Vdc
Emitter–Base Voltage	$V_{EB}$	50	Vdc
Collector Current — Continuous Peak	$I_C$	15 30	Adc
Base Current	$I_B$	0.5	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	175 1.16	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +175 -65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

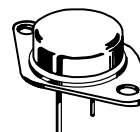
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.86	$^\circ\text{C/W}$

(1) Pulse Test: Pulse Width 5.0 ms, Duty Cycle  $\leq 10\%$ .

PNP  
**MJ11021** \*  
 NPN  
**MJ11022**

\*ON Semiconductor Preferred Device

**30 AMPERE  
 DARLINGTON  
 POWER TRANSISTORS  
 COMPLEMENTARY  
 SILICON  
 60–120 VOLTS  
 200 WATTS**



**CASE 1–07  
 TO–204AA  
 (TO–3)**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJ11021 MJ11022

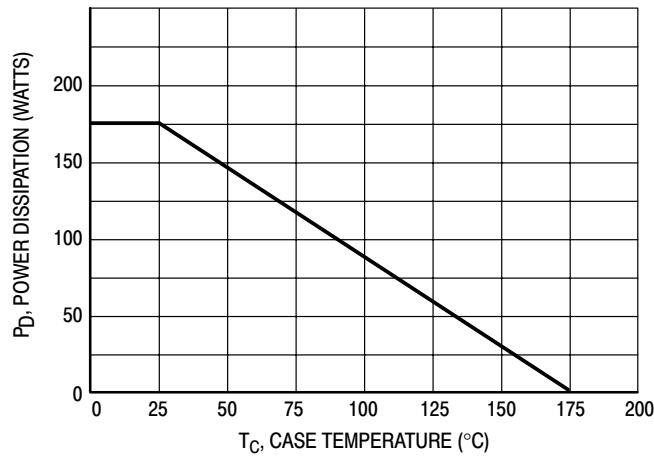


Figure 1. Power Derating

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) (I <sub>C</sub> = 0.1 Adc, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	250	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 125, I <sub>B</sub> = 0)	I <sub>CEO</sub>	—	1.0	mAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>J</sub> = 150°C)	I <sub>CEV</sub>	—	0.5 5.0	mAdc
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	2.0	mAdc

## ON CHARACTERISTICS (1)

DC Current Gain (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 5.0 Vdc) (I <sub>C</sub> = 15 Adc, V <sub>CE</sub> = 5.0 Vdc)	h <sub>FE</sub>	400 100	15,000 —	—
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 10 Adc, I <sub>B</sub> = 100 mA) (I <sub>C</sub> = 15 Adc, I <sub>B</sub> = 150 mA)	V <sub>CE(sat)</sub>	— —	2.0 3.4	Vdc
Base–Emitter On Voltage I <sub>C</sub> = 10 A, V <sub>CE</sub> = 5.0 Vdc	V <sub>BE(on)</sub>	—	2.8	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 15 Adc, I <sub>B</sub> = 150 mA)	V <sub>BE(sat)</sub>	—	3.8	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain Bandwidth Product (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 MHz)	[h <sub>fe</sub> ]	3.0	—	Mhz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	C <sub>ob</sub>	— —	400 600	pF
Small–Signal Current Gain (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 kHz)	h <sub>fe</sub>	75	—	—

## SWITCHING CHARACTERISTICS

Characteristic	Symbol	Typical		Unit
		NPN	PNP	
Delay Time	t <sub>d</sub>	150	75	ns
Rise Time	t <sub>r</sub>	1.2	0.5	μs
Storage Time	t <sub>s</sub>	4.4	2.7	μs
Fall Time	t <sub>f</sub>	10.0	2.5	μs

(V<sub>CC</sub> = 100 V, I<sub>C</sub> = 10 A, I<sub>B</sub> = 100 mA, V<sub>BE(off)</sub> = 50 V) (See Figure 2.)

(1) Pulsed Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

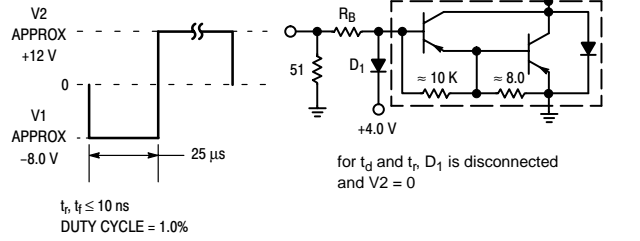
# MJ11021 MJ11022

$R_B$  and  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS

$D_1$  MUST BE FAST RECOVERY TYPE, e.g.:

1N5825 USED ABOVE  $I_B \approx 100$  mA

MSD6100 USED BELOW  $I_B \approx 100$  mA



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

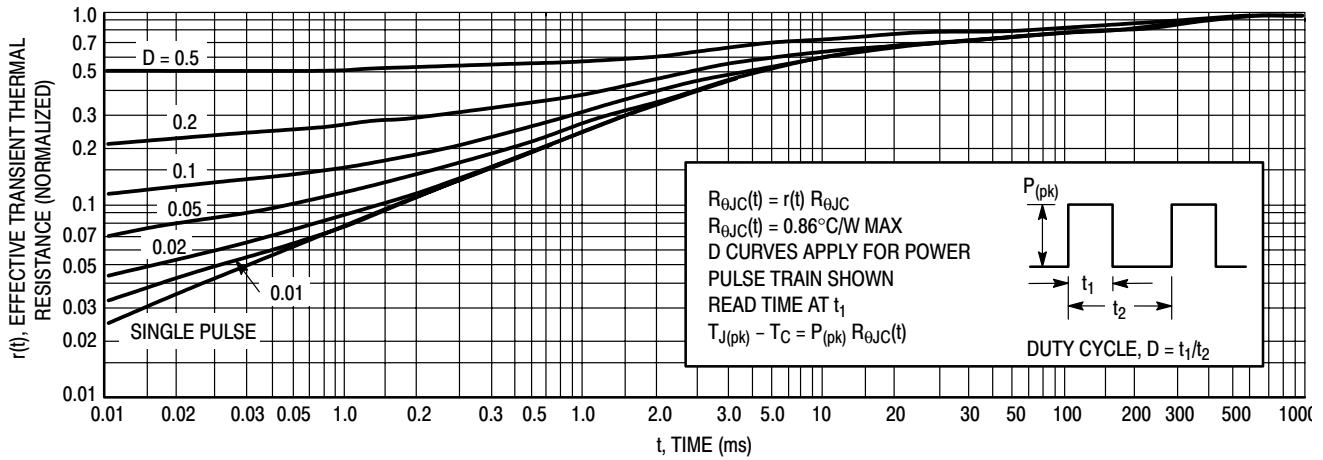


Figure 3. Thermal Response



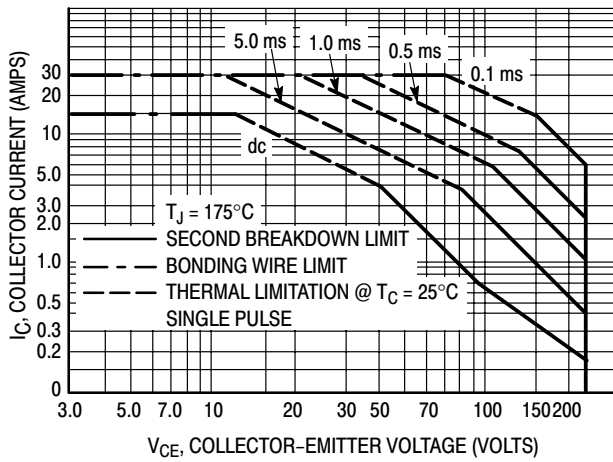


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

**FORWARD BIAS**

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on  $T_{J(pk)} = 175^\circ\text{C}$ ,  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 175^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 3. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

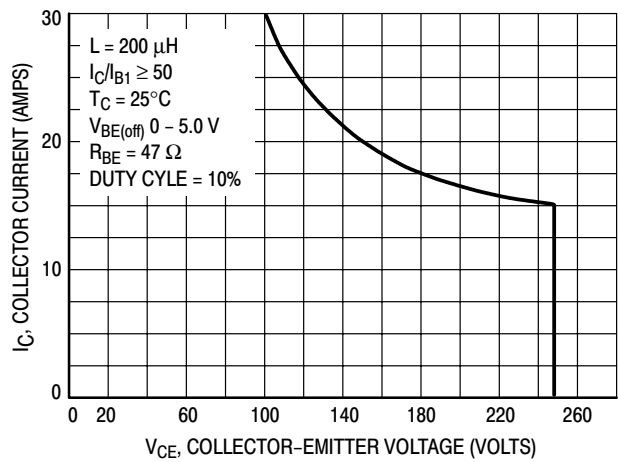


Figure 5. Maximum RBSOA, Reverse Bias Safe Operating Area

**REVERSE BIAS**

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives ROSOA characteristics.

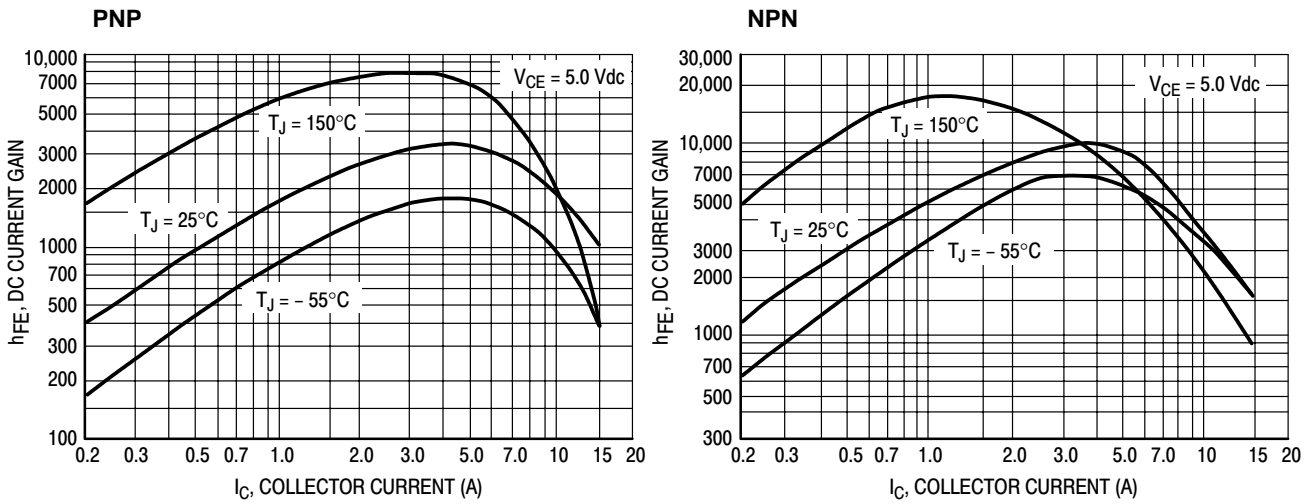


Figure 6. DC Current Gain

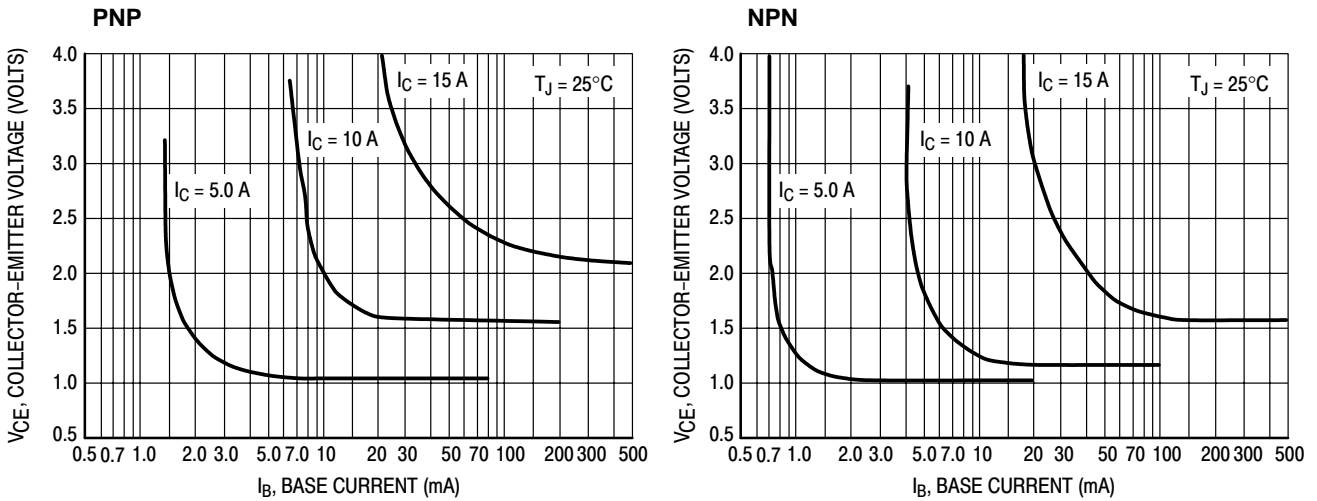


Figure 7. Collector Saturation Region

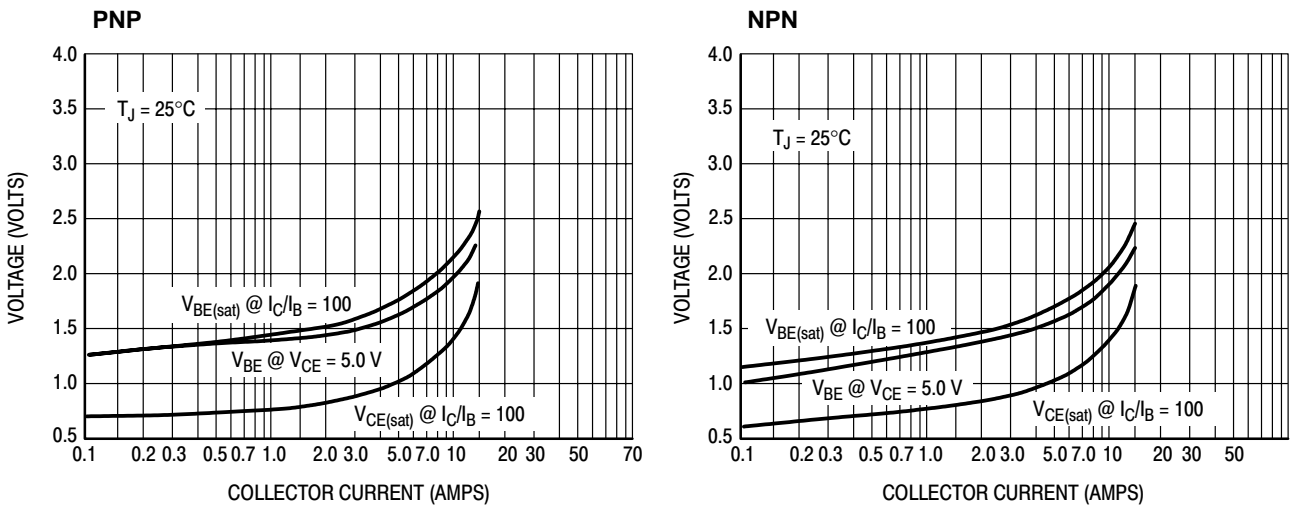


Figure 8. "On" Voltages

# High-Current Complementary Silicon Transistors

... for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain —  
 $h_{FE} = 1000$  (Min) @  $I_C = 25$  Adc  
 $h_{FE} = 400$  (Min) @  $I_C = 50$  Adc
- Curves to 100 A (Pulsed)
- Diode Protection to Rated  $I_C$
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor
- Junction Temperature to +200°C

## MAXIMUM RATINGS

Rating	Symbol	MJ11028 MJ11029	MJ11032 MJ11033	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	120	Vdc
Collector-Base Voltage	$V_{CB}$	60	120	Vdc
Emitter-Base Voltage	$V_{EB}$	5		Vdc
Collector Current — Continuous Peak	$I_C$ $I_{CM}$	50 100		Adc
Base Current — Continuous	$I_B$	2		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	$P_D$	300 1.71		Watts W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +200		°C

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Maximum Lead Temperature for Soldering Purposes for $\leq 10$ seconds	$T_L$	275	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.584	°C

**NPN**  
**MJ11028**  
**MJ11032\***  
**PNP**  
**MJ11029**  
**MJ11033\***

\*ON Semiconductor Preferred Device

**50 AMPERE  
 COMPLEMENTARY  
 SILICON  
 DARLINGTON  
 POWER TRANSISTORS  
 60-120 VOLTS  
 300 WATTS**

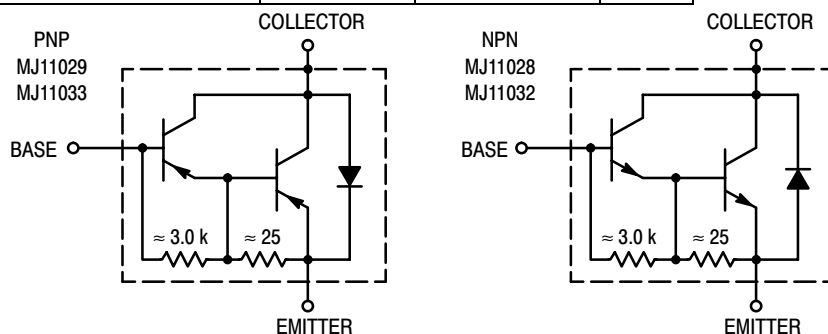
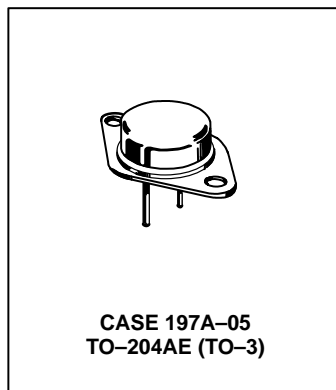


Figure 1. Darlington Circuit Schematic

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJ11028 MJ11032 MJ11029 MJ11033

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Breakdown Voltage (1) ( $I_C = 1\ 00\ \text{mA}$ , $I_B = 0$ )	MJ11028, MJ11029 MJ11032, MJ11033	$V_{(BR)CEO}$	60 120	— — Vdc
Collector–Emitter Leakage Current ( $V_{CE} = 60\ \text{Vdc}$ , $R_{BE} = 1\ \text{k}\ \Omega$ ) ( $V_{CE} = 120\ \text{Vdc}$ , $R_{BE} = 1\ \text{k}\ \Omega$ ) ( $V_{CE} = 60\ \text{Vdc}$ , $R_{BE} = 1\ \text{k}\ \Omega$ , $T_C = 150^\circ\text{C}$ ) ( $V_{CE} = 120\ \text{Vdc}$ , $R_{BE} = 1\ \text{k}\ \Omega$ , $T_C = 150^\circ\text{C}$ )	MJ11028, MJ11029 MJ11032, MJ11033 MJ11028, MJ11029 MJ11032, MJ11033	$I_{CER}$	— — — —	2 2 10 10 mAdc
Emitter Cutoff Current ( $V_{BE} = 5\ \text{Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	5 mAdc
Collector–Emitter Leakage Current ( $V_{CE} = 50\ \text{Vdc}$ , $I_B = 0$ )		$I_{CEO}$	—	2 mAdc
<b>ON CHARACTERISTICS (1)</b>				
DC Current Gain ( $I_C = 25\ \text{Adc}$ , $V_{CE} = 5\ \text{Vdc}$ ) ( $I_C = 50\ \text{Adc}$ , $V_{CE} = 5\ \text{Vdc}$ )		$h_{FE}$	1 k 400	18 k — —
Collector–Emitter Saturation Voltage ( $I_C = 25\ \text{Adc}$ , $I_B = 250\ \text{mAdc}$ ) ( $I_C = 50\ \text{Adc}$ , $I_B = 500\ \text{mAdc}$ )		$V_{CE(sat)}$	— —	2.5 3.5 Vdc
Base–Emitter Saturation Voltage ( $I_C = 25\ \text{Adc}$ , $I_B = 200\ \text{mAdc}$ ) ( $I_C = 50\ \text{Adc}$ , $I_B = 300\ \text{mAdc}$ )		$V_{BE(sat)}$	— —	3.0 4.5 Vdc

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

# MJ11028 MJ11032 MJ11029 MJ11033

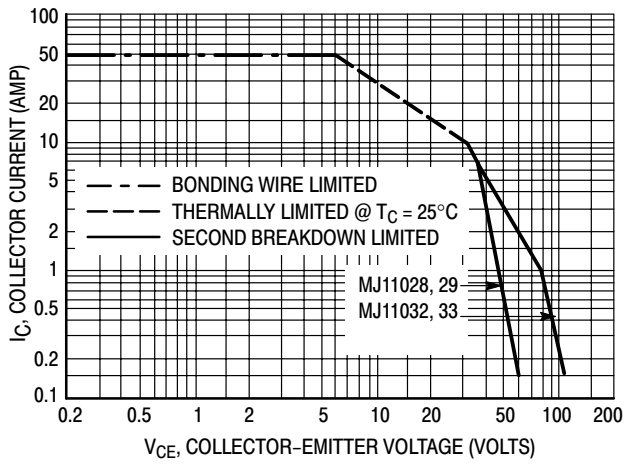


Figure 2. DC Safe Operating Area

There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

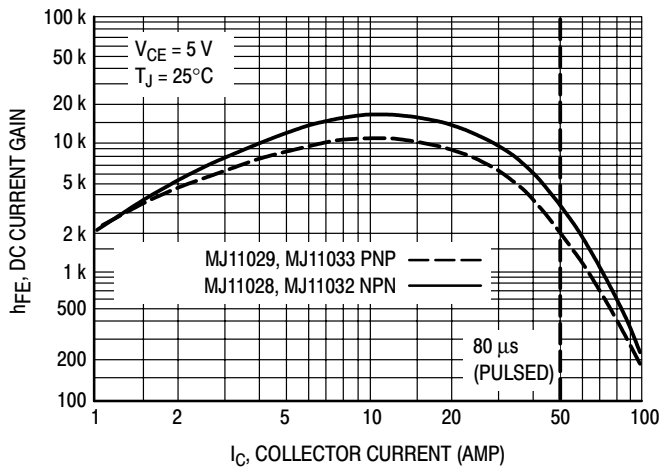


Figure 3. DC Current Gain

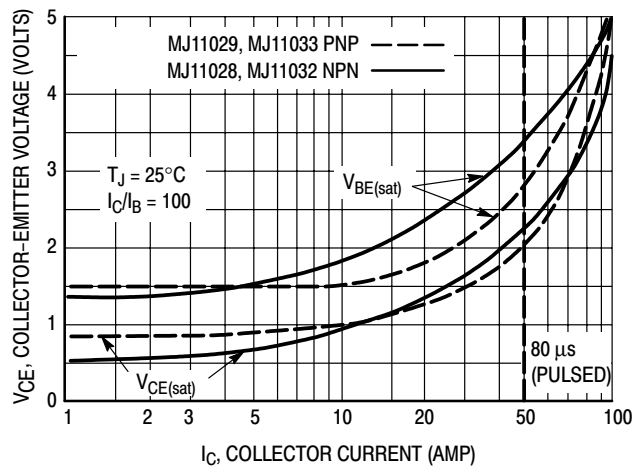


Figure 4. "On" Voltage

# High-Current Complementary Silicon Power Transistors

... designed for use in high-power amplifier and switching circuit applications,

- High Current Capability —  
 $I_C$  Continuous = 60 Amperes
- DC Current Gain —  
 $h_{FE} = 15-100 @ I_C = 50 \text{ Adc}$
- Low Collector-Emmitter Saturation Voltage —  
 $V_{CE(sat)} = 2.5 \text{ Vdc (Max) @ } I_C = 50 \text{ Adc}$

## MAXIMUM RATINGS

Rating	Symbol	MJ14001	MJ14002 MJ14003	Unit
Collector-Emmitter Voltage	$V_{CEO}$	60	80	Vdc
Collector Base Voltage	$V_{CBO}$	60	80	Vdc
Emmitter-Base Voltage	$V_{EBO}$	5		Vdc
Collector Current — Continuous	$I_C$	60		Adc
Base Current — Continuous	$I_B$	15		Adc
Emmitter Current — Continuous	$I_E$	75		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300	17	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.584	$^\circ\text{C/W}$

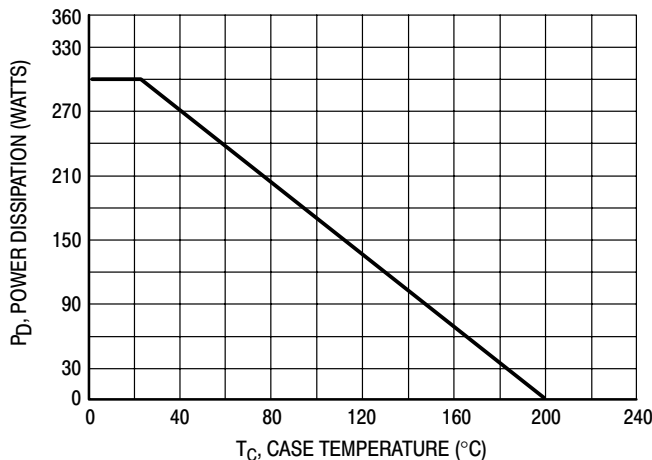


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**NPN**  
**MJ14002\***  
**PNP**  
**MJ14001**  
**MJ14003\***

\*ON Semiconductor Preferred Device

**60 AMPERES**  
**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**60-80 VOLTS**  
**300 WATTS**

**CASE 197A-05**  
**TO-204AE (TO-3)**

# MJ14002 MJ14001 MJ14003

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	MJ14001 MJ14002, MJ14003	$V_{CEO(sus)}$	60 80	— — Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) MJ14003	MJ14001 MJ14002, MJ14003	$I_{CEO}$	— —	1.0 1.0 mA
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ V}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ V}$ ) MJ14003	MJ14001 MJ14002, MJ14003	$I_{CEX}$	— —	1.0 1.0 mA
Collector Cutoff Current ( $V_{CB} = 60\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ ) MJ14003	MJ14001 MJ14002, MJ14003	$I_{CBO}$	— —	1.0 1.0 mA
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	1.0 mA

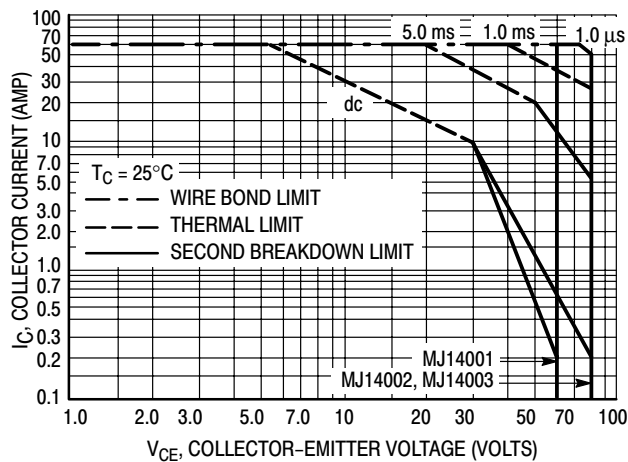
## ON CHARACTERISTICS

DC Current Gain (1) ( $I_C = 25\text{ Adc}$ , $V_{CE} = 3.0\text{ V}$ ) ( $I_C = 50\text{ Adc}$ , $V_{CE} = 3.0\text{ V}$ ) ( $I_C = 60\text{ Adc}$ , $V_{CE} = 3.0\text{ V}$ )	$h_{FE}$	30 15 5	— 100 —	—
Collector–Emitter Saturation Voltage (1) ( $I_C = 25\text{ Adc}$ , $I_B = 2.5\text{ Adc}$ ) ( $I_C = 50\text{ Adc}$ , $I_B = 5.0\text{ Adc}$ ) ( $I_C = 60\text{ Adc}$ , $I_B = 12\text{ Adc}$ )	$V_{CE(sat)}$	— — —	1 2.5 3	Vdc
Base–Emitter Saturation Voltage (1) ( $I_C = 25\text{ Adc}$ , $I_B = 2.5\text{ Adc}$ ) ( $I_C = 50\text{ Adc}$ , $I_B = 5.0\text{ Adc}$ ) ( $I_C = 60\text{ Adc}$ , $I_B = 12\text{ Adc}$ )	$V_{BE(sat)}$	— — —	2 3 4	Vdc

## DYNAMIC CHARACTERISTICS

Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	—	2000	pF
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(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .



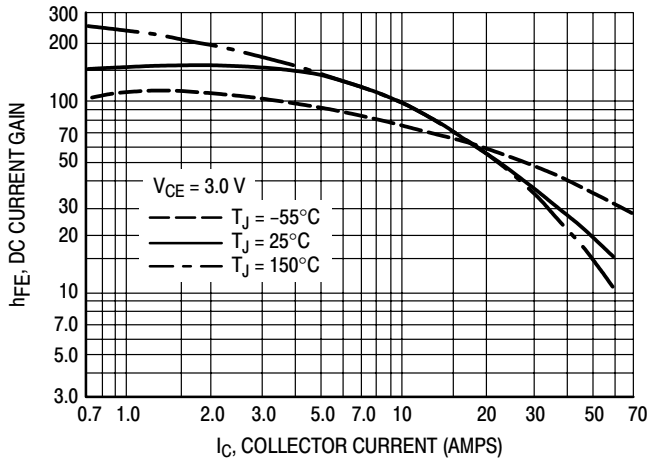
**Figure 2. Maximum Rated Forward Biased Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

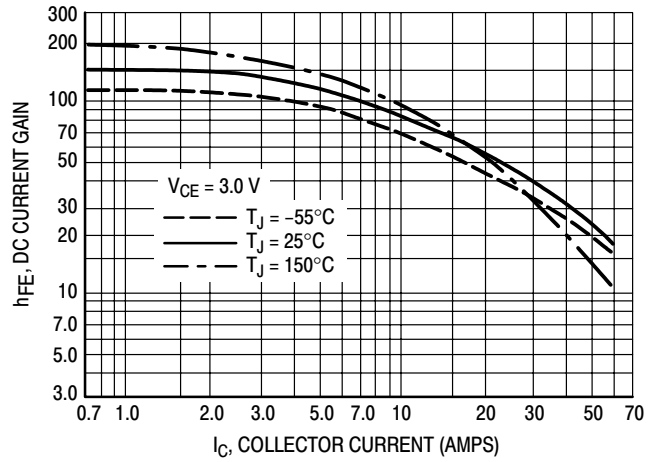
TYPICAL ELECTRICAL CHARACTERISTICS

**NPN  
MJ14002**

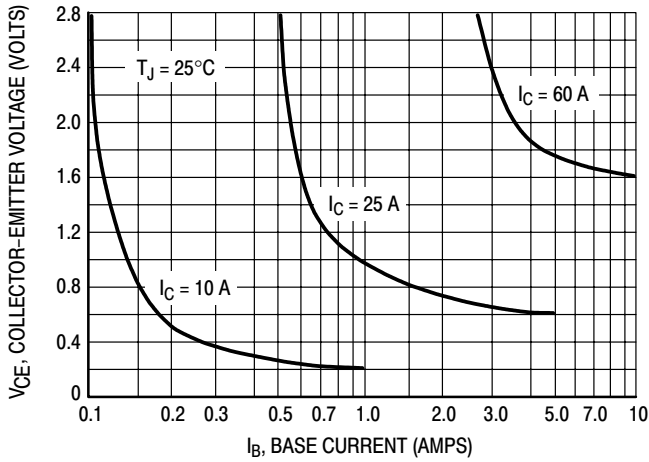


**Figure 3. DC Current Gain**

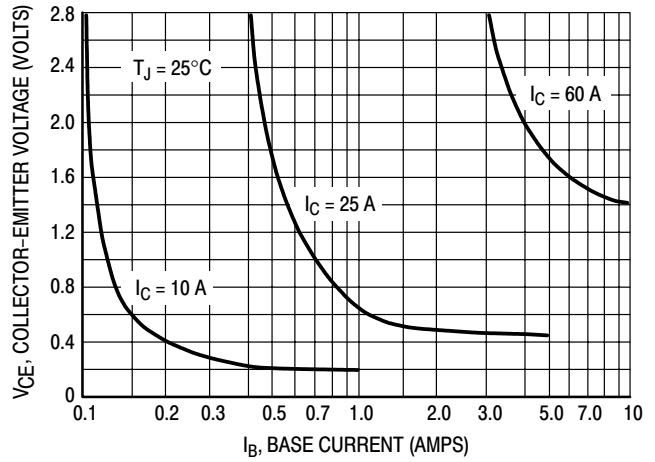
**PNP  
MJ14001, MJ14003**



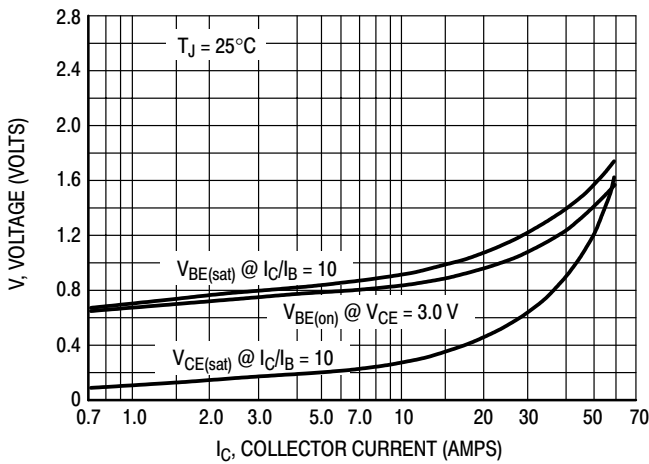
**Figure 4. DC Current Gain**



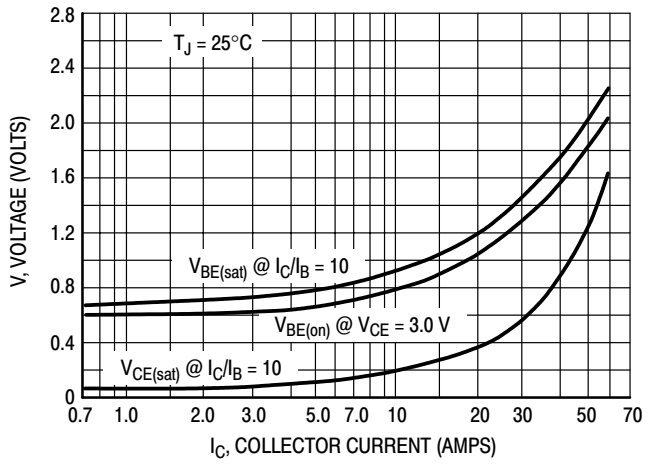
**Figure 5. Collector Saturation Region**



**Figure 6. Collector Saturation Region**



**Figure 7. "On" Voltages**



**Figure 8. "On" Voltages**



# MJ14002 MJ14001 MJ14003

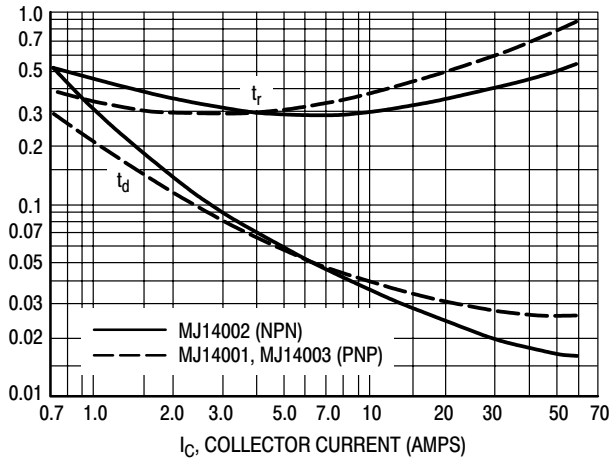


Figure 9. Turn-On Switching Times

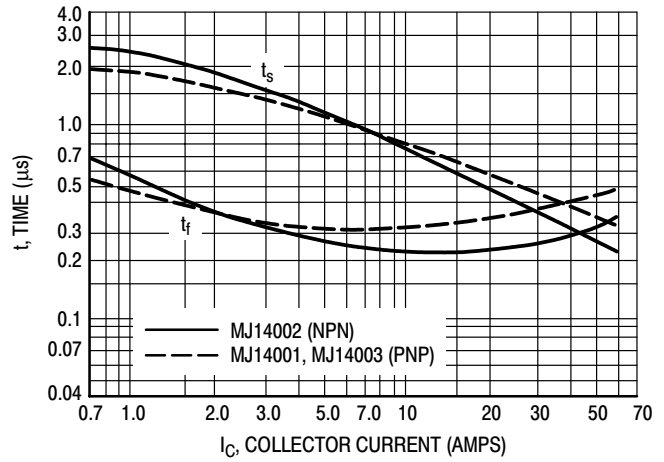


Figure 10. Turn-Off Switching Times

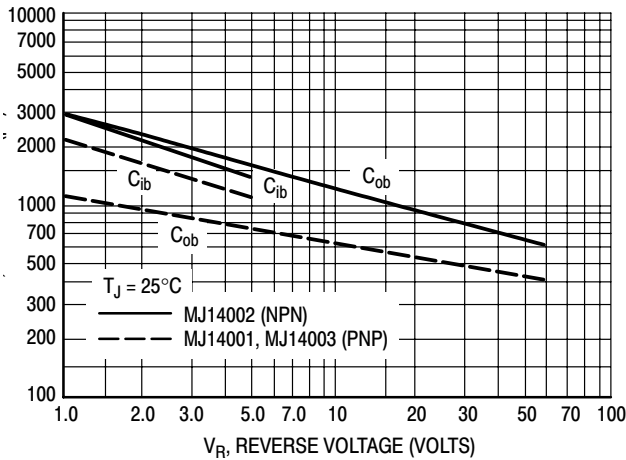
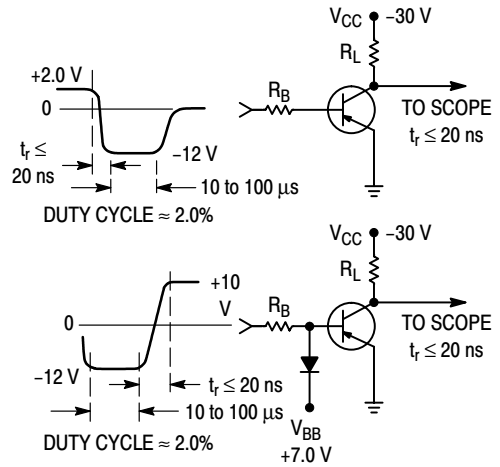


Figure 11. Capacitance Variation



FOR CURVES OF FIGURES 3 & 6,  $R_B$  &  $R_L$  ARE VARIED. INPUT LEVELS ARE APPROXIMATELY AS SHOWN. FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 12. Switching Test Circuit

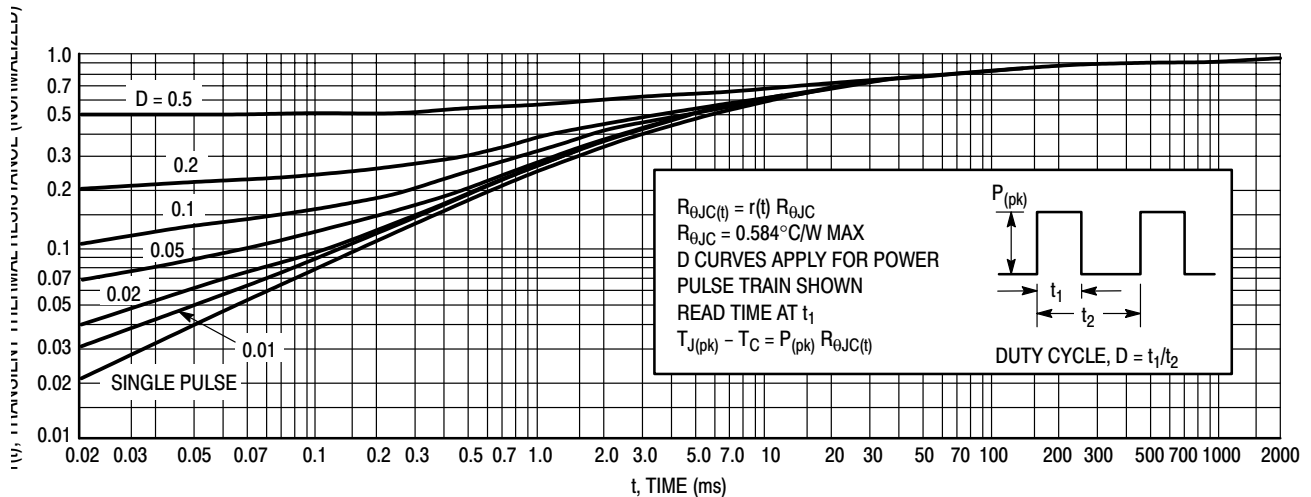


Figure 13. Thermal Response

# Complementary Silicon Power Transistors

The MJ15001 and MJ15002 are EpiBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —  
200 W @ 40 V  
50 W @ 100 V
- For Low Distortion Complementary Designs
- High DC Current Gain —  
 $h_{FE} = 25$  (Min) @  $I_C = 4$  Adc

## MAXIMUM RATINGS

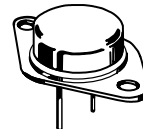
Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	140	Vdc
Collector–Base Voltage	$V_{CBO}$	140	Vdc
Emitter–Base Voltage	$V_{EBO}$	5	Vdc
Collector Current — Continuous	$I_C$	15	Adc
Base Current — Continuous	$I_B$	5	Adc
Emitter Current — Continuous	$I_E$	20	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.14	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for $\leq 10$ seconds	$T_L$	265	$^\circ\text{C}$

**NPN  
MJ15001  
PNP  
MJ15002**

**15 AMPERE  
POWER TRANSISTORS  
COMPLEMENTARY  
SILICON  
140 VOLTS  
200 WATTS**



**CASE 1-07  
TO-204AA  
(TO-3)**

# MJ15001 MJ15002

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	140	—	Vdc
Collector Cutoff Current ( $V_{CE} = 140\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 140\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	— —	100 2	$\mu\text{Adc}$ mAdc
Collector Cutoff Current ( $V_{CE} = 140\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	250	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	100	$\mu\text{Adc}$

## SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 40\text{ Vdc}$ , $t = 1\text{ s}$ (non-repetitive)) ( $V_{CE} = 100\text{ Vdc}$ , $t = 1\text{ s}$ (non-repetitive))	$I_{S/b}$	5 0.5	— —	Adc
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## ON CHARACTERISTICS

DC Current Gain ( $I_C = 4\text{ Adc}$ , $V_{CE} = 2\text{ Vdc}$ )	$h_{FE}$	25	150	—
Collector–Emitter Saturation Voltage ( $I_C = 4\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )	$V_{CE(sat)}$	—	1	Vdc
Base–Emitter On Voltage ( $I_C = 4\text{ Adc}$ , $V_{CE} = 2\text{ Vdc}$ )	$V_{BE(on)}$	—	2	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 0.5\text{ MHz}$ )	$f_T$	2	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ )	$C_{ob}$	—	1000	pF

(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

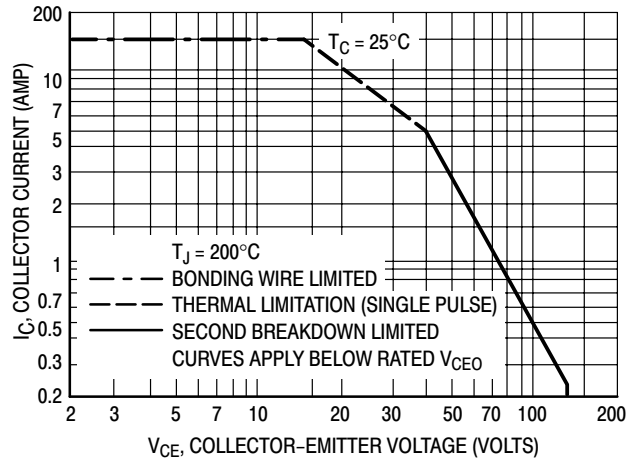


Figure 1. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on  $T_J(pk) = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# MJ15001 MJ15002

## TYPICAL CHARACTERISTICS

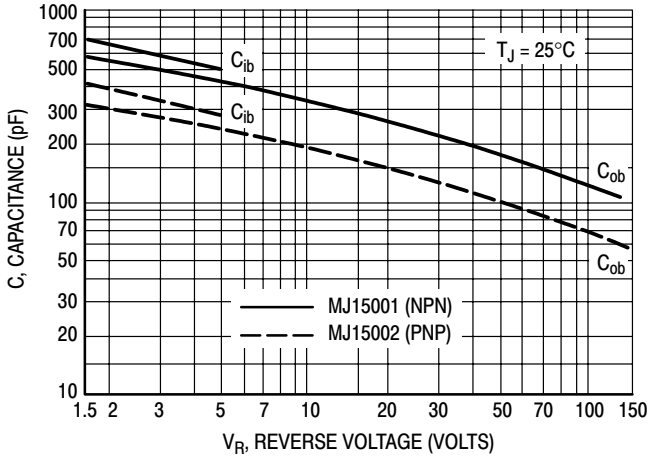


Figure 2. Capacitances

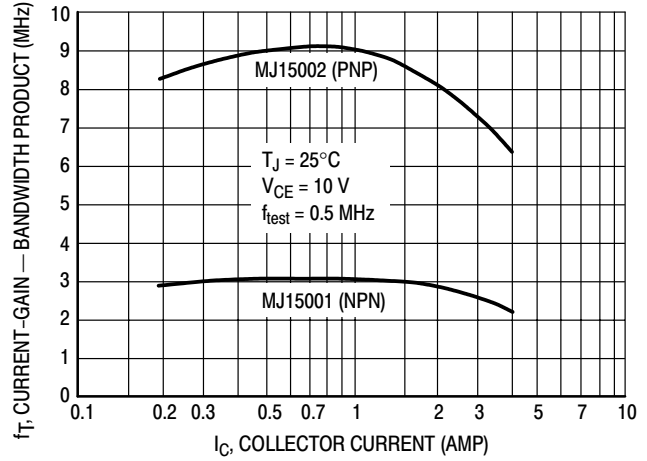


Figure 3. Current-Gain — Bandwidth Product

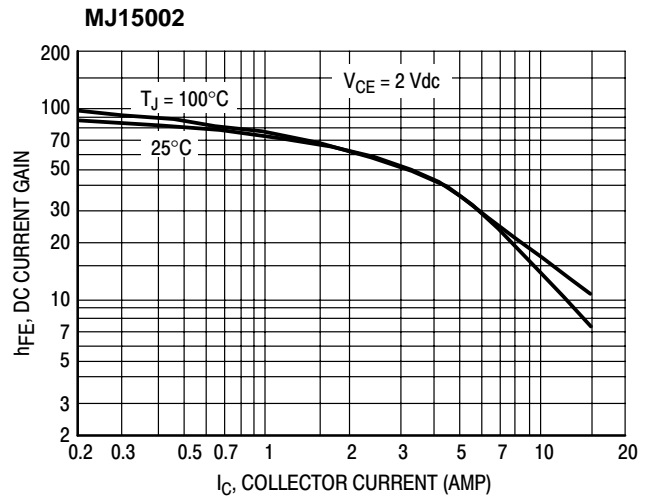
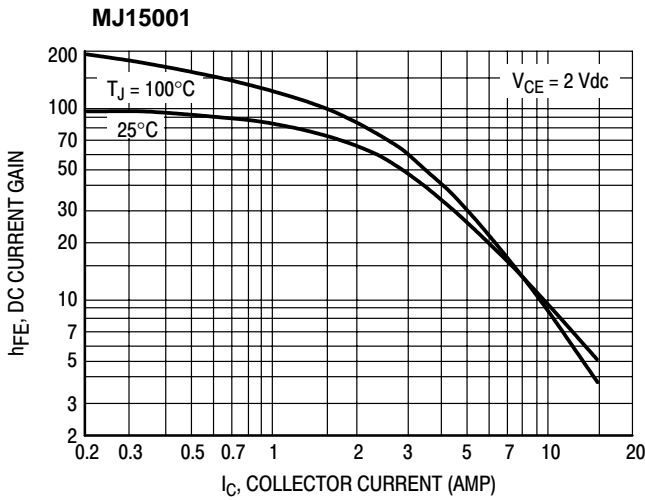


Figure 4. DC Current Gain

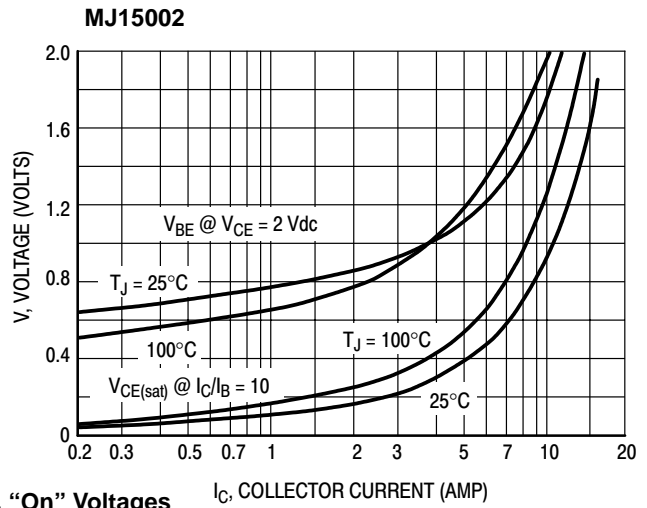
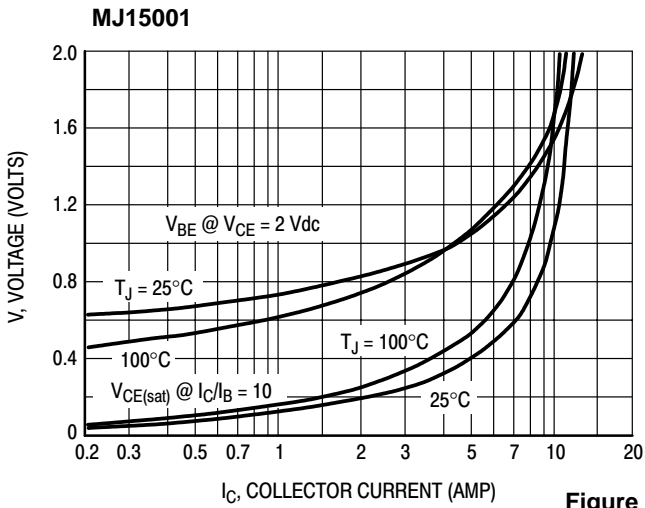


Figure 5. "On" Voltages

# Complementary Silicon Power Transistors

The MJ15003 and MJ15004 are PowerBase™ power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —  
250 W @ 50 V
- For Low Distortion Complementary Designs
- High DC Current Gain —  
 $h_{FE} = 25$  (Min) @  $I_C = 5$  Adc

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	140	Vdc
Collector–Base Voltage	$V_{CBO}$	140	Vdc
Emitter–Base Voltage	$V_{EBO}$	5	Vdc
Collector Current — Continuous	$I_C$	20	Adc
Base Current — Continuous	$I_B$	5	Adc
Emitter Current — Continuous	$I_E$	25	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	250 1.43	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

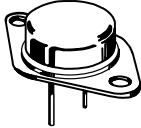
## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for $\leq 10$ seconds	$T_L$	265	$^\circ\text{C}$

**NPN**  
**MJ15003\***  
**PNP**  
**MJ15004\***

\*ON Semiconductor Preferred Device

**20 AMPERE**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**140 VOLTS**  
**250 WATTS**



**CASE 1-07**  
**TO-204AA**  
**(TO-3)**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJ15003 MJ15004

\*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector Emitter Sustaining Voltage (1) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	$V_{CE(sus)}$	140	—	Vdc
Collector Cutoff Current ( $V_{CE} = 140\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 140\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	—	100 2	$\mu\text{Adc}$ mAdc
Collector Cutoff Current ( $V_{CE} = 140\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	250	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	100	$\mu\text{Adc}$

## SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 50\text{ Vdc}$ , $t = 1\text{ s}$ (non repetitive)) ( $V_{CE} = 100\text{ Vdc}$ , $t = 1\text{ s}$ (non repetitive))	$I_{S/b}$	5 1	— —	Adc
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## ON CHARACTERISTICS

DC Current Gain ( $I_C = 5\text{ Adc}$ , $V_{CE} = 2\text{ Vdc}$ )	$h_{FE}$	25	150	
Collector Emitter Saturation Voltage ( $I_C = 5\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ )	$V_{CE(sat)}$	—	1	Vdc
Base Emitter On Voltage ( $I_C = 5\text{ Adc}$ , $V_{CE} = 2\text{ Vdc}$ )	$V_{BE(on)}$	—	2	Vdc

## DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 0.5\text{ MHz}$ )	$f_T$	2	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ )	$C_{ob}$	—	1000	pF

(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

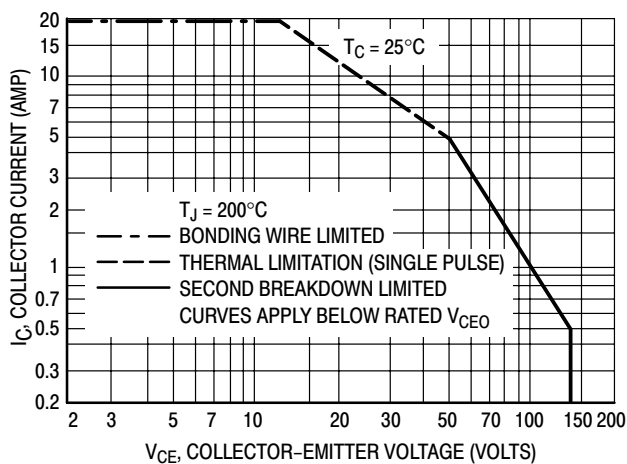


Figure 1. Active-Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# Complementary Silicon Power Transistors

The MJ15011 and MJ15012 are PowerBase power transistors designed for high-power audio, disk head positioners, and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters or inverters.

- High Safe Operating Area (100% Tested)  
1.2 A @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage  
 $h_{FE} = 20$  (Min) @ 2 A, 2 V  
 $V_{CE(sat)} = 2.5$  V (Max) @  $I_C = 4$  A,  $I_B = 0.4$  A
- For Low Distortion Complementary Designs

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	Vdc
Collector–Emitter Voltage	$V_{CEX}$	250	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
Collector Current — Continuous	$I_C$	10	Adc
— Peak (1)	$I_{CM}$	15	
Base Current — Continuous	$I_B$	2	Adc
— Peak (1)	$I_{BM}$	5	
Emitter Current — Continuous	$I_E$	12	Adc
— Peak (1)	$I_{EM}$	20	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.14	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

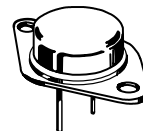
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes	$T_L$	265	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq 10\%$ .

**NPN**  
**MJ15011\***  
**PNP**  
**MJ15012\***

\*ON Semiconductor Preferred Device

**10 AMPERE**  
**COMPLEMENTARY**  
**POWER TRANSISTORS**  
**250 VOLTS**  
**200 WATTS**



**CASE 1-07**  
**TO-204AA**  
**(TO-3)**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJ15011 MJ15012

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Breakdown Voltage (1) ( $I_C = 100\text{ mA}$ )	$V_{(BR)CEO}$	250	—	Vdc
Collector Cutoff Current ( $V_{CE} = 200\text{ Vdc}$ )	$I_{CEO}$	—	1	mAdc
Collector Cutoff Current ( $V_{CE} = 250\text{ Vdc}$ , $V_{BE(off)} = 15\text{ Vdc}$ )	$I_{CEX}$	—	500	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ )	$I_{EBO}$	—	500	$\mu\text{Adc}$

### ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 2\text{ Adc}$ , $V_{CE} = 2\text{ Vdc}$ ) ( $I_C = 4\text{ Adc}$ , $V_{CE} = 2\text{ Vdc}$ )	$h_{FE}$	20 5	100 —	—
Collector–Emitter Saturation Voltage ( $I_C = 2\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ ) ( $I_C = 4\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )	$V_{CE(sat)}$	— —	0.8 2.5	Vdc
Base–Emitter On Voltage ( $I_C = 4\text{ Adc}$ , $V_{CE} = 2\text{ Vdc}$ )	$V_{BE(on)}$	—	2	Vdc

### DYNAMIC CHARACTERISTICS

Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$C_{ob}$	—	750	pF
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### SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 40\text{ Vdc}$ , $t = 0.5\text{ s}$ ) ( $V_{CE} = 100\text{ Vdc}$ , $t = 0.5\text{ s}$ )	$I_{S/b}$	5 1.4	— —	Adc
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(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

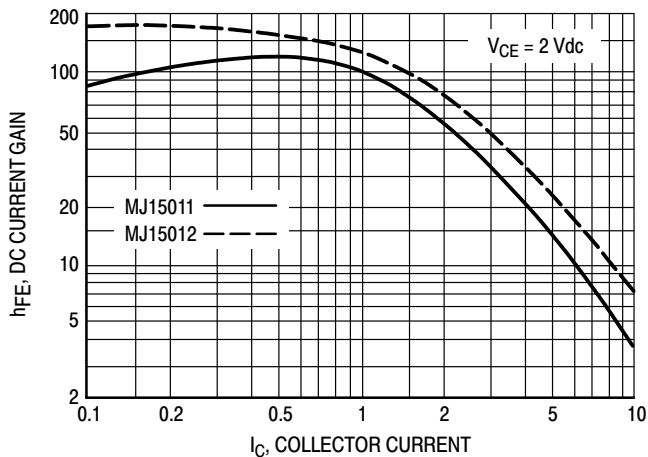


Figure 2. DC Current Gain

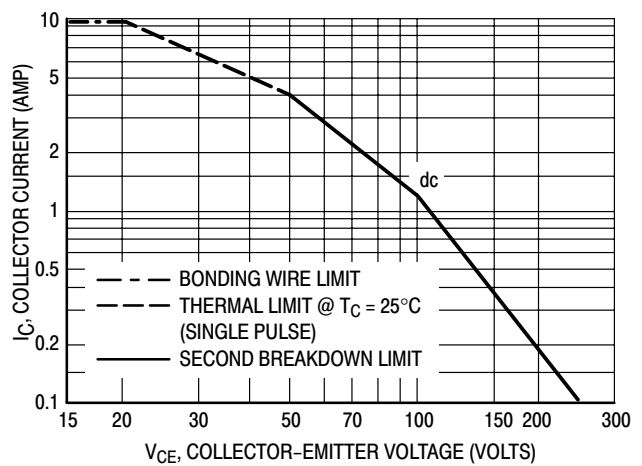


Figure 3. Active Region Safe Operating Area



# Complementary Silicon Power Transistors

... designed for use as high frequency drivers in Audio Amplifiers.

- High Gain Complementary Silicon Power Transistors
- Safe Operating Area 100% Tested 50 V, 3.0 A, 1.0 Sec.
- Excellent Frequency Response —  
 $f_T = 20 \text{ MHz min.}$

## MAXIMUM RATINGS

Rating	Symbol	MJ15020 MJ15021	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	Vdc
Collector–Base Voltage	$V_{CBO}$	250	Vdc
Emitter–Base Voltage	$V_{EBO}$	7.0	Vdc
Collector Current — Continuous	$I_C$	4.0	Adc
Base Current — Continuous	$I_B$	2.0	Adc
Emitter Current — Continuous	$I_E$	6.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	150 0.86	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	$^\circ\text{C/W}$

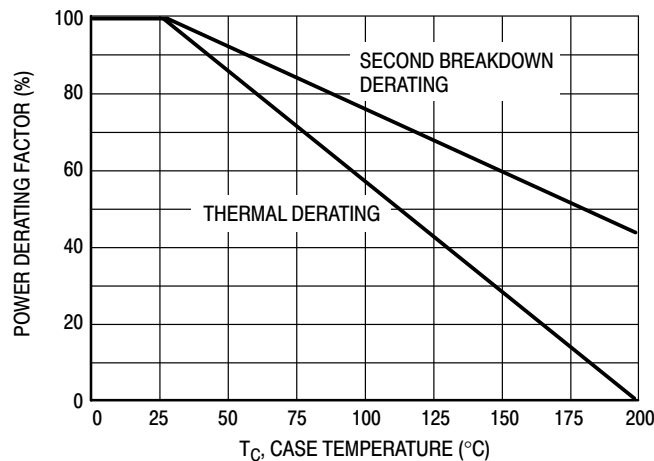
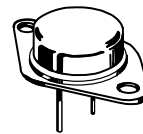


Figure 1. Power Derating

**NPN** \*  
**MJ15020** \*  
**PNP** \*  
**MJ15021**

\*ON Semiconductor Preferred Device

**4.0 AMPERES  
 COMPLEMENTARY  
 SILICON  
 POWER TRANSISTORS  
 200 AND 250 VOLTS  
 150 WATTS**



**CASE 1-07  
 TO-204AA  
 (TO-3)**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJ15020 MJ15021

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	250	—	Vdc
Collector Cutoff Current ( $V_{CE} = 200\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	500	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = 7.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	500	$\mu\text{Adc}$
<b>SECOND BREAKDOWN</b>				
Second Breakdown Collector Current with Base Forward–Biased ( $V_{CE} = 50\text{ Vdc}$ , $t = 0.5\text{ s}$ (non–repetitive))	$I_{S/b}$	3.0	—	Adc
<b>ON CHARACTERISTICS (1)</b>				
DC Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 4.0\text{ V}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ V}$ )	$h_{FE}$	30 10	— —	
Collector–Emitter Saturation Voltage ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )	$V_{CE(sat)}$	—	1.0	Vdc
Base–Emitter on Voltage ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	2.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain — Bandwidth Product ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	20	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $F_{test} = 1.0\text{ MHz}$ )	$C_{ob}$	—	500	pF

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$

## TYPICAL DYNAMIC CHARACTERISTICS

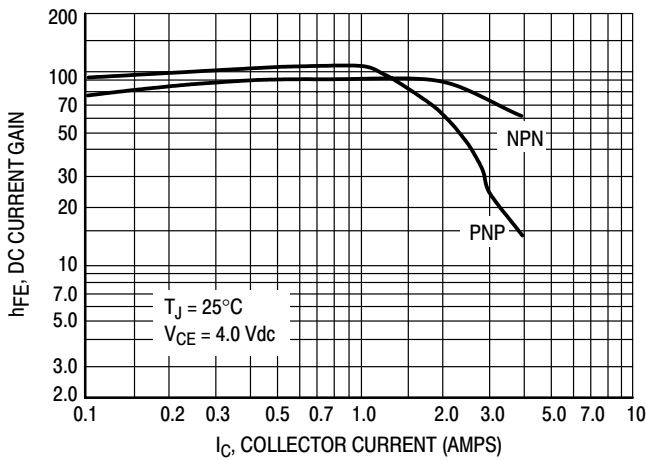


Figure 2. DC Current Gain

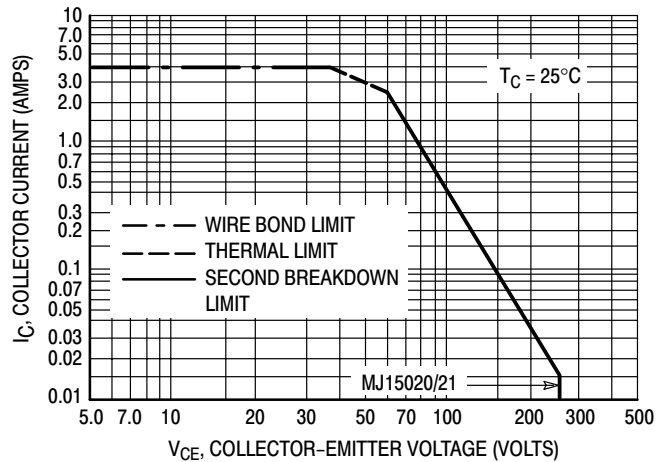


Figure 3. Maximum Rated Forward Biased Safe Operating Area

## Silicon Power Transistors

The MJ15022 and MJ15024 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —  
2 A @ 80 V
- High DC Current Gain —  
 $h_{FE} = 15$  (Min) @  $I_C = 8$  Adc

### MAXIMUM RATINGS

Rating	Symbol	MJ15022	MJ15024	Unit
Collector–Emitter Voltage	$V_{CEO}$	200	250	Vdc
Collector–Base Voltage	$V_{CBO}$	350	400	Vdc
Emitter–Base Voltage	$V_{EBO}$	5		Vdc
Collector–Emitter Voltage	$V_{CEX}$	400		Vdc
Collector Current — Continuous Peak (1)	$I_C$	16 30		Adc
Base Current — Continuous	$I_B$	5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	250 1.43		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +200		$^\circ\text{C}$

### THERMAL CHARACTERISTICS

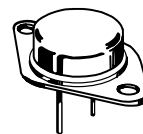
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	$^\circ\text{C}/\text{W}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq$  10%.

**NPN**  
**MJ15022**  
**MJ15024 \***

\*ON Semiconductor Preferred Device

**16 AMPERE**  
**SILICON**  
**POWER TRANSISTORS**  
**200 AND 250 VOLTS**  
**250 WATTS**



**CASE 1–07**  
**TO–204AA**  
**(TO–3)**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJ15022 MJ15024

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	MJ15022 MJ15024	$V_{CE(sus)}$	200 250	—
Collector Cutoff Current ( $V_{CE} = 200\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 250\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ )	MJ15022 MJ15024	$I_{CEX}$	— —	250 250
Collector Cutoff Current ( $V_{CE} = 150\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 200\text{ vdc}$ , $I_B = 0$ )	MJ15022 MJ15024	$I_{CEO}$	— —	500 500
Emitter Cutoff Current ( $V_{CE} = 5\text{ Vdc}$ , $I_B = 0$ )		$I_{EBO}$	—	500
<b>SECOND BREAKDOWN</b>				
Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 50\text{ Vdc}$ , $t = 0.5\text{ s}$ (non-repetitive)) ( $V_{CE} = 80\text{ Vdc}$ , $t = 0.5\text{ s}$ (non-repetitive))		$I_{S/b}$	5 2	— —
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = 8\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 16\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )		$h_{FE}$	15 5	60 —
Collector–Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.8\text{ Adc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 3.2\text{ Adc}$ )		$V_{CE(sat)}$	— —	1.4 4.0
Base–Emitter On Voltage ( $I_C = 8\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )		$V_{BE(on)}$	—	2.2
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain — Bandwidth Product ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )		$f_T$	4	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ )		$C_{ob}$	—	500

(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

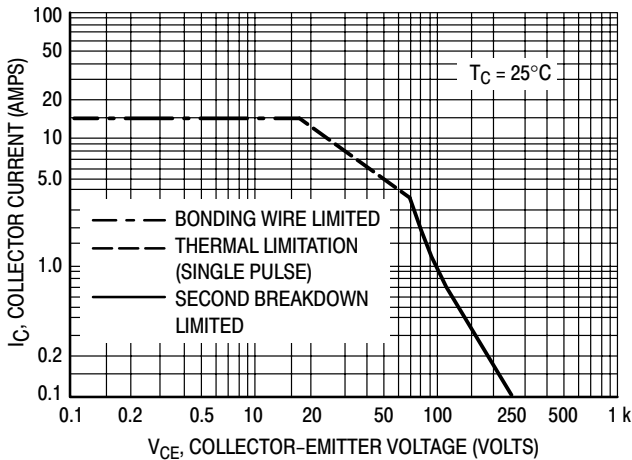


Figure 1. Active–Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values  $I_{on}$  than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

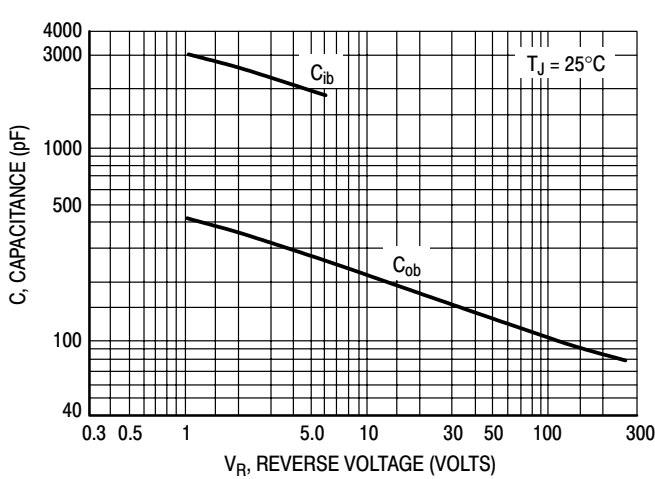


Figure 2. Capacitances

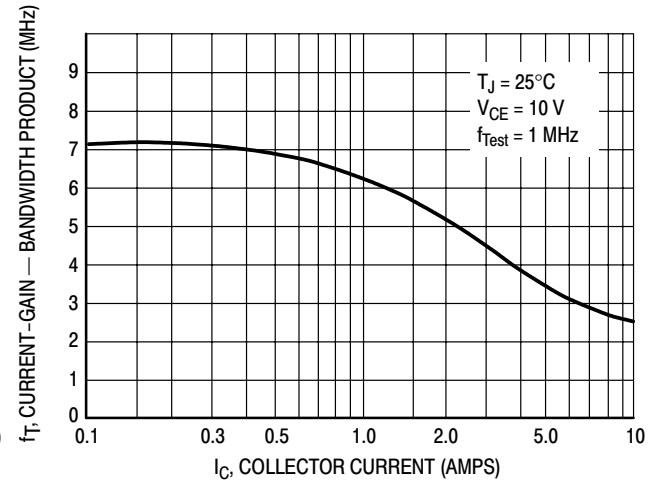


Figure 3. Current-Gain — Bandwidth Product

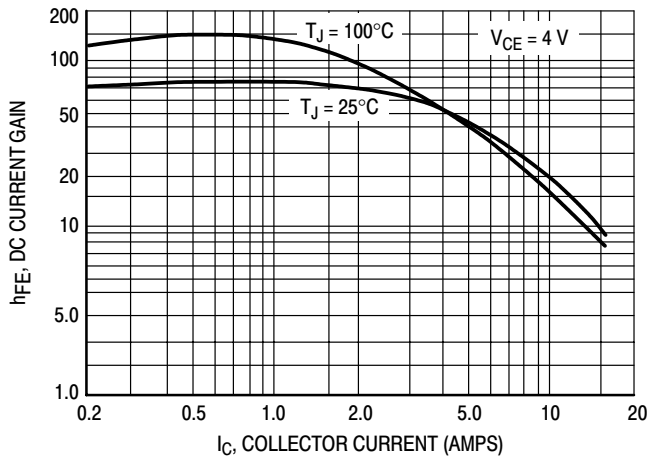


Figure 4. DC Current Gain

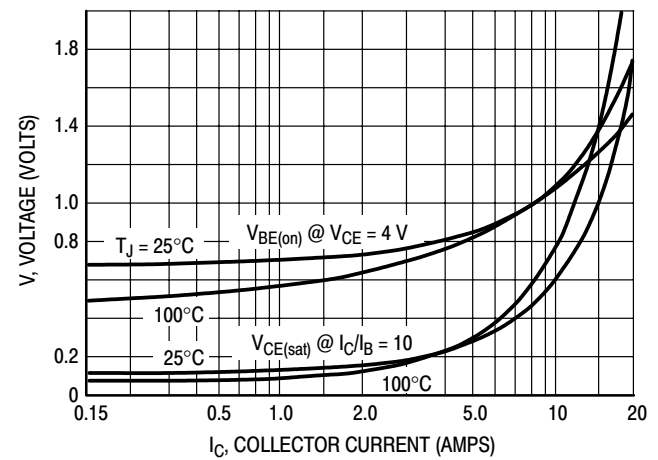


Figure 5. "On" Voltage

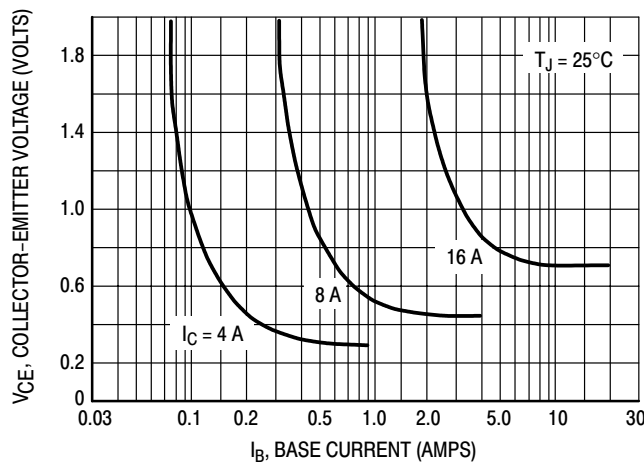


Figure 6. Collector Saturation Region

## Silicon Power Transistors

The MJ15023 and MJ15025 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —  
2 A @ 80 V
- High DC Current Gain —  
 $h_{FE} = 15$  (Min) @  $I_C = 8$  Adc

### MAXIMUM RATINGS

Rating	Symbol	MJ15023	MJ15025	Unit
Collector–Emitter Voltage	$V_{CEO}$	200	250	Vdc
Collector–Base Voltage	$V_{CBO}$	350	400	Vdc
Emitter–Base Voltage	$V_{EBO}$	5		Vdc
Collector–Emitter Voltage	$V_{CEX}$	400		Vdc
Collector Current — Continuous Peak (1)	$I_C$	16 30		Adc
Base Current — Continuous	$I_B$	5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	250 1.43		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +200		$^\circ\text{C}$

### THERMAL CHARACTERISTICS

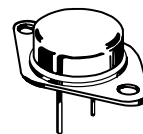
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	$^\circ\text{C/W}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq 10\%$ .

PNP  
**MJ15023**  
**MJ15025 \***

\*ON Semiconductor Preferred Device

16 AMPERE  
SILICON  
POWER TRANSISTORS  
200 AND 250 VOLTS  
250 WATTS



CASE 1–07  
TO–204AA  
(TO–3)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJ15023 MJ15025

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (1) ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	MJ15023 MJ15025	$V_{CEO(sus)}$	200 250	— —	
Collector Cutoff Current ( $V_{CE} = 200\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 250\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ )	MJ15023 MJ15025	$I_{CEX}$	— —	250 250	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 150\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 200\text{ Vdc}$ , $I_B = 0$ )	MJ15023 MJ15025	$I_{CEO}$	— —	500 500	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{CE} = 5\text{ Vdc}$ , $I_B = 0$ )	Both	$I_{EBO}$	—	500	$\mu\text{Adc}$

## SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 50\text{ Vdc}$ , $t = 0.5\text{ s}$ (non-repetitive)) ( $V_{CE} = 80\text{ Vdc}$ , $t = 0.5\text{ s}$ (non-repetitive))		$I_{S/b}$	5 2	— —	Adc
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## ON CHARACTERISTICS

DC Current Gain ( $I_C = 8\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 16\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )		$h_{FE}$	15 5	60 —	—
Collector–Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.8\text{ Adc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 3.2\text{ Adc}$ )		$V_{CE(sat)}$	—	1.4 4.0	Vdc
Base–Emitter On Voltage ( $I_C = 8\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )		$V_{BE(on)}$	—	2.2	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )		$f_T$	4	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ )		$C_{ob}$	—	600	pF

(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

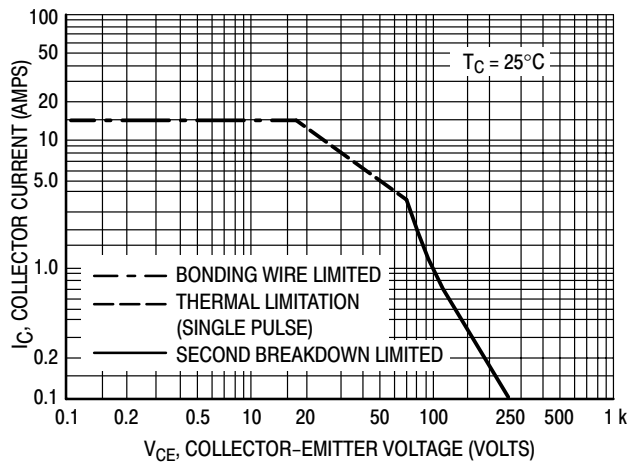


Figure 1. Active–Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

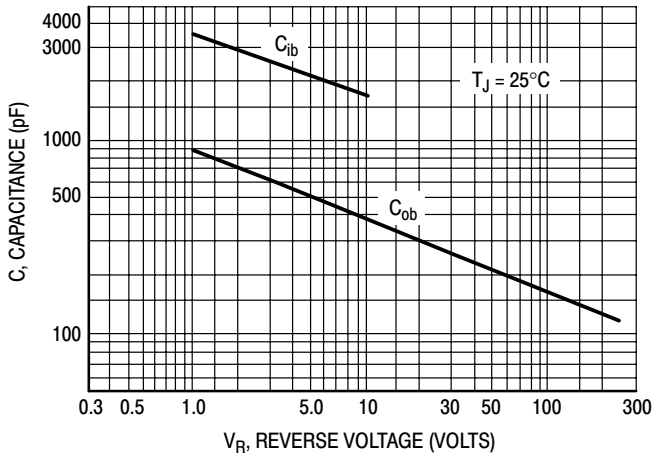


Figure 2. Capacitances

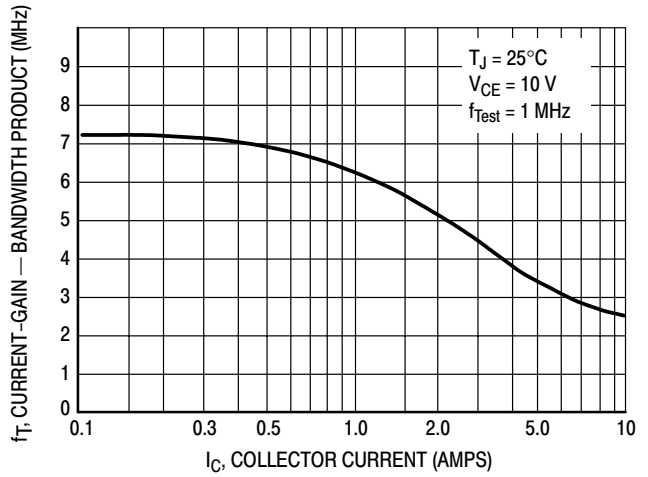


Figure 3. Current-Gain — Bandwidth Product

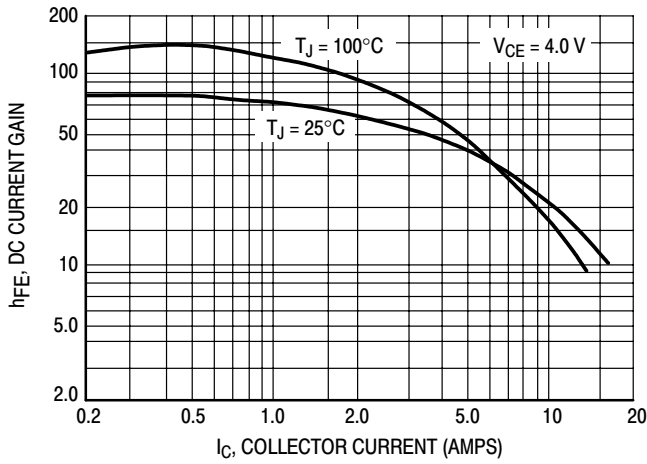


Figure 4. DC Current Gain

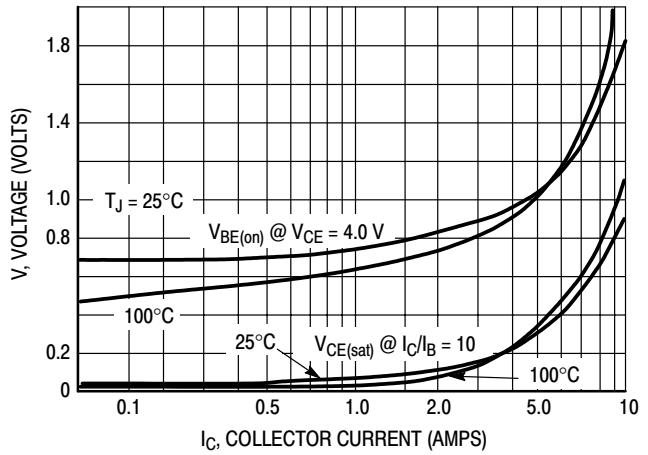


Figure 5. "On" Voltages



# Silicon Power Transistors

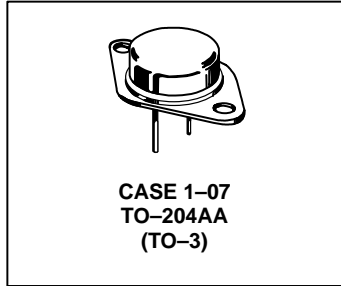
The MJ21193 and MJ21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –  
 $h_{FE} = 25 \text{ Min @ } I_C = 8 \text{ Adc}$
- Excellent Gain Linearity
- High SOA: 2.5 A, 80 V, 1 Second

**PNP**  
**MJ21193\***  
**NPN**  
**MJ21194\***

\*ON Semiconductor Preferred Device

**16 AMPERE**  
**COMPLEMENTARY**  
**SILICON POWER**  
**TRANSISTORS**  
**250 VOLTS**  
**250 WATTS**



## MAXIMUM RATINGS

Rating	Sym- bol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	Vdc
Collector–Base Voltage	$V_{CBO}$	400	Vdc
Emitter–Base Voltage	$V_{EBO}$	5	Vdc
Collector–Emitter Voltage – 1.5 V	$V_{CEX}$	400	Vdc
Collector Current — Continuous Peak (1)	$I_C$	16 30	Adc
Base Current — Continuous	$I_B$	5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	250 1.43	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J$ , $T_{stg}$	–65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
----------------	--------	-----	---------	-----	------

## OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100 \text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = 200 \text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	—	100	$\mu\text{Adc}$

(1) Pulse Test: Pulse Width = 5  $\mu\text{s}$ , Duty Cycle  $\leq 10\%$ . (continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJ21193 MJ21194

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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### OFF CHARACTERISTICS

Emitter Cutoff Current ( $V_{CE} = 5 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 250 \text{ Vdc}$ , $V_{BE(\text{off})} = 1.5 \text{ Vdc}$ )	$I_{CEX}$	—	—	100	$\mu\text{Adc}$

### SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 50 \text{ Vdc}$ , $t = 1 \text{ s}$ (non-repetitive)) ( $V_{CE} = 80 \text{ Vdc}$ , $t = 1 \text{ s}$ (non-repetitive))	$I_{S/b}$	5 2.5	— —	— —	A <sub>dc</sub>
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### ON CHARACTERISTICS

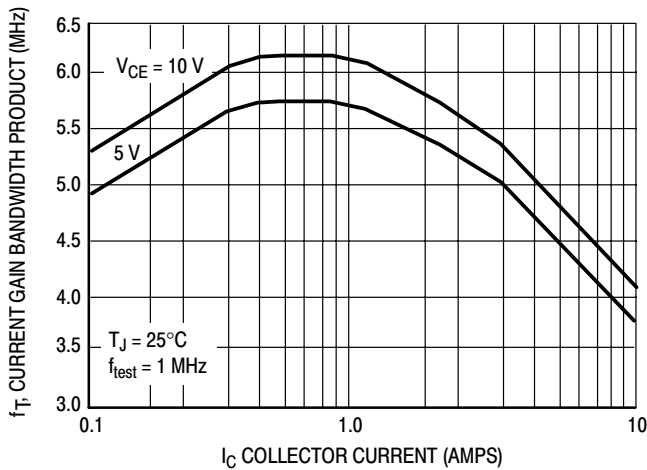
DC Current Gain ( $I_C = 8 \text{ Adc}$ , $V_{CE} = 5 \text{ Vdc}$ ) ( $I_C = 16 \text{ Adc}$ , $I_B = 5 \text{ Adc}$ )	$h_{FE}$	25 8	— —	75	
Base-Emitter On Voltage ( $I_C = 8 \text{ Adc}$ , $V_{CE} = 5 \text{ Vdc}$ )	$V_{BE(\text{on})}$	—	—	2.2	V <sub>dc</sub>
Collector-Emitter Saturation Voltage ( $I_C = 8 \text{ Adc}$ , $I_B = 0.8 \text{ Adc}$ ) ( $I_C = 16 \text{ Adc}$ , $I_B = 3.2 \text{ Adc}$ )	$V_{CE(\text{sat})}$	— —	— —	1.4 4	V <sub>dc</sub>

### DYNAMIC CHARACTERISTICS

Total Harmonic Distortion at the Output $V_{RMS} = 28.3 \text{ V}$ , $f = 1 \text{ kHz}$ , $P_{LOAD} = 100 \text{ W}_{RMS}$  ed (Matched pair $h_{FE} = 50 @ 5 \text{ A}/5 \text{ V}$ )	$T_{HD}$	$h_{FE}$ unmatch  $h_{FE}$ matched	—  —	0.8  0.08	—  —	%
Current Gain Bandwidth Product ( $I_C = 1 \text{ Adc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f_{\text{test}} = 1 \text{ MHz}$ )	$f_T$	4	—	—	—	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f_{\text{test}} = 1 \text{ MHz}$ )	$C_{ob}$	—	—	500	—	pF

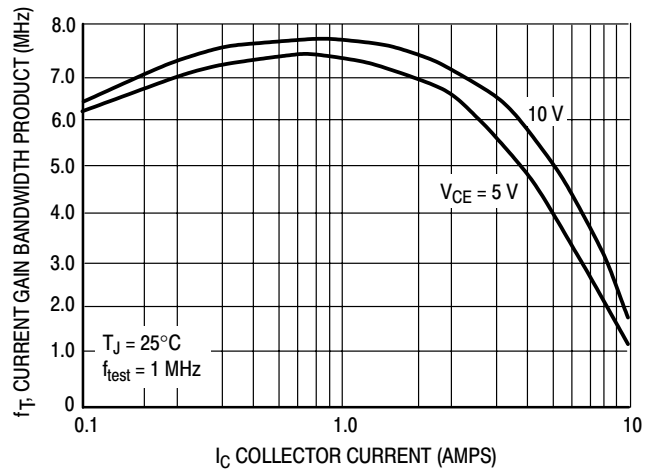
(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$

**PNP MJ21193**



**Figure 1. Typical Current Gain Bandwidth Product**

**NPN MJ21194**



**Figure 2. Typical Current Gain Bandwidth Product**

TYPICAL CHARACTERISTICS

PNP MJ21193

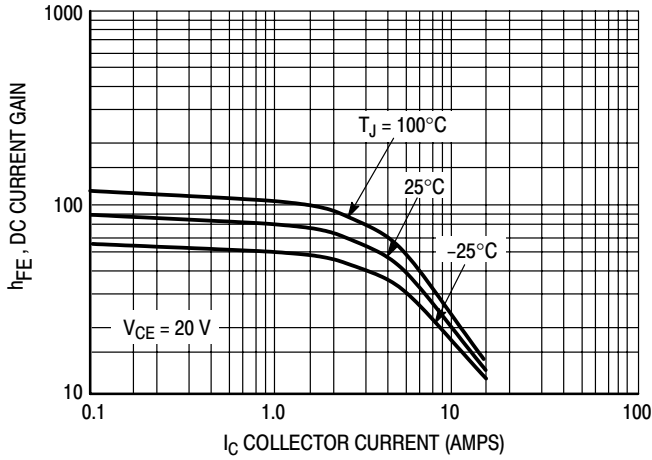


Figure 3. DC Current Gain,  $V_{CE} = 20\text{ V}$

NPN MJ21194

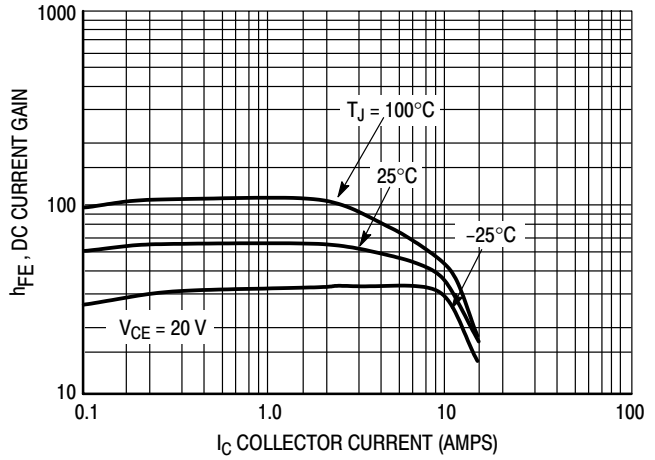


Figure 4. DC Current Gain,  $V_{CE} = 20\text{ V}$

PNP MJ21193

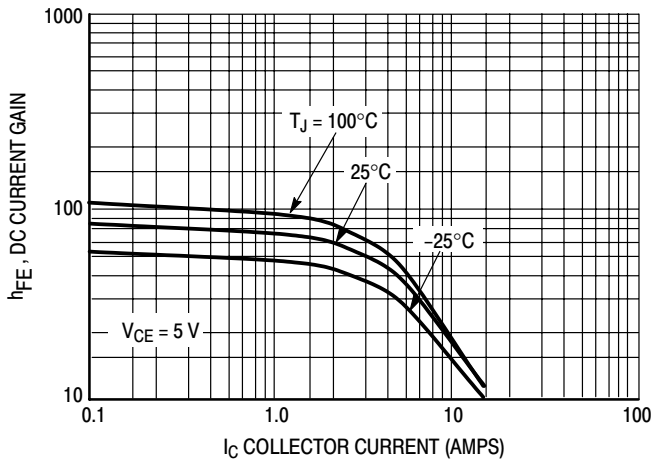


Figure 5. DC Current Gain,  $V_{CE} = 5\text{ V}$

NPN MJ21194

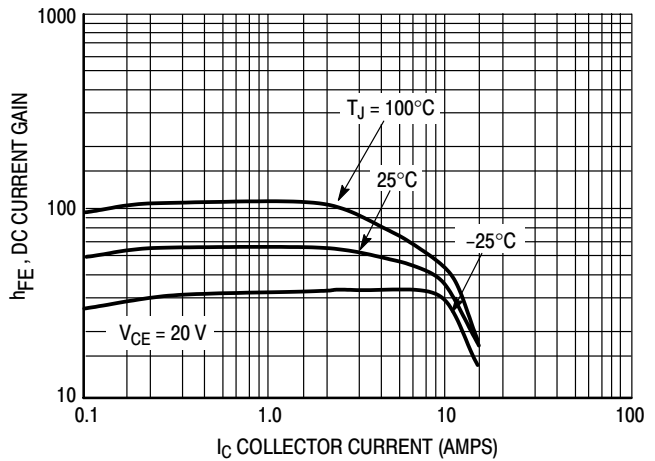


Figure 6. DC Current Gain,  $V_{CE} = 5\text{ V}$

PNP MJ21193

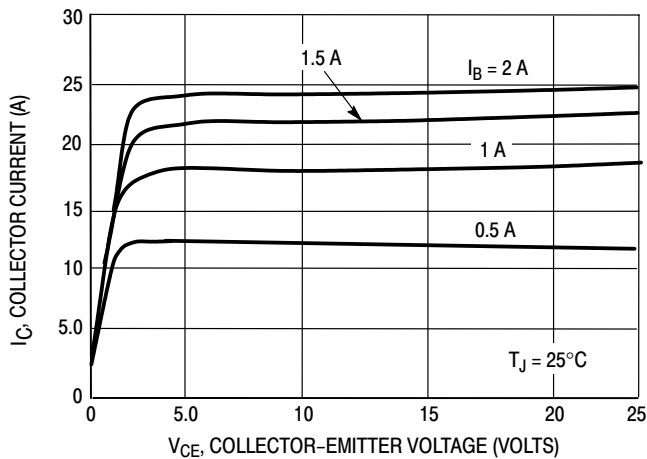


Figure 7. Typical Output Characteristics

NPN MJ21194

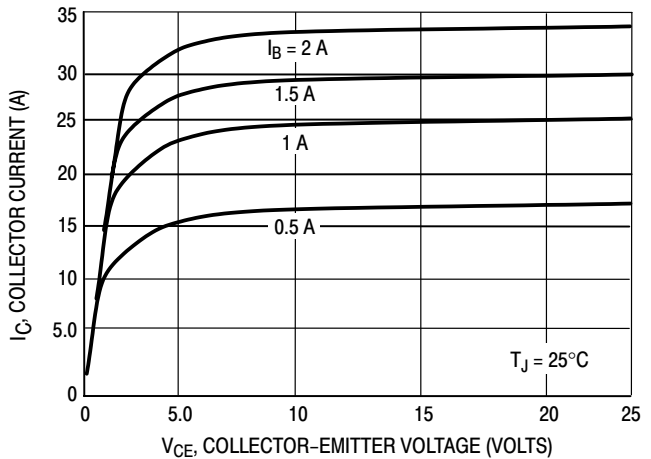


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

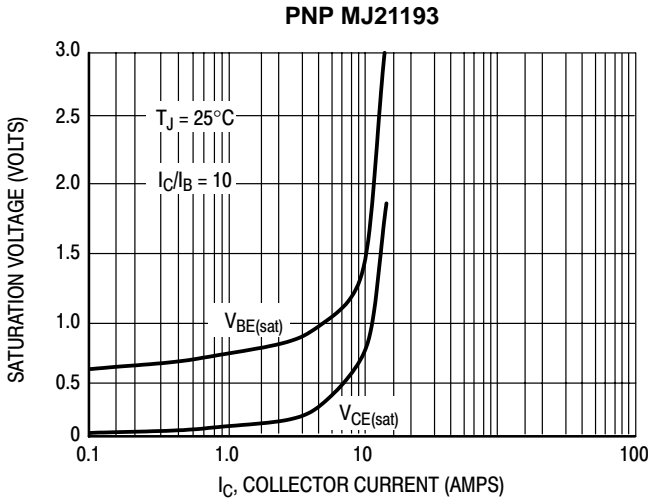


Figure 9. Typical Saturation Voltages

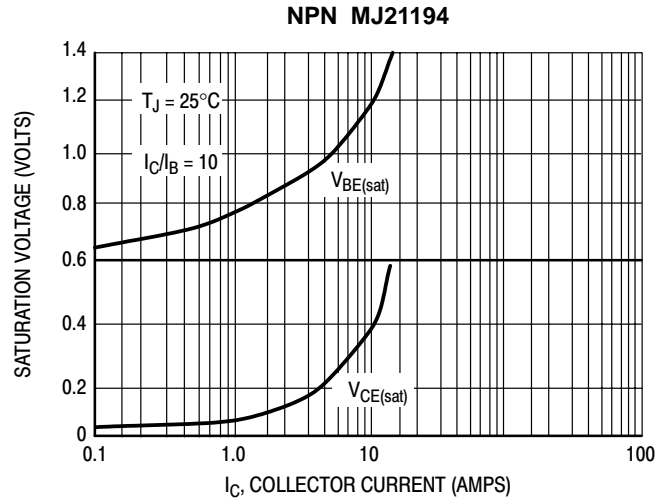


Figure 10. Typical Saturation Voltages

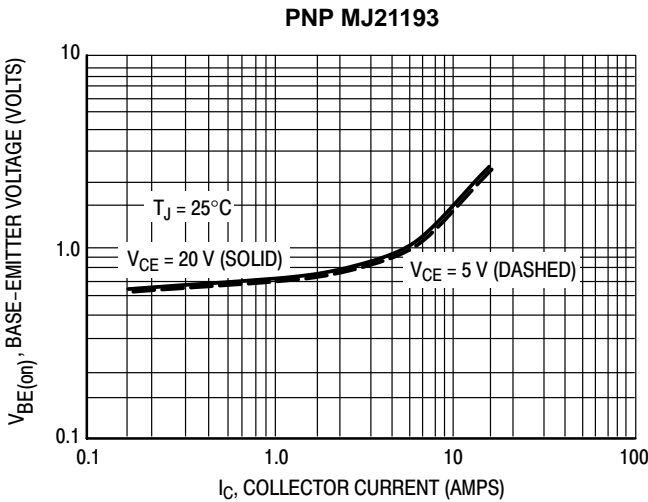


Figure 11. Typical Base-Emitter Voltage

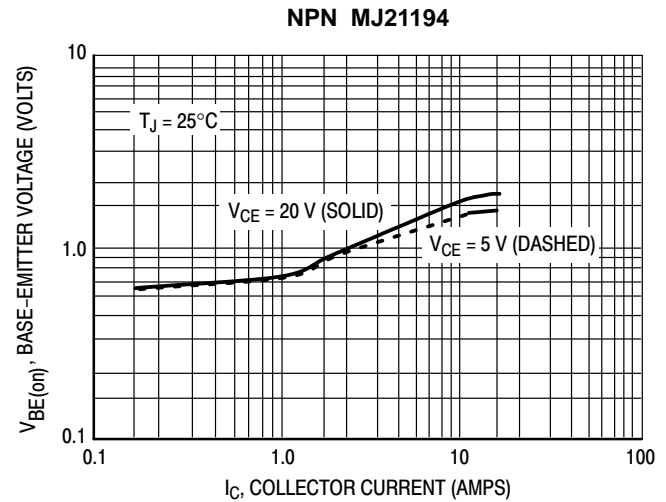


Figure 12. Typical Base-Emitter Voltage

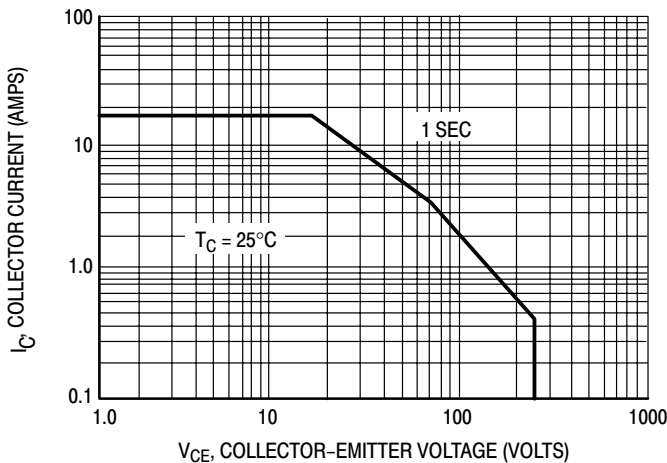


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

# MJ21193 MJ21194

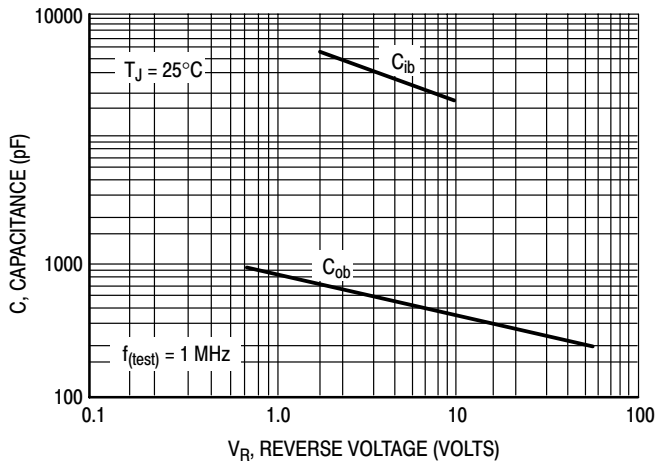


Figure 14. MJ21193 Typical Capacitance

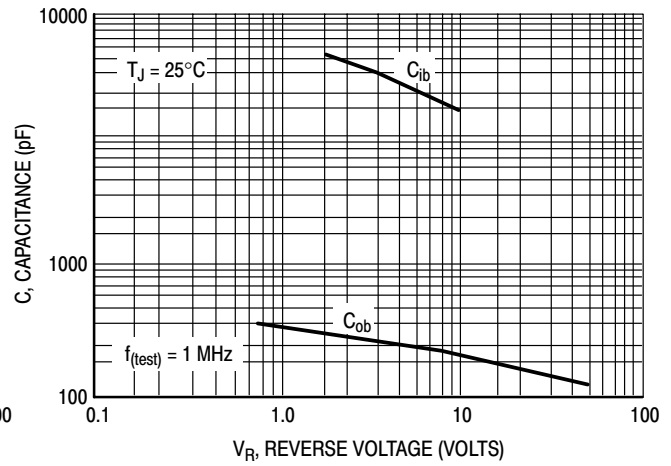


Figure 15. MJ21194 Typical Capacitance

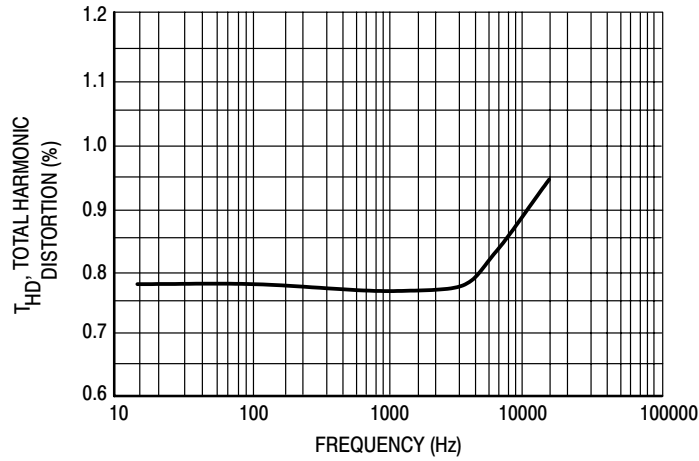


Figure 16. Typical Total Harmonic Distortion

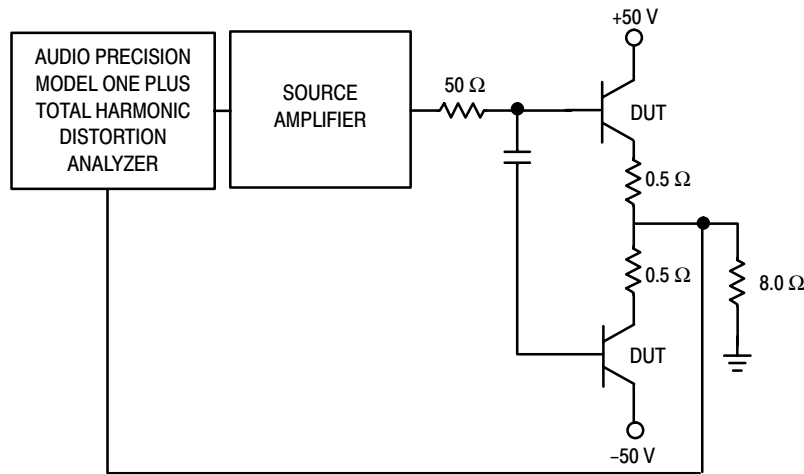


Figure 17. Total Harmonic Distortion Test Circuit

## Silicon Power Transistors

The MJ21195 and MJ21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –  
 $h_{FE} = 25 \text{ Min @ } I_C = 8 \text{ Adc}$
- Excellent Gain Linearity
- High SOA: 3 A, 80 V, 1 Second

### MAXIMUM RATINGS

Rating	Sym- bol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	Vdc
Collector–Base Voltage	$V_{CBO}$	400	Vdc
Emitter–Base Voltage	$V_{EBO}$	5	Vdc
Collector–Emitter Voltage – 1.5 V	$V_{CEX}$	400	Vdc
Collector Current — Continuous Peak <sup>(1)</sup>	$I_C$	16 30	Adc
Base Current — Continuous	$I_B$	5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +200	°C

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C} \pm 5^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
Collector–Emitter Sustaining Voltage ( $I_C = 100 \text{ mAdc}, I_B = 0$ )	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = 200 \text{ Vdc}, I_B = 0$ )	$I_{CEO}$	—	—	100	$\mu\text{Adc}$

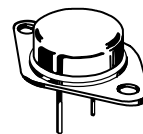
(1) Pulse Test: Pulse Width = 5  $\mu\text{s}$ , Duty Cycle  $\leq 10\%$ .

(continued)

**PNP**  
**MJ21195\***  
**NPN**  
**MJ21196\***

\*ON Semiconductor Preferred Device

**16 AMPERE**  
**COMPLEMENTARY**  
**SILICON POWER**  
**TRANSISTORS**  
**250 VOLTS**  
**250 WATTS**



**CASE 1-07**  
**TO-204AA**  
**(TO-3)**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJ21195 MJ21196

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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### OFF CHARACTERISTICS

Emitter Cutoff Current ( $V_{CE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 250\text{ Vdc}$ , $V_{BE(\text{off})} = 1.5\text{ Vdc}$ )	$I_{CEX}$	—	—	100	$\mu\text{Adc}$

### SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 50\text{ Vdc}$ , $t = 1\text{ s}$ (non-repetitive)) ( $V_{CE} = 80\text{ Vdc}$ , $t = 1\text{ s}$ (non-repetitive))	$I_{S/b}$	5 2.5	— —	— —	A <sub>dc</sub>
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### ON CHARACTERISTICS

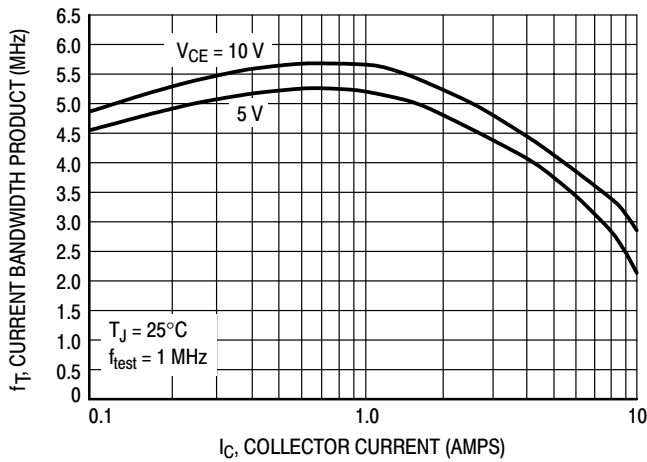
DC Current Gain ( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 16\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$h_{FE}$	25 8	— —	75	
Base-Emitter On Voltage ( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$V_{BE(\text{on})}$	—	—	2.2	V <sub>dc</sub>
Collector-Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.8\text{ Adc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 3.2\text{ Adc}$ )	$V_{CE(\text{sat})}$	— —	— —	1.4 4	V <sub>dc</sub>

### DYNAMIC CHARACTERISTICS

Total Harmonic Distortion at the Output $V_{RMS} = 28.3\text{ V}$ , $f = 1\text{ kHz}$ , $P_{LOAD} = 100\text{ W}_{RMS}$  ed (Matched pair $h_{FE} = 50 @ 5\text{ A}/5\text{ V}$ )	$h_{FE}$ unmatch  $h_{FE}$ matched	$T_{HD}$	— —	0.8 0.08	— —	%
Current Gain Bandwidth Product ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{\text{test}} = 1\text{ MHz}$ )		$f_T$	4	—	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{\text{test}} = 1\text{ MHz}$ )		$C_{ob}$	—	—	500	pF

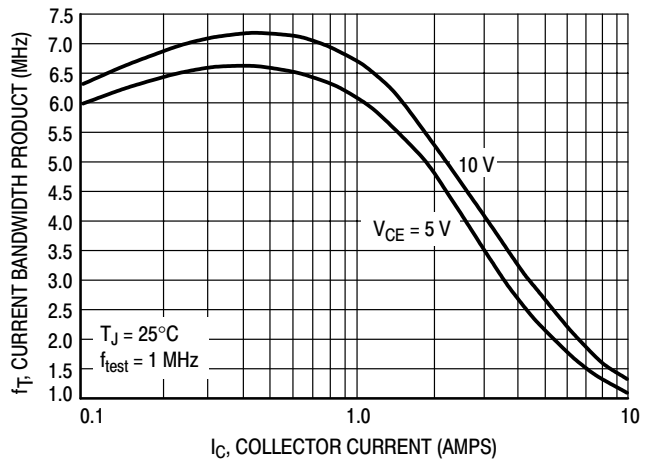
(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$

**PNP MJ21195**



**Figure 1. Typical Current Gain Bandwidth Product**

**NPN MJ21196**



**Figure 2. Typical Current Gain Bandwidth Product**

TYPICAL CHARACTERISTICS

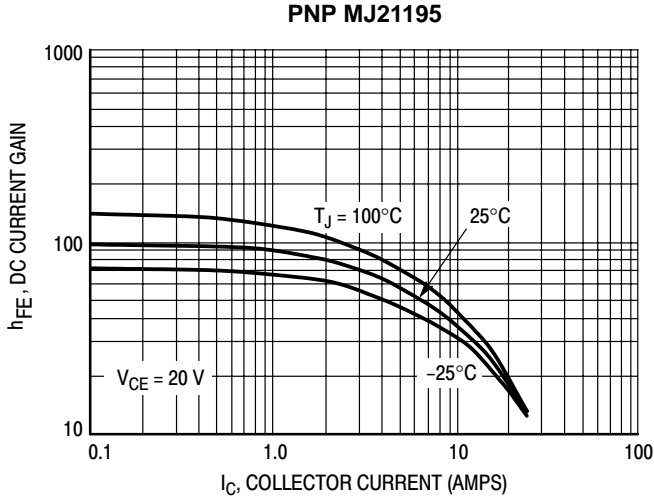


Figure 3. DC Current Gain,  $V_{CE} = 20\text{ V}$

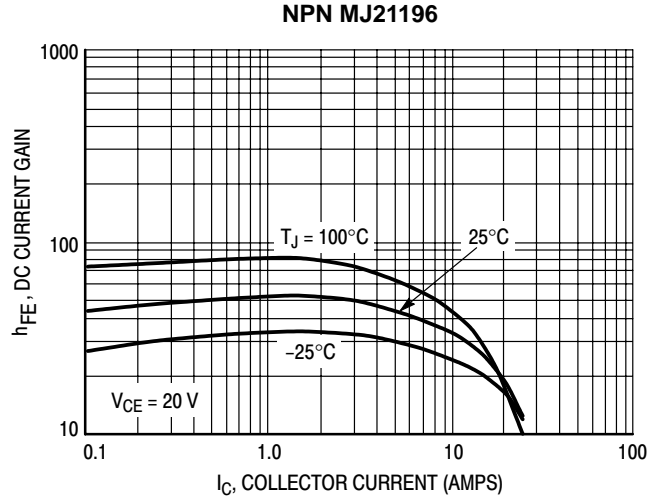


Figure 4. DC Current Gain,  $V_{CE} = 20\text{ V}$

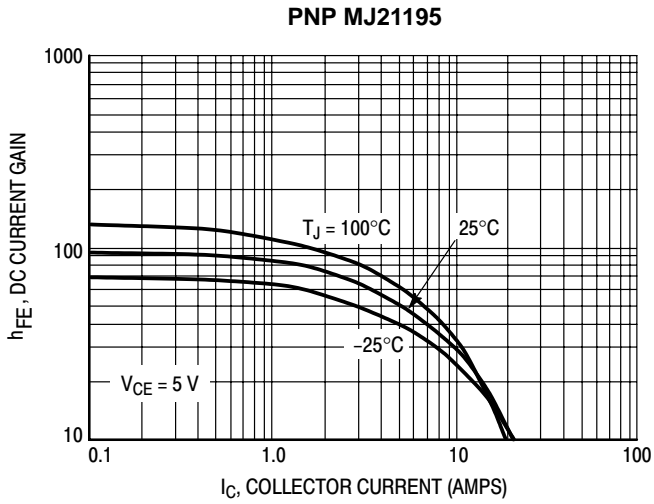


Figure 5. DC Current Gain,  $V_{CE} = 5\text{ V}$

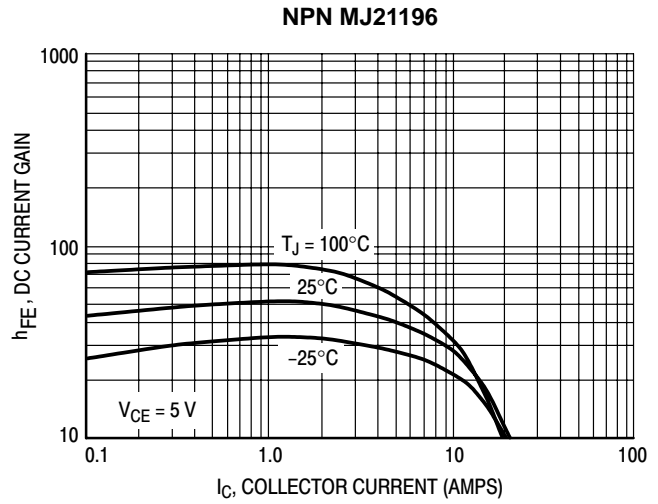


Figure 6. DC Current Gain,  $V_{CE} = 5\text{ V}$

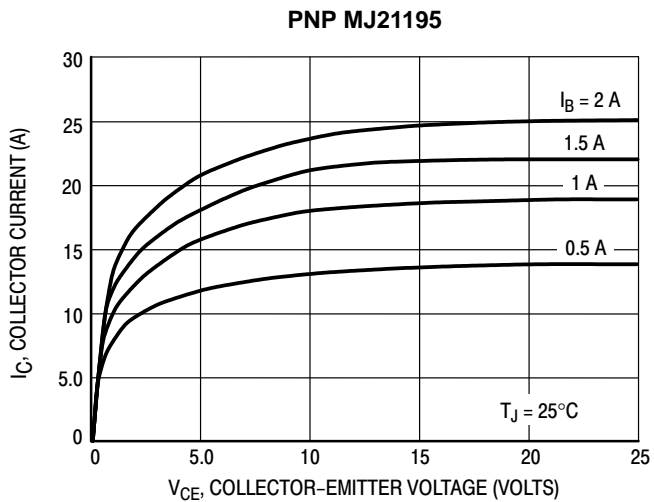


Figure 7. Typical Output Characteristics

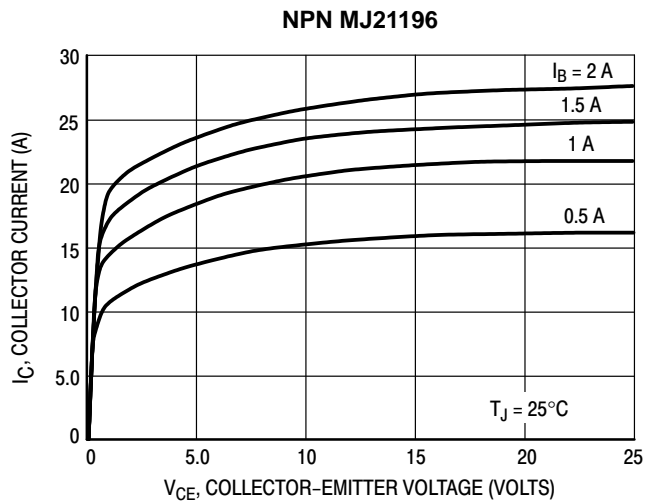


Figure 8. Typical Output Characteristics



TYPICAL CHARACTERISTICS

PNP MJ21195

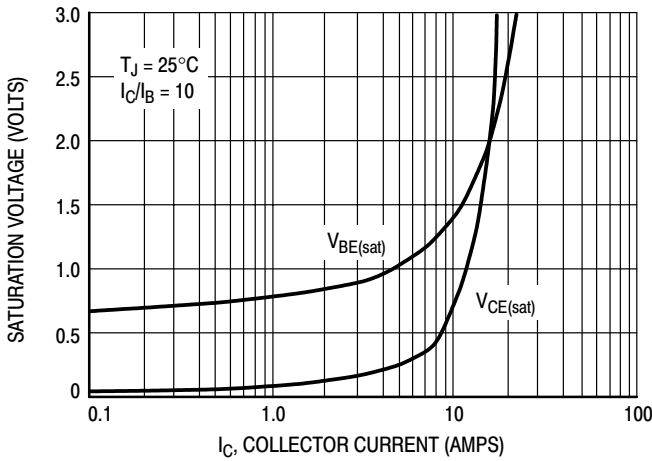


Figure 9. Typical Saturation Voltages

NPN MJ21196

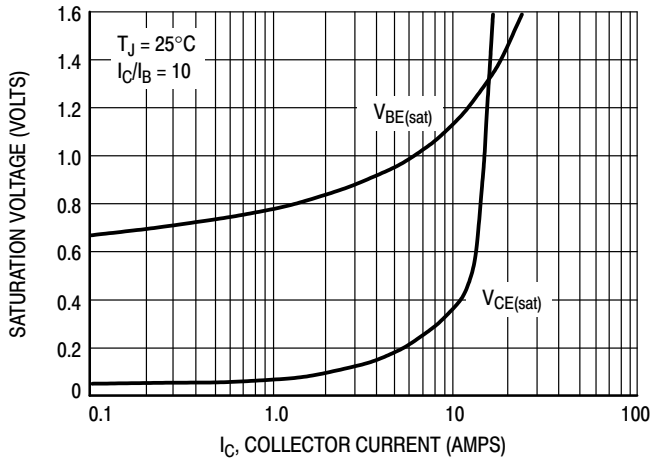


Figure 10. Typical Saturation Voltages

PNP MJ21195

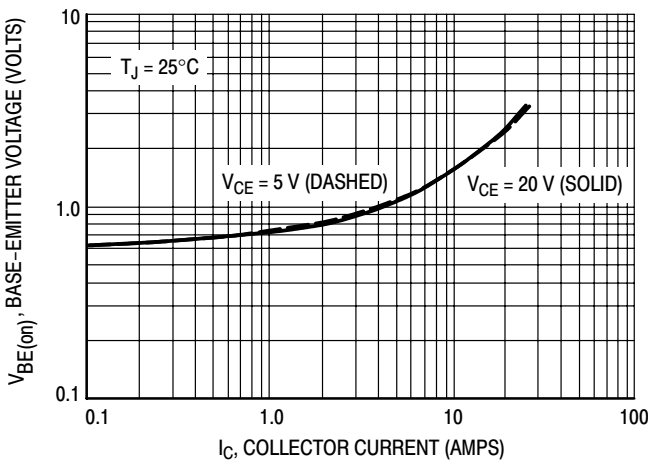


Figure 11. Typical Base-Emitter Voltage

NPN MJ21196

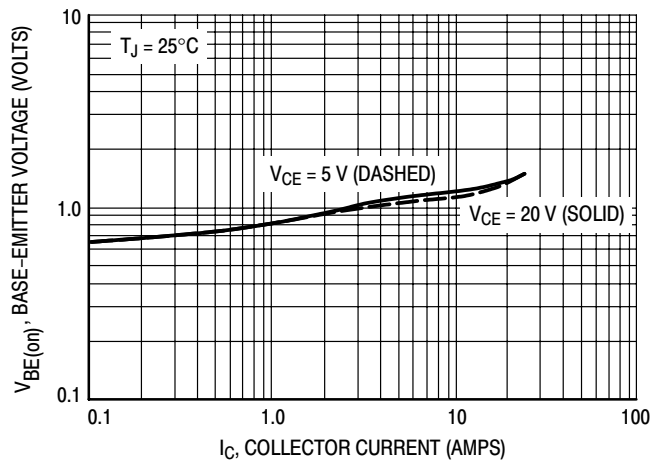


Figure 12. Typical Base-Emitter Voltage

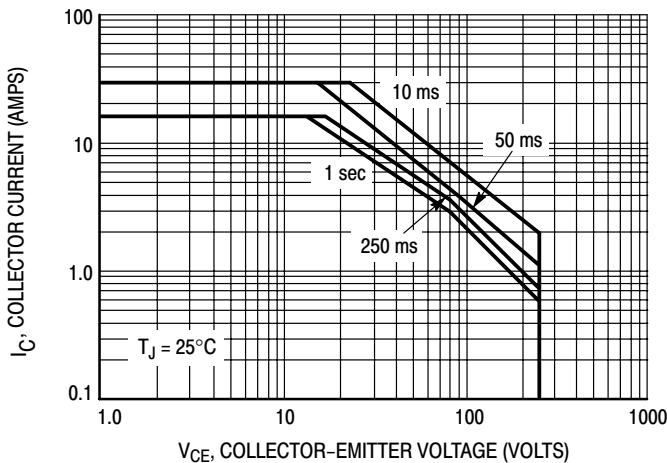


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

# MJ21195 MJ21196

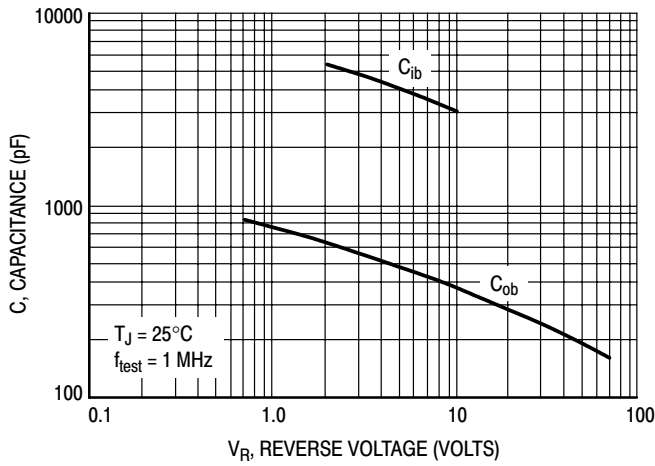


Figure 14. MJ21195 Typical Capacitance

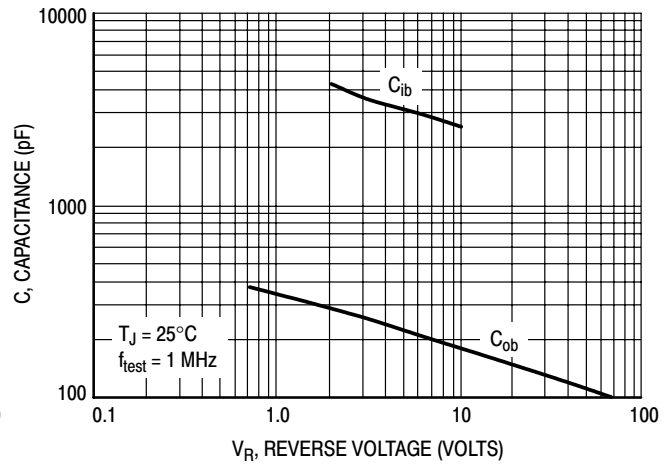


Figure 15. MJ21196 Typical Capacitance

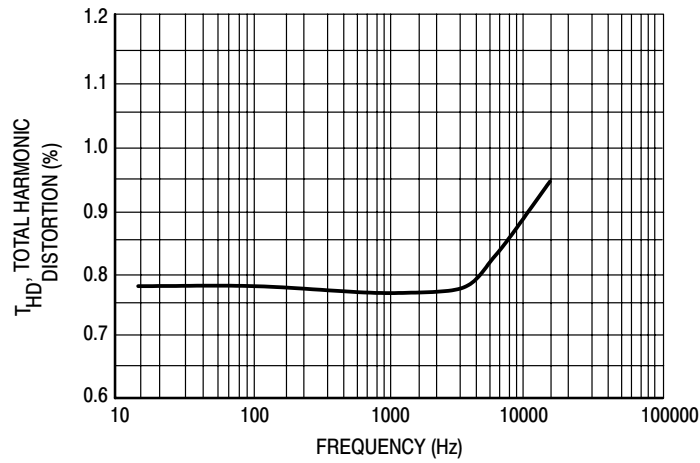


Figure 16. Typical Total Harmonic Distortion

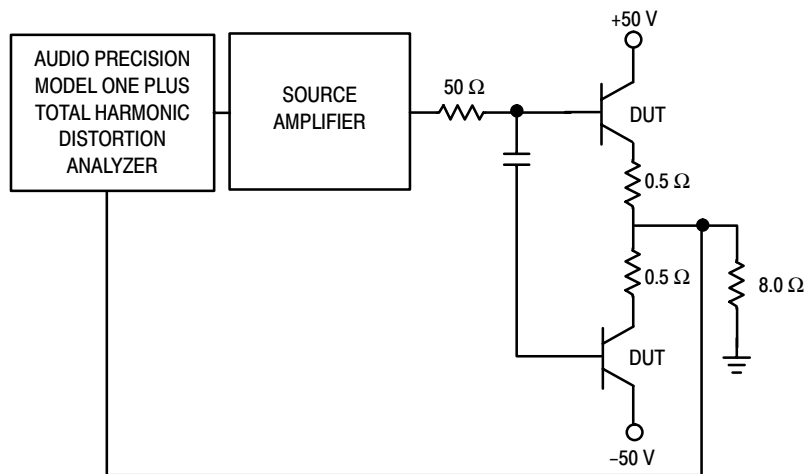


Figure 17. Total Harmonic Distortion Test Circuit

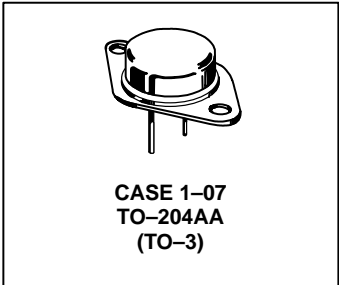
# High-Power PNP Silicon Transistor

... for use as an output device in complementary audio amplifiers to 100-Watts music power per channel.

- High DC Current Gain —  
 $h_{FE} = 25-100 @ I_C = 7.5 \text{ A}$
- Excellent Safe Operating Area
- Complement to the NPN MJ802

**MJ4502**

**30 AMPERE  
 POWER TRANSISTOR  
 PNP SILICON  
 100 VOLTS  
 200 WATTS**

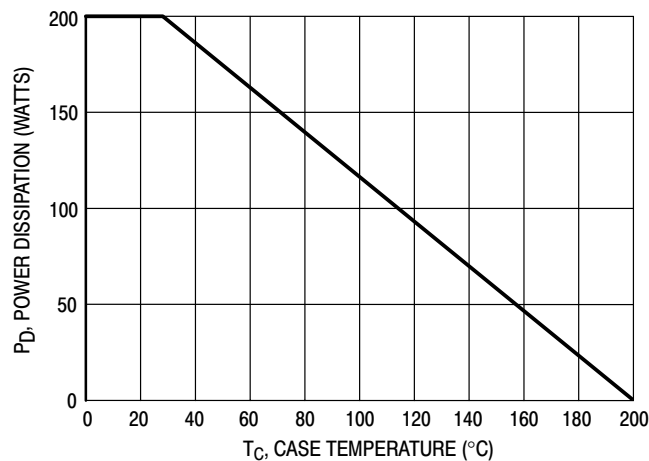


**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CER}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Collector-Emitter Voltage	$V_{CEO}$	90	Vdc
Emitter-Base Voltage	$V_{EB}$	4.0	Vdc
Collector Current	$I_C$	30	Adc
Base Current	$I_B$	7.5	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.14	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

**MAXIMUM RATINGS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.875	$^\circ\text{C/W}$



**Figure 1. Power-Temperature Derating Curve**

# MJ4502

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Breakdown Voltage <sup>(1)</sup> ( $I_C = 200\text{ mAdc}$ , $R_{BE} = 100\text{ Ohms}$ )	$V_{(BR)CER}$	100	—	Vdc
Collector–Emitter Sustaining Voltage <sup>(1)</sup> ( $I_C = 200\text{ mAdc}$ )	$V_{CEO(sus)}$	90	—	Vdc
Collector–Base Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ , $T_C = 150^\circ\text{C}$ )	$I_{CBO}$	—	1.0 5.0	mAdc
Emitter–Base Cutoff Current ( $V_{BE} = 4.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc

## ON CHARACTERISTICS

DC Current Gain ( $I_C = 7.5\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$h_{FE}$	25	100	—
Base–Emitter “On” Voltage ( $I_C = 7.5\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$V_{BE(on)}$	—	1.3	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 7.5\text{ Adc}$ , $I_B = 0.75\text{ Adc}$ )	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter Saturation Voltage ( $I_C = 7.5\text{ Adc}$ , $I_B = 0.75\text{ Adc}$ )	$V_{BE(sat)}$	—	1.3	Vdc

## DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	2.0	—	MHz
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<sup>(1)</sup>Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

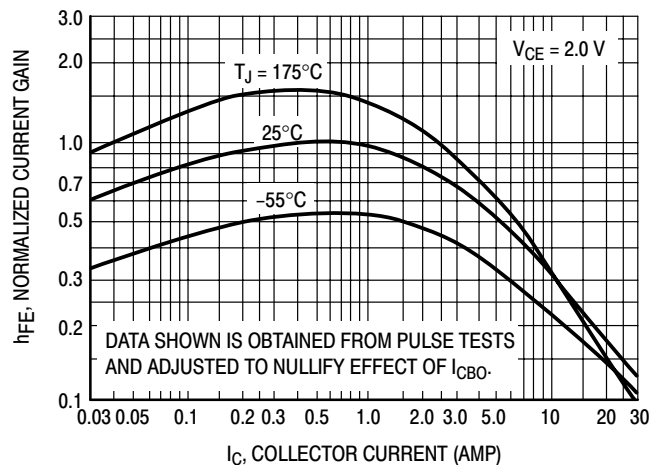


Figure 2. DC Current Gain

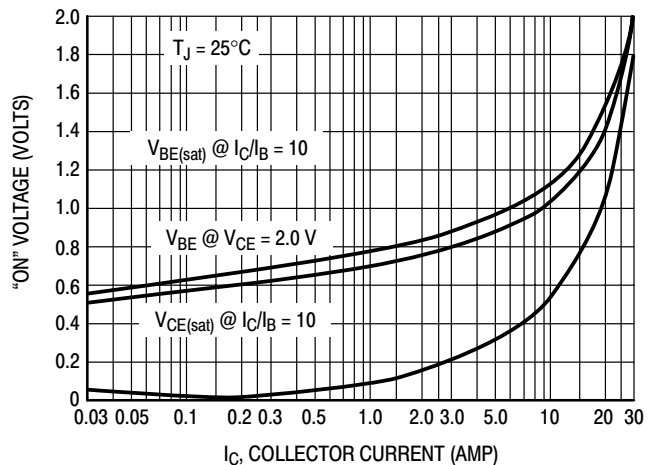


Figure 3. “On” Voltages

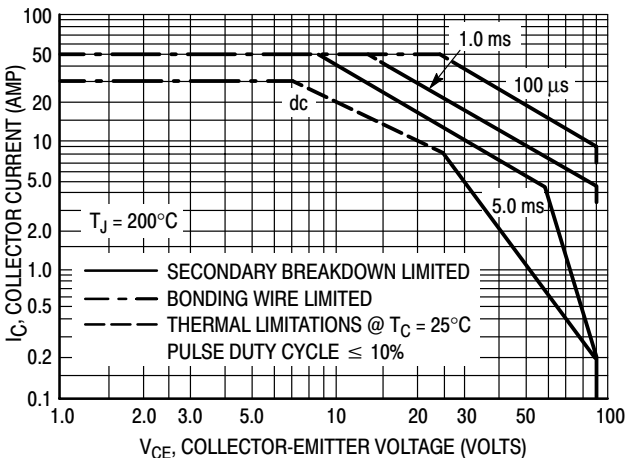


Figure 4. Active Region Safe Operating Area

The Safe Operating Area Curves indicate  $I_C - V_{CE}$  limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum  $T_J$ , power–temperature derating must be observed for both steady state and pulse power conditions.

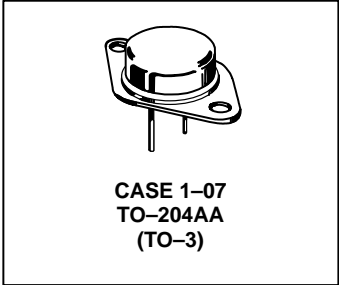
# High-Power NPN Silicon Transistor

... for use as an output device in complementary audio amplifiers to 100-Watts music power per channel.

- High DC Current Gain —  
 $h_{FE} = 25-100 @ I_C = 7.5 \text{ A}$
- Excellent Safe Operating Area
- Complement to the PNP MJ4502

**MJ802**

**30 AMPERE  
POWER TRANSISTOR  
NPN SILICON  
100 VOLTS  
200 WATTS**



## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CER}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Collector-Emitter Voltage	$V_{CEO}$	90	Vdc
Emitter-Base Voltage	$V_{EB}$	4.0	Vdc
Collector Current	$I_C$	30	Adc
Base Current	$I_B$	7.5	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.14	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.875	$^\circ\text{C}/\text{W}$

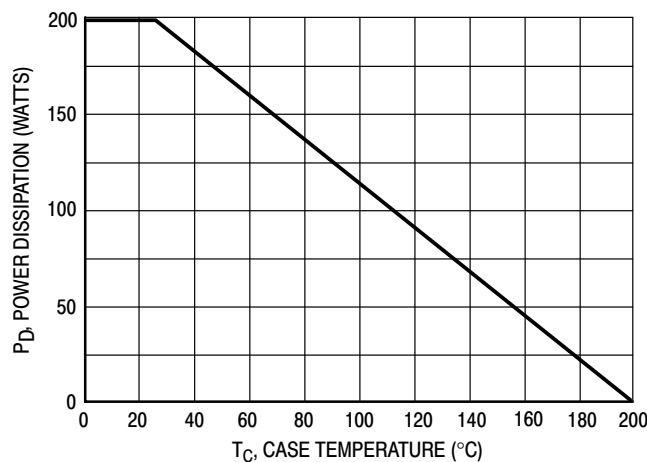


Figure 1. Power-Temperature Derating Curve

# MJ802

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage <sup>(1)</sup> ( $I_C = 200\text{ mA}$ , $R_{BE} = 100\ \Omega$ )	$BV_{CEr}$	100	—	Vdc
Collector–Emitter Sustaining Voltage <sup>(1)</sup> ( $I_C = 200\text{ mA}$ )	$V_{CEO(sus)}$	90	—	Vdc
Collector–Base Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ , $T_C = 150^\circ\text{C}$ )	$I_{CBO}$	— —	1.0 5.0	mAdc
Emitter–Base Cutoff Current ( $V_{BE} = 4.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc

### ON CHARACTERISTICS<sup>(1)</sup>

DC Current Gain <sup>(1)</sup> ( $I_C = 7.5\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$h_{FE}$	25	100	—
Base–Emitter “On” Voltage ( $I_C = 7.5\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$V_{BE(on)}$	—	1.3	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 7.5\text{ Adc}$ , $I_B = 0.75\text{ Adc}$ )	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter Saturation Voltage ( $I_C = 7.5\text{ Adc}$ , $I_B = 0.75\text{ Adc}$ )	$V_{BE(sat)}$	—	1.3	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	2.0	—	MHz
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<sup>(1)</sup>Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

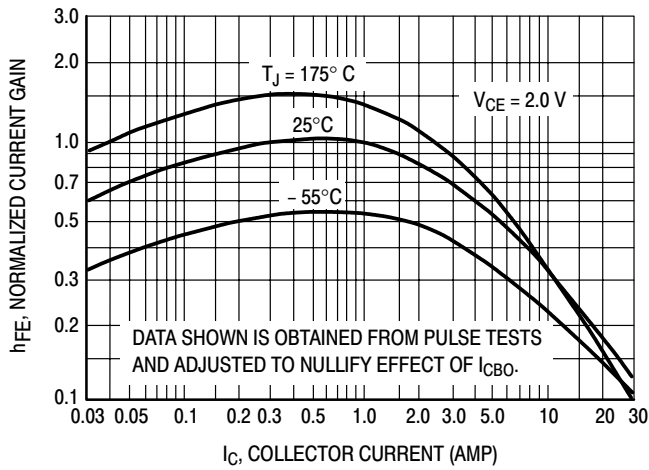


Figure 2. DC Current Gain

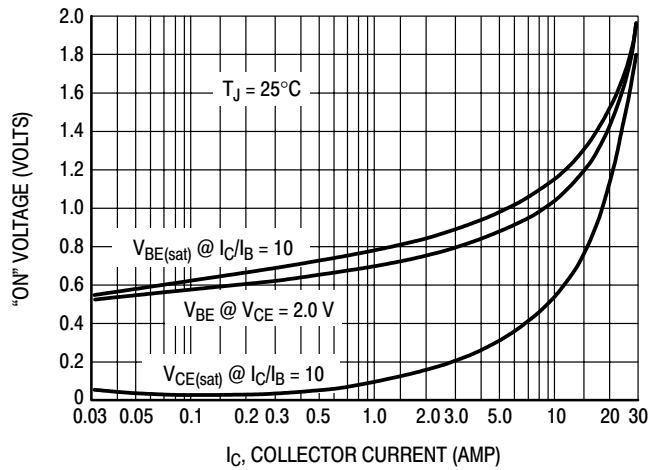


Figure 3. "On" Voltages

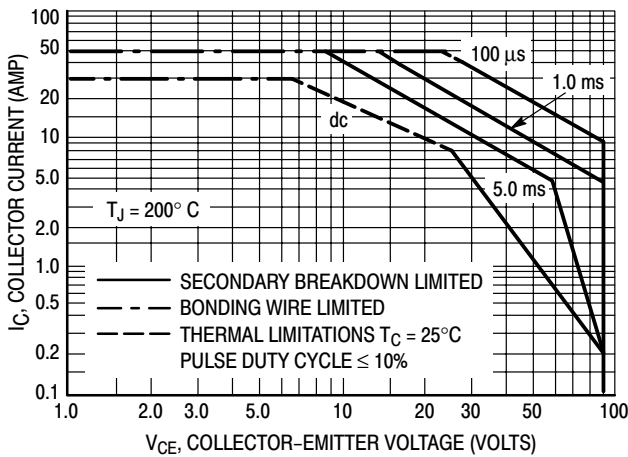


Figure 4. Active Region Safe Operating Area

The Safe Operating Area Curves indicate  $I_C - V_{CE}$  limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum  $T_J$ , power temperature derating must be observed for both steady state and pulse power conditions.

# High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

## D2PAK For Surface Mount

The MJB18004D2T4 is state-of-art High Speed High gain Bipolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread ( $\pm 150$  ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an  $h_{FE}$  window.

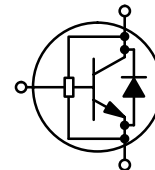
### Main features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @  $I_C = 100$  mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector-Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic  $V_{CE(sat)}$
- “6 Sigma” Process Providing Tight and Reproducible Parameter Spreads

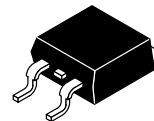
It's characteristics make it also suitable for PFC application.

## MJB18004D2T4

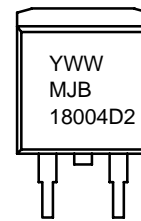
POWER TRANSISTORS  
5 AMPERES  
1000 VOLTS  
75 WATTS



### MARKING DIAGRAM



D<sup>2</sup>PAK  
CASE 418B  
STYLE 1



Y = Year  
WW = Work Week



# MJB18004D2T4

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	$V_{CEO}$	450	Vdc
Collector–Base Breakdown Voltage	$V_{CBO}$	1000	Vdc
Collector–Emitter Breakdown Voltage	$V_{CES}$	1000	Vdc
Emitter–Base Voltage	$V_{EBO}$	12	Vdc
Collector Current — Continuous — Peak (1)	$I_C$ $I_{CM}$	5 10	Adc
Base Current — Continuous — Peak (1)	$I_B$ $I_{BM}$	2 4	Adc
*Total Device Dissipation @ $T_C = 25^\circ\text{C}$ *Derate above $25^\circ\text{C}$	$P_D$	75 0.6	Watt $\text{W}/^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{stg}$	–65 to 150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	$^\circ\text{C}/\text{W}$
Junction to Ambient, When Mounted With the Minimum Recommended Pad Size.	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from case for 5 seconds	$T_L$	260	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq$  10%.

# MJB18004D2T4

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	450	547		Vdc
Collector–Base Breakdown Voltage ( $I_{CBO} = 1\text{ mA}$ )	$V_{CBO}$	1000	1100		Vdc
Emitter–Base Breakdown Voltage ( $I_{EBO} = 1\text{ mA}$ )	$V_{EBO}$	12	14		Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$			100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )  ( $V_{CE} = 500\text{ V}$ , $V_{EB} = 0$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$I_{CES}$		100 500 100	$\mu\text{Adc}$
Emitter–Cutoff Current ( $V_{EB} = 10\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$			100	$\mu\text{Adc}$

## ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 0.8\text{ Adc}$ , $I_B = 80\text{ mAdc}$ )  ( $I_C = 2\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{BE(sat)}$		0.8 0.7	1 0.9	Vdc
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.9 0.8	1 0.9	
Collector–Emitter Saturation Voltage ( $I_C = 0.8\text{ Adc}$ , $I_B = 80\text{ mAdc}$ )  ( $I_C = 2\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )  ( $I_C = 0.8\text{ Adc}$ , $I_B = 40\text{ mAdc}$ )  ( $I_C = 1\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(sat)}$		0.38 0.55	0.5 0.75	Vdc
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.45 0.75	0.75 1	
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.9 1.6	1.5	
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.25 0.28	0.5 0.6	
DC Current Gain ( $I_C = 0.8\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )  ( $I_C = 2\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )  ( $I_C = 1\text{ Adc}$ , $V_{CE} = 2.5\text{ Vdc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$h_{FE}$	15 10	28 14		—
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		6 4	8 6		
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		18 14	28 20		

## DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 1 $\mu\text{s}$ and 3 $\mu\text{s}$ respectively after rising $I_{B1}$ reaches 90% of final $I_{B1}$	$I_C = 1\text{ Adc}$ $I_{B1} = 100\text{ mA}$ $V_{CC} = 300\text{ V}$	@ 1 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(dsat)}$		9 16	V
		@ 3 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			3.1 9	
	$I_C = 2\text{ Adc}$ $I_{B1} = 0.4\text{ A}$ $V_{CC} = 300\text{ V}$	@ 1 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		11 18		
		@ 3 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		1.4 8		

# MJB18004D2T4

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### DIODE CHARACTERISTICS

Forward Diode Voltage ( $I_{EC} = 1 \text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$	$V_{EC}$		0.96	1.5	V	
	@ $T_C = 125^\circ\text{C}$			0.72			
( $I_{EC} = 2 \text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$			1.15	1.7		
	@ $T_C = 125^\circ\text{C}$			0.8			
Forward Recovery Time ( $I_F = 0.4 \text{ Adc}$ , $di/dt = 10 \text{ A}/\mu\text{s}$ )	@ $T_C = 25^\circ\text{C}$	$t_{fr}$		440		ns	
	( $I_F = 1 \text{ Adc}$ , $di/dt = 10 \text{ A}/\mu\text{s}$ )			@ $T_C = 25^\circ\text{C}$			335
	( $I_F = 2 \text{ Adc}$ , $di/dt = 10 \text{ A}/\mu\text{s}$ )			@ $T_C = 25^\circ\text{C}$			335

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 0.5 \text{ Adc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1 \text{ MHz}$ )	$f_T$		13		MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 1 \text{ MHz}$ )	$C_{ob}$		60	100	pF
Input Capacitance ( $I_C = 0.5 \text{ Adc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1 \text{ MHz}$ )	$C_{ib}$		450	750	pF

### SWITCHING CHARACTERISTICS: Resistive Load ( $D.C. \leq 10\%$ , Pulse Width = 40 $\mu\text{s}$ )

Turn-on Time	$I_C = 2.5 \text{ Adc}$ , $I_{B1} = 0.5 \text{ Adc}$ $I_{B2} = 1 \text{ Adc}$ $V_{CC} = 250 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$		500	750	ns
Turn-off Time		@ $T_C = 25^\circ\text{C}$	$t_{off}$	1.1		1.4	$\mu\text{s}$
Turn-on Time	$I_C = 2 \text{ Adc}$ , $I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 1 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$		100	150	ns
Turn-off Time		@ $T_C = 125^\circ\text{C}$			150		
Turn-on Time	$I_C = 2.5 \text{ Adc}$ , $I_{B1} = 0.5 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$		120	150	ns
		@ $T_C = 125^\circ\text{C}$			500		
Turn-off Time		@ $T_C = 25^\circ\text{C}$	$t_{off}$	1.85		2.15	$\mu\text{s}$
		@ $T_C = 125^\circ\text{C}$			2.6		

### SWITCHING CHARACTERISTICS: Inductive Load ( $V_{CC} = 15 \text{ V}$ )

Fall Time	$I_C = 2.5 \text{ Adc}$ $I_{B1} = 500 \text{ mAdc}$ $I_{B2} = 500 \text{ mAdc}$ $V_Z = 350 \text{ V}$ $L_C = 300 \mu\text{H}$	@ $T_C = 25^\circ\text{C}$	$t_f$		130	175	ns
		@ $T_C = 125^\circ\text{C}$			300		
Storage Time		@ $T_C = 25^\circ\text{C}$	$t_s$	2.12	2.4	$\mu\text{s}$	
		@ $T_C = 125^\circ\text{C}$		2.6			
Crossover Time		@ $T_C = 25^\circ\text{C}$	$t_c$		355	500	ns
		@ $T_C = 125^\circ\text{C}$			750		
Fall Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 400 \text{ mAdc}$ $I_{B2} = 400 \text{ mAdc}$ $V_Z = 300 \text{ V}$ $L_C = 200 \mu\text{H}$	@ $T_C = 25^\circ\text{C}$	$t_f$		95	150	ns
		@ $T_C = 125^\circ\text{C}$			230		
Storage Time		@ $T_C = 25^\circ\text{C}$	$t_s$	2.1	2.4	$\mu\text{s}$	
		@ $T_C = 125^\circ\text{C}$		2.9			
Crossover Time		@ $T_C = 25^\circ\text{C}$	$t_c$		300	450	ns
		@ $T_C = 125^\circ\text{C}$			700		
Fall Time	$I_C = 1 \text{ Adc}$ $I_{B1} = 100 \text{ mAdc}$ $I_{B2} = 500 \text{ mAdc}$ $V_Z = 300 \text{ V}$ $L_C = 200 \mu\text{H}$	@ $T_C = 25^\circ\text{C}$	$t_f$		70	90	ns
		@ $T_C = 125^\circ\text{C}$			100		
Storage Time		@ $T_C = 25^\circ\text{C}$	$t_s$	0.7	0.9	$\mu\text{s}$	
		@ $T_C = 125^\circ\text{C}$		1.05			
Crossover Time		@ $T_C = 25^\circ\text{C}$	$t_c$		75	120	ns
		@ $T_C = 125^\circ\text{C}$			160		

TYPICAL STATIC CHARACTERISTICS

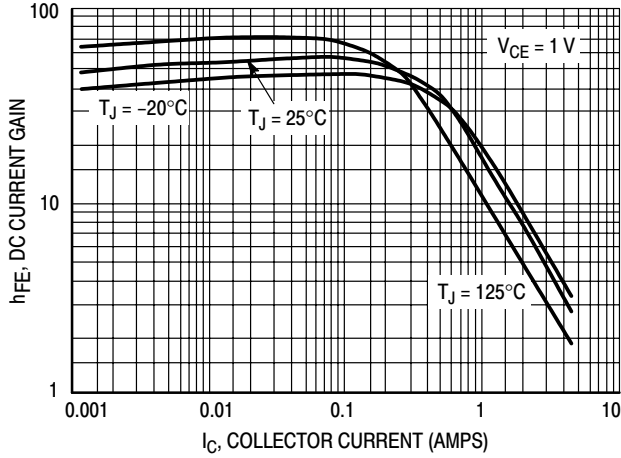


Figure 1. DC Current Gain @ 1 Volt

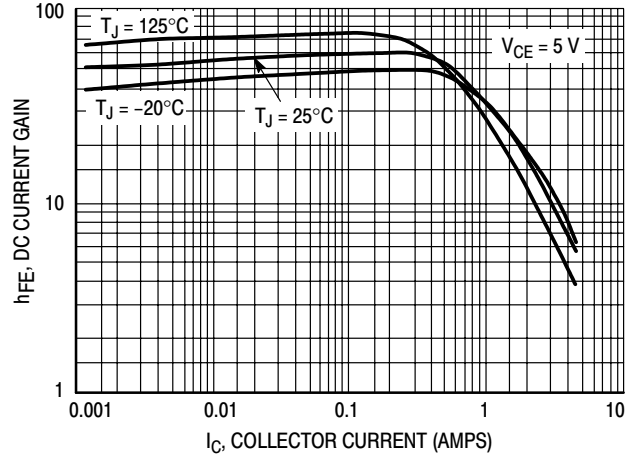


Figure 2. DC Current Gain @ 5 Volt

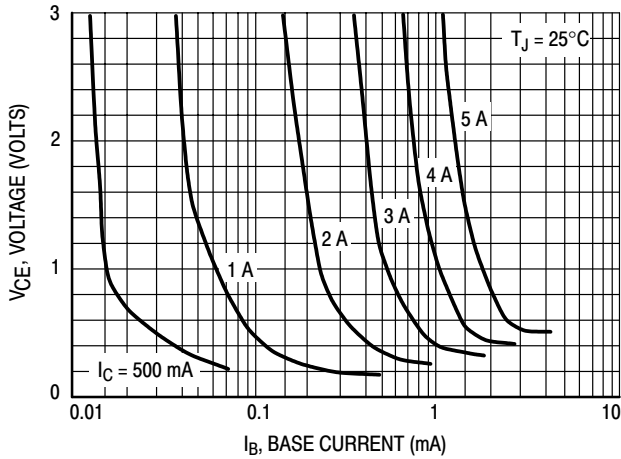


Figure 3. Collector Saturation Region

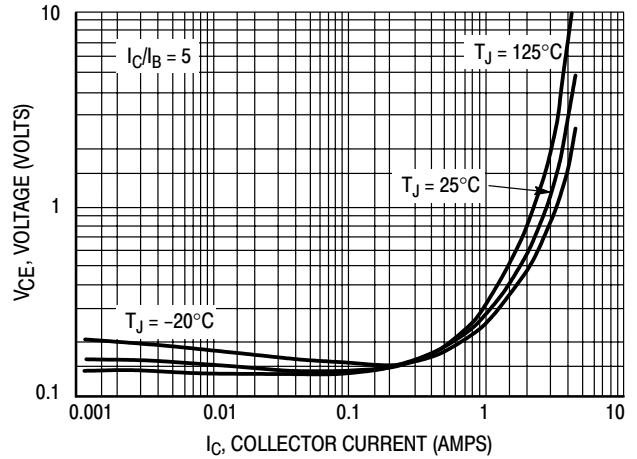


Figure 4. Collector-Emitter Saturation Voltage

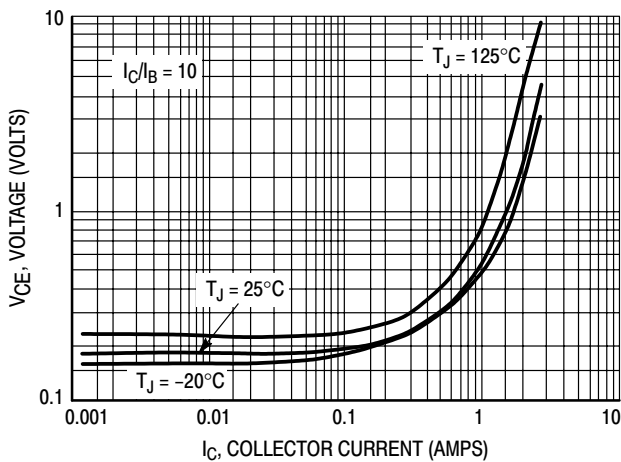


Figure 5. Collector-Emitter Saturation Voltage

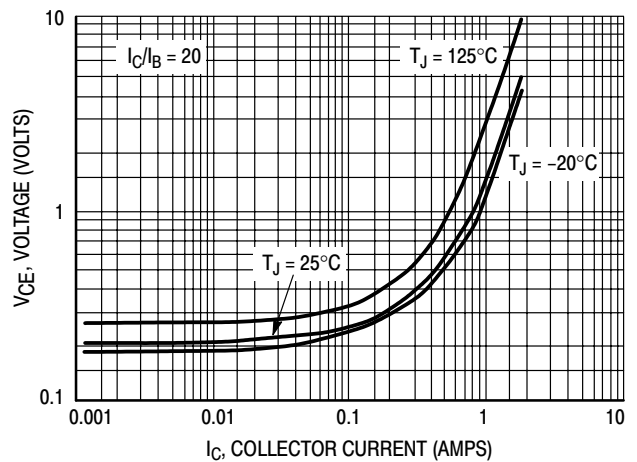


Figure 6. Collector-Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

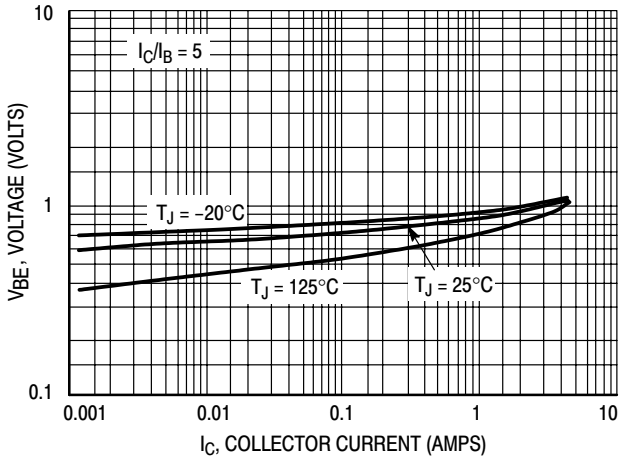


Figure 7. Base-Emitter Saturation Region

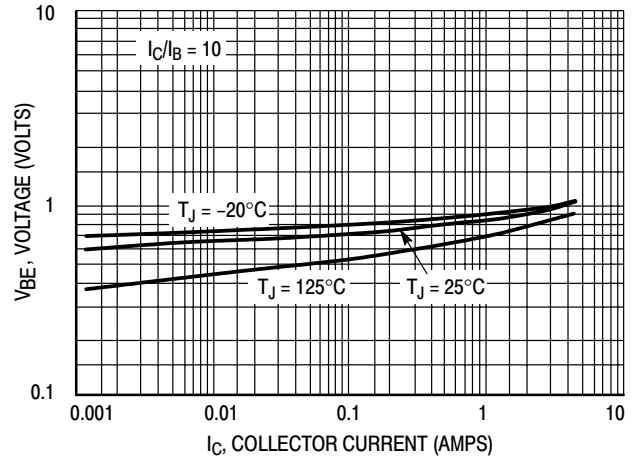


Figure 8. Base-Emitter Saturation Region

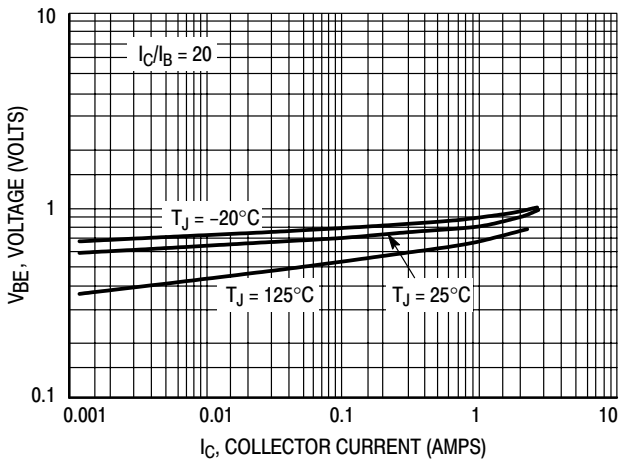


Figure 9. Base-Emitter Saturation Region

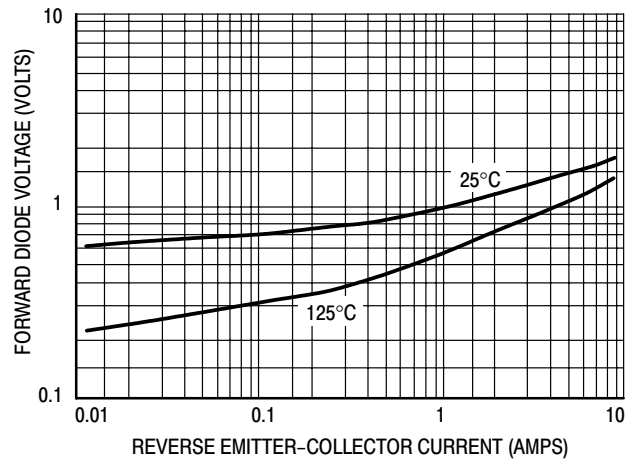


Figure 10. Forward Diode Voltage

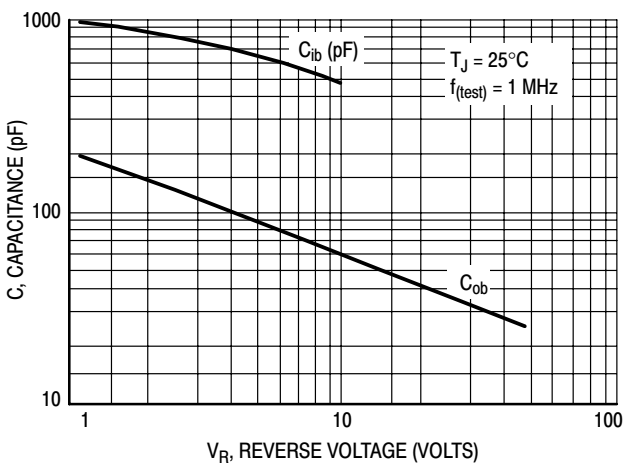


Figure 11. Capacitance

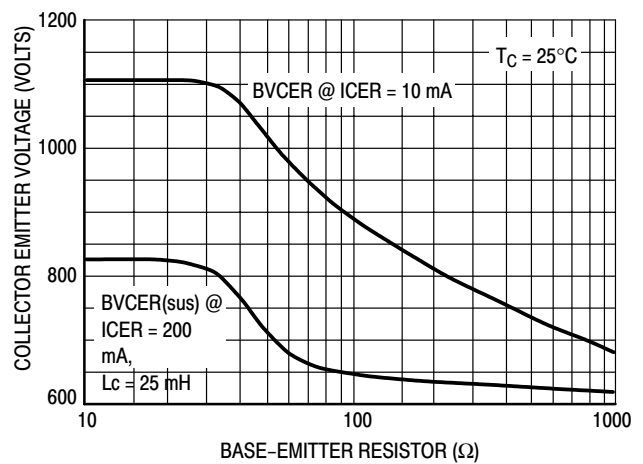


Figure 12. BVCER = f(R<sub>BE</sub>)

TYPICAL SWITCHING CHARACTERISTICS

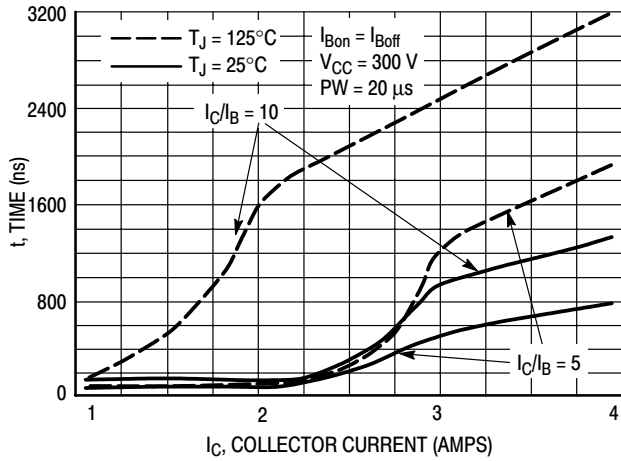


Figure 13. Resistive Switch Time,  $t_{on}$

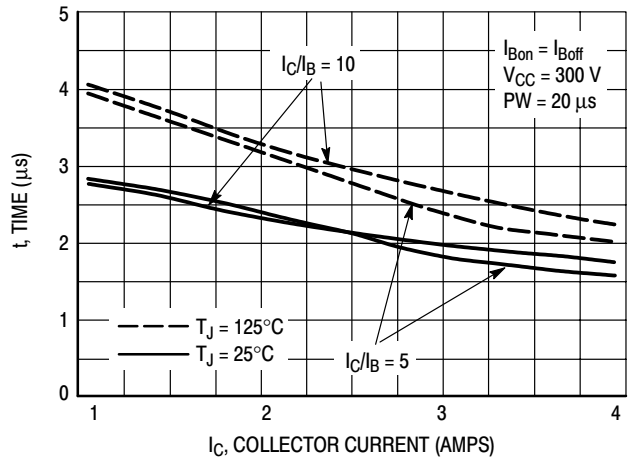


Figure 14. Resistive Switch Time,  $t_{off}$

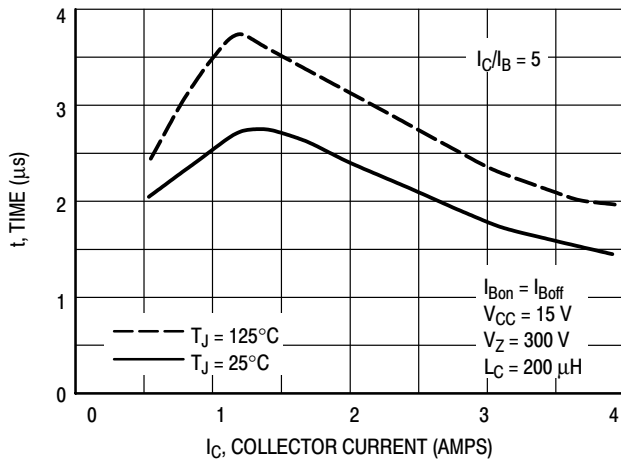


Figure 15. Inductive Storage Time,  $t_{si}$  @  $I_C/I_B = 5$

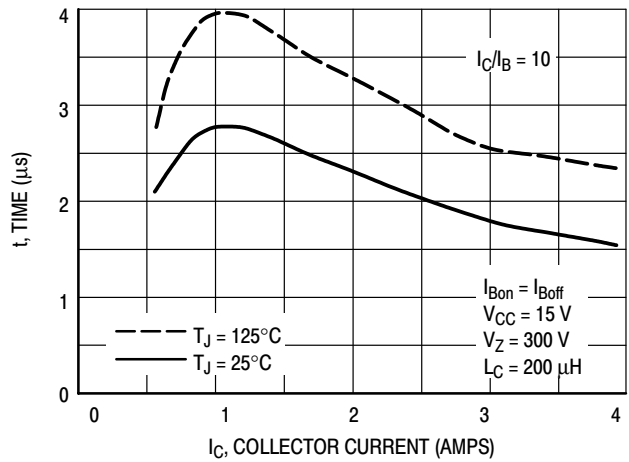


Figure 16. Inductive Storage Time,  $t_{si}$  @  $I_C/I_B = 10$

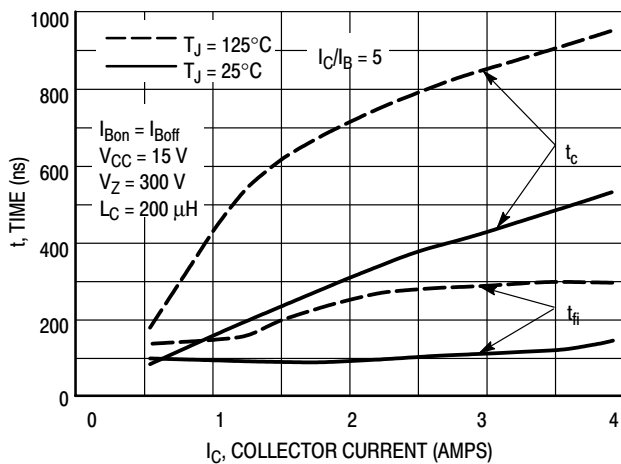


Figure 17. Inductive Switching Time,  $t_c$  and  $t_{fi}$  @  $I_C/I_B = 5$

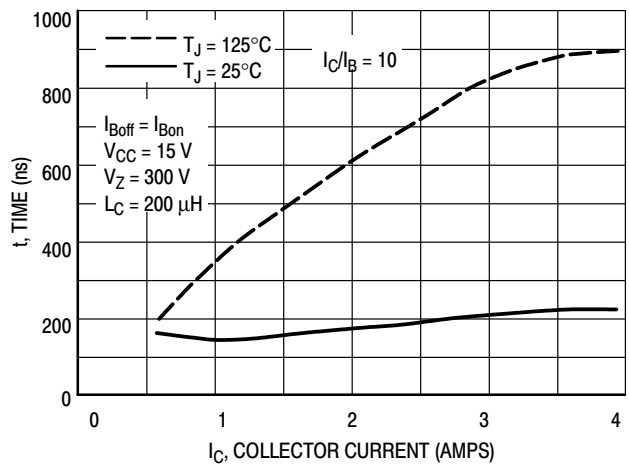


Figure 18. Inductive Switching Time,  $t_{fi}$  @  $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS

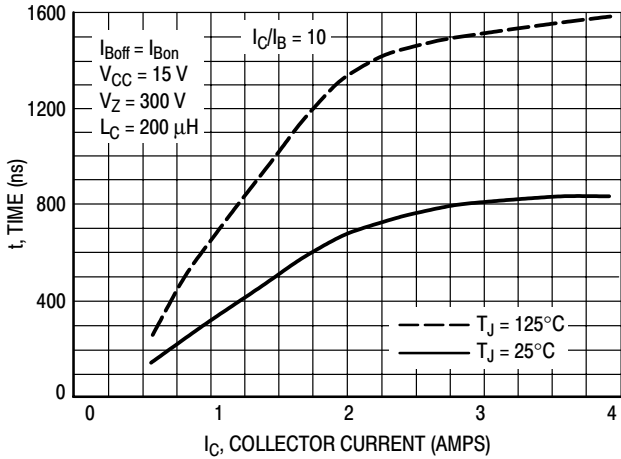


Figure 19. Inductive Switching,  $t_c$  @  $I_C/I_B = 10$

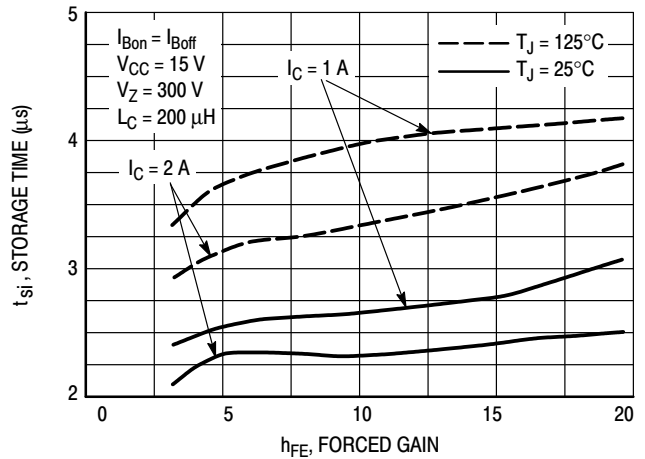


Figure 20. Inductive Storage Time

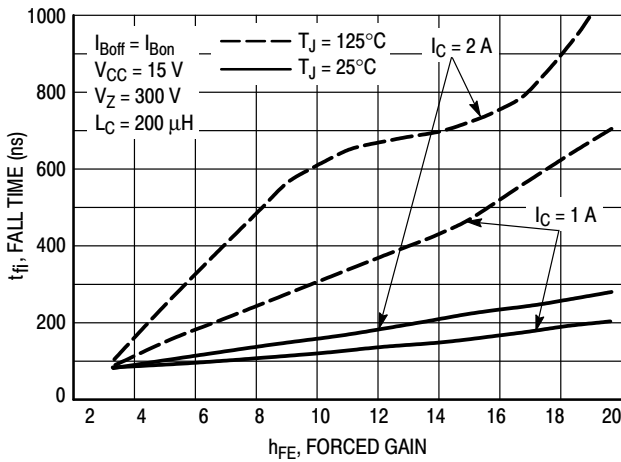


Figure 21. Inductive Fall Time

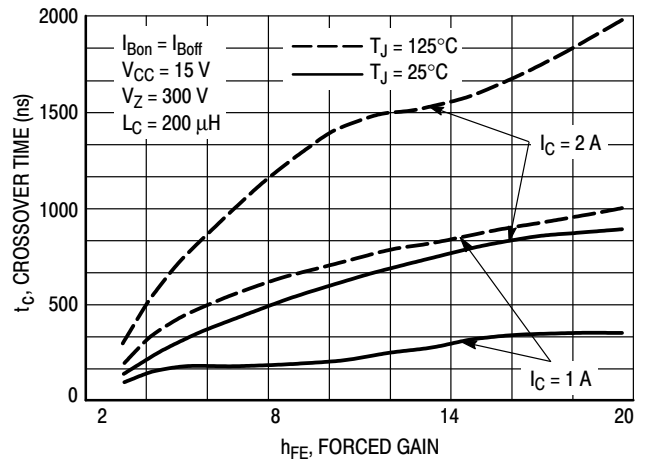


Figure 22. Inductive Crossover Time

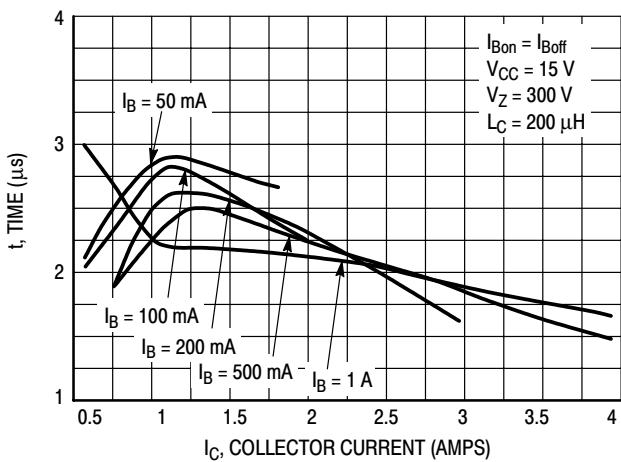


Figure 23. Inductive Storage Time,  $t_{si}$

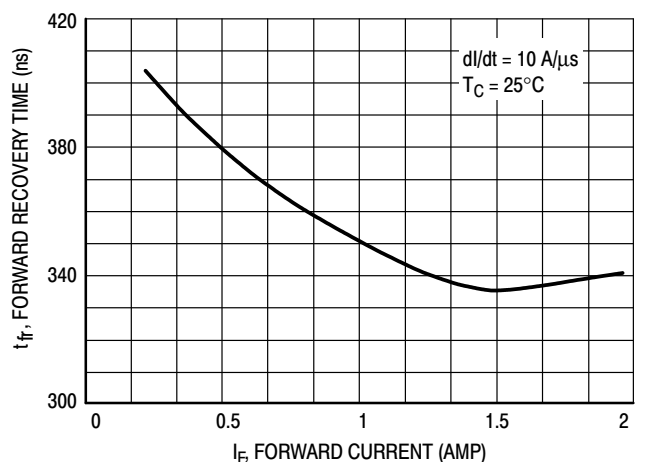


Figure 24. Forward Recovery Time,  $T_{FR}$

TYPICAL SWITCHING CHARACTERISTICS

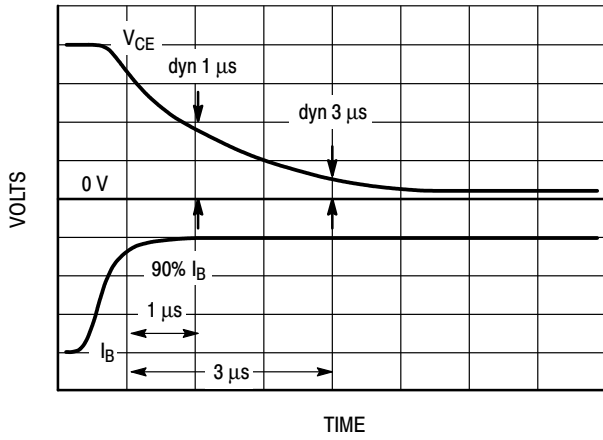


Figure 25. Dynamic Saturation Voltage Measurements

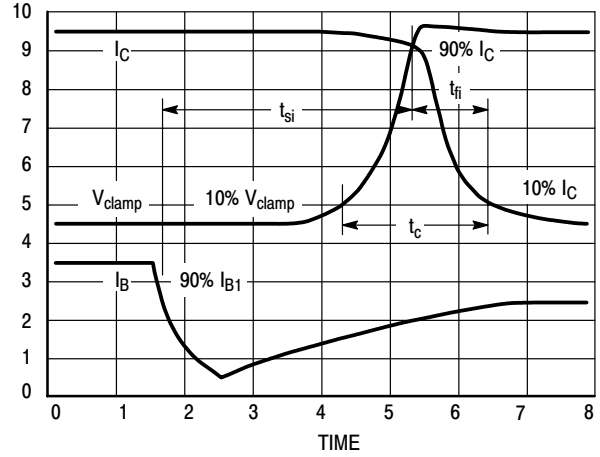


Figure 26. Inductive Switching Measurements

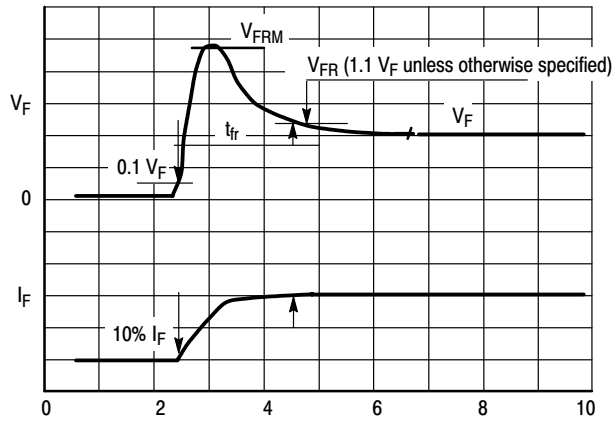


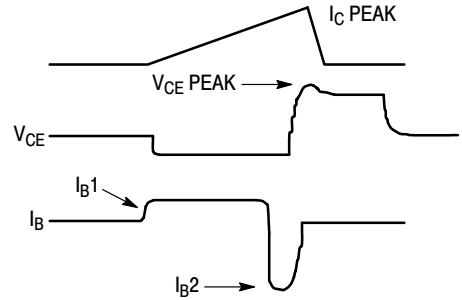
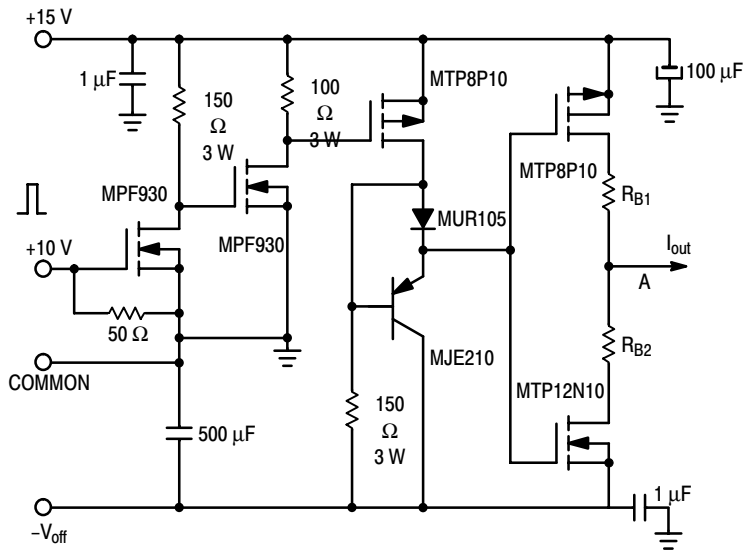
Figure 27.  $t_{fr}$  Measurements



# MJB18004D2T4

## TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



$V_{(BR)CEO(sus)}$   
 $L = 10 \text{ mH}$   
 $RB2 = \infty$   
 $V_{CC} = 20 \text{ Volts}$   
 $I_{C(pk)} = 100 \text{ mA}$

**Inductive Switching**  
 $L = 200 \mu\text{H}$   
 $RB2 = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $RB1$  selected for  
 desired  $I_{B1}$

**RBSOA**  
 $L = 500 \mu\text{H}$   
 $RB2 = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $RB1$  selected for  
 desired  $I_{B1}$

## TYPICAL CHARACTERISTICS

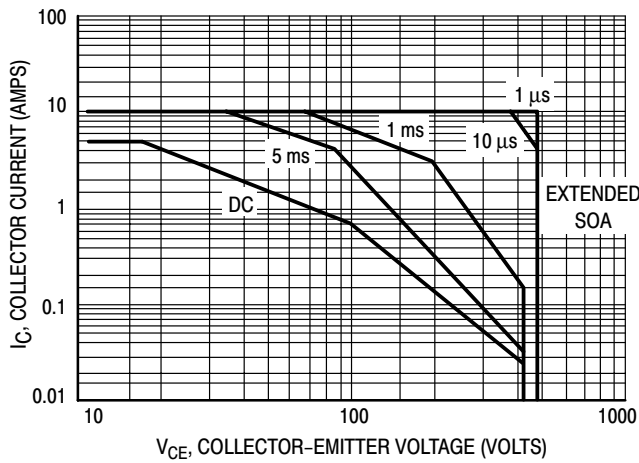


Figure 28. Forward Bias Safe Operating Area

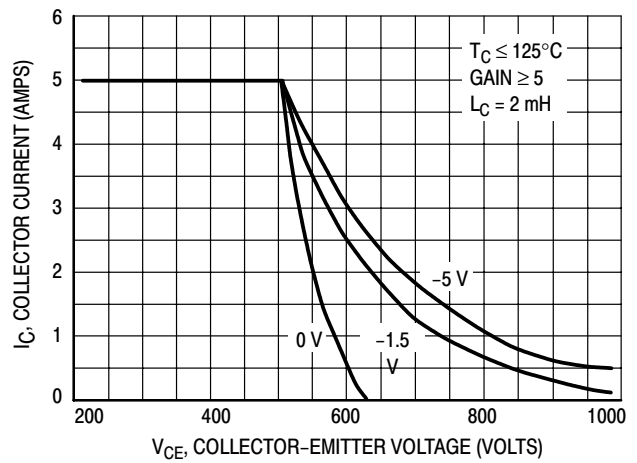


Figure 29. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

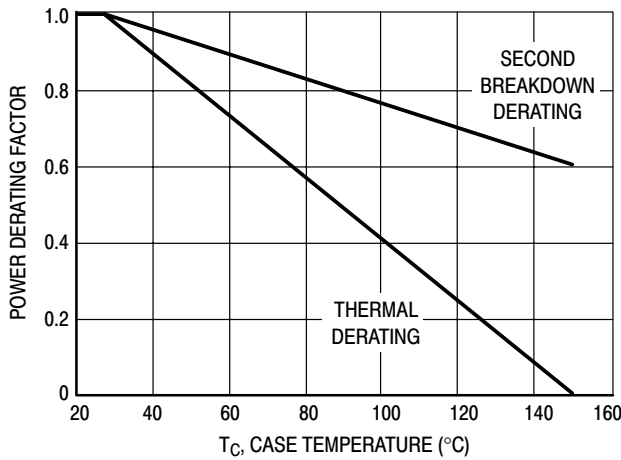


Figure 30. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on  $T_C = 25^\circ\text{C}$ ;  $T_J(\text{pk})$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

$T_J(\text{pk})$  may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse biased. The safe level is specified as a reverse-biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

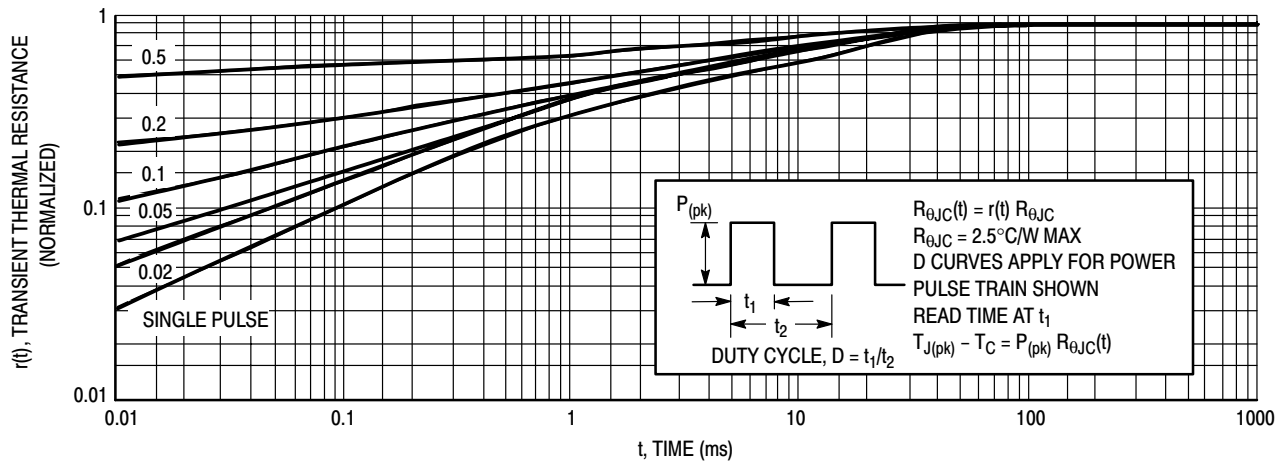


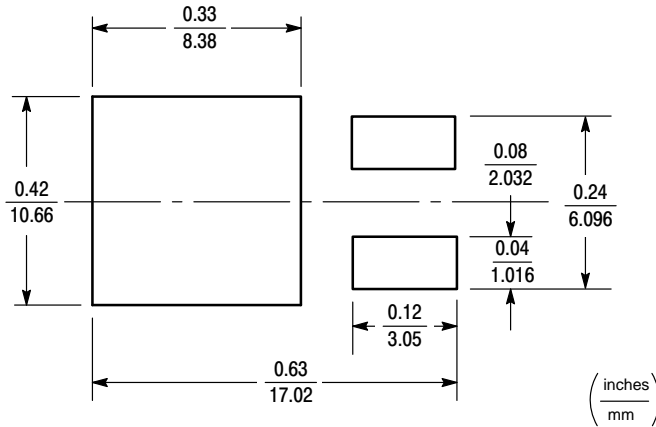
Figure 31. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for MJB18004D2T4

INFORMATION FOR USING THE D<sup>2</sup>PAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the Collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by  $T_{J(max)}$ , the maximum rated junction temperature of the die,  $R_{\theta JA}$ , the thermal resistance from the device junction to ambient, and the operating temperature,  $T_A$ . Using the values provided on the data sheet,  $P_D$  can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature  $T_A$  of 25°C, one can calculate the power dissipation of the device. For a D<sup>2</sup>PAK device,  $P_D$  is calculated as follows.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{50^\circ\text{C/W}} = 2.5 \text{ Watts}$$

The 50°C/W for the D<sup>2</sup>PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the Collector pad. By increasing the area of the collection pad, the power dissipation can be increased.

Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of  $R_{\theta JA}$  versus Collector pad area is shown in Figure 32

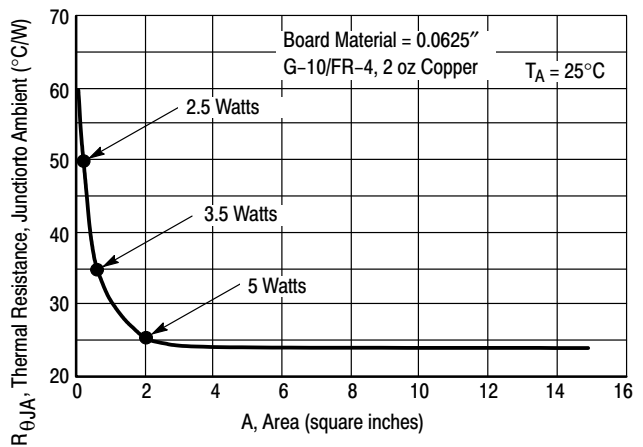


Figure 32. Thermal Resistance versus Collector Pad Area for the D<sup>2</sup>PAK Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad<sup>®</sup>. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC-59, SC-70/SOT-323, SOD-123, SOT-23, SOT-143, SOT-223, SO-8, SO-14, SO-16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D<sup>2</sup>PAK packages. If one uses a 1:1 opening to screen solder onto the Collector pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 33 shows a

typical stencil for the DPAK and D<sup>2</sup>PAK packages. The pattern of the opening in the stencil for the Collector pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

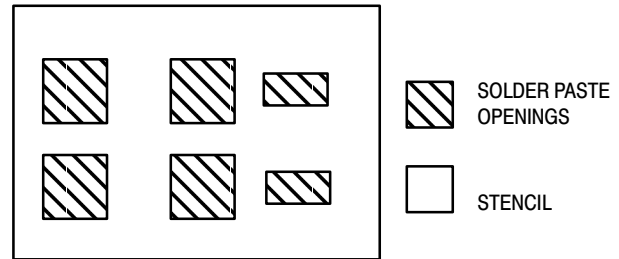


Figure 33. Typical Stencil for DPAK and D<sup>2</sup>PAK Packages

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.

- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

\* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D<sup>2</sup>PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 34 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time.

The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

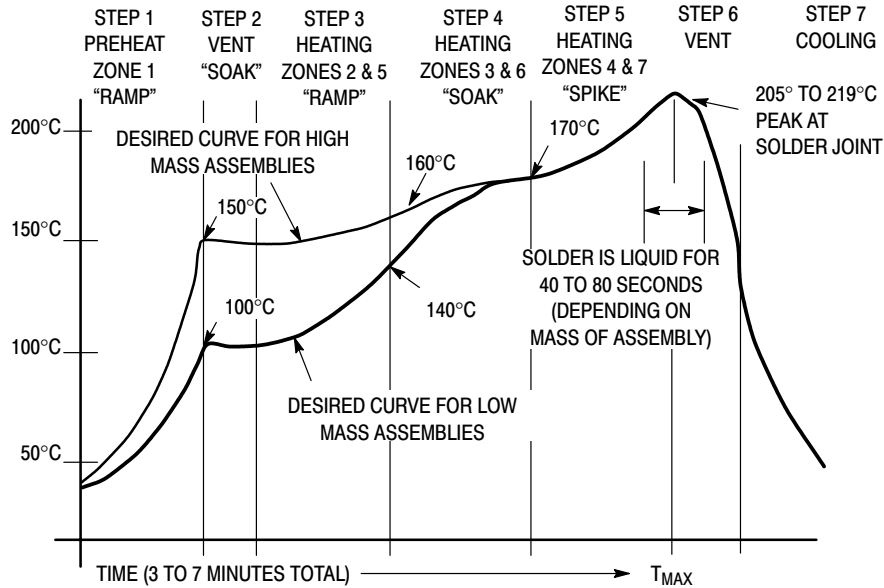


Figure 34. Typical Solder Heating Profile

# MJB41C (NPN), MJB42C (PNP)

Preferred Devices

## Complementary Silicon Plastic Power Transistors

### D<sup>2</sup>PAK for Surface Mount

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Lead Formed Version in 16 mm Tape & Reel ("T4" Suffix)
- Electrically the Same as TIP41 and T1P42 Series

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	100	Vdc
Collector–Base Voltage	$V_{CB}$	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current – Continuous – Peak	$I_C$	6.0 10	Adc
Base Current	$I_B$	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	65 0.52	Watts $\text{W}/^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016	Watts $\text{W}/^\circ\text{C}$
Unclamped Inductive Load Energy (Note 1.)	E	62.5	mJ
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient (Note 2.)	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	$T_L$	260	$^\circ\text{C}$

1.  $I_C = 2.5\text{ A}$ ,  $L = 20\text{ mH}$ , P.R.F. = 10 Hz,  $V_{CC} = 10\text{ V}$ ,  $R_{BE} = 100\ \Omega$
2. When surface mounted to an FR-4 board using the minimum recommended pad size.



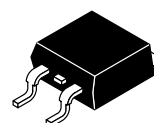
ON Semiconductor™

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### COMPLEMENTARY SILICON POWER TRANSISTORS

**6 AMPERES**  
**100 VOLTS**  
**65 WATTS**

#### MARKING DIAGRAM



**D<sup>2</sup>PAK  
CASE 418B  
STYLE 1**



MJB4xC = Specific Device Code  
x = 1 or 2  
Y = Year  
WW = Work Week

#### ORDERING INFORMATION

Device	Package	Shipping
MJB41C	D <sup>2</sup> PAK	50 Units/Rail
MJB41CT4	D <sup>2</sup> PAK	800/Tape & Reel
MJB42C	D <sup>2</sup> PAK	50 Units/Rail
MJB42CT4	D <sup>2</sup> PAK	800/Tape & Reel

**Preferred** devices are recommended choices for future use and best overall value.

# MJB41C (NPN), MJB42C (PNP)

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 3.) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	0.7	mAdc
Collector Cutoff Current ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB} = 0$ )	$I_{CES}$	–	100	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	50	$\mu\text{Adc}$

## ON CHARACTERISTICS (Note 3.)

DC Current Gain ( $I_C = 0.3\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	30 15	– 75	–
Collector–Emitter Saturation Voltage ( $I_C = 6.0\text{ Adc}$ , $I_B = 600\text{ mAdc}$ )	$V_{CE(sat)}$	–	1.5	Vdc
Base–Emitter On Voltage ( $I_C = 6.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	–	2.0	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	3.0	–	MHz
Small–Signal Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	20	–	–

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

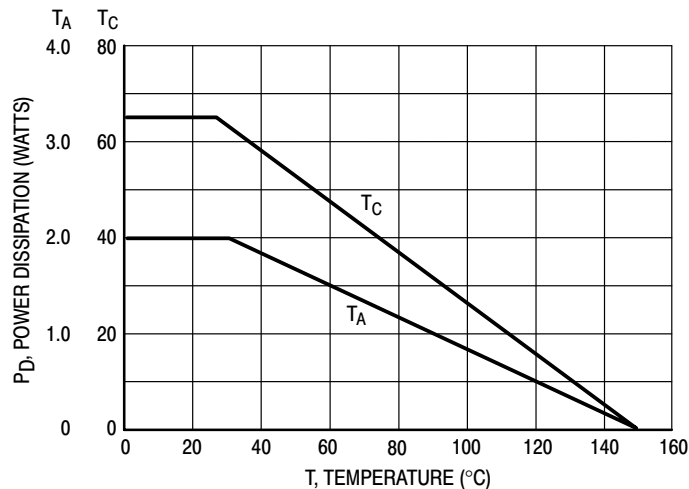


Figure 35. Power Derating

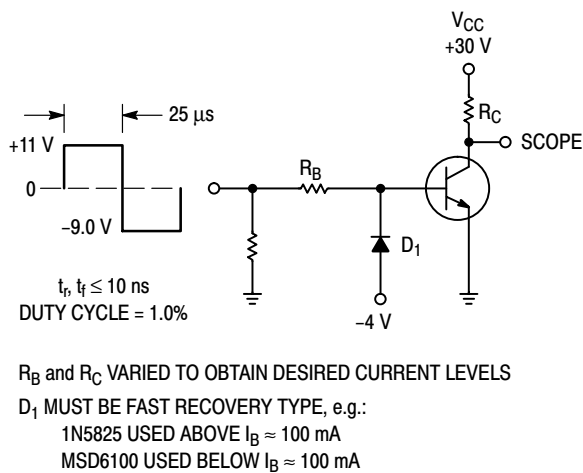


Figure 36. Switching Time Test Circuit

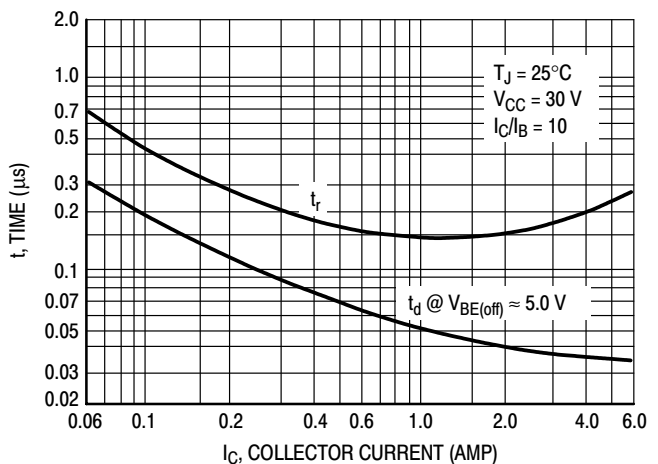


Figure 37. Turn–On Time

# MJB41C (NPN), MJB42C (PNP)

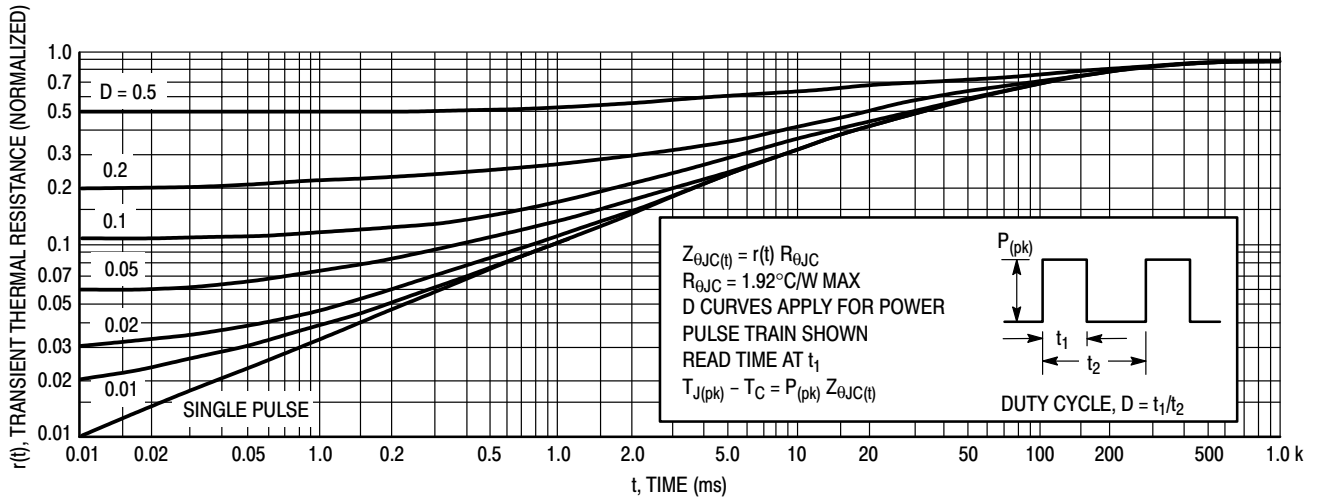


Figure 38. Thermal Response

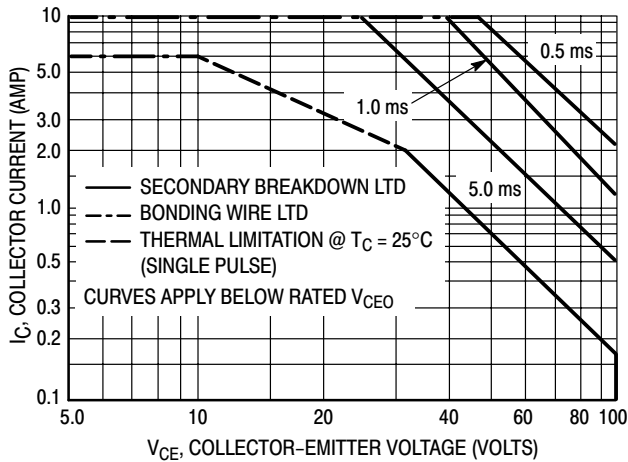


Figure 39. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

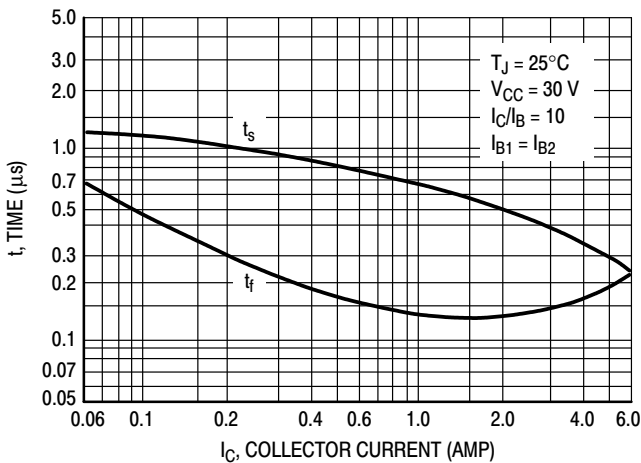


Figure 40. Turn-Off Time

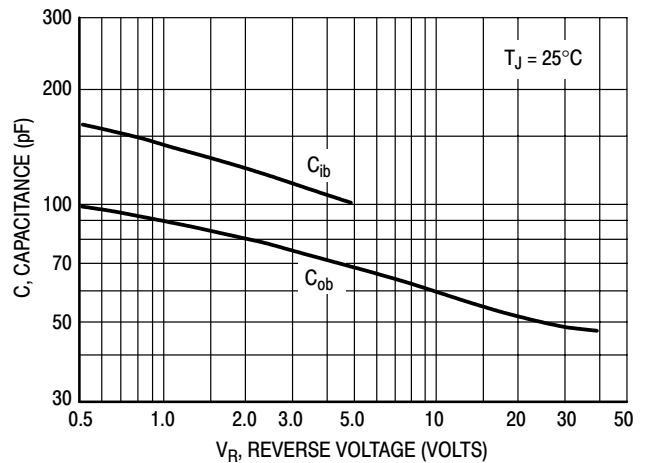


Figure 41. Capacitance



# MJB41C (NPN), MJB42C (PNP)

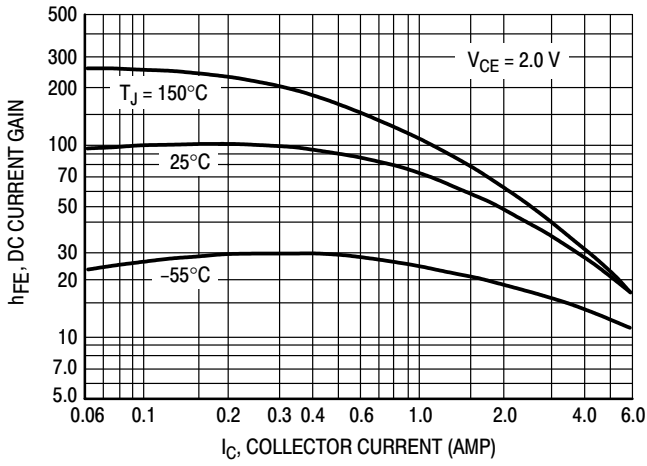


Figure 42. DC Current Gain

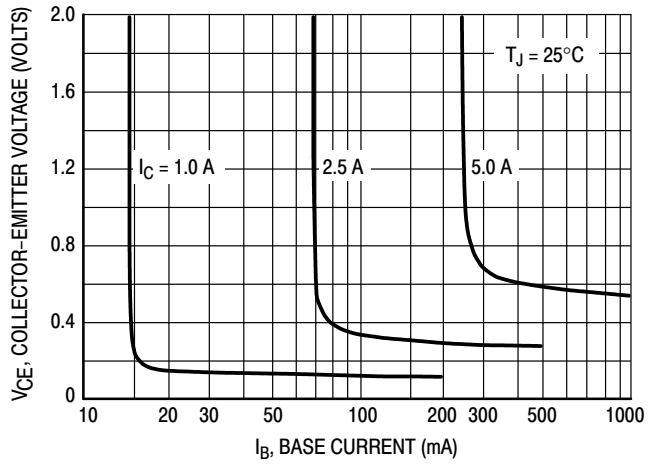


Figure 43. Collector Saturation Region

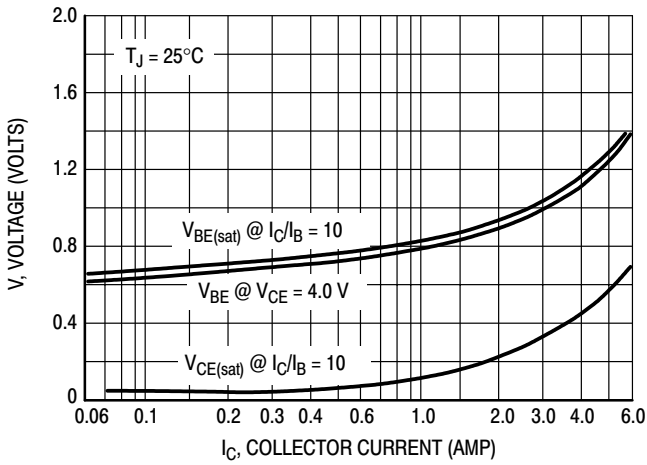


Figure 44. "On" Voltages

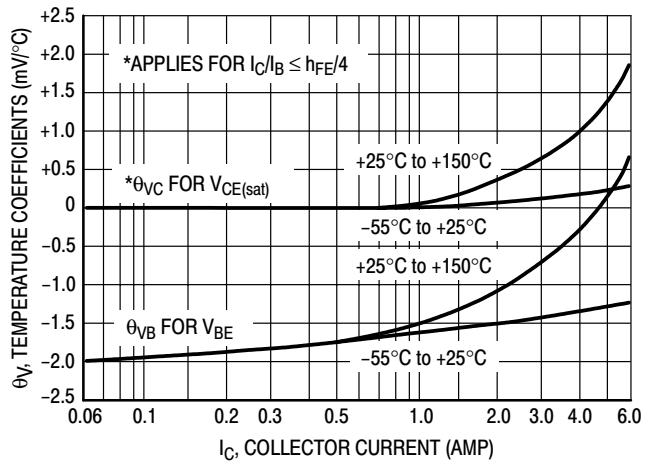


Figure 45. Temperature Coefficients

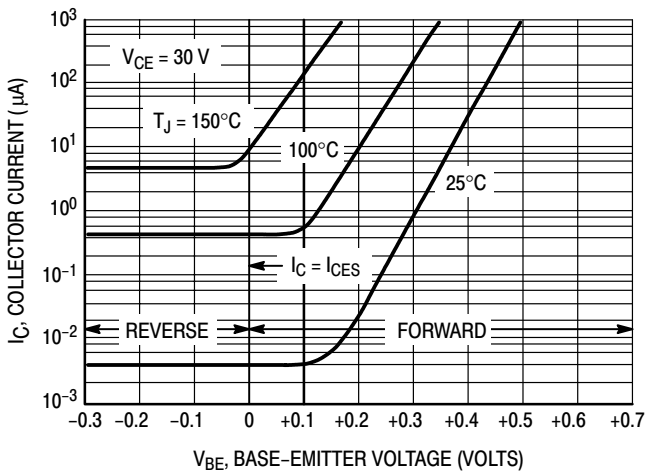


Figure 46. Collector Cut-Off Region

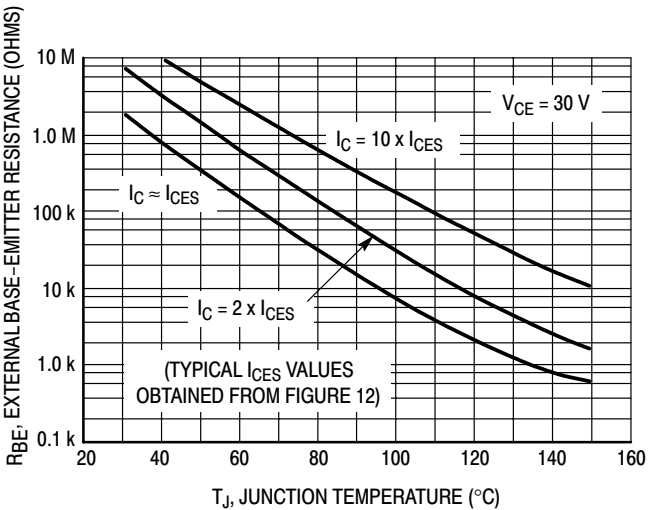


Figure 47. Effects of Base-Emitter Resistance

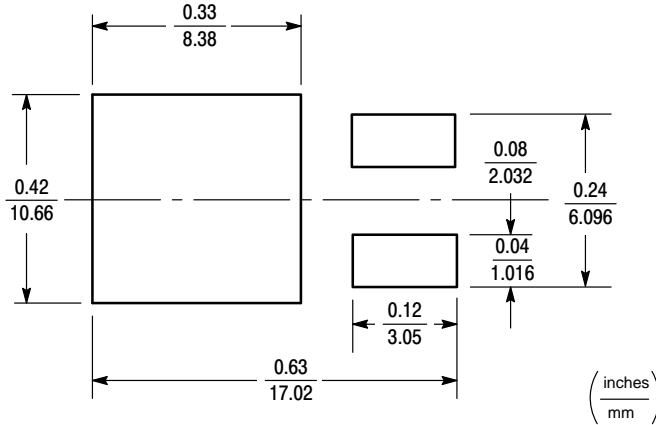
# MJB41C (NPN), MJB42C (PNP)

## INFORMATION FOR USING THE D<sup>2</sup>PAK SURFACE MOUNT PACKAGE

### RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



### POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the Collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by  $T_{J(max)}$ , the maximum rated junction temperature of the die,  $R_{\theta JA}$ , the thermal resistance from the device junction to ambient, and the operating temperature,  $T_A$ . Using the values provided on the data sheet,  $P_D$  can be calculated as follows:

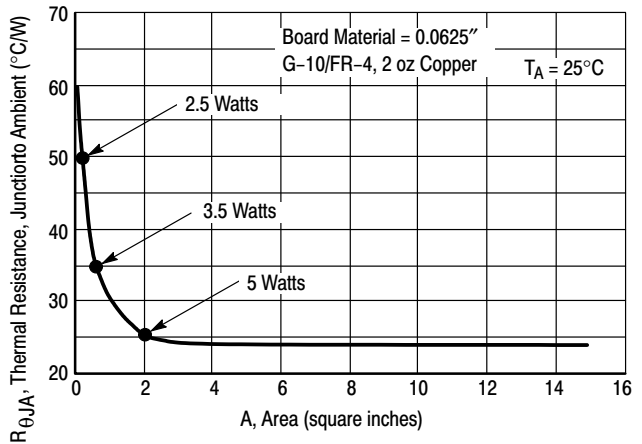
$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature  $T_A$  of 25°C, one can calculate the power dissipation of the device. For a D<sup>2</sup>PAK device,  $P_D$  is calculated as follows.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{50^\circ\text{C/W}} = 2.5 \text{ Watts}$$

The 50°C/W for the D<sup>2</sup>PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the Collector pad. By increasing the area of the collection pad, the power dissipation can be increased.

Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of  $R_{\theta JA}$  versus Collector pad area is shown in Figure 48



**Figure 48. Thermal Resistance versus Collector Pad Area for the D<sup>2</sup>PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad<sup>®</sup>. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## MJB41C (NPN), MJB42C (PNP)

### SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC-59, SC-70/SOT-323, SOD-123, SOT-23, SOT-143, SOT-223, SO-8, SO-14, SO-16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D<sup>2</sup>PAK packages. If one uses a 1:1 opening to screen solder onto the Collector pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 49 shows a

typical stencil for the DPAK and D<sup>2</sup>PAK packages. The pattern of the opening in the stencil for the Collector pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

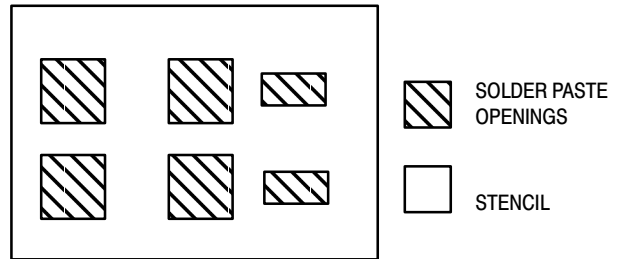


Figure 49. Typical Stencil for DPAK and D<sup>2</sup>PAK Packages

### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.

- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

\* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D<sup>2</sup>PAK is not recommended for wave soldering.

# MJB41C (NPN), MJB42C (PNP)

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 50 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time.

The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

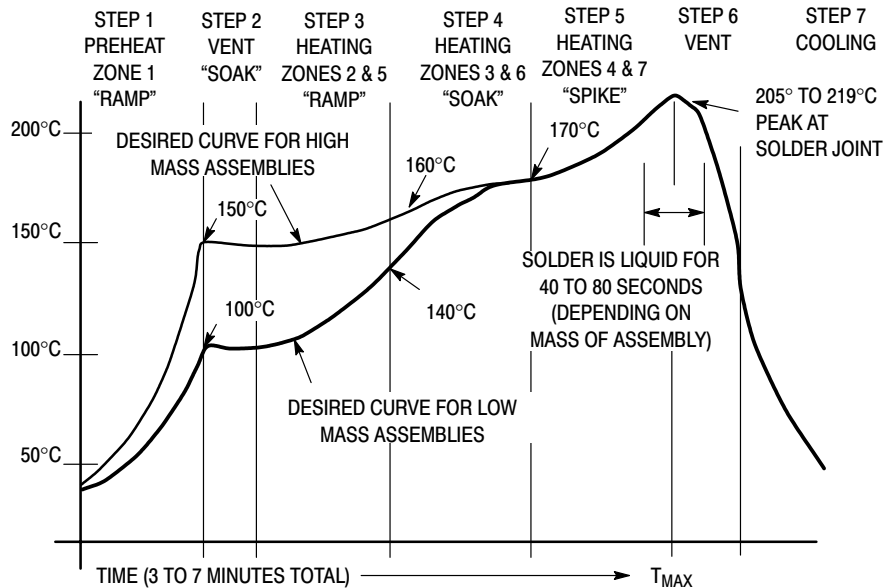


Figure 50. Typical Solder Heating Profile

# MJB44H11 (NPN), MJB45H11 (PNP)

Preferred Devices

## Complementary Power Transistors

### D<sup>2</sup>PAK for Surface Mount

... for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector–Emitter Saturation Voltage –  
 $V_{CE(sat)} = 1.0 \text{ V (Max) @ } 8.0 \text{ A}$
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
Collector Current – Continuous – Peak	$I_C$	10 20	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	50 1.67	Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–55 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^\circ\text{C/W}$

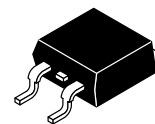


ON Semiconductor™

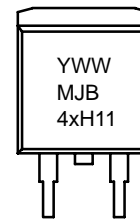
<http://onsemi.com>

**SILICON POWER  
TRANSISTORS  
10 AMPERES  
80 VOLTS  
50 WATTS**

#### MARKING DIAGRAM



**D<sup>2</sup>PAK  
CASE 418B  
STYLE 1**



Y = Year  
WW = Work Week  
MJB4xH11 = Specific Device Code  
x = 4 or 5

#### ORDERING INFORMATION

Device	Package	Shipping
MJB44H11	D <sup>2</sup> PAK	50 Units/Rail
MJB44H11T4	D <sup>2</sup> PAK	800/Tape & Reel
MJB45H11	D <sup>2</sup> PAK	50 Units/Rail
MJB45H11T4	D <sup>2</sup> PAK	800/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

## MJB44H11 (NPN), MJB45H11 (PNP)

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CE(sus)}$	80	–	–	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CE0}$ , $V_{BE} = 0$ )	$I_{CES}$	–	–	10	$\mu\text{A}$
Emitter Cutoff Current ( $V_{EB} = 5\text{ Vdc}$ )	$I_{EBO}$	–	–	50	$\mu\text{A}$

### ON CHARACTERISTICS

Collector–Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )	$V_{CE(sat)}$	–	–	1.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.8\text{ Adc}$ )	$V_{BE(sat)}$	–	–	1.5	Vdc
DC Current Gain ( $V_{CE} = 1\text{ Vdc}$ , $I_C = 2\text{ Adc}$ )	$h_{FE}$	60	–	–	–
DC Current Gain ( $V_{CE} = 1\text{ Vdc}$ , $I_C = 4\text{ Adc}$ )		40	–	–	–

### DYNAMIC CHARACTERISTICS

Collector Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )	MJB44H11 MJB45H11	$C_{cb}$	– –	130 230	– –	$\mu\text{F}$
Gain Bandwidth Product ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 20\text{ MHz}$ )	MJB44H11 MJB45H11	$f_T$	– –	50 40	– –	MHz

### SWITCHING TIMES

Delay and Rise Times ( $I_C = 5\text{ Adc}$ , $I_{B1} = 0.5\text{ Adc}$ )	MJB44H11 MJB45H11	$t_d + t_r$	– –	300 135	– –	ns
Storage Time ( $I_C = 5\text{ Adc}$ , $I_{B1} = I_{B2} = 0.5\text{ Adc}$ )	MJB44H11 MJB45H11	$t_s$	– –	500 500	– –	ns
Fall Time ( $I_C = 5\text{ Adc}$ , $I_{B1} = I_{B2} = 0.5\text{ Adc}$ )	MJB44H11 MJB45H11	$t_f$	– –	140 100	– –	ns

# MJB44H11 (NPN), MJB45H11 (PNP)

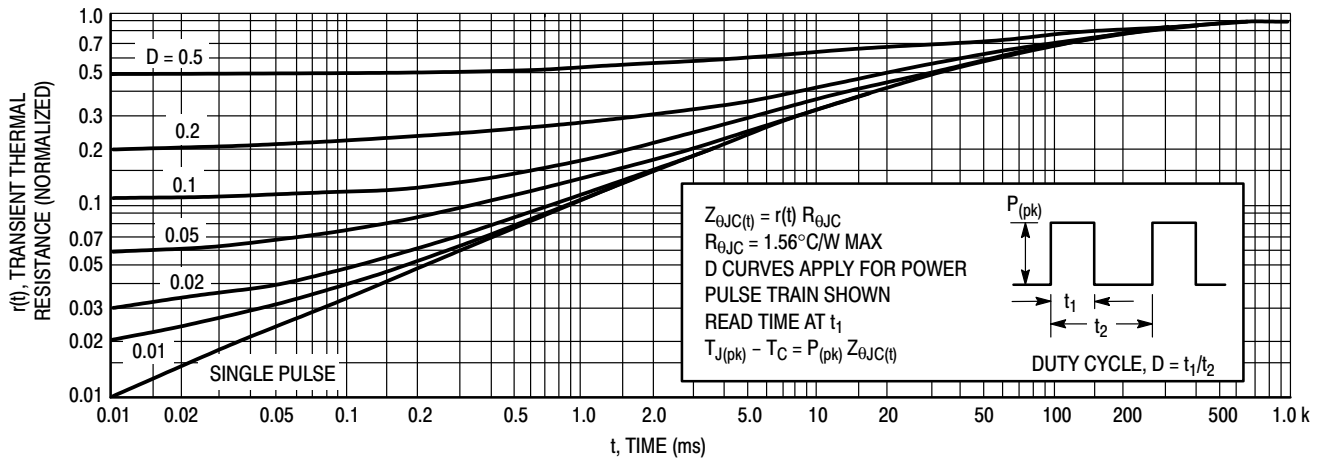


Figure 1. Thermal Response

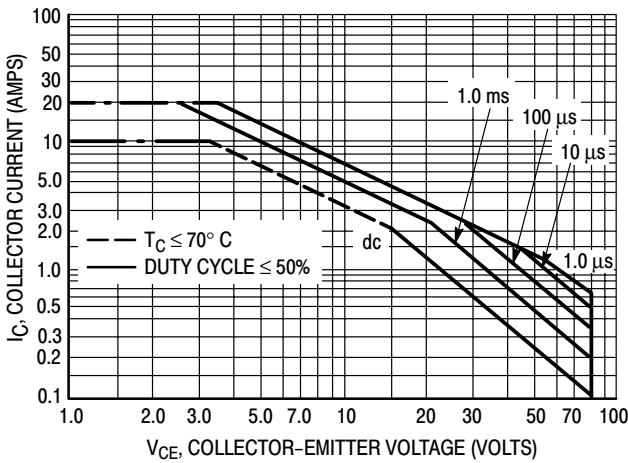


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

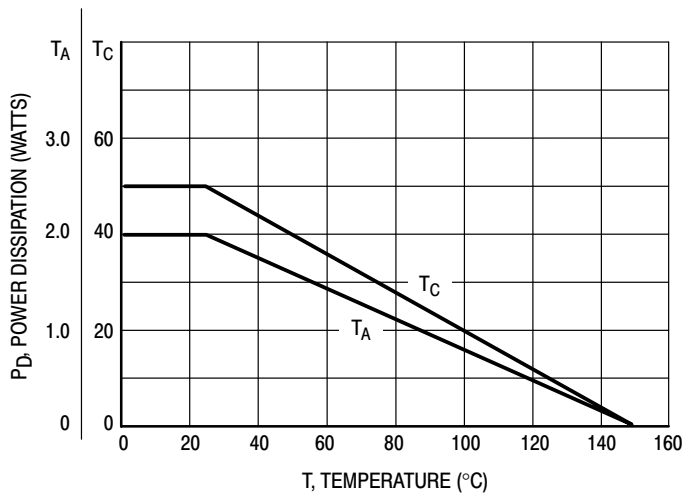


Figure 3. Power Derating

# MJB44H11 (NPN), MJB45H11 (PNP)

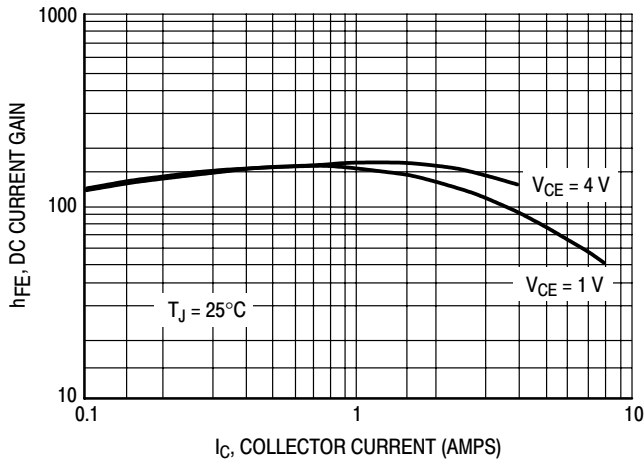


Figure 4. MJB44H11 DC Current Gain

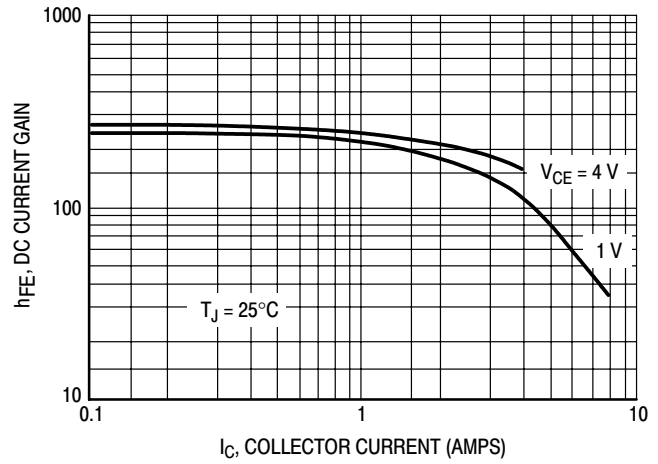


Figure 5. MJB45H11 DC Current Gain

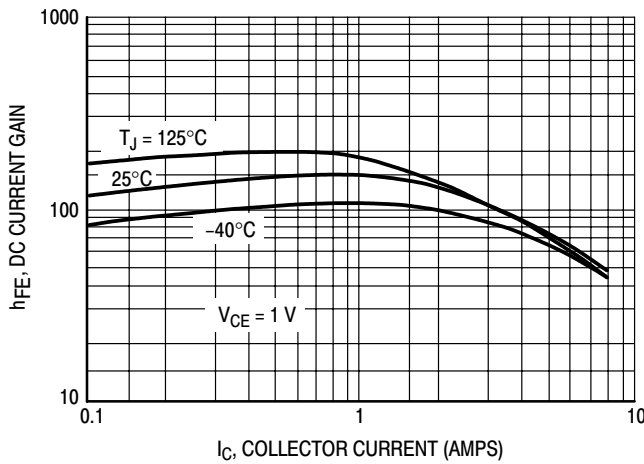


Figure 6. MJB44H11 Current Gain versus Temperature

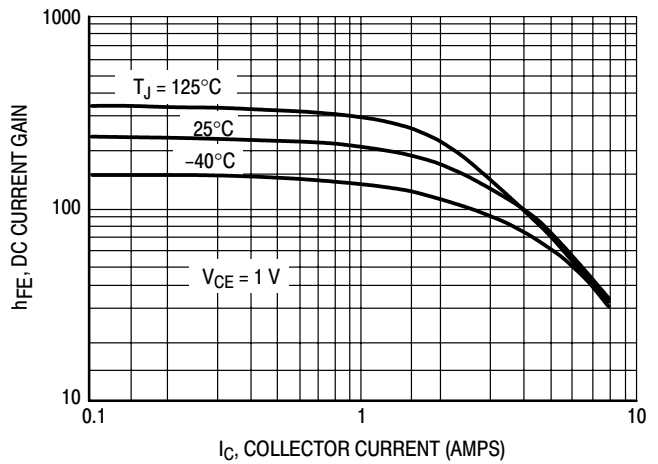


Figure 7. MJB45H11 Current Gain versus Temperature

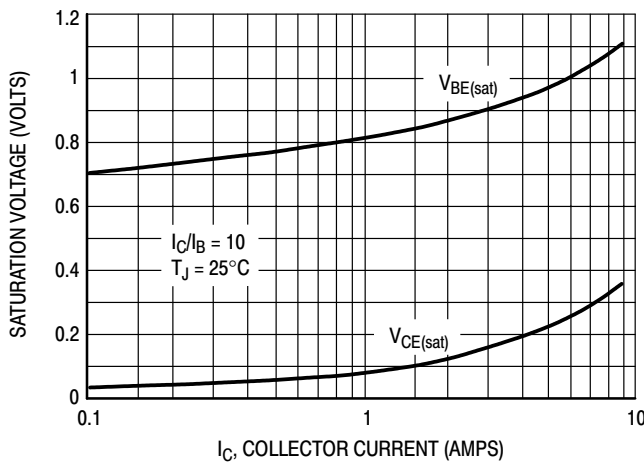


Figure 8. MJB44H11 On-Voltages

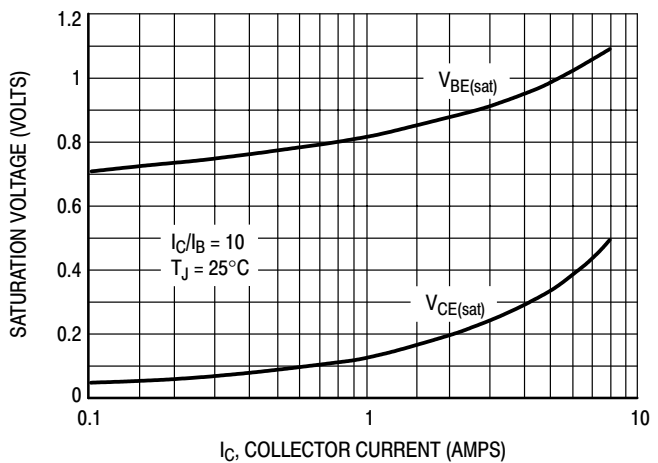


Figure 9. MJB45H11 On-Voltages

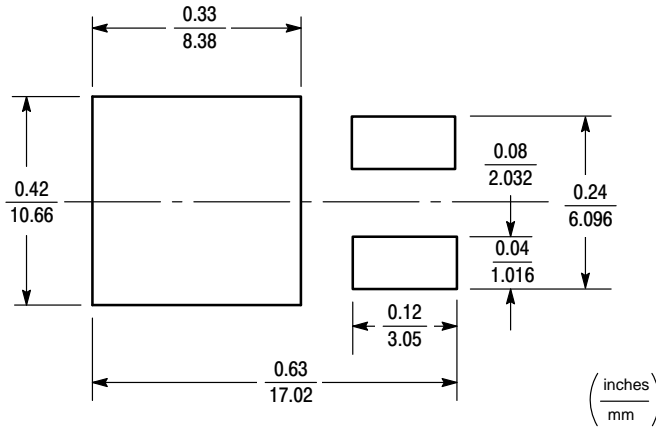


INFORMATION FOR USING THE D<sup>2</sup>PAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the Collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by  $T_{J(max)}$ , the maximum rated junction temperature of the die,  $R_{\theta JA}$ , the thermal resistance from the device junction to ambient, and the operating temperature,  $T_A$ . Using the values provided on the data sheet,  $P_D$  can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature  $T_A$  of 25°C, one can calculate the power dissipation of the device. For a D<sup>2</sup>PAK device,  $P_D$  is calculated as follows.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{50^\circ\text{C/W}} = 2.5 \text{ Watts}$$

The 50°C/W for the D<sup>2</sup>PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the Collector pad. By increasing the area of the collection pad, the power dissipation can be increased.

Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of  $R_{\theta JA}$  versus Collector pad area is shown in Figure 10

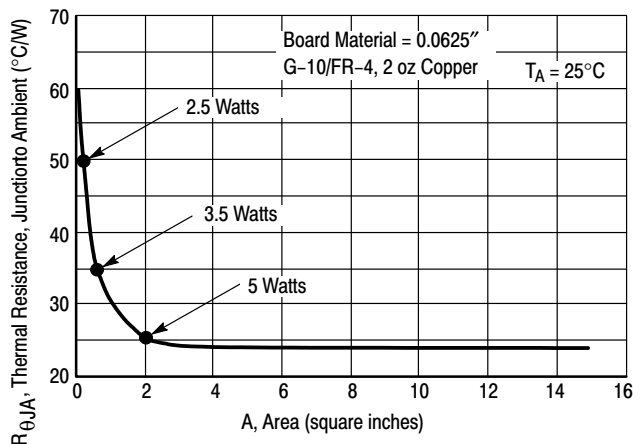


Figure 10. Thermal Resistance versus Collector Pad Area for the D<sup>2</sup>PAK Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad<sup>®</sup>. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## MJB44H11 (NPN), MJB45H11 (PNP)

### SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC-59, SC-70/SOT-323, SOD-123, SOT-23, SOT-143, SOT-223, SO-8, SO-14, SO-16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D<sup>2</sup>PAK packages. If one uses a 1:1 opening to screen solder onto the Collector pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 11 shows a

typical stencil for the DPAK and D<sup>2</sup>PAK packages. The pattern of the opening in the stencil for the Collector pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

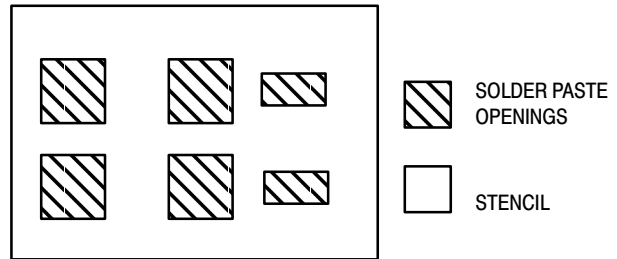


Figure 11. Typical Stencil for DPAK and D<sup>2</sup>PAK Packages

### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.

- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

\* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D<sup>2</sup>PAK is not recommended for wave soldering.

# MJB44H11 (NPN), MJB45H11 (PNP)

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time.

The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

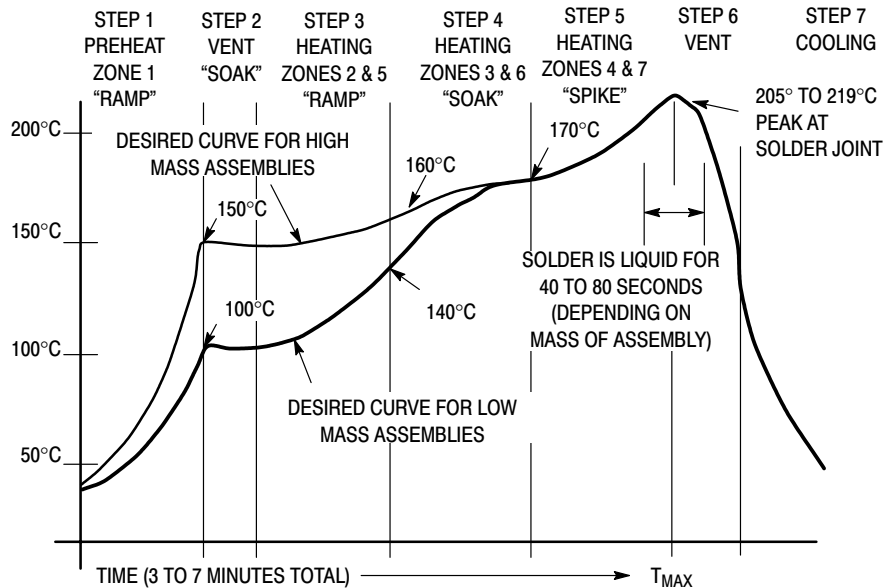


Figure 12. Typical Solder Heating Profile

# Complementary Darlington Power Transistors

## DPAK For Surface Mount Applications

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Surface Mount Replacements for TIP110–TIP117 Series
- Monolithic Construction With Built-in Base–Emitter Shunt Resistors
- High DC Current Gain —  
 $h_{FE} = 2500$  (Typ) @  $I_C = 2.0$  Adc
- Complementary Pairs Simplifies Designs

### MAXIMUM RATINGS

Rating	Symbol	MJD112 MJD117	Unit
Collector–Emitter Voltage	$V_{CEO}$	100	Vdc
Collector–Base Voltage	$V_{CB}$	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
Collector Current — Continuous Peak	$I_C$	2 4	Adc
Base Current	$I_B$	50	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	Watts W/ $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

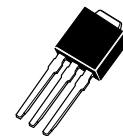
**NPN  
MJD112\***  
**PNP  
MJD117\***

\*ON Semiconductor Preferred Device

**SILICON  
POWER TRANSISTORS  
2 AMPERES  
100 VOLTS  
20 WATTS**

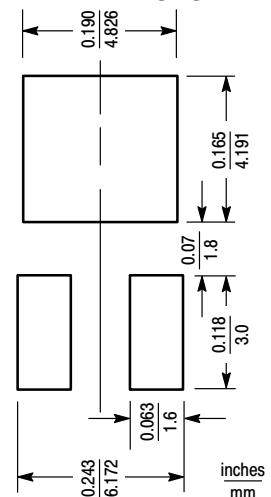


CASE 369A-13



CASE 369-07

### MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJD112 MJD117

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^{\circ}C/W$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	$^{\circ}C/W$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CE(sus)}$	100	—	Vdc
Collector Cutoff Current ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	20	$\mu\text{A}$
Collector Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	20	$\mu\text{A}$
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	2	$\text{mA}$
Collector–Cutoff Current ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	10	$\mu\text{A}$
Emitter–Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	2	$\text{mA}$

### ON CHARACTERISTICS

DC Current Gain ( $I_C = 0.5\text{ A}$ , $V_{CE} = 3\text{ Vdc}$ ) ( $I_C = 2\text{ A}$ , $V_{CE} = 3\text{ Vdc}$ ) ( $I_C = 4\text{ A}$ , $V_{CE} = 3\text{ Vdc}$ )	$h_{FE}$	500 1000 200	— 12,000 —	—
Collector–Emitter Saturation Voltage ( $I_C = 2\text{ A}$ , $I_B = 8\text{ mA}$ ) ( $I_C = 4\text{ A}$ , $I_B = 40\text{ mA}$ )	$V_{CE(sat)}$	— —	2 3	Vdc
Base–Emitter Saturation Voltage ( $I_C = 4\text{ A}$ , $I_B = 40\text{ mA}$ )	$V_{BE(sat)}$	—	4	Vdc
Base–Emitter On Voltage ( $I_C = 2\text{ A}$ , $V_{CE} = 3\text{ Vdc}$ )	$V_{BE(on)}$	—	2.8	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 0.75\text{ A}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$f_T$	25	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	— —	200 100	$\text{pF}$
	MJD117			
	MJD112			

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

\*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

# MJD112 MJD117

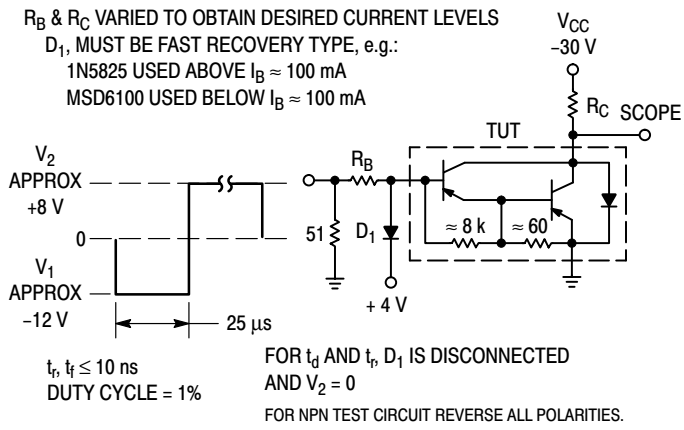


Figure 13. Switching Times Test Circuit

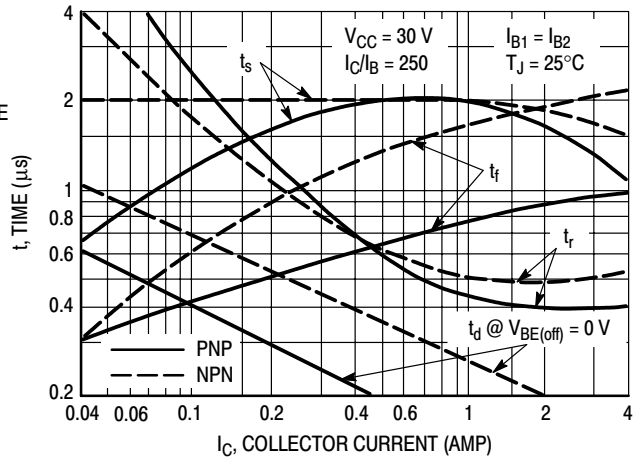


Figure 14. Switching Times

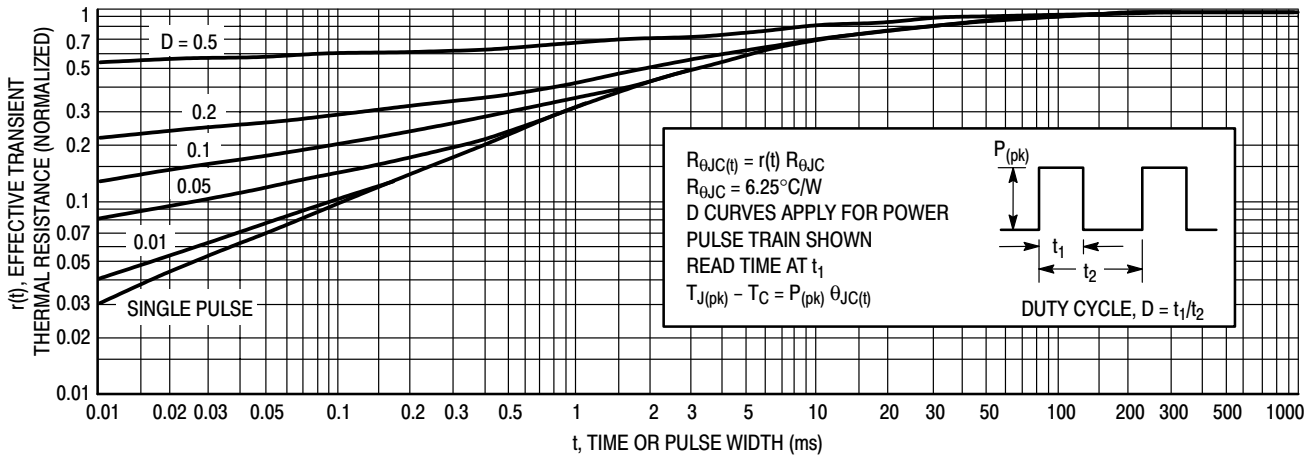


Figure 15. Thermal Response

ACTIVE-REGION SAFE-OPERATING AREA

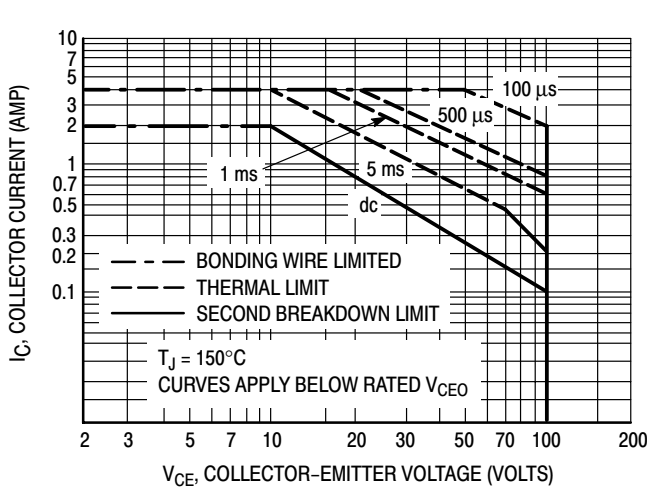


Figure 16. Maximum Rated Forward Biased Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 17 and 18 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

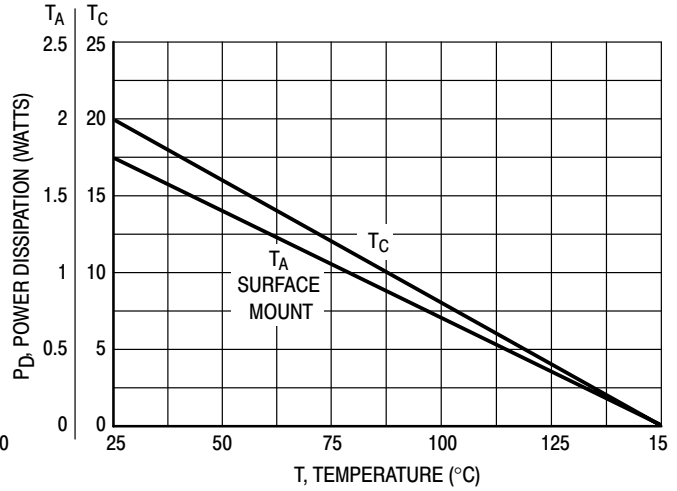


Figure 17. Power Derating

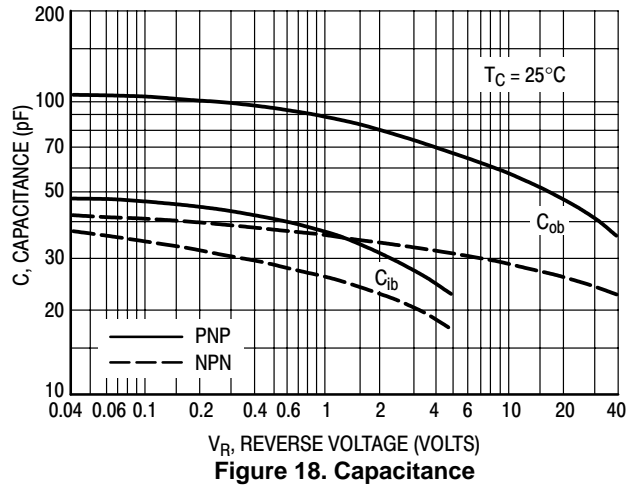


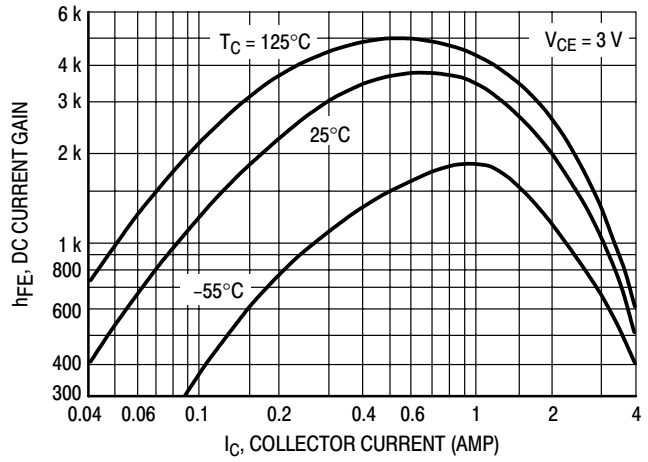
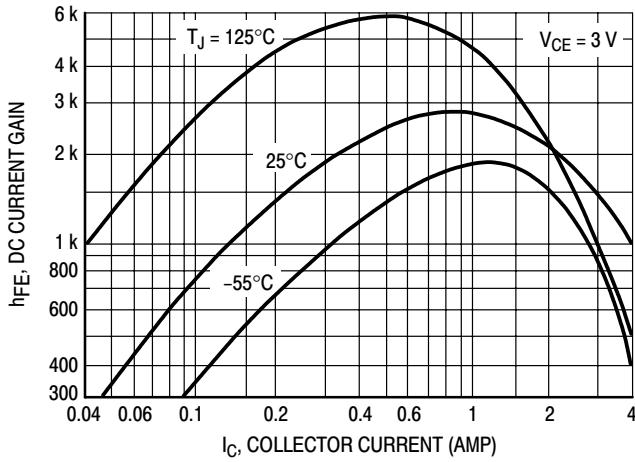
Figure 18. Capacitance

# MJD112 MJD117

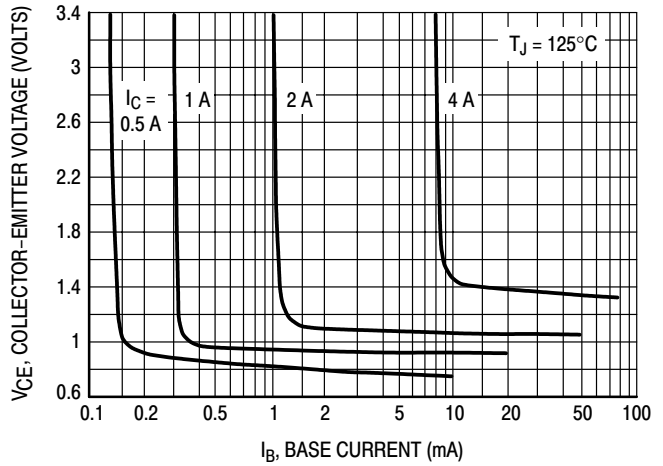
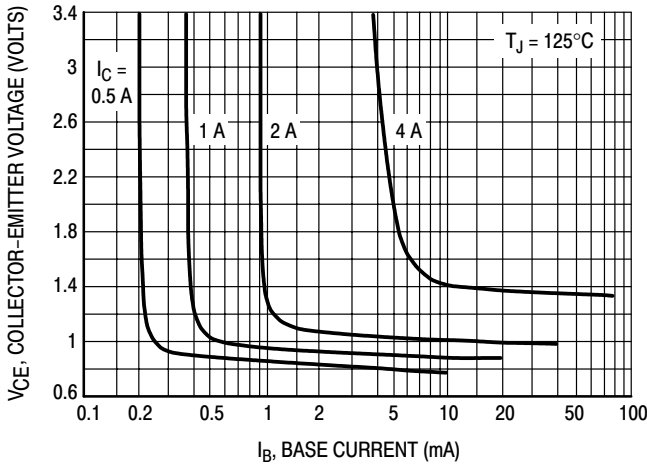
## TYPICAL ELECTRICAL CHARACTERISTICS

**NPN MJD112**

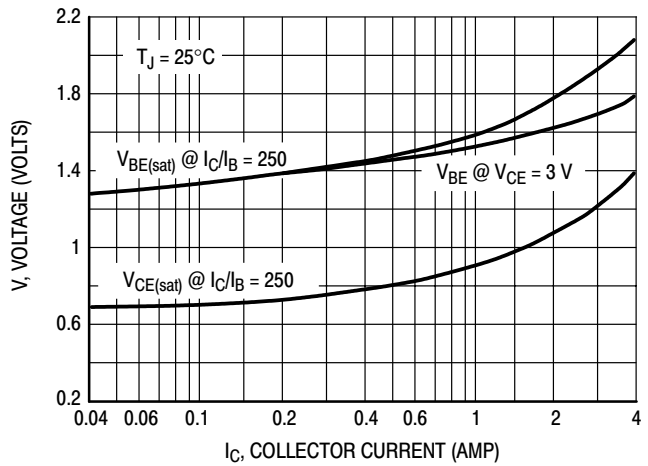
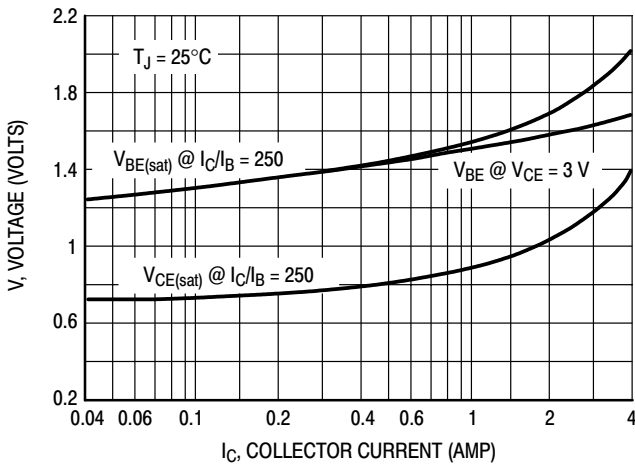
**PNP MJD117**



**Figure 19. DC Current Gain**



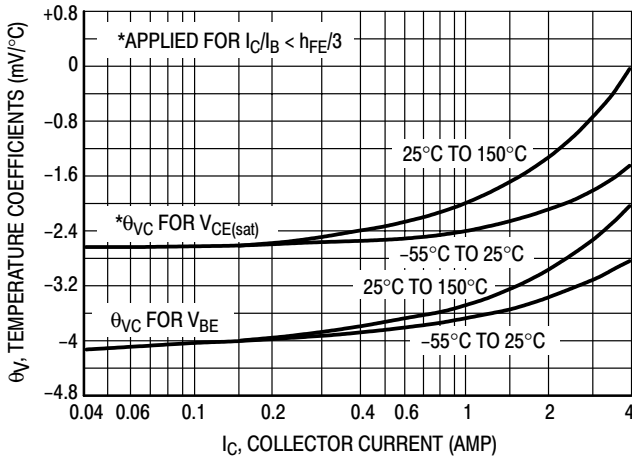
**Figure 20. Collector Saturation Region**



**Figure 21. "On Voltages"**



NPN MJD112



PNP MJD117

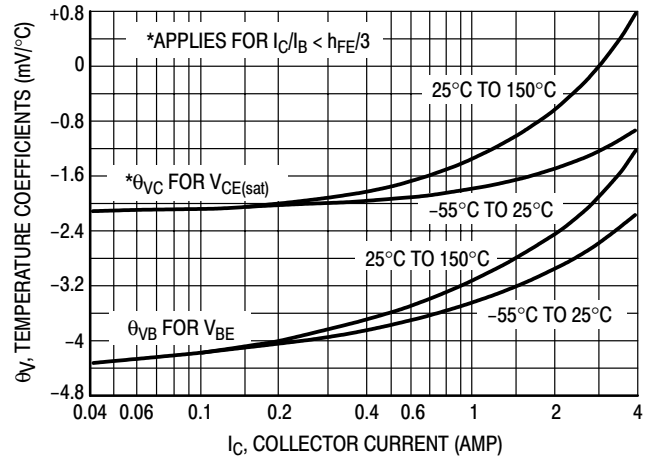


Figure 22. Temperature Coefficients

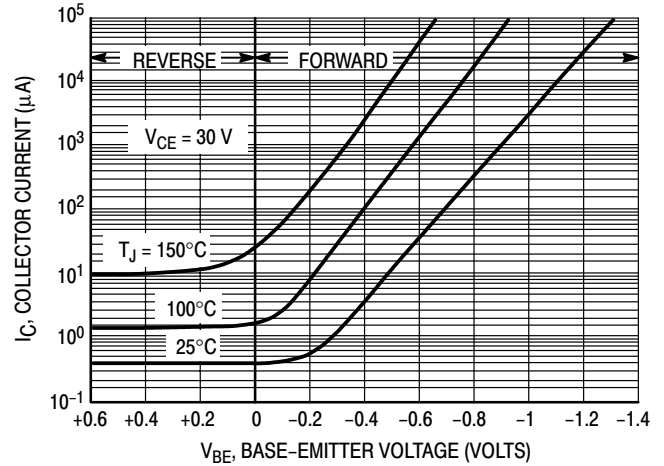
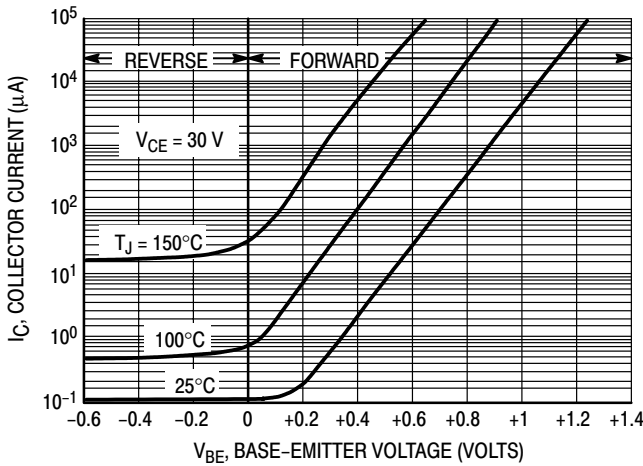


Figure 23. Collector Cut-Off Region

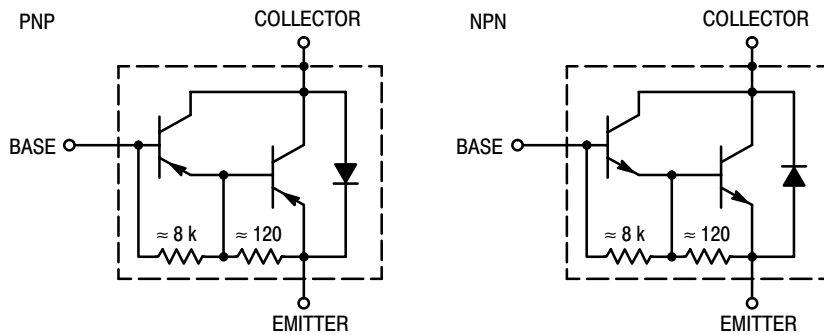


Figure 24. Darlington Schematic

# Complementary Darlington Power Transistors

## DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel (“T4” Suffix)
- Surface Mount Replacements for 2N6040–2N6045 Series, TIP120–TIP122 Series, and TIP125–TIP127 Series
- Monolithic Construction With Built-in Base-Emitter Shunt Resistors
- High DC Current Gain —  
 $h_{FE} = 2500$  (Typ) @  $I_C = 4.0$  Adc
- Complementary Pairs Simplifies Designs

### MAXIMUM RATINGS

Rating	Symbol	MJD122 MJD127	Unit
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5	Vdc
Collector Current — Continuous Peak	$I_C$	8 16	Adc
Base Current	$I_B$	120	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	Watts W/ $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	$^\circ\text{C}/\text{W}$

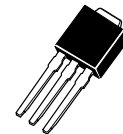
**NPN  
MJD122\***  
**PNP  
MJD127\***

\*ON Semiconductor Preferred Device

**SILICON  
POWER TRANSISTORS  
8 AMPERES  
100 VOLTS  
20 WATTS**

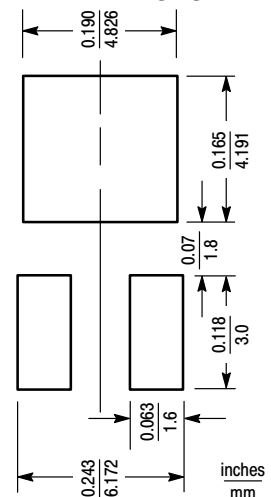


CASE 369A-13



CASE 369-07

### MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJD122 MJD127

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CE(sus)}$	100	—	Vdc
Collector Cutoff Current ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	10	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	2	mAdc

### ON CHARACTERISTICS

DC Current Gain ( $I_C = 4\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 8\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$h_{FE}$	1000 100	12,000 —	—
Collector–Emitter Saturation Voltage ( $I_C = 4\text{ Adc}$ , $I_B = 16\text{ mAdc}$ ) ( $I_C = 8\text{ Adc}$ , $I_B = 80\text{ mAdc}$ )	$V_{CE(sat)}$	— —	2 4	Vdc
Base–Emitter Saturation Voltage (1) ( $I_C = 8\text{ Adc}$ , $I_B = 80\text{ mAdc}$ )	$V_{BE(sat)}$	—	4.5	Vdc
Base–Emitter On Voltage ( $I_C = 4\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$V_{BE(on)}$	—	2.8	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain–Bandwidth Product ( $I_C = 3\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$ h_{fe} $	4	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	— —	300 200	pF
Small–Signal Current Gain ( $I_C = 3\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ , $f = 1\text{ kHz}$ )	$h_{fe}$	300	—	—

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

\*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

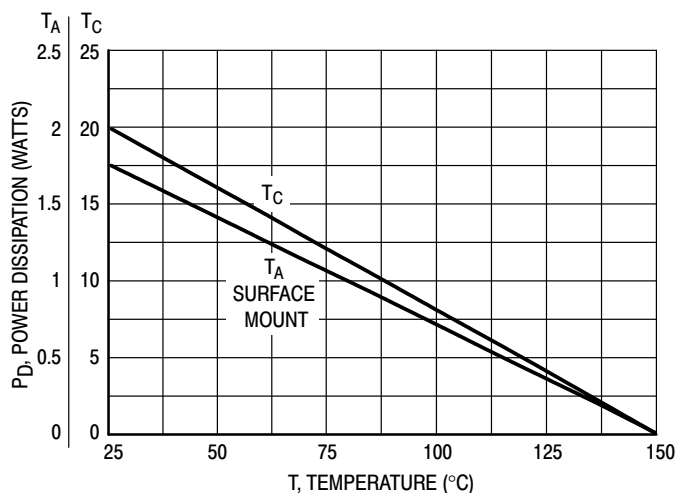


Figure 1. Power Derating

# MJD122 MJD127

## TYPICAL ELECTRICAL CHARACTERISTICS

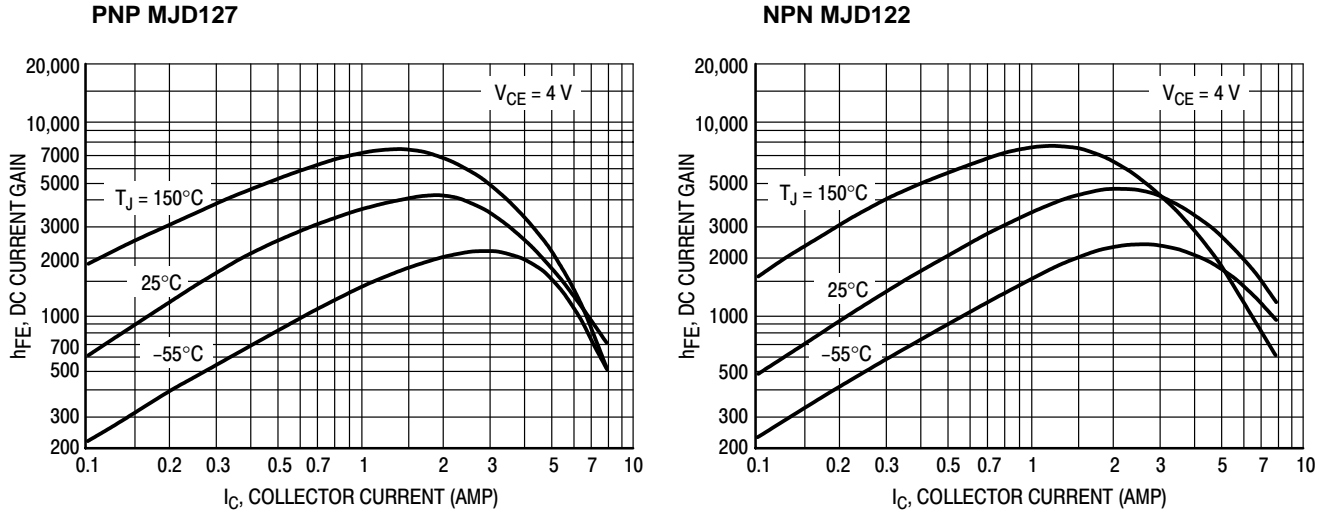


Figure 2. DC Current Gain

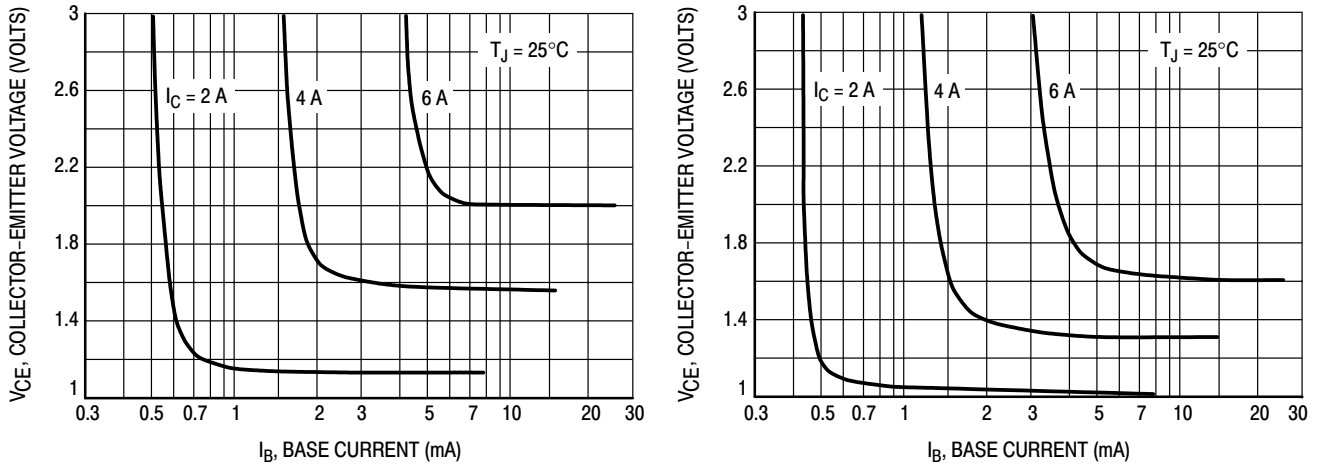


Figure 3. Collector Saturation Region

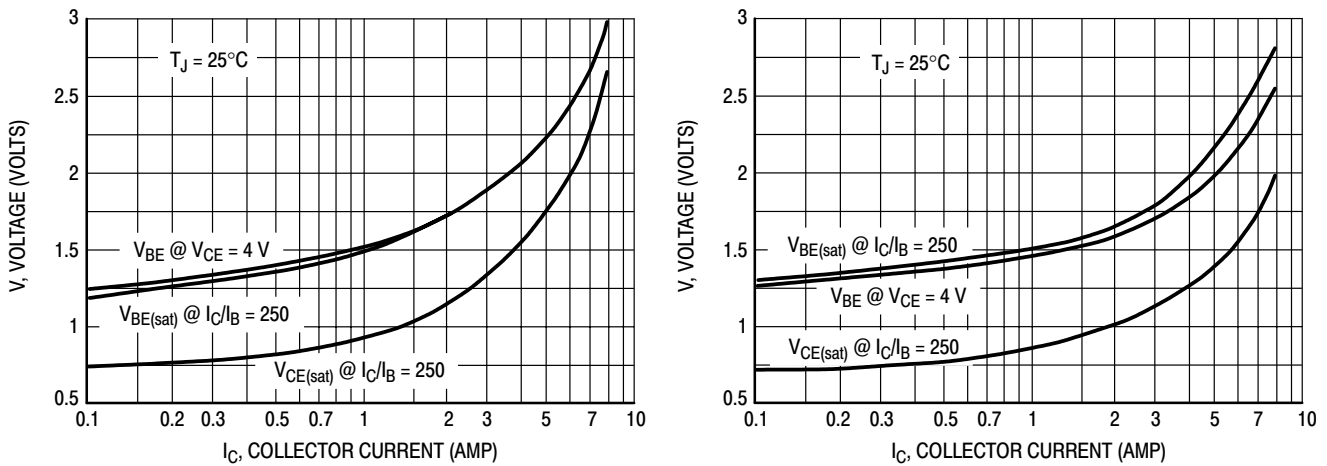


Figure 4. "On" Voltages

TYPICAL ELECTRICAL CHARACTERISTICS

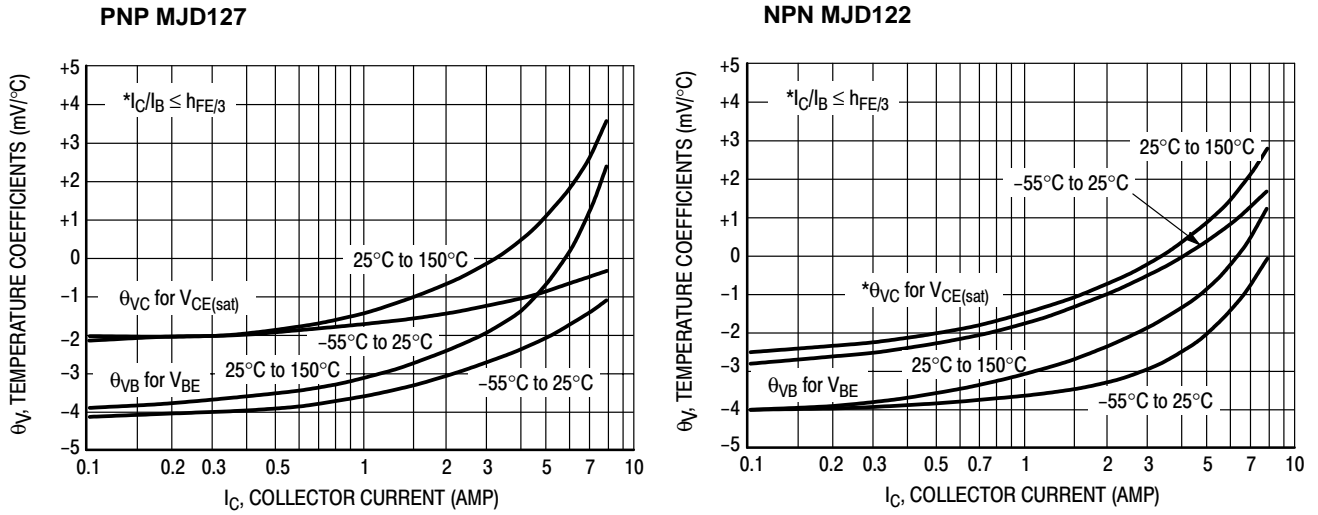


Figure 5. Temperature Coefficients

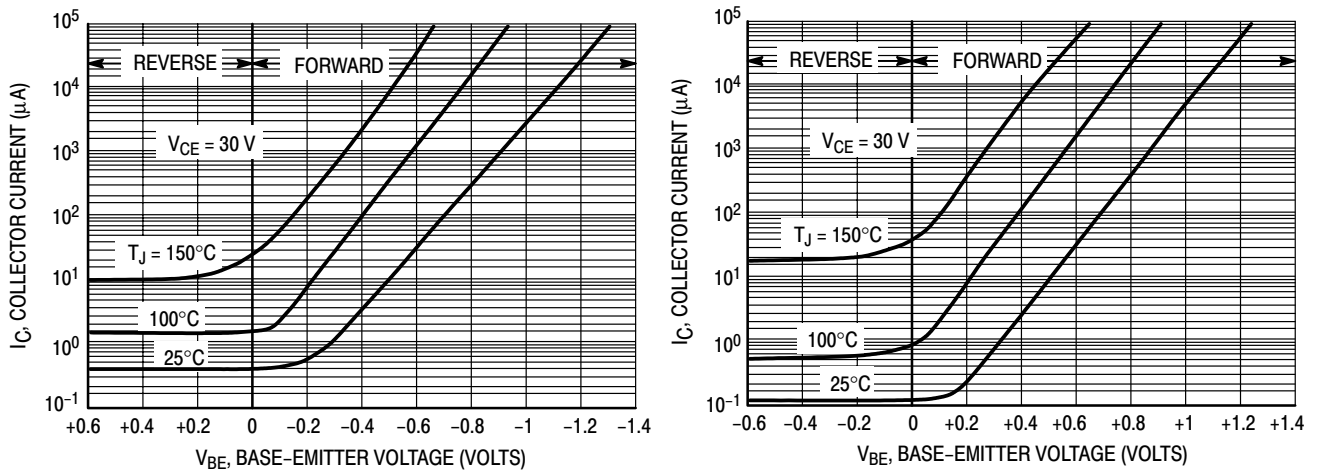


Figure 6. Collector Cut-Off Region

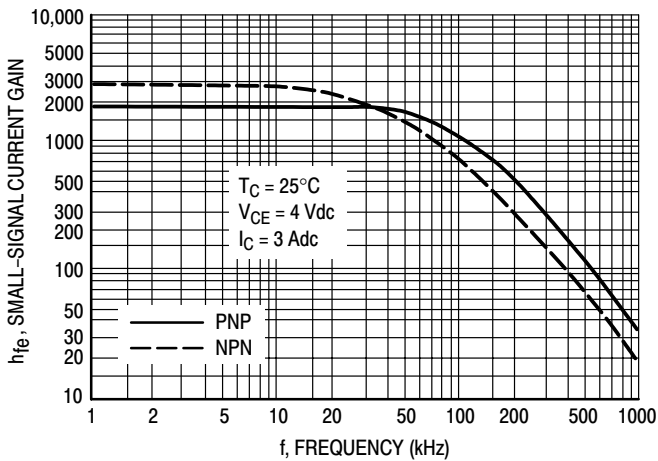


Figure 7. Small-Signal Current Gain

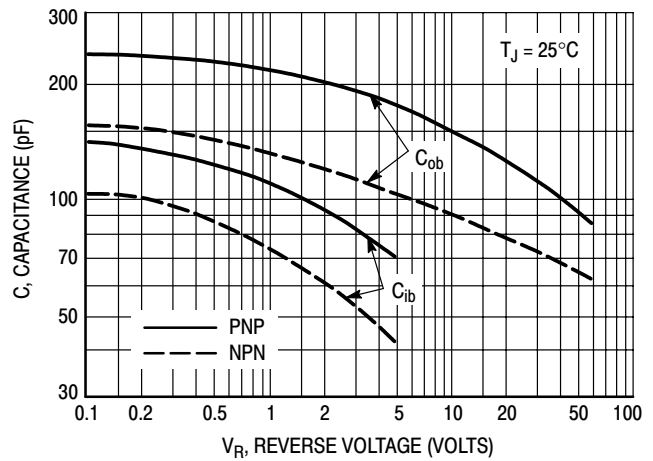


Figure 8. Capacitance

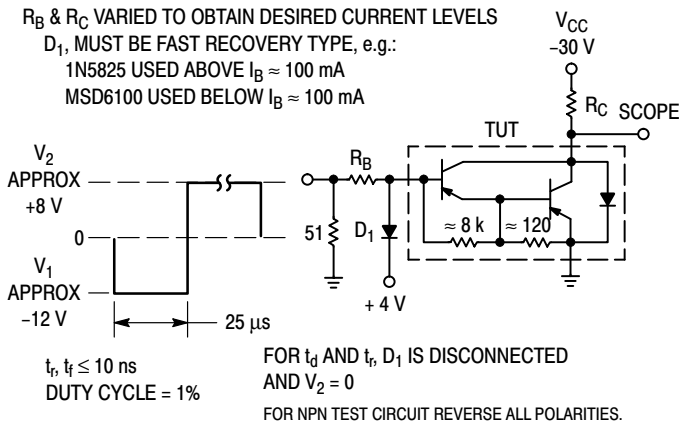


Figure 9. Switching Times Test Circuit

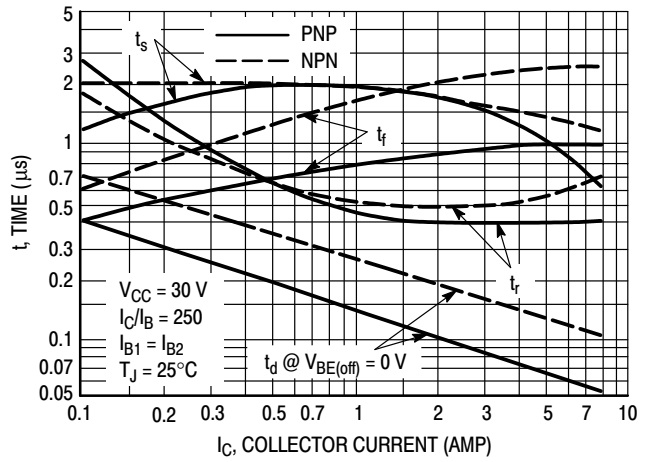


Figure 10. Switching Times

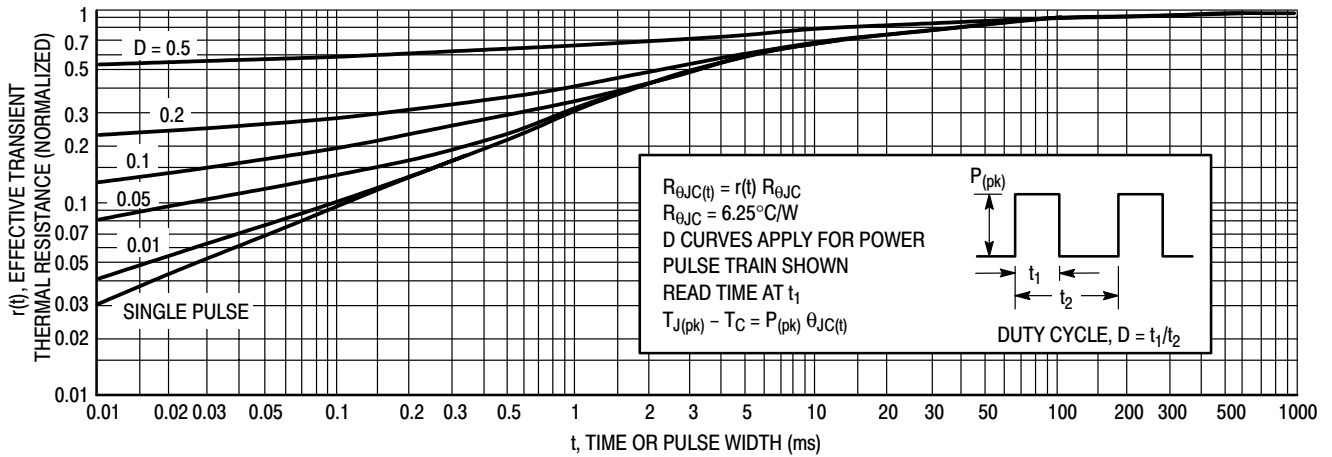


Figure 11. Thermal Response

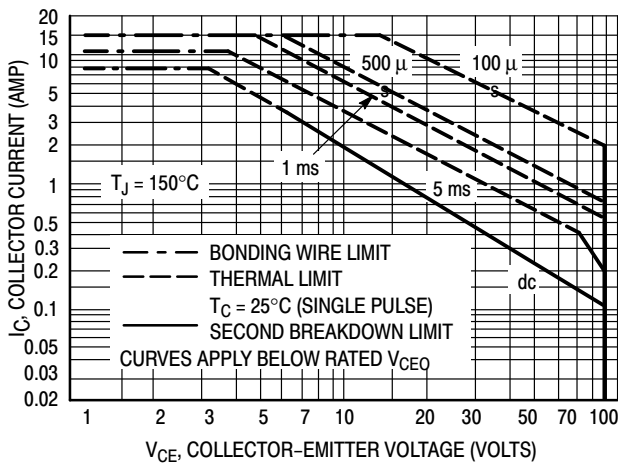


Figure 12. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# MJD122 MJD127

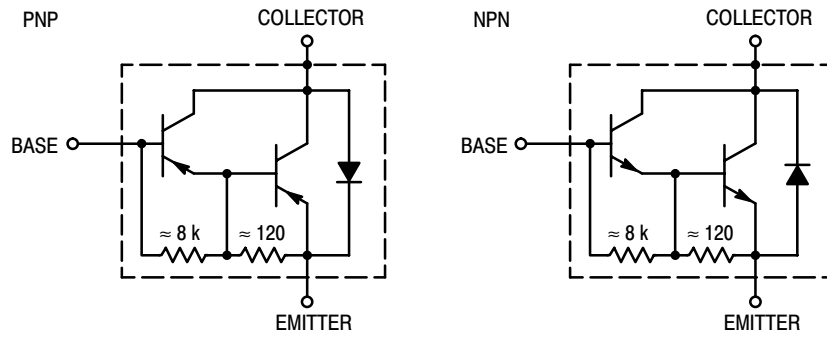


Figure 13. Darlington Schematic

# MJD18002D2

## Bipolar NPN Transistor

### High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector–Emitter Diode and Built–In Efficient Antisaturation Network

The MJD18002D2 is a state-of-the-art high speed, high gain bipolar transistor (H2BIP). Tight dynamic characteristics and lot to lot minimum spread ( $\pm 150$  ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no longer a need to guarantee an  $h_{FE}$  window.

#### Main Features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @  $I_C = 100$  mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic  $V_{CEsat}$
- Characteristics Make It Suitable for PFC Application
- “6 Sigma” Process Providing Tight and Reproducible Parameter Spreads

#### Two Versions:

- MJD18002D2–1: Case 369 for Insertion Mode
- MJD18002D2: Case 369A for Surface Mount Mode

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	$V_{CEO}$	450	Vdc
Collector–Base Breakdown Voltage	$V_{CBO}$	1000	Vdc
Collector–Emitter Breakdown Voltage	$V_{CES}$	1000	Vdc
Emitter–Base Voltage	$V_{EBO}$	11	Vdc
Collector Current – Continuous – Peak (Note 1.)	$I_C$ $I_{CM}$	2.0 5.0	Adc
Base Current – Continuous – Peak (Note 1.)	$I_B$ $I_{BM}$	1.0 2.0	Adc

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	50 0.4	W W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$
Thermal Resistance – Junction–to–Case	$R_{\theta JC}$	5.0	$^\circ\text{C}/\text{W}$
Thermal Resistance – Junction–to–Ambient	$R_{\theta JA}$	71.4	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 sec.	$T_L$	260	$^\circ\text{C}$

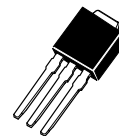
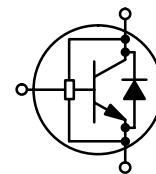
1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%



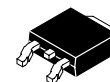
ON Semiconductor™

<http://onsemi.com>

**2 AMPERES  
1000 VOLTS  
50 WATTS  
POWER TRANSISTOR**

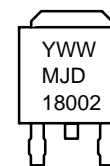
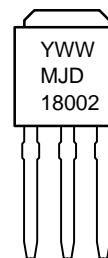


DPAK  
CASE 369  
STYLE 1



DPAK  
CASE 369A  
STYLE 1

#### MARKING DIAGRAMS



Y = Year  
WW = Work Week  
MJD18002  
= Device Code

#### ORDERING INFORMATION

Device	Package	Shipping
MJD18002D2–1	DPAK	75 Units/Rail
MJD18002D2T4	DPAK	3000/Tape & Reel



# MJD18002D2

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	450	570	–	Vdc
Collector–Base Breakdown Voltage ( $I_{CBO} = 1\text{ mA}$ )	$V_{CBO}$	1000	1100	–	Vdc
Emitter–Base Breakdown Voltage ( $I_{EBO} = 1\text{ mA}$ )	$V_{EBO}$	11	14	–	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$	–	–	100	$\mu\text{A}$ dc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )  ( $V_{CE} = 500\text{ V}$ , $V_{EB} = 0$ )	@ $T_C = 25^\circ\text{C}$	–	–	100	$\mu\text{A}$ dc
	@ $T_C = 125^\circ\text{C}$	–	–	500	
	@ $T_C = 125^\circ\text{C}$	–	–	100	
Emitter–Cutoff Current ( $V_{EB} = 10\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	–	500	$\mu\text{A}$ dc

### ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 0.4\text{ Adc}$ , $I_B = 40\text{ mA}$ dc) ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$	$V_{BE(sat)}$	–	0.78	1.0	Vdc
	@ $T_C = 125^\circ\text{C}$		–	0.87	1.1	
Collector–Emitter Saturation Voltage ( $I_C = 0.4\text{ Adc}$ , $I_B = 40\text{ mA}$ dc)  ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$	$V_{CE(sat)}$	–	0.36	0.6	Vdc
	@ $T_C = 125^\circ\text{C}$		–	0.50	1.0	
	@ $T_C = 25^\circ\text{C}$		–	0.40	0.75	
	@ $T_C = 125^\circ\text{C}$		–	0.65	1.2	
DC Current Gain ( $I_C = 0.4\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )  ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )	@ $T_C = 25^\circ\text{C}$	$h_{FE}$	14	25	–	–
	@ $T_C = 125^\circ\text{C}$		8.0	15	–	
	@ $T_C = 25^\circ\text{C}$		6.0	10	–	
	@ $T_C = 125^\circ\text{C}$		4.0	6.0	–	

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$f_t$	–	13	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1\text{ MHz}$ )	$C_{ob}$	–	50	100	pF
Input Capacitance ( $V_{EB} = 8\text{ Vdc}$ )	$C_{ib}$	–	340	500	pF

### DIODE CHARACTERISTICS

Forward Diode Voltage ( $I_{EC} = 1.0\text{ Adc}$ )  ( $I_{EC} = 0.4\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$	$V_{EC}$	–	1.2	1.5	Vdc
	@ $T_C = 25^\circ\text{C}$		–	1.0	1.3	
	@ $T_C = 125^\circ\text{C}$		–	0.6	–	
Forward Recovery Time ( $I_F = 0.4\text{ Adc}$ , $di/dt = 10\text{ A}/\mu\text{s}$ )  ( $I_F = 1.0\text{ Adc}$ , $di/dt = 10\text{ A}/\mu\text{s}$ )	@ $T_C = 25^\circ\text{C}$	$t_{fr}$	–	517	–	ns
	@ $T_C = 25^\circ\text{C}$		–	480	–	

# MJD18002D2

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage Determined 1 $\mu\text{s}$ and 3 $\mu\text{s}$ respectively after rising $I_{B1}$ reaches 90% of final $I_{B1}$	$I_C = 0.4 \text{ Adc}$ $I_{B1} = 40 \text{ mA}$ $V_{CC} = 300 \text{ Vdc}$	@ 1 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$	$V_{CE(dsat)}$	–	7.4	–	V
		@ 3 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$		–	2.5	–	
	$I_C = 1 \text{ Adc}$ $I_{B1} = 0.2 \text{ A}$ $V_{CC} = 300 \text{ Vdc}$	@ 1 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$		–	11.7	–	
		@ 3 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$		–	1.3	–	

### SWITCHING CHARACTERISTICS: Resistive Load (D.C.S. 10%, Pulse Width = 40 $\mu\text{s}$ )

Turn-on Time	$I_C = 0.4 \text{ Adc}$ , $I_{B1} = 40 \text{ mAdc}$ $I_{B2} = 200 \text{ mAdc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$	–	225	350	ns
Turn-off Time		@ $T_C = 125^\circ\text{C}$	$t_{off}$	0.8	–	1.1	$\mu\text{s}$
Turn-on Time	$I_C = 1.0 \text{ Adc}$ , $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	$t_{on}$	–	100	150	ns
Turn-off Time		@ $T_C = 125^\circ\text{C}$	$t_{off}$	0.95	–	1.25	$\mu\text{s}$

### SWITCHING CHARACTERISTICS: Inductive Load ( $V_{clamp} = 300 \text{ V}$ , $V_{CC} = 15 \text{ V}$ , $L = 200 \mu\text{H}$ )

Fall Time	$I_C = 0.4 \text{ Adc}$ $I_{B1} = 40 \text{ mAdc}$ $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_f$	–	130	175	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	$t_s$	0.4	–	0.7	$\mu\text{s}$
Cross-over Time		@ $T_C = 25^\circ\text{C}$	$t_c$	–	110	175	ns
		@ $T_C = 125^\circ\text{C}$		–	100	–	
Fall Time	$I_C = 0.8 \text{ Adc}$ $I_{B1} = 160 \text{ mAdc}$ $I_{B2} = 160 \text{ mAdc}$	@ $T_C = 25^\circ\text{C}$	$t_f$	–	130	175	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	$t_s$	2.1	–	2.4	$\mu\text{s}$
Cross-over Time		@ $T_C = 25^\circ\text{C}$	$t_c$	–	275	350	ns
		@ $T_C = 125^\circ\text{C}$		–	350	–	
Fall Time	$I_C = 1.0 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	$t_f$	–	100	150	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	$t_s$	–	1.05	1.2	$\mu\text{s}$
Cross-over Time		@ $T_C = 25^\circ\text{C}$	$t_c$	–	100	150	ns
		@ $T_C = 125^\circ\text{C}$		–	115	–	

Typical Static Characteristics

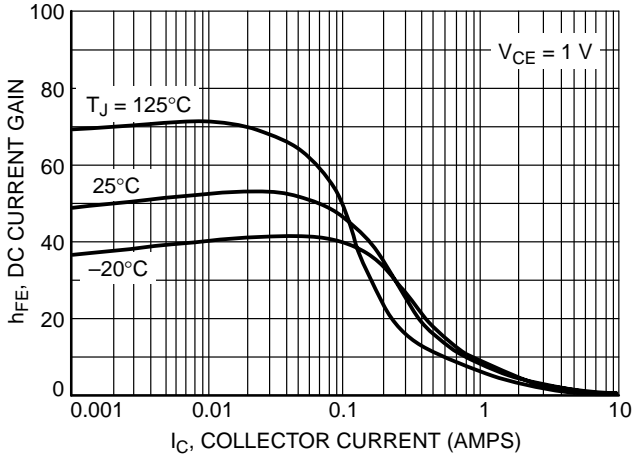


Figure 1. DC Current Gain @ 1 V

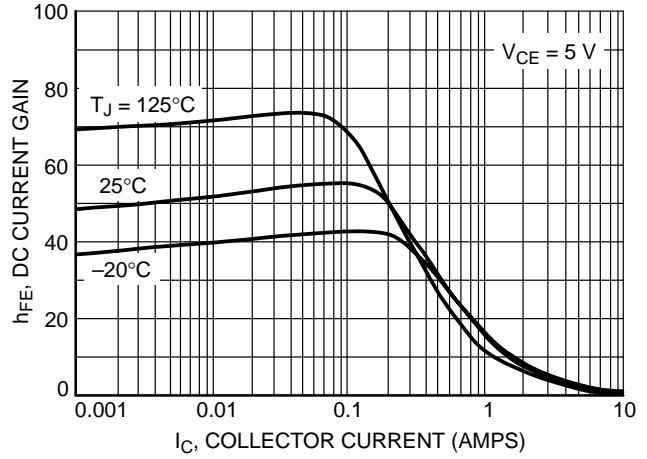


Figure 2. DC Current Gain @ 5 V

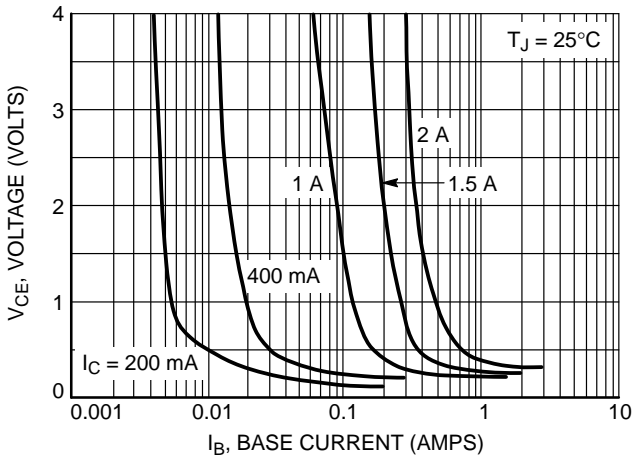


Figure 3. Collector Saturation Region

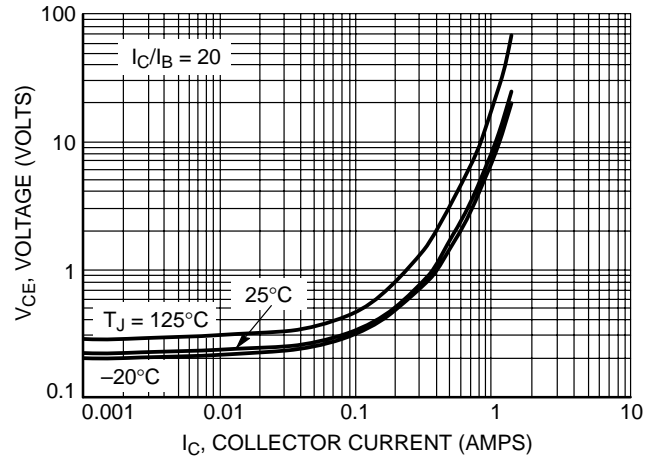


Figure 4. Collector-Emitter Saturation Voltage

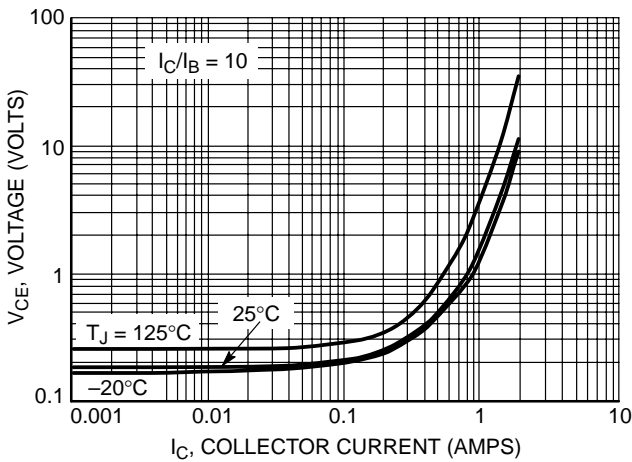


Figure 5. Collector-Emitter Saturation Voltage

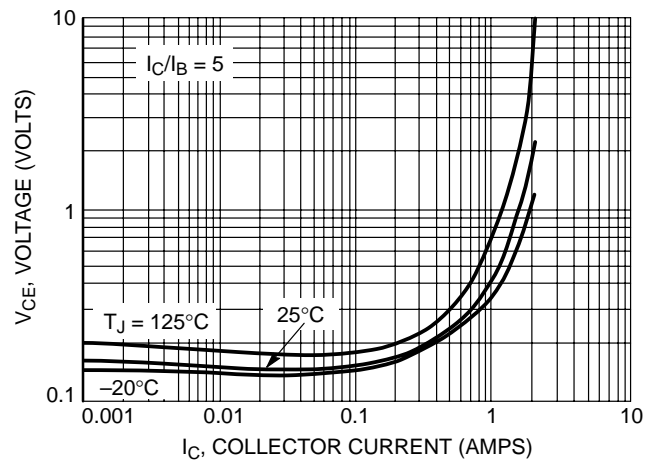


Figure 6. Collector-Emitter Saturation Voltage

Typical Static Characteristics

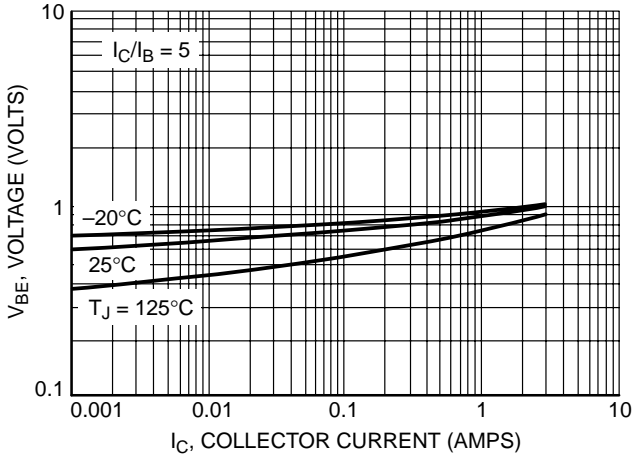


Figure 7. Base-Emitter Saturation Region  
 $I_C/I_B = 5$

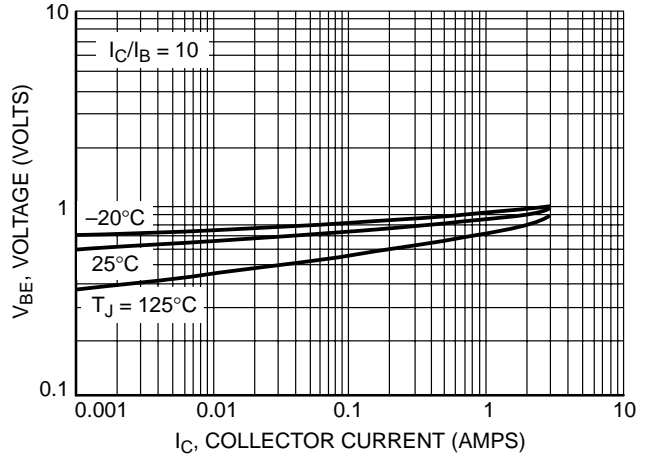


Figure 8. Base-Emitter Saturation Region  
 $I_C/I_B = 10$

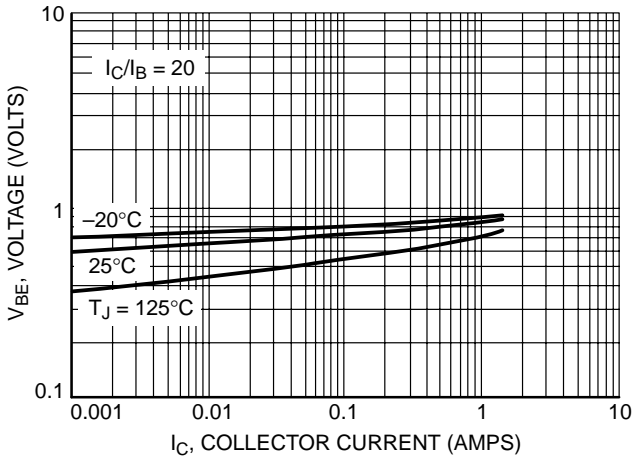


Figure 9. Base-Emitter Saturation Region  
 $I_C/I_B = 20$

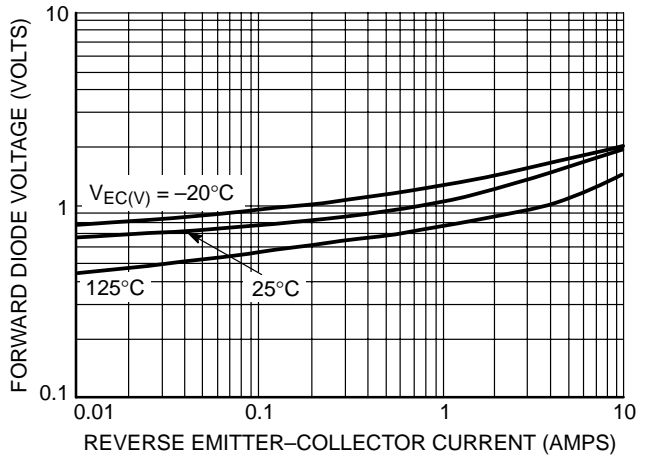


Figure 10. Forward Diode Voltage

Typical Switching Characteristics

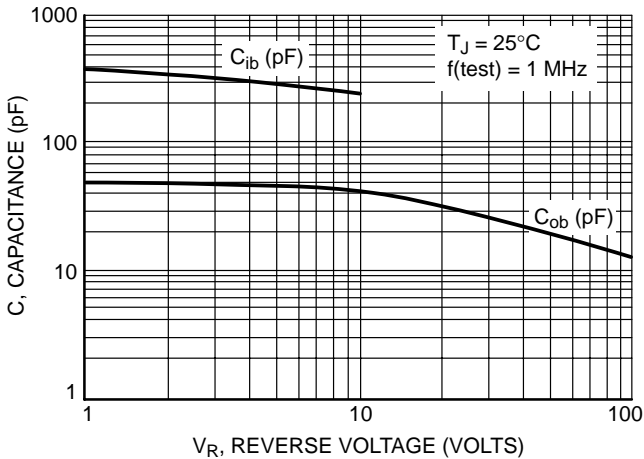


Figure 11. Capacitance

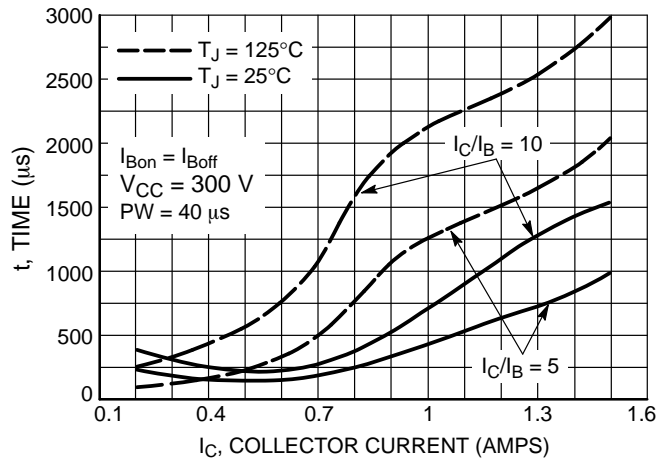


Figure 12. Resistive Switch Time,  $t_{on}$

Typical Switching Characteristics

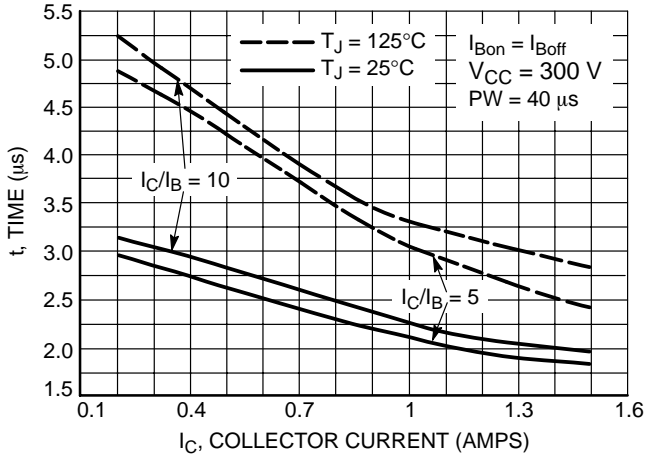


Figure 13. Resistive Switch Time,  $t_{off}$

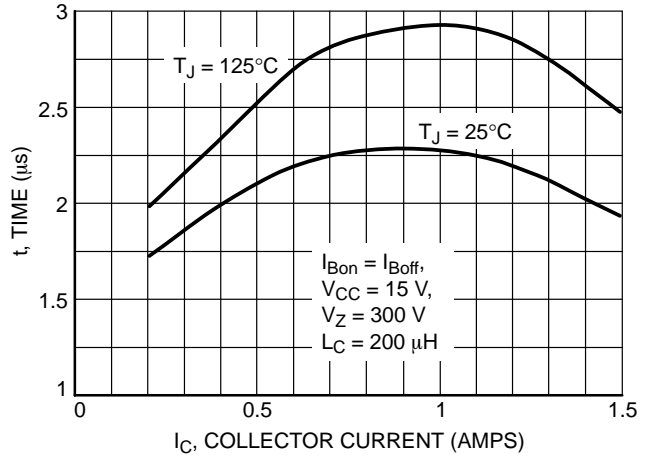


Figure 14. Inductive Storage Time,  $t_{si}$  @  $I_C/I_B = 5$

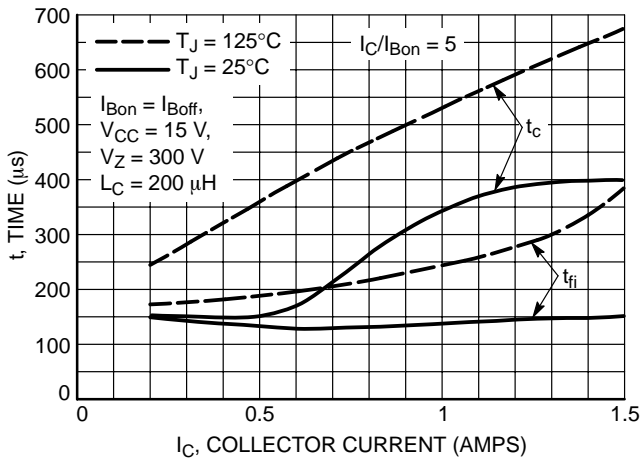


Figure 15. Inductive Switching,  $t_c$  &  $t_{fi}$  @  $I_C/I_B = 5$

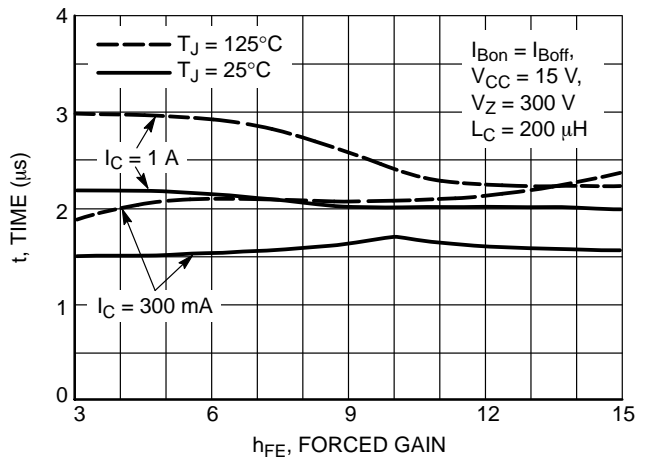


Figure 16. Inductive Storage Time

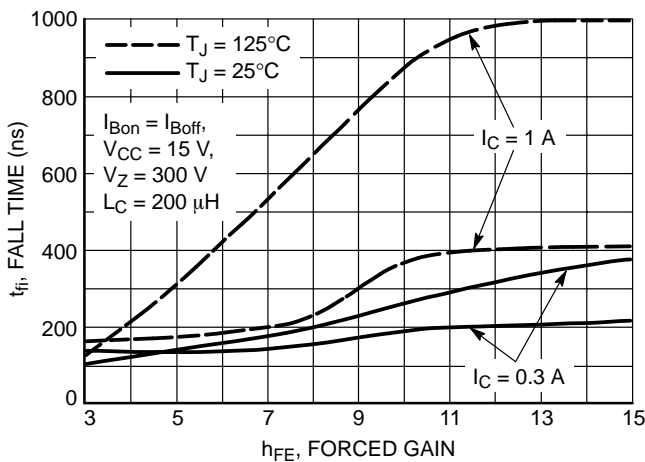


Figure 17. Inductive Fall Time

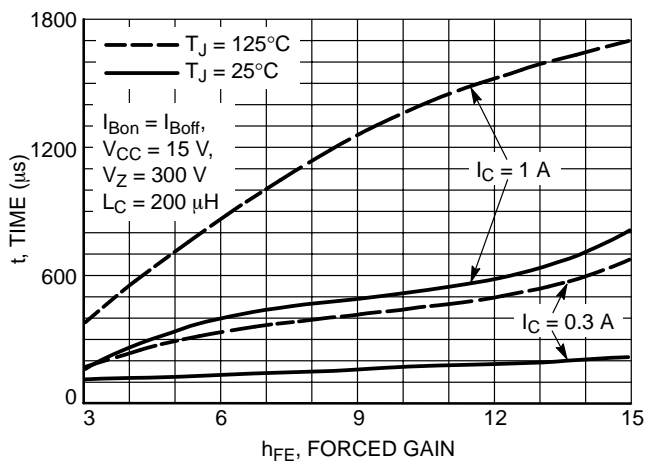


Figure 18. Inductive Cross-Over Time

Typical Switching Characteristics

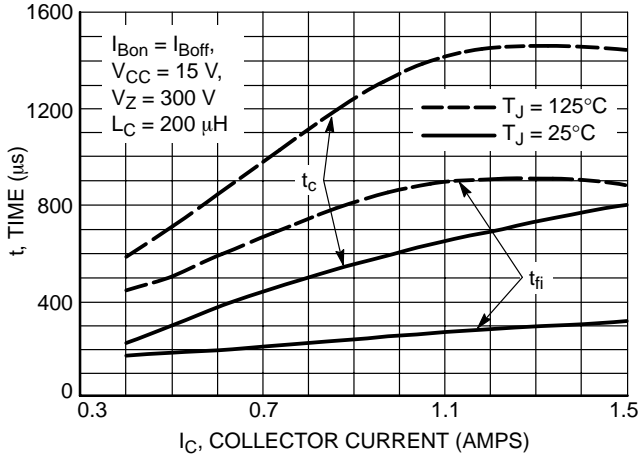


Figure 19. Inductive Switching Time,  $t_{fi}$  &  $T_C$  @  $G = 10$

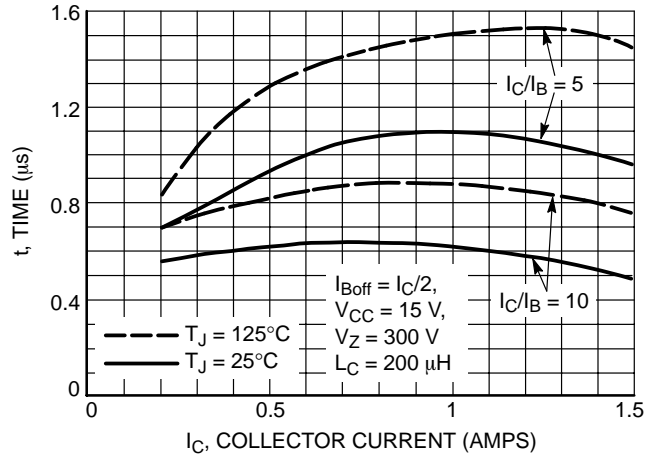


Figure 20. Inductive Switching Time,  $t_{si}$

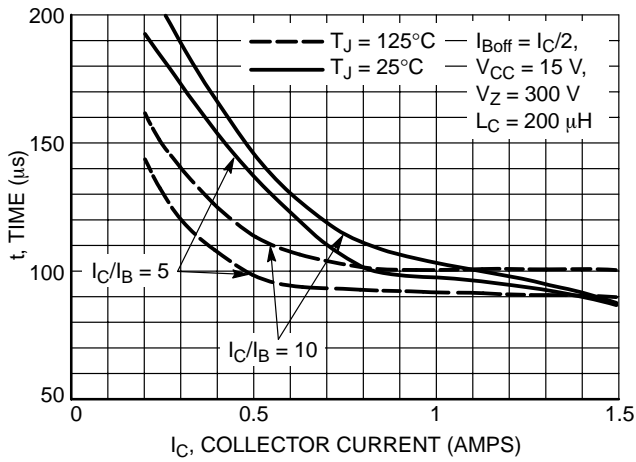


Figure 21. Inductive Storage Time,  $t_{fi}$

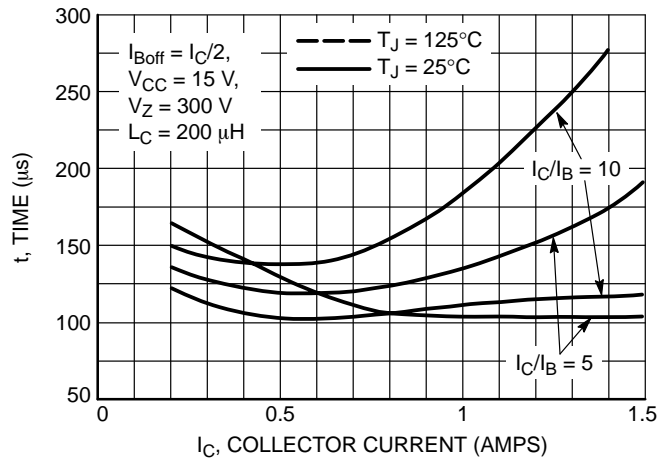


Figure 22. Inductive Storage Time,  $t_c$

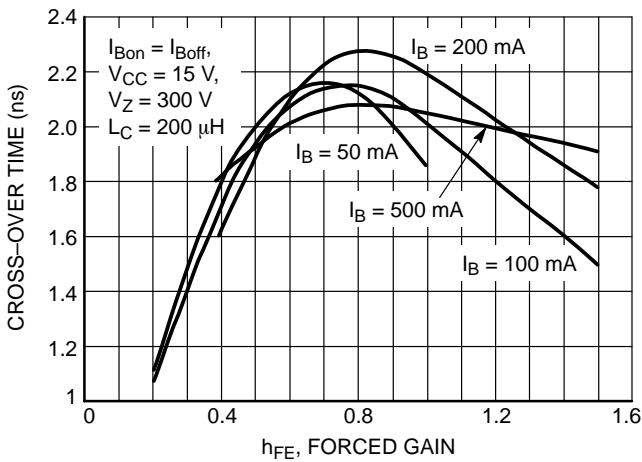


Figure 23. Inductive Storage Time,  $t_{si}$

Figure 24. Dynamic Saturation Voltage Measurements

# MJD18002D2

## Typical Switching Characteristics

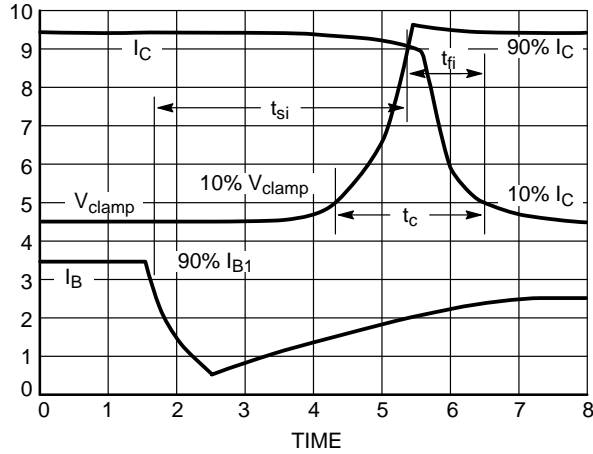
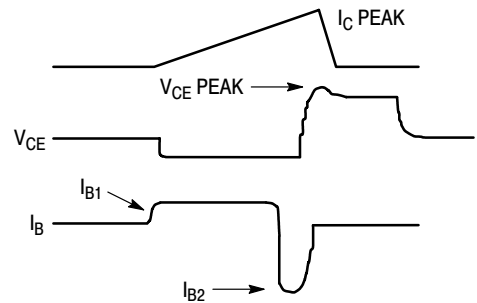
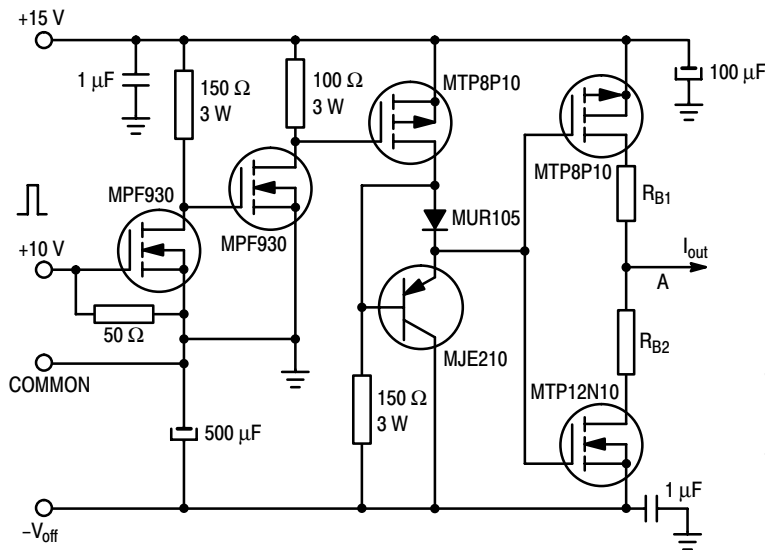


Figure 25. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit



**V<sub>(BR)CEO(sus)</sub>**  
 L = 10 mH  
 R<sub>B2</sub> = ∞  
 V<sub>CC</sub> = 20 Volts  
 I<sub>C(pk)</sub> = 100 mA

**Inductive Switching**  
 L = 200 μH  
 R<sub>B2</sub> = 0  
 V<sub>CC</sub> = 15 Volts  
 R<sub>B1</sub> selected for  
 desired I<sub>B1</sub>

**RBSOA**  
 L = 500 μH  
 R<sub>B2</sub> = 0  
 V<sub>CC</sub> = 15 Volts  
 R<sub>B1</sub> selected for  
 desired I<sub>B1</sub>

# MJD18002D2

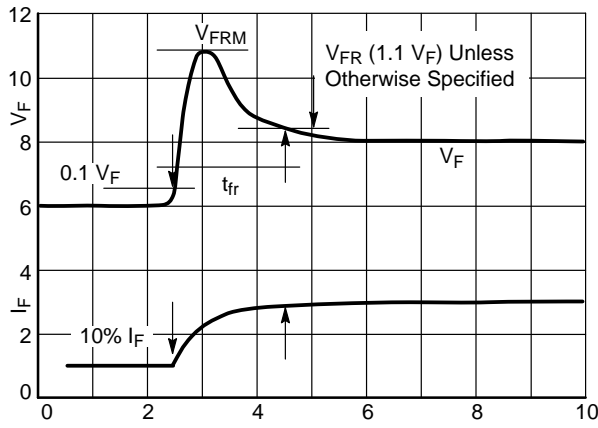


Figure 26.  $t_{fr}$  Measurement

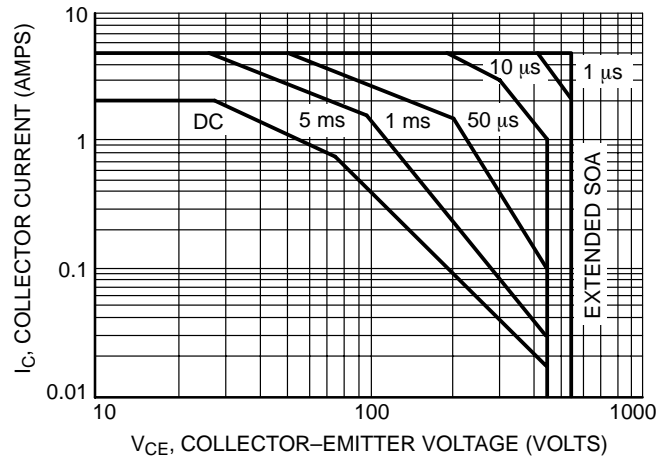


Figure 27. Forward Bias Safe Operating Area

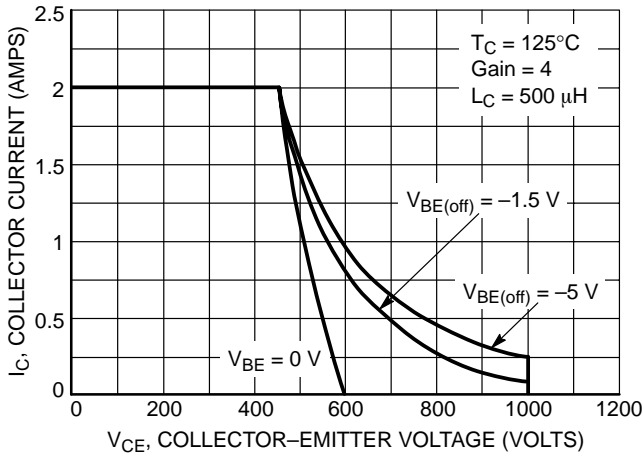


Figure 28. Reverse Bias Safe Operating Area

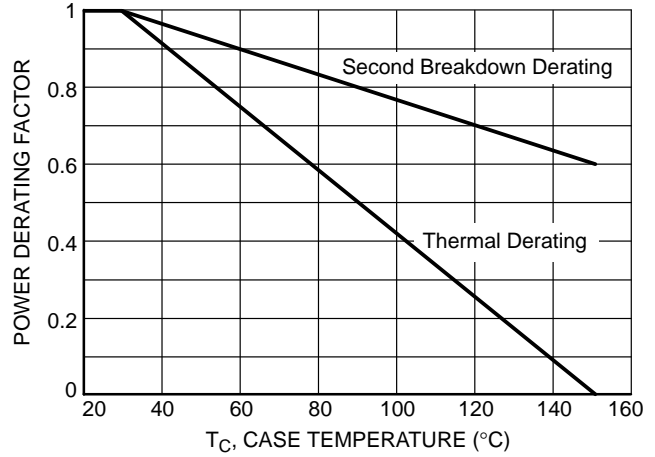


Figure 29. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 27 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second Breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on

Figure 27 may be found at any case temperature by using the appropriate curve on Figure 29.

$T_{J(pk)}$  may be calculated from the data in Figure 30. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 28). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.



# MJD18002D2

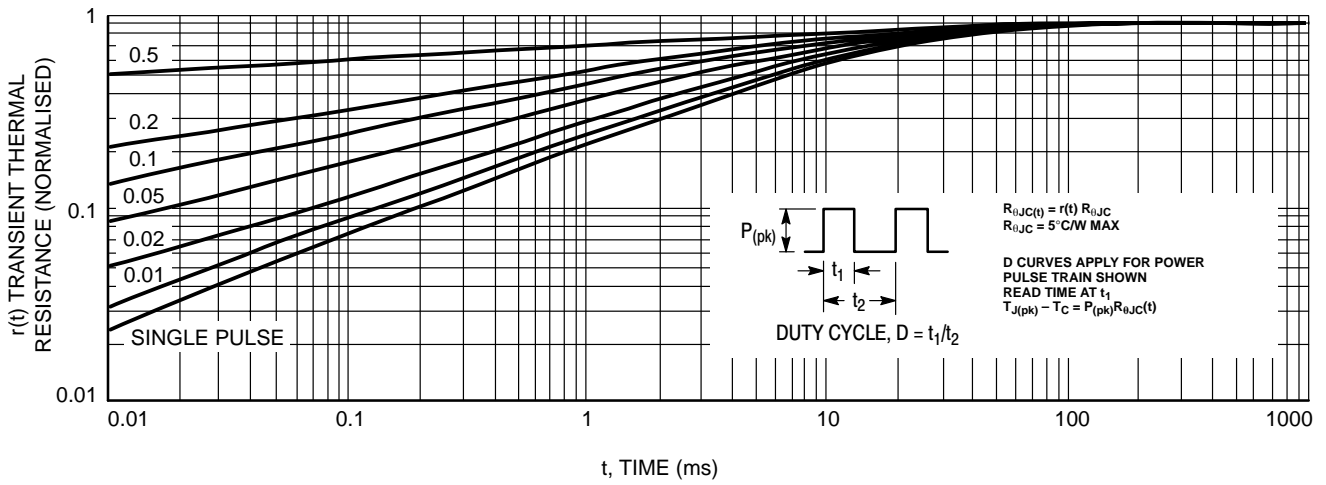


Figure 30. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for MJD18002D2

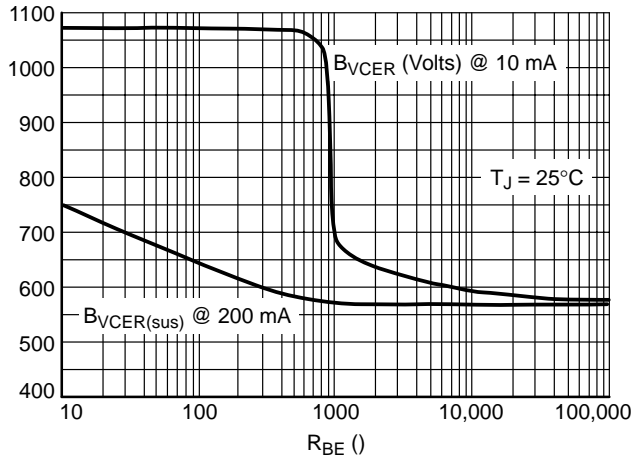


Figure 31.  $B_{VCER}$

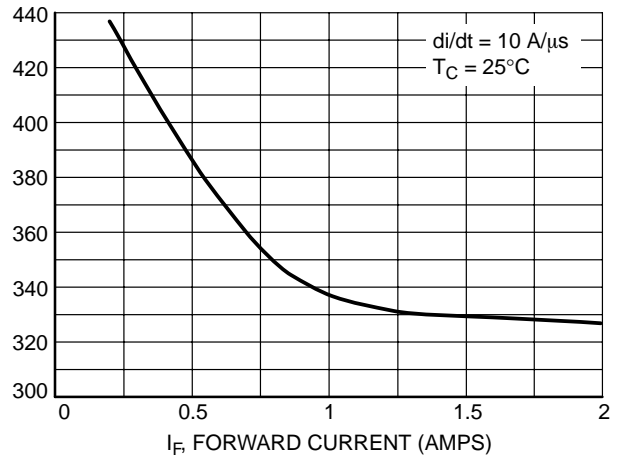
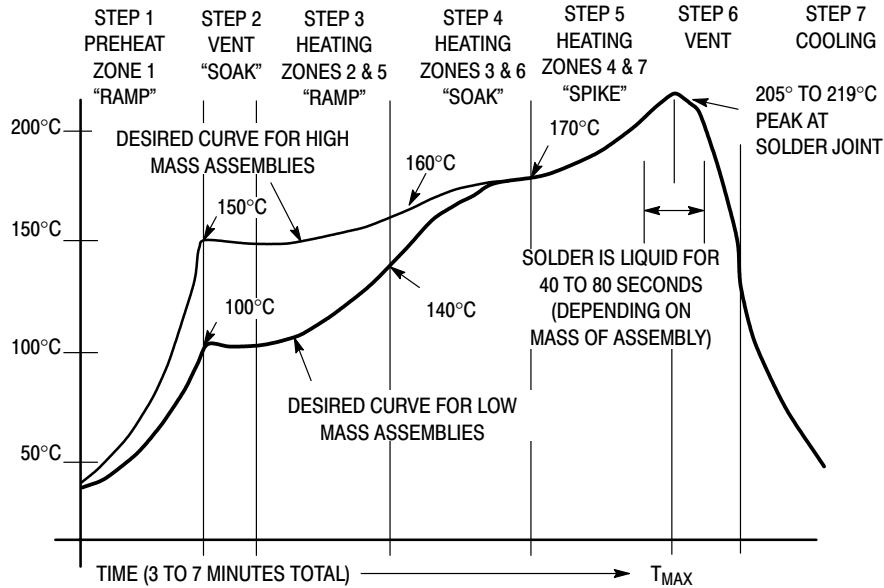


Figure 32. Forward Recovery Time,  $t_{fr}$

**TYPICAL SOLDER HEATING PROFILE**

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 33 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time.

The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.



**Figure 33. Typical Solder Heating Profile**

# Complementary Plastic Power Transistors

## NPN/PNP Silicon DPAK For Surface Mount Applications

... designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 25 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain —  
 $h_{FE} = 70 \text{ (Min) @ } I_C = 500 \text{ mAdc}$   
 $= 45 \text{ (Min) @ } I_C = 2 \text{ Adc}$   
 $= 10 \text{ (Min) @ } I_C = 5 \text{ Adc}$
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Low Collector-Emitter Saturation Voltage —  
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$   
 $= 0.75 \text{ Vdc (Max) @ } I_C = 2.0 \text{ Adc}$
- High Current-Gain — Bandwidth Product —  
 $f_T = 65 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakage —  
 $I_{CBO} = 100 \text{ nAdc @ Rated } V_{CB}$

### MAXIMUM RATINGS

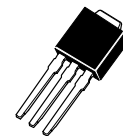
Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CB}$	40	Vdc
Collector-Emitter Voltage	$V_{CEO}$	25	Vdc
Emitter-Base Voltage	$V_{EB}$	8	Vdc
Collector Current — Continuous Peak	$I_C$	5 10	Adc
Base Current	$I_B$	1	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	12.5 0.1	Watts W/ $^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}^*$ Derate above $25^\circ\text{C}$	$P_D$	1.4 0.011	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

**NPN  
MJD200  
PNP  
MJD210**

**SILICON  
POWER TRANSISTORS  
5 AMPERES  
25 VOLTS  
12.5 WATTS**

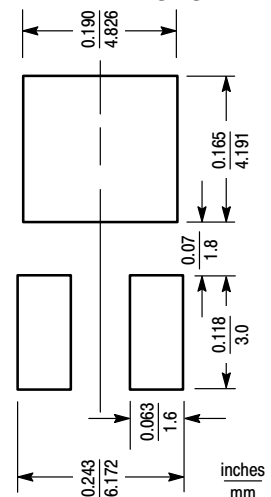


CASE 369A-13



CASE 369-07

### MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



# MJD200 MJD210

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	$^{\circ}C/W$
Junction to Ambient*	$R_{\theta JA}$	89.3	

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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## OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) ( $I_C = 10$ mAdc, $I_B = 0$ )	$V_{CE(sus)}$	25	—	Vdc
Collector Cutoff Current ( $V_{CB} = 40$ Vdc, $I_E = 0$ ) ( $V_{CB} = 40$ Vdc, $I_E = 0$ , $T_J = 125^{\circ}C$ )	$I_{CBO}$	— —	100 100	nAdc
Emitter Cutoff Current ( $V_{BE} = 8$ Vdc, $I_C = 0$ )	$I_{EBO}$	—	100	nAdc

## ON CHARACTERISTICS

DC Current Gain (2) ( $I_C = 500$ mAdc, $V_{CE} = 1$ Vdc) ( $I_C = 2$ Adc, $V_{CE} = 1$ Vdc) ( $I_C = 5$ Adc, $V_{CE} = 2$ Vdc)	$h_{FE}$	70 45 10	— 180 —	—
Collector–Emitter Saturation Voltage (2) ( $I_C = 500$ mAdc, $I_B = 50$ mAdc) ( $I_C = 2$ Adc, $I_B = 200$ mAdc) ( $I_C = 5$ Adc, $I_B = 1$ Adc)	$V_{CE(sat)}$	— — —	0.3 0.75 1.8	Vdc
Base–Emitter Saturation Voltage (1) ( $I_C = 5$ Adc, $I_B = 1$ Adc)	$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (1) ( $I_C = 2$ Adc, $V_{CE} = 1$ Vdc)	$V_{BE(on)}$	—	1.6	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product (3) ( $I_C = 100$ mAdc, $V_{CE} = 10$ Vdc, $f_{test} = 10$ MHz)	$f_T$	65	—	MHz
Output Capacitance ( $V_{CB} = 10$ Vdc, $I_E = 0$ , $f = 0.1$ MHz)	MJD200 MJD210 $C_{ob}$	— —	80 120	pF

\*When surface mounted on minimum pad sizes recommended.

(continued)

(1) Pulse Test: Pulse Width = 300  $\mu s$ , Duty Cycle  $\approx$  2%.

(2) Pulse Test: Pulse Width = 300  $\mu s$ , Duty Cycle  $\approx$  2%.

(3)  $f_T = |h_{fe}| \cdot f_{test}$ .

# MJD200 MJD210

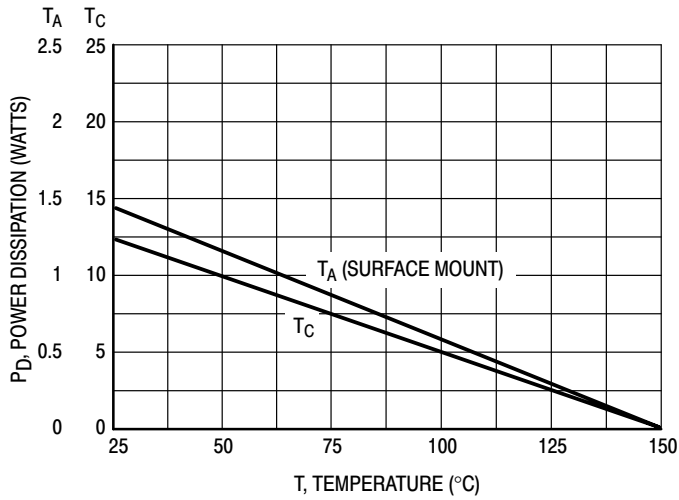


Figure 34. Power Derating

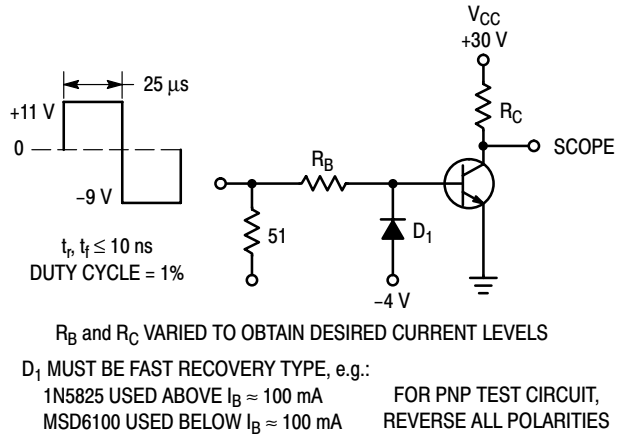


Figure 35. Switching Time Test Circuit

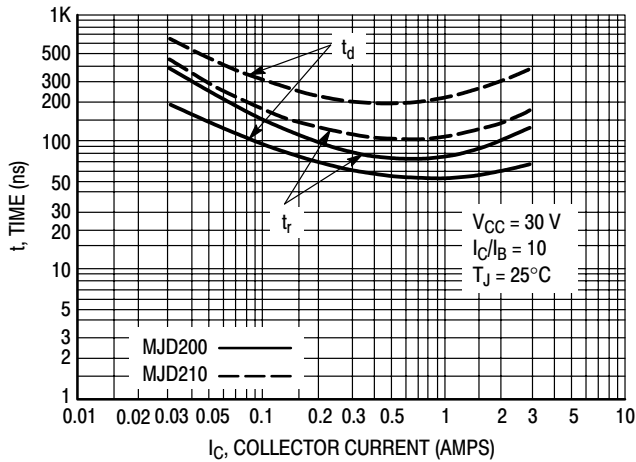


Figure 36. Turn-On Time

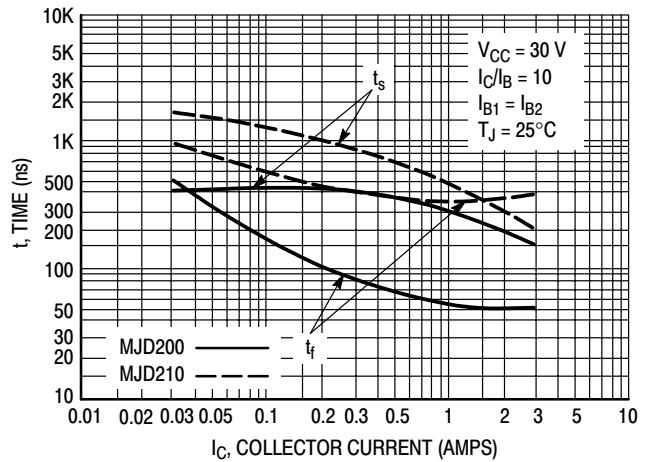
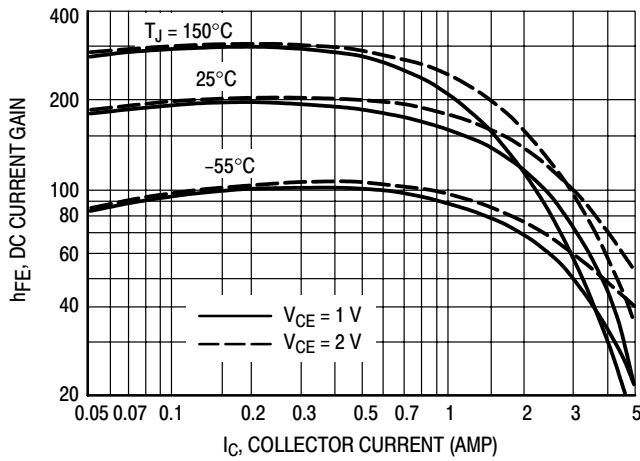


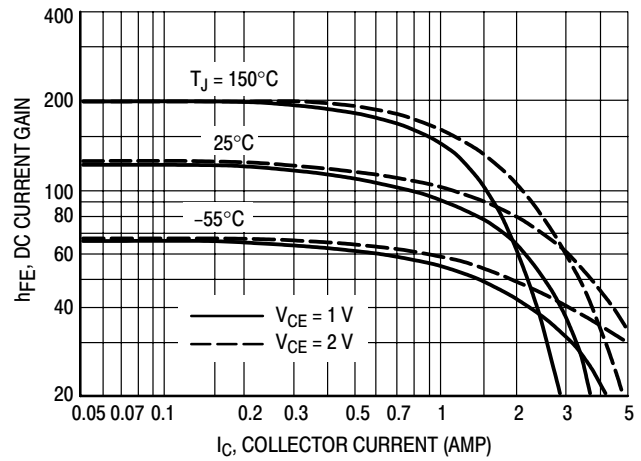
Figure 37. Turn-Off Time

# MJD200 MJD210

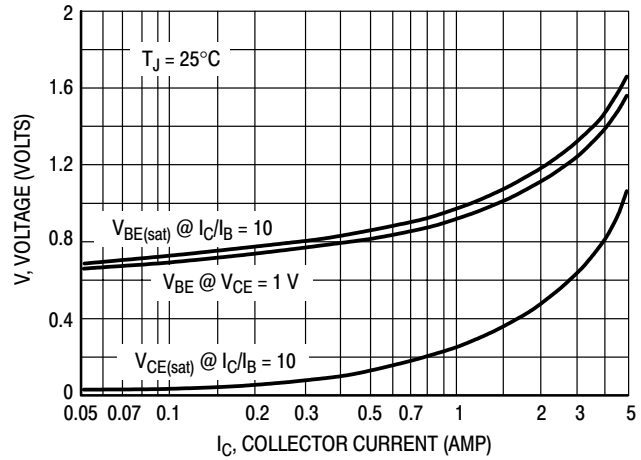
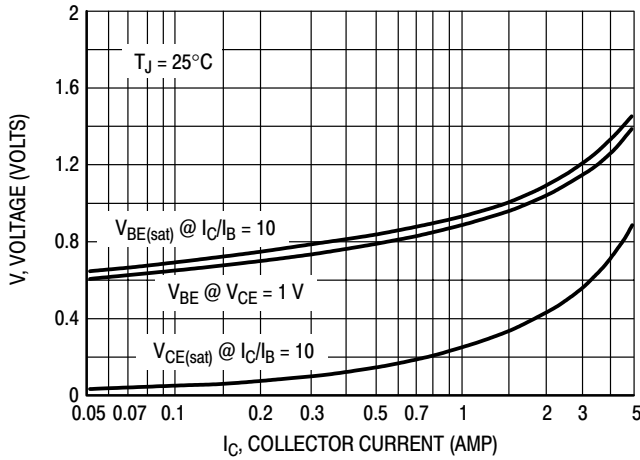
**NPN  
MJD200**



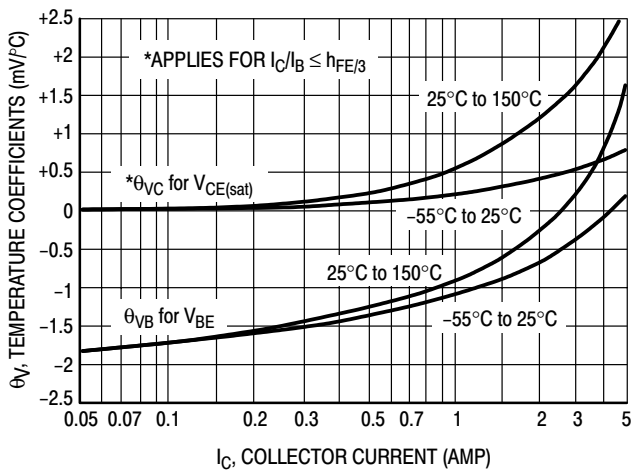
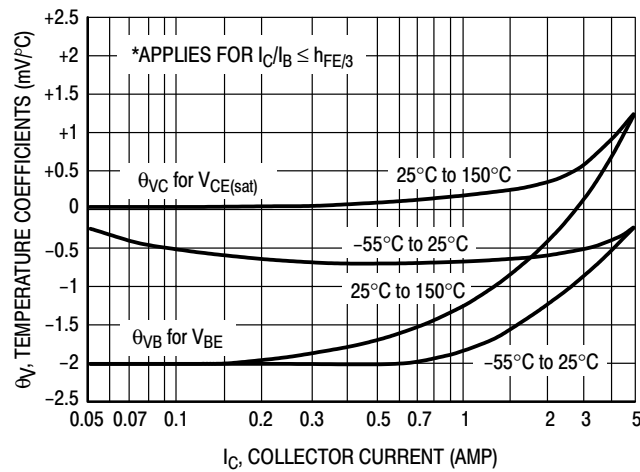
**PNP  
MJD210**



**Figure 38. DC Current Gain**



**Figure 39. "On" Voltage**



**Figure 40. Temperature Coefficients**

# MJD200 MJD210

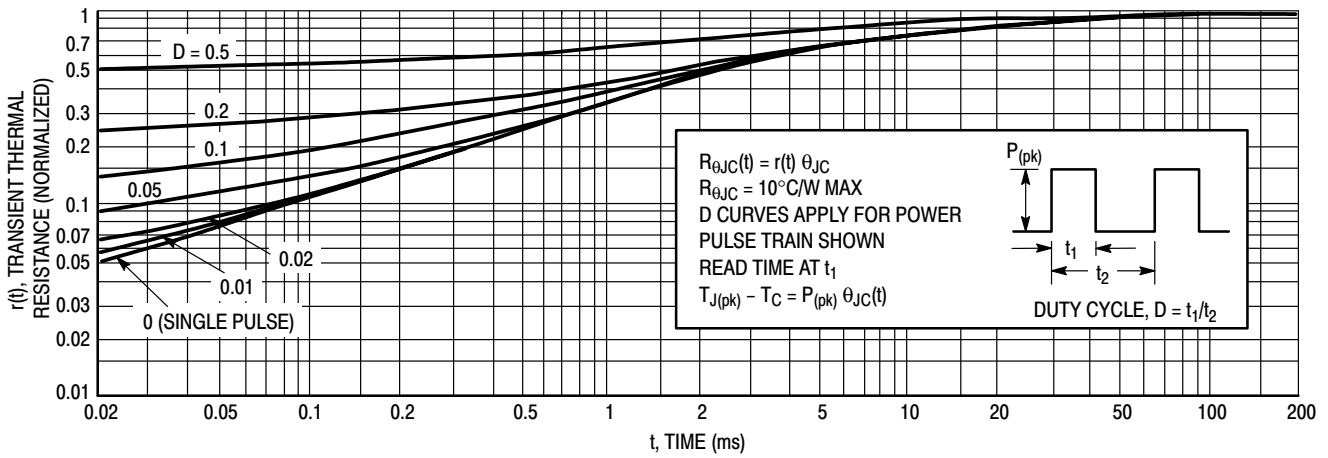


Figure 41. Thermal Response

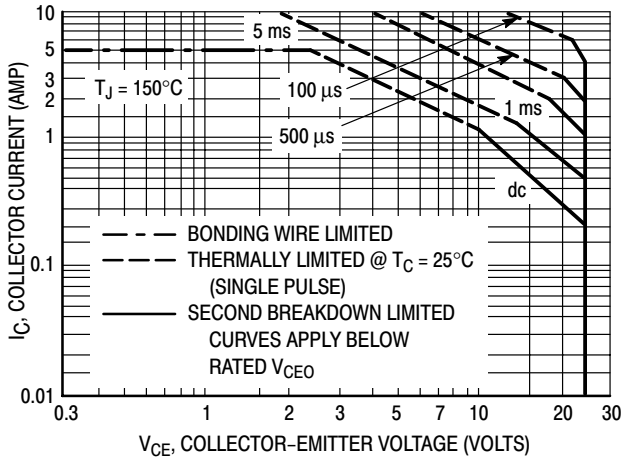


Figure 42. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 42 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Case 369 may be ordered by adding a “-1” suffix to the device title (i.e. MJD200-1)

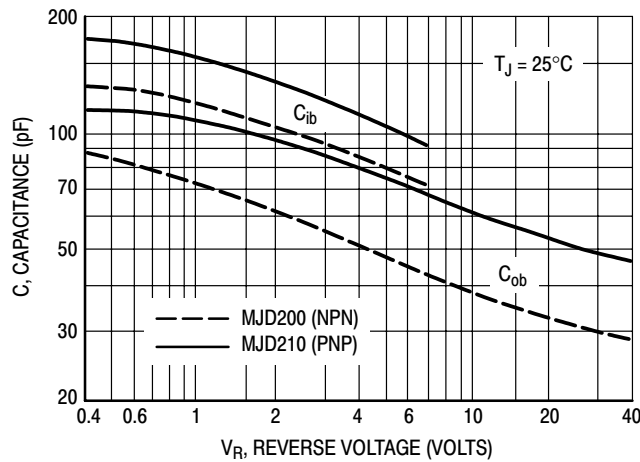


Figure 43. Capacitance

# MJD243 (NPN), MJD253 (PNP)

MJD243 is a Preferred Device

## Complementary Silicon Plastic Power Transistor

### DPAK for Surface Mount Applications

... designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage –  
 $V_{CEO(sus)} = 100 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain –  
 $h_{FE} = 40 \text{ (Min) @ } I_C = 200 \text{ mAdc}$   
 $= 15 \text{ (Min) @ } I_C = 1.0 \text{ Adc}$
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Low Collector-Emitter Saturation Voltage –  
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$   
 $= 0.6 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Adc}$
- High Current-Gain – Bandwidth Product –  
 $f_T = 40 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakage –  
 $I_{CBO} = 100 \text{ nAdc @ Rated } V_{CB}$

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CB}$	100	Vdc
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	7	Vdc
Collector Current – Continuous – Peak	$I_C$	4 8	Adc
Base Current	$I_B$	1	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	12.5 0.1	Watts $\text{W}/^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1.) Derate above $25^\circ\text{C}$	$P_D$	1.4 0.011	Watts $\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

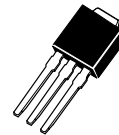
1. When surface mounted on minimum pad sizes recommended.



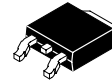
ON Semiconductor™

<http://onsemi.com>

**4 AMPERES  
100 VOLTS  
12.5 WATTS  
POWER TRANSISTOR**

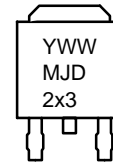
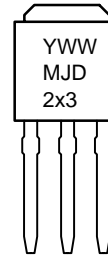


DPAK  
CASE 369  
STYLE 1



DPAK  
CASE 369A  
STYLE 1

#### MARKING DIAGRAMS



Y = Year  
 WW = Work Week  
 MJD2x3 = Device Code  
 x = 4 or 5

#### ORDERING INFORMATION

Device	Package	Shipping
MJD243-1	DPAK	75 Units/Rail
MJD253T4	DPAK	3000/Tape & Reel
MJD253-1	DPAK	75 Units/Rail
MJD253T4	DPAK	3000/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.



## MJD243 (NPN), MJD253 (PNP)

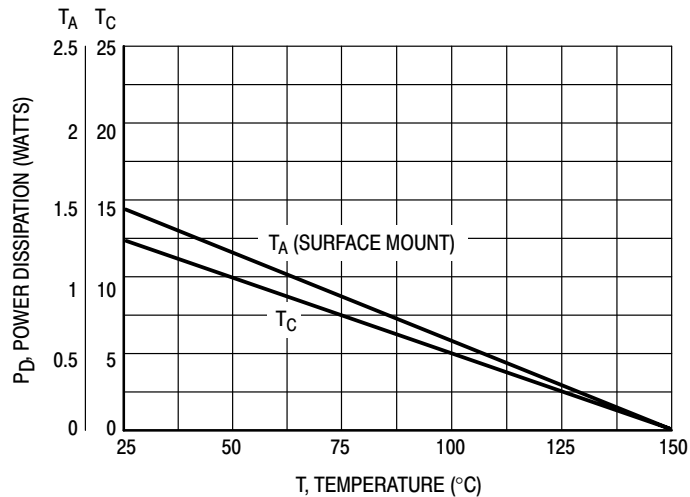


Figure 1. Power Derating

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Junction to Ambient (Note 2.)	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

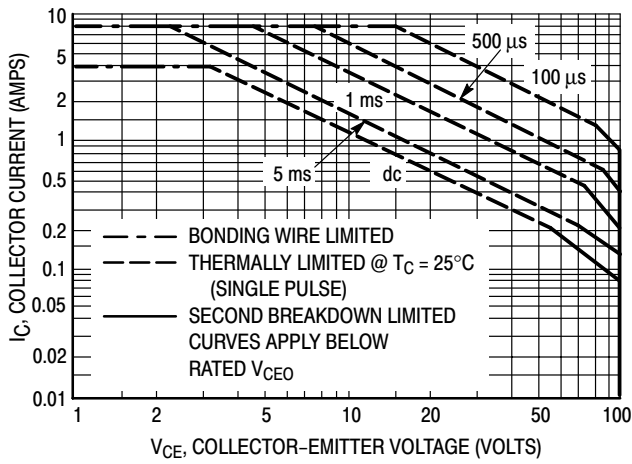
Collector–Emitter Sustaining Voltage (Note 3.) ( $I_C = 10\text{ mA}_{dc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ , $T_J = 125^\circ\text{C}$ )	$I_{CBO}$	–	100 100	nAdc $\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 7\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	100	nAdc
DC Current Gain (Note 3.) ( $I_C = 200\text{ mA}_{dc}$ , $V_{CE} = 1\text{ Vdc}$ ) ( $I_C = 1\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )	$h_{FE}$	40 15	180 –	–
Collector–Emitter Saturation Voltage (Note 3.) ( $I_C = 500\text{ mA}_{dc}$ , $I_B = 50\text{ mA}_{dc}$ ) ( $I_C = 1\text{ Adc}$ , $I_B = 100\text{ mA}_{dc}$ )	$V_{CE(sat)}$	– –	0.3 0.6	Vdc
Base–Emitter Saturation Voltage (Note 3.) ( $I_C = 2\text{ Adc}$ , $I_B = 200\text{ mA}_{dc}$ )	$V_{BE(sat)}$	–	1.8	Vdc
Base–Emitter On Voltage (Note 3.) ( $I_C = 500\text{ mA}_{dc}$ , $V_{CE} = 1\text{ Vdc}$ )	$V_{BE(on)}$	–	1.5	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product (Note 4.) ( $I_C = 100\text{ mA}_{dc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 10\text{ MHz}$ )	$f_T$	40	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	–	50	pF

- When surface mounted on minimum pad sizes recommended.
- Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\approx 2\%$ .
- $f_T = |h_{FE}| \cdot f_{test}$ .

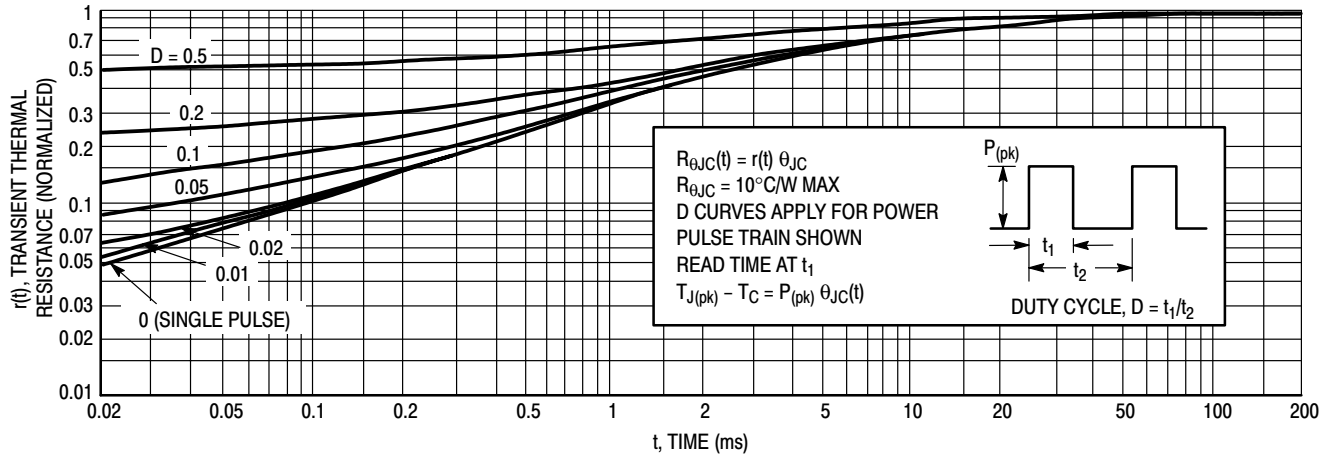
## MJD243 (NPN), MJD253 (PNP)



**Figure 2. Active Region Maximum Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

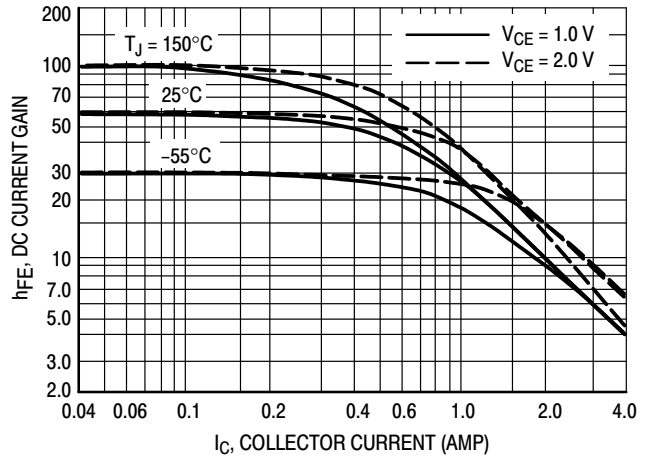
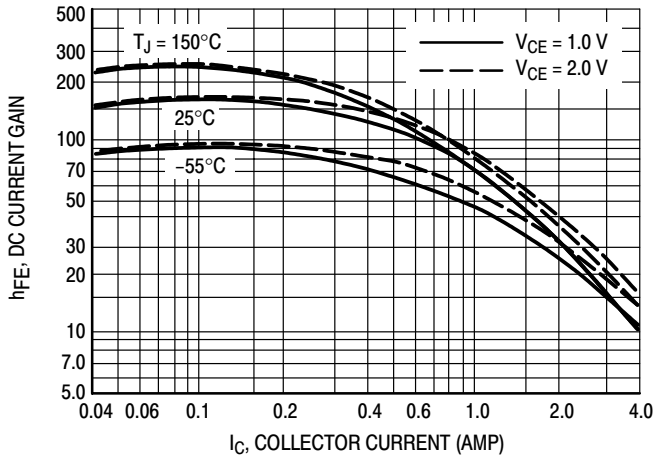


**Figure 3. Thermal Response**

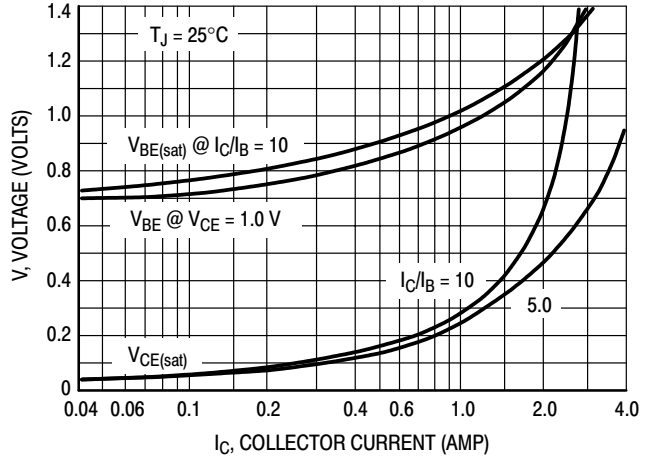
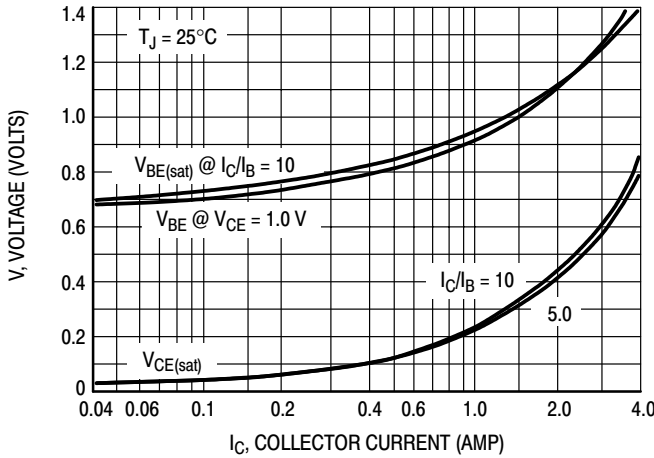
# MJD243 (NPN), MJD253 (PNP)

**NPN  
MJD243**

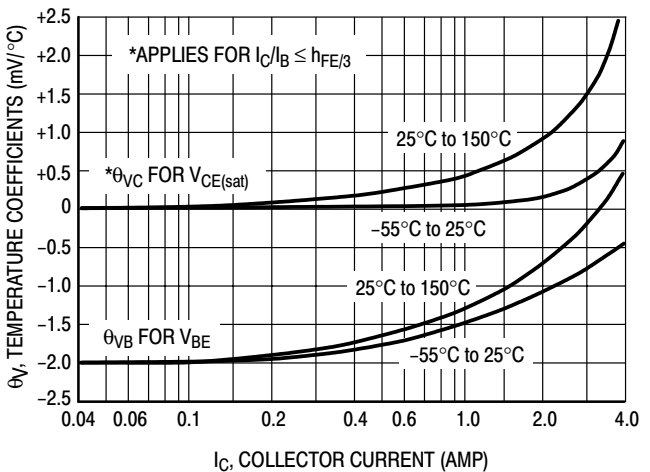
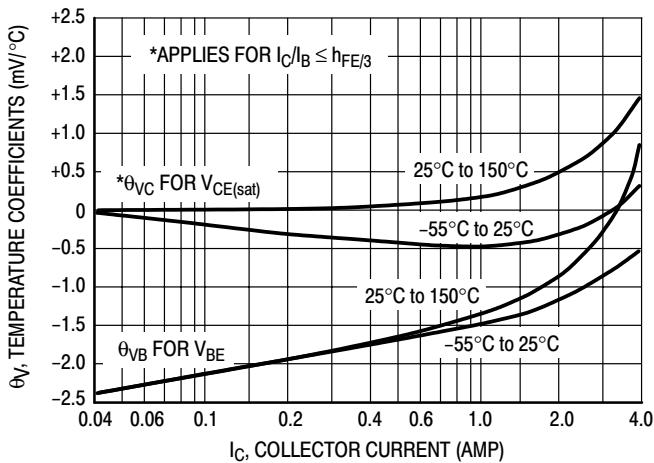
**PNP  
MJD253**



**Figure 4. DC Current Gain**



**Figure 5. "On" Voltages**



**Figure 6. Temperature Coefficients**

# MJD243 (NPN), MJD253 (PNP)

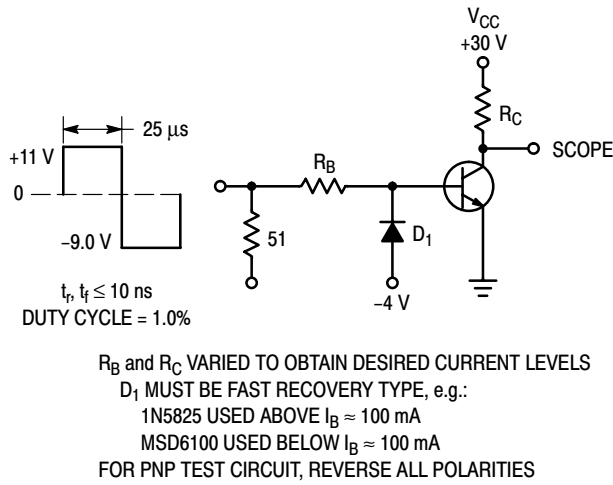


Figure 7. Switching Time Test Circuit

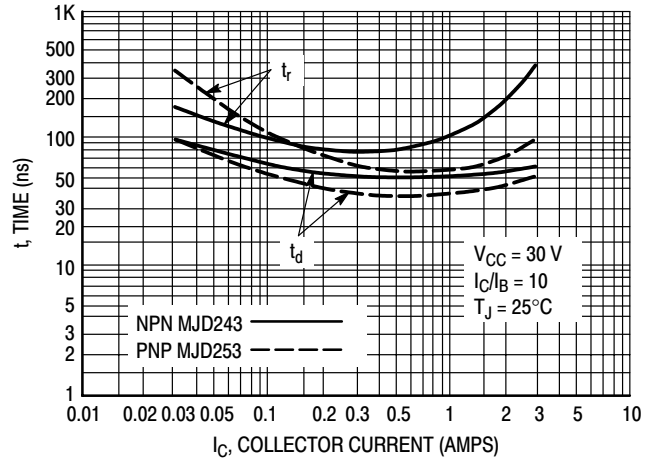


Figure 8. Turn-On Time

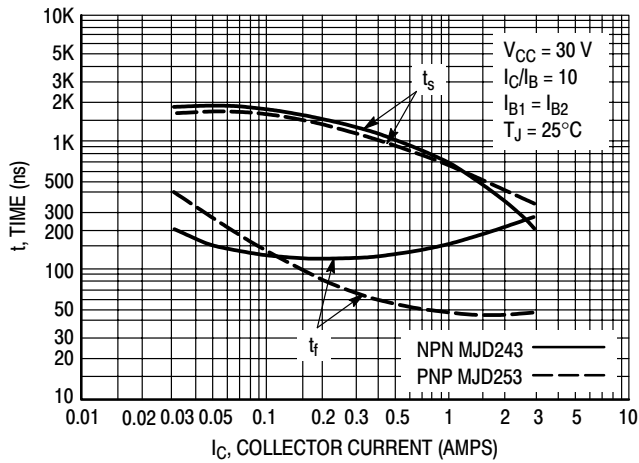


Figure 9. Turn-Off Time

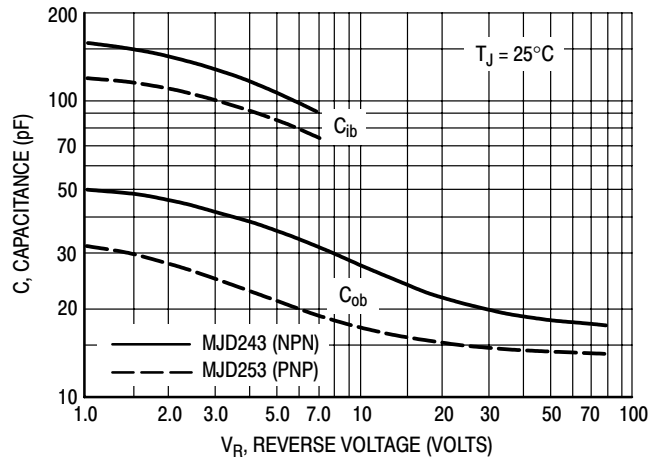


Figure 10. Capacitance

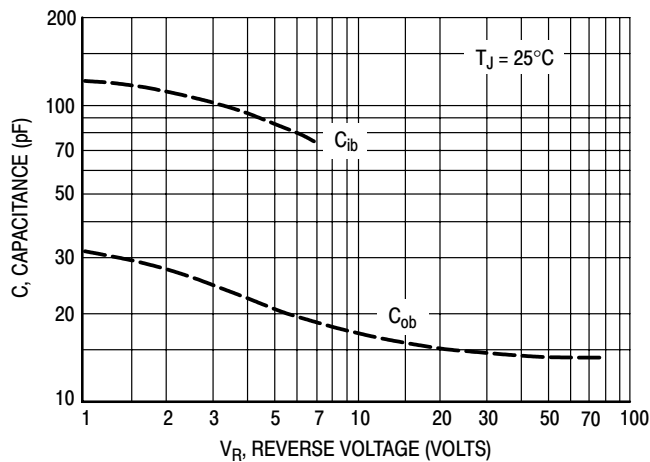


Figure 11. Capacitance

## MJD243 (NPN), MJD253 (PNP)

### TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time.

The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

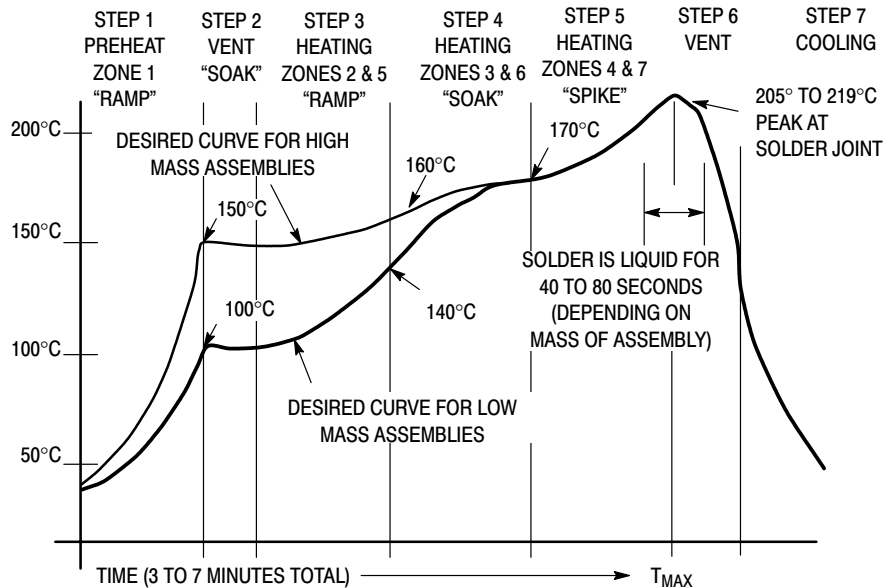


Figure 12. Typical Solder Heating Profile

# Complementary Power Transistors

## DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel (“T4” Suffix)
- Electrically Similar to MJE2955 and MJE3055
- DC Current Gain Specified to 10 Amperes
- High Current Gain–Bandwidth Product —  
 $f_T = 2.0 \text{ MHz (Min) @ } I_C$   
 $= 500 \text{ mAdc}$

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	Vdc
Collector–Base Voltage	$V_{CB}$	70	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
Collector Current	$I_C$	10	Adc
Base Current	$I_B$	6	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_{D\dagger}$	20 0.16	Watts W/ $^\circ\text{C}$
Total Power Dissipation (1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$

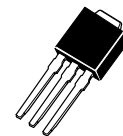
(1) These ratings are applicable when surface mounted on the minimum pad sizes recommended.  
 †Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

**PNP**  
**MJD2955**  
**NPN**  
**MJD3055**

**SILICON**  
**POWER TRANSISTORS**  
**10 AMPERES**  
**60 VOLTS**  
**20 WATTS**

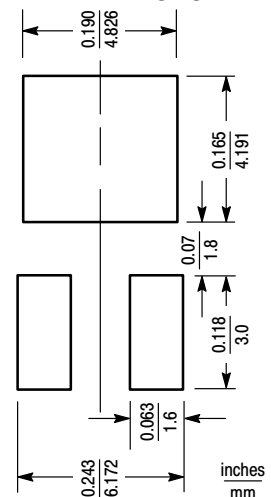


CASE 369A-13



CASE 369-07

### MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



# MJD2955 MJD3055

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	50	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 70\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 70\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	— —	0.02 2	mAdc
Collector Cutoff Current ( $V_{CB} = 70\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 70\text{ Vdc}$ , $I_E = 0$ , $T_C = 150^\circ\text{C}$ )	$I_{CBO}$	— —	0.02 2	mAdc
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	0.5	mAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain (1) ( $I_C = 4\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 10\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$h_{FE}$	20 5	100 —	—
Collector–Emitter Saturation Voltage (1) ( $I_C = 4\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 3.3\text{ Adc}$ )	$V_{CE(sat)}$	— —	1.1 8	Vdc
Base–Emitter On Voltage (1) ( $I_C = 4\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$V_{BE(on)}$	—	1.8	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain — Bandwidth Product ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 500\text{ kHz}$ )	$f_T$	2	—	MHz

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

# MJD2955 MJD3055

## TYPICAL CHARACTERISTICS

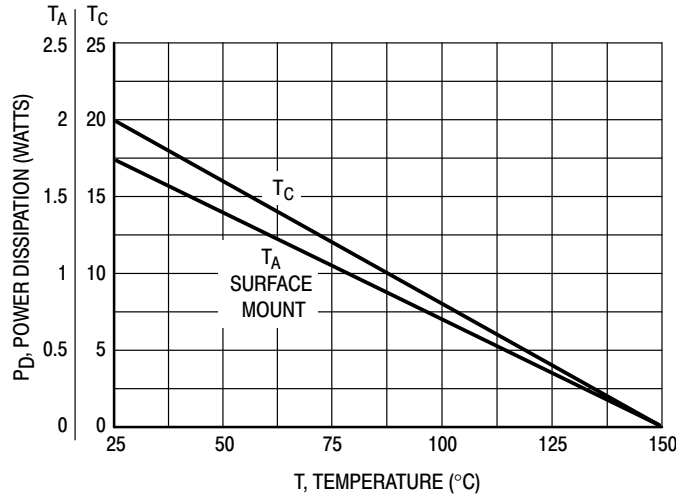


Figure 1. Power Derating

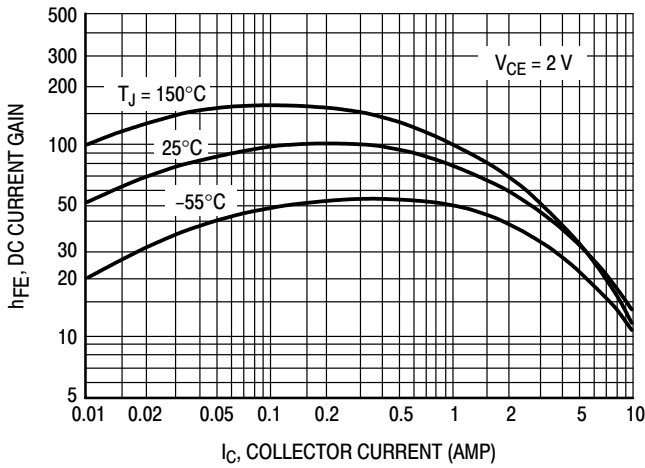


Figure 2. DC Current Gain

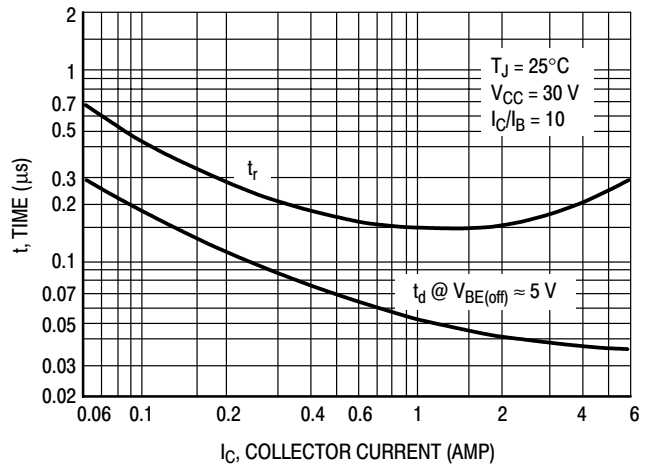


Figure 3. Turn-On Time

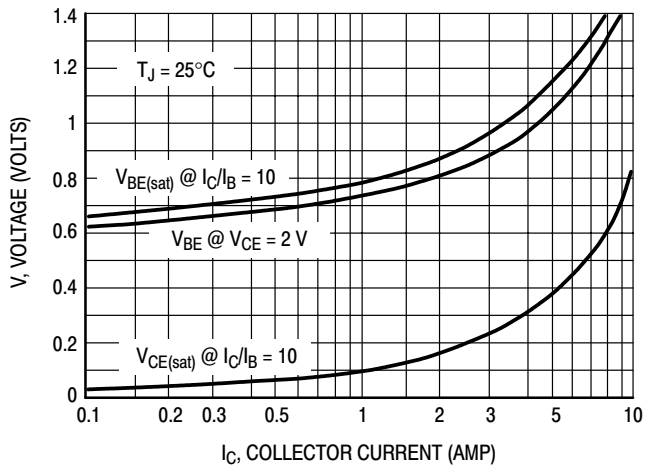


Figure 4. "On" Voltages. MJD3055

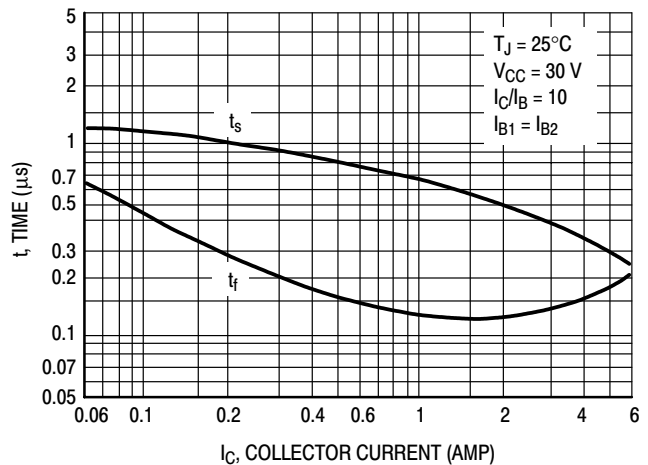


Figure 5. Turn-Off Time



# MJD2955 MJD3055

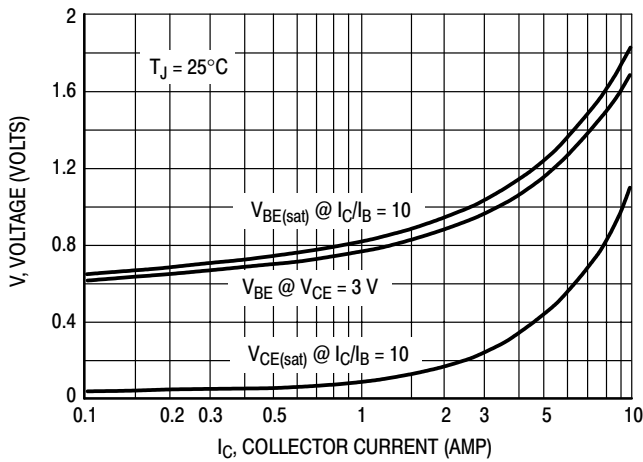


Figure 6. "On" Voltages, MJD2955

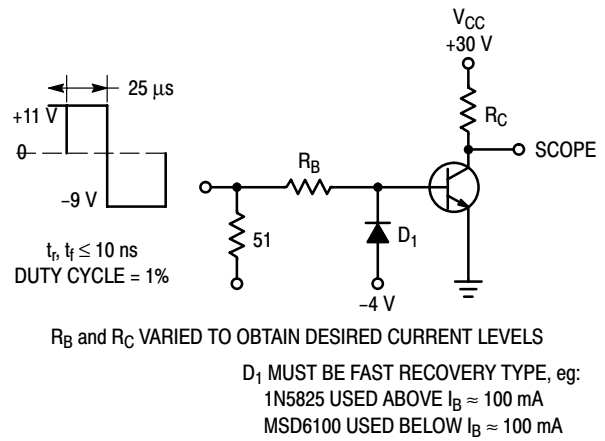


Figure 7. Switching Time Test Circuit

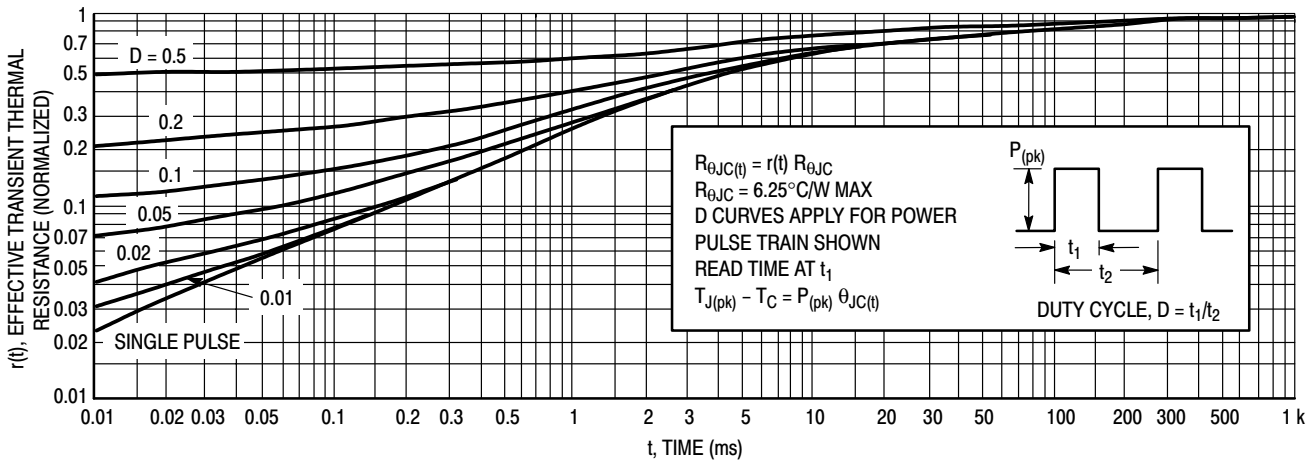


Figure 8. Thermal Response

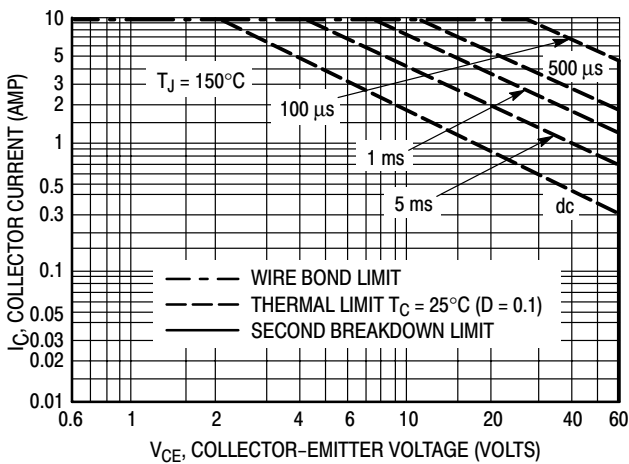


Figure 9. Maximum Forward Bias Safe Operating Area

## FORWARD BIAS SAFE OPERATING AREA INFORMATION

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# MJD31, MJD31C (NPN), MJD32, MJD32C (PNP)

MJD31C and MJD32C are Preferred Devices

## Complementary Power Transistors

### DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Electrically Similar to Popular TIP31 and TIP32 Series

#### MAXIMUM RATINGS

Rating	Symbol	MJD31 MJD32	MJD31C MJD32C	Unit
Collector–Emitter Voltage	$V_{CEO}$	40	100	Vdc
Collector–Base Voltage	$V_{CB}$	40	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5		Vdc
Collector Current – Continuous Peak	$I_C$	3 5		Adc
Base Current	$I_B$	1		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	15 0.12		Watts W/ $^\circ\text{C}$
Total Power Dissipation (Note 1.) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.56 0.012		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C}$

1. These ratings are applicable when surface mounted on the minimum pad size recommended.

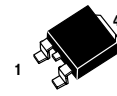


ON Semiconductor™

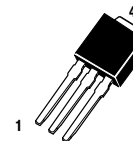
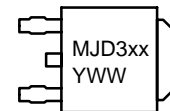
<http://onsemi.com>

**SILICON  
POWER TRANSISTORS  
3 AMPERES  
40 AND 100 VOLTS  
15 WATTS**

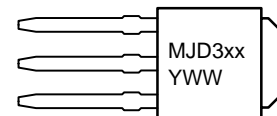
#### MARKING DIAGRAMS



DPAK  
CASE 369A  
STYLE 1



DPAK  
STRAIGHT LEADS  
CASE 369  
STYLE 1



MJD3xx = Specific Device Code  
xx = 1, 1C, 2 or 2C  
Y = Year  
WW = Work Week

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 437 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

# MJD31, MJD31C (NPN), MJD32, MJD32C (PNP)

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.3	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient (Note 2.)	$R_{\theta JA}$	80	$^{\circ}\text{C}/\text{W}$
Lead Temperature for Soldering Purposes	$T_L$	260	$^{\circ}\text{C}$

2. These ratings are applicable when surface mounted on the minimum pad size recommended.

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (Note 3.) ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	MJD31, MJD32 MJD31C, MJD32C	$V_{CE(sus)}$	40 100	– –	Vdc
Collector Cutoff Current ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	MJD31, MJD32 MJD31C, MJD32C	$I_{CEO}$	–	50	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB} = 0$ )		$I_{CES}$	–	20	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	–	1	mAdc

### ON CHARACTERISTICS (Note 3.)

DC Current Gain ( $I_C = 1\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 3\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )		$h_{FE}$	25 10	– 50	–
Collector–Emitter Saturation Voltage ( $I_C = 3\text{ Adc}$ , $I_B = 375\text{ mA}$ )		$V_{CE(sat)}$	–	1.2	Vdc
Base–Emitter On Voltage ( $I_C = 3\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )		$V_{BE(on)}$	–	1.8	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product (Note 4.) ( $I_C = 500\text{ mA}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )		$f_T$	3	–	MHz
Small–Signal Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ kHz}$ )		$h_{fe}$	20	–	–

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

4.  $f_T = |h_{fe}| \cdot f_{test}$ .

# MJD31, MJD31C (NPN), MJD32, MJD32C (PNP)

## TYPICAL CHARACTERISTICS

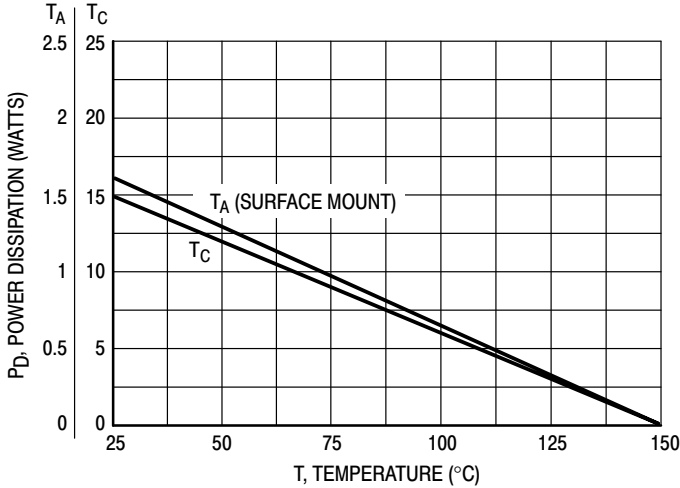
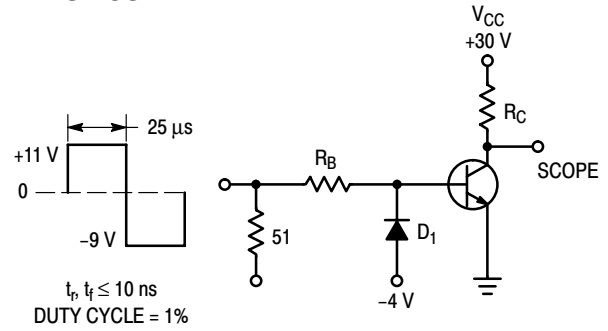


Figure 1. Power Derating



$R_B$  and  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS  
 $D_1$  MUST BE FAST RECOVERY TYPE, e.g.:  
 1N5825 USED ABOVE  $I_B \approx 100$  mA  
 MSD6100 USED BELOW  $I_B \approx 100$  mA  
 REVERSE ALL POLARITIES FOR PNP.

Figure 2. Switching Time Test Circuit

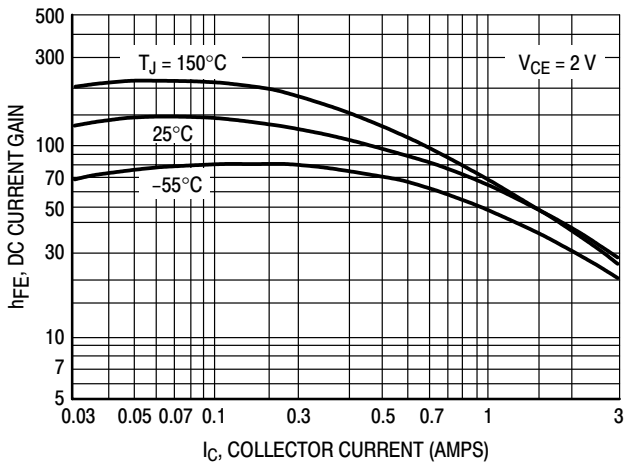


Figure 3. DC Current Gain

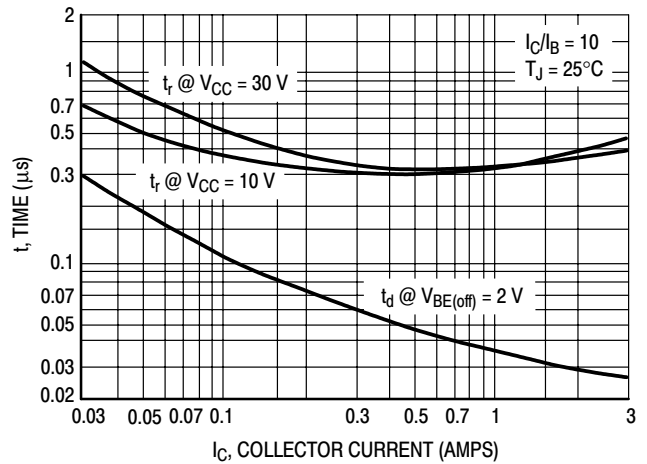


Figure 4. Turn-On Time

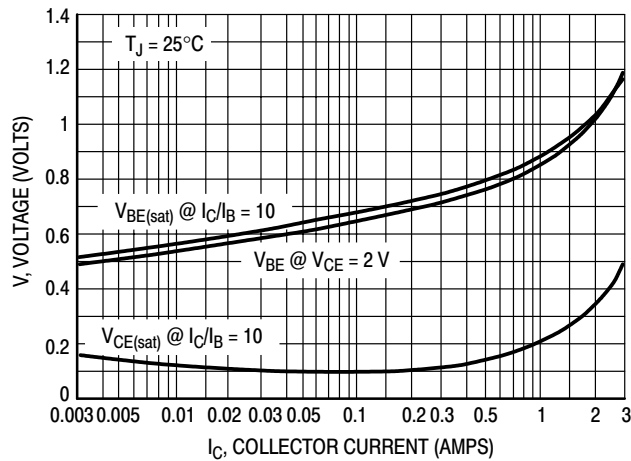


Figure 5. "On" Voltages

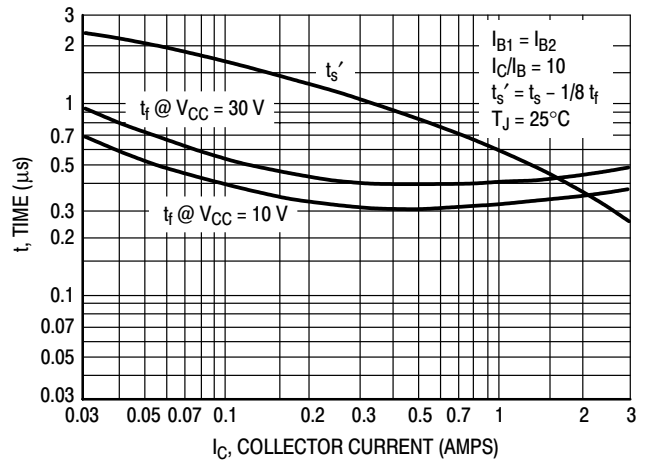


Figure 6. Turn-Off Time

# MJD31, MJD31C (NPN), MJD32, MJD32C (PNP)

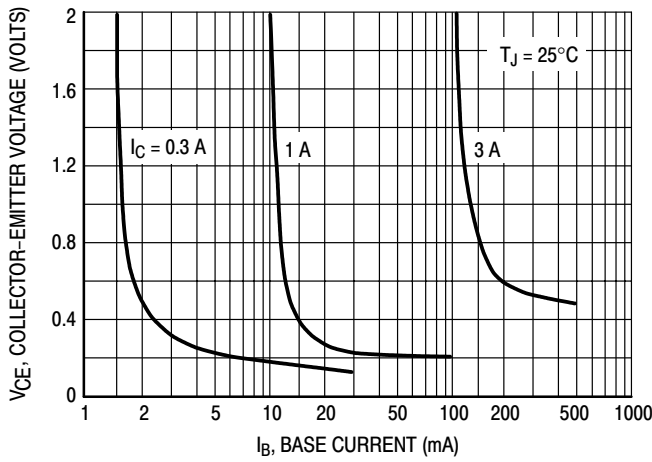


Figure 7. Collector Saturation Region

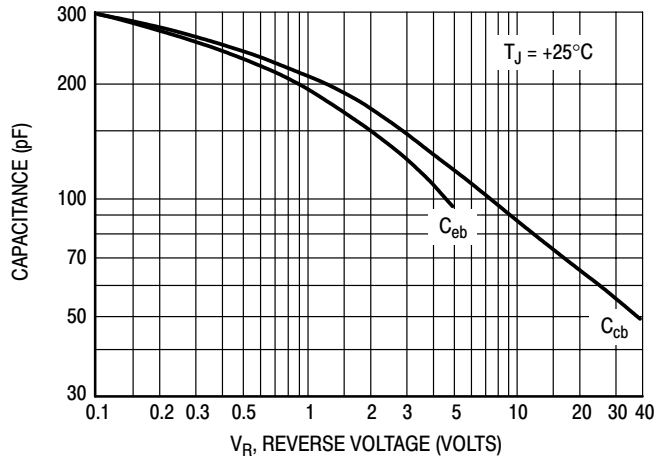


Figure 8. Capacitance

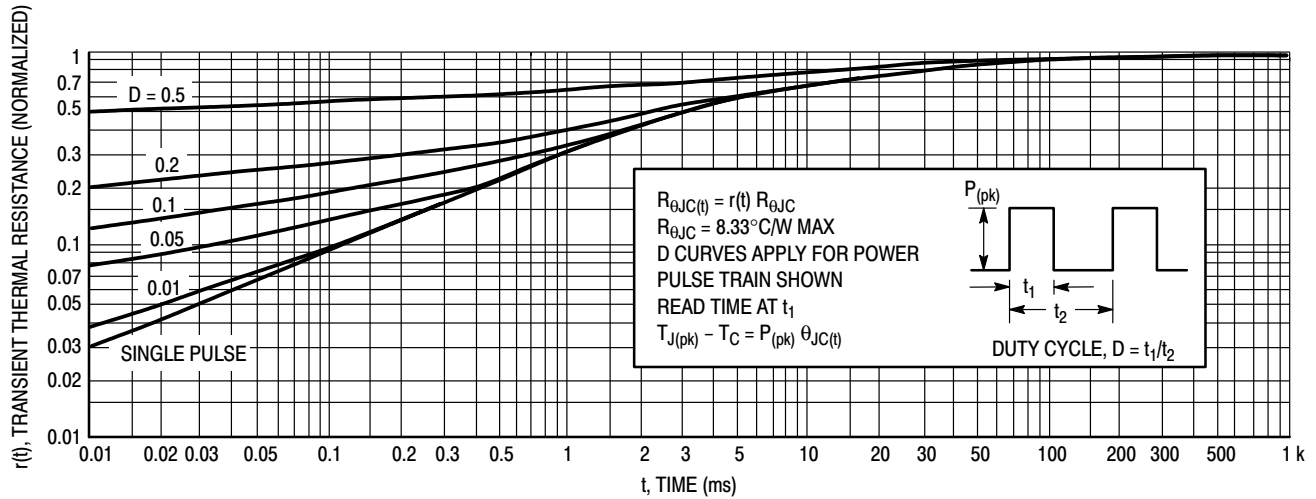


Figure 9. Thermal Response

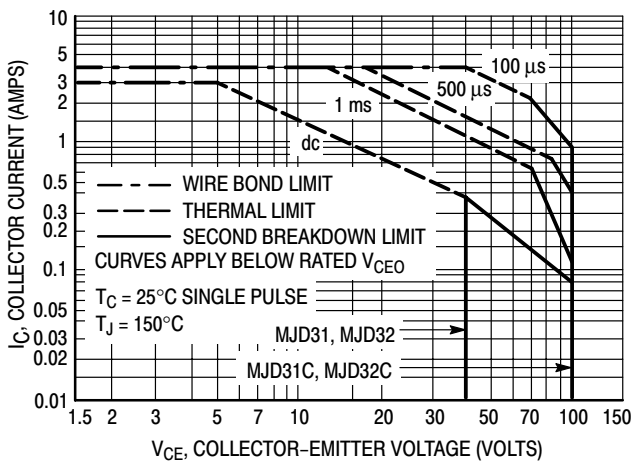


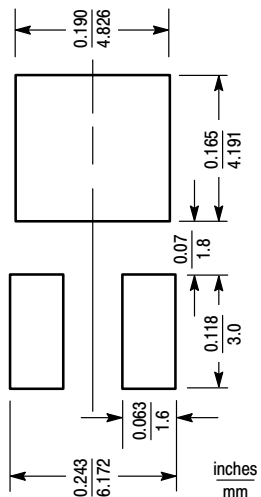
Figure 10. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# MJD31, MJD31C (NPN), MJD32, MJD32C (PNP)

## MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



### ORDERING INFORMATION

Device	Package	Shipping
MJD31C	DPAK	75 Units / Rail
MJD31CRL	DPAK	1800 Tape & Reel
MJD31CT4	DPAK	2500 Tape & Reel
MJD31C-1	DPAK Straight Leads	75 Units / Rail
MJD31T4	DPAK	2500 Tape & Reel
MJD32C	DPAK	75 Units / Rail
MJD32CRL	DPAK	1800 Tape & Reel
MJD32CT4	DPAK	2500 Tape & Reel
MJD32C-1	DPAK Straight Leads	75 Units / Rail
MJD32RL	DPAK	1800 Tape & Reel
MJD32T4	DPAK	2500 Tape & Reel

# High Voltage Power Transistors

## DPAK For Surface Mount Applications

Designed for line operated audio output amplifier, switchmode power supply drivers and other switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Electrically Similar to Popular MJE340 and MJE350
- 300 V (Min) —  $V_{CEO(sus)}$
- 0.5 A Rated Collector Current

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	300	Vdc
Collector–Base Voltage	$V_{CB}$	300	Vdc
Emitter–Base Voltage	$V_{EB}$	3	Vdc
Collector Current — Continuous — Peak	$I_C$	0.5 0.75	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	15 0.12	Watts W/ $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.56 0.012	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	$^\circ\text{C/W}$
Lead Temperature for Soldering Purpose	$T_L$	260	$^\circ\text{C}$

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) ( $I_C = 1 \text{ mAdc}, I_B = 0$ )	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current ( $V_{CB} = 300 \text{ Vdc}, I_E = 0$ )	$I_{CBO}$	—	0.1	mAdc
Emitter Cutoff Current ( $V_{BE} = 3 \text{ Vdc}, I_C = 0$ )	$I_{EBO}$	—	0.1	mAdc

### ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 50 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$ )	$h_{FE}$	30	240	—
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\*When surface mounted on minimum pad sizes recommended.

(1) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

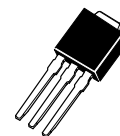
**NPN**  
**MJD340\***  
**PNP**  
**MJD350\***

\*ON Semiconductor Preferred Device

**SILICON**  
**POWER TRANSISTORS**  
**0.5 AMPERE**  
**300 VOLTS**  
**15 WATTS**

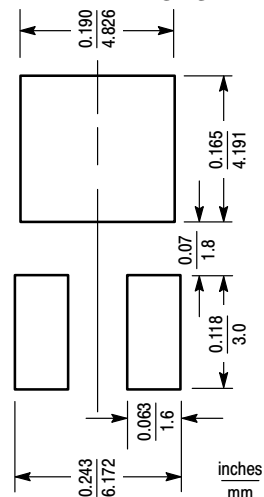


CASE 369A-13



CASE 369-07

### MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



# MJD340 MJD350

## TYPICAL CHARACTERISTICS

### MJD340

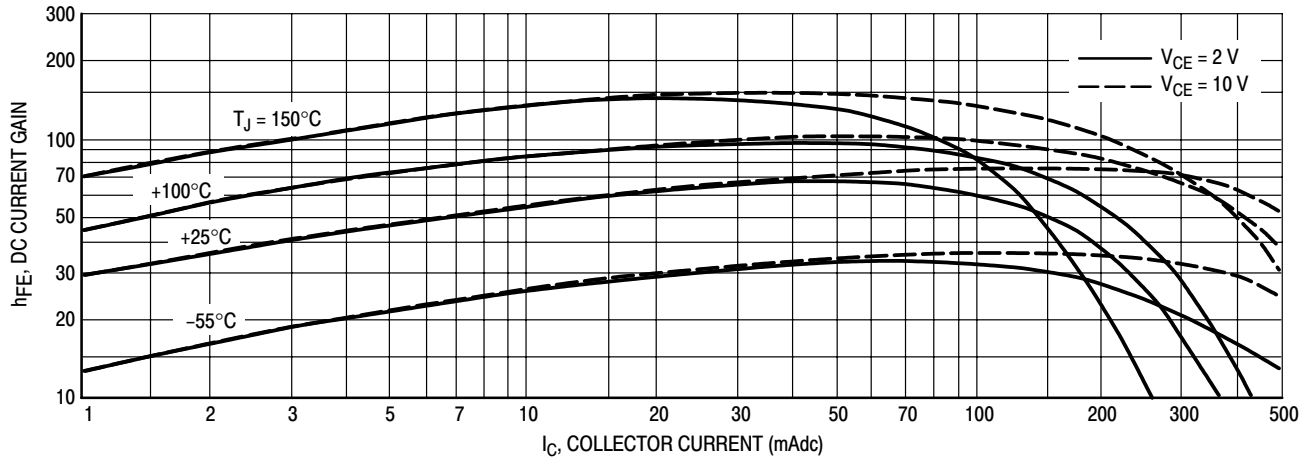


Figure 1. DC Current Gain

### MJD340

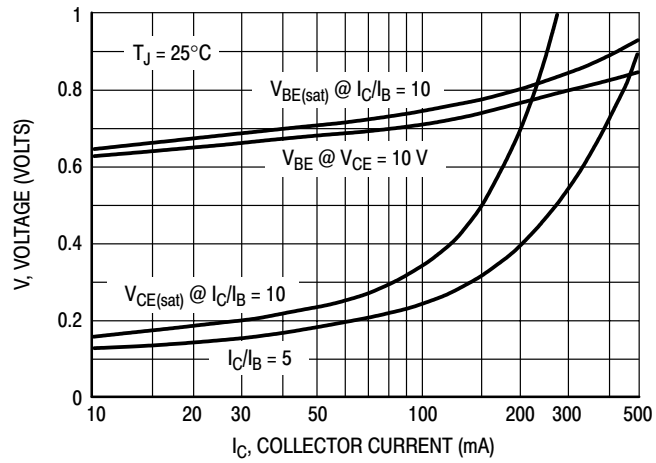


Figure 2. "On" Voltages



# MJD340 MJD350

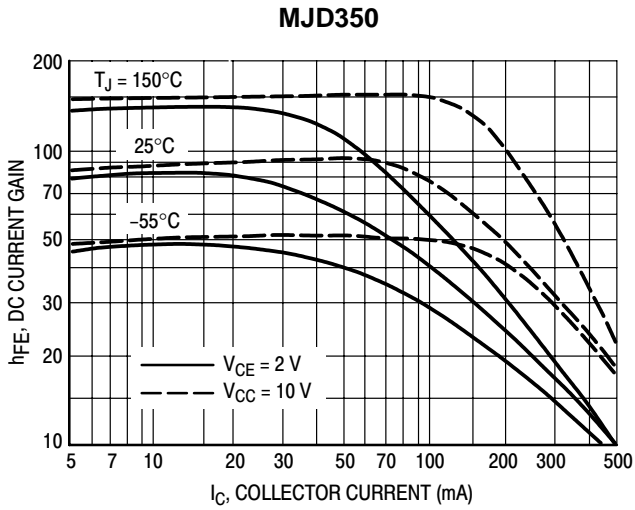


Figure 3. DC Current Gain

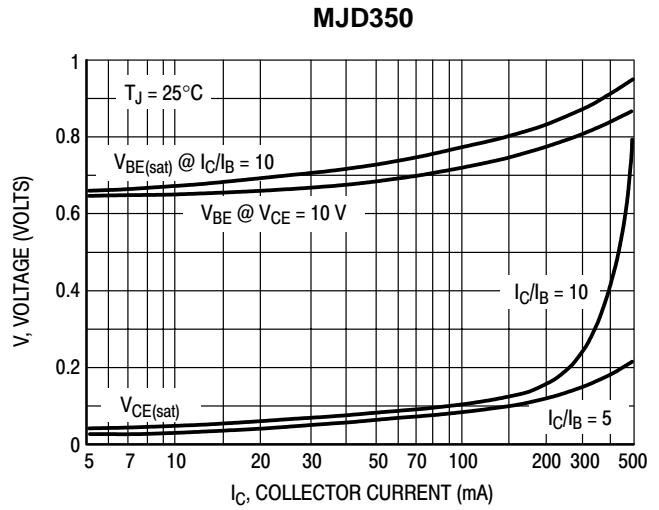


Figure 4. "On" Voltages

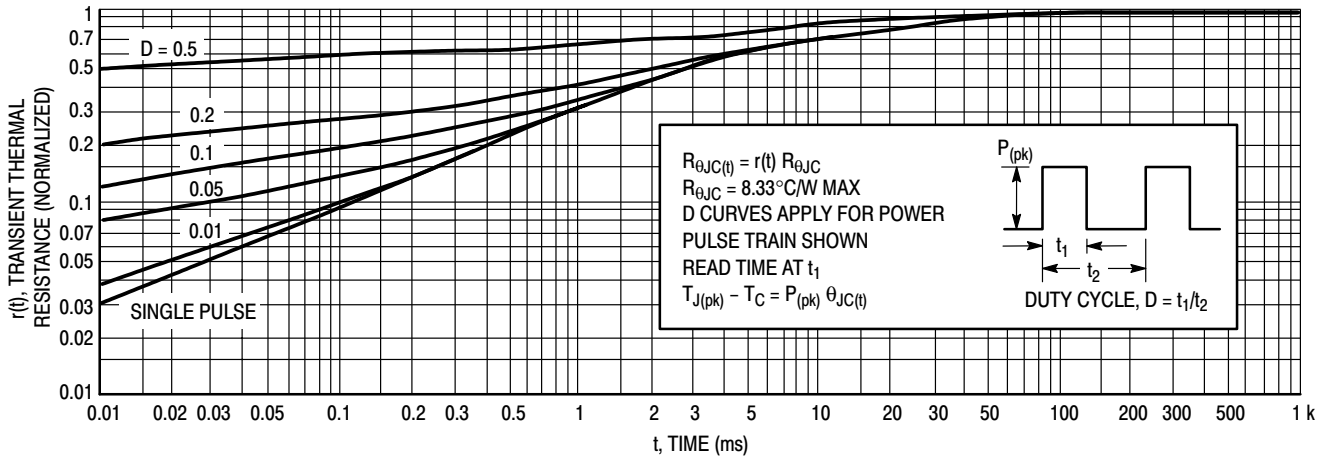


Figure 5. Thermal Response

## MJD340 MJD350

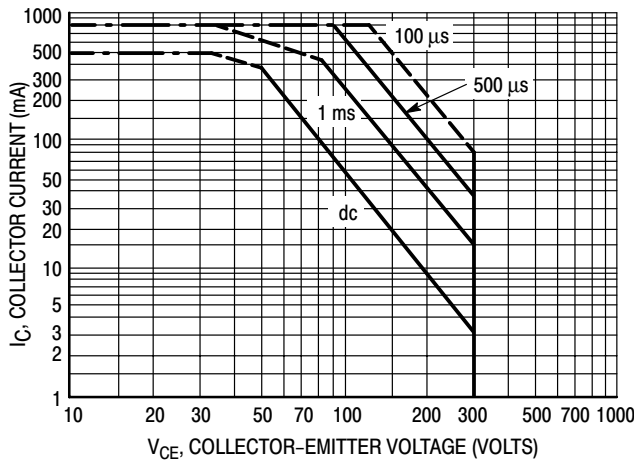


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

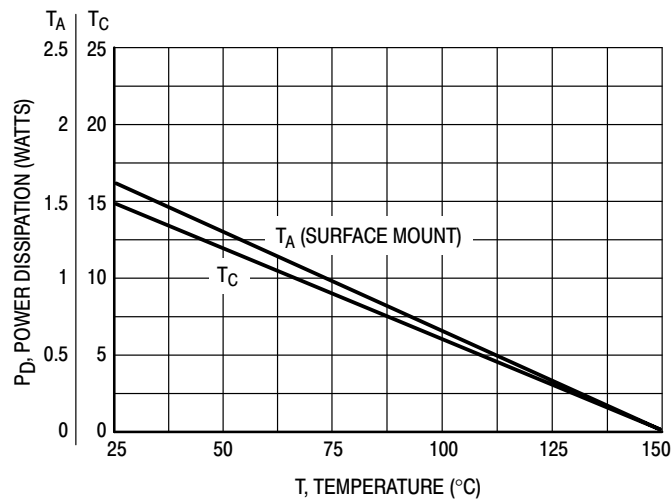


Figure 7. Power Derating

# Complementary Power Transistors

## DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Electrically Similar to Popular TIP41 and TIP42 Series
- Monolithic Construction With Built-in Base-Emitter Resistors

### MAXIMUM RATINGS

Rating	Symbol	MJD41C MJD42C	Unit
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5	Vdc
Collector Current — Continuous Peak	$I_C$	6 10	Adc
Base Current	$I_B$	2	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	Watts W/ $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$

\*These ratings are applicable when surface mounted on the minimum pad size recommended.

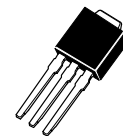
**NPN  
MJD41C\***  
**PNP  
MJD42C\***

\*ON Semiconductor Preferred Device

**SILICON  
POWER TRANSISTORS  
6 AMPERES  
100 VOLTS  
20 WATTS**

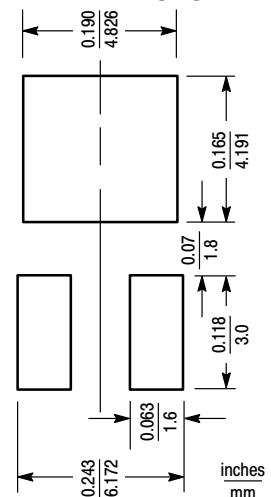


CASE 369A-13



CASE 369-07

### MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJD41C MJD42C

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	50	$\mu\text{A}$
Collector Cutoff Current ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB} = 0$ )	$I_{CES}$	—	10	$\mu\text{A}$
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	0.5	$\text{mA}$

### ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 0.3\text{ A}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 3\text{ A}$ , $V_{CE} = 4\text{ Vdc}$ )	$h_{FE}$	30 15	— 75	—
Collector–Emitter Saturation Voltage ( $I_C = 6\text{ A}$ , $I_B = 600\text{ mA}$ )	$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter On Voltage ( $I_C = 6\text{ A}$ , $V_{CE} = 4\text{ Vdc}$ )	$V_{BE(on)}$	—	2	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product (2) ( $I_C = 500\text{ mA}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )	$f_T$	3	—	MHz
Small–Signal Current Gain ( $I_C = 0.5\text{ A}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ kHz}$ )	$h_{fe}$	20	—	—

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

(2)  $f_T = |h_{fe}| \cdot f_{test}$ .

# MJD41C MJD42C

## TYPICAL CHARACTERISTICS

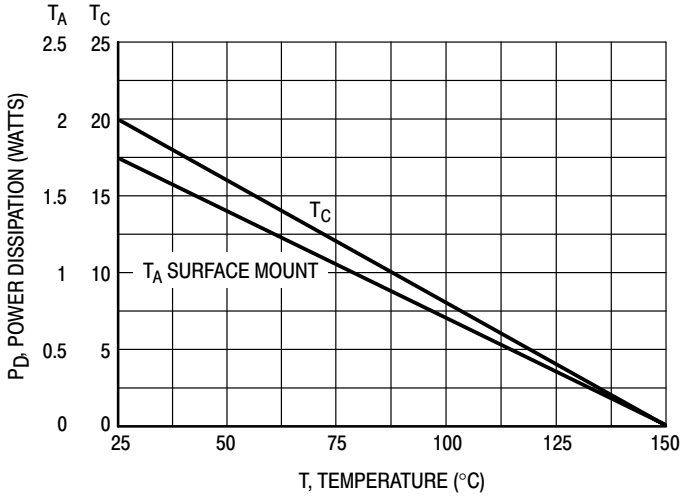
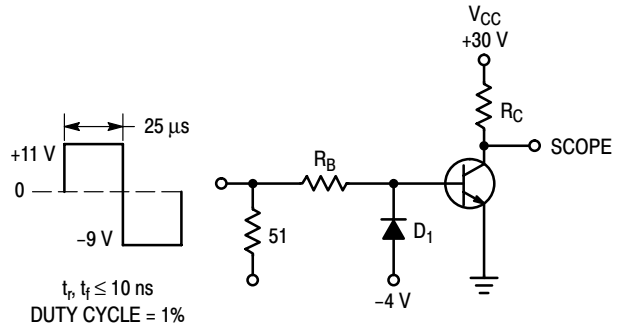


Figure 8. Power Derating



R<sub>B</sub> and R<sub>C</sub> VARIED TO OBTAIN DESIRED CURRENT LEVELS  
 D<sub>1</sub> MUST BE FAST RECOVERY TYPE, e.g.:  
 MSB5300 USED ABOVE I<sub>B</sub> ≈ 100 mA  
 MSD6100 USED BELOW I<sub>B</sub> ≈ 100 mA  
 REVERSE ALL POLARITIES FOR PNP.

Figure 9. Switching Time Test Circuit

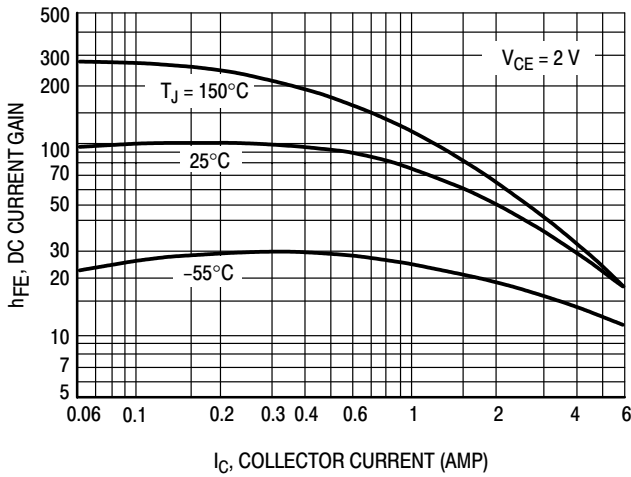


Figure 10. DC Current Gain

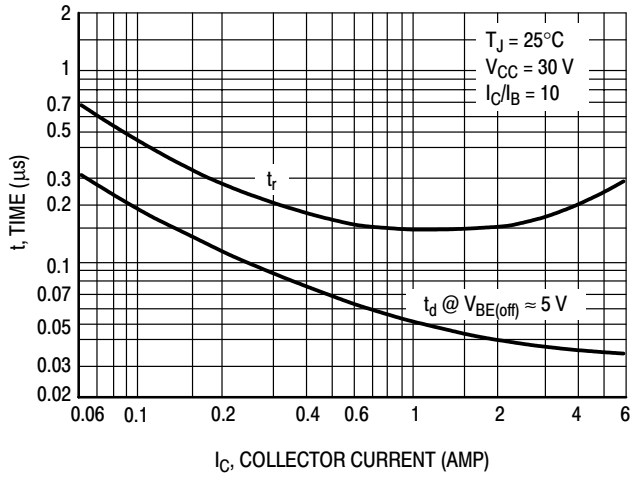


Figure 11. Turn-On Time

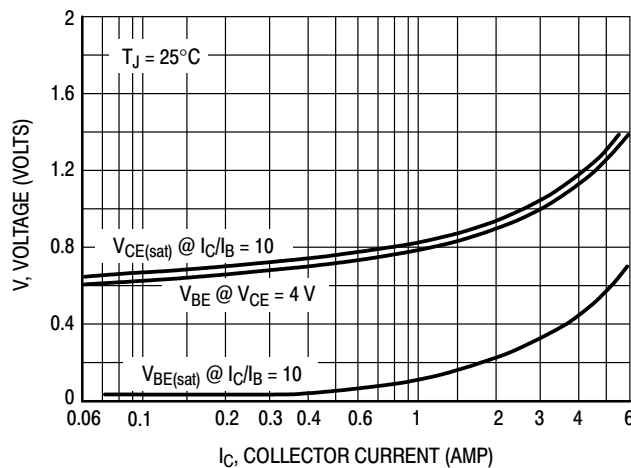


Figure 12. "On" Voltages

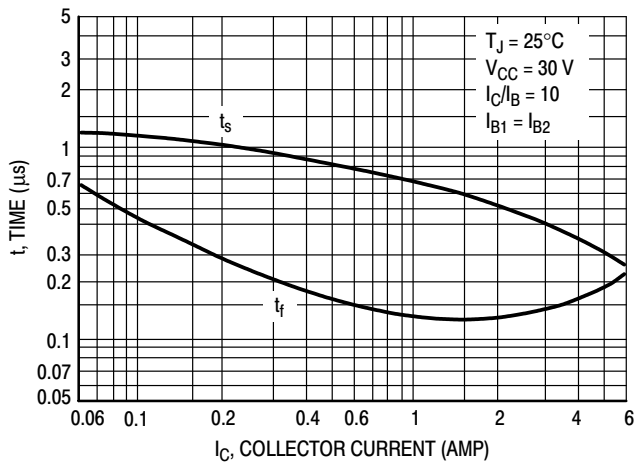


Figure 13. Turn-Off Time

# MJD41C MJD42C

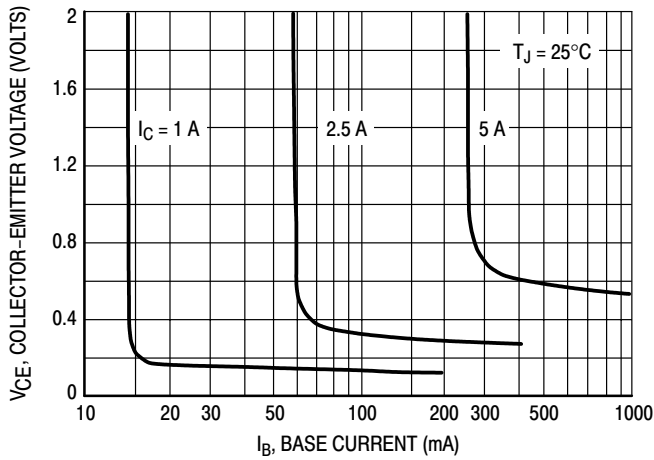


Figure 14. Collector Saturation Region

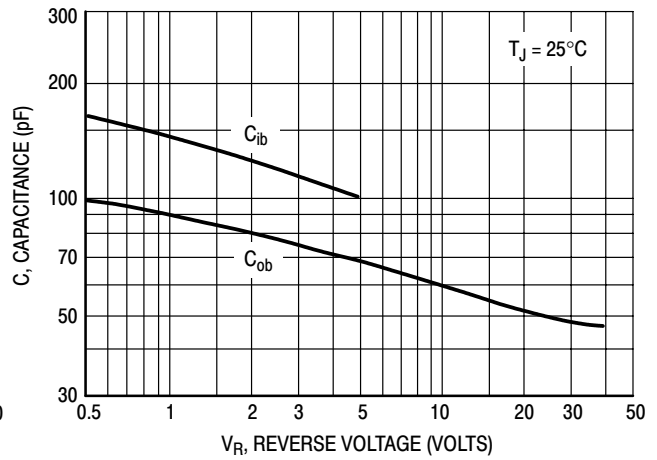


Figure 15. Capacitance

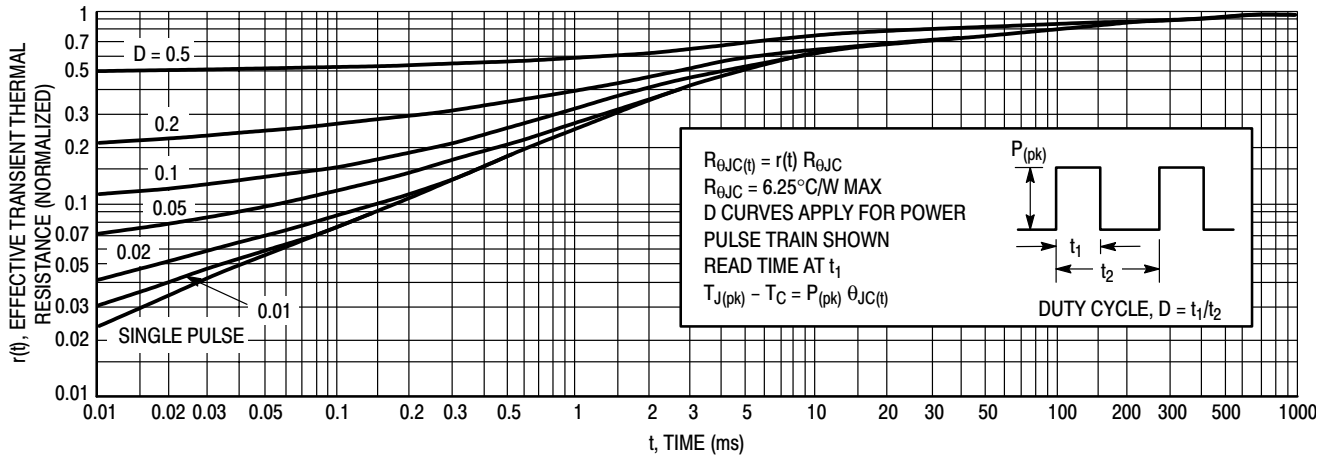


Figure 16. Thermal Response

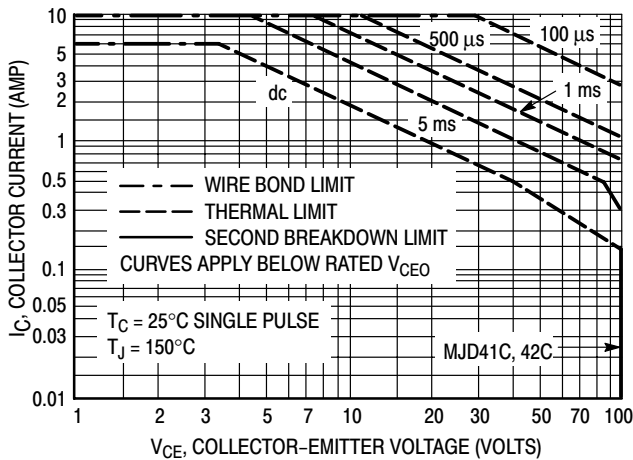


Figure 17. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 17 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 16. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# Darlington Power Transistor DPAK For Surface Mount Application

... for general purpose power and switching output or driver stages in applications such as switching regulators, converters, and power amplifiers.

- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel for Surface Mount (“T4” Suffix)
- Electrically Similar to Popular D44E3 Device
- High DC Gain — 1000 Min @ 5.0 Adc
- Low Sat. Voltage — 1.5 V @ 5.0 Adc
- Compatible With Existing Automatic Pick & Place Equipment

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Emitter–Base Voltage	$V_{EB}$	7	Vdc
Collector Current — Continuous	$I_C$	10	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	Watts W/ $^\circ\text{C}$
Total Power Dissipation (1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

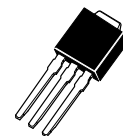
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$
Lead Temperature for Soldering	$T_L$	260	$^\circ\text{C}$

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

## MJD44E3\*

\*ON Semiconductor Preferred Device

**NPN DARLINGTON  
SILICON  
POWER TRANSISTOR  
10 AMPERES  
80 VOLTS  
20 WATTS**

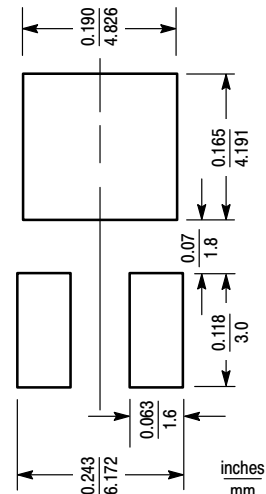


CASE 369-07



CASE 369A-13

## MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJD44E3

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}, V_{BE} = 0$ )	$I_{CES}$	—	—	10	$\mu\text{A}$
Emitter Cutoff Current ( $V_{EB} = 7 \text{ Vdc}$ )	$I_{EBO}$	—	—	1	$\mu\text{A}$

## ON CHARACTERISTICS

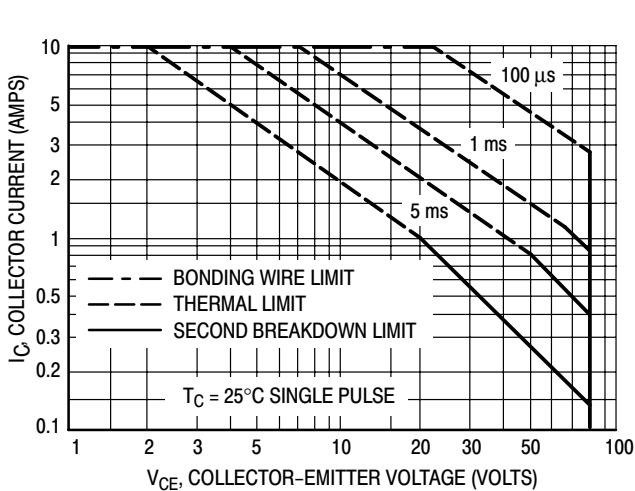
Collector–Emitter Saturation Voltage ( $I_C = 5 \text{ Adc}, I_B = 10 \text{ mAdc}$ ) ( $I_C = 10 \text{ Adc}, I_B = 20 \text{ mAdc}$ )	$V_{CE(\text{sat})}$	— —	— —	1.5 2	Vdc
Base–Emitter Saturation Voltage ( $I_C = 5 \text{ Adc}, I_B = 10 \text{ mAdc}$ )	$V_{BE(\text{sat})}$	—	—	2.5	Vdc
DC Current Gain ( $V_{CE} = 5 \text{ Vdc}, I_C = 5 \text{ Adc}$ )	$h_{FE}$	1000	—	—	—

## DYNAMIC CHARACTERISTICS

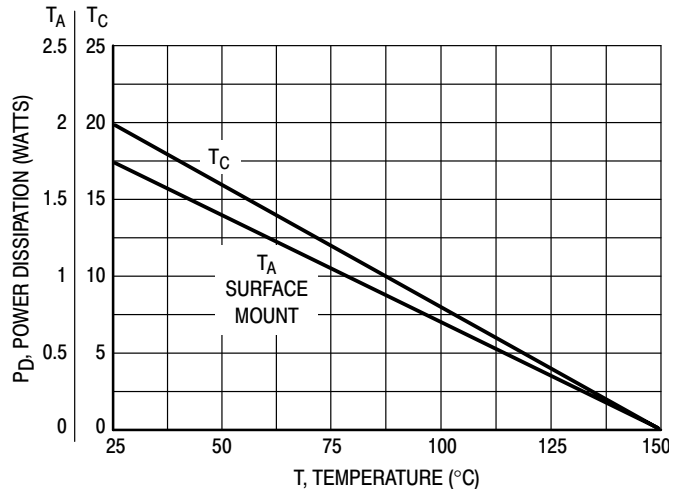
Collector Capacitance ( $V_{CB} = 10 \text{ Vdc}, f_{\text{test}} = 1 \text{ MHz}$ )	$C_{cb}$	—	—	130	$\text{pF}$
---	----------	---	---	-----	-------------

## SWITCHING TIMES

Delay and Rise Times ( $I_C = 10 \text{ Adc}, I_{B1} = 20 \text{ mAdc}$ )	$t_d + t_r$	—	0.6	—	$\mu\text{s}$
Storage Time ( $I_C = 10 \text{ Adc}, I_{B1} = I_{B2} = 20 \text{ mAdc}$ )	$t_s$	—	2	—	$\mu\text{s}$
Fall Time ( $I_C = 10 \text{ Adc}, I_{B1} = I_{B2} = 20 \text{ mAdc}$ )	$t_f$	—	0.5	—	$\mu\text{s}$



**Figure 1. Maximum Forward Bias Safe Operating Area**



**Figure 2. Power Derating**



# Complementary Power Transistors

## DPAK For Surface Mount Applications

... for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel for Surface Mount (“T4” Suffix)
- Electrically Similar to Popular D44H/D45H Series
- Low Collector Emitter Saturation Voltage —  
 $V_{CE(sat)} = 1.0 \text{ Volt Max @ } 8.0 \text{ Amperes}$
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

### MAXIMUM RATINGS

Rating	Symbol	D44H11 or D45H11	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
Collector Current — Continuous Peak	$I_C$	8 16	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	Watts W/ $^\circ\text{C}$
Total Power Dissipation (1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$
Lead Temperature for Soldering	$T_L$	260	$^\circ\text{C}$

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

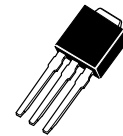
**NPN**  
**MJD44H11 \***  
**PNP**  
**MJD45H11 \***

\*ON Semiconductor Preferred Device

**SILICON**  
**POWER TRANSISTORS**  
**8 AMPERES**  
**80 VOLTS**  
**20 WATTS**

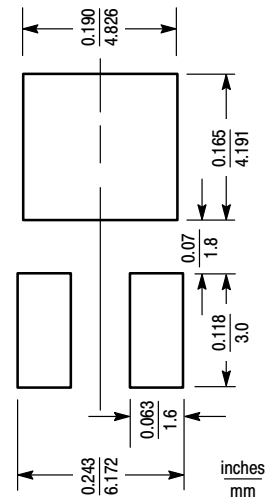


CASE 369A-13



CASE 369-07

### MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



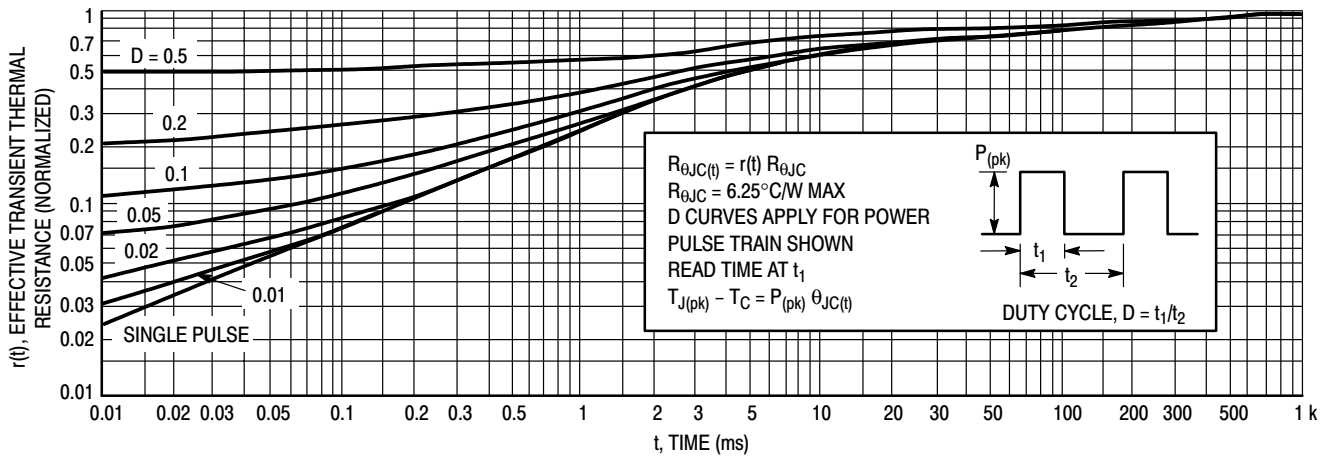
Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJD44H11 MJD45H11

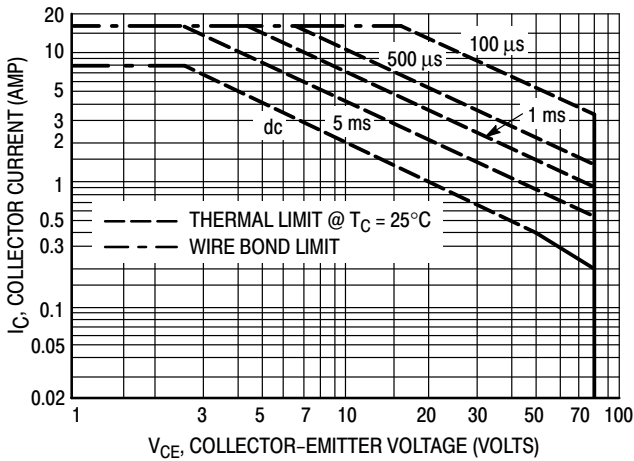
## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
<b>OFF CHARACTERISTICS</b>						
Collector–Emitter Sustaining Voltage ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CE(sus)}$	80	—	—	Vdc	
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CE0}$ , $V_{BE} = 0$ )	$I_{CES}$	—	—	10	$\mu\text{A}$	
Emitter Cutoff Current ( $V_{EB} = 5\text{ Vdc}$ )	$I_{EBO}$	—	—	50	$\mu\text{A}$	
<b>ON CHARACTERISTICS</b>						
Collector–Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )	$V_{CE(sat)}$	—	—	1	Vdc	
Base–Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.8\text{ Adc}$ )	$V_{BE(sat)}$	—	—	1.5	Vdc	
DC Current Gain ( $V_{CE} = 1\text{ Vdc}$ , $I_C = 2\text{ Adc}$ )	$h_{FE}$	60	—	—	—	
DC Current Gain ( $V_{CE} = 1\text{ Vdc}$ , $I_C = 4\text{ Adc}$ )		40	—	—		
<b>DYNAMIC CHARACTERISTICS</b>						
Collector Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )	MJD44H11 MJD45H11	$C_{cb}$	—	130	—	$\mu\text{F}$
			—	230	—	
Gain Bandwidth Product ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 20\text{ MHz}$ )	MJD44H11 MJD45H11	$f_T$	—	50	—	MHz
			—	40	—	
<b>SWITCHING TIMES</b>						
Delay and Rise Times ( $I_C = 5\text{ Adc}$ , $I_{B1} = 0.5\text{ Adc}$ )	MJD44H11 MJD45H11	$t_d + t_r$	—	300	—	ns
			—	135	—	
Storage Time ( $I_C = 5\text{ Adc}$ , $I_{B1} = I_{B2} = 0.5\text{ Adc}$ )	MJD44H11 MJD45H11	$t_s$	—	500	—	ns
			—	500	—	
Fall Time ( $I_C = 5\text{ Adc}$ , $I_{B1} = I_{B2} = 0.5\text{ Adc}$ )	MJD44H11 MJD45H11	$t_f$	—	140	—	ns
			—	100	—	

# MJD44H11 MJD45H11



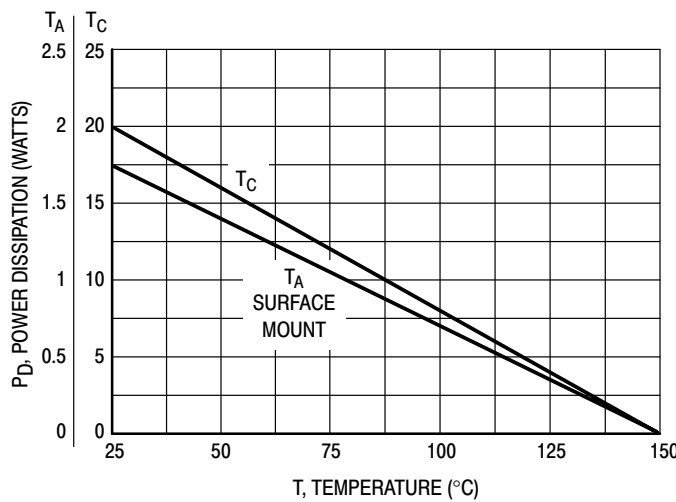
**Figure 1. Thermal Response**



**Figure 2. Maximum Forward Bias Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 3. Power Derating**

# MJD44H11 MJD45H11

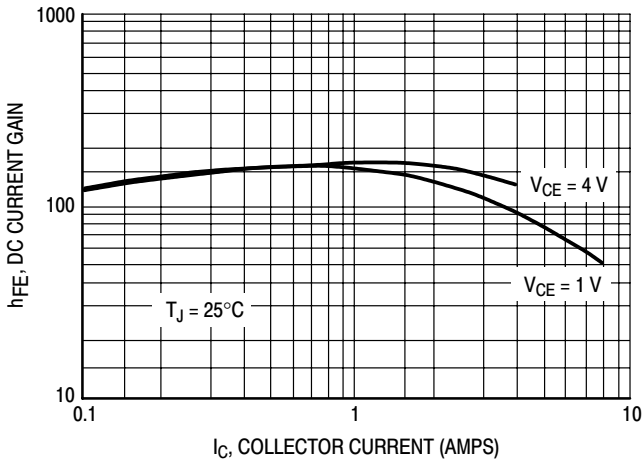


Figure 4. MJD44H11 DC Current Gain

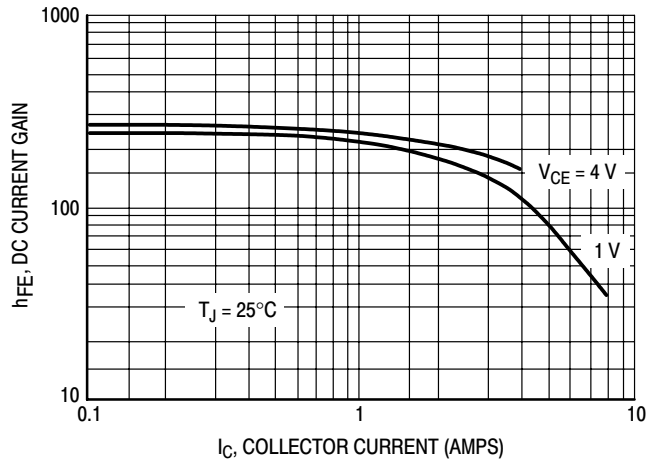


Figure 5. MJD45H11 DC Current Gain

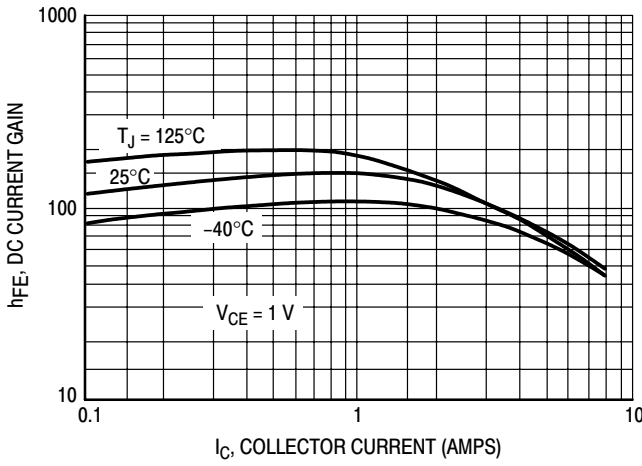


Figure 6. MJD44H11 Current Gain versus Temperature

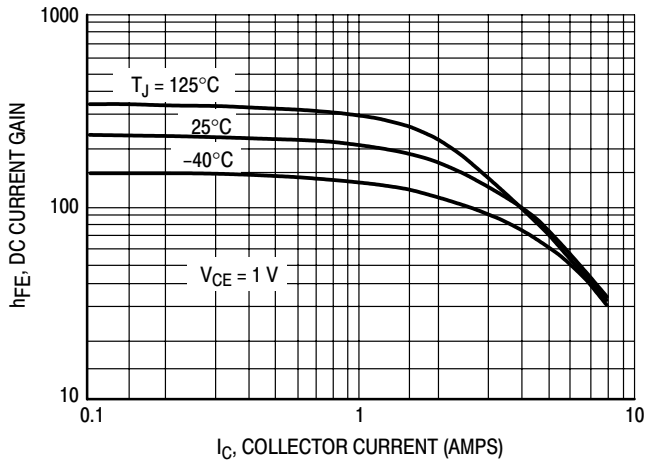


Figure 7. MJD45H11 Current Gain versus Temperature

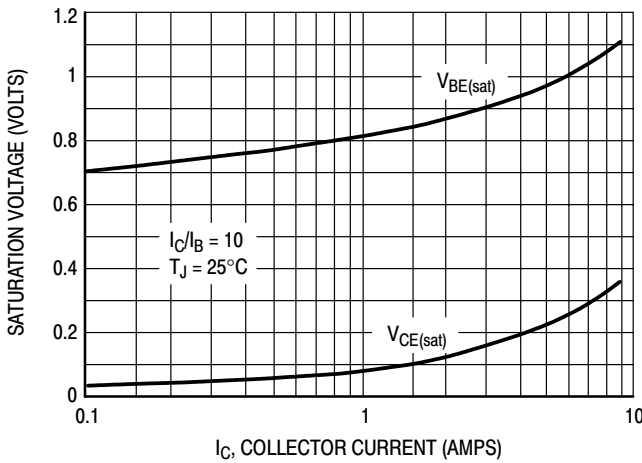


Figure 8. MJD44H11 On-Voltages

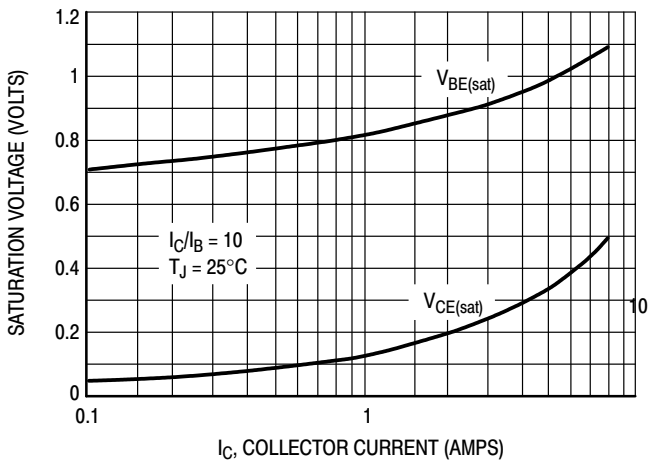


Figure 9. MJD45H11 On-Voltages

# High Voltage Power Transistors

## DPAK For Surface Mount Applications

Designed for line operated audio output amplifier, SWITCHMODE™ power supply drivers and other switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Electrically Similar to Popular TIP47, and TIP50
- 250 and 400 V (Min) —  $V_{CEO(sus)}$
- 1 A Rated Collector Current

### MAXIMUM RATINGS

Rating	Symbol	MJD47	MJD50	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	400	Vdc
Collector–Base Voltage	$V_{CB}$	350	500	Vdc
Emitter–Base Voltage	$V_{EB}$	5		Vdc
Collector Current — Continuous Peak	$I_C$	1 2		A dc
Base Current	$I_B$	0.6		A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	15 0.12		Watts W/ $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.56 0.0125		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150		$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	$^\circ\text{C/W}$
Lead Temperature for Soldering Purpose	$T_L$	260	$^\circ\text{C}$

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) ( $I_C = 30 \text{ mAdc}, I_B = 0$ )	MJD47 MJD50	$V_{CEO(sus)}$	250 400	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 150 \text{ Vdc}, I_B = 0$ ) ( $V_{CE} = 300 \text{ Vdc}, I_B = 0$ )	MJD47 MJD50	$I_{CEO}$	— —	0.2 0.2	mAdc

\*When surface mounted on minimum pad sizes recommended.

(continued)

(1) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

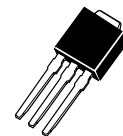
## MJD47\* MJD50\*

\*ON Semiconductor Preferred Device

**NPN SILICON  
POWER TRANSISTORS  
1 AMPERE  
250, 400 VOLTS  
15 WATTS**

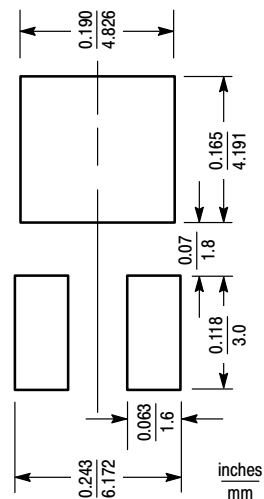


CASE 369A-13



CASE 369-07

### MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJD47 MJD50

## ELECTRICAL CHARACTERISTICS – continued ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS — continued

Collector Cutoff Current ( $V_{CE} = 350\text{ Vdc}$ , $V_{BE} = 0$ ) ( $V_{CE} = 500\text{ Vdc}$ , $V_{BE} = 0$ )	MJD47 MJD50	$I_{CES}$	— 0.1	mAdc
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	— 1	mAdc

### ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 0.3\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ ) ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ )	$h_{FE}$	30 10	150 —	—
Collector–Emitter Saturation Voltage ( $I_C = 1\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	$V_{CE(sat)}$	—	1	Vdc
Base–Emitter On Voltage ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ )	$V_{BE(on)}$	—	1.5	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ( $I_C = 0.2\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 2\text{ MHz}$ )	$f_T$	10	—	MHz
Small–Signal Current Gain ( $I_C = 0.2\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ kHz}$ )	$h_{fe}$	25	—	—

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

## TYPICAL CHARACTERISTICS

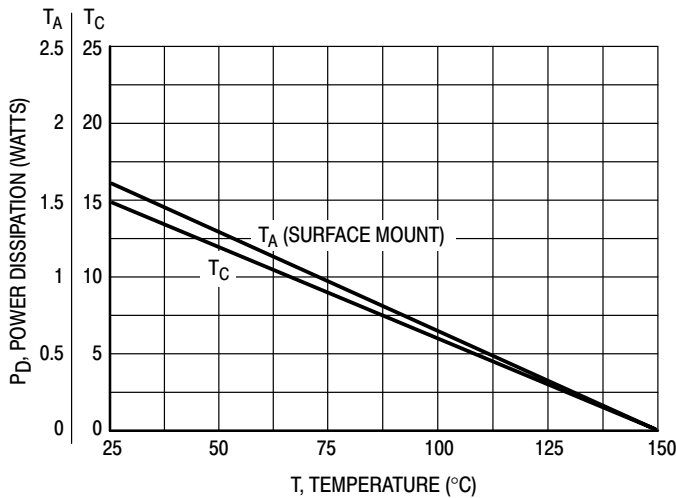


Figure 1. Power Derating

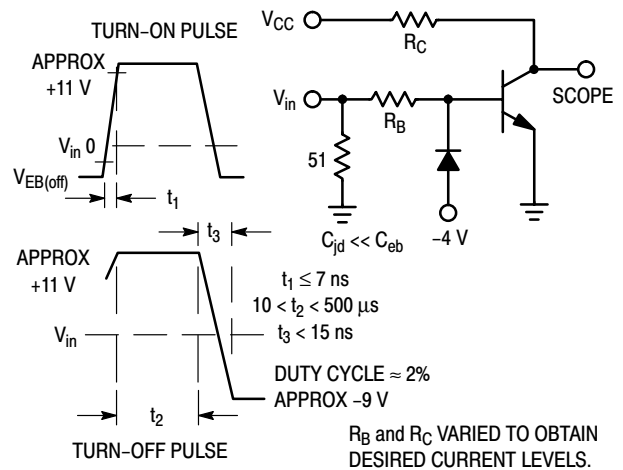


Figure 2. Switching Time Equivalent Circuit

# MJD47 MJD50

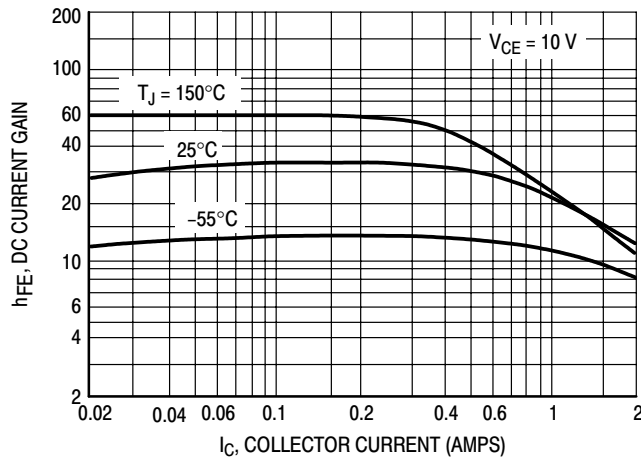


Figure 3. DC Current Gain

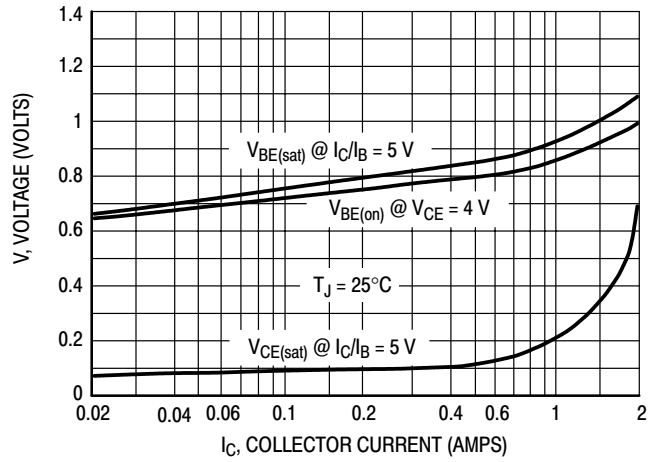


Figure 4. "On" Voltages

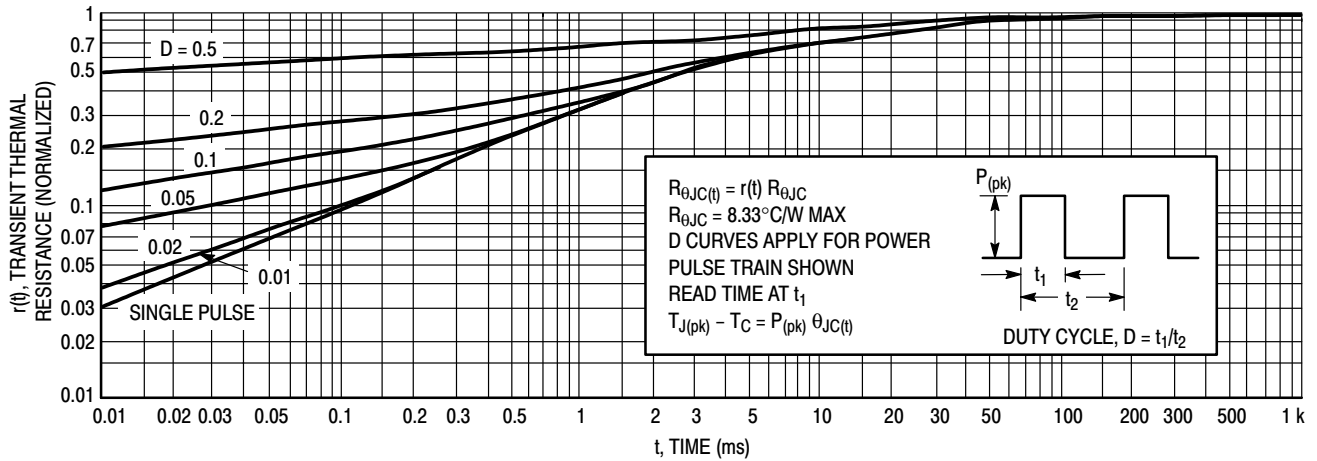
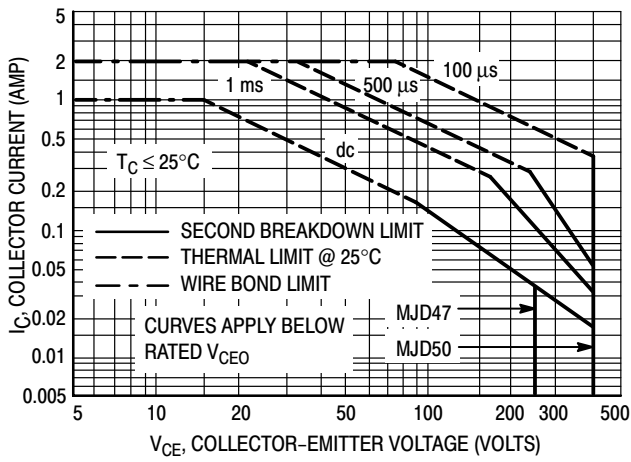


Figure 5. Thermal Response

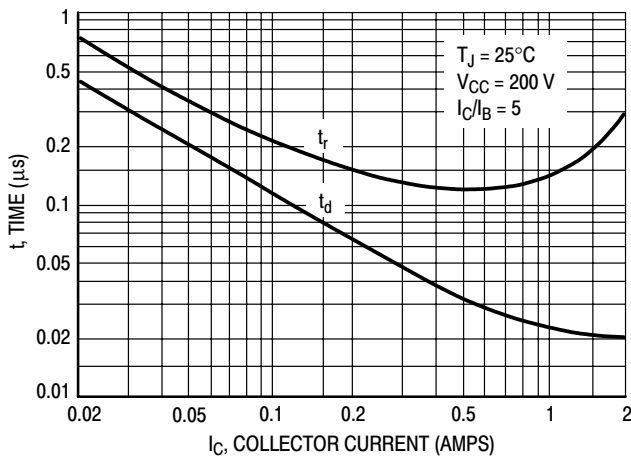
# MJD47 MJD50



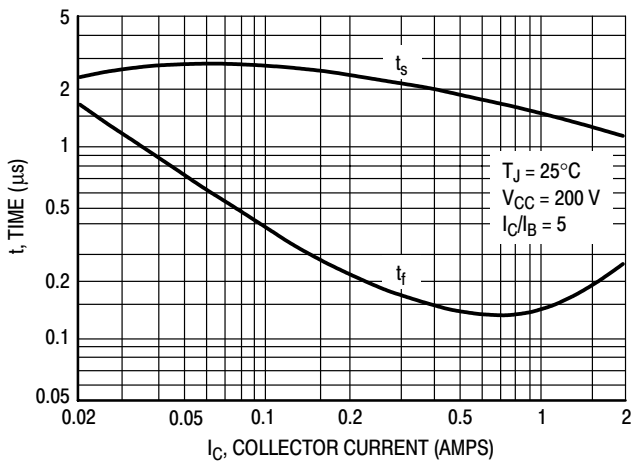
**Figure 6. Active Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 7. Turn-On Time**



**Figure 8. Turn-Off Time**



# Complementary Darlington Power Transistors

## DPAK For Surface Mount Applications

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Available on 16 mm Tape and Reel for Automatic Handling (“T4” Suffix)
- Surface Mount Replacements for 2N6034–2N6039 Series
- Monolithic Construction With Built-in Base–Emitter Shunt Resistors
- High DC Current Gain —  
 $h_{FE} = 2500$  (Typ) @  $I_C = 4.0$  Adc
- Complementary Pairs Simplifies Designs

### MAXIMUM RATINGS

Rating	Symbol	MJD6036 MJD6039	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Collector–Base Voltage	$V_{CB}$	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
Collector Current — Continuous Peak	$I_C$	4 8	Adc
Base Current	$I_B$	100	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	Watts W/ $^\circ\text{C}$
Total Power Dissipation (1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

(1) These ratings are applicable when surface mounted on the minimum pad sizes recommended.

### THERMAL CHARACTERISTICS

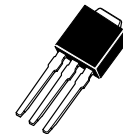
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	$^\circ\text{C}/\text{W}$

**NPN**  
**MJD6036**  
**PNP**  
**MJD6039**

**SILICON**  
**POWER TRANSISTORS**  
**4 AMPERES**  
**80 VOLTS**  
**20 WATTS**

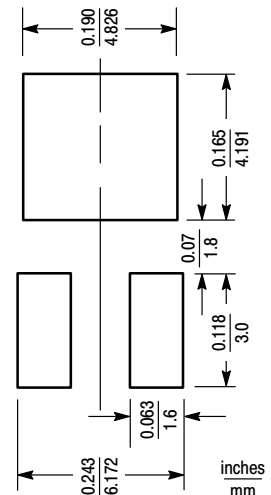


CASE 369A-13



CASE 369-07

### MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



# MJD6036 MJD6039

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**\*ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	80	—	Vdc
Collector–Cutoff Current ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	10	$\mu\text{Adc}$

**ON CHARACTERISTICS (1)**

DC Current Gain ( $I_C = 1\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 2\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$h_{FE}$	1000 500	— —	—
Collector–Emitter Saturation Voltage ( $I_C = 2\text{ Adc}$ , $I_B = 8\text{ mAdc}$ )	$V_{CE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage ( $I_C = 2\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$V_{BE(on)}$	—	2.8	Vdc

**DYNAMIC CHARACTERISTICS**

Small–Signal Current Gain ( $I_C = 0.75\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ kHz}$ )	$h_{fe}$	25	—	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	— —	200 100	pF
		MJD6036 MJD6039		

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

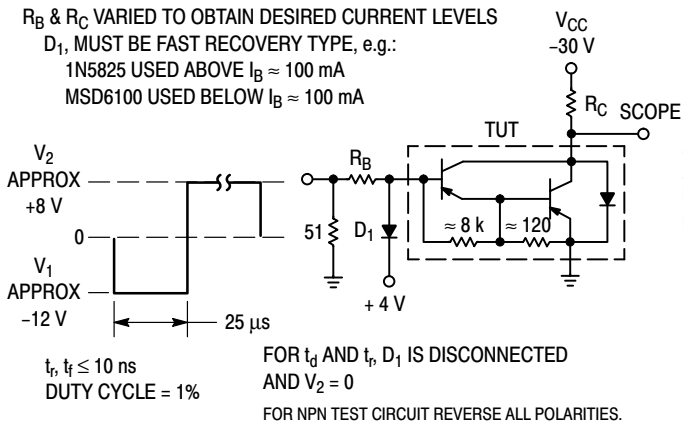


Figure 9. Switching Times Test Circuit

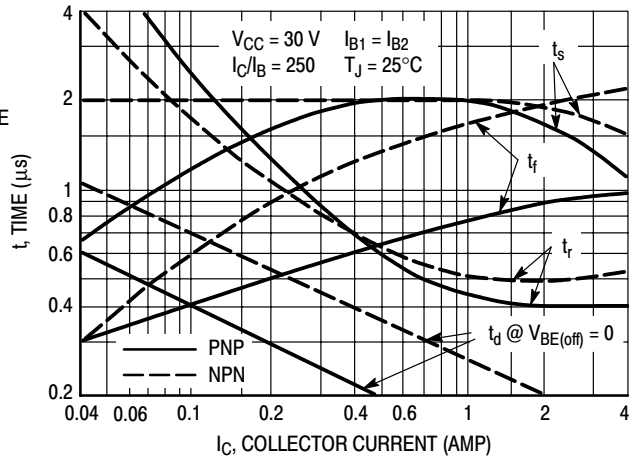


Figure 10. Switching Times

TYPICAL ELECTRICAL CHARACTERISTICS

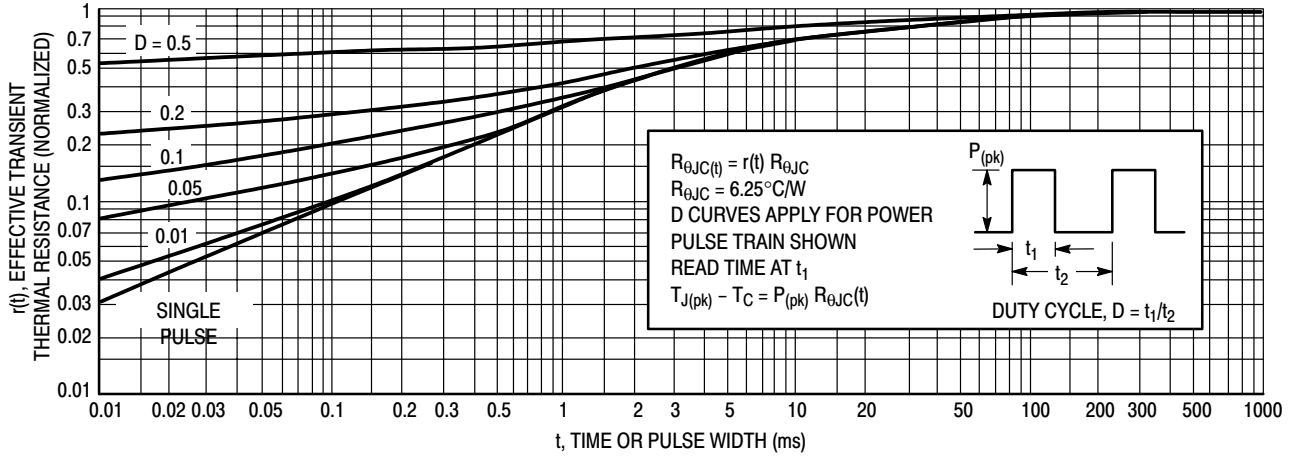


Figure 11. Thermal Response

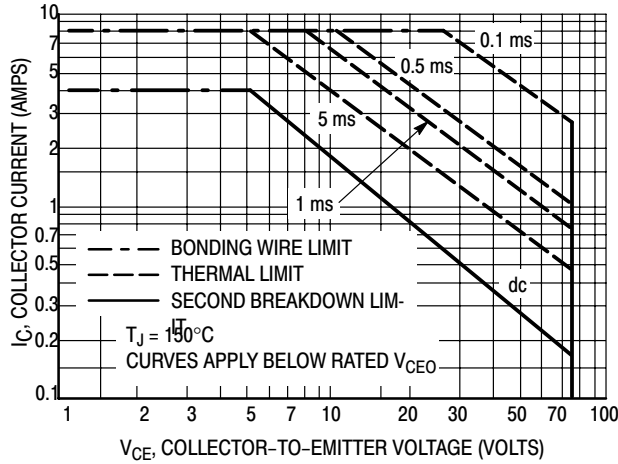


Figure 12. Maximum Rated Forward Biased Safe Operating Area

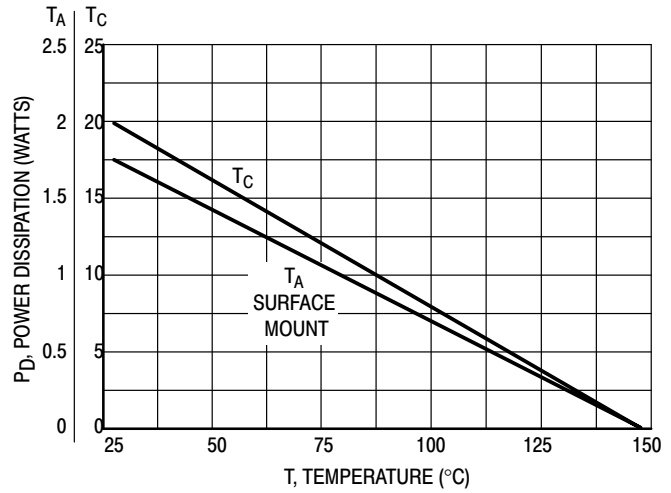


Figure 13. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 14 and 15 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

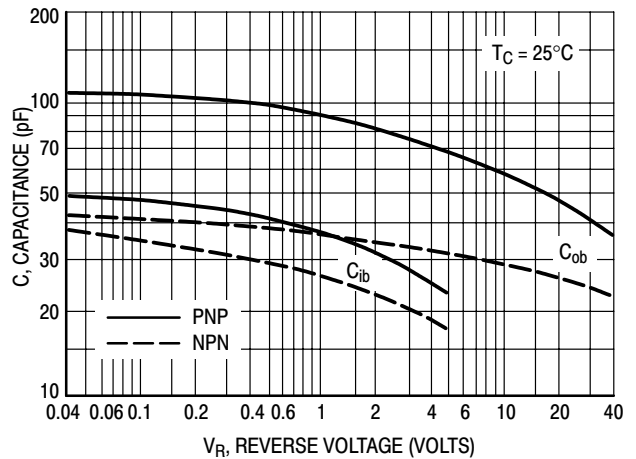
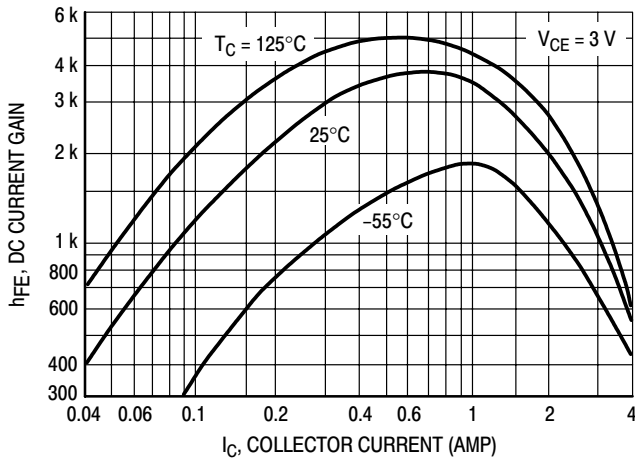


Figure 14. Capacitance

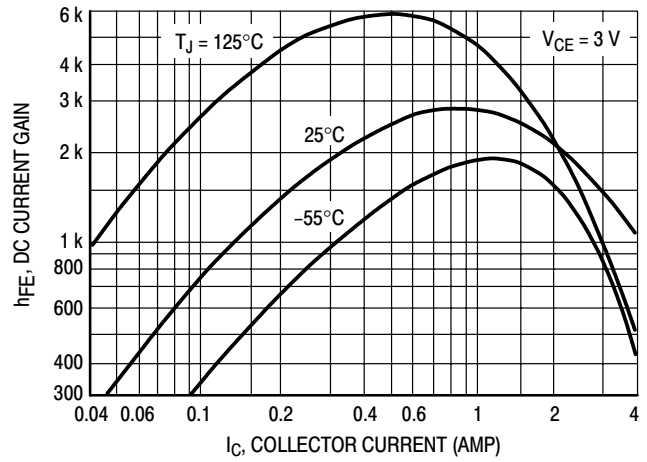
# MJD6036 MJD6039

## TYPICAL ELECTRICAL CHARACTERISTICS

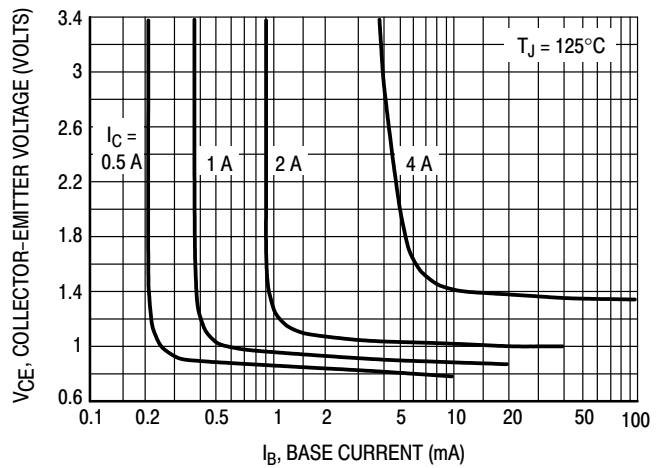
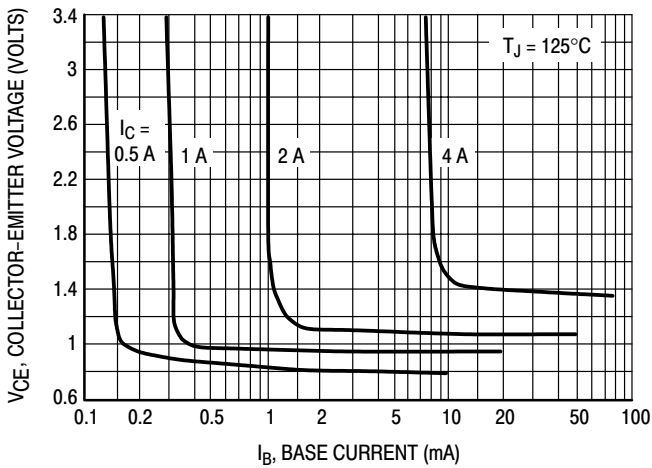
**PNP MJD6036**



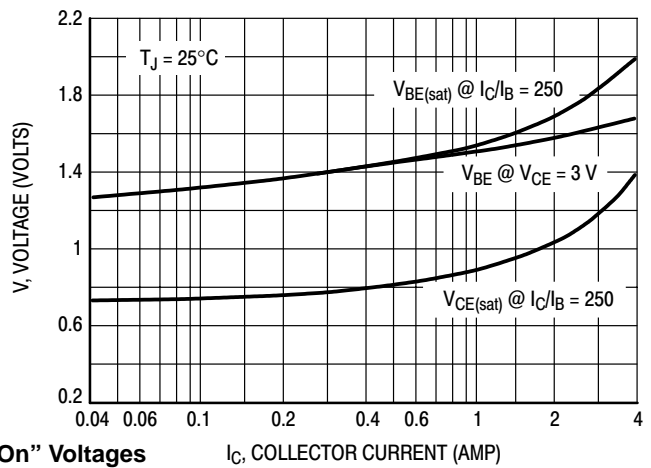
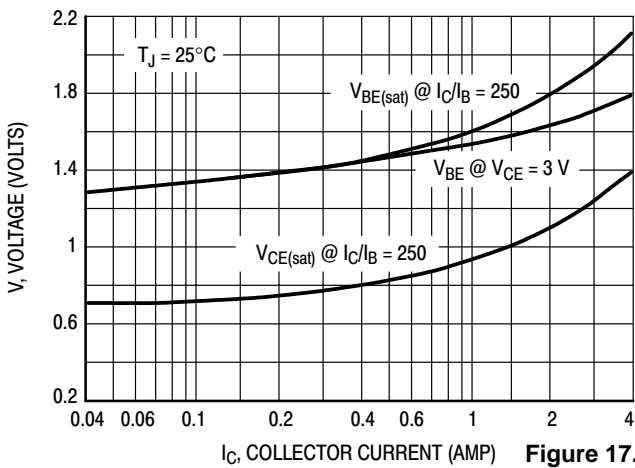
**NPN MJD6039**



**Figure 15. DC Current Gain**



**Figure 16. Collector Saturation Region**



**Figure 17. "On" Voltages**

# MJD6036 MJD6039

PNP MJD6036

NPN MJD6039

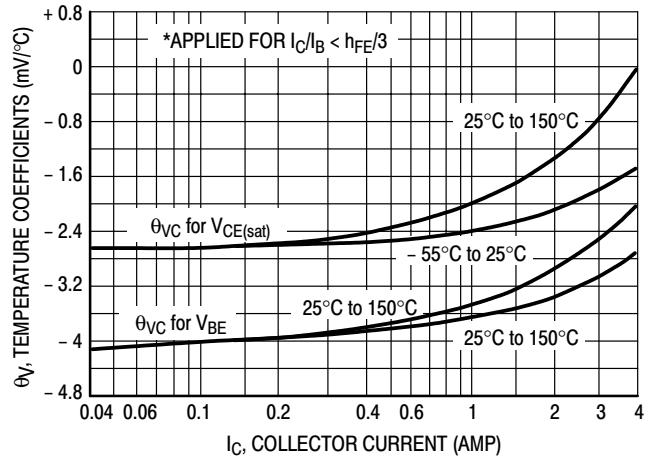
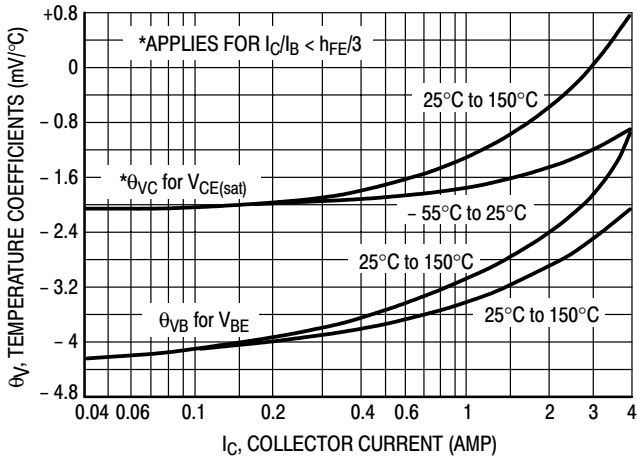


Figure 18. Temperature Coefficients

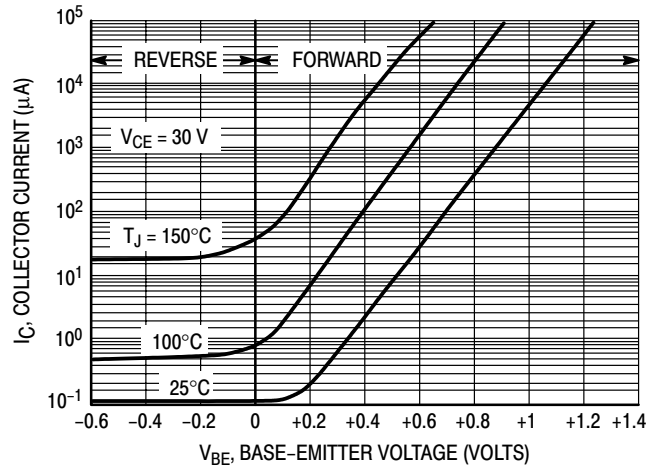
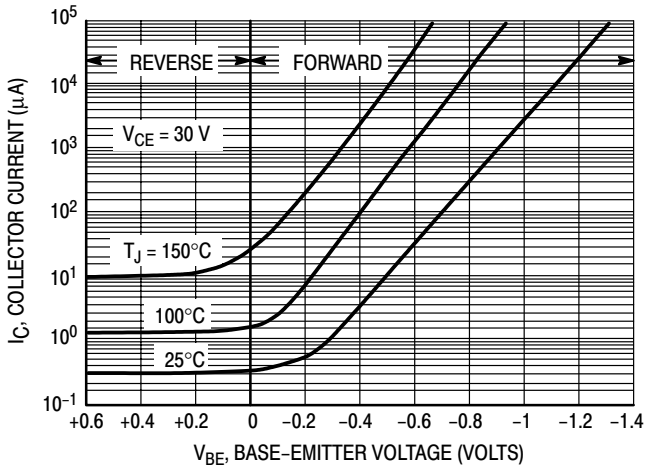


Figure 19. Collector Cut-Off Region

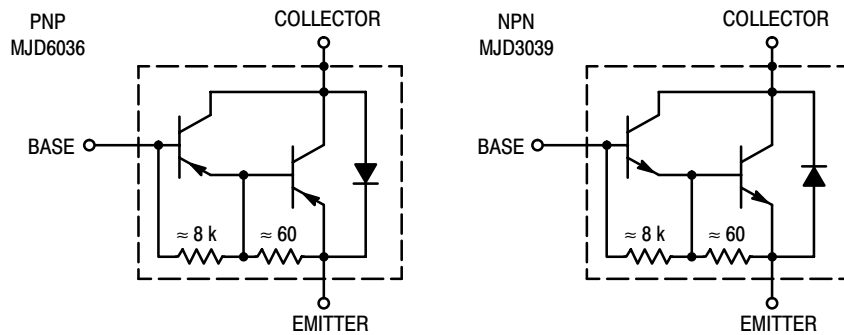


Figure 20. Darlington Schematic

# MJE13003

## SWITCHMODE™ Series NPN Silicon Power Transistor

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

### SPECIFICATION FEATURES:

- Reverse Biased SOA with Inductive Loads @  $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and  $100^\circ\text{C}$   
 $t_c$  @ 1 A,  $100^\circ\text{C}$  is 290 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	$V_{CEV}$	700	Vdc
Emitter Base Voltage	$V_{EBO}$	9	Vdc
Collector Current – Continuous – Peak (Note 1.)	$I_C$ $I_{CM}$	1.5 3	Adc
Base Current – Continuous – Peak (Note 1.)	$I_B$ $I_{BM}$	0.75 1.5	Adc
Emitter Current – Continuous – Peak (Note 1.)	$I_E$ $I_{EM}$	2.25 4.5	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.4 11.2	Watts mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 320	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	89	$^\circ\text{C/W}$
Maximum Load Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	$^\circ\text{C}$

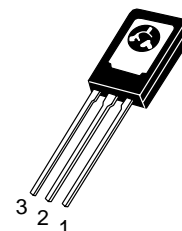
1. Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq 10\%$ .



ON Semiconductor™

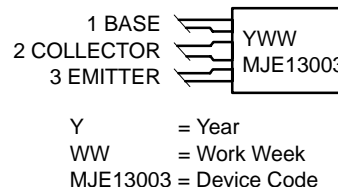
<http://onsemi.com>

**1.5 AMPERES  
NPN SILICON POWER  
TRANSISTORS  
300 AND 400 VOLTS  
40 WATTS**



TO-225  
CASE 77  
STYLE 3

### MARKING DIAGRAM



### ORDERING INFORMATION

Device	Package	Shipping
MJE13003	TO-225	500 Units/Box

# MJE13003

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS (Note 5..)

Collector–Emitter Sustaining Voltage ( $I_C = 10\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 100^\circ\text{C}$ )	$I_{CEV}$	–	–	1 5	mAdc
Emitter Cutoff Current ( $V_{EB} = 9\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	–	1	mAdc

### SECOND BREAKDOWN

Second Breakdown Collector Current with bass forward biased	$I_{S/b}$	See Figure 11			
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 12			

### ON CHARACTERISTICS (Note 5..)

DC Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 2\text{ Vdc}$ ) ( $I_C = 1\text{ Adc}$ , $V_{CE} = 2\text{ Vdc}$ )	$h_{FE}$	8 5	– –	40 25	–
Collector–Emitter Saturation Voltage ( $I_C = 0.5\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ ) ( $I_C = 1\text{ Adc}$ , $I_B = 0.25\text{ Adc}$ ) ( $I_C = 1.5\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ ) ( $I_C = 1\text{ Adc}$ , $I_B = 0.25\text{ Adc}$ , $T_C = 100^\circ\text{C}$ )	$V_{CE(sat)}$	– – – –	– – – –	0.5 1 3 1	Vdc
Base–Emitter Saturation Voltage ( $I_C = 0.5\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ ) ( $I_C = 1\text{ Adc}$ , $I_B = 0.25\text{ Adc}$ ) ( $I_C = 1\text{ Adc}$ , $I_B = 0.25\text{ Adc}$ , $T_C = 100^\circ\text{C}$ )	$V_{BE(sat)}$	– – –	– – –	1 1.2 1.1	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product ( $I_C = 100\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$f_T$	4	10	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	–	21	–	pF

### SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 125\text{ Vdc}$ , $I_C = 1\text{ A}$ , $I_{B1} = I_{B2} = 0.2\text{ A}$ , $t_p = 25\text{ }\mu\text{s}$ , Duty Cycle $\leq 1\%$ )	$t_d$	–	0.05	0.1	$\mu\text{s}$
Rise Time		$t_r$	–	0.5	1	$\mu\text{s}$
Storage Time		$t_s$	–	2	4	$\mu\text{s}$
Fall Time		$t_f$	–	0.4	0.7	$\mu\text{s}$
Inductive Load, Clamped (Table 1, Figure 13)						
Storage Time	$(I_C = 1\text{ A}$ , $V_{clamp} = 300\text{ Vdc}$ , $I_{B1} = 0.2\text{ A}$ , $V_{BE(off)} = 5\text{ Vdc}$ , $T_C = 100^\circ\text{C}$ )	$t_{sv}$	–	1.7	4	$\mu\text{s}$
Crossover Time		$t_c$	–	0.29	0.75	$\mu\text{s}$
Fall Time		$t_{fi}$	–	0.15	–	$\mu\text{s}$

5. Pulse Test:  $PW = 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

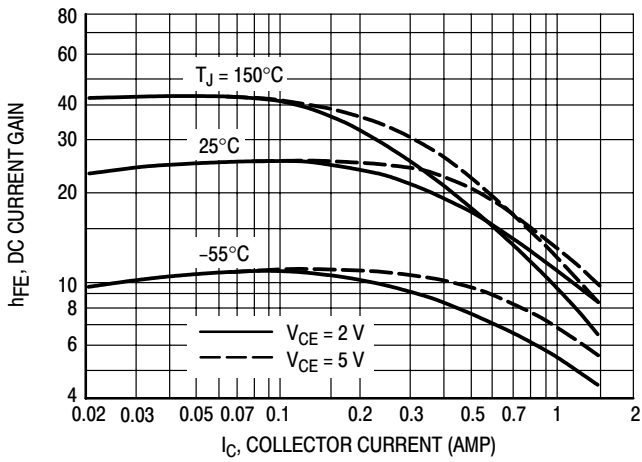


Figure 1. DC Current Gain

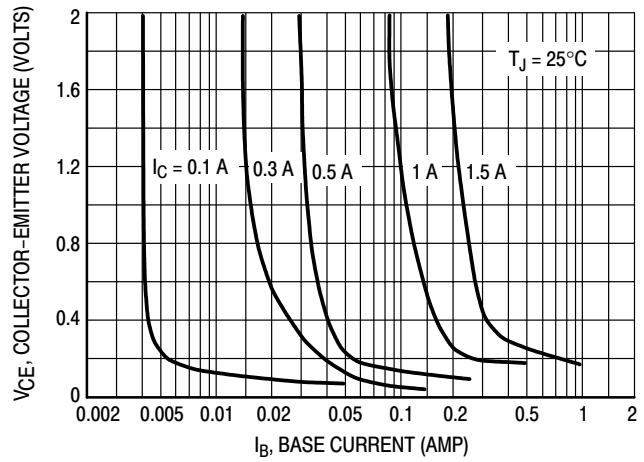


Figure 2. Collector Saturation Region

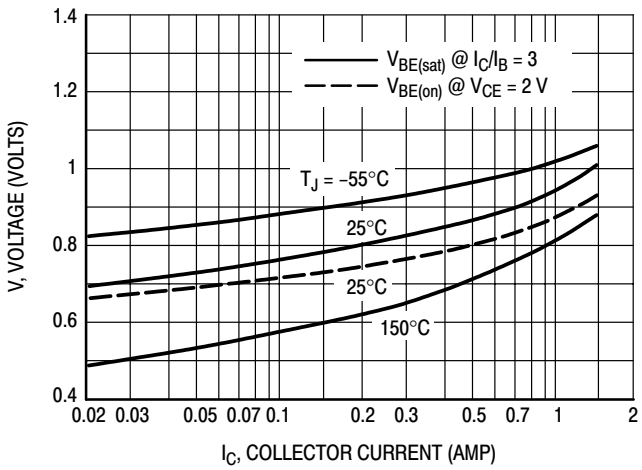


Figure 3. Base-Emitter Voltage

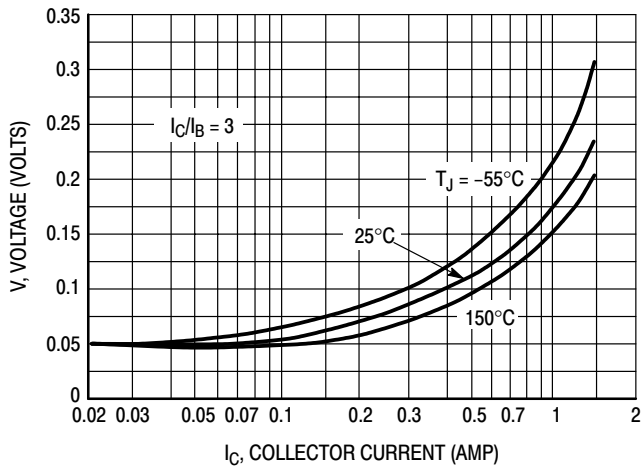


Figure 4. Collector-Emitter Saturation Region

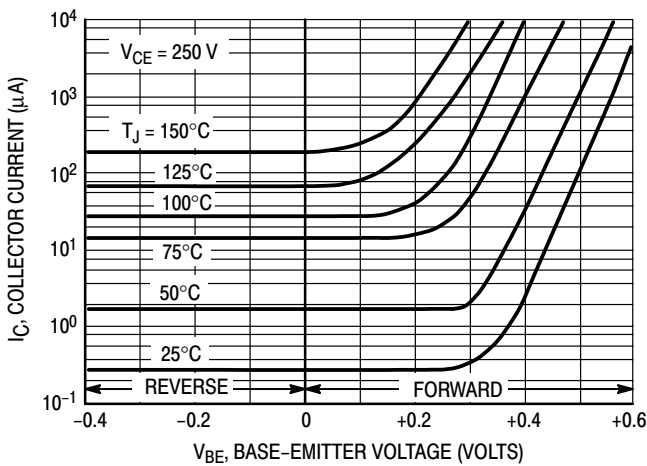


Figure 5. Collector Cutoff Region

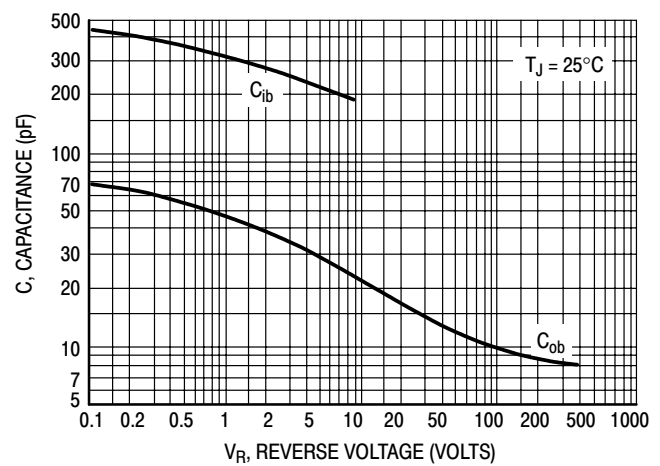


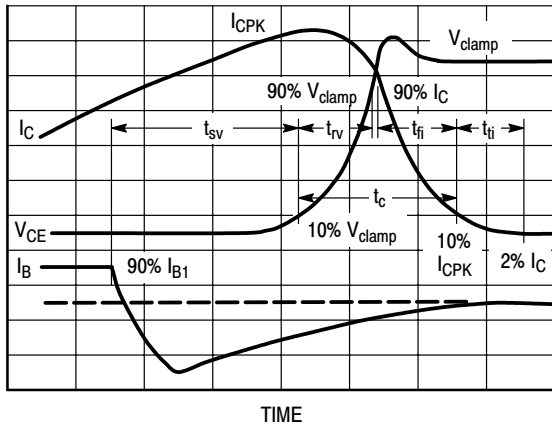
Figure 6. Capacitance



# MJE13003

Table 1. Test Conditions for Dynamic Performance

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
TEST CIRCUITS	<p>DUTY CYCLE <math>\leq 10\%</math>  <math>t_r, t_f \leq 10 \text{ ns}</math></p> <p>NOTE  PW and <math>V_{CC}</math> Adjusted for Desired <math>I_C</math>  <math>R_B</math> Adjusted for Desired <math>I_{B1}</math></p>	<p>*SELECTED FOR <math>\geq 1 \text{ kV}</math></p>
CIRCUIT VALUES	<p>Coil Data:  Ferroxcube Core #6656  Full Bobbin (~200 Turns) #20</p> <p>GAP for 30 mH/2 A  <math>L_{\text{coil}} = 50 \text{ mH}</math></p> <p><math>V_{CC} = 20 \text{ V}</math>  <math>V_{\text{clamp}} = 300 \text{ Vdc}</math></p>	<p><math>V_{CC} = 125 \text{ V}</math>  <math>R_C = 125 \Omega</math>  <math>D1 = 1N5820 \text{ or Equiv.}</math>  <math>R_B = 47 \Omega</math></p>
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p><math>t_1</math> Adjusted to Obtain <math>I_C</math></p> $t_1 \approx \frac{L_{\text{coil}} (I_{C_{pk}})}{V_{CC}}$ <p>Test Equipment  Scope—Tektronics 475 or Equivalent</p> $t_2 \approx \frac{L_{\text{coil}} (I_{C_{pk}})}{V_{\text{clamp}}}$	<p><math>t_r, t_f &lt; 10 \text{ ns}</math>  Duty Cycle = 1.0%  <math>R_B</math> and <math>R_C</math> adjusted for desired <math>I_B</math> and <math>I_C</math></p>



**Figure 7. Inductive Switching Measurements**

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

**Table 2. Typical Inductive Switching Performance**

I <sub>C</sub> AMP	T <sub>C</sub> °C	t <sub>sv</sub> μs	t <sub>rv</sub> μs	t <sub>fi</sub> μs	t <sub>ti</sub> μs	t <sub>c</sub> μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

**SWITCHING TIMES NOTE**

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t<sub>sv</sub> = Voltage Storage Time, 90% I<sub>B1</sub> to 10% V<sub>clamp</sub>
- t<sub>rv</sub> = Voltage Rise Time, 10–90% V<sub>clamp</sub>
- t<sub>fi</sub> = Current Fall Time, 90–10% I<sub>C</sub>
- t<sub>ti</sub> = Current Tail, 10–2% I<sub>C</sub>
- t<sub>c</sub> = Crossover Time, 10% V<sub>clamp</sub> to 10% I<sub>C</sub>

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2 V_{CC}I_C(t_c)f$$

In general, t<sub>rv</sub> + t<sub>fi</sub> ≈ t<sub>c</sub>. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t<sub>c</sub> and t<sub>sv</sub>) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

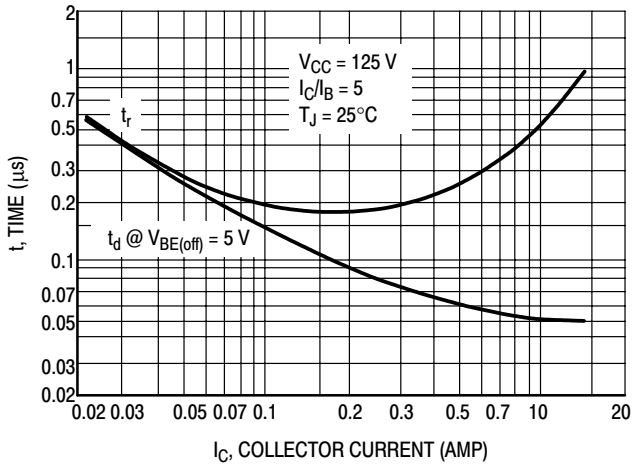


Figure 8. Turn-On Time

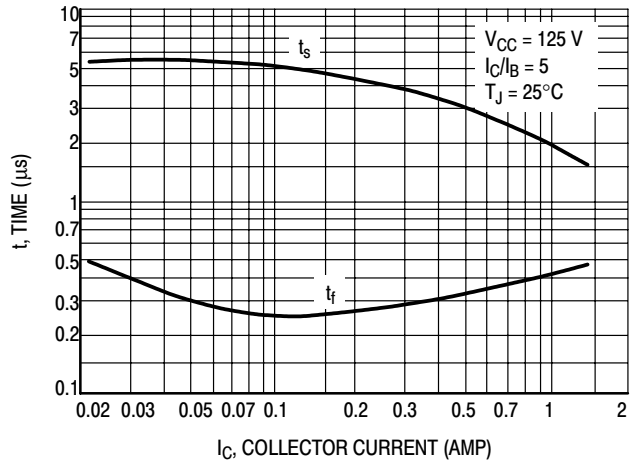


Figure 9. Turn-Off Time

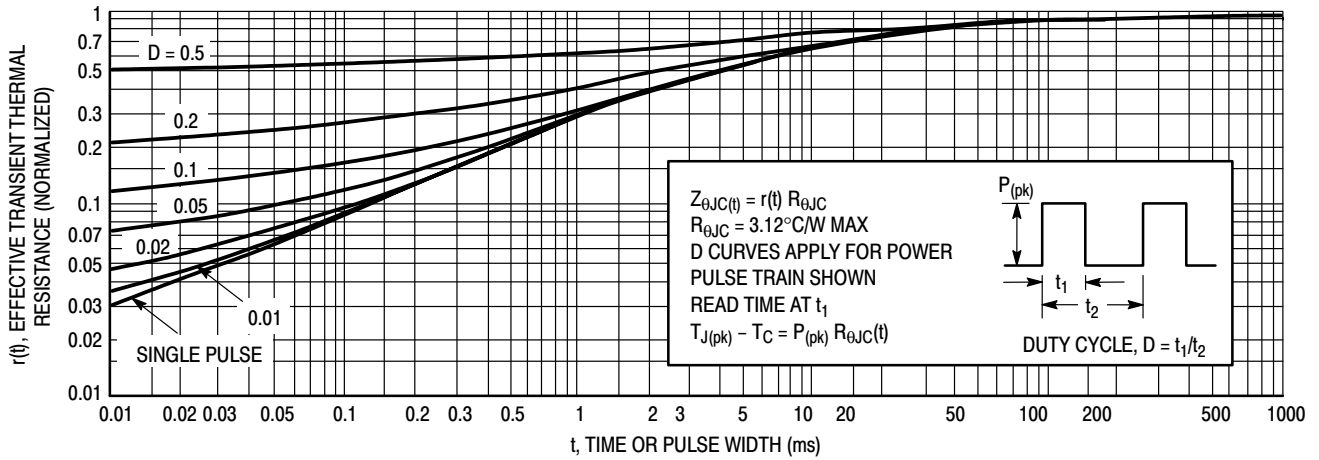


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

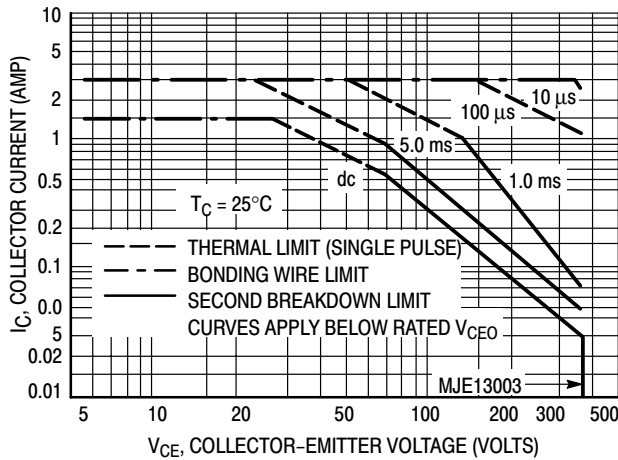


Figure 11. Active Region Safe Operating Area

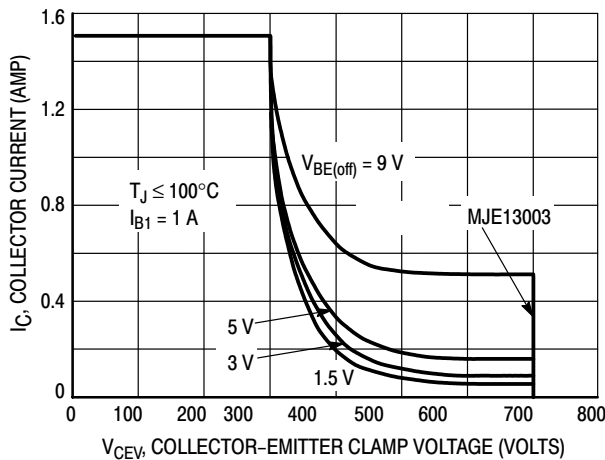


Figure 12. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$  may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

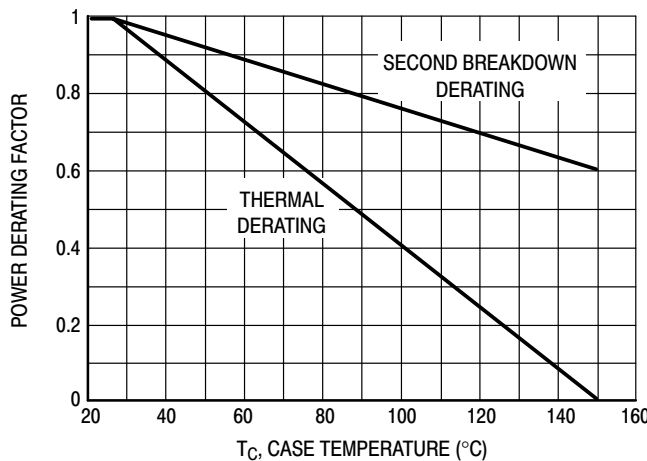


Figure 13. Forward Bias Power Derating

## SWITCHMODE™ Series NPN Silicon Power Transistors

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulator's, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

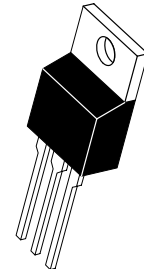
### SPECIFICATION FEATURES:

- $V_{CEO(sus)}$  400 V
- Reverse Bias SOA with Inductive Loads @  $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 2 to 4 Amp, 25 and  $100^\circ\text{C}$   
 $t_c$  @ 3A,  $100^\circ\text{C}$  is 180 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information.

# MJE13005\*

\*ON Semiconductor Preferred Device

**4 AMPERE  
NPN SILICON  
POWER TRANSISTOR  
400 VOLTS  
75 WATTS**



**CASE 221A-09  
TO-220AB**

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	$V_{CEV}$	700	Vdc
Emitter Base Voltage	$V_{EBO}$	9	Vdc
Collector Current — Continuous — Peak (1)	$I_C$ $I_{CM}$	4 8	Adc
Base Current — Continuous — Peak (1)	$I_B$ $I_{BM}$	2 4	Adc
Emitter Current — Continuous — Peak (1)	$I_E$ $I_{EM}$	6 12	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2 16	Watts mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	75 600	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq$  10%.

# MJE13005

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>*OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 10\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 100^\circ\text{C}$ )	$I_{CEV}$	—	—	1 5	mAdc
Emitter Cutoff Current ( $V_{EB} = 9\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	1	mAdc

## SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$			See Figure 11	
Clamped Inductive SOA with Base Reverse Biased	RBSOA			See Figure 12	

## \*ON CHARACTERISTICS

DC Current Gain ( $I_C = 1\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 2\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$h_{FE}$	10 8	— —	60 40	—
Collector–Emitter Saturation Voltage ( $I_C = 1\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ ) ( $I_C = 2\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ ) ( $I_C = 4\text{ Adc}$ , $I_B = 1\text{ Adc}$ ) ( $I_C = 2\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ , $T_C = 100^\circ\text{C}$ )	$V_{CE(sat)}$	— — — —	— — — —	0.5 0.6 1 1	Vdc
Base–Emitter Saturation Voltage ( $I_C = 1\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ ) ( $I_C = 2\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ ) ( $I_C = 2\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ , $T_C = 100^\circ\text{C}$ )	$V_{BE(sat)}$	— — —	— — —	1.2 1.6 1.5	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$f_T$	4	—	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	—	65	—	pF

## SWITCHING CHARACTERISTICS

Resistive Load (Table 2)						
Delay Time	$(V_{CC} = 125\text{ Vdc}$ , $I_C = 2\text{ A}$ , $I_{B1} = I_{B2} = 0.4\text{ A}$ , $t_p = 25\text{ }\mu\text{s}$ , Duty Cycle $\leq 1\%$ )	$t_d$	—	0.025	0.1	$\mu\text{s}$
Rise Time		$t_r$	—	0.3	0.7	$\mu\text{s}$
Storage Time		$t_s$	—	1.7	4	$\mu\text{s}$
Fall Time		$t_f$	—	0.4	0.9	$\mu\text{s}$
Inductive Load, Clamped (Table 2, Figure 13)						
Voltage Storage Time	$(I_C = 2\text{ A}$ , $V_{clamp} = 300\text{ Vdc}$ , $I_{B1} = 0.4\text{ A}$ , $V_{BE(off)} = 5\text{ Vdc}$ , $T_C = 100^\circ\text{C}$ )	$t_{sv}$	—	0.9	4	$\mu\text{s}$
Crossover Time		$t_c$	—	0.32	0.9	$\mu\text{s}$
Fall Time		$t_{fi}$	—	0.16	—	$\mu\text{s}$

\*Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 2%.

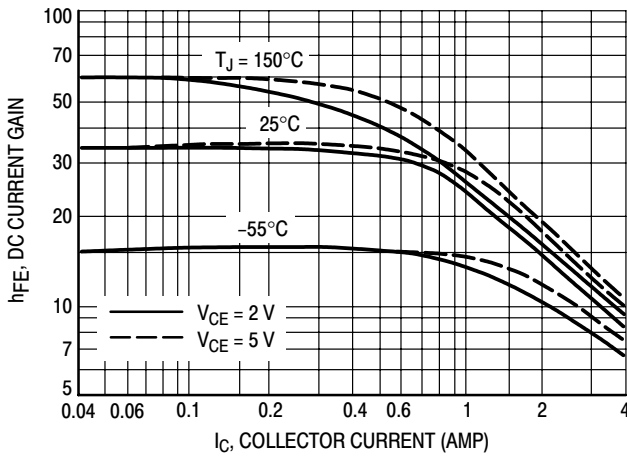


Figure 1. DC Current Gain

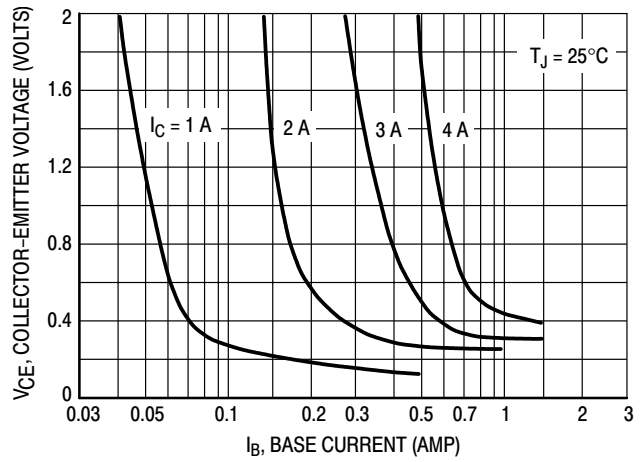


Figure 2. Collector Saturation Region

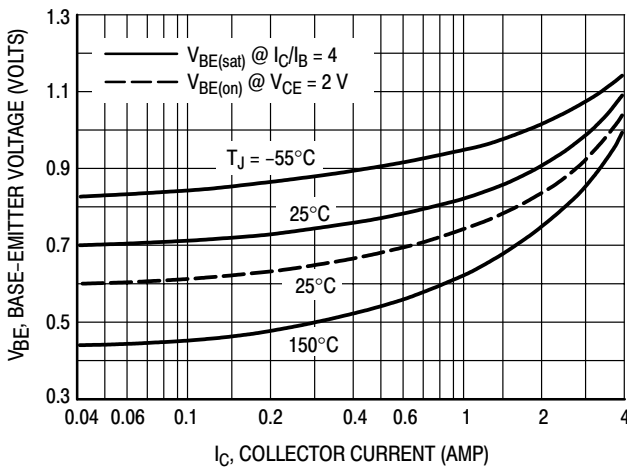


Figure 3. Base-Emitter Voltage

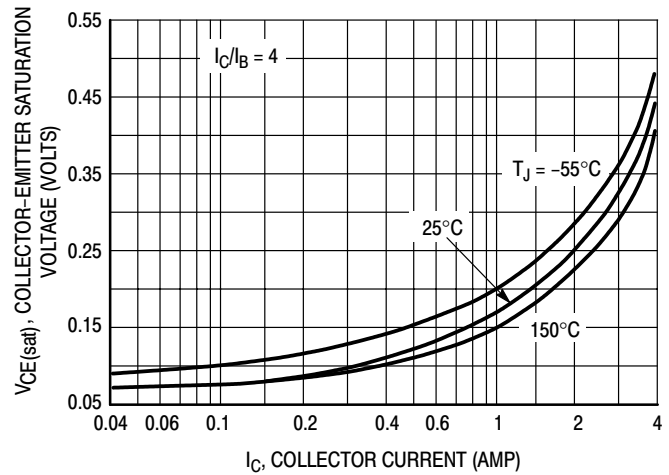


Figure 4. Collector-Emitter Saturation Voltage

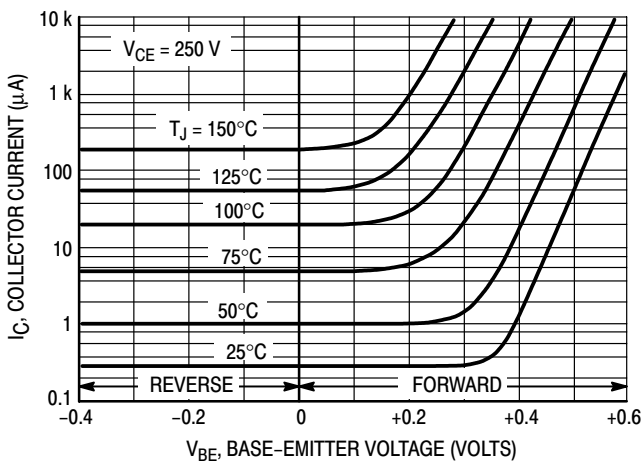


Figure 5. Collector Cutoff Region

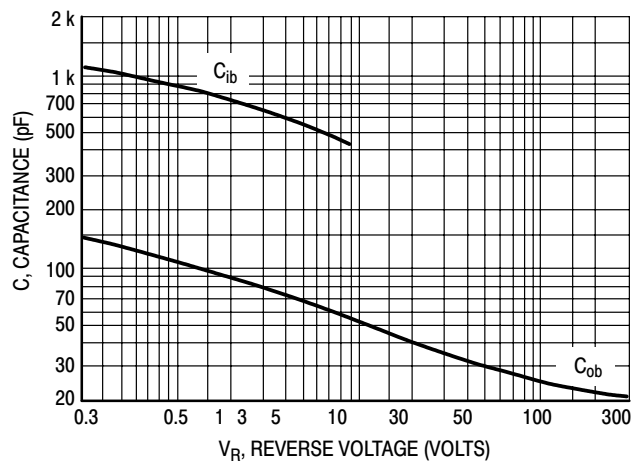


Figure 6. Capacitance

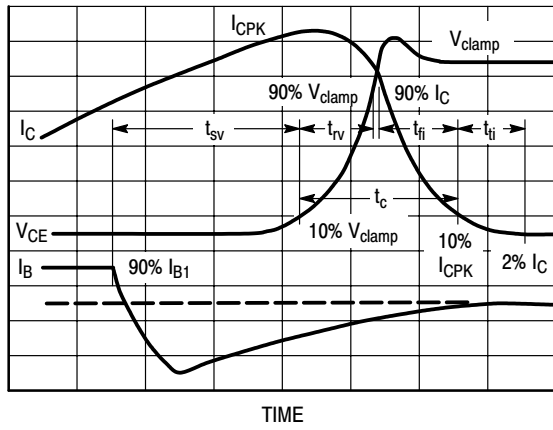


Figure 7. Inductive Switching Measurements

Table 1. Typical Inductive Switching Performance

I <sub>C</sub> AMP	T <sub>C</sub> °C	t <sub>sv</sub> ns	t <sub>rv</sub> ns	t <sub>fi</sub> ns	t <sub>ti</sub> ns	t <sub>c</sub> ns
2	25	600	70	100	80	180
	100	900	110	240	130	320
3	25	650	60	140	60	200
	100	950	100	330	100	350
4	25	550	70	160	100	220
	100	850	110	350	160	390

NOTE: All Data recorded in the inductive Switching Circuit In Table 2.

**SWITCHING TIMES NOTE**

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t<sub>sv</sub> = Voltage Storage Time, 90% I<sub>B1</sub> to 10% V<sub>clamp</sub>
- t<sub>rv</sub> = Voltage Rise Time, 10–90% V<sub>clamp</sub>
- t<sub>fi</sub> = Current Fall Time, 90–10% I<sub>C</sub>
- t<sub>ti</sub> = Current Tail, 10–2% I<sub>C</sub>
- t<sub>c</sub> = Crossover Time, 10% V<sub>clamp</sub> to 10% I<sub>C</sub>

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, t<sub>rv</sub> + t<sub>fi</sub> ≈ t<sub>c</sub>. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t<sub>c</sub> and t<sub>sv</sub>) which are guaranteed at 100°C.

**RESISTIVE SWITCHING PERFORMANCE**

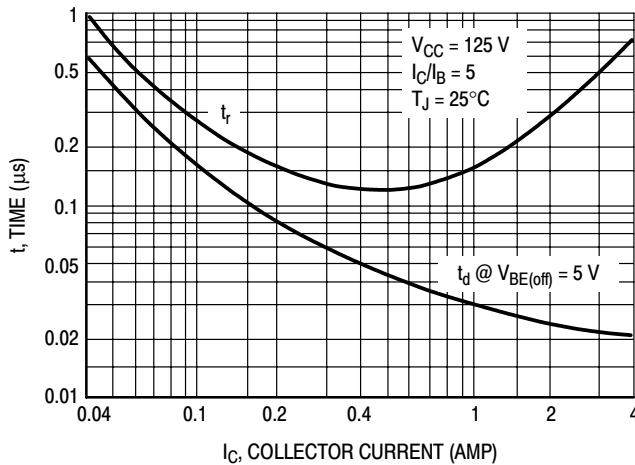


Figure 8. Turn-On Time

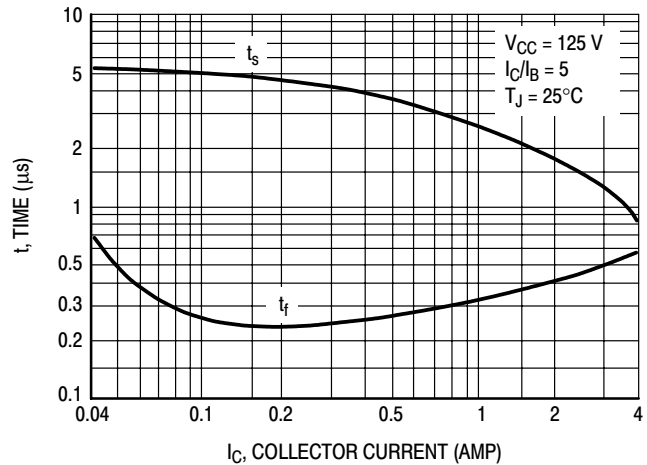


Figure 9. Turn-Off Time



# MJE13005

Table 2. Test Conditions for Dynamic Performance

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
TEST CIRCUITS	<p>DUTY CYCLE <math>\leq 10\%</math>  <math>t_p, t_f \leq 10</math> ns</p> <p>NOTE            PW and <math>V_{CC}</math> Adjusted for Desired <math>I_C</math>  <math>R_B</math> Adjusted for Desired <math>I_{B1}</math></p>	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 $\mu$ H/20 A $L_{coil} = 200 \mu$ H $V_{CC} = 20$ V $V_{clamp} = 300$ Vdc	$V_{CC} = 125$ V $R_C = 62 \Omega$ $D1 = 1N5820$ or Equiv. $R_B = 22 \Omega$
TEST WAVEFORMS	<p> <math>t_1</math> ADJUSTED TO OBTAIN <math>I_C</math>  <math>t_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}</math>  <math>t_2 \approx \frac{L_{coil} (I_{Cpk})}{V_{clamp}}</math> </p> <p>Test Equipment            Scope—Tektronics            475 or Equivalent</p>	<p> <math>t_p, t_f &lt; 10</math> ns            Duty Cycle = 1.0%  <math>R_B</math> and <math>R_C</math> adjusted for desired <math>I_B</math> and <math>I_C</math> </p>

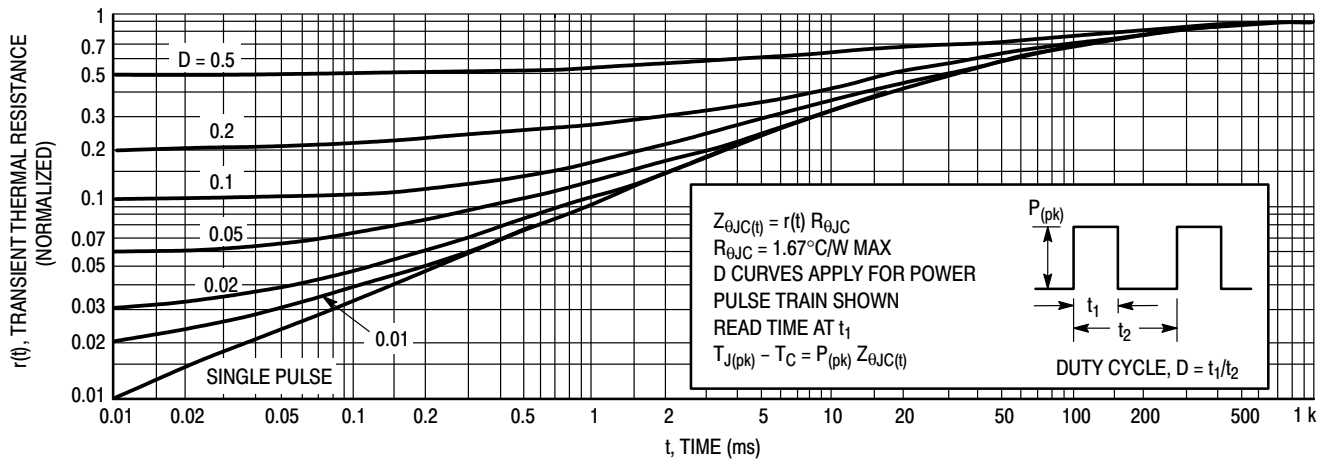


Figure 10. Typical Thermal Response [ $Z_{\theta JC}(t)$ ]

SAFE OPERATING AREA INFORMATION

The Safe Operating Area Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

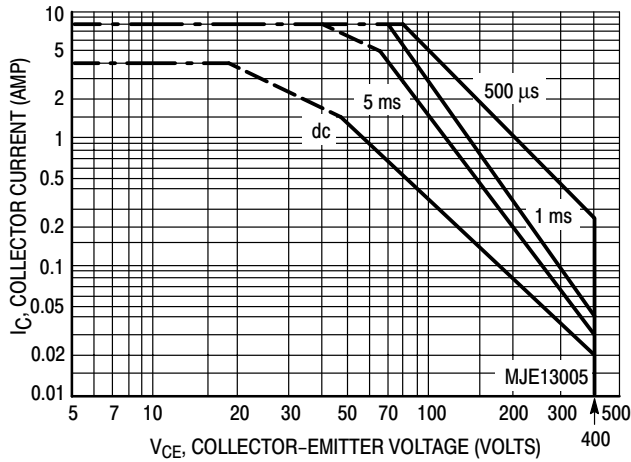


Figure 11. Forward Bias Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$  may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

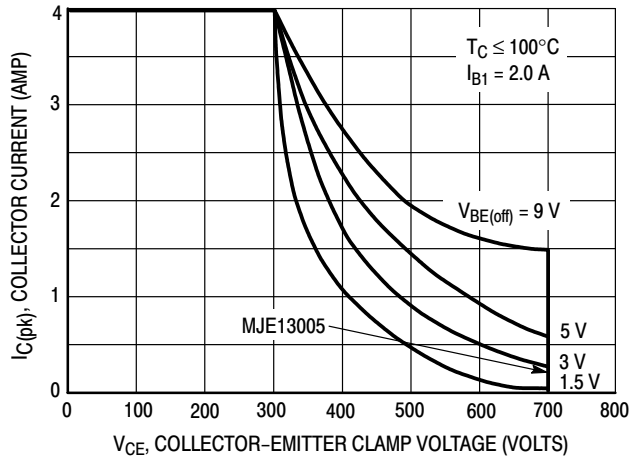


Figure 12. Reverse Bias Switching Safe Operating Area

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

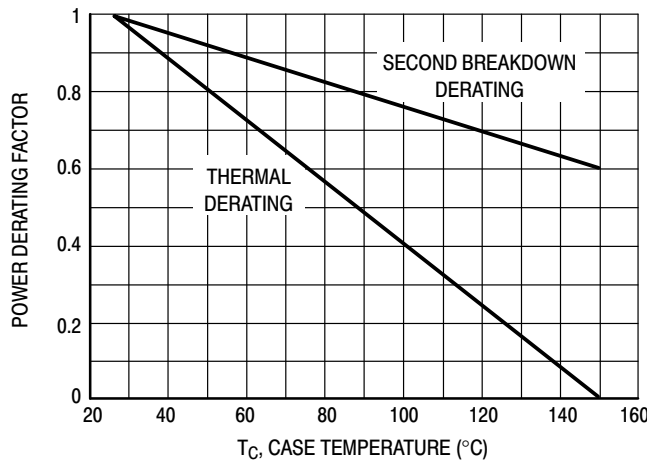


Figure 13. Forward Bias Power Derating

# SWITCHMODE™

## NPN Bipolar Power Transistor

### For Switching Power Supply Applications

The MJE13007 is designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V switchmode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

- $V_{CEO(sus)}$  400 V
- Reverse Bias SOA with Inductive Loads @  $T_C = 100^\circ\text{C}$
- 700 V Blocking Capability
- SOA and Switching Applications Information
- Standard TO-220

#### MAXIMUM RATINGS

Rating	Symbol	MJE13007	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	400	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	700	Vdc
Emitter-Base Voltage	$V_{EBO}$	9.0	Vdc
Collector Current — Continuous	$I_C$	8.0	Adc
— Peak (1)	$I_{CM}$	16	
Base Current — Continuous	$I_B$	4.0	Adc
— Peak (1)	$I_{BM}$	8.0	
Emitter Current — Continuous	$I_E$	12	Adc
— Peak (1)	$I_{EM}$	24	
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	80 0.64	Watts W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{stg}$	- 65 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

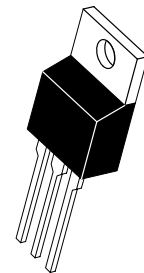
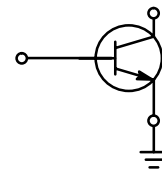
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.56 62.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	260	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle  $\leq 10\%$ .

\*Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink with thermal grease applied at a mounting torque of 6 to 8•lbs.

# MJE13007

**POWER TRANSISTOR**  
**8.0 AMPERES**  
**400 VOLTS**  
**80 WATTS**



**CASE 221A-09**  
**TO-220AB**  
**MJE13007**

# MJE13007

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>*OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	400	—	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 700 Vdc) (V <sub>CE</sub> = 700 Vdc, T <sub>C</sub> = 125°C)	I <sub>CES</sub>	— —	— —	0.1 1.0	mAdc
Emitter Cutoff Current (V <sub>EB</sub> = 9.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	—	100	μAdc

## SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I <sub>S/b</sub>	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased	—	See Figure 7			

## \*ON CHARACTERISTICS

DC Current Gain (I <sub>C</sub> = 2.0 Adc, V <sub>CE</sub> = 5.0 Vdc) (I <sub>C</sub> = 5.0 Adc, V <sub>CE</sub> = 5.0 Vdc)	h <sub>FE</sub>	8.0 5.0	— —	40 30	—
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 0.4 Adc) (I <sub>C</sub> = 5.0 Adc, I <sub>B</sub> = 1.0 Adc) (I <sub>C</sub> = 8.0 Adc, I <sub>B</sub> = 2.0 Adc) (I <sub>C</sub> = 5.0 Adc, I <sub>B</sub> = 1.0 Adc, T <sub>C</sub> = 100°C)	V <sub>CE(sat)</sub>	— — — —	— — — —	1.0 2.0 3.0 3.0	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 0.4 Adc) (I <sub>C</sub> = 5.0 Adc, I <sub>B</sub> = 1.0 Adc) (I <sub>C</sub> = 5.0 Adc, I <sub>B</sub> = 1.0 Adc, T <sub>C</sub> = 100°C)	V <sub>BE(sat)</sub>	— — —	— — —	1.2 1.6 1.5	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product (I <sub>C</sub> = 500 mAdc, V <sub>CE</sub> = 10 Vdc, f = 1.0 MHz)	f <sub>T</sub>	4.0	14	—	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	C <sub>ob</sub>	—	80	—	pF

## SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	(V <sub>CC</sub> = 125 Vdc, I <sub>C</sub> = 5.0 A, I <sub>B1</sub> = I <sub>B2</sub> = 1.0 A, t <sub>p</sub> = 25 μs, Duty Cycle ≤ 1.0%)	t <sub>d</sub>	—	0.025	0.1	μs	
Rise Time		t <sub>r</sub>	—	0.5	1.5		
Storage Time		t <sub>s</sub>	—	1.8	3.0		
Fall Time		t <sub>f</sub>	—	0.23	0.7		
Inductive Load, Clamped (Table 1)							
Voltage Storage Time	V <sub>CC</sub> = 15 Vdc, I <sub>C</sub> = 5.0 A V <sub>clamp</sub> = 300 Vdc	T <sub>C</sub> = 25°C T <sub>C</sub> = 100°C	t <sub>sv</sub>	— —	1.2 1.6	2.0 3.0	μs
Crossover Time	I <sub>B(on)</sub> = 1.0 A, I <sub>B(off)</sub> = 2.5 A L <sub>C</sub> = 200 μH	T <sub>C</sub> = 25°C T <sub>C</sub> = 100°C	t <sub>c</sub>	— —	0.15 0.21	0.30 0.50	μs
Fall Time		T <sub>C</sub> = 25°C T <sub>C</sub> = 100°C	t <sub>fi</sub>	— —	0.04 0.10	0.12 0.20	μs

\* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

# MJE13007

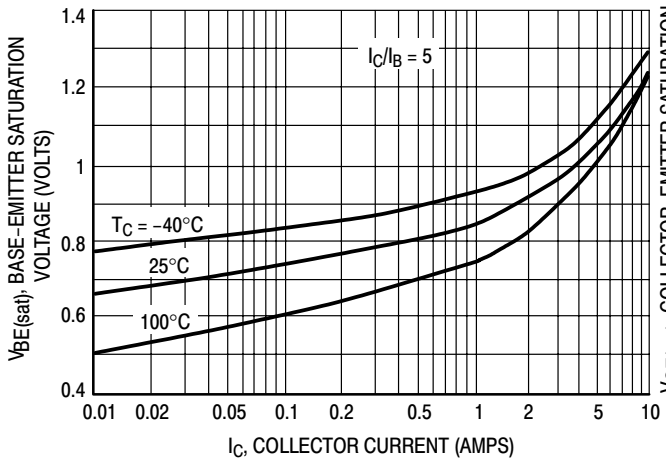


Figure 1. Base-Emitter Saturation Voltage

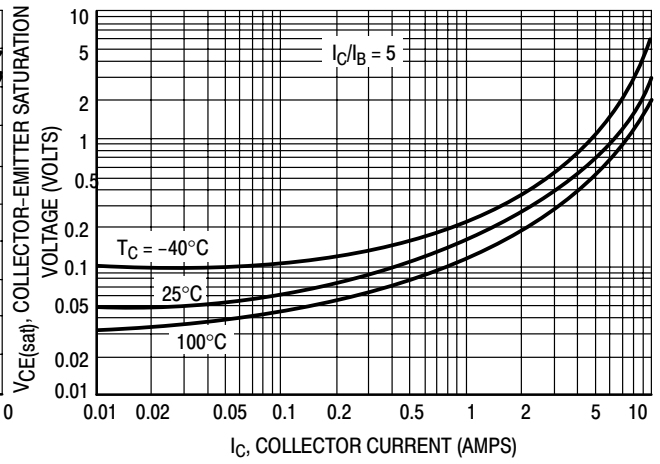


Figure 2. Collector-Emitter Saturation Voltage

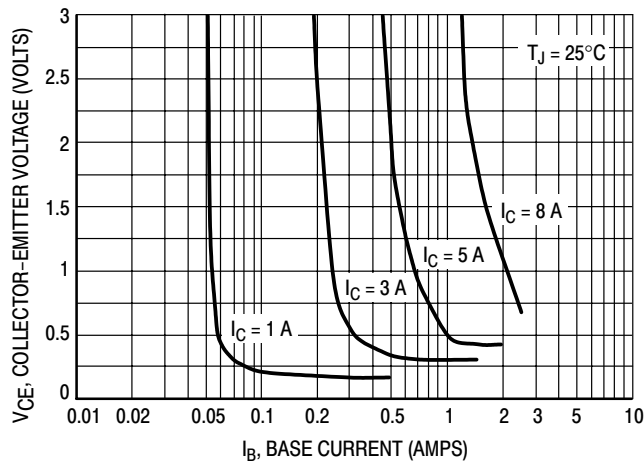


Figure 3. Collector Saturation Region

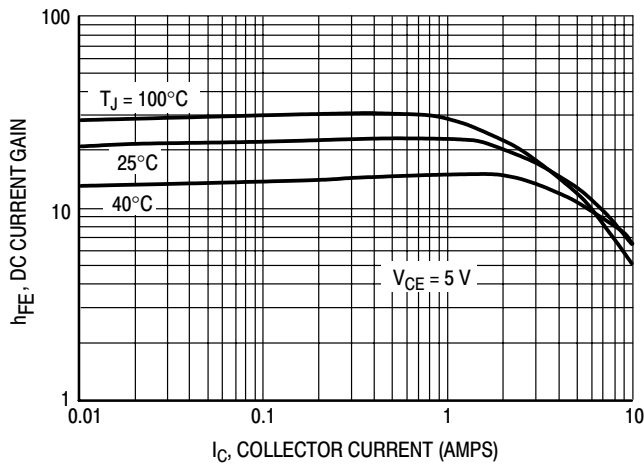


Figure 4. DC Current Gain

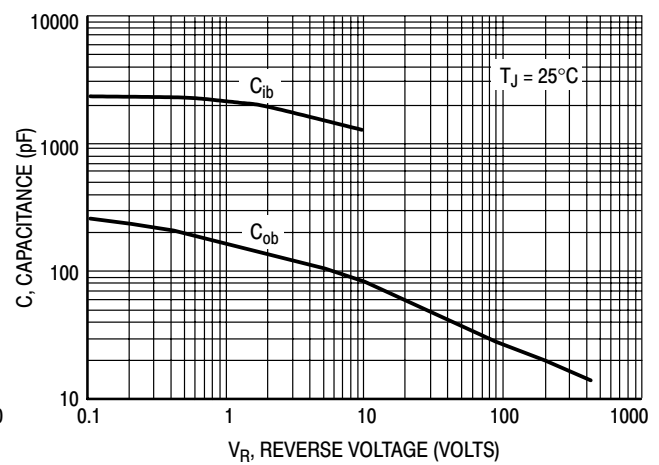


Figure 5. Capacitance

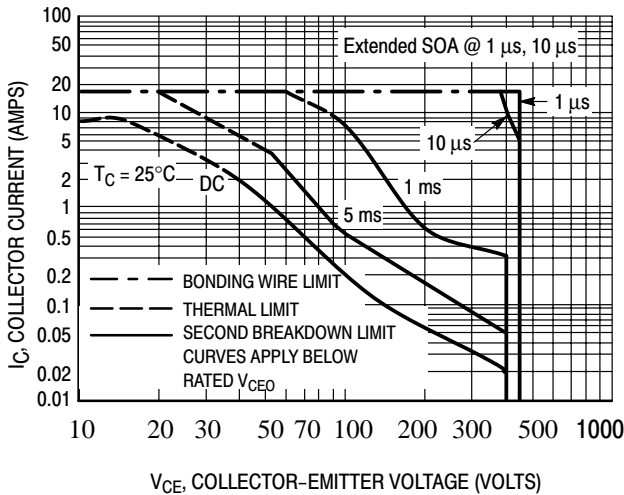


Figure 6. Maximum Forward Bias Safe Operating Area

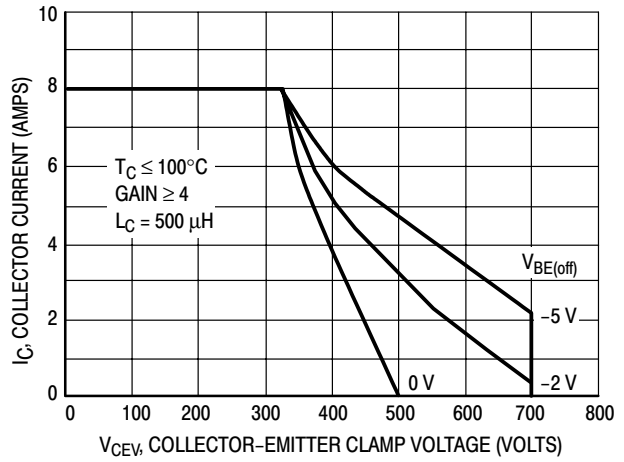


Figure 7. Maximum Reverse Bias Switching Safe Operating Area

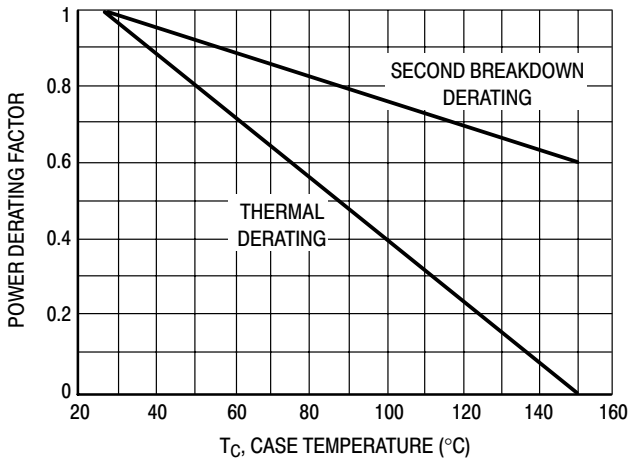


Figure 8. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 8.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 7) is discussed in the applications information section.

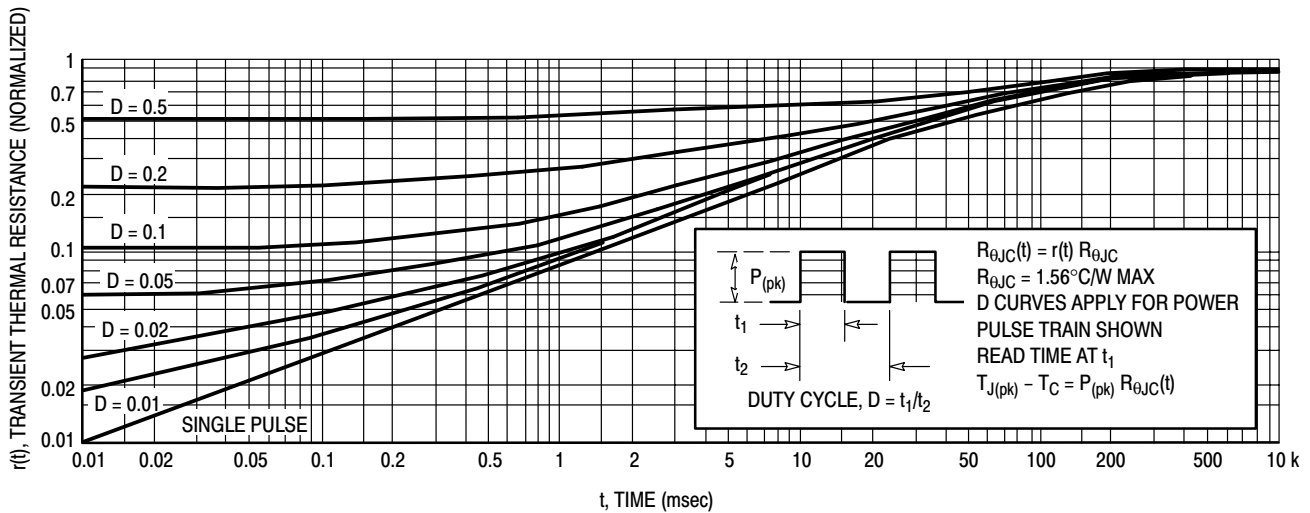


Figure 9. Typical Thermal Response for MJE13007

## SPECIFICATION INFORMATION FOR SWITCHMODE APPLICATIONS

## INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.<sup>(1)</sup>

## VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than  $V_{CC}$  after the device is completely off (see load line diagrams at  $I_C = I_{leakage} \approx 0$  in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased ( $V_{CEV}$ ), this is the recommended and specified use condition. Maximum  $I_{CEV}$  at rated  $V_{CEV}$  is specified at a relatively low reverse bias (1.5 Volts) both

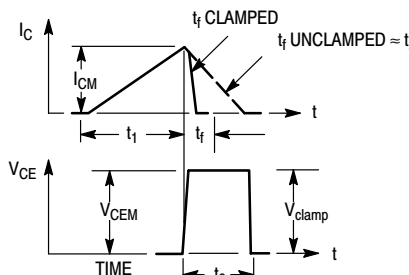
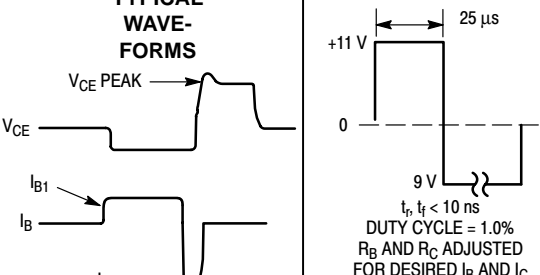
at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 6) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 7) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

- (1) For detailed information on specific switching applications, see ON Semiconductor Application Note AN719, AN873, AN875, AN951.

Table 1. Test Conditions For Dynamic Performance

TEST CIRCUITS	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING						
CIRCUIT VALUES	<table border="1"> <thead> <tr> <th><math>V_{(BR)CEO(sus)}</math></th> <th>Inductive Switching</th> <th>RBSOA</th> </tr> </thead> <tbody> <tr> <td> <math>L = 10 \text{ mH}</math>  <math>R_{B2} = 8</math>  <math>V_{CC} = 20 \text{ Volts}</math>  <math>I_{C(pk)} = 100 \text{ mA}</math> </td> <td> <math>L = 200 \text{ mH}</math>  <math>R_{B2} = 0</math>  <math>V_{CC} = 15 \text{ Volts}</math>  <math>R_{B1}</math> selected for desired <math>I_{B1}</math> </td> <td> <math>L = 500 \text{ mH}</math>  <math>R_{B2} = 0</math>  <math>V_{CC} = 15 \text{ Volts}</math>  <math>R_{B1}</math> selected for desired <math>I_{B1}</math> </td> </tr> </tbody> </table>	$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA	$L = 10 \text{ mH}$ $R_{B2} = 8$ $V_{CC} = 20 \text{ Volts}$ $I_{C(pk)} = 100 \text{ mA}$	$L = 200 \text{ mH}$ $R_{B2} = 0$ $V_{CC} = 15 \text{ Volts}$ $R_{B1}$ selected for desired $I_{B1}$	$L = 500 \text{ mH}$ $R_{B2} = 0$ $V_{CC} = 15 \text{ Volts}$ $R_{B1}$ selected for desired $I_{B1}$	<p><math>V_{CC} = 125 \text{ V}</math>  <math>R_C = 25 \Omega</math>  <math>D1 = 1N5820 \text{ OR EQUIV.}</math></p>
$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA						
$L = 10 \text{ mH}$ $R_{B2} = 8$ $V_{CC} = 20 \text{ Volts}$ $I_{C(pk)} = 100 \text{ mA}$	$L = 200 \text{ mH}$ $R_{B2} = 0$ $V_{CC} = 15 \text{ Volts}$ $R_{B1}$ selected for desired $I_{B1}$	$L = 500 \text{ mH}$ $R_{B2} = 0$ $V_{CC} = 15 \text{ Volts}$ $R_{B1}$ selected for desired $I_{B1}$						
TEST WAVEFORMS	 <p><math>t_1</math> ADJUSTED TO OBTAIN <math>I_C</math></p> $t_1 \approx \frac{L_{coil} (I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{CM})}{V_{clamp}}$ <p>TEST EQUIPMENT SCOPE — TEKTRONIX 475 OR EQUIVALENT</p>	<p><b>TYPICAL WAVEFORMS</b></p>  <p><math>t_f, t_r &lt; 10 \text{ ns}</math>  DUTY CYCLE = 1.0%  <math>R_B</math> AND <math>R_C</math> ADJUSTED FOR DESIRED <math>I_B</math> AND <math>I_C</math></p>						



**VOLTAGE REQUIREMENTS** (continued)

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

3. The device thermal limitations are not exceeded.
4. The turn-on time does not exceed 10  $\mu$ s  
(see standard pulsed forward SOA curves in Figure 6).
5. The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 7).

**CURRENT REQUIREMENTS**

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5.0 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the  $V_{CE(sat)}$  specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

**SWITCHING REQUIREMENTS**

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time ( $t_{fi}$ ). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are shown in Figures 12 and 13 and resistive loads in Figures 10 and 11. Usually the inductive load components will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (see Table 1) providing correlation between test procedures and actual use conditions.

**SWITCHING TIME NOTES**

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and any coil driver, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

$t_{sv}$  = Voltage Storage Time, 90%  $I_{B1}$  to 10%  $V_{clamp}$

$t_{rv}$  = Voltage Rise Time, 10–90%  $V_{clamp}$

$t_{fi}$  = Current Fall Time, 90–10%  $I_C$

$t_{ti}$  = Current Tail, 10–2%  $I_C$

$t_c$  = Crossover Time, 10%  $V_{clamp}$  to 10%  $I_C$

An enlarged portion of the turn-off waveforms is shown in Figure 12 to aid in the visual identity of these terms. For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

Typical inductive switching times are shown in Figure 13. In general,  $t_{rv} + t_{fi} \approx t_c$ . However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds ( $t_c$  and  $t_{sv}$ ) which are guaranteed at 100°C.

SWITCHING PERFORMANCE

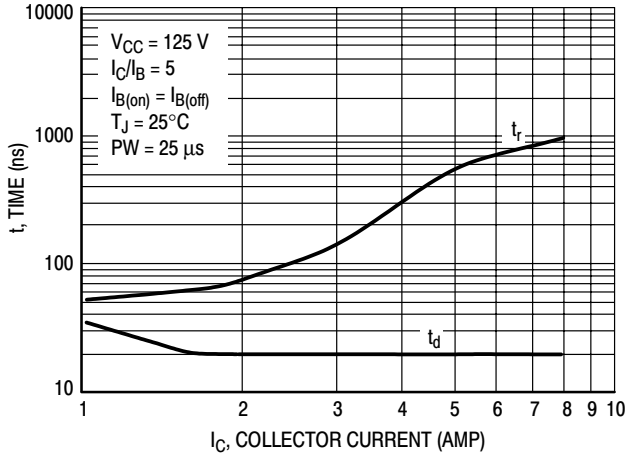


Figure 10. Turn-On Time (Resistive Load)

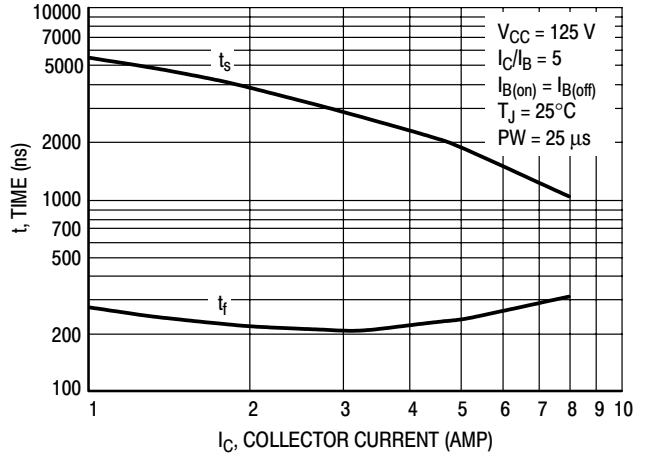


Figure 11. Turn-Off Time (Resistive Load)

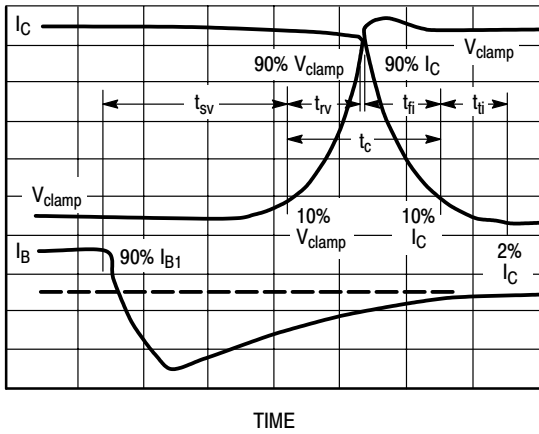


Figure 12. Inductive Switching Measurements

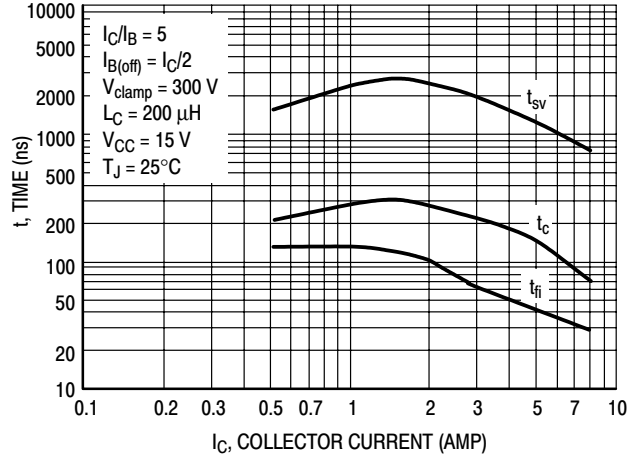
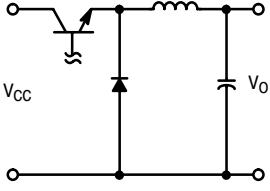
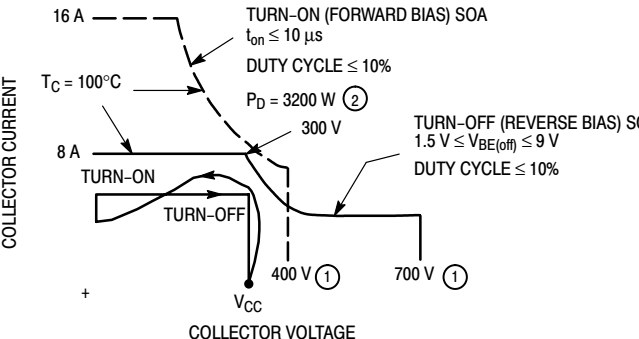
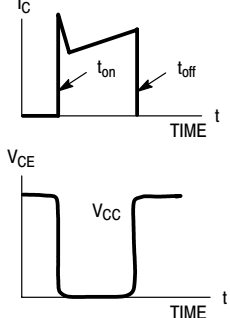
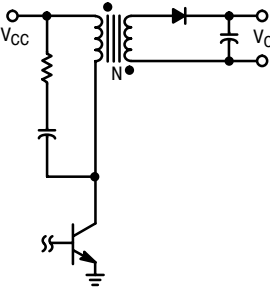
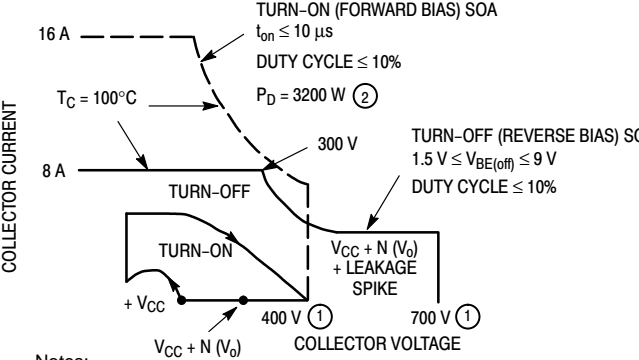
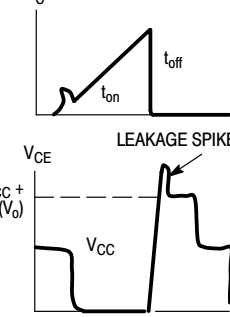
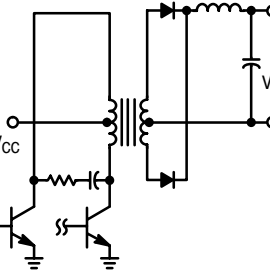
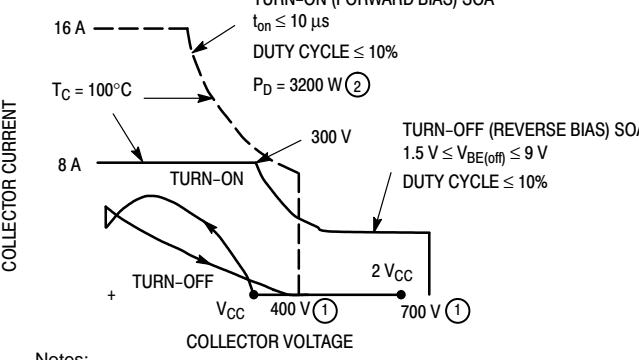
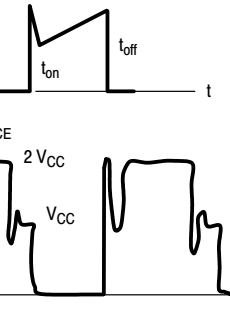
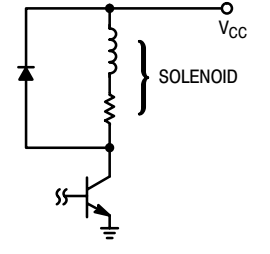
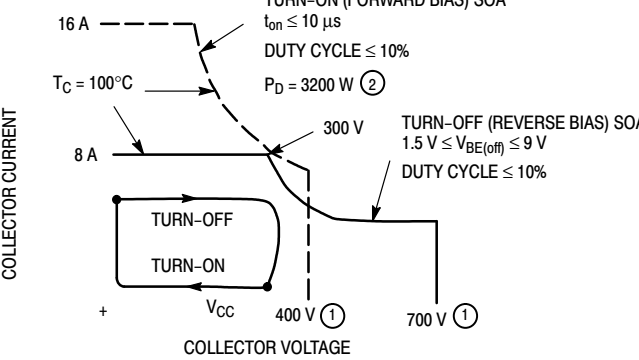
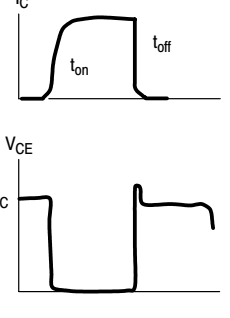


Figure 13. Typical Inductive Switching Times

Table 2. Applications Examples of Switching Circuits

CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
<p><b>A</b></p> <p><b>SERIES SWITCHING REGULATOR</b></p> 	 <p>Notes:              (1) See AN569 for Pulse Power Derating Procedure.</p>	
<p><b>B</b></p> <p><b>FLYBACK INVERTER</b></p> 	 <p>Notes:              (1) See AN569 for Pulse Power Derating Procedure.</p>	
<p><b>C</b></p> <p><b>PUSH-PULL INVERTER/CONVERTER</b></p> 	 <p>Notes:              (1) See AN569 for Pulse Power Derating Procedure.</p>	
<p><b>D</b></p> <p><b>SOLENOID DRIVER</b></p> 	 <p>Notes:              (1) See AN569 for Pulse Power Derating Procedure.</p>	

# SWITCHMODE™ Series NPN Silicon Power Transistors

The MJE13009 is designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

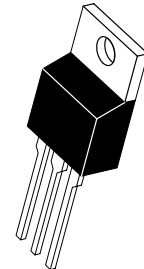
## SPECIFICATION FEATURES:

- $V_{CEO(sus)}$  400 V and 300 V
- Reverse Bias SOA with Inductive Loads @  $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 3 to 12 Amp, 25 and  $100^\circ\text{C}$   
 $t_c$  @ 8 A,  $100^\circ\text{C}$  is 120 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

## MJE13009\*

\*ON Semiconductor Preferred Device

**12 AMPERE  
NPN SILICON  
POWER TRANSISTOR  
400 VOLTS  
100 WATTS**



**CASE 221A-09  
TO-220AB**

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	$V_{CEV}$	700	Vdc
Emitter Base Voltage	$V_{EBO}$	9	Vdc
Collector Current — Continuous — Peak (1)	$I_C$ $I_{CM}$	12 24	Adc
Base Current — Continuous — Peak (1)	$I_B$ $I_{BM}$	6 12	Adc
Emitter Current — Continuous — Peak (1)	$I_E$ $I_{EM}$	18 36	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2 16	Watts mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	100 800	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq$  10%.

# MJE13009

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### \*OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	400	—	—	Vdc
Collector Cutoff Current (V <sub>CEV</sub> = Rated Value, V <sub>BE(off)</sub> = 1.5 Vdc) (V <sub>CEV</sub> = Rated Value, V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 100°C)	I <sub>CEV</sub>	—	—	1 5	mAdc
Emitter Cutoff Current (V <sub>EB</sub> = 9 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	—	1	mAdc

### SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased Clamped Inductive SOA with Base Reverse Biased	I <sub>S/b</sub> —	See Figure 1 See Figure 2			
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### \*ON CHARACTERISTICS

DC Current Gain (I <sub>C</sub> = 5 Adc, V <sub>CE</sub> = 5 Vdc) (I <sub>C</sub> = 8 Adc, V <sub>CE</sub> = 5 Vdc)	h <sub>FE</sub>	8 6	— —	40 30	
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 5 Adc, I <sub>B</sub> = 1 Adc) (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 1.6 Adc) (I <sub>C</sub> = 12 Adc, I <sub>B</sub> = 3 Adc) (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 1.6 Adc, T <sub>C</sub> = 100°C)	V <sub>CE(sat)</sub>	— — — —	— — — —	1 1.5 3 2	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 5 Adc, I <sub>B</sub> = 1 Adc) (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 1.6 Adc) (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 1.6 Adc, T <sub>C</sub> = 100°C)	V <sub>BE(sat)</sub>	— — —	— — —	1.2 1.6 1.5	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product (I <sub>C</sub> = 500 mAdc, V <sub>CE</sub> = 10 Vdc, f = 1 MHz)	f <sub>T</sub>	4	—	—	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	C <sub>ob</sub>	—	180	—	pF

### SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V <sub>CC</sub> = 125 Vdc, I <sub>C</sub> = 8 A, I <sub>B1</sub> = I <sub>B2</sub> = 1.6 A, t <sub>p</sub> = 25 μs, Duty Cycle ≤ 1%)	t <sub>d</sub>	—	0.06	0.1	μs
Rise Time		t <sub>r</sub>	—	0.45	1	μs
Storage Time		t <sub>s</sub>	—	1.3	3	μs
Fall Time		t <sub>f</sub>	—	0.2	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Voltage Storage Time	(I <sub>C</sub> = 8 A, V <sub>clamp</sub> = 300 Vdc, I <sub>B1</sub> = 1.6 A, V <sub>BE(off)</sub> = 5 Vdc, T <sub>C</sub> = 100°C)	t <sub>sv</sub>	—	0.92	2.3	μs
Crossover Time		t <sub>c</sub>	—	0.12	0.7	μs

\*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

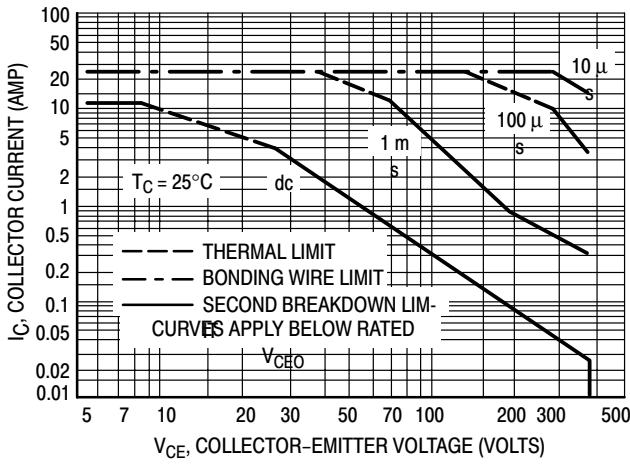


Figure 1. Forward Bias Safe Operating Area

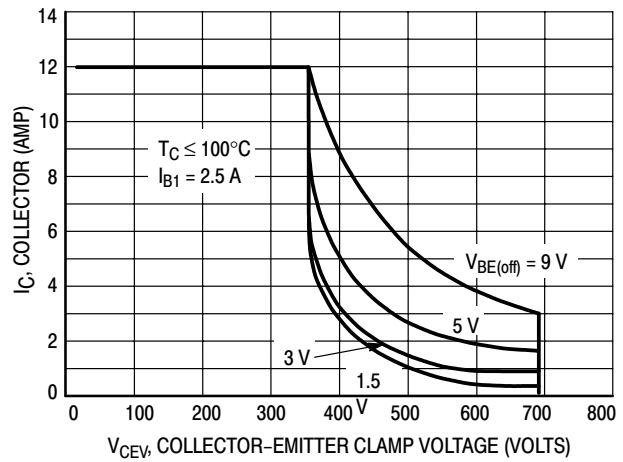


Figure 2. Reverse Bias Switching Safe Operating Area

The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

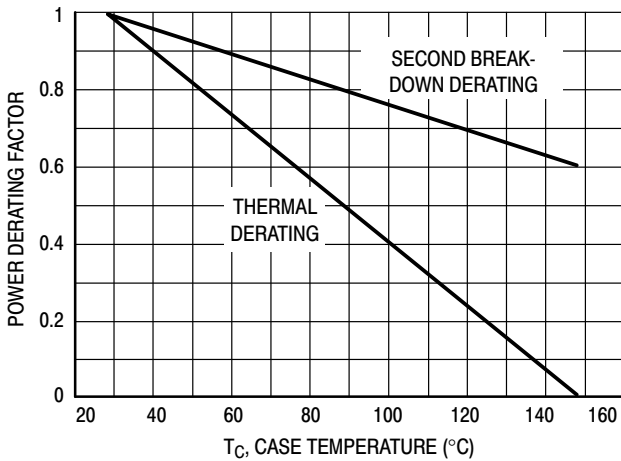


Figure 3. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

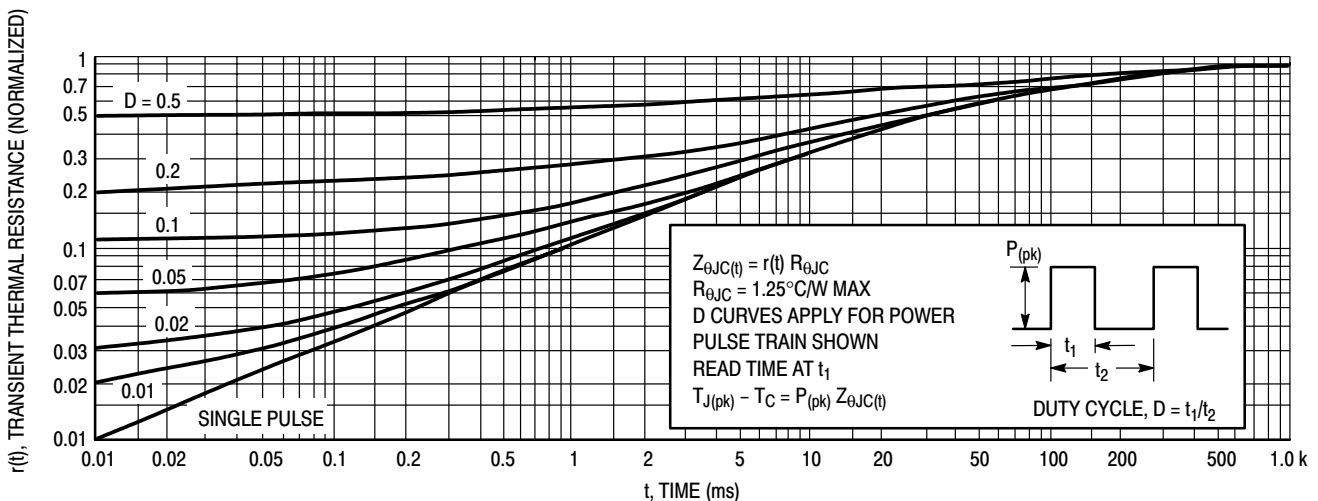


Figure 4. Typical Thermal Response [ $Z_{\theta JC}(t)$ ]

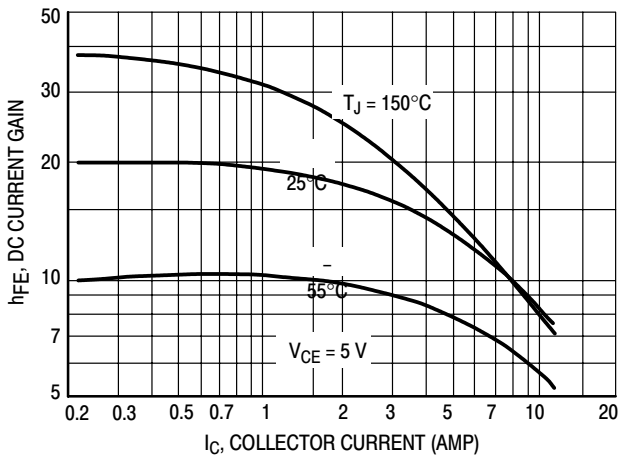


Figure 5. DC Current Gain

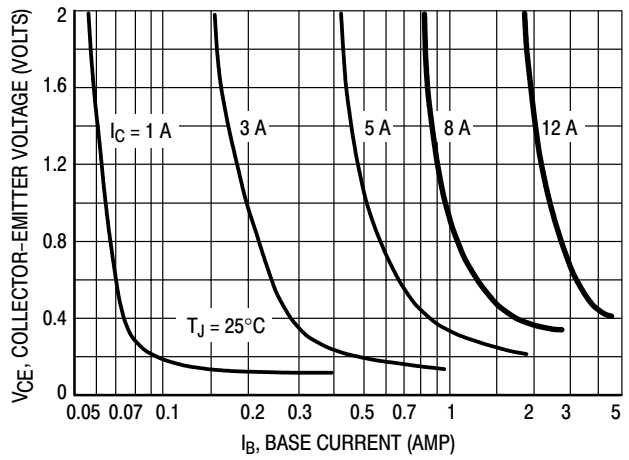


Figure 6. Collector Saturation Region

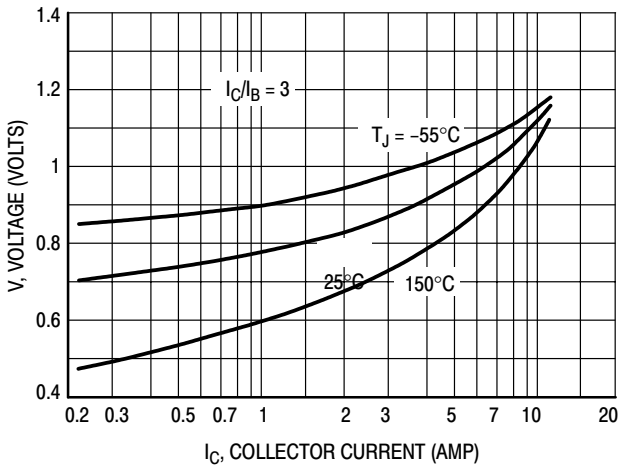


Figure 7. Base-Emitter Saturation Voltage

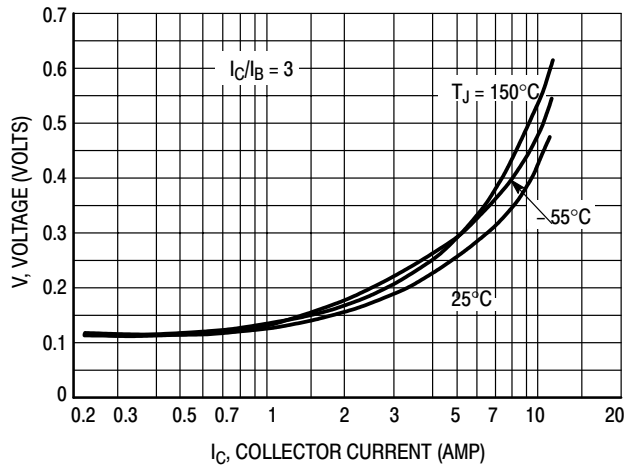


Figure 8. Collector-Emitter Saturation Voltage

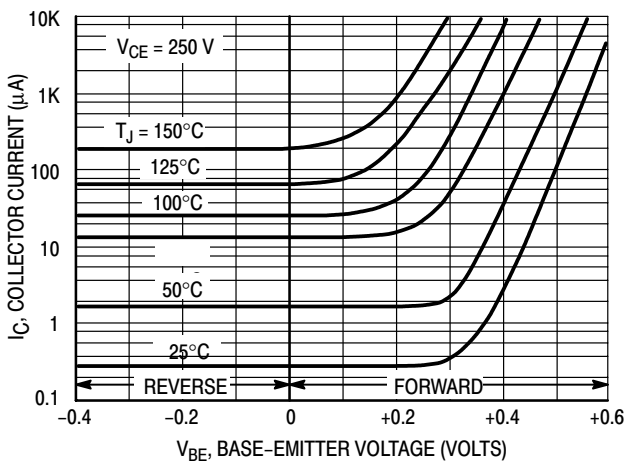


Figure 9. Collector Cutoff Region

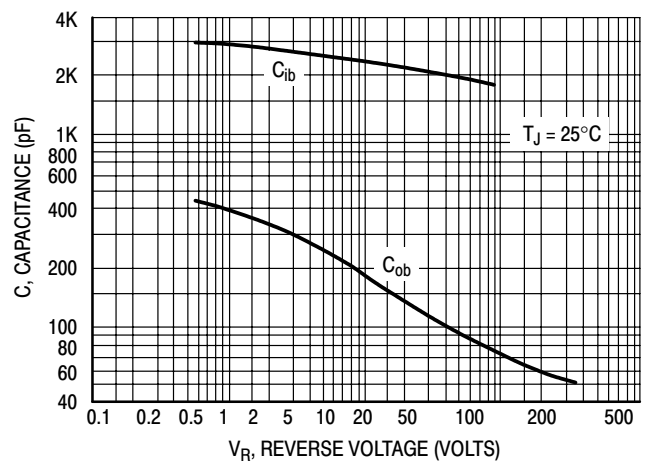


Figure 10. Capacitance

# MJE13009

Table 1. Test Conditions for Dynamic Performance

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
TEST CIRCUITS	<p>DUTY CYCLE <math>\leq 10\%</math>  <math>t_r, t_f \leq 10 \text{ ns}</math></p> <p>NOTE  PW and <math>V_{CC}</math> Adjusted for Desired <math>I_C</math>  <math>R_B</math> Adjusted for Desired <math>I_{B1}</math></p>	<p>*SELECTED FOR <math>\geq 1 \text{ kV}</math></p>
CIRCUIT VALUES	<p>Coil Data:  Ferroxcube Core #6656  Full Bobbin (~16 Turns) #16</p> <p>GAP for 200 <math>\mu\text{H}/20 \text{ A}</math>  <math>L_{\text{coil}} = 200 \mu\text{H}</math></p> <p><math>V_{CC} = 20 \text{ V}</math>  <math>V_{\text{clamp}} = 300 \text{ Vdc}</math></p>	<p><math>V_{CC} = 125 \text{ V}</math>  <math>R_C = 15 \Omega</math>  <math>D1 = 1\text{N}5820 \text{ or Equiv.}</math>  <math>R_B = \Omega</math></p>
TEST WAVEFORMS	<p><b>OUTPUT WAVEFORMS</b></p> <p><math>t_1</math> ADJUSTED TO OBTAIN <math>I_C</math></p> $t_1 \approx \frac{L_{\text{coil}} (I_{CM})}{V_{CC}}$ <p><math>t_2 \approx \frac{L_{\text{coil}} (I_{CM})}{V_{\text{clamp}}}</math></p> <p>Test Equipment  Scope—Tektronics 475 or Equivalent</p>	<p><math>t_r, t_f &lt; 10 \text{ ns}</math>  Duty Cycle = 1.0%  <math>R_B</math> and <math>R_C</math> adjusted for desired <math>I_B</math> and <math>I_C</math></p>



## APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

### INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.<sup>(1)</sup>

### VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than  $V_{CC}$  after the device is completely off (see load line diagrams at  $I_C = I_{leakage} \approx 0$  in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased ( $V_{CEV}$ ), this is the recommended and specified use condition. Maximum  $I_{CEV}$  at rated  $V_{CEV}$  is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

6. The device thermal limitations are not exceeded.
7. The turn-on time does not exceed 10  $\mu$ s (see standard pulsed forward SOA curves in Figure 1).
8. The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

### CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the  $V_{CE(sat)}$  specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

### SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time ( $t_{fi}$ ). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

(1) For detailed information on specific switching applications, see ON Semiconductor Application Notes AN-719, AN-767.

RESISTIVE SWITCHING PERFORMANCE

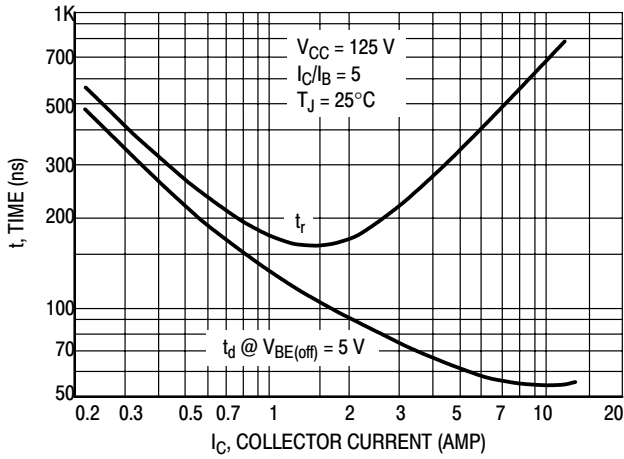


Figure 11. Turn-On Time

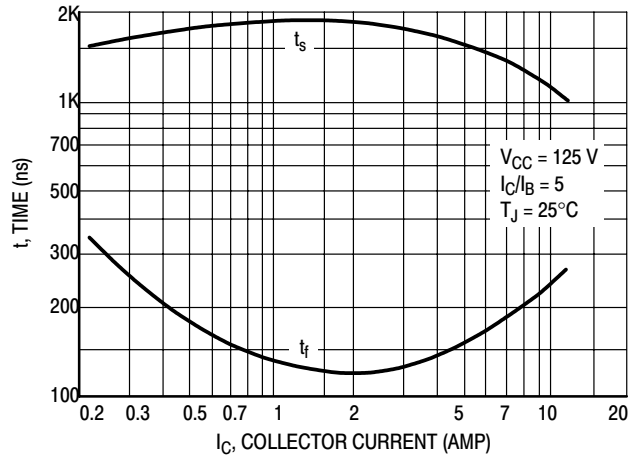


Figure 12. Turn-Off Time

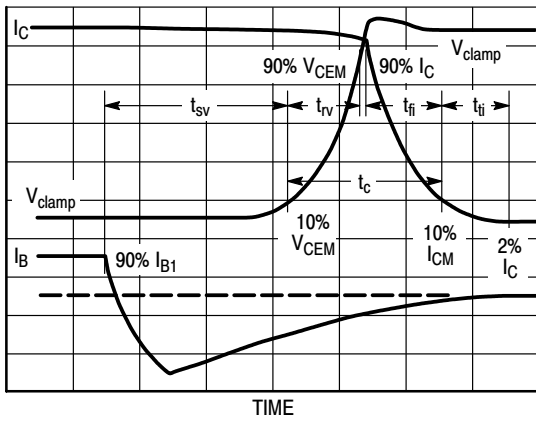


Figure 13. Inductive Switching Measurements

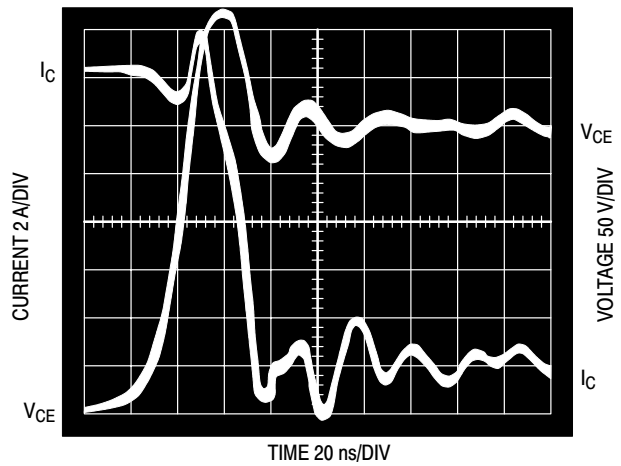


Figure 14. Typical Inductive Switching Waveforms (at 300 V and 12 A with  $I_{B1} = 2.4$  A and  $V_{BE(off)} = 5$  V)

Table 2. Applications Examples of Switching Circuits

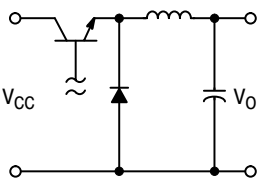
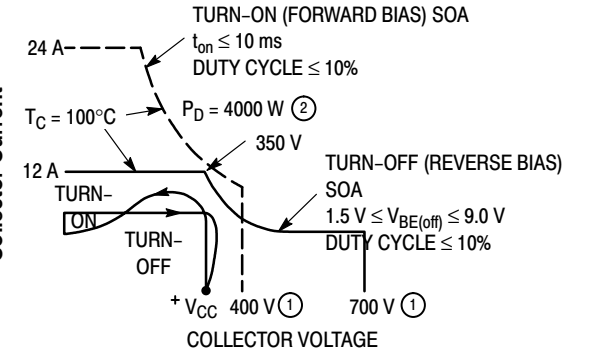
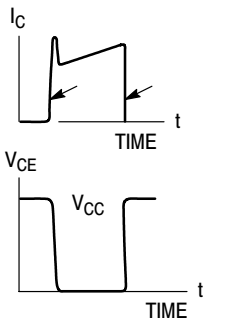
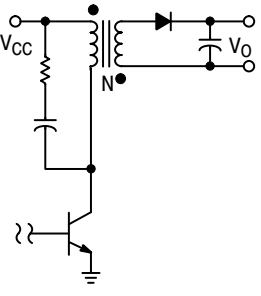
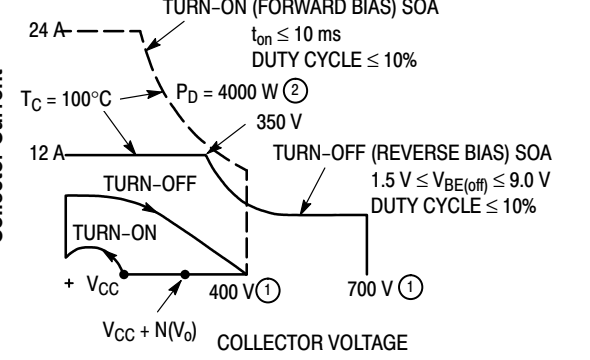
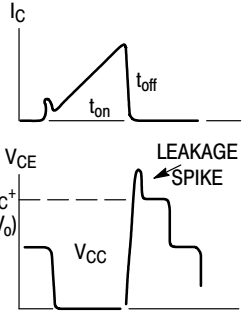
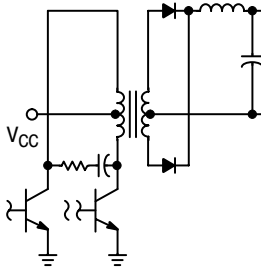
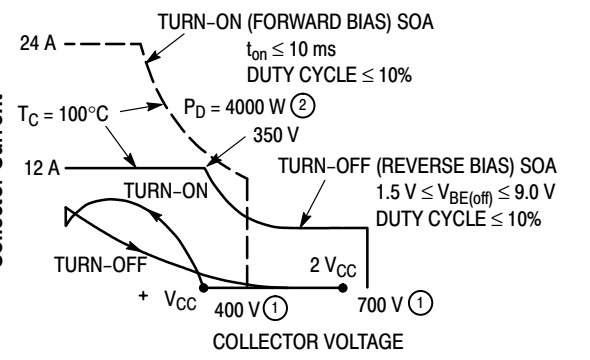
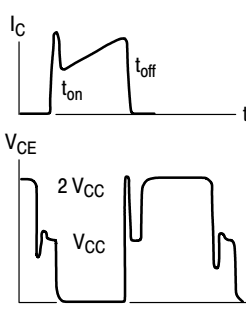
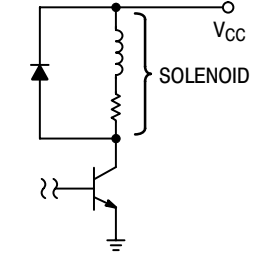
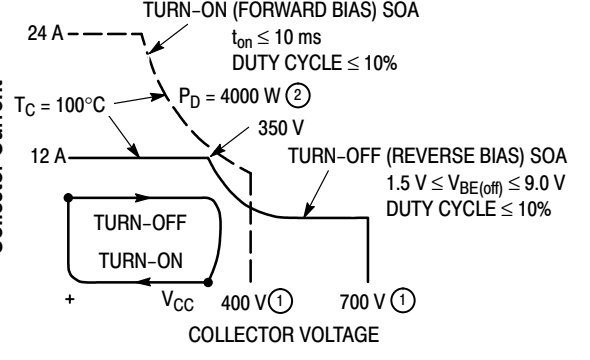
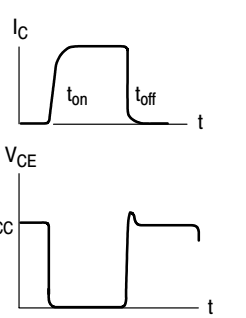
CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
<p><b>SERIES SWITCHING REGULATOR</b></p> 	<p><b>LOAD LINE DIAGRAMS</b></p> 	<p><b>TIME DIAGRAMS</b></p> 
<p><b>RINGING CHOKE INVERTER</b></p> 	<p><b>LOAD LINE DIAGRAMS</b></p> 	<p><b>TIME DIAGRAMS</b></p> 
<p><b>PUSH-PULL INVERTER/CONVERTER</b></p> 	<p><b>LOAD LINE DIAGRAMS</b></p> 	<p><b>TIME DIAGRAMS</b></p> 
<p><b>SOLENOID DRIVER</b></p> 	<p><b>LOAD LINE DIAGRAMS</b></p> 	<p><b>TIME DIAGRAMS</b></p> 

Table 3. Typical Inductive Switching Performance

I <sub>C</sub> AMP	T <sub>C</sub> °C	t <sub>sv</sub> ns	t <sub>rv</sub> ns	t <sub>fi</sub> ns	t <sub>ti</sub> ns	t <sub>c</sub> ns
3	25	770	100	150	200	240
	100	1000	230	160	200	320
5	25	630	72	26	10	100
	100	820	100	55	30	180
8	25	720	55	27	2	77
	100	920	70	50	8	120
12	25	640	20	17	2	41
	100	800	32	24	4	54

NOTE: All Data recorded In the Inductive Switching Circuit In Table 1.

**SWITCHING TIME NOTES**

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t<sub>sv</sub> = Voltage Storage Time, 90% I<sub>B1</sub> to 10% V<sub>CEM</sub>
- t<sub>rv</sub> = Voltage Rise Time, 10–90% V<sub>CEM</sub>
- t<sub>fi</sub> = Current Fall Time, 90–10% I<sub>CM</sub>
- t<sub>ti</sub> = Current Tail, 10–2% I<sub>CM</sub>
- t<sub>c</sub> = Crossover Time, 10% V<sub>CEM</sub> to 10% I<sub>CM</sub>

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

Typical inductive switching waveforms are shown in Figure 14. In general, t<sub>rv</sub> + t<sub>fi</sub> ≈ t<sub>c</sub>. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t<sub>c</sub> and t<sub>sv</sub>) which are guaranteed at 100°C.

# Complementary Silicon Plastic Power Transistors

... designed for use as high-frequency drivers in audio amplifiers.

- DC Current Gain Specified to 4.0 Amperes  
 $h_{FE} = 40$  (Min) @  $I_C = 3.0$  Adc  
 $= 20$  (Min) @  $I_C = 4.0$  Adc
- Collector–Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 120$  Vdc (Min) — MJE15028, MJE15029  
 $= 150$  Vdc (Min) — MJE15030, MJE15031
- High Current Gain — Bandwidth Product  
 $f_T = 30$  MHz (Min) @  $I_C = 500$  mAdc
- TO–220AB Compact Package

## MAXIMUM RATINGS

Rating	Symbol	MJE15028 MJE15029	MJE15030 MJE15031	Unit
Collector–Emitter Voltage	$V_{CEO}$	120	150	Vdc
Collector–Base Voltage	$V_{CB}$	120	150	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous — Peak	$I_C$	8.0 16		Adc
Base Current	$I_B$	2.0		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	50 0.40		Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

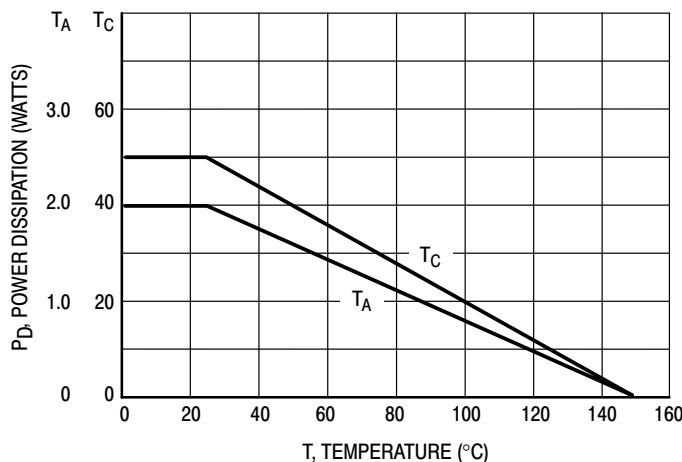


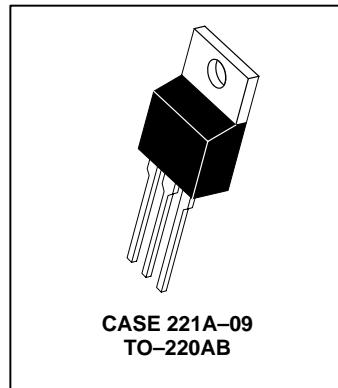
Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**NPN**  
**MJE15028\***  
**MJE15030\***  
**PNP**  
**MJE15029\***  
**MJE15031\***

\*ON Semiconductor Preferred Device

**8 AMPERE**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**120–150 VOLTS**  
**50 WATTS**



# MJE15028 MJE15030 MJE15029 MJE15031

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (1) ( $I_C = 10\text{ mA}$ , $I_B = 0$ )	MJE15028, MJE15029 MJE15030, MJE15031	$V_{CEO(sus)}$	120 150	— —	Vdc
Collector Cutoff Current ( $V_{CE} = 120\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 150\text{ Vdc}$ , $I_B = 0$ )	MJE15028, MJE15029 MJE15030, MJE15031	$I_{CEO}$	— —	0.1 0.1	mA
Collector Cutoff Current ( $V_{CB} = 120\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 150\text{ Vdc}$ , $I_E = 0$ )	MJE15028, MJE15029 MJE15030, MJE15031	$I_{CBO}$	— —	10 10	$\mu\text{A}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	10	$\mu\text{A}$
<b>ON CHARACTERISTICS (1)</b>					
DC Current Gain ( $I_C = 0.1\text{ A}$ , $V_{CE} = 2.0\text{ Vdc}$ ) ( $I_C = 2.0\text{ A}$ , $V_{CE} = 2.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ A}$ , $V_{CE} = 2.0\text{ Vdc}$ ) ( $I_C = 4.0\text{ A}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$h_{FE}$	40 40 40 20	— — — —	—	
DC Current Gain Linearity ( $V_{CE}$ From 2.0 V to 20 V, $I_C$ From 0.1 A to 3 A) (NPN TO PNP)	$h_{FE}$	<b>Typ</b> 2 3			
Collector–Emitter Saturation Voltage ( $I_C = 1.0\text{ A}$ , $I_B = 0.1\text{ A}$ )	$V_{CE(sat)}$	—	0.5		Vdc
Base–Emitter On Voltage ( $I_C = 1.0\text{ A}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$V_{BE(on)}$	—	1.0		Vdc
<b>DYNAMIC CHARACTERISTICS</b>					
Current Gain — Bandwidth Product (2) ( $I_C = 500\text{ mA}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 10\text{ MHz}$ )	$f_T$	30	—		MHz

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

(2)  $f_T = |h_{fe}| \cdot f_{test}$ .

MJE15028 MJE15030 MJE15029 MJE15031

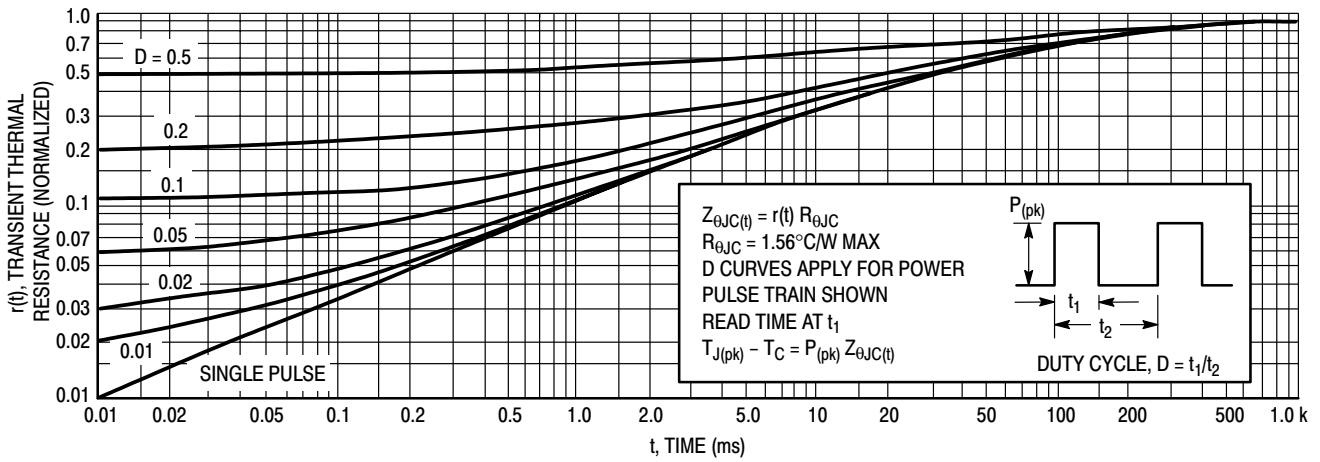


Figure 2. Thermal Response

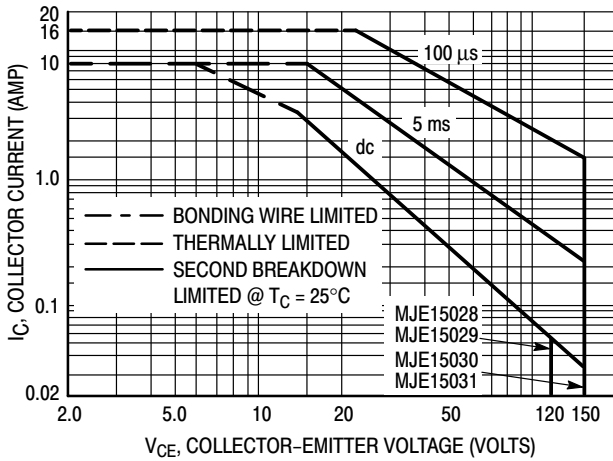


Figure 3. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 3 and 4 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

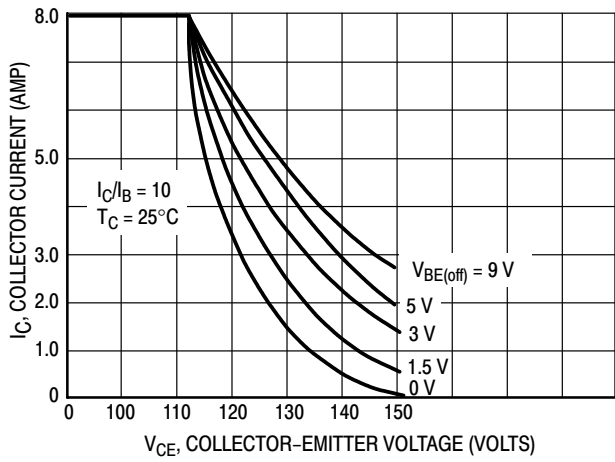


Figure 4. Reverse-Bias Switching Safe Operating Area

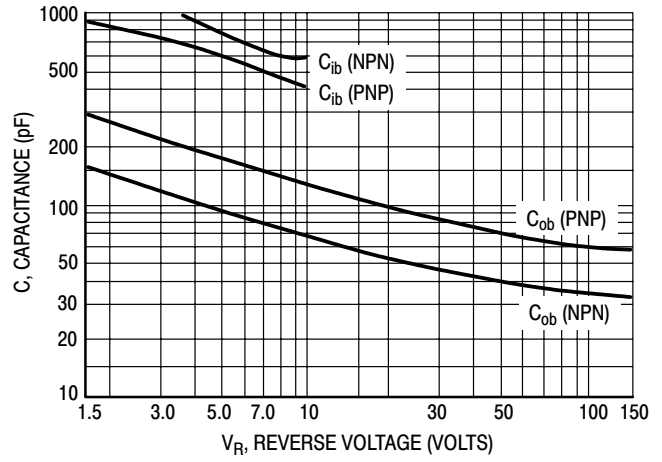


Figure 5. Capacitances

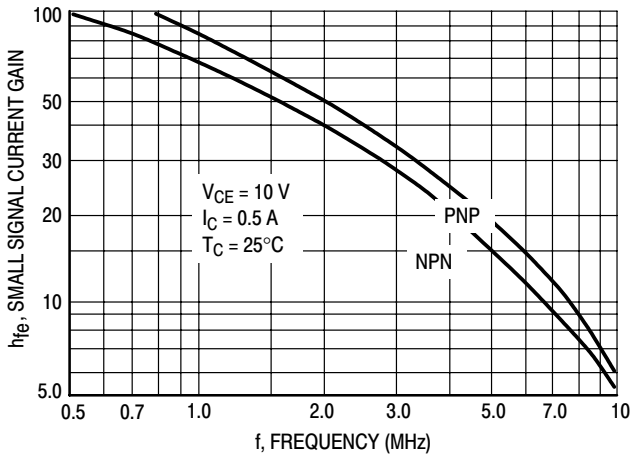


Figure 6. Small-Signal Current Gain

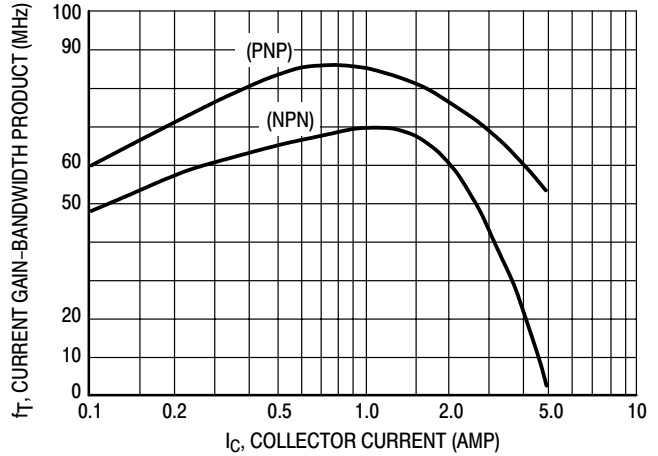
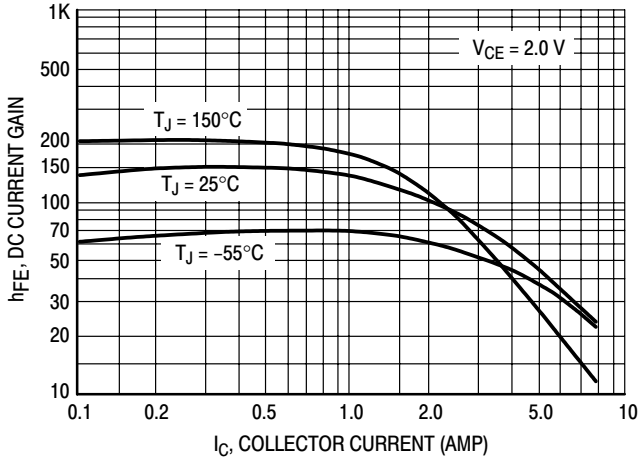


Figure 7. Current Gain-Bandwidth Product

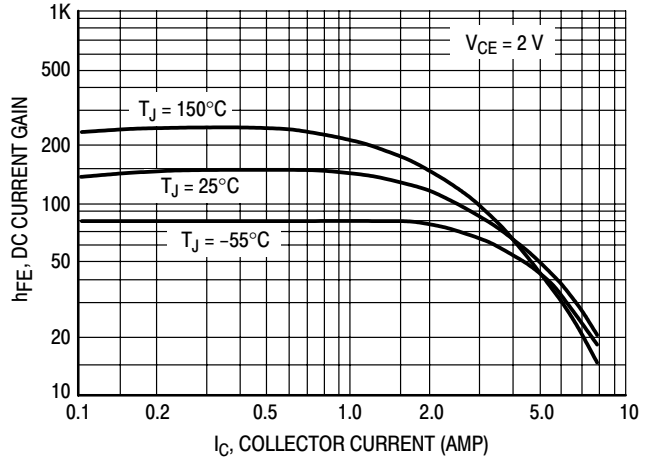


# MJE15028 MJE15030 MJE15029 MJE15031

**NPN — MJE15028 MJE15030**

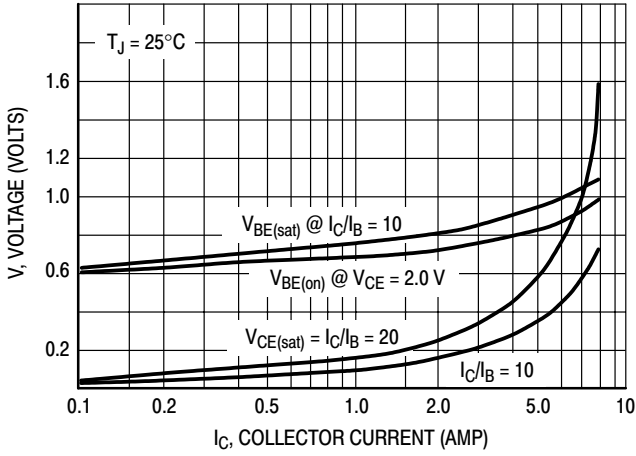


**PNP — MJE15029 MJE15031**

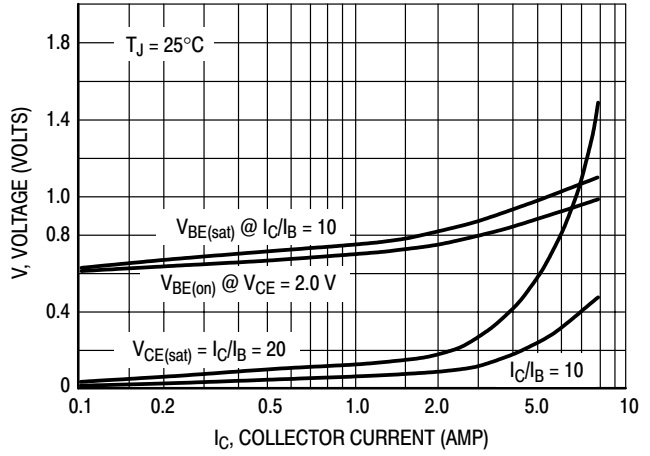


**Figure 8. DC Current Gain**

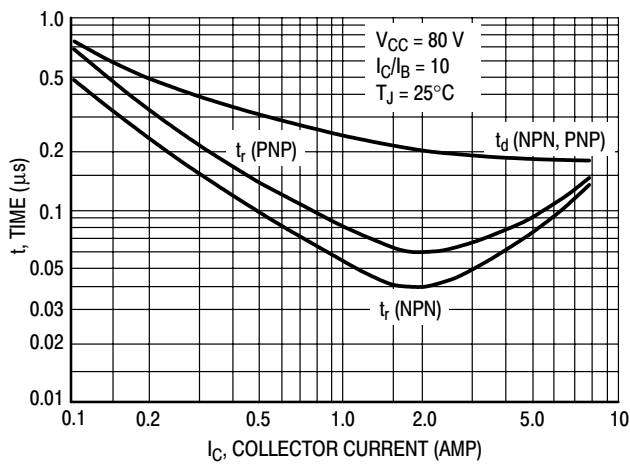
**NPN**



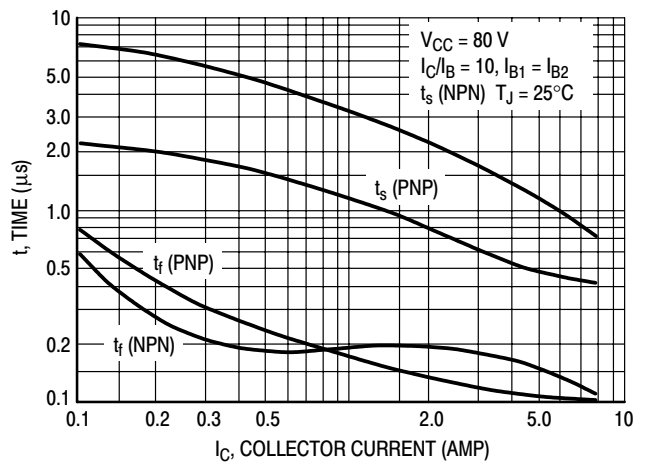
**PNP**



**Figure 9. "On" Voltage**



**Figure 10. Turn-On Times**



**Figure 11. Turn-Off Times**

# Complementary Silicon Plastic Power Transistors

... designed for use as high-frequency drivers in audio amplifiers.

- DC Current Gain Specified to 5.0 Amperes  
 $h_{FE} = 50$  (Min) @  $I_C = 0.5$  Adc  
 $= 10$  (Min) @  $I_C = 2.0$  Adc
- Collector-Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 250$  Vdc (Min) — MJE15032, MJE15033
- High Current Gain — Bandwidth Product  
 $f_T = 30$  MHz (Min) @  $I_C = 500$  mAdc
- TO-220AB Compact Package

## MAXIMUM RATINGS

Rating	Symbol	MJE15032 MJE15033	Unit
Collector-Emitter Voltage	$V_{CEO}$	250	Vdc
Collector-Base Voltage	$V_{CB}$	250	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous — Peak	$I_C$	8.0 16	Adc
Base Current	$I_B$	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	50 0.40	Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

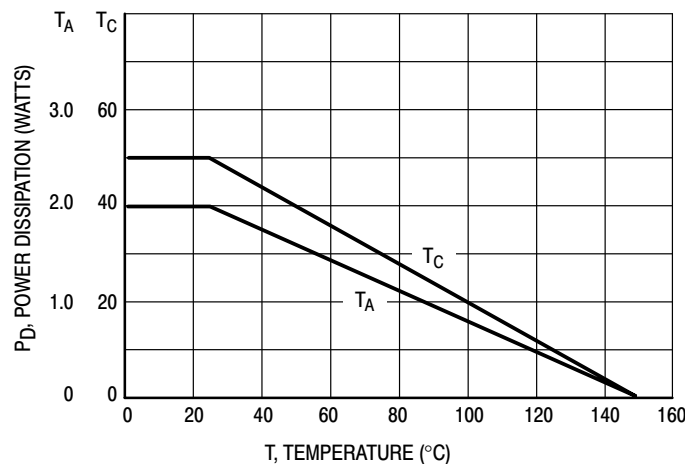


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**NPN**  
**MJE15032\***  
  
**PNP**  
**MJE15033\***

\*ON Semiconductor Preferred Device

**8.0 AMPERES**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**250 VOLTS**  
**50 WATTS**

**CASE 221A-09**  
**TO-220AB**

# MJE15032 MJE15033

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 10\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	250	—	Vdc
Collector Cutoff Current ( $V_{CB} = 150\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	10	$\mu\text{Adc}$

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ )	$h_{FE}$	50 50 10	— — —	—
Collector–Emitter Saturation Voltage ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter On Voltage ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ )	$V_{BE(on)}$	—	1.0	Vdc

## DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product (2) ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	30	—	MHz
--	-------	----	---	-----

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

(2)  $f_T = |h_{fe}| \cdot f_{test}$ .

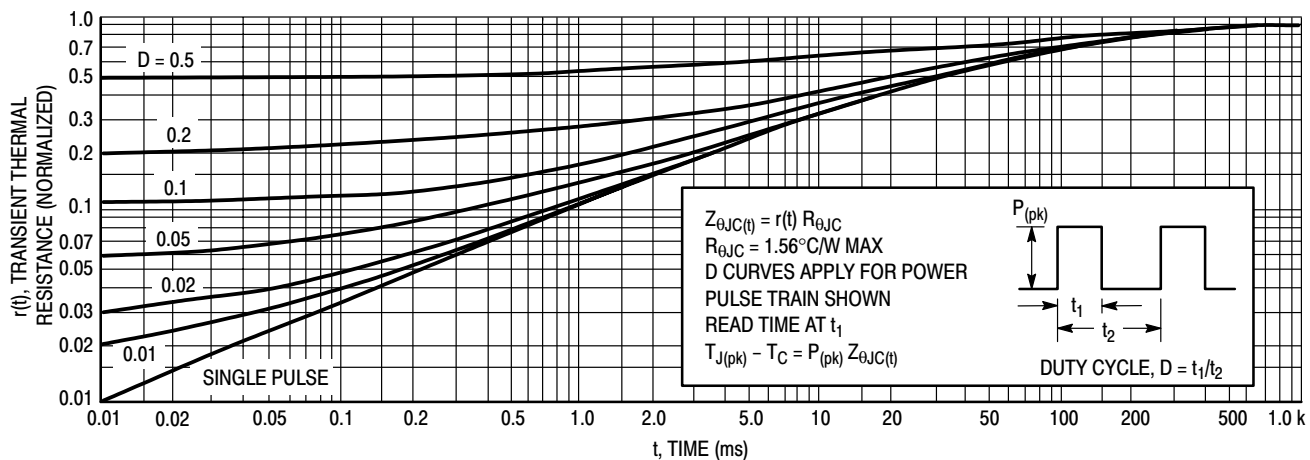
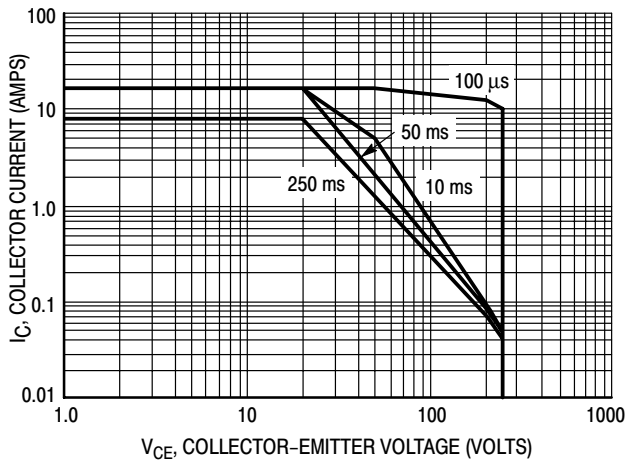


Figure 2. Thermal Response

# MJE15032 MJE15033

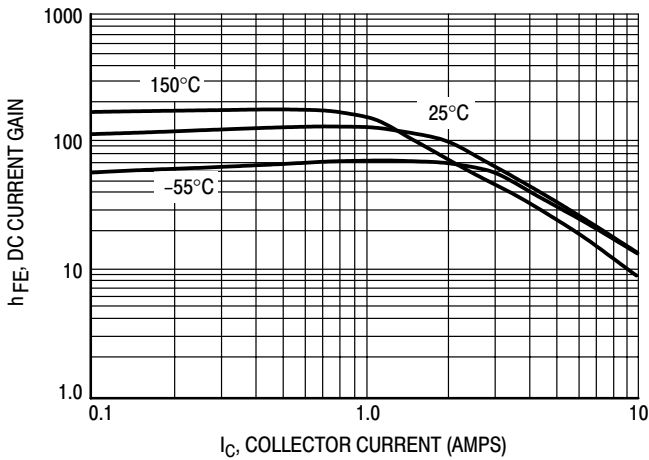


**Figure 3. MJE15032 & MJE15033  
Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

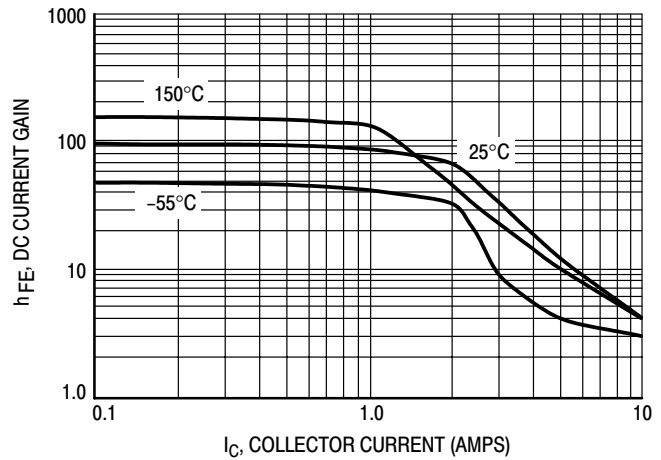
The data of Figures 3 and 4 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

## NPN — MJE15032

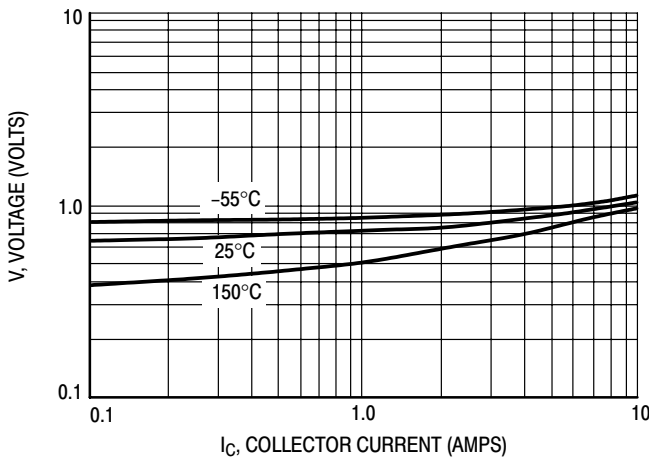


**Figure 4. NPN — MJE15032  
 $V_{CE} = 5\text{ V}$  DC Current Gain**

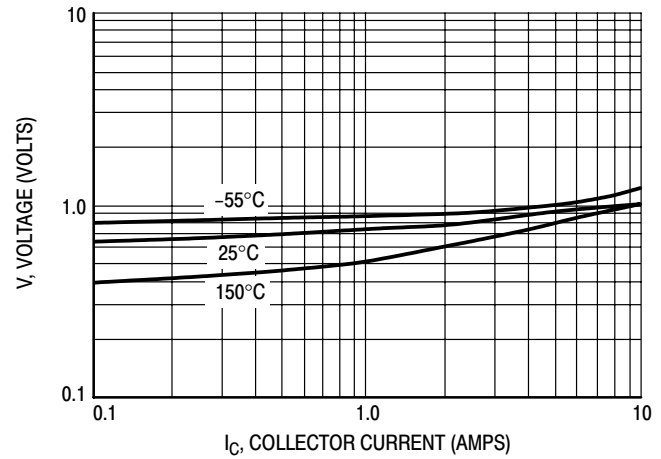
## PNP — MJE15033



**Figure 5. PNP — MJE15033  
 $V_{CE} = 5\text{ V}$  DC Current Gain**



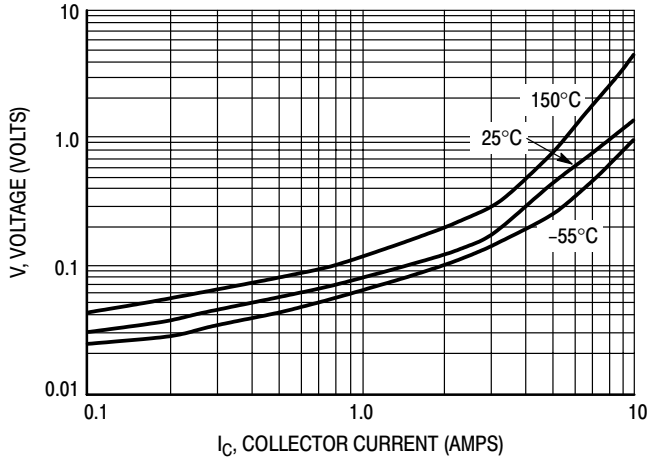
**Figure 6. NPN — MJE15032  
 $V_{CE} = 5\text{ V}$   $V_{BE(on)}$  Curve**



**Figure 7. PNP — MJE15033  
 $V_{CE} = 5\text{ V}$   $V_{BE(on)}$  Curve**

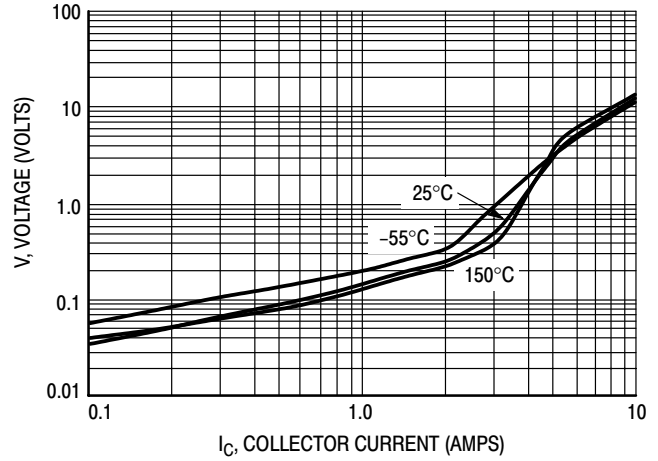
# MJE15032 MJE15033

**NPN — MJE15032**

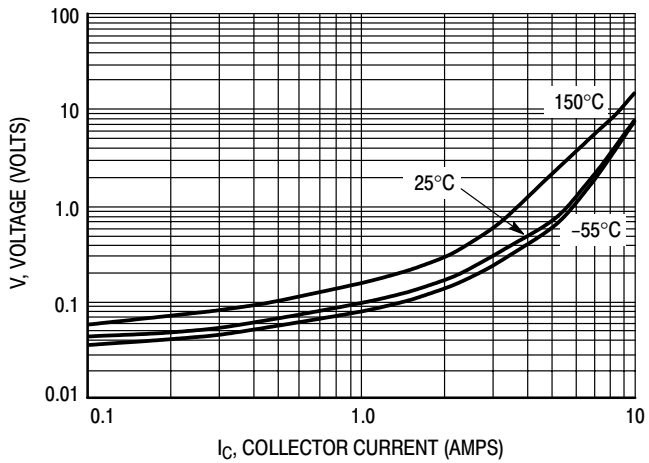


**Figure 8. NPN — MJE15032**  
 $V_{CE(sat)} I_C/I_B = 10$

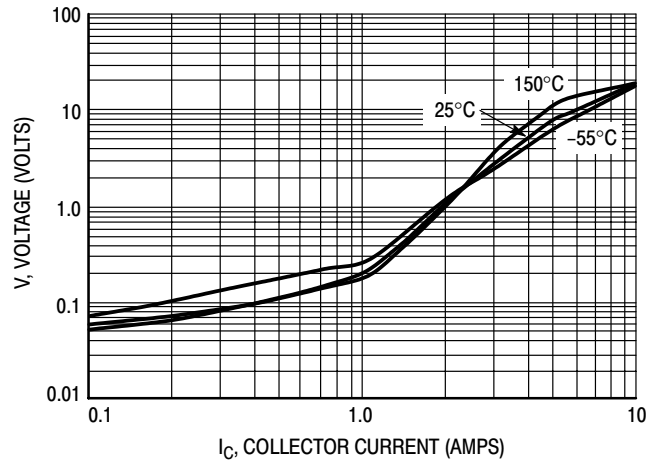
**PNP — MJE15033**



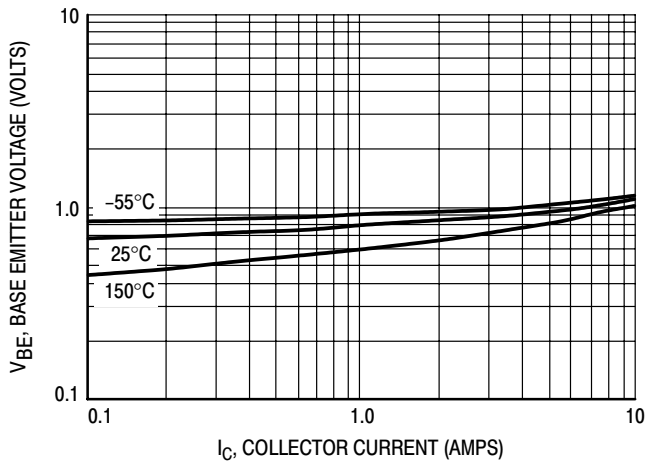
**Figure 9. PNP — MJE15033**  
 $V_{CE(sat)} I_C/I_B = 10$



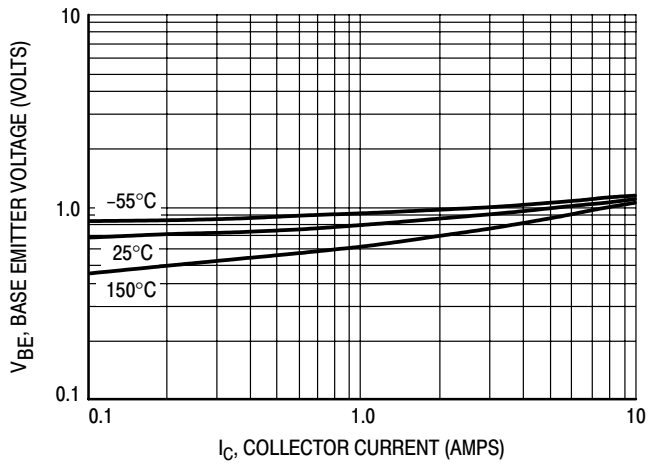
**Figure 10. NPN — MJE15032**  
 $V_{CE(sat)} I_C/I_B = 20$



**Figure 11. PNP — MJE15033**  
 $V_{CE(sat)} I_C/I_B = 20$



**Figure 12. NPN — MJE15032**  
 $V_{BE(sat)} I_C/I_B = 10$



**Figure 13. PNP — MJE15033**  
 $V_{BE(sat)} I_C/I_B = 10$

# Complementary Plastic Silicon Power Transistors

... designed for low power audio amplifier and low current, high speed switching applications.

- Collector–Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 60 \text{ Vdc}$  — MJE171, MJE181  
 $= 80 \text{ Vdc}$  — MJE172, MJE182
- DC Current Gain —  
 $h_{FE} = 30 \text{ (Min) @ } I_C = 0.5 \text{ Adc}$   
 $= 12 \text{ (Min) @ } I_C = 1.5 \text{ Adc}$
- Current–Gain — Bandwidth Product —  
 $f_T = 50 \text{ MHz (Min) @ } I_C$   
 $= 100 \text{ mAdc}$
- Annular Construction for Low Leakages —  
 $I_{CBO} = 100 \text{ nA (Max) @ Rated } V_{CB}$

## MAXIMUM RATINGS

Rating	Symbol	MJE171 MJE181	MJE172 MJE182	Unit
Collector–Base Voltage	$V_{CB}$	80	100	Vdc
Collector–Emitter Voltage	$V_{CEO}$	60	80	Vdc
Emitter–Base Voltage	$V_{EB}$	7.0		Vdc
Collector Current — Continuous Peak	$I_C$	3.0 6.0		Adc
Base Current	$I_B$	1.0		Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.5 0.012		Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	12.5 0.1		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C}$

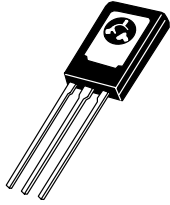
## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	10	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	83.4	$^\circ\text{C/W}$

**PNP**  
**MJE171\***  
  
**MJE172\***  
**NPN**  
**MJE181\***  
  
**MJE182\***

\*ON Semiconductor Preferred Device

**3 AMPERE**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**60–80 VOLTS**  
**12.5 WATTS**



**CASE 77–09**  
**TO–225AA**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJE171 MJE172 MJE181 MJE182

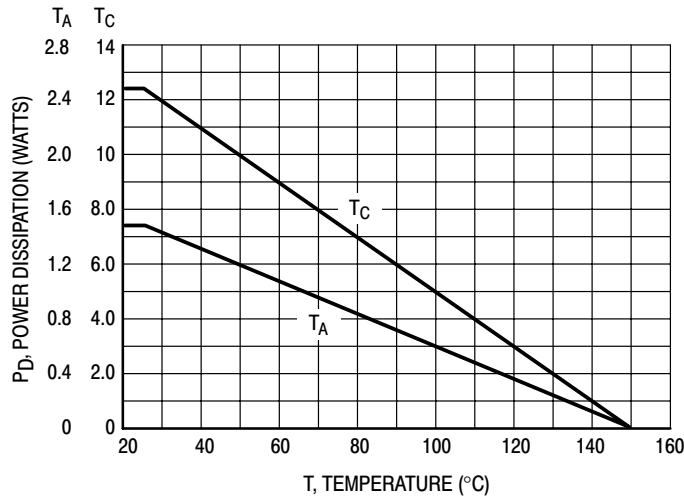


Figure 1. Power Derating

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 10 mAdc, I <sub>B</sub> = 0)	MJE171, MJE181 MJE172, MJE182	V <sub>CEO(sus)</sub>	60 80	— —	Vdc
Collector Cutoff Current (V <sub>CB</sub> = 80 Vdc, I <sub>E</sub> = 0) (V <sub>CB</sub> = 100 Vdc, I <sub>E</sub> = 0) (V <sub>CB</sub> = 80 Vdc, I <sub>E</sub> = 0, T <sub>C</sub> = 150°C) (V <sub>CB</sub> = 100 Vdc, I <sub>E</sub> = 0, T <sub>C</sub> = 150°C)	MJE171, MJE181 MJE172, MJE182 MJE171, MJE181 MJE172, MJE182	I <sub>CBO</sub>	— — — —	0.1 0.1 0.1 0.1	μAdc mAdc
Emitter Cutoff Current (V <sub>BE</sub> = 7.0 Vdc, I <sub>C</sub> = 0)		I <sub>EBO</sub>	—	0.1	μAdc

### ON CHARACTERISTICS

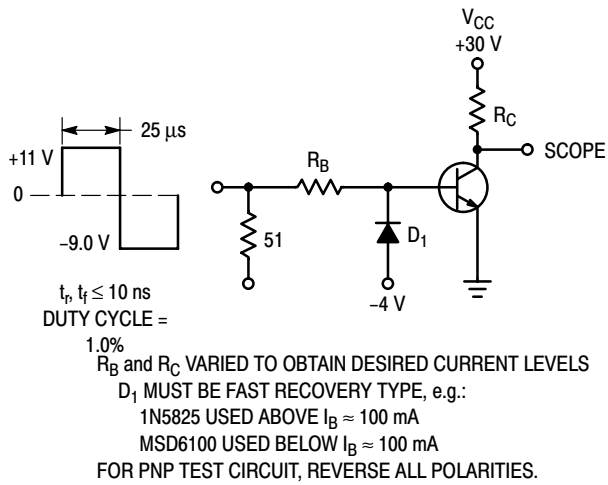
DC Current Gain (I <sub>C</sub> = 100 mAdc, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 500 mAdc, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 1.5 Adc, V <sub>CE</sub> = 1.0 Vdc)		h <sub>FE</sub>	50 30 12	250 — —	—
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 500 mAdc, I <sub>B</sub> = 50 mAdc) (I <sub>C</sub> = 1.5 Adc, I <sub>B</sub> = 150 mAdc) (I <sub>C</sub> = 3.0 Adc, I <sub>B</sub> = 600 mAdc)		V <sub>CE(sat)</sub>	— — —	0.3 0.9 1.7	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 1.5 Adc, I <sub>B</sub> = 150 mAdc) (I <sub>C</sub> = 3.0 Adc, I <sub>B</sub> = 600 mAdc)		V <sub>BE(sat)</sub>	— —	1.5 2.0	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 500 mAdc, V <sub>CE</sub> = 1.0 Vdc)		V <sub>BE(on)</sub>	—	1.2	Vdc

### DYNAMIC CHARACTERISTICS

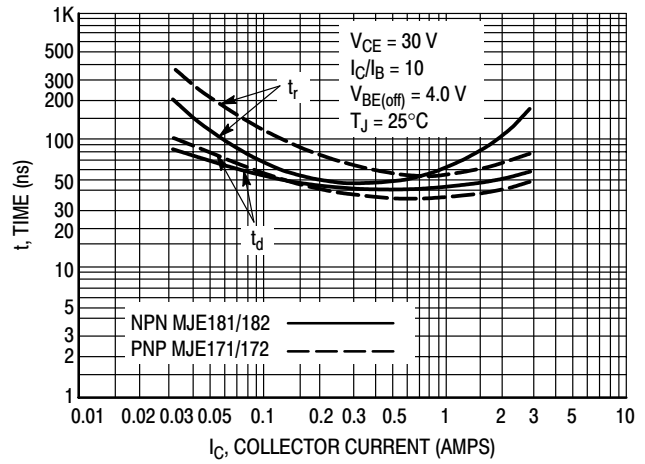
Current–Gain — Bandwidth Product (1) (I <sub>C</sub> = 100 mAdc, V <sub>CE</sub> = 10 Vdc, f <sub>test</sub> = 10 MHz)		f <sub>T</sub>	50	—	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	MJE171/MJE172 MJE181/MJE182	C <sub>ob</sub>	— —	60 40	pF

(1) f<sub>T</sub> = |h<sub>fe</sub>| • f<sub>test</sub>.

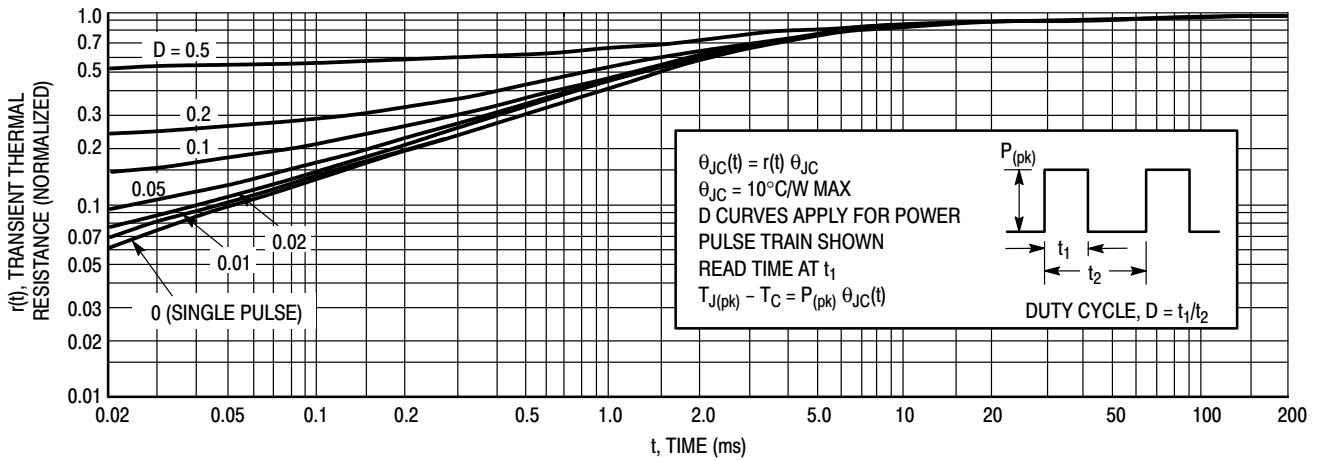
# MJE171 MJE172 MJE181 MJE182



**Figure 2. Switching Time Test Circuit**



**Figure 3. Turn-On Time**



**Figure 4. Thermal Response**



# MJE171 MJE172 MJE181 MJE182

## ACTIVE-REGION SAFE OPERATING AREA

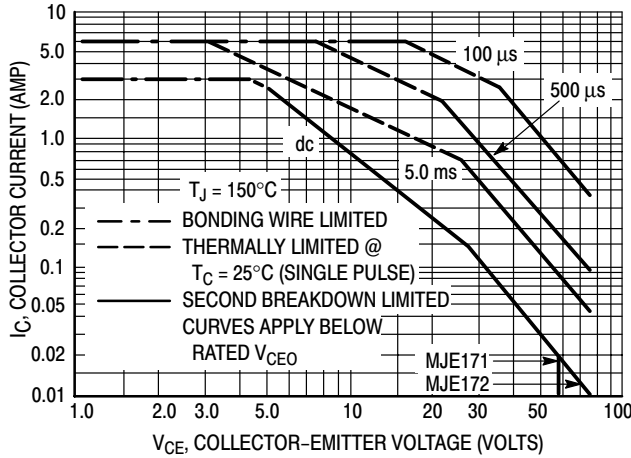


Figure 5. MJE171, MJE172

There are two limitations on the power handling ability of a transistor — average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown

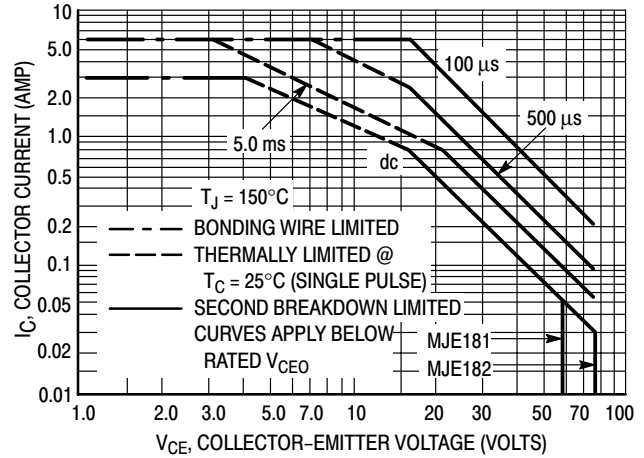


Figure 6. MJE181, MJE182

pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

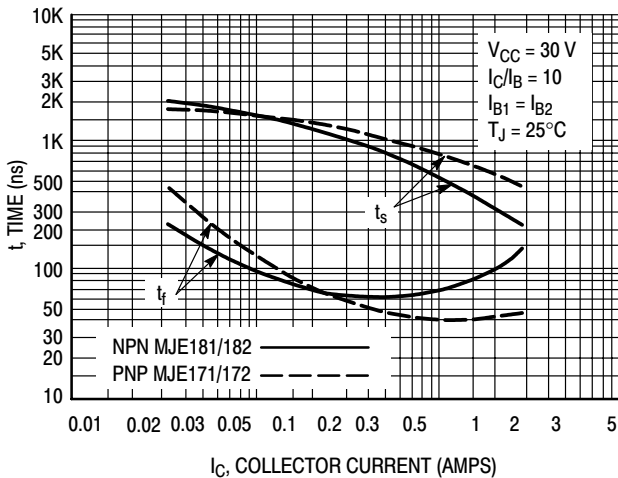


Figure 7. Turn-Off Time

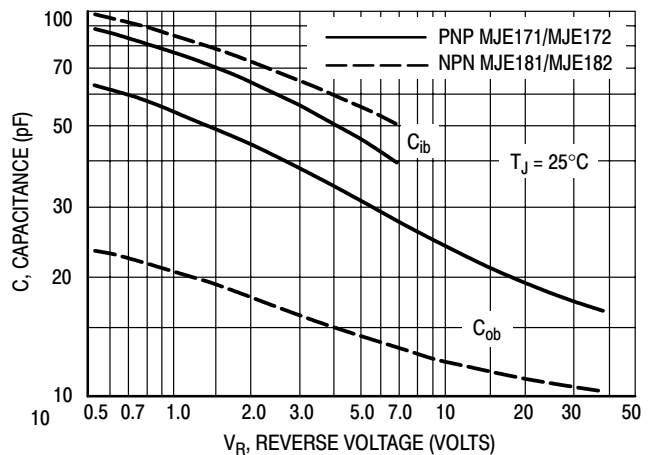


Figure 8. Capacitance

# SWITCHMODE™

## NPN Bipolar Power Transistor For Switching Power Supply Applications

The MJE18002 have an applications specific state-of-the-art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain  $h_{FE}$
  - Fast Switching
  - No Coil Required in Base Circuit for Turn-Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot-to-Lot
- Standard TO-220

### MAXIMUM RATINGS

Rating	Symbol	MJE18002	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	450	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	1000	Vdc
Emitter-Base Voltage	$V_{EBO}$	9.0	Vdc
Collector Current – Continuous	$I_C$	2.0	Adc
– Peak(1)	$I_{CM}$	5.0	
Base Current – Continuous	$I_B$	1.0	Adc
– Peak(1)	$I_{BM}$	2.0	
Total Device Dissipation Derate above 25°C	$P_D$	50 0.4	Watts W/°C
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150	°C

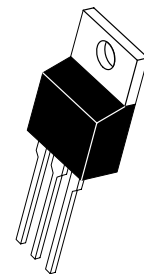
### THERMAL CHARACTERISTICS

Rating	Symbol	MJE18002	Unit
Thermal Resistance – Junction to Case	$R_{\theta JC}$	2.5	°C/W
– Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	260	°C

**MJE18002\***

\*ON Semiconductor Preferred Device

**POWER TRANSISTOR  
2.0 AMPERES  
1000 VOLTS  
50 WATTS**



**CASE 221A-09  
TO-220AB  
MJE18002**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJE18002

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	450	–	–	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$	–	–	100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ ) ( $V_{CE} = 800\text{ V}$ , $V_{EB} = 0$ )	$I_{CES}$	–	–	100	$\mu\text{Adc}$
		–	–	500	
		–	–	100	
Emitter Cutoff Current ( $V_{EB} = 9.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	–	100	$\mu\text{Adc}$

## ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 0.4\text{ Adc}$ , $I_B = 40\text{ mAdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	$V_{BE(sat)}$	–	0.825	1.1	Vdc
		–	0.92	1.25	
Collector–Emitter Saturation Voltage ( $I_C = 0.4\text{ Adc}$ , $I_B = 40\text{ mAdc}$ )  @ $T_C = 125^\circ\text{C}$	$V_{CE(sat)}$	–	0.2	0.5	Vdc
		–	0.2	0.5	
( $I_C = 1.0\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )  @ $T_C = 125^\circ\text{C}$		–	0.25	0.5	
		–	0.3	0.6	
DC Current Gain ( $I_C = 0.2\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ )  @ $T_C = 125^\circ\text{C}$	$h_{FE}$	14	–	34	–
		–	27	–	
( $I_C = 0.4\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )  @ $T_C = 125^\circ\text{C}$		11	17	–	
		11	20	–	
( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )  @ $T_C = 125^\circ\text{C}$		6.0	8.0	–	
		5.0	8.0	–	
( $I_C = 10\text{ mAdc}$ , $V_{CE} = 5.0\text{ Vdc}$ )  @ $T_C = 125^\circ\text{C}$		10	20	–	

## DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 0.2\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	–	13	–	MHz			
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	$C_{ob}$	–	35	60	pF			
Input Capacitance ( $V_{EB} = 8.0\text{ V}$ )	$C_{ib}$	–	400	600	pF			
Dynamic Saturation:  determined 1.0 $\mu\text{s}$ and 3.0 $\mu\text{s}$ after rising $I_{B1}$ reach 0.9 final $I_{B1}$ (see Figure 18)	$I_C = 0.4\text{ A}$ $I_{B1} = 40\text{ mA}$ $V_{CC} = 300\text{ V}$	1.0 $\mu\text{s}$	@ $T_C = 125^\circ\text{C}$	$V_{CE(dsat)}$	–	3.5	–	Vdc
						–	8.0	–
	$I_C = 1.0\text{ A}$ $I_{B1} = 0.2\text{ A}$ $V_{CC} = 300\text{ V}$	3.0 $\mu\text{s}$	@ $T_C = 125^\circ\text{C}$		–	1.5	–	
						–	3.8	–
		1.0 $\mu\text{s}$	@ $T_C = 125^\circ\text{C}$		–	8.0	–	
						–	14	–
	3.0 $\mu\text{s}$	@ $T_C = 125^\circ\text{C}$		–	2.0	–		
					–	7.0	–	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle  $\leq 10\%$ .

(2) Proper strike and creepage distance must be provided.

# MJE18002

## ELECTRICAL CHARACTERISTICS – continued ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### SWITCHING CHARACTERISTICS: Resistive Load (D.C. $\leq 10\%$ , Pulse Width = 20 $\mu\text{s}$ )

Turn-On Time	$I_C = 0.4 \text{ Adc}$ $I_{B1} = 40 \text{ mAdc}$ $I_{B2} = 0.2 \text{ Adc}$ $V_{CC} = 300 \text{ V}$	@ $T_C = 125^\circ\text{C}$	$t_{on}$	–	200	300	ns
Turn-Off Time		@ $T_C = 125^\circ\text{C}$	$t_{off}$	–	1.2	2.5	$\mu\text{s}$
Turn-On Time	$I_C = 1.0 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$ $V_{CC} = 300 \text{ V}$	@ $T_C = 125^\circ\text{C}$	$t_{on}$	–	85	150	ns
Turn-Off Time		@ $T_C = 125^\circ\text{C}$	$t_{off}$	–	1.7	2.5	$\mu\text{s}$

### SWITCHING CHARACTERISTICS: Inductive Load ( $V_{clamp} = 300 \text{ V}$ , $V_{CC} = 15 \text{ V}$ , $L = 200 \mu\text{H}$ )

Fall Time	$I_C = 0.4 \text{ Adc}$ , $I_{B1} = 40 \text{ mAdc}$ , $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 125^\circ\text{C}$	$t_{fi}$	–	125	200	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	$t_{si}$	–	0.7	1.25	$\mu\text{s}$
Crossover Time		@ $T_C = 125^\circ\text{C}$	$t_c$	–	110	200	ns
Fall Time	$I_C = 1.0 \text{ Adc}$ , $I_{B1} = 0.2 \text{ Adc}$ , $I_{B2} = 0.5 \text{ Adc}$	@ $T_C = 125^\circ\text{C}$	$t_{fi}$	–	110	175	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	$t_{si}$	–	1.7	2.75	$\mu\text{s}$
Crossover Time		@ $T_C = 125^\circ\text{C}$	$t_c$	–	200	300	ns
Fall Time	$I_C = 0.4 \text{ Adc}$ , $I_{B1} = 50 \text{ mAdc}$ , $I_{B2} = 50 \text{ mAdc}$	@ $T_C = 125^\circ\text{C}$	$t_{fi}$	–	140	200	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	$t_{si}$	–	2.2	3.0	$\mu\text{s}$
Crossover Time		@ $T_C = 125^\circ\text{C}$	$t_c$	–	140	250	ns

TYPICAL STATIC CHARACTERISTICS

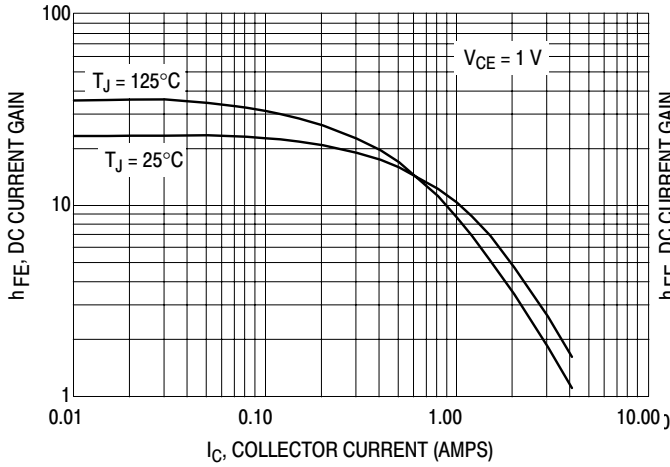


Figure 1. DC Current Gain @ 1 Volt

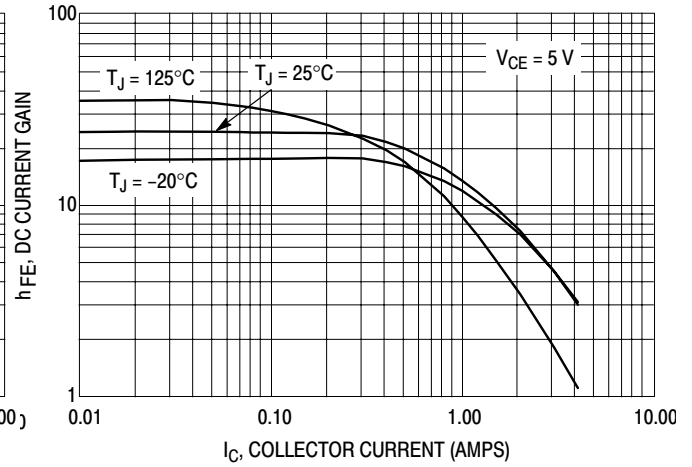


Figure 2. DC Current Gain @ 5 Volts

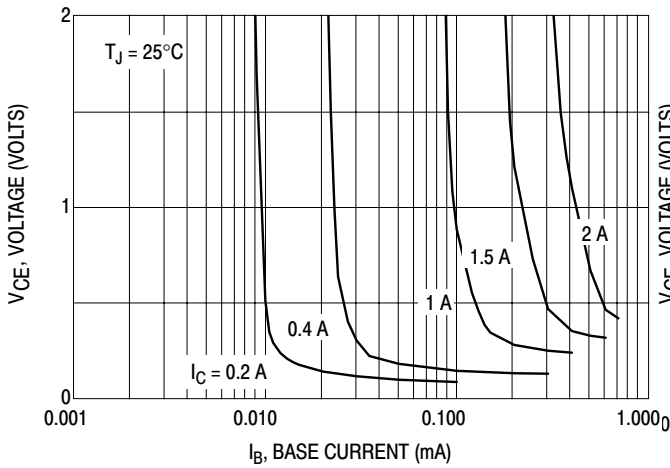


Figure 3. Collector Saturation Region

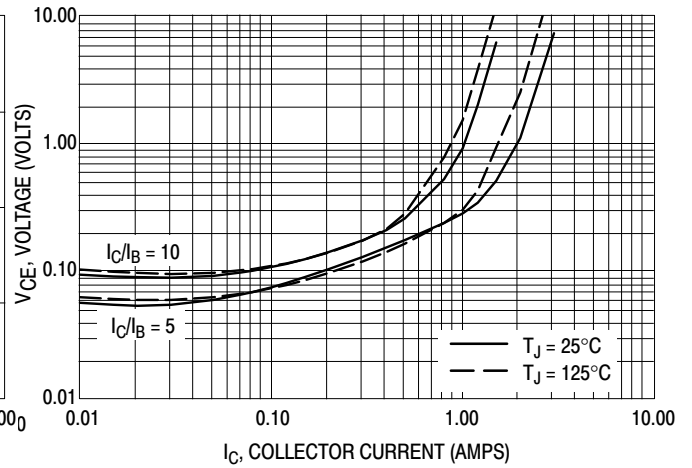


Figure 4. Collector-Emitter Saturation Voltage

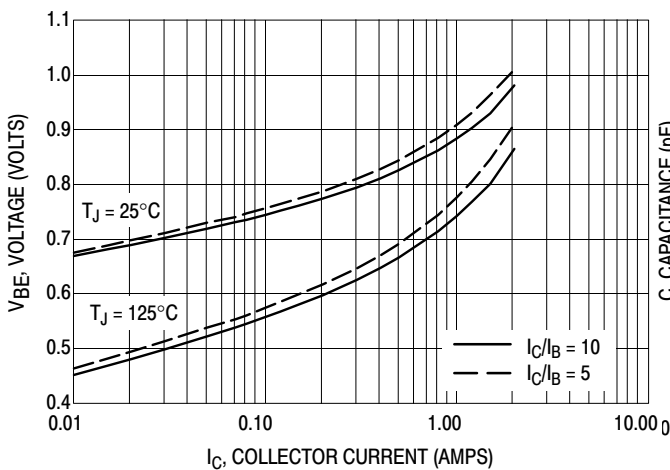


Figure 5. Base-Emitter Saturation Region

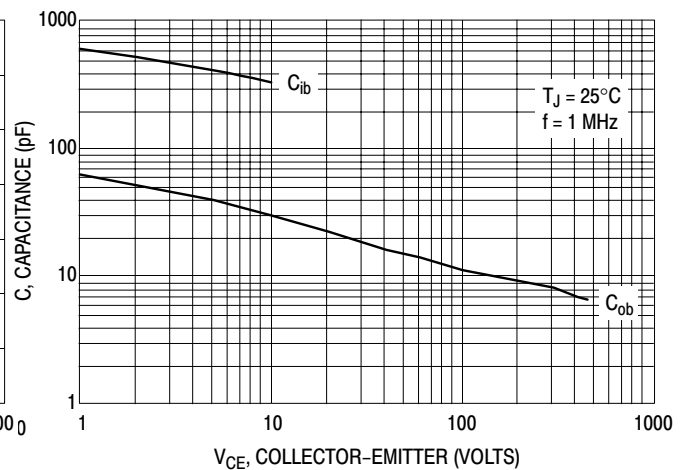


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

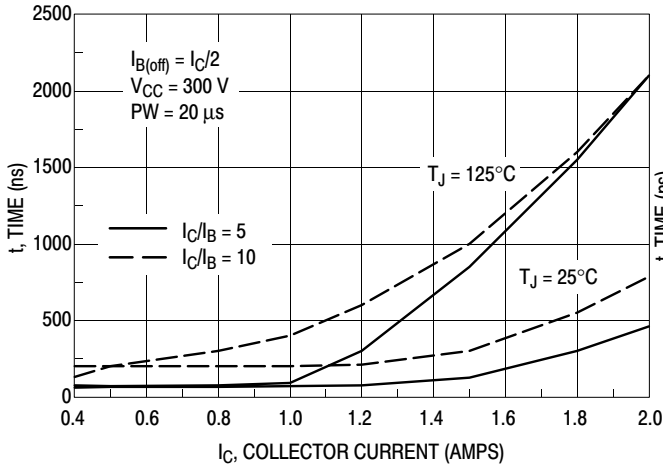


Figure 7. Resistive Switching,  $t_{on}$

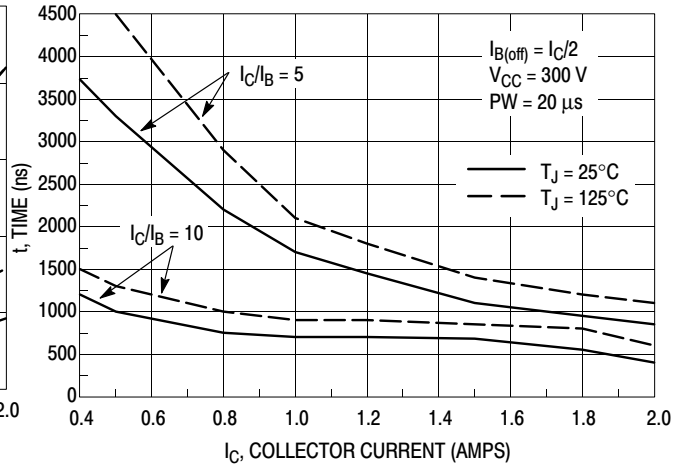


Figure 8. Resistive Switching,  $t_{off}$

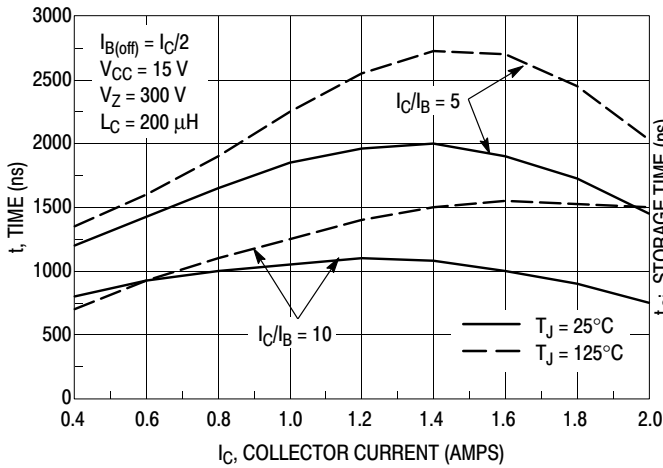


Figure 9. Inductive Storage Time,  $t_{si}$

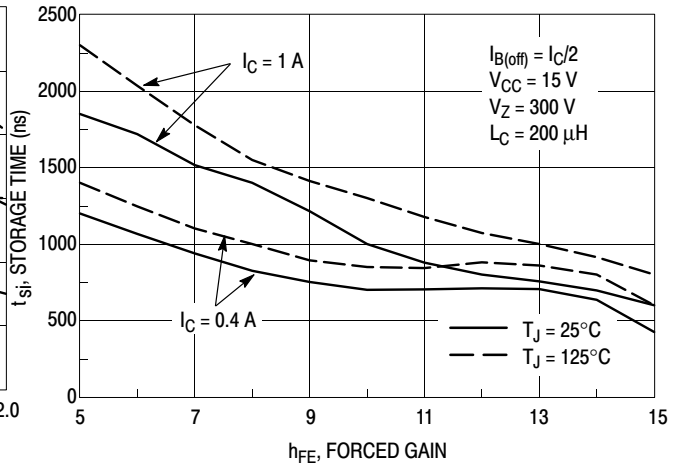


Figure 10. Inductive Storage Time

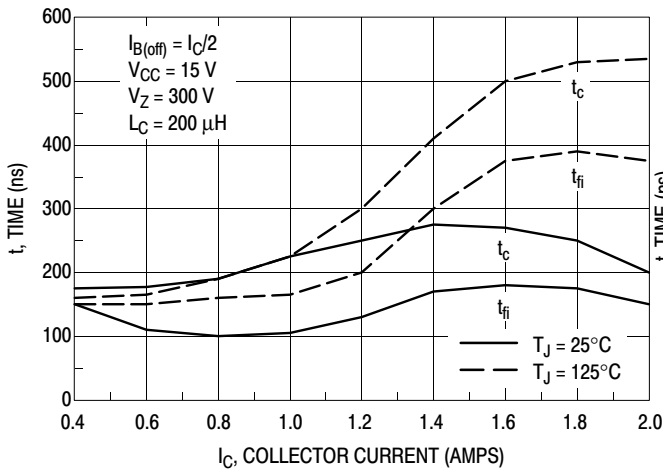


Figure 11. Inductive Switching,  $t_c$  and  $t_{fi}$ ,  $I_C/I_B = 5$

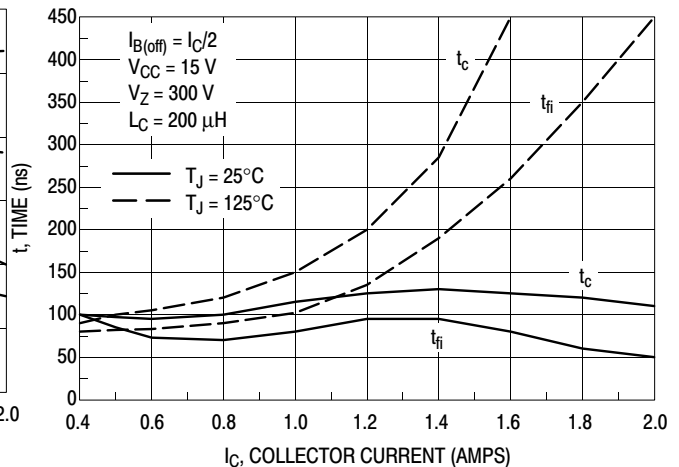


Figure 12. Inductive Switching,  $t_c$  and  $t_{fi}$ ,  $I_C/I_B = 10$

**TYPICAL SWITCHING CHARACTERISTICS**  
( $I_{B2} = I_C/2$  for all switching)

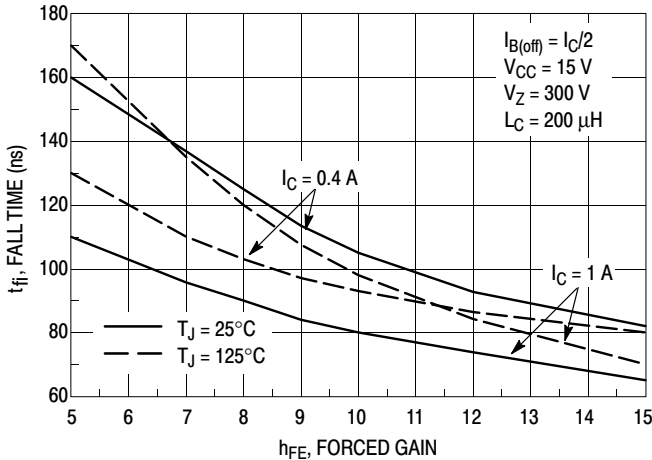


Figure 13. Inductive Fall Time

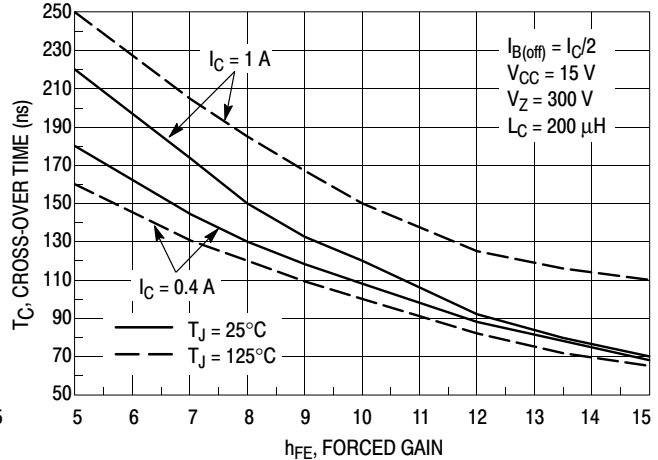


Figure 14. Inductive Crossover Time

**GUARANTEED SAFE OPERATING AREA INFORMATION**

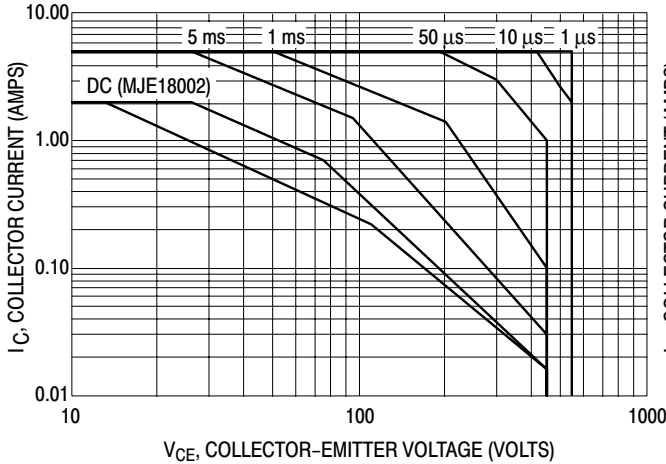


Figure 15. Forward Bias Safe Operating Area

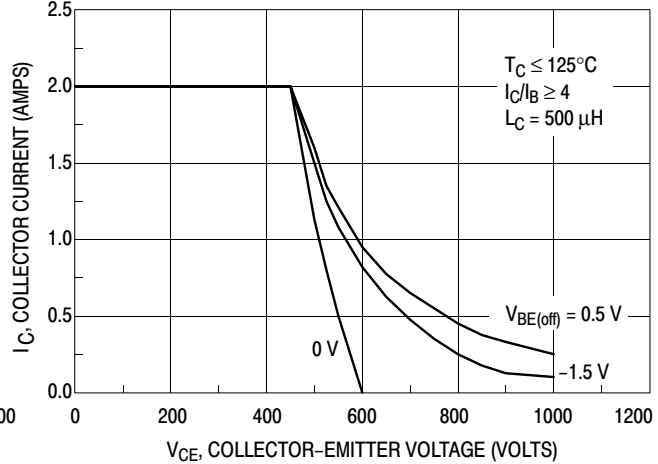


Figure 16. Reverse Bias Switching Safe Operating Area

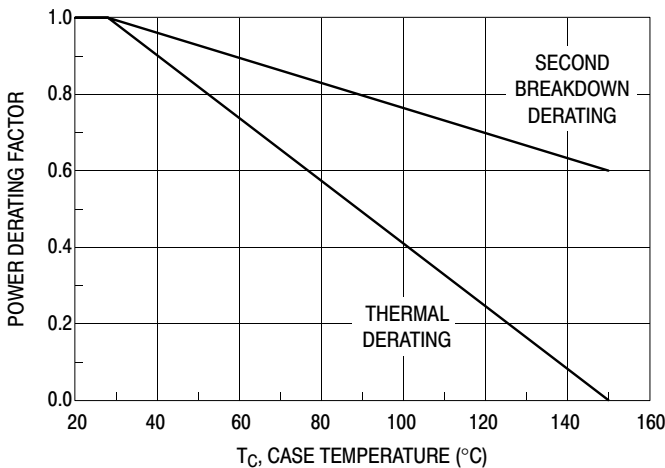


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on  $T_C = 25^\circ\text{C}$ ;  $T_J(\text{pk})$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.  $T_J(\text{pk})$  may be calculated from the data in Figures 20 and NO TAG. At any case temperatures, thermal limitations will reduce the power that can be handled to values less the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

# MJE18002

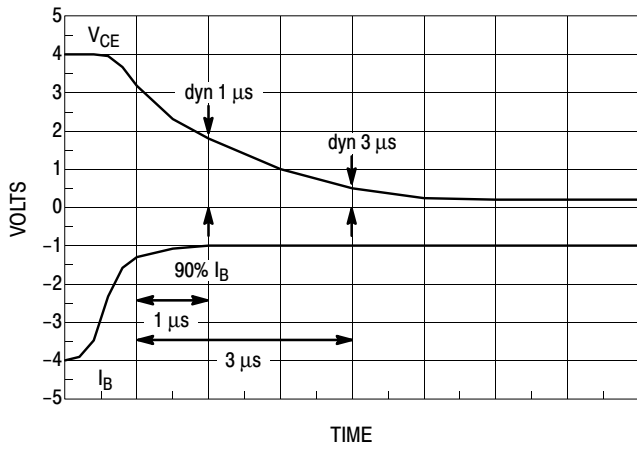


Figure 18. Dynamic Saturation Voltage Measurements

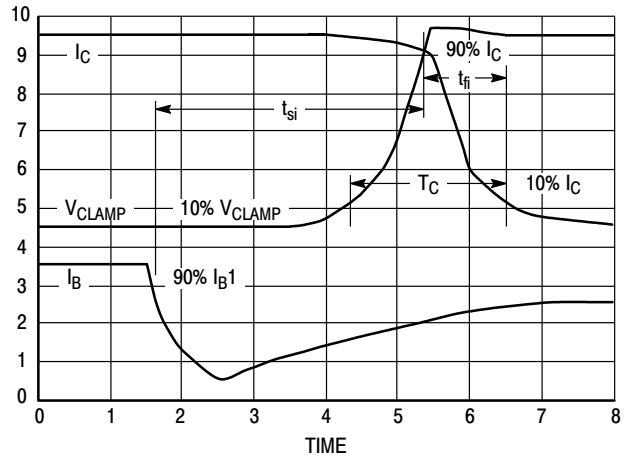
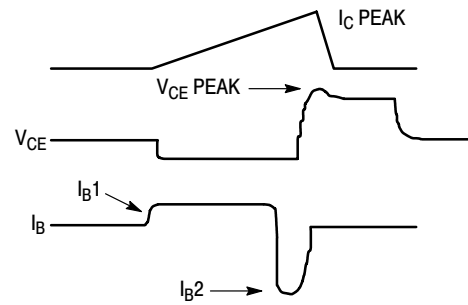
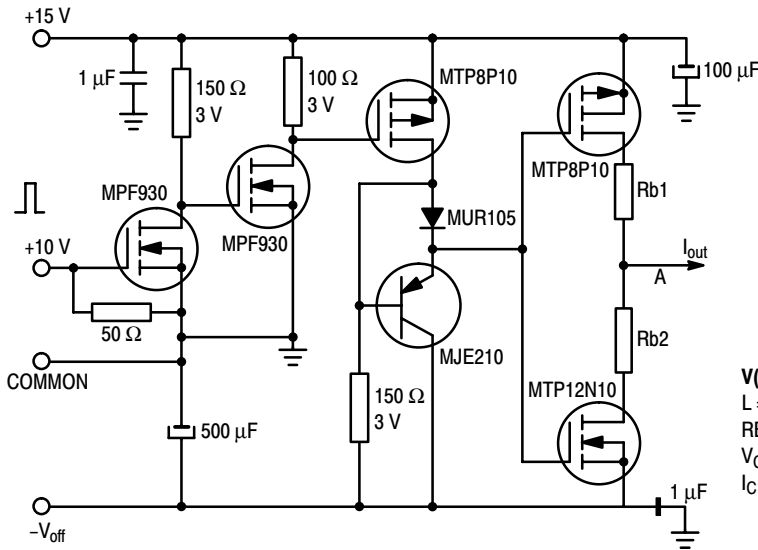


Figure 19. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 μH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
VCC = 20 VOLTS	VCC = 15 VOLTS	VCC = 15 VOLTS
IC(pk) = 100 mA	RB1 SELECTED FOR DESIRED IB1	RB1 SELECTED FOR DESIRED IB1

Table 1. Inductive Load Switching Drive Circuit

## TYPICAL THERMAL RESPONSE

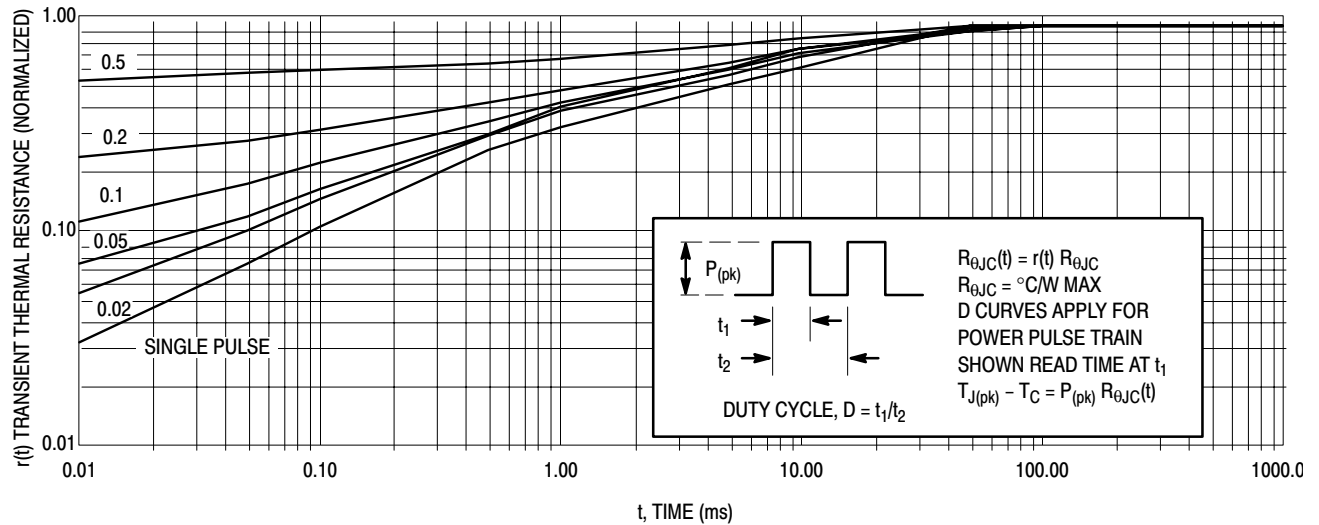


Figure 20. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for MJE18002



# High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

The MJE18004D2 is state-of-art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread ( $\pm 150$  ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an  $h_{FE}$  window.

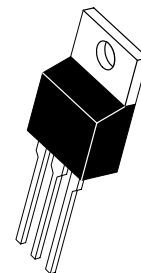
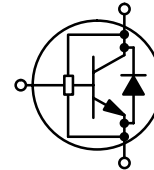
## Main features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @  $I_C = 100$  mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector-Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic  $V_{CE(sat)}$
- “6 Sigma” Process Providing Tight and Reproducible Parameter Spreads

It's characteristics make it also suitable for PFC application.

## MJE18004D2

POWER TRANSISTORS  
5 AMPERES  
1000 VOLTS  
75 WATTS



CASE 221A-09  
TO-220AB

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	450	Vdc
Collector-Base Breakdown Voltage	$V_{CBO}$	1000	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	1000	Vdc
Emitter-Base Voltage	$V_{EBO}$	12	Vdc
Collector Current — Continuous — Peak (1)	$I_C$ $I_{CM}$	5 10	Adc
Base Current — Continuous — Peak (1)	$I_B$ $I_{BM}$	2 4	Adc
*Total Device Dissipation @ $T_C = 25^\circ\text{C}$ *Derate above $25^\circ\text{C}$	$P_D$	75 0.6	Watt W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from case for 5 seconds	$T_L$	260	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq 10\%$ .

# MJE18004D2

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	450	547		Vdc
Collector–Base Breakdown Voltage ( $I_{CBO} = 1\text{ mA}$ )	$V_{CBO}$	1000	1100		Vdc
Emitter–Base Breakdown Voltage ( $I_{EBO} = 1\text{ mA}$ )	$V_{EBO}$	12	14		Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$			100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )  ( $V_{CE} = 500\text{ V}$ , $V_{EB} = 0$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$I_{CES}$		100 500 100	$\mu\text{Adc}$
Emitter–Cutoff Current ( $V_{EB} = 10\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$			100	$\mu\text{Adc}$

## ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 0.8\text{ Adc}$ , $I_B = 80\text{ mAdc}$ )  ( $I_C = 2\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{BE(sat)}$		0.8 0.7	1 0.9	Vdc
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.9 0.8	1 0.9	
Collector–Emitter Saturation Voltage ( $I_C = 0.8\text{ Adc}$ , $I_B = 80\text{ mAdc}$ )  ( $I_C = 2\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )  ( $I_C = 0.8\text{ Adc}$ , $I_B = 40\text{ mAdc}$ )  ( $I_C = 1\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(sat)}$		0.38 0.55	0.5 0.75	Vdc
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.45 0.75	0.75 1	
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.9 1.6	1.5	
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			0.25 0.28	0.5 0.6	
DC Current Gain ( $I_C = 0.8\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )  ( $I_C = 2\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )  ( $I_C = 1\text{ Adc}$ , $V_{CE} = 2.5\text{ Vdc}$ )	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$h_{FE}$	15 10	28 14		—
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		6 4	8 6		
	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		18 14	28 20		

## DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 1 $\mu\text{s}$ and 3 $\mu\text{s}$ respectively after rising $I_{B1}$ reaches 90% of final $I_{B1}$	$I_C = 1\text{ Adc}$ $I_{B1} = 100\text{ mA}$ $V_{CC} = 300\text{ V}$	@ 1 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(dsat)}$		9 16	V
		@ 3 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$			3.1 9	
	$I_C = 2\text{ Adc}$ $I_{B1} = 0.4\text{ A}$ $V_{CC} = 300\text{ V}$	@ 1 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		11 18		
		@ 3 $\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		1.4 8		

# MJE18004D2

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### DIODE CHARACTERISTICS

Forward Diode Voltage (I <sub>EC</sub> = 1 Adc)	@ T <sub>C</sub> = 25°C	V <sub>EC</sub>		0.96	1.5	V	
	@ T <sub>C</sub> = 125°C			0.72			
(I <sub>EC</sub> = 2 Adc)	@ T <sub>C</sub> = 25°C			1.15	1.7		
	@ T <sub>C</sub> = 125°C			0.8			
Forward Recovery Time (I <sub>F</sub> = 0.4 Adc, di/dt = 10 A/μs)	@ T <sub>C</sub> = 25°C	t <sub>fr</sub>		440		ns	
	(I <sub>F</sub> = 1 Adc, di/dt = 10 A/μs)			@ T <sub>C</sub> = 25°C			335
	(I <sub>F</sub> = 2 Adc, di/dt = 10 A/μs)			@ T <sub>C</sub> = 25°C			335

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1 MHz)	f <sub>T</sub>		13		MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1 MHz)	C <sub>ob</sub>		60	100	pF
Input Capacitance (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1 MHz)	C <sub>ib</sub>		450	750	pF

### SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)

Turn-on Time	I <sub>C</sub> = 2.5 Adc, I <sub>B1</sub> = 0.5 Adc I <sub>B2</sub> = 1 Adc V <sub>CC</sub> = 250 Vdc	@ T <sub>C</sub> = 25°C	t <sub>on</sub>		500	750	ns
Turn-off Time		@ T <sub>C</sub> = 25°C	t <sub>off</sub>	1.1		1.4	μs
Turn-on Time	I <sub>C</sub> = 2 Adc, I <sub>B1</sub> = 0.4 Adc I <sub>B2</sub> = 1 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C	t <sub>on</sub>		100	150	ns
Turn-off Time		@ T <sub>C</sub> = 125°C			150		
Turn-on Time	I <sub>C</sub> = 2.5 Adc, I <sub>B1</sub> = 0.5 Adc I <sub>B2</sub> = 0.5 Adc V <sub>CC</sub> = 300 Vdc	@ T <sub>C</sub> = 25°C	t <sub>on</sub>		120	150	ns
		@ T <sub>C</sub> = 125°C			500		
Turn-off Time		@ T <sub>C</sub> = 25°C	t <sub>off</sub>	1.85		2.15	μs
		@ T <sub>C</sub> = 125°C		2.6			

### SWITCHING CHARACTERISTICS: Inductive Load (V<sub>CC</sub> = 15 V)

Fall Time	I <sub>C</sub> = 2.5 Adc I <sub>B1</sub> = 500 mAcd I <sub>B2</sub> = 500 mAcd V <sub>Z</sub> = 350 V L <sub>C</sub> = 300 μH	@ T <sub>C</sub> = 25°C	t <sub>f</sub>		130	175	ns
		@ T <sub>C</sub> = 125°C			300		
Storage Time		@ T <sub>C</sub> = 25°C	t <sub>s</sub>		2.12	2.4	μs
		@ T <sub>C</sub> = 125°C			2.6		
Crossover Time		@ T <sub>C</sub> = 25°C	t <sub>c</sub>		355	500	ns
		@ T <sub>C</sub> = 125°C			750		
Fall Time	I <sub>C</sub> = 2 Adc I <sub>B1</sub> = 400 mAcd I <sub>B2</sub> = 400 mAcd V <sub>Z</sub> = 300 V L <sub>C</sub> = 200 μH	@ T <sub>C</sub> = 25°C	t <sub>f</sub>		95	150	ns
		@ T <sub>C</sub> = 125°C			230		
Storage Time		@ T <sub>C</sub> = 25°C	t <sub>s</sub>	2.1		2.4	μs
		@ T <sub>C</sub> = 125°C			2.9		
Crossover Time		@ T <sub>C</sub> = 25°C	t <sub>c</sub>		300	450	ns
		@ T <sub>C</sub> = 125°C			700		
Fall Time	I <sub>C</sub> = 1 Adc I <sub>B1</sub> = 100 mAcd I <sub>B2</sub> = 500 mAcd V <sub>Z</sub> = 300 V L <sub>C</sub> = 200 μH	@ T <sub>C</sub> = 25°C	t <sub>f</sub>		70	90	ns
		@ T <sub>C</sub> = 125°C			100		
Storage Time		@ T <sub>C</sub> = 25°C	t <sub>s</sub>		0.7	0.9	μs
		@ T <sub>C</sub> = 125°C			1.05		
Crossover Time		@ T <sub>C</sub> = 25°C	t <sub>c</sub>		75	120	ns
		@ T <sub>C</sub> = 125°C			160		

TYPICAL STATIC CHARACTERISTICS

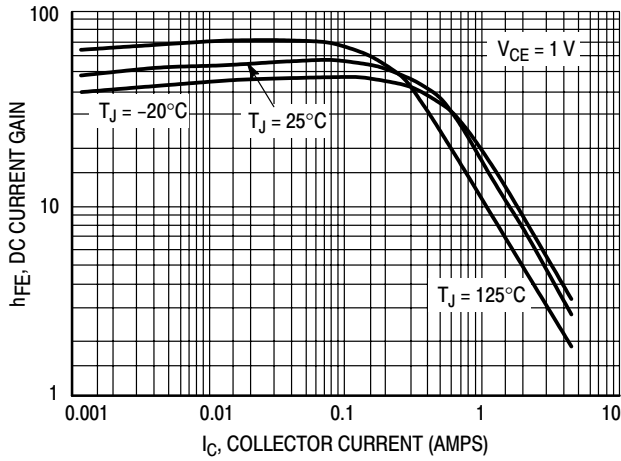


Figure 1. DC Current Gain @ 1 Volt

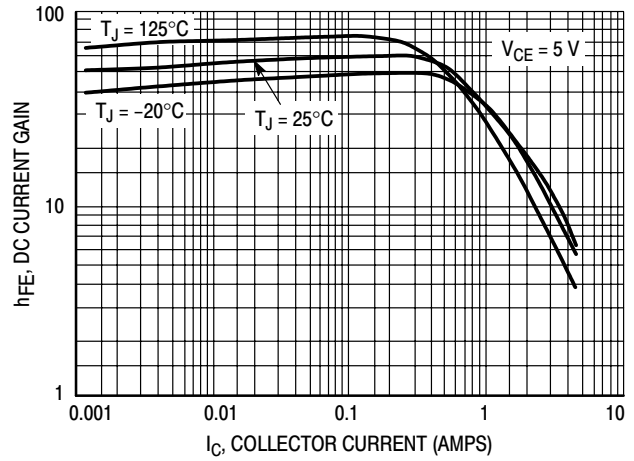


Figure 2. DC Current Gain @ 5 Volt

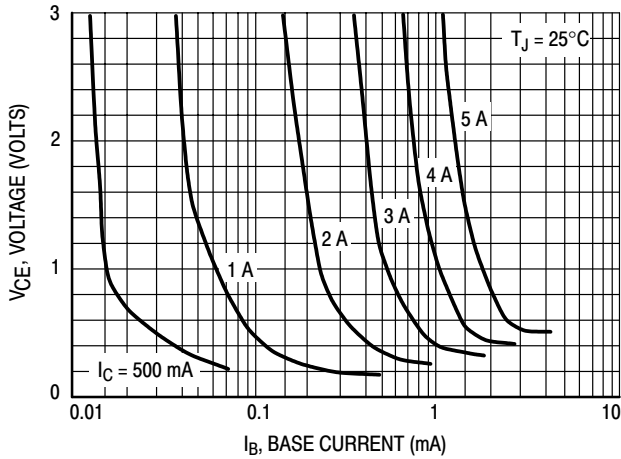


Figure 3. Collector Saturation Region

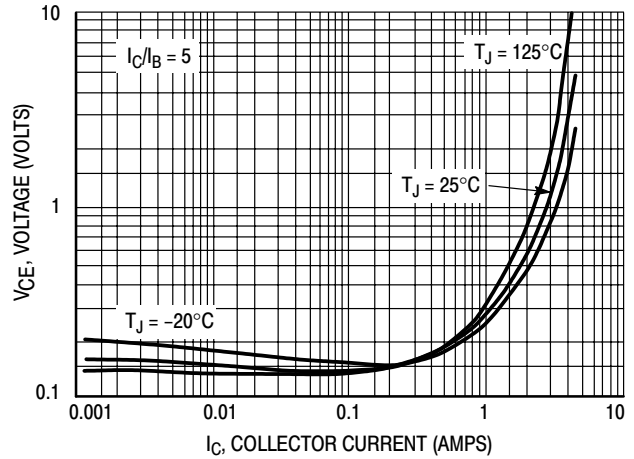


Figure 4. Collector-Emitter Saturation Voltage

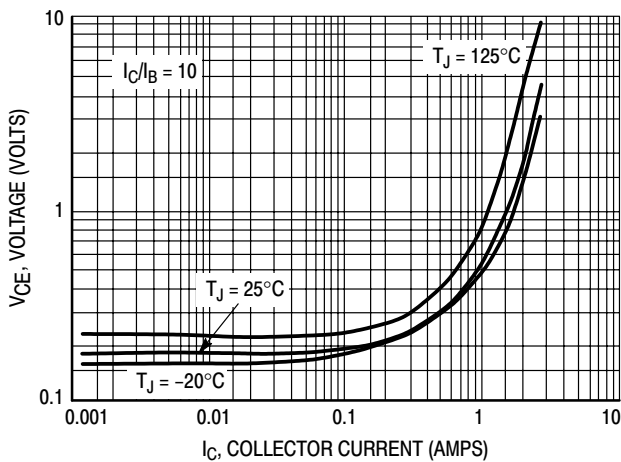


Figure 5. Collector-Emitter Saturation Voltage

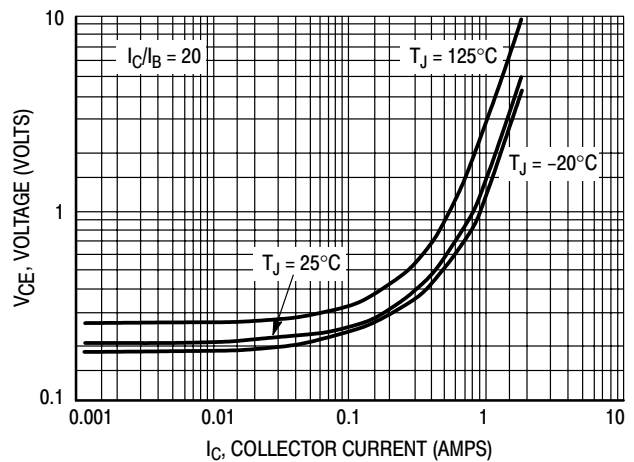


Figure 6. Collector-Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

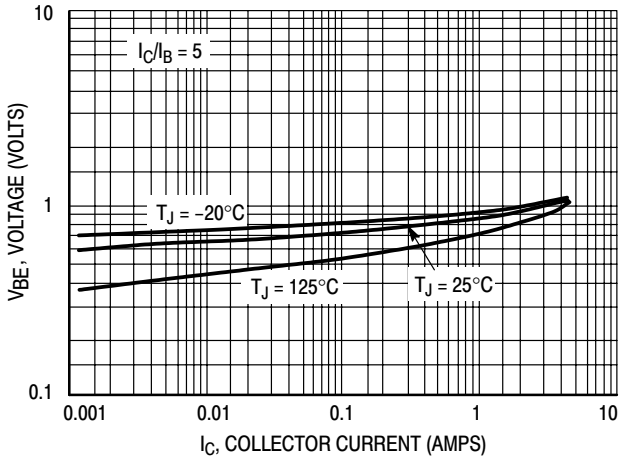


Figure 7. Base-Emitter Saturation Region

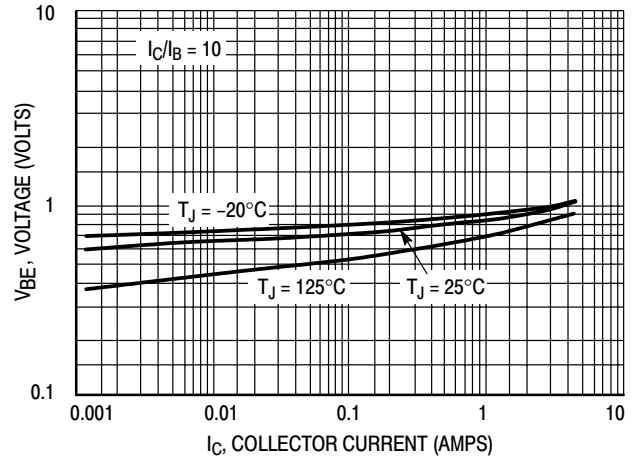


Figure 8. Base-Emitter Saturation Region

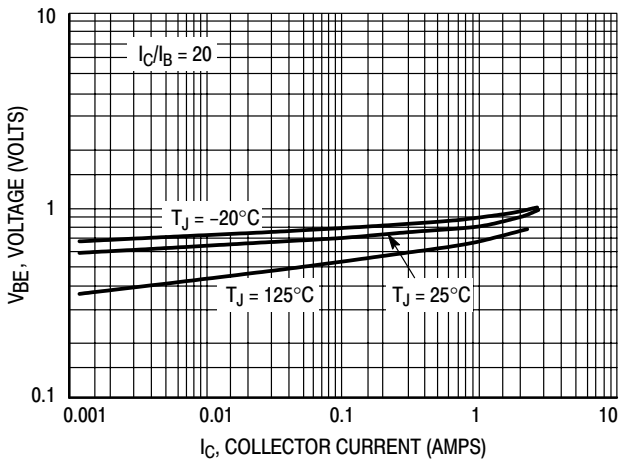


Figure 9. Base-Emitter Saturation Region

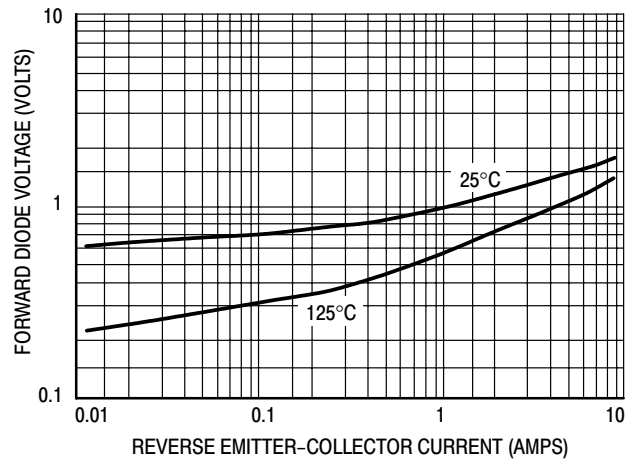


Figure 10. Forward Diode Voltage

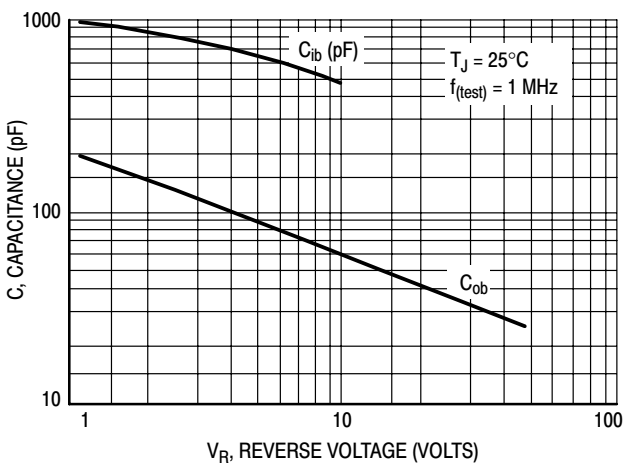


Figure 11. Capacitance

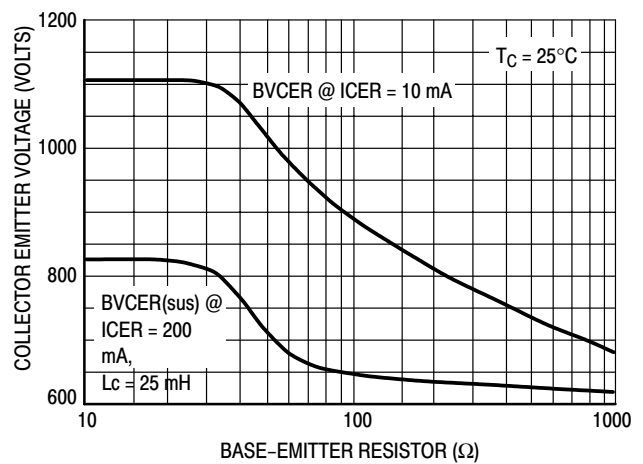


Figure 12. BVCER = f(R<sub>BE</sub>)

TYPICAL SWITCHING CHARACTERISTICS

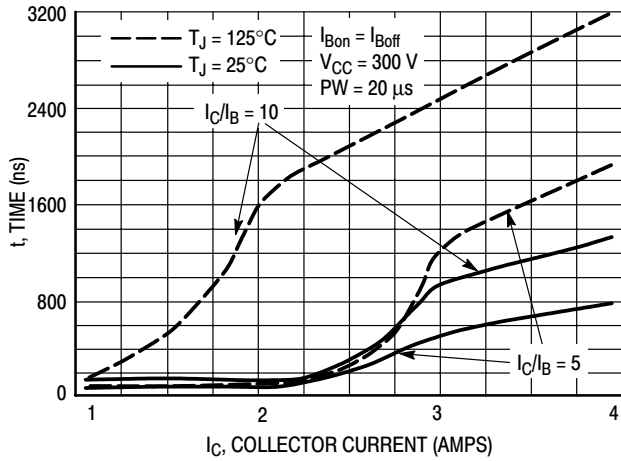


Figure 13. Resistive Switch Time,  $t_{on}$

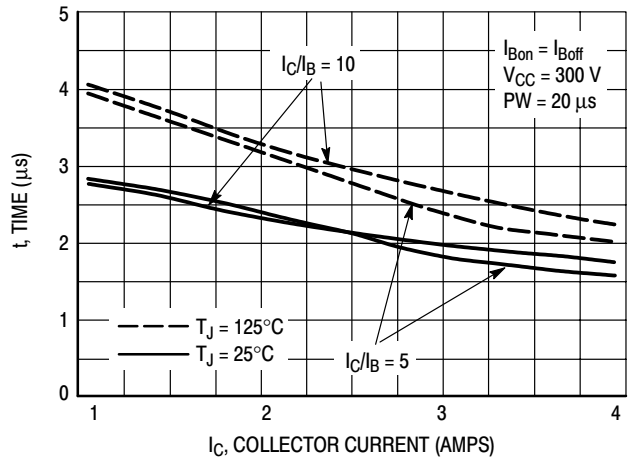


Figure 14. Resistive Switch Time,  $t_{off}$

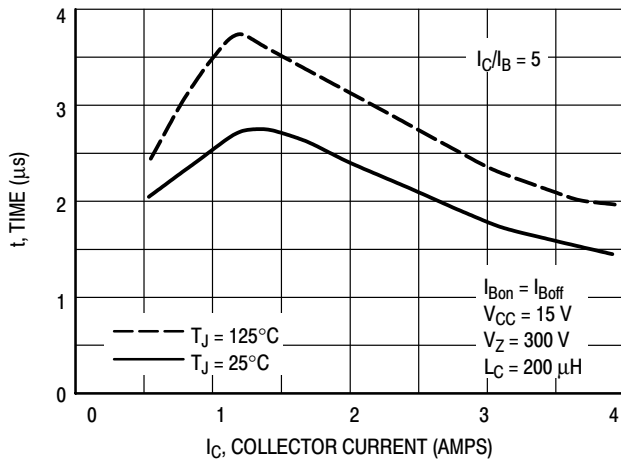


Figure 15. Inductive Storage Time,  $t_{si}$  @  $I_C/I_B = 5$

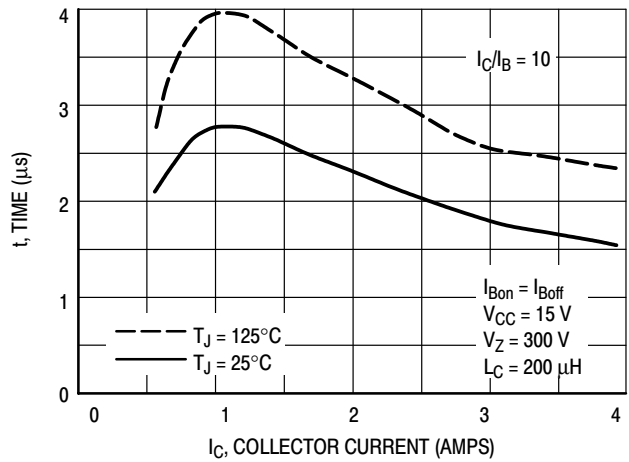


Figure 16. Inductive Storage Time,  $t_{si}$  @  $I_C/I_B = 10$

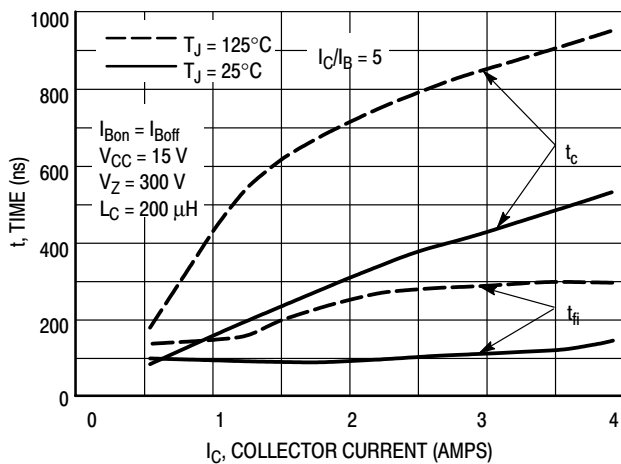


Figure 17. Inductive Switching Time,  $t_c$  and  $t_{fi}$  @  $I_C/I_B = 5$

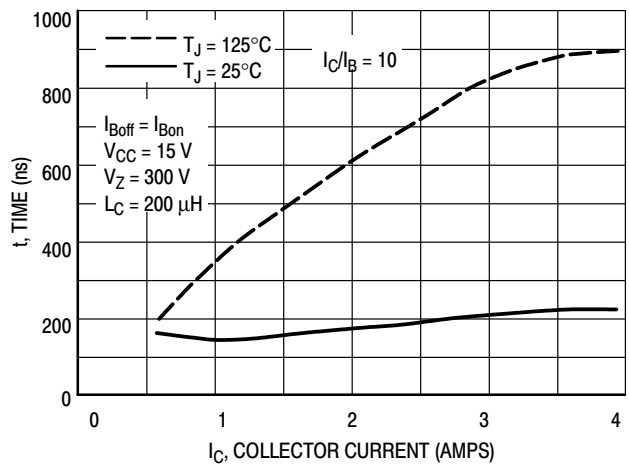


Figure 18. Inductive Switching Time,  $t_{fi}$  @  $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS

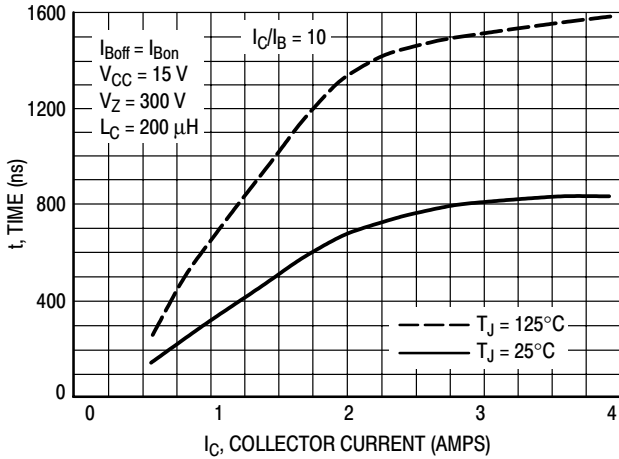


Figure 19. Inductive Switching,  $t_c$  @  $I_C/I_B = 10$

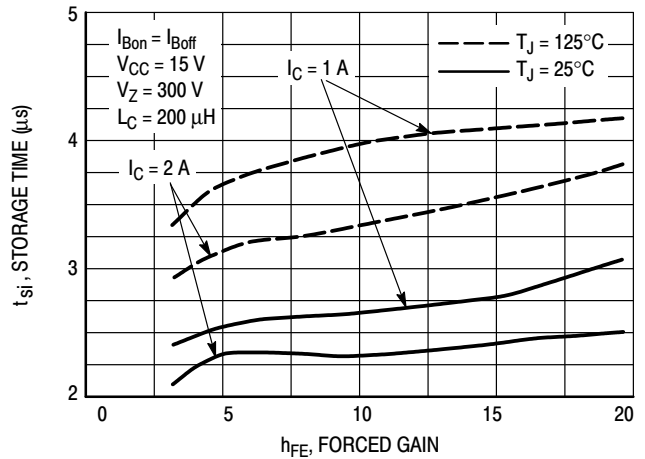


Figure 20. Inductive Storage Time

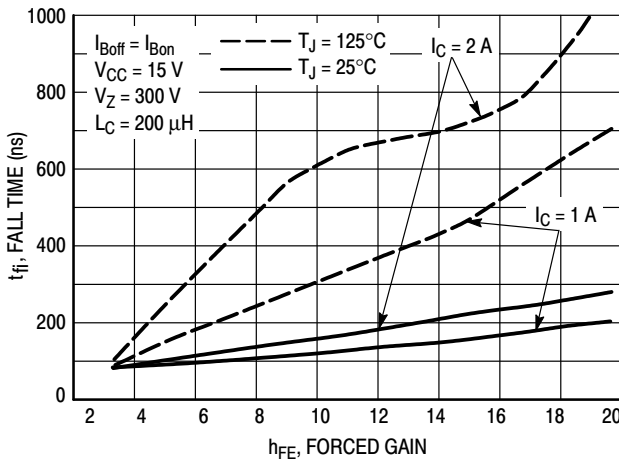


Figure 21. Inductive Fall Time

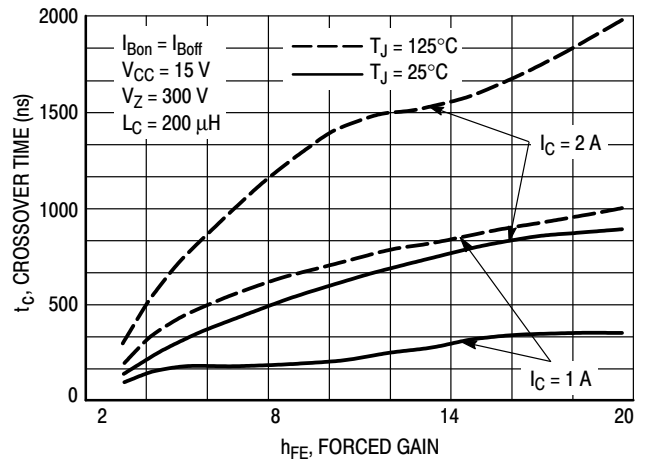


Figure 22. Inductive Crossover Time

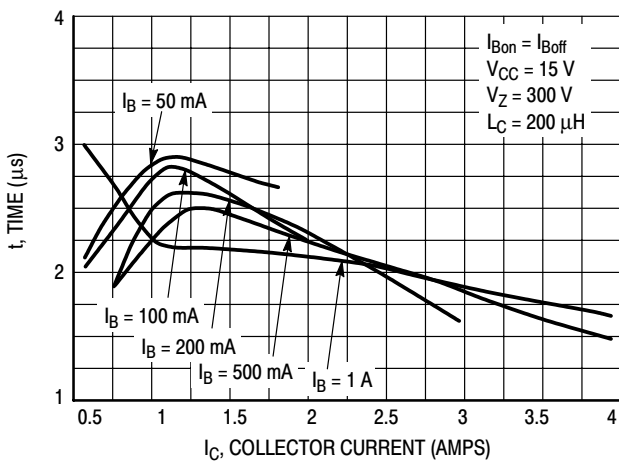


Figure 23. Inductive Storage Time,  $t_{si}$

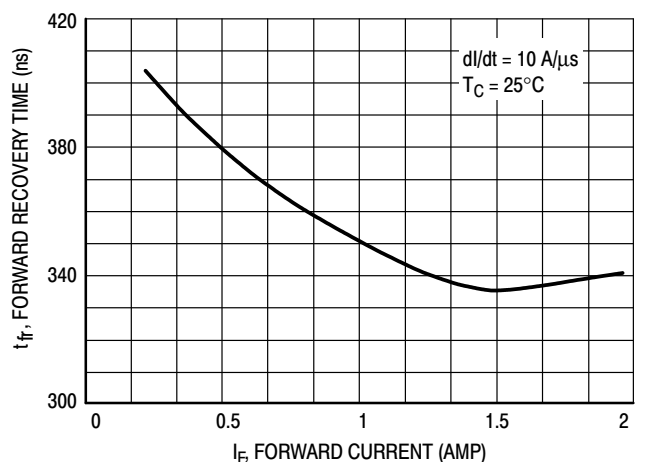


Figure 24. Forward Recovery Time,  $T_{FR}$

TYPICAL SWITCHING CHARACTERISTICS

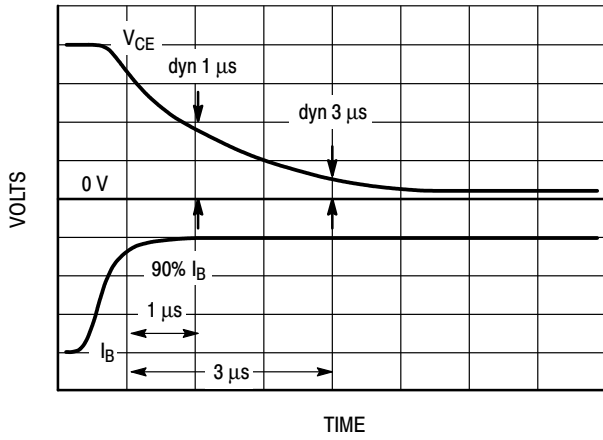


Figure 25. Dynamic Saturation Voltage Measurements

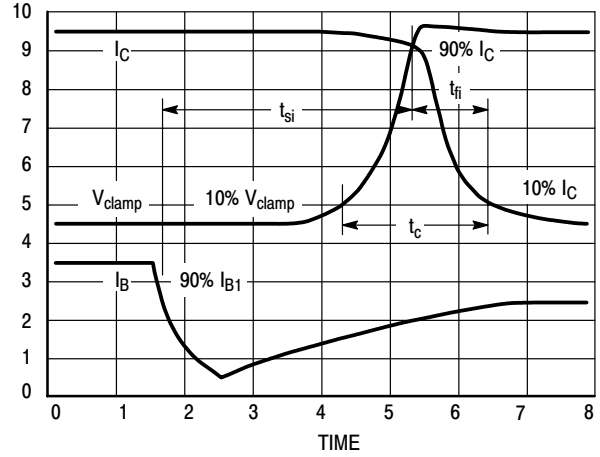


Figure 26. Inductive Switching Measurements

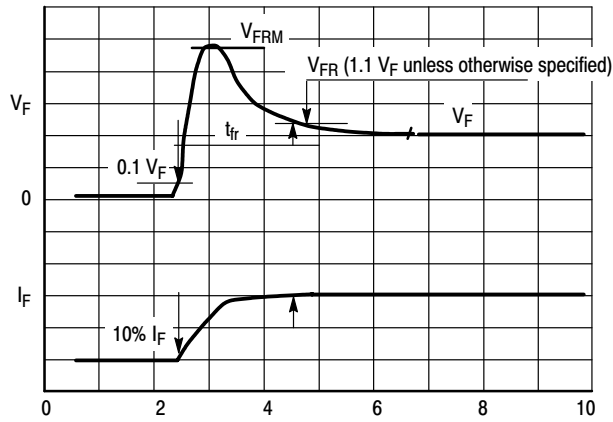


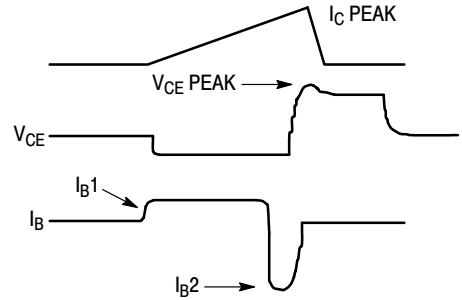
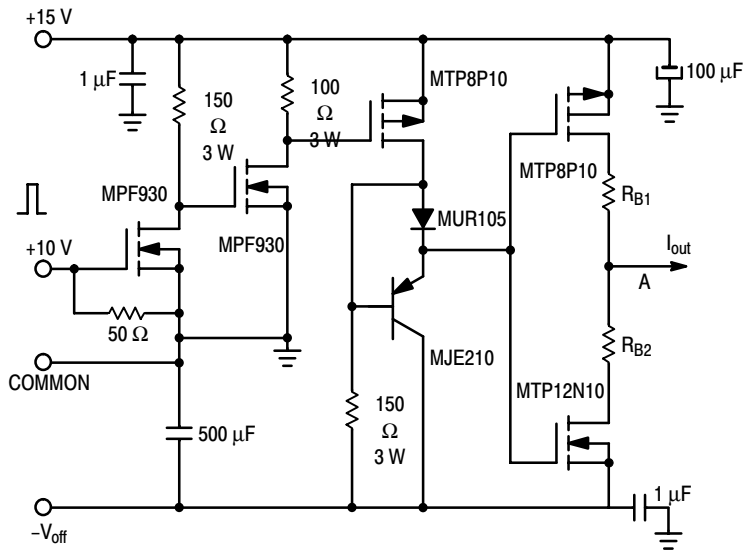
Figure 27.  $t_{fr}$  Measurements



# MJE18004D2

## TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



$V_{(BR)CEO(sus)}$   
 $L = 10 \text{ mH}$   
 $RB2 = \infty$   
 $V_{CC} = 20 \text{ Volts}$   
 $I_{C(pk)} = 100 \text{ mA}$

**Inductive Switching**  
 $L = 200 \mu\text{H}$   
 $RB2 = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $RB1$  selected for  
 desired  $I_{B1}$

**RBSOA**  
 $L = 500 \mu\text{H}$   
 $RB2 = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $RB1$  selected for  
 desired  $I_{B1}$

## TYPICAL CHARACTERISTICS

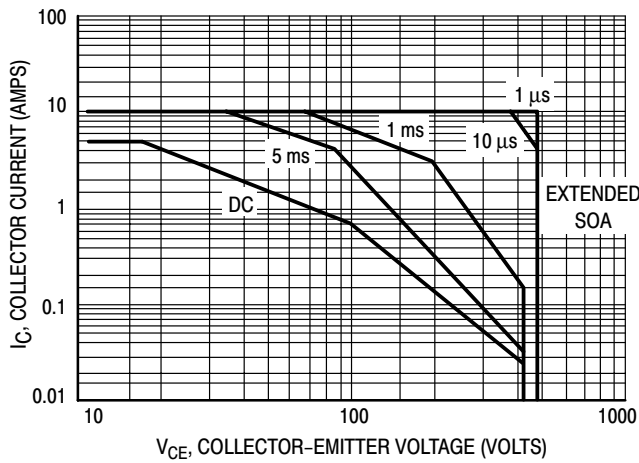


Figure 28. Forward Bias Safe Operating Area

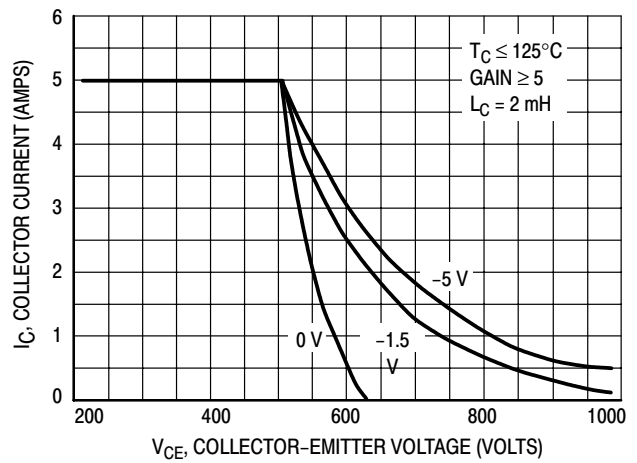


Figure 29. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

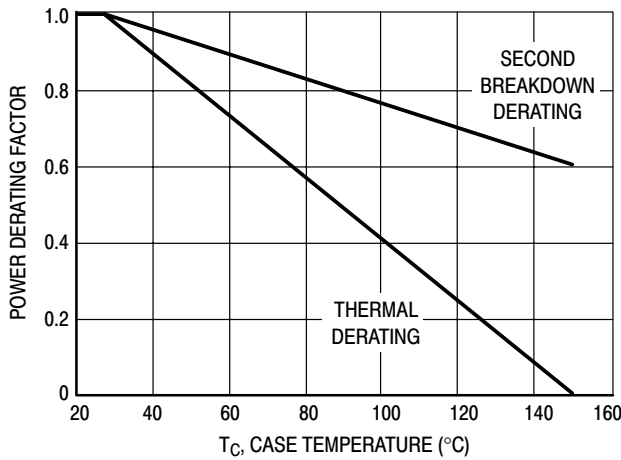


Figure 30. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C-V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on  $T_C = 25^\circ\text{C}$ ;  $T_J(\text{pk})$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

$T_J(\text{pk})$  may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse biased. The safe level is specified as a reverse-biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

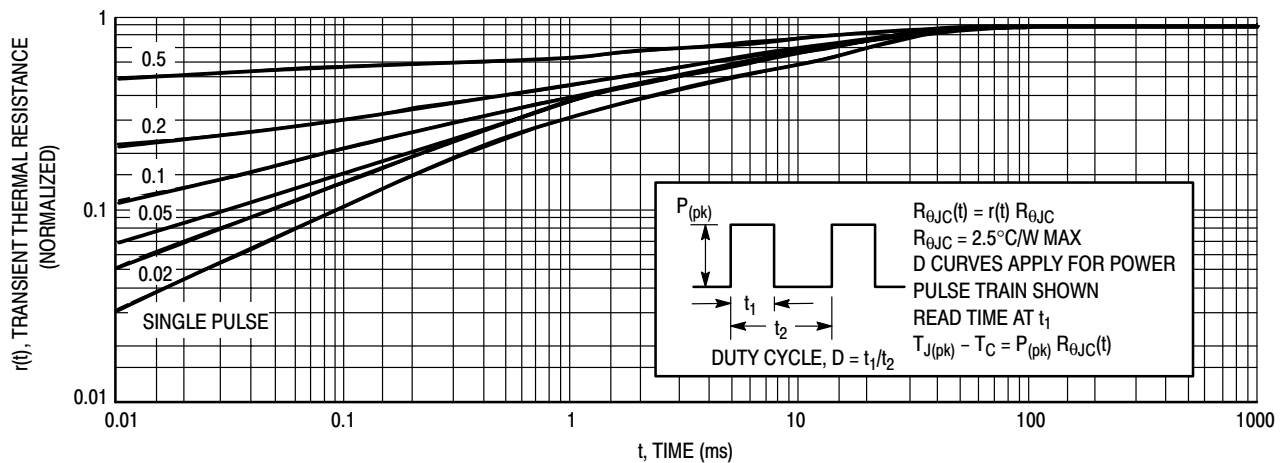


Figure 31. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for MJE18004D2

# SWITCHMODE™

## NPN Bipolar Power Transistor

### For Switching Power Supply Applications

The MJE/MJF18004 have an applications specific state-of-the-art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. This high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain  $h_{FE}$
  - Fast Switching
  - No Coil Required in Base Circuit for Turn-Off (No Current Tail)
- Full Characterization at 125°C
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions
- Two Package Choices: Standard TO-220 or Isolated TO-220
- MJF18004, Case 221D, is UL Recognized at 3500 V<sub>RMS</sub>: File #E69369

#### MAXIMUM RATINGS

Rating	Symbol	MJE18004	MJF18004	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	450		Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	1000		Vdc
Emitter-Base Voltage	$V_{EBO}$	9.0		Vdc
Collector Current — Continuous	$I_C$	5.0		Adc
— Peak(1)	$I_{CM}$	10		
Base Current — Continuous	$I_B$	2.0		Adc
— Peak(1)	$I_{BM}$	4.0		
RMS Isolation Voltage(2) Test No. 1 Per Fig. 22a	$V_{ISOL}$	—	4500	Volts
(for 1 sec, R.H. Test No. 2 Per Fig. 22b		—	3500	
< 30%, $T_A = 25^\circ\text{C}$ ) Test No. 3 Per Fig. 22c		—	1500	
Total Device Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_D$	75	35	Watts
Derate above 25°C		0.6	0.28	W/°C
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150		°C

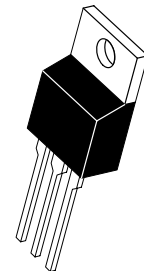
#### THERMAL CHARACTERISTICS

Rating	Symbol	MJE18004	MJF18004	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.65	3.55	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	62.5	
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	260		°C

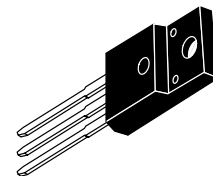
**MJE18004 \***  
**MJF18004 \***

\*ON Semiconductor Preferred Device

**POWER TRANSISTOR**  
**5.0 AMPERES**  
**1000 VOLTS**  
**35 and 75 WATTS**



**CASE 221A-09**  
**TO-220AB**  
**MJE18004**



**CASE 221D-02**  
**ISOLATED TO-220 TYPE**  
**MJF18004**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJE18004 MJF18004

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$	—	—	100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )	$I_{CES}$	—	—	100	$\mu\text{Adc}$
( $T_C = 25^\circ\text{C}$ )		—	—	500	
( $T_C = 125^\circ\text{C}$ )		—	—	100	
( $V_{CE} = 800\text{ V}$ , $V_{EB} = 0$ )	( $T_C = 125^\circ\text{C}$ )	—	—	100	
Emitter Cutoff Current ( $V_{EB} = 9.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	100	$\mu\text{Adc}$

## ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ ) ( $I_C = 2.0\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )	$V_{BE(sat)}$	— —	0.82 0.92	1.1 1.25	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )	$V_{CE(sat)}$	—	0.25	0.5	Vdc
( $T_C = 125^\circ\text{C}$ )		—	0.29	0.6	
( $I_C = 2.0\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )		—	0.3	0.45	
( $T_C = 125^\circ\text{C}$ )		—	0.36	0.8	
( $I_C = 2.5\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ )	—	0.5	0.75		
DC Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 2.5\text{ Vdc}$ )	$h_{FE}$	12	21	—	—
( $T_C = 125^\circ\text{C}$ )		—	20	—	
( $I_C = 0.3\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ )		14	—	34	
( $T_C = 125^\circ\text{C}$ )		—	32	—	
( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )		6.0	11	—	
( $T_C = 125^\circ\text{C}$ )	—	7.5	—		
( $I_C = 10\text{ mAdc}$ , $V_{CE} = 5.0\text{ Vdc}$ )	10	22	—		

## DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	—	13	—	MHz			
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	$C_{ob}$	—	50	65	pF			
Input Capacitance ( $V_{EB} = 8.0\text{ V}$ )	$C_{ib}$	—	800	1000	pF			
Dynamic Saturation Voltage:  Determined 1.0 $\mu\text{s}$ and 3.0 $\mu\text{s}$ respectively after rising $I_{B1}$ reaches 90% of final $I_{B1}$ (see Figure 18)	$V_{CE(dsat)}$	( $I_C = 1.0\text{ Adc}$ $I_{B1} = 100\text{ mAdc}$ $V_{CC} = 300\text{ V}$ )	1.0 $\mu\text{s}$	( $T_C = 125^\circ\text{C}$ )	—	6.8	—	Vdc
—			3.0 $\mu\text{s}$	( $T_C = 125^\circ\text{C}$ )	—	14	—	
( $I_C = 2.0\text{ Adc}$ $I_{B1} = 400\text{ mAdc}$ $V_{CC} = 300\text{ V}$ )		1.0 $\mu\text{s}$	( $T_C = 125^\circ\text{C}$ )	—	11.3	—		
				—	15.5	—		
		3.0 $\mu\text{s}$	( $T_C = 125^\circ\text{C}$ )	—	1.3	—		
				—	6.1	—		

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle  $\leq$  10%.

(2) Proper strike and creepage distance must be provided.

(continued)

# MJE18004 MJF18004

## ELECTRICAL CHARACTERISTICS — continued ( $T_C = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
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### SWITCHING CHARACTERISTICS: Resistive Load (D.C. $\leq 10\%$ , Pulse Width = 20 $\mu\text{s}$ )

Turn-On Time	( $I_C = 1.0 \text{ Adc}$ , $I_{B1} = 0.1 \text{ Adc}$ , $I_{B2} = 0.5 \text{ Adc}$ , $V_{CC} = 300 \text{ V}$ ) ( $T_C = 125^\circ\text{C}$ )	$t_{on}$	—	210 180	300 —	ns	
Turn-Off Time		( $T_C = 125^\circ\text{C}$ )	$t_{off}$	—	1.0 1.3	1.7 —	$\mu\text{s}$
Turn-On Time	( $I_C = 2.0 \text{ Adc}$ , $I_{B1} = 0.4 \text{ Adc}$ , $I_{B1} = 1.0 \text{ Adc}$ , $V_{CC} = 300 \text{ V}$ ) ( $T_C = 125^\circ\text{C}$ )	$t_{on}$	—	75 90	110 —	ns	
Turn-Off Time		( $T_C = 125^\circ\text{C}$ )	$t_{off}$	—	1.5 1.8	2.5 —	$\mu\text{s}$
Turn-On Time	( $I_C = 2.5 \text{ Adc}$ , $I_{B1} = 0.5 \text{ Adc}$ , $I_{B2} = 0.5 \text{ Adc}$ , $V_{CC} = 250 \text{ V}$ ) ( $T_C = 125^\circ\text{C}$ )	$t_{on}$	—	450 900	800 1400	ns	
Storage Time		( $T_C = 125^\circ\text{C}$ )	$t_s$	—	2.0 2.2	3.0 3.5	$\mu\text{s}$
Fall Time		( $T_C = 125^\circ\text{C}$ )	$t_f$	—	275 500	400 800	ns

### SWITCHING CHARACTERISTICS: Inductive Load ( $V_{clamp} = 300 \text{ V}$ , $V_{CC} = 15 \text{ V}$ , $L = 200 \mu\text{H}$ )

Fall Time	( $I_C = 1.0 \text{ Adc}$ , $I_{B1} = 0.1 \text{ Adc}$ , $I_{B2} = 0.5 \text{ Adc}$ ) ( $T_C = 125^\circ\text{C}$ )	$t_{fi}$	—	100 100	150 —	ns	
Storage Time		( $T_C = 125^\circ\text{C}$ )	$t_{si}$	—	1.1 1.4	1.7 —	$\mu\text{s}$
Crossover Time		( $T_C = 125^\circ\text{C}$ )	$t_c$	—	180 160	250 —	ns
Fall Time	( $I_C = 2.0 \text{ Adc}$ , $I_{B1} = 0.4 \text{ Adc}$ , $I_{B2} = 1.0 \text{ Adc}$ ) ( $T_C = 125^\circ\text{C}$ )	$t_{fi}$	—	90 150	175 —	ns	
Storage Time		( $T_C = 125^\circ\text{C}$ )	$t_{si}$	—	1.7 2.2	2.5 —	$\mu\text{s}$
Crossover Time		( $T_C = 125^\circ\text{C}$ )	$t_c$	—	180 250	300 —	ns
Fall Time	( $I_C = 2.5 \text{ Adc}$ , $I_{B1} = 0.5 \text{ Adc}$ , $I_{B2} = 0.5 \text{ Adc}$ , $V_{BE(off)} = -5.0 \text{ Vdc}$ ) ( $T_C = 125^\circ\text{C}$ )	$t_{fi}$	—	70 100	130 175	ns	
Storage Time		( $T_C = 125^\circ\text{C}$ )	$t_{si}$	—	0.75 1.0	1.0 1.3	$\mu\text{s}$
Crossover Time		( $T_C = 125^\circ\text{C}$ )	$t_c$	—	250 250	350 500	ns

TYPICAL STATIC CHARACTERISTICS

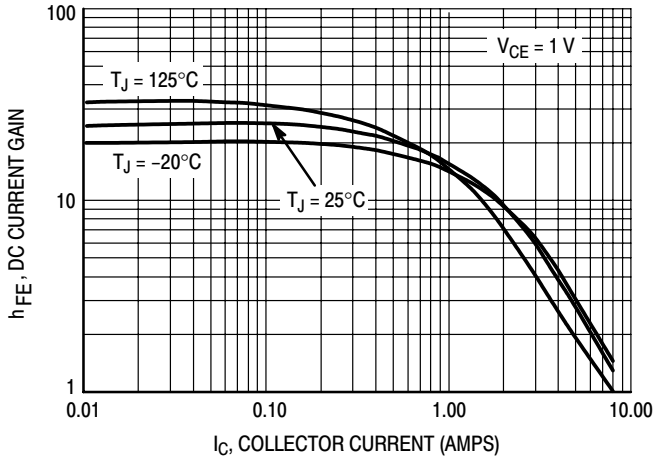


Figure 1. DC Current Gain @ 1 Volt

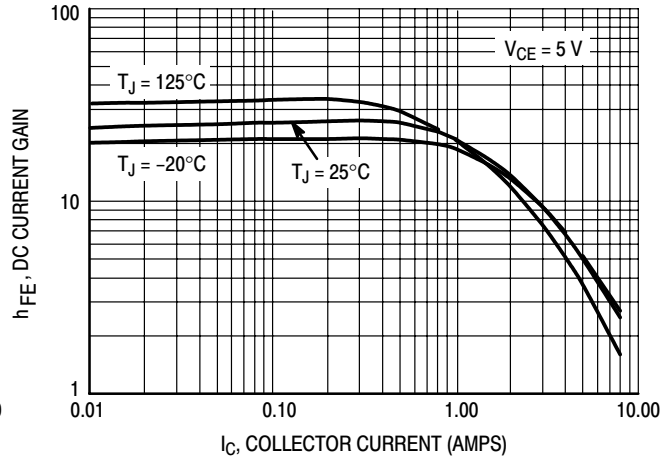


Figure 2. DC Current Gain @ 5 Volts

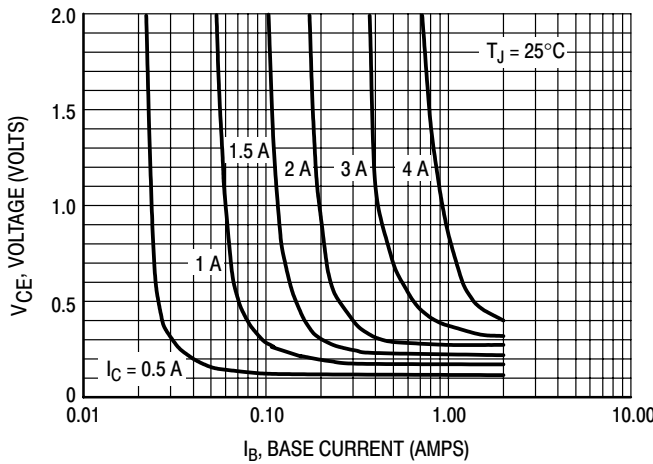


Figure 3. Collector Saturation Region

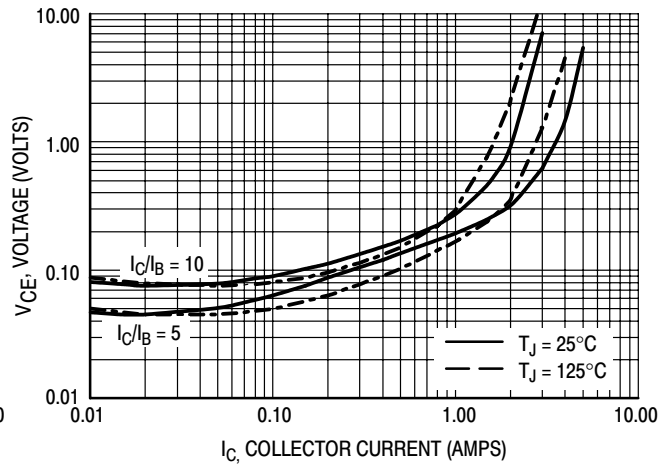


Figure 4. Collector-Emitter Saturation Voltage

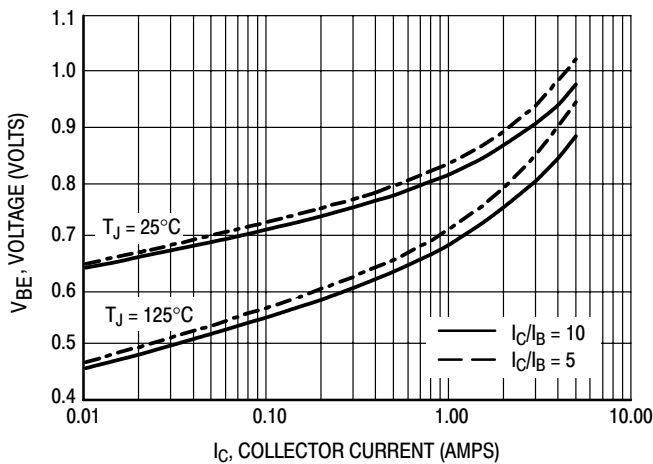


Figure 5. Base-Emitter Saturation Region

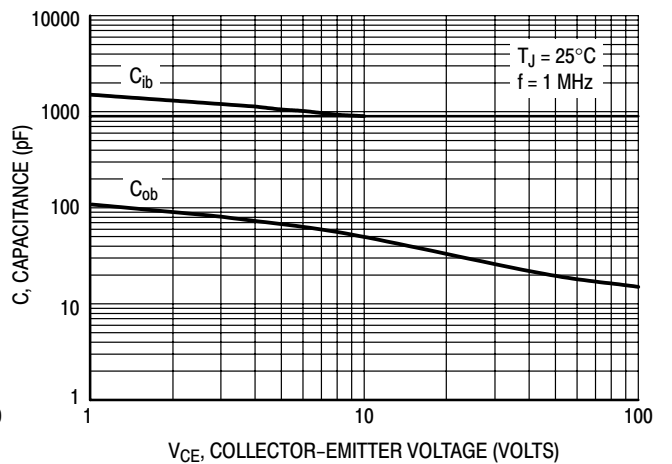


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

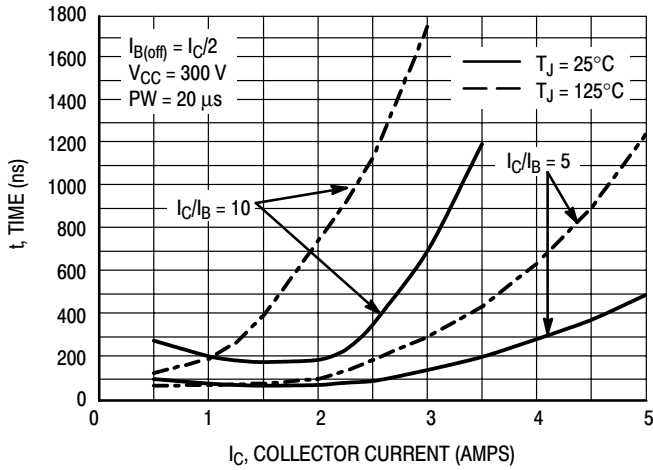


Figure 7. Resistive Switching,  $t_{on}$

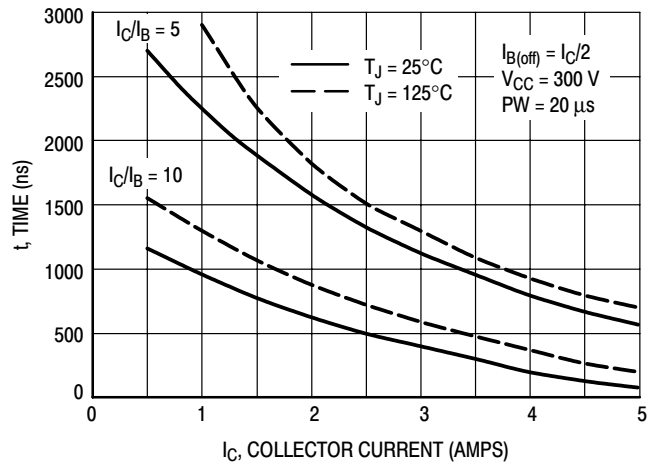


Figure 8. Resistive Switching,  $t_{off}$

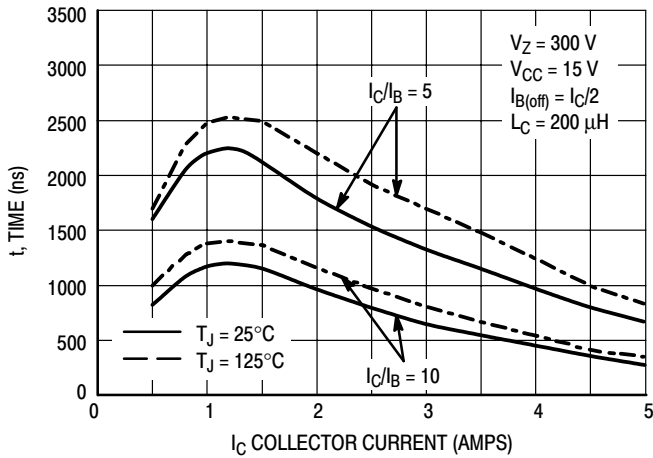


Figure 9. Inductive Storage Time,  $t_{si}$

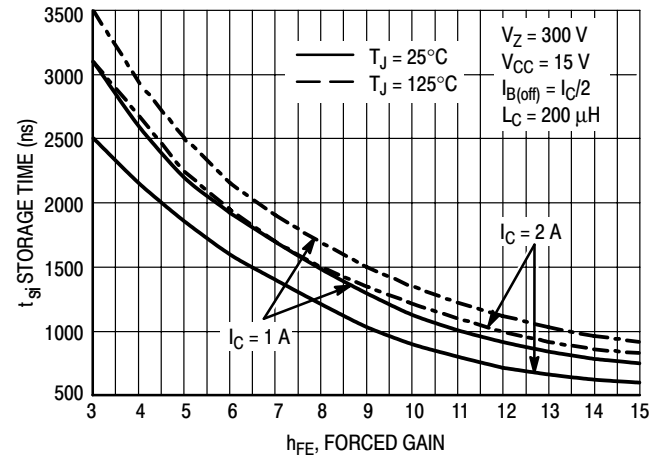


Figure 10. Inductive Storage Time,  $t_{si}(h_{FE})$

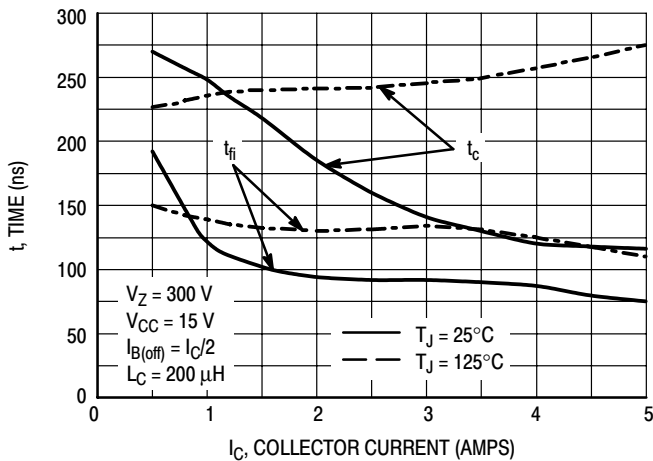


Figure 11. Inductive Switching,  $t_c$  and  $t_{fi}$ ,  $I_C/I_B = 5$

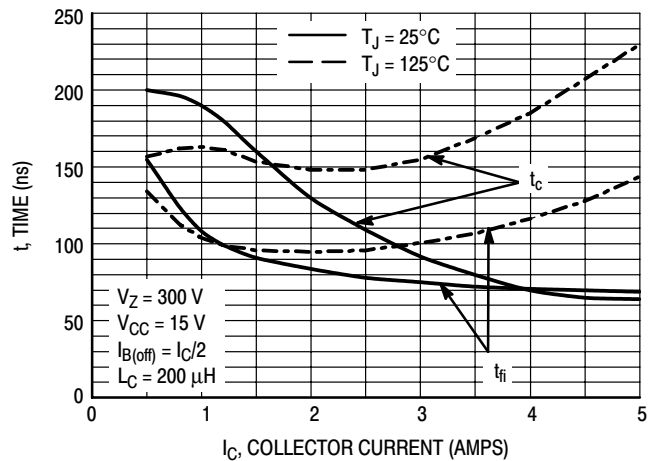


Figure 12. Inductive Switching,  $t_c$  and  $t_{fi}$ ,  $I_C/I_B = 10$

# MJE18004 MJF18004

## TYPICAL SWITCHING CHARACTERISTICS ( $I_{B2} = I_C/2$ for all switching)

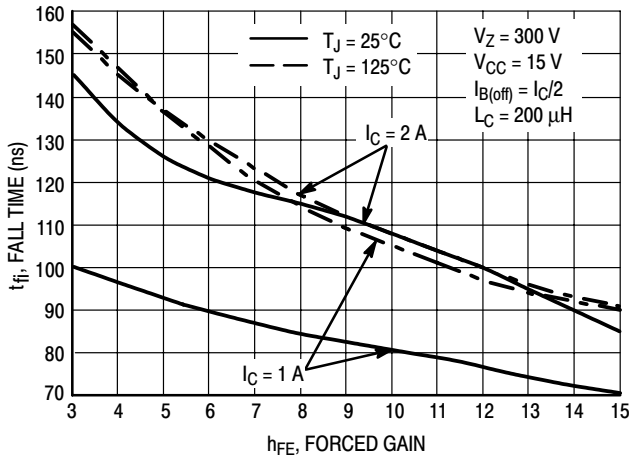


Figure 13. Inductive Fall Time

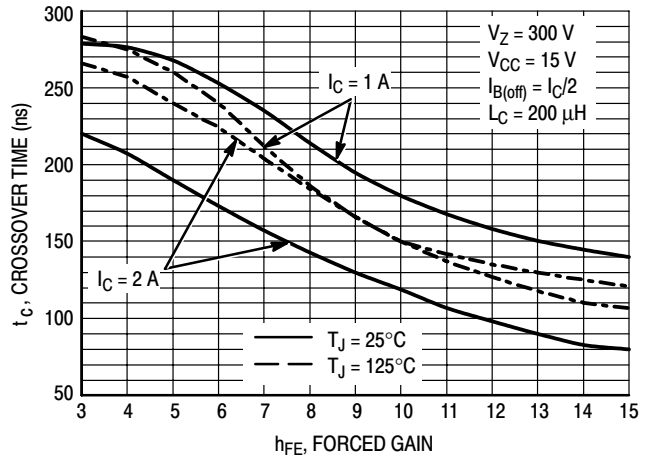


Figure 14. Inductive Crossover Time

## GUARANTEED SAFE OPERATING AREA INFORMATION

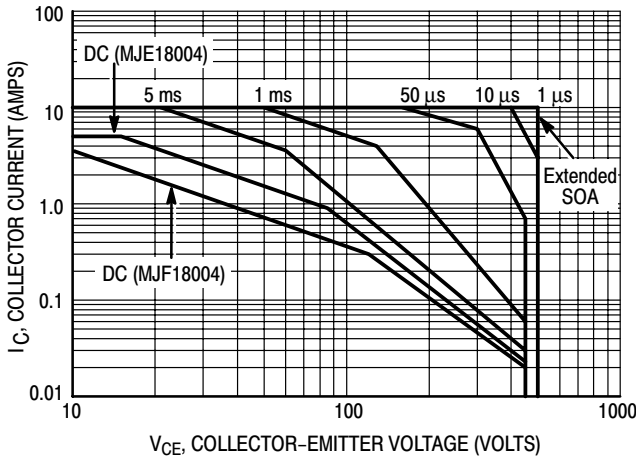


Figure 15. Forward Bias Safe Operating Area

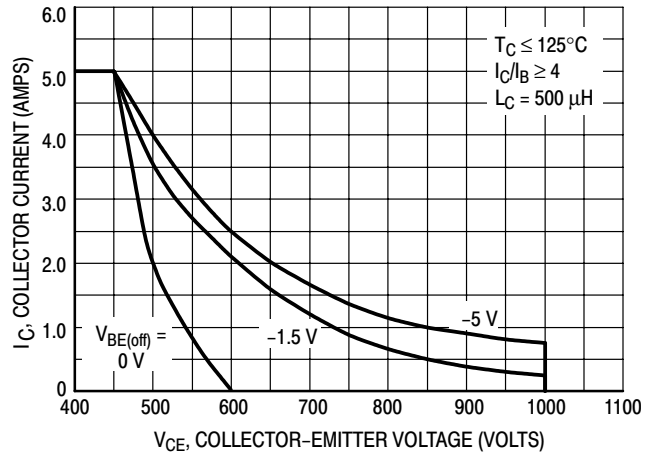


Figure 16. Reverse Bias Safe Operating Area

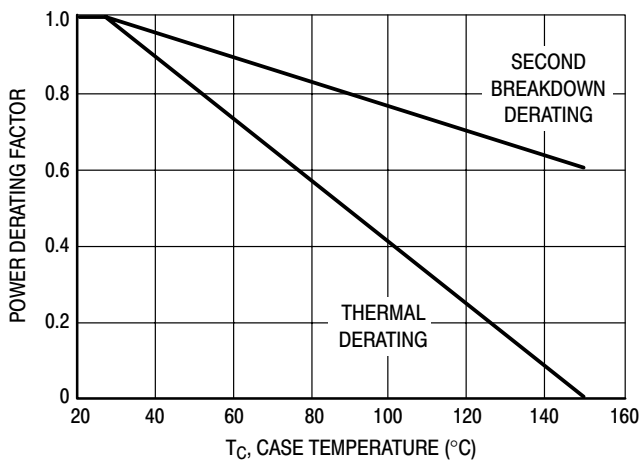


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on  $T_C = 25^\circ\text{C}$ ;  $T_J(\text{pk})$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.  $T_J(\text{pk})$  may be calculated from the data in Figures 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse biased. The safe level is specified as a reverse-biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.



# MJE18004 MJF18004

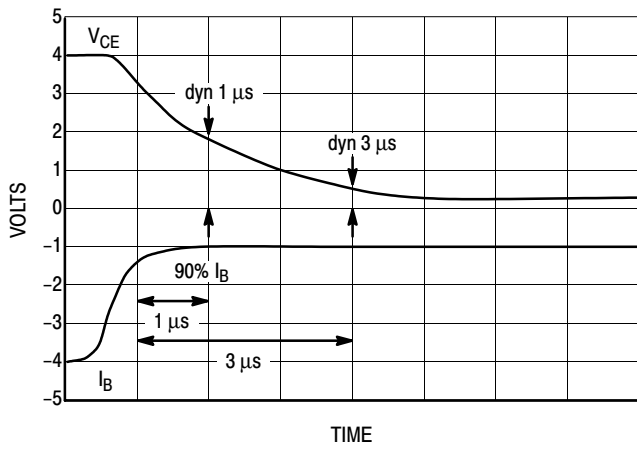


Figure 18. Dynamic Saturation Voltage Measurements

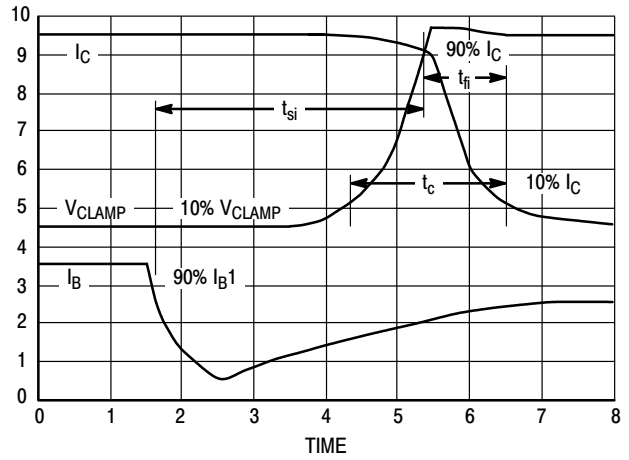
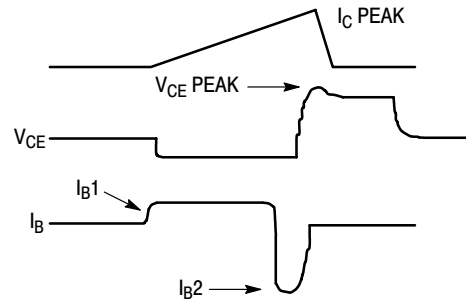
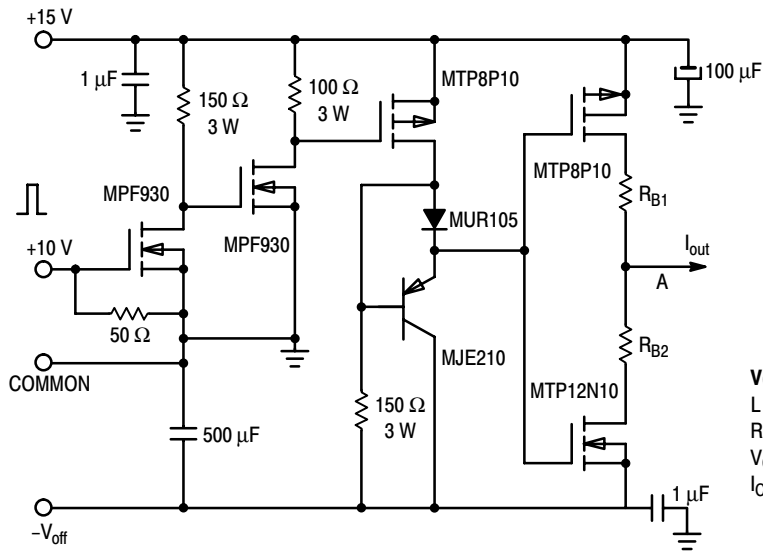


Figure 19. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
VCC = 20 VOLTS	VCC = 15 VOLTS	VCC = 15 VOLTS
IC(pk) = 100 mA	RB1 SELECTED FOR DESIRED IB1	RB1 SELECTED FOR DESIRED IB1

Table 1. Inductive Load Switching Drive Circuit

# MJE18004 MJF18004

## TYPICAL THERMAL RESPONSE

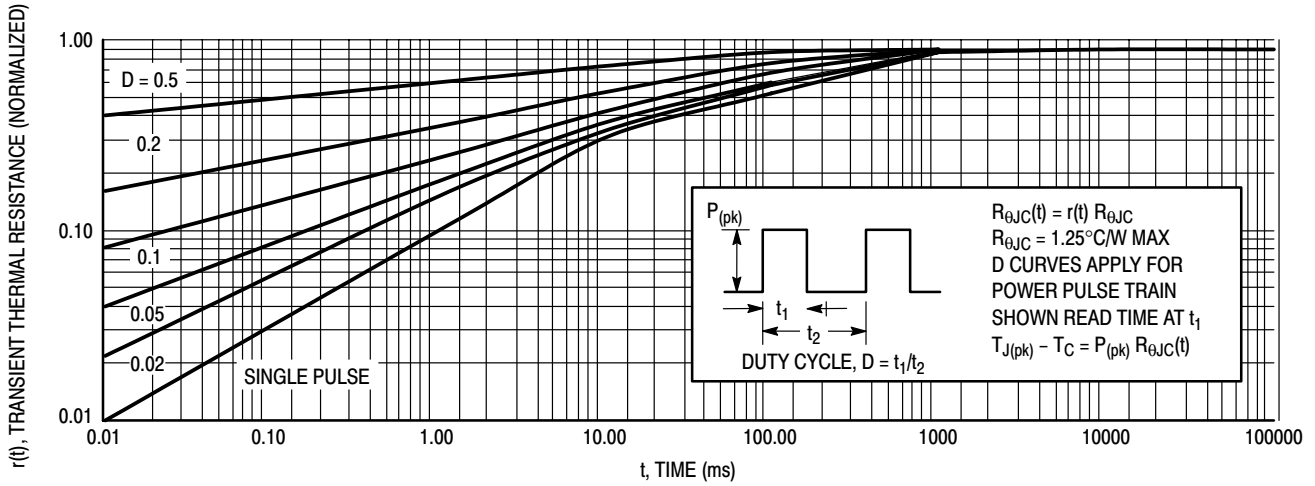


Figure 20. Typical Thermal Response ( $Z_{\theta_{JC}(t)}$ ) for MJE18004

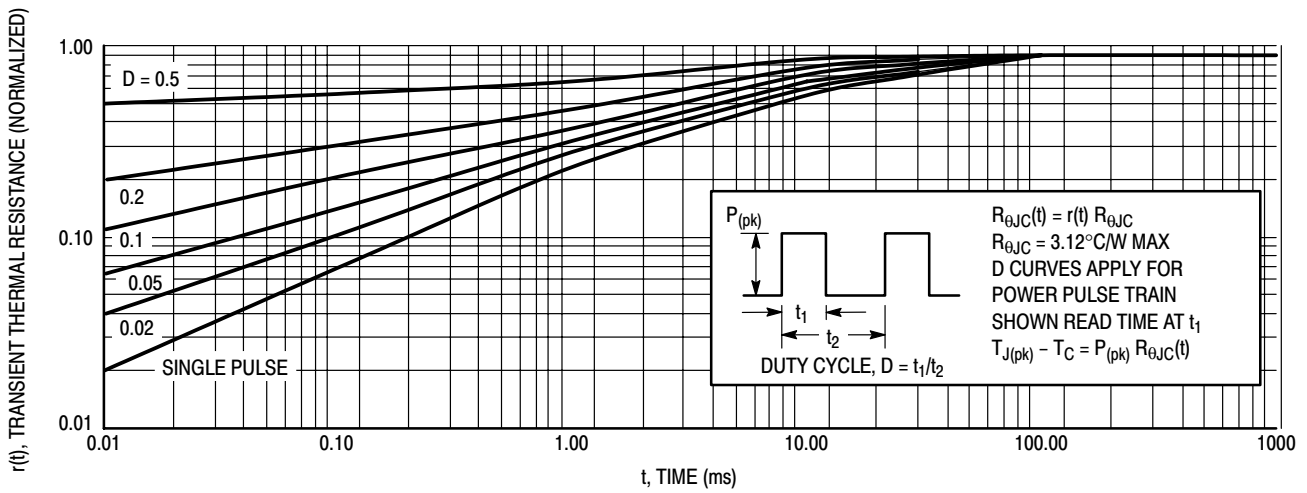


Figure 21. Typical Thermal Response for MJF18004

TEST CONDITIONS FOR ISOLATION TESTS\*

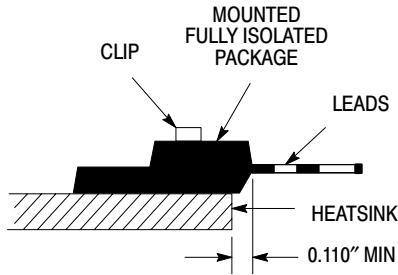


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

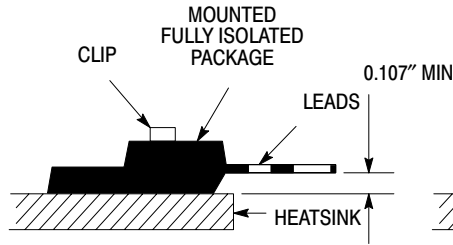


Figure 22b. Clip Mounting Position for Isolation Test Number 2

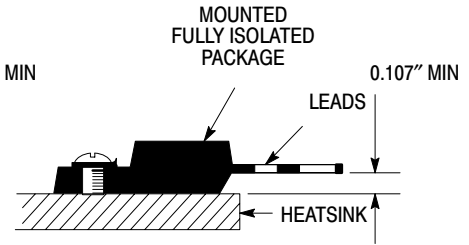


Figure 22c. Screw Mounting Position for Isolation Test Number 3

\*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION\*\*

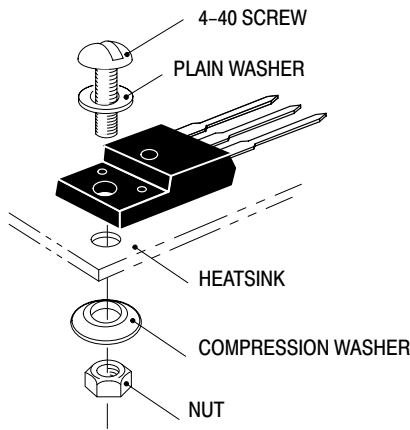


Figure 23a. Screw-Mounted

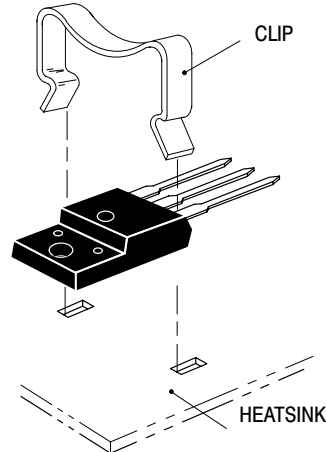


Figure 23b. Clip-Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.

**SWITCHMODE™****NPN Bipolar Power Transistor  
For Switching Power Supply Applications**

The MJE18006 has an applications specific state-of-the-art die designed for use in 220 V line-operated SWITCHMODE Power supplies and electronic light ballasts. This high voltage/high speed transistor offers the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain  $h_{FE}$
  - Fast Switching
  - No Coil Required in Base Circuit for Turn-Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot-to-Lot
- Standard TO-220

**MAXIMUM RATINGS**

Rating	Symbol	MJE18006	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	450	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	1000	Vdc
Emitter-Base Voltage	$V_{EBO}$	9.0	Vdc
Collector Current — Continuous	$I_C$	6.0	Adc
— Peak(1)	$I_{CM}$	15	
Base Current — Continuous	$I_B$	4.0	Adc
— Peak(1)	$I_{BM}$	8.0	
Total Device Dissipation Derate above 25°C	$P_D$	100 0.8	Watts W/°C
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150	°C

**THERMAL CHARACTERISTICS**

Rating	Symbol	MJE18006	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.25	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	260	°C

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Collector-Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$	—	—	100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )	$I_{CES}$	—	—	100	$\mu\text{Adc}$
( $V_{CE} = 800\text{ V}$ , $V_{EB} = 0$ )		—	—	500	
( $T_C = 125^\circ\text{C}$ )		—	—	100	
( $T_C = 125^\circ\text{C}$ )		—	—	100	
Emitter Cutoff Current ( $V_{EB} = 9.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	100	$\mu\text{Adc}$

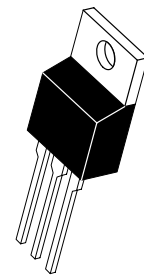
- (1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle  $\leq 10\%$ .  
 (2) Proper strike and creepage distance must be provided.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**MJE18006\***

\*ON Semiconductor Preferred Device

**POWER TRANSISTOR**  
**6.0 AMPERES**  
**1000 VOLTS**  
**100 WATTS**



**CASE 221A-09**  
**TO-220AB**

# MJE18006

## ELECTRICAL CHARACTERISTICS — continued ( $T_C = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b>					
Base–Emitter Saturation Voltage ( $I_C = 1.3\text{ Adc}$ , $I_B = 0.13\text{ Adc}$ ) ( $I_C = 3.0\text{ Adc}$ , $I_B = 0.6\text{ Adc}$ )	$V_{BE(sat)}$	— —	0.83 0.94	1.2 1.3	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 1.3\text{ Adc}$ , $I_B = 0.13\text{ Adc}$ )  ( $T_C = 125^\circ\text{C}$ ) ( $I_C = 3.0\text{ Adc}$ , $I_B = 0.6\text{ Adc}$ )  ( $T_C = 125^\circ\text{C}$ )	$V_{CE(sat)}$	— — — —	0.25 0.27 0.35 0.4	0.6 0.65 0.7 0.8	Vdc
DC Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ )  ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )  ( $I_C = 1.3\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 10\text{ mAdc}$ , $V_{CE} = 5.0\text{ Vdc}$ )	$h_{FE}$	14 — 6.0 5.0 11 10	— 32 10 8.0 17 22	34 — — — — —	—

## DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	—	14	—	MHz	
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	$C_{ob}$	—	75	120	pF	
Input Capacitance ( $V_{EB} = 8.0\text{ V}$ )	$C_{ib}$	—	1000	1500	pF	
Dynamic Saturation Voltage:  Determined 1.0 $\mu\text{s}$ and 3.0 $\mu\text{s}$ respectively after rising $I_{B1}$ reaches 90% of final $I_{B1}$ (see Figure 18)	$V_{CE(dsat)}$	$I_C = 1.3\text{ Adc}$ $I_{B1} = 130\text{ mAdc}$ $V_{CC} = 300\text{ V}$	1.0 $\mu\text{s}$ 3.0 $\mu\text{s}$	$T_C = 125^\circ\text{C}$ $T_C = 125^\circ\text{C}$	— — — — — — — —	Volts

## SWITCHING CHARACTERISTICS: Resistive Load ( $D.C. \leq 10\%$ , Pulse Width = 20 $\mu\text{s}$ )

Turn–On Time	$I_C = 3.0\text{ Adc}$ , $I_{B1} = 0.6\text{ Adc}$ , $I_{B2} = 1.5\text{ Adc}$ , $V_{CC} = 300\text{ V}$	$T_C = 125^\circ\text{C}$	$t_{on}$	— —	90 100	180 —	ns
Turn–Off Time			$t_{off}$	— —	1.7 2.1	2.5 —	$\mu\text{s}$
Turn–On Time	$I_C = 1.3\text{ Adc}$ , $I_{B1} = 0.13\text{ Adc}$ , $I_{B2} = 0.65\text{ Adc}$ , $V_{CC} = 300\text{ V}$	$T_C = 125^\circ\text{C}$	$t_{on}$	— —	200 130	300 —	ns
Turn–Off Time			$t_{off}$	— —	1.2 1.5	2.5 —	$\mu\text{s}$

## SWITCHING CHARACTERISTICS: Inductive Load ( $V_{clamp} = 300\text{ V}$ , $V_{CC} = 15\text{ V}$ , $L = 200\text{ }\mu\text{H}$ )

Fall Time	$I_C = 1.5\text{ Adc}$ , $I_{B1} = 0.13\text{ Adc}$ , $I_{B2} = 0.65\text{ Adc}$	$T_C = 125^\circ\text{C}$	$t_{fi}$	— —	100 120	180 —	ns
Storage Time			$t_{si}$	— —	1.5 1.9	2.5 —	$\mu\text{s}$
Crossover Time			$t_c$	— —	220 230	350 —	ns
Fall Time	$I_C = 3.0\text{ Adc}$ , $I_{B1} = 0.6\text{ Adc}$ , $I_{B2} = 1.5\text{ Adc}$	$T_C = 125^\circ\text{C}$	$t_{fi}$	— —	85 120	150 —	ns
Storage Time			$t_{si}$	— —	2.15 2.75	3.2 —	$\mu\text{s}$
Crossover Time			$t_c$	— —	200 310	300 —	ns

TYPICAL STATIC CHARACTERISTICS

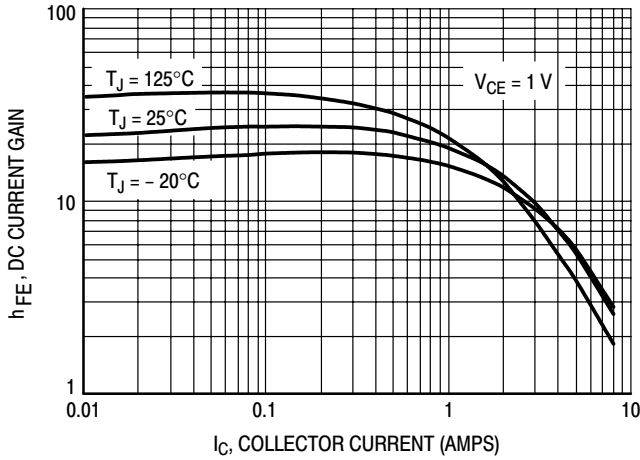


Figure 1. DC Current Gain @ 1 Volt

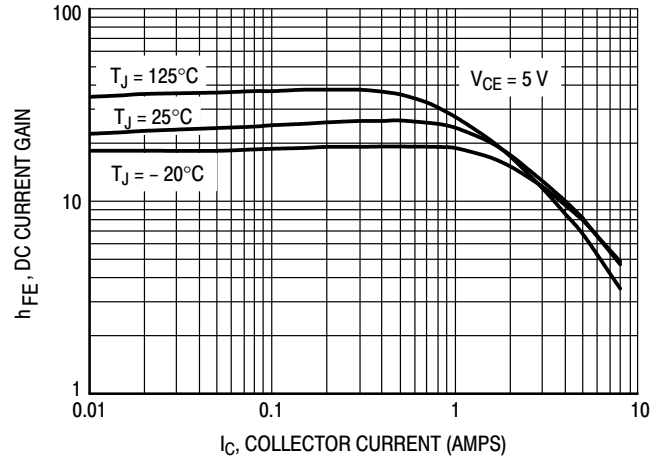


Figure 2. DC Current Gain @ 5 Volts

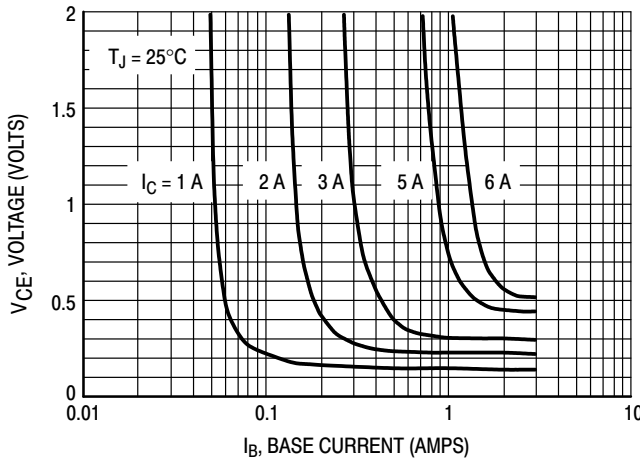


Figure 3. Collector Saturation Region

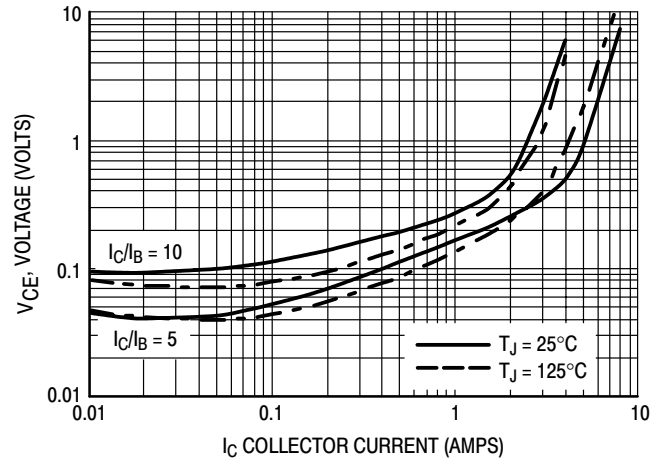


Figure 4. Collector-Emitter Saturation Voltage

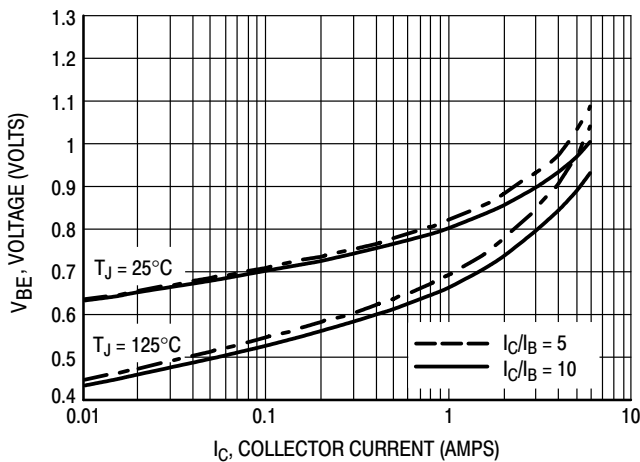


Figure 5. Base-Emitter Saturation Region

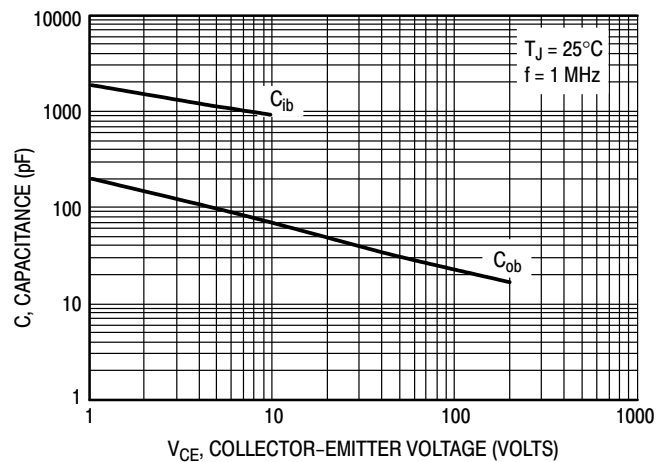


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

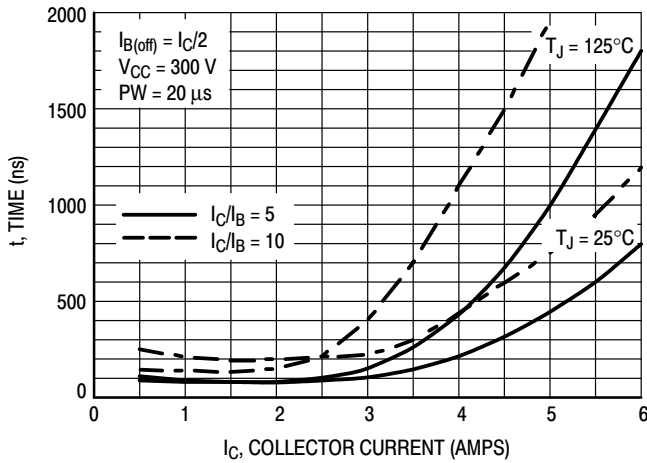


Figure 7. Resistive Switching,  $t_{on}$

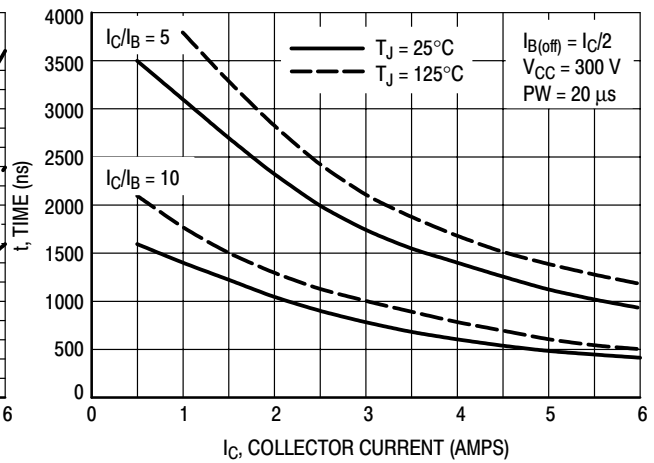


Figure 8. Resistive Switching,  $t_{off}$

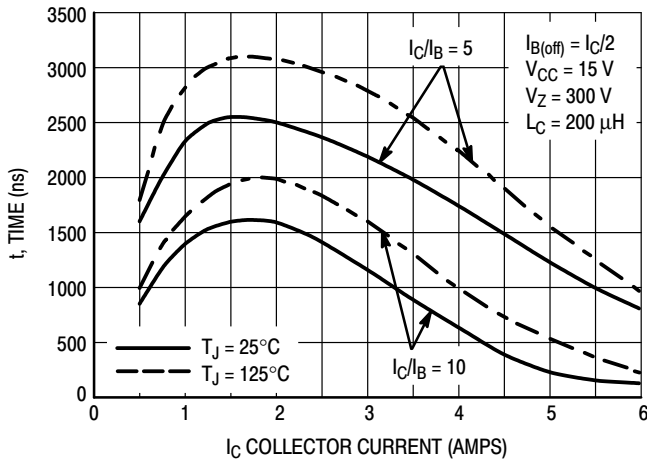


Figure 9. Inductive Storage Time,  $t_{si}$

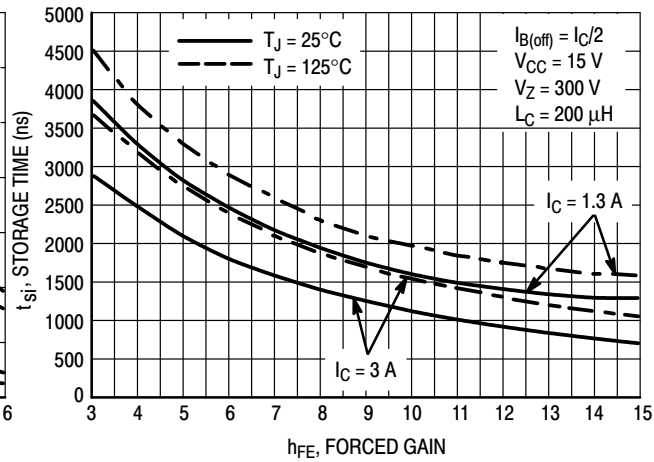


Figure 10. Inductive Storage Time,  $t_{si}(h_{FE})$

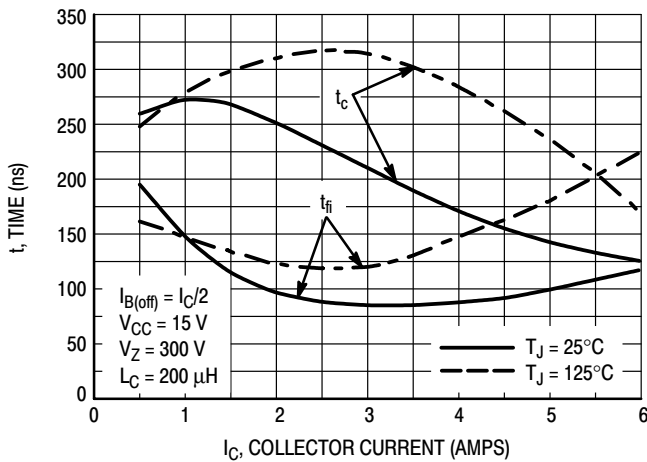


Figure 11. Inductive Switching,  $t_c$  and  $t_{fi}$   
 $I_C/I_B = 5$

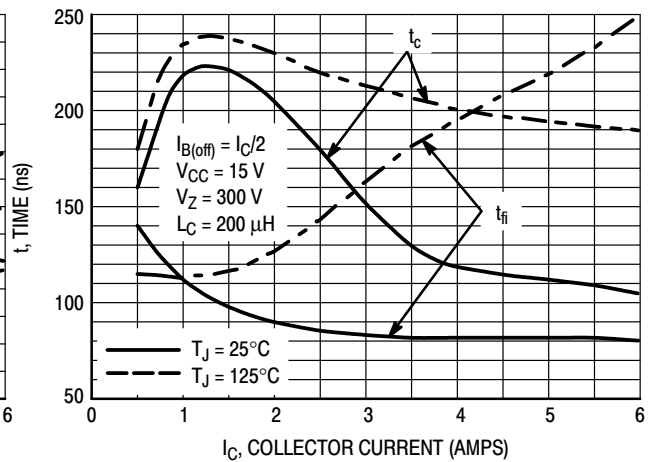


Figure 12. Inductive Switching,  $t_c$  and  $t_{fi}$   
 $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS  
 ( $I_{B2} = I_C/2$  for all switching)

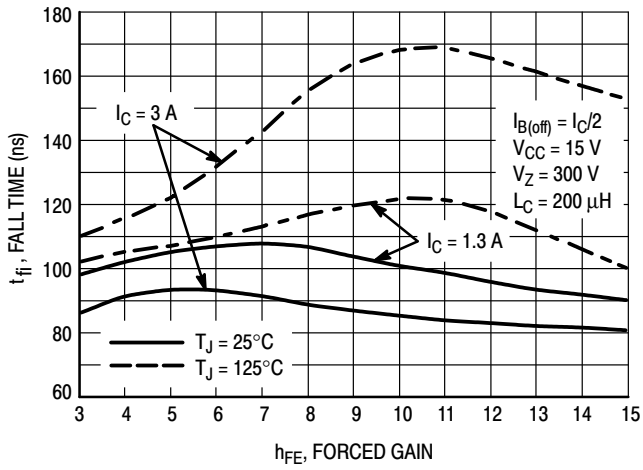


Figure 13. Inductive Fall Time

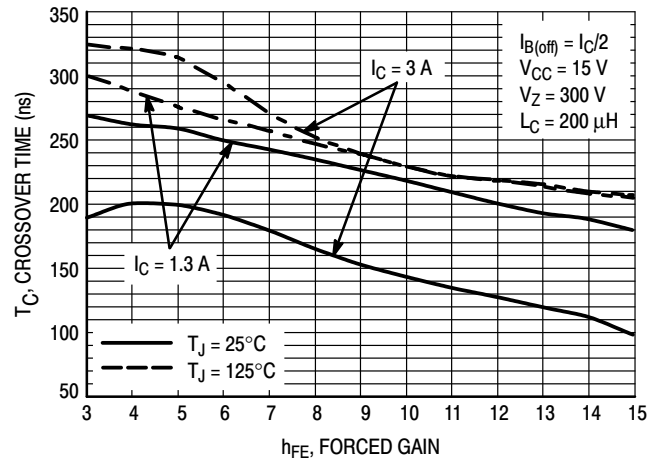


Figure 14. Inductive Crossover Time



GUARANTEED SAFE OPERATING AREA INFORMATION

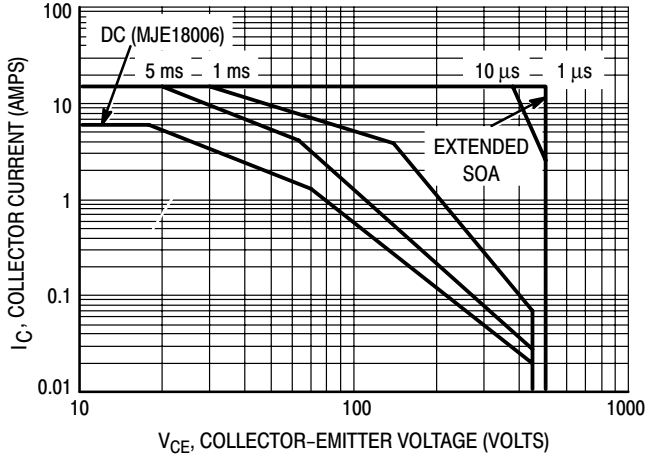


Figure 15. Forward Bias Safe Operating Area

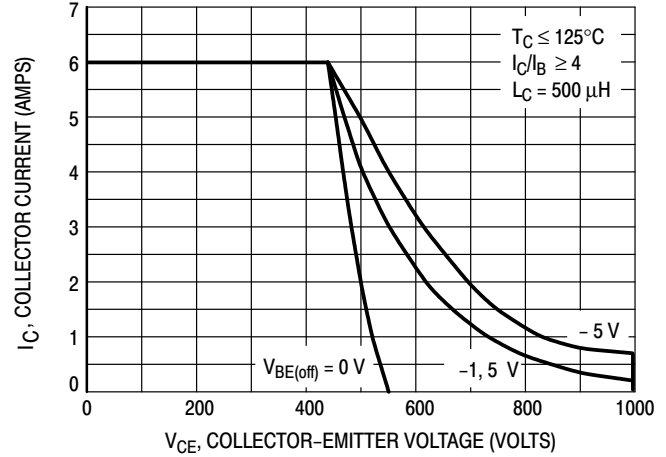


Figure 16. Reverse Bias Switching Safe Operating Area

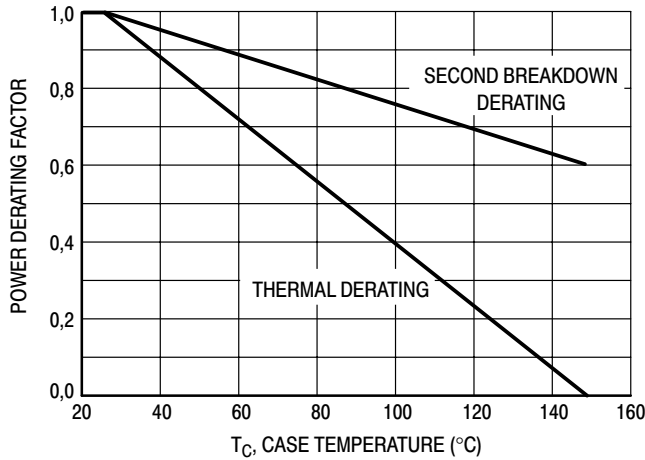


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.  $T_{J(pk)}$  may be calculated from the data in Figure 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse-biased. The safe level is specified as a reverse-biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

# MJE18006

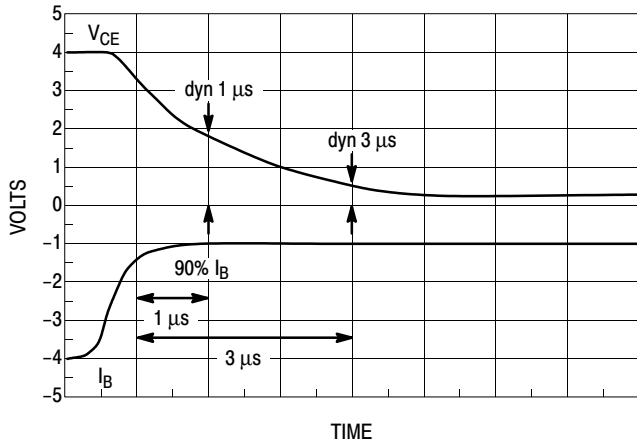


Figure 18. Dynamic Saturation Voltage Measurements

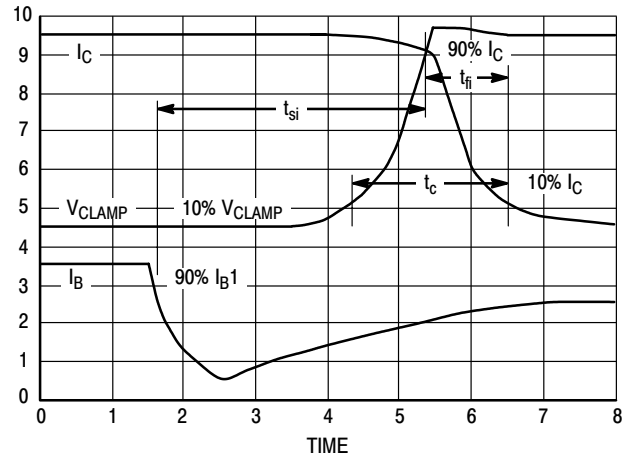
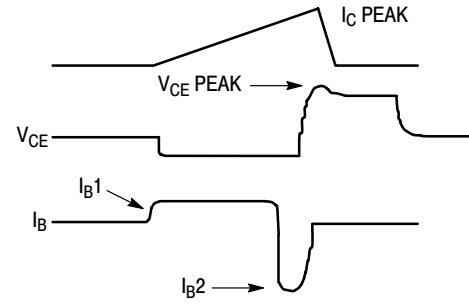
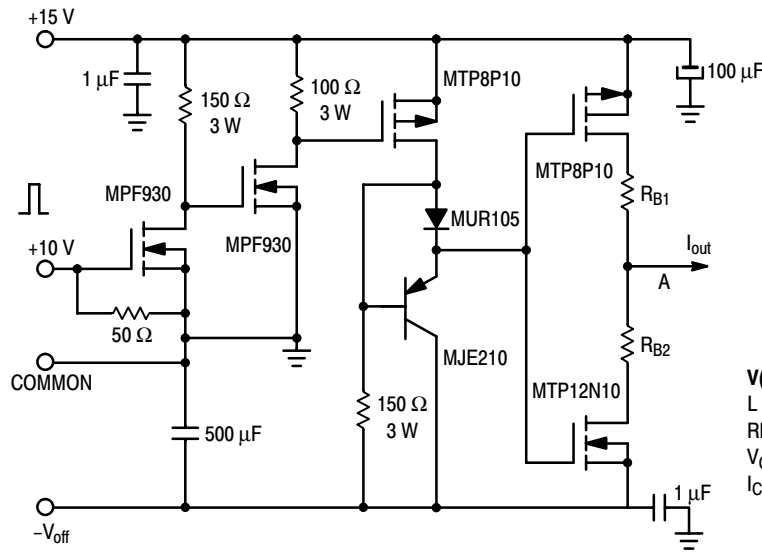


Figure 19. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
VCC = 20 VOLTS	VCC = 15 VOLTS	VCC = 15 VOLTS
IC(pk) = 100 mA	RB1 SELECTED FOR DESIRED IB1	RB1 SELECTED FOR DESIRED IB1

Table 1. Inductive Load Switching Drive Circuit

## TYPICAL THERMAL RESPONSE

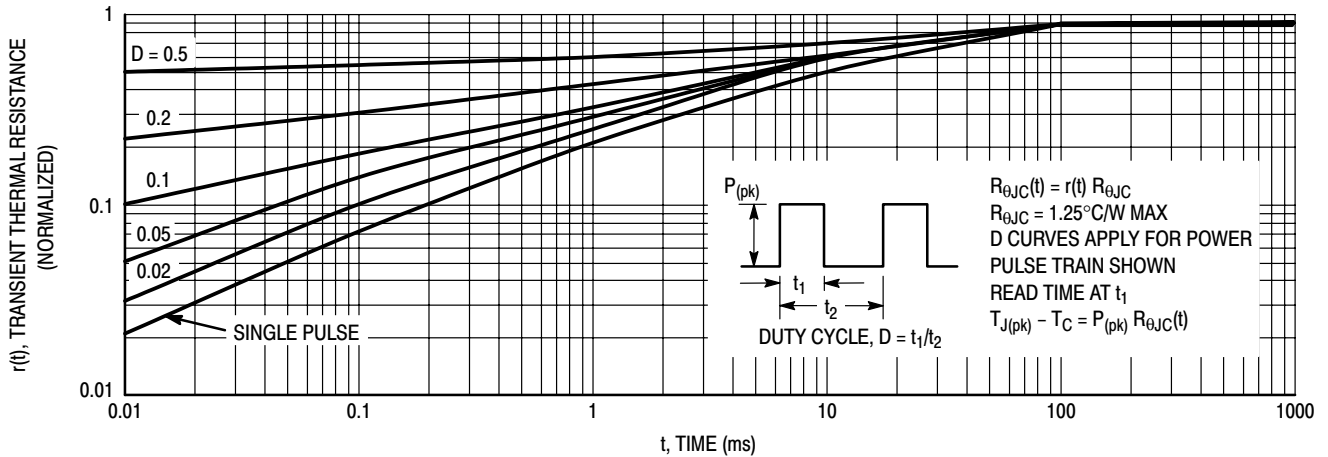


Figure 20. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for MJE18006

# SWITCHMODE™

## NPN Bipolar Power Transistor

### For Switching Power Supply Applications

The MJE/MJF18008 have an applications specific state-of-the-art die designed for use in 220 V line-operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain  $h_{FE}$
  - Fast Switching
  - No Coil Required in Base Circuit for Turn-Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot-to-Lot
- Two Package Choices: Standard TO-220 or Isolated TO-220
- MJF18008, Case 221D, is UL Recognized at 3500 V<sub>RMS</sub>: File #E69369

#### MAXIMUM RATINGS

Rating	Symbol	MJE18008	MJF18008	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	450		Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	1000		Vdc
Emitter-Base Voltage	$V_{EBO}$	9.0		Vdc
Collector Current — Continuous	$I_C$	8.0		Adc
— Peak(1)	$I_{CM}$	16		
Base Current — Continuous	$I_B$	4.0		Adc
— Peak(1)	$I_{BM}$	8.0		
RMS Isolation Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec,] R.H. < 30%, Test No. 1 Per Fig. 22b $T_C = 25^\circ\text{C}$ Test No. 1 Per Fig. 22c	$V_{ISOL}$	—	4500	Volts
		—	3500	
		—	1500	
Total Device Dissipation ( $T_C = 25^\circ\text{C}$ ) Derate above $25^\circ\text{C}$	$P_D$	125 1.0	45 0.36	Watts W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150		$^\circ\text{C}$

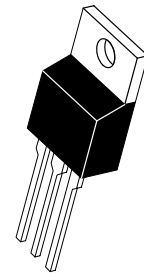
#### THERMAL CHARACTERISTICS

Rating	Symbol	MJE18008	MJF18008	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.0	2.78	$^\circ\text{C}/\text{W}$
— Junction to Ambient	$R_{\theta JA}$	62.5	62.5	
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	260		$^\circ\text{C}$

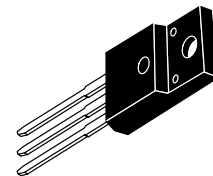
**MJE18008\***  
**MJF18008\***

\*ON Semiconductor Preferred Device

**POWER TRANSISTOR**  
**8.0 AMPERES**  
**1000 VOLTS**  
**45 and 125 WATTS**



**CASE 221A-09**  
**TO-220AB**  
**MJE18008**



**CASE 221D-02**  
**ISOLATED TO-220 TYPE**  
**UL RECOGNIZED**  
**MJF18008**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJE18008 MJF18008

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $I_B = 0$ )	$I_{CEO}$	—	—	100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CES}$ , $V_{EB} = 0$ )	$I_{CES}$	—	—	100	$\mu\text{Adc}$
$(T_C = 125^\circ\text{C})$		—	—	500	
$(V_{CE} = 800\text{ V}$ , $V_{EB} = 0$ )		—	—	100	
$(T_C = 125^\circ\text{C})$		—	—	100	
Emitter Cutoff Current ( $V_{EB} = 9.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	100	$\mu\text{Adc}$

### ON CHARACTERISTICS

Base–Emitter Saturation Voltage ( $I_C = 2.0\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ ) ( $I_C = 4.5\text{ Adc}$ , $I_B = 0.9\text{ Adc}$ )	$V_{BE(sat)}$	—	0.82	1.1	Vdc
		—	0.92	1.25	
Collector–Emitter Saturation Voltage ( $I_C = 2.0\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	$V_{CE(sat)}$	—	0.3	0.6	Vdc
$(T_C = 125^\circ\text{C})$		—	0.3	0.65	
( $I_C = 4.5\text{ Adc}$ , $I_B = 0.9\text{ Adc}$ )		—	0.35	0.7	
$(T_C = 125^\circ\text{C})$		—	0.4	0.8	
DC Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ )	$h_{FE}$	14	—	34	—
		—	28	—	
$(T_C = 125^\circ\text{C})$		6.0	9.0	—	
( $I_C = 4.5\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )		5.0	8.0	—	
$(T_C = 125^\circ\text{C})$		11	15	—	
( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )		11	16	—	
$(T_C = 125^\circ\text{C})$		11	16	—	
( $I_C = 10\text{ mAdc}$ , $V_{CE} = 5.0\text{ Vdc}$ )		10	20	—	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle  $\leq$  10%.

(2) Proper strike and creepage distance must be provided.

(continued)

# MJE18008 MJF18008

Characteristic	Symbol	Min	Typ	Max	Unit
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## DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 0.5 \text{ Adc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )			$f_T$	—	13	—	MHz	
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 1.0 \text{ MHz}$ )			$C_{ob}$	—	100	150	pF	
Input Capacitance ( $V_{EB} = 8.0 \text{ V}$ )			$C_{ib}$	—	1750	2500	pF	
Dynamic Saturation Voltage:  Determined 1.0 $\mu\text{s}$ and 3.0 $\mu\text{s}$ respectively after rising $I_{B1}$ reaches 90% of final $I_{B1}$ (see Figure 18)	$(I_C = 2.0 \text{ Adc}$ $I_{B1} = 200 \text{ mAdc}$ $V_{CC} = 300 \text{ V})$	1.0 $\mu\text{s}$	$(T_C = 125^\circ\text{C})$	$V_{CE(dsat)}$	—	5.5	—	Vdc
		3.0 $\mu\text{s}$	$(T_C = 125^\circ\text{C})$		—	11.5	—	
	$(I_C = 5.0 \text{ Adc}$ $I_{B1} = 1.0 \text{ Adc}$ $V_{CC} = 300 \text{ V})$	1.0 $\mu\text{s}$	$(T_C = 125^\circ\text{C})$		—	3.5	—	
		3.0 $\mu\text{s}$	$(T_C = 125^\circ\text{C})$		—	6.5	—	
	1.0 $\mu\text{s}$	$(T_C = 125^\circ\text{C})$	—		11.5	—		
	3.0 $\mu\text{s}$	$(T_C = 125^\circ\text{C})$	—		14.5	—		

## SWITCHING CHARACTERISTICS: Resistive Load (D.C. $\leq 10\%$ , Pulse Width = 20 $\mu\text{s}$ )

Turn-On Time	$(I_C = 2.0 \text{ Adc}$ , $I_{B1} = 0.2 \text{ Adc}$ , $I_{B2} = 1.0 \text{ Adc}$ , $V_{CC} = 300 \text{ V})$	$(T_C = 125^\circ\text{C})$	$t_{on}$	—	200	300	ns
Turn-Off Time		$(T_C = 125^\circ\text{C})$	$t_{off}$	—	1.2	2.5	$\mu\text{s}$
Turn-On Time	$(I_C = 4.5 \text{ Adc}$ , $I_{B1} = 0.9 \text{ Adc}$ , $I_{B2} = 2.25 \text{ Adc}$ , $V_{CC} = 300 \text{ V})$	$(T_C = 125^\circ\text{C})$	$t_{on}$	—	100	180	ns
Turn-Off Time		$(T_C = 125^\circ\text{C})$	$t_{off}$	—	1.6	2.5	$\mu\text{s}$

## SWITCHING CHARACTERISTICS: Inductive Load ( $V_{clamp} = 300 \text{ V}$ , $V_{CC} = 15 \text{ V}$ , $L = 200 \mu\text{H}$ )

Fall Time	$(I_C = 2.0 \text{ Adc}$ , $I_{B1} = 0.2 \text{ Adc}$ , $I_{B2} = 1.0 \text{ Adc})$	$(T_C = 125^\circ\text{C})$	$t_{fi}$	—	100	180	ns
Storage Time		$(T_C = 125^\circ\text{C})$	$t_{si}$	—	1.5	2.75	$\mu\text{s}$
Crossover Time		$(T_C = 125^\circ\text{C})$	$t_c$	—	250	350	ns
Fall Time	$(I_C = 4.5 \text{ Adc}$ , $I_{B1} = 0.9 \text{ Adc}$ , $I_{B2} = 2.25 \text{ Adc})$	$(T_C = 125^\circ\text{C})$	$t_{fi}$	—	85	150	ns
Storage Time		$(T_C = 125^\circ\text{C})$	$t_{si}$	—	2.0	3.2	$\mu\text{s}$
Crossover Time		$(T_C = 125^\circ\text{C})$	$t_c$	—	210	300	ns

TYPICAL STATIC CHARACTERISTICS

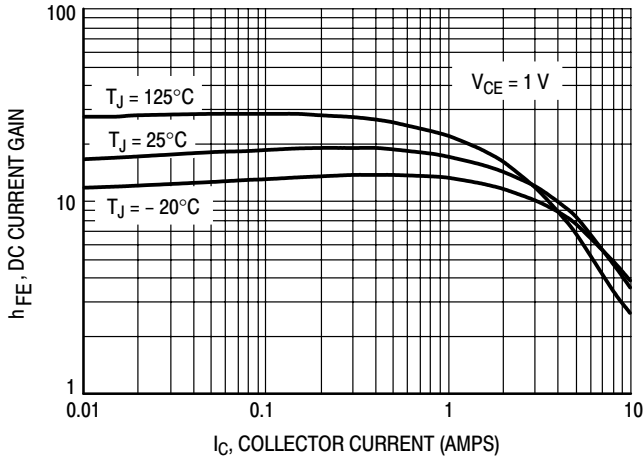


Figure 21. DC Current Gain @ 1 Volt

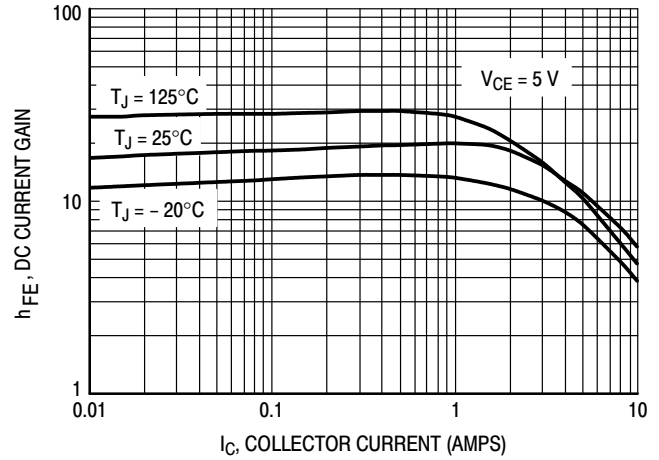


Figure 22. DC Current Gain @ 5 Volts

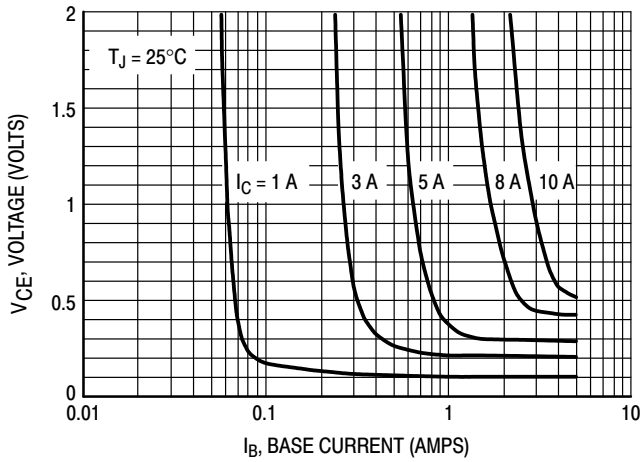


Figure 23. Collector Saturation Region

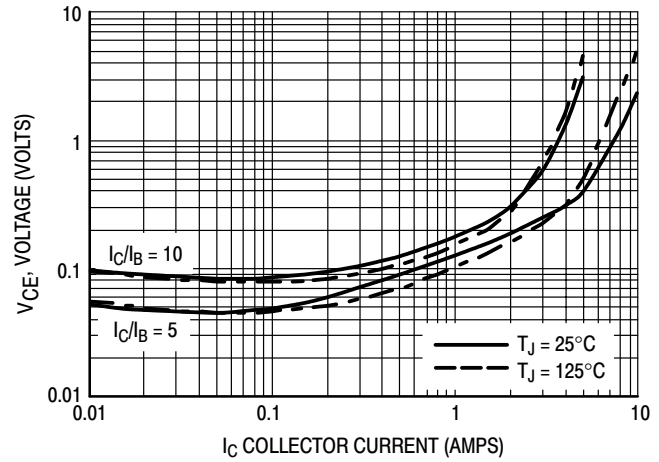


Figure 24. Collector-Emitter Saturation Voltage

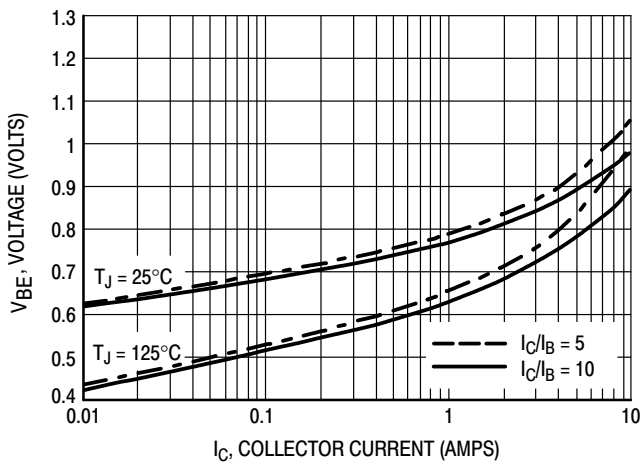


Figure 25. Base-Emitter Saturation Region

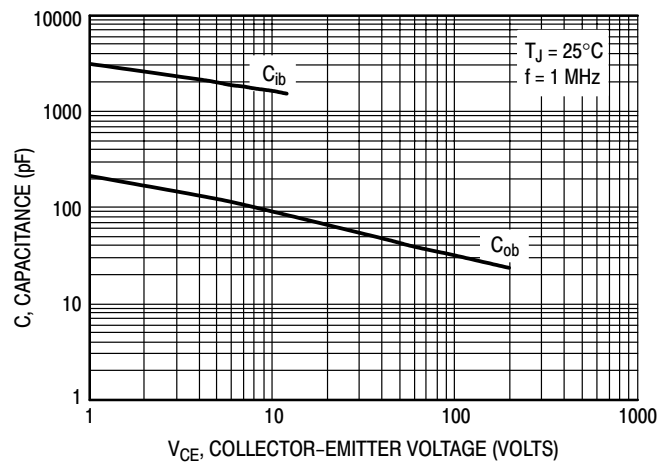


Figure 26. Capacitance

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

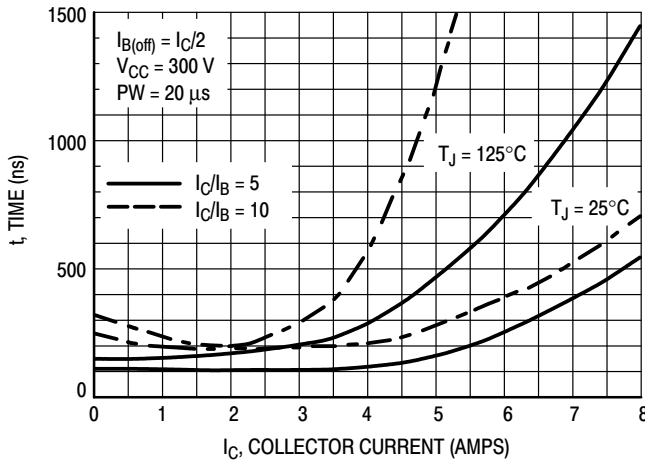


Figure 27. Resistive Switching,  $t_{on}$

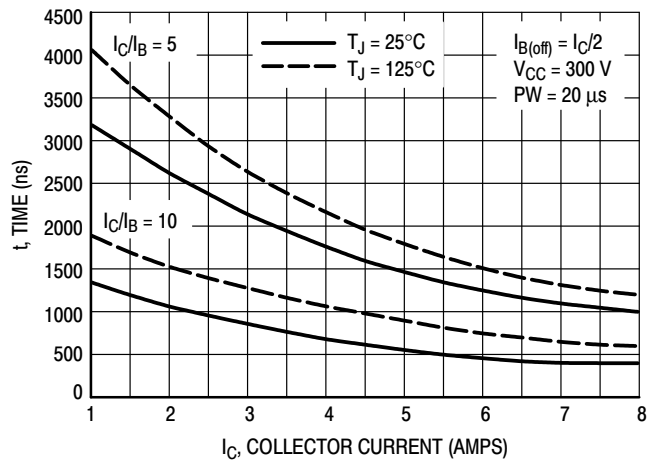


Figure 28. Resistive Switching,  $t_{off}$

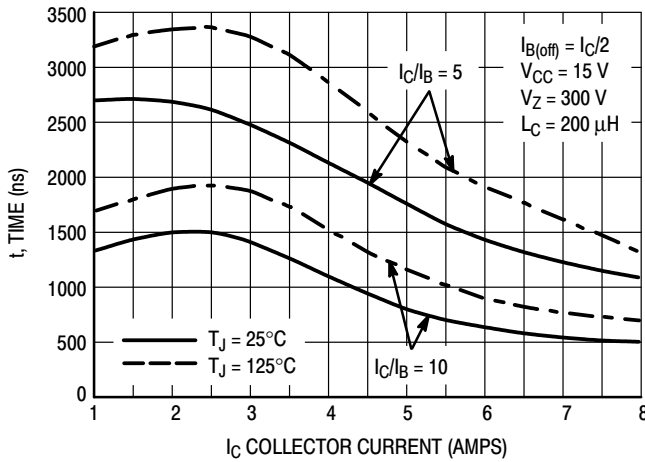


Figure 29. Inductive Storage Time,  $t_{si}$

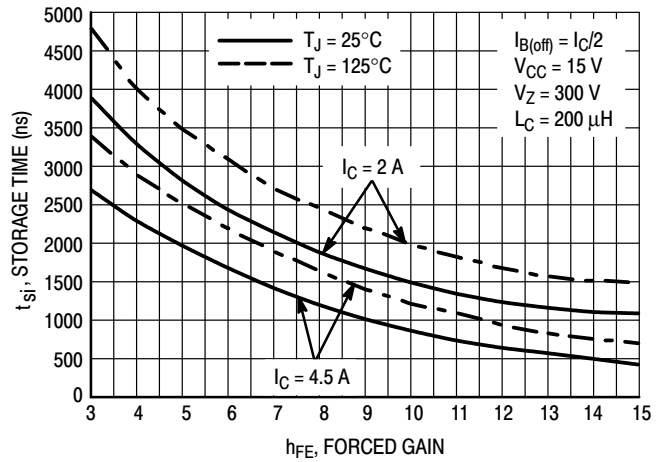


Figure 30. Inductive Storage Time,  $t_{si}(h_{FE})$

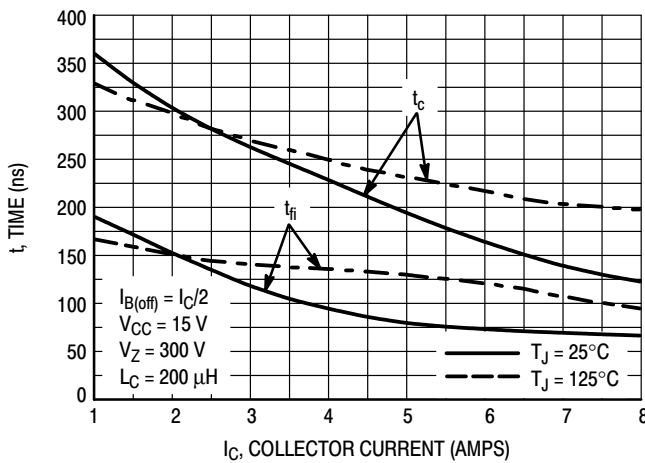


Figure 31. Inductive Switching,  $t_c$  and  $t_{fi}$   
 $I_C/I_B = 5$

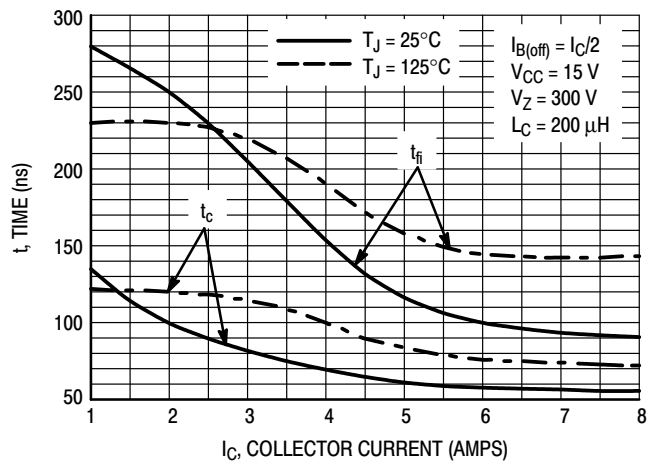


Figure 32. Inductive Switching,  $t_c$  and  $t_{fi}$   
 $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

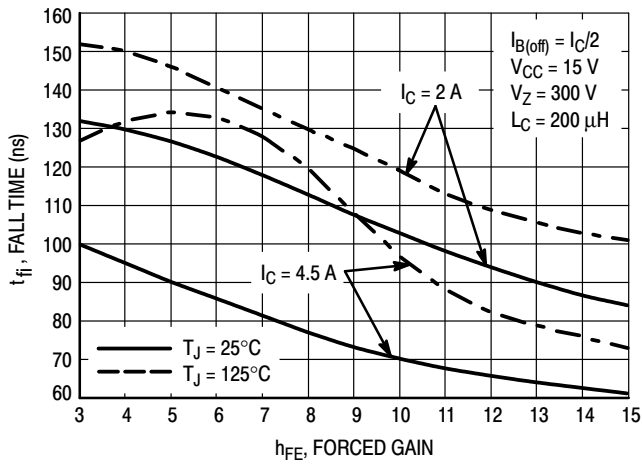


Figure 33. Inductive Fall Time

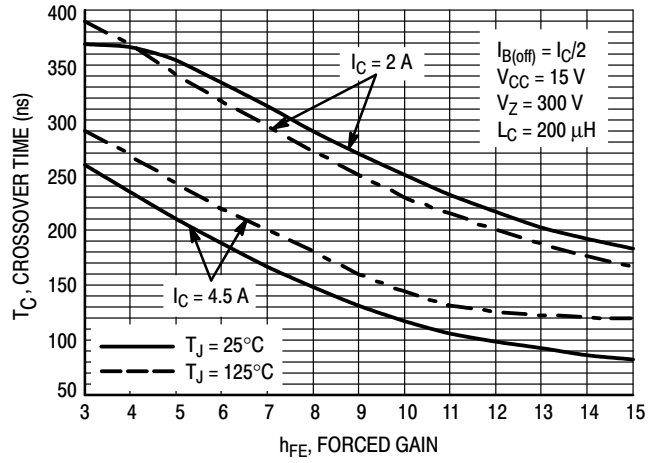


Figure 34. Inductive Crossover Time



GUARANTEED SAFE OPERATING AREA INFORMATION

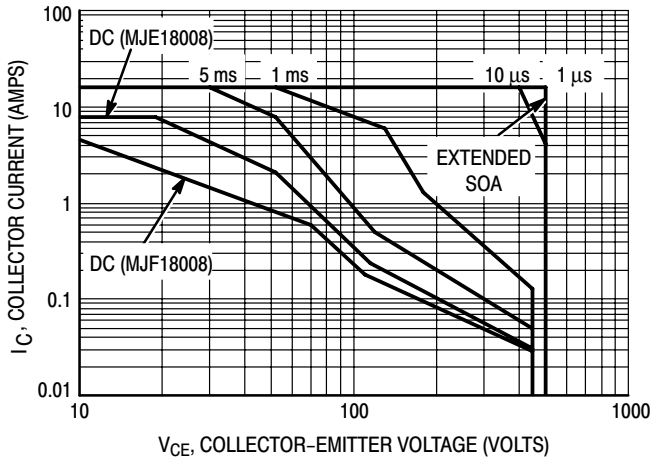


Figure 35. Forward Bias Safe Operating Area

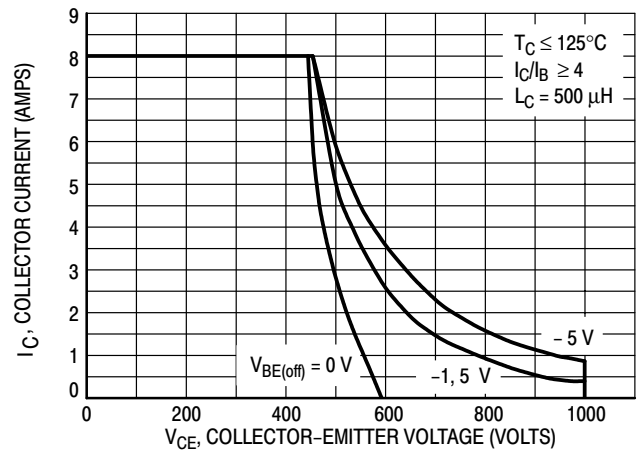


Figure 36. Reverse Bias Switching Safe Operating Area

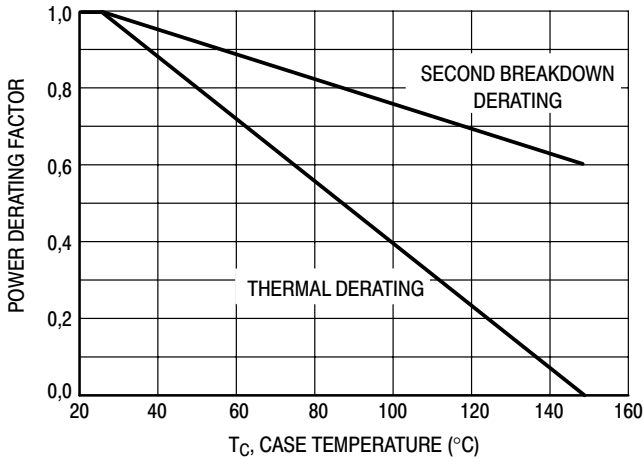


Figure 37. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 35 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 35 may be found at any case temperature by using the appropriate curve on Figure 37.  $T_{J(pk)}$  may be calculated from the data in Figure 40 and 41. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse-biased. The safe level is specified as a reverse-biased safe operating area (Figure 36). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

# MJE18008 MJF18008

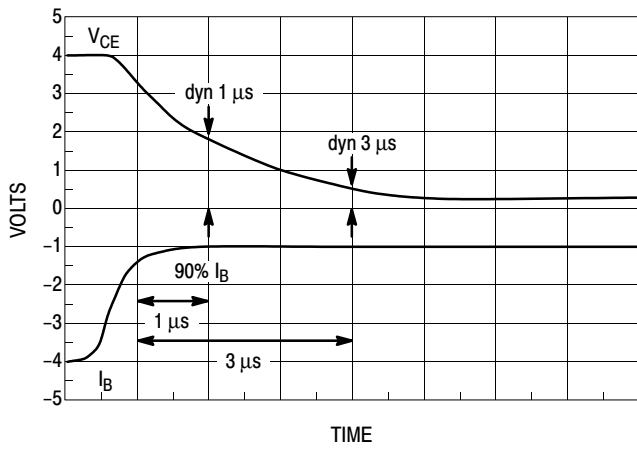


Figure 38. Dynamic Saturation Voltage Measurements

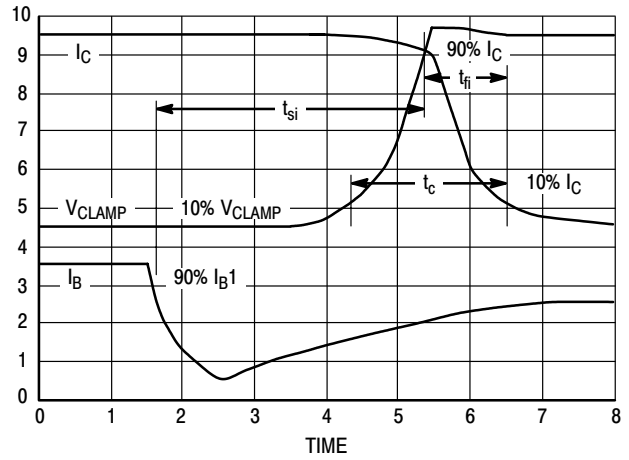
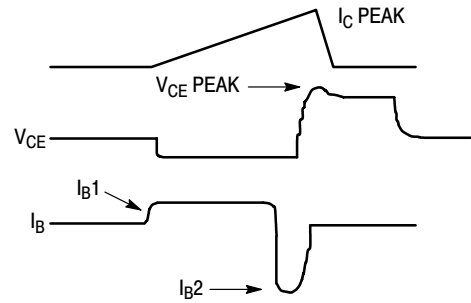
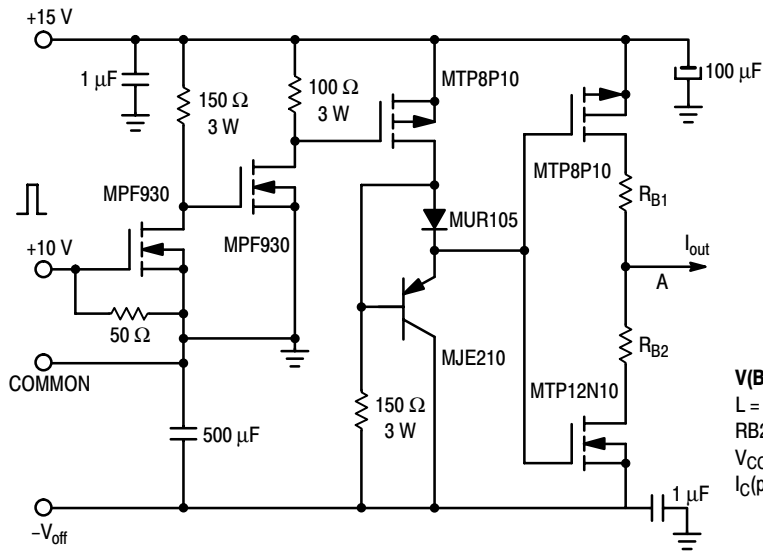


Figure 39. Inductive Switching Measurements



$V(BR)_{CEO}(sus)$	INDUCTIVE SWITCHING	RBSOA
$L = 10 \text{ mH}$	$L = 200 \mu\text{H}$	$L = 500 \mu\text{H}$
$RB2 = \infty$	$RB2 = 0$	$RB2 = 0$
$V_{CC} = 20 \text{ VOLTS}$	$V_{CC} = 15 \text{ VOLTS}$	$V_{CC} = 15 \text{ VOLTS}$
$I_C(pk) = 100 \text{ mA}$	$RB1$ SELECTED FOR DESIRED $I_{B1}$	$RB1$ SELECTED FOR DESIRED $I_{B1}$

Table 1. Inductive Load Switching Drive Circuit

# MJE18008 MJF18008

## TYPICAL THERMAL RESPONSE

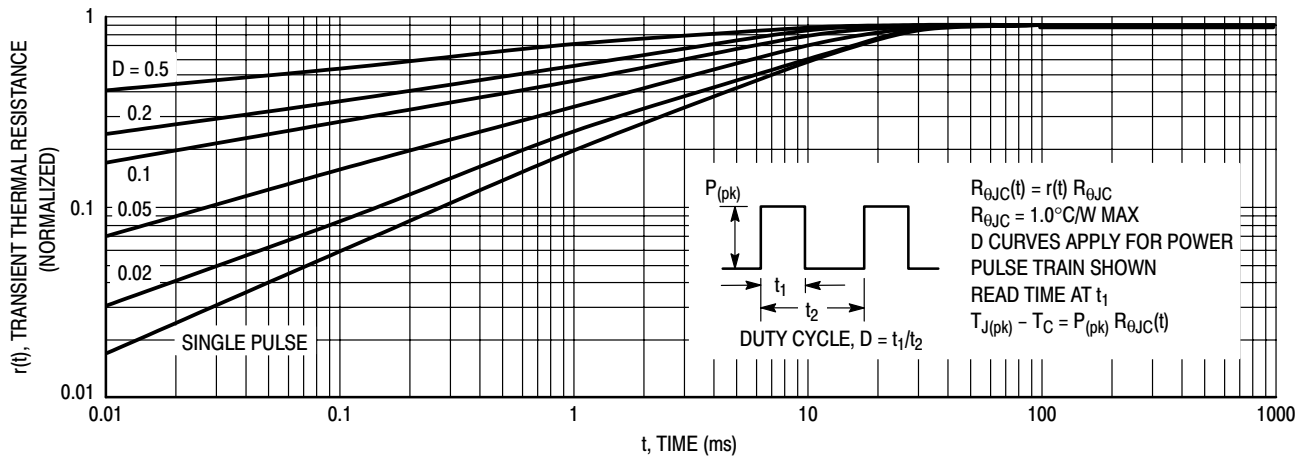


Figure 40. Typical Thermal Response ( $Z_{\theta_{JC}}(t)$ ) for MJE18008

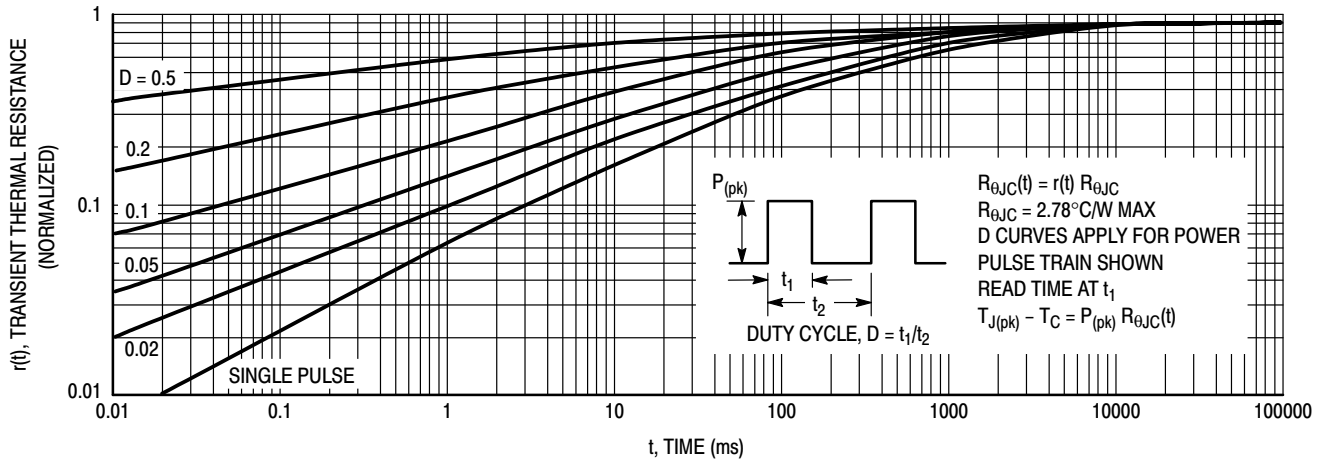


Figure 41. Typical Thermal Response ( $Z_{\theta_{JC}}(t)$ ) for MJF18008

TEST CONDITIONS FOR ISOLATION TESTS\*

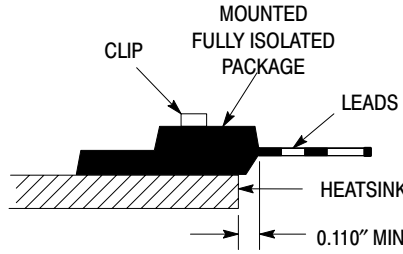


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

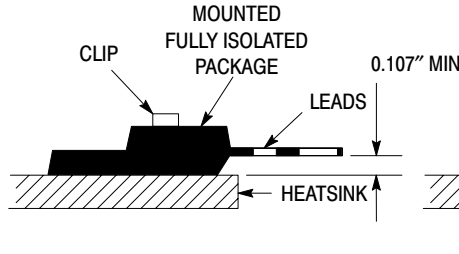


Figure 22b. Clip Mounting Position for Isolation Test Number 2

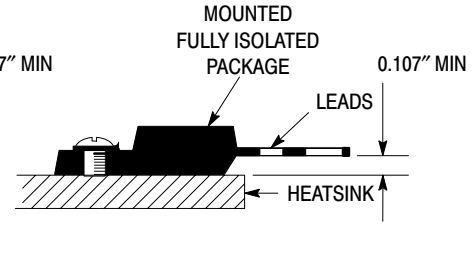


Figure 22c. Screw Mounting Position for Isolation Test Number 3

\*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION\*\*

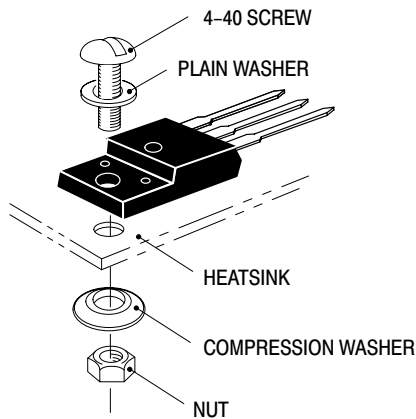


Figure 23a. Screw-Mounted

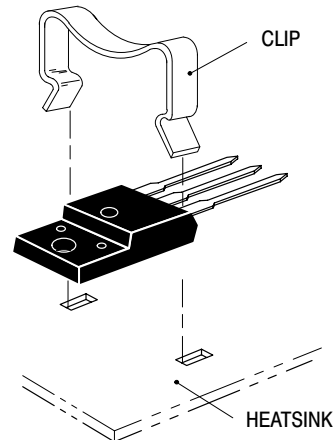


Figure 23b. Clip-Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.

# Complementary Silicon Power Plastic Transistors

... designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage —  
 $V_{CE(sus)} = 25 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain —  
 $h_{FE} = 70 \text{ (Min) @ } I_C = 500 \text{ mAdc}$   
 $= 45 \text{ (Min) @ } I_C = 2.0 \text{ Adc}$   
 $= 10 \text{ (Min) @ } I_C = 5.0 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage —  
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$   
 $= 0.75 \text{ Vdc (Max) @ } I_C = 2.0 \text{ Adc}$
- High Current-Gain — Bandwidth Product —  
 $f_T = 65 \text{ MHz (Min) @ } I_C$   
 $= 100 \text{ mAdc}$
- Annular Construction for Low Leakage —  
 $I_{CBO} = 100 \text{ nAdc @ Rated } V_{CB}$

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CB}$	40	Vdc
Collector-Emitter Voltage	$V_{CEO}$	25	Vdc
Emitter-Base Voltage	$V_{EB}$	8.0	Vdc
Collector Current — Continuous Peak	$I_C$	5.0 10	Adc
Base Current	$I_B$	1.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	15 0.12	Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.5 0.012	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

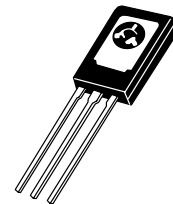
## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	8.34	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	83.4	$^\circ\text{C/W}$

**NPN**  
**MJE200\***  
**PNP**  
**MJE210\***

\*ON Semiconductor Preferred Device

**5 AMPERE**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**25 VOLTS**  
**15 WATTS**



**CASE 77-09**  
**TO-225AA**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJE200 MJE210

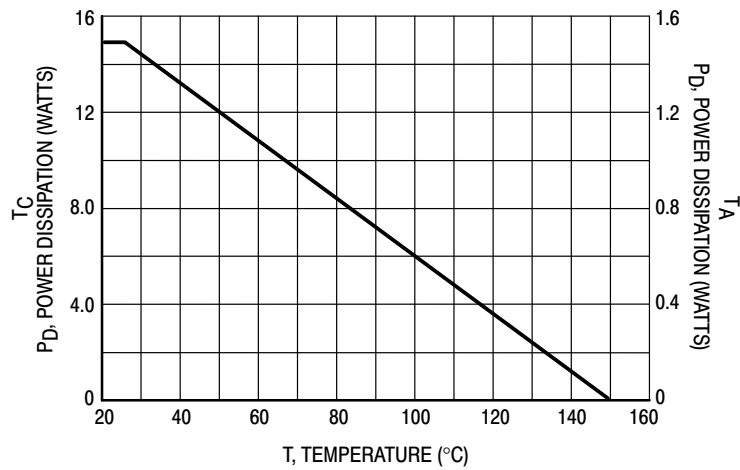


Figure 1. Power Derating

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) (I <sub>C</sub> = 10 mAdc, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	25	—	Vdc
Collector Cutoff Current (V <sub>CB</sub> = 40 Vdc, I <sub>E</sub> = 0) (V <sub>CB</sub> = 40 Vdc, I <sub>E</sub> = 0, T <sub>J</sub> = 125°C)	I <sub>CBO</sub>	—	100	nAdc μAdc
Emitter Cutoff Current (V <sub>BE</sub> = 8.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	100	nAdc

### ON CHARACTERISTICS

DC Current Gain (1) (I <sub>C</sub> = 500 mAdc, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 2.0 Adc, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 5.0 Adc, V <sub>CE</sub> = 2.0 Vdc)	h <sub>FE</sub>	70 45 10	— 180 —	—
Collector–Emitter Saturation Voltage (1) (I <sub>C</sub> = 500 mAdc, I <sub>B</sub> = 50 mAdc) (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 200 mAdc) (I <sub>C</sub> = 5.0 Adc, I <sub>B</sub> = 1.0 Adc)	V <sub>CE(sat)</sub>	— — —	0.3 0.75 1.8	Vdc
Base–Emitter Saturation Voltage (1) (I <sub>C</sub> = 5.0 Adc, I <sub>B</sub> = 1.0 Adc)	V <sub>BE(sat)</sub>	—	2.5	Vdc
Base–Emitter On Voltage (1) (I <sub>C</sub> = 2.0 Adc, V <sub>CE</sub> = 1.0 Vdc)	V <sub>BE(on)</sub>	—	1.6	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product (2) (I <sub>C</sub> = 100 mAdc, V <sub>CE</sub> = 10 Vdc, f <sub>test</sub> = 10 MHz)	f <sub>T</sub>	65	—	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	C <sub>ob</sub>	—	80 120	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2.0%.

(2) f<sub>T</sub> = |h<sub>fe</sub>| • f<sub>test</sub>.

# MJE200 MJE210

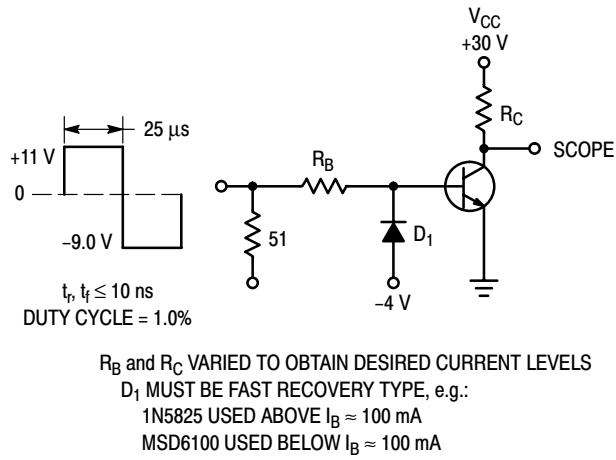


Figure 2. Switching Time Test Circuit

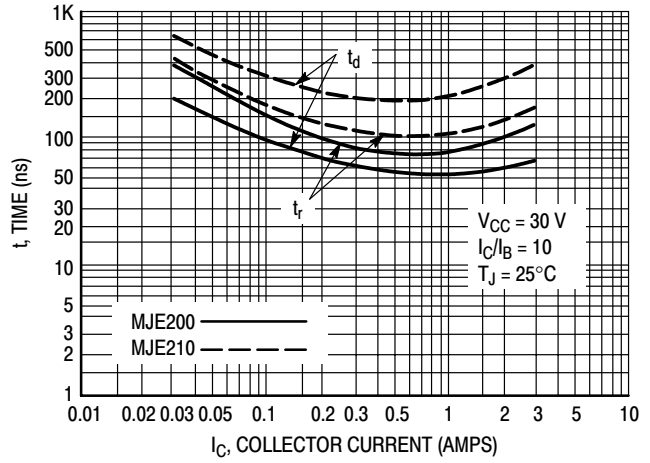


Figure 3. Turn-On Time

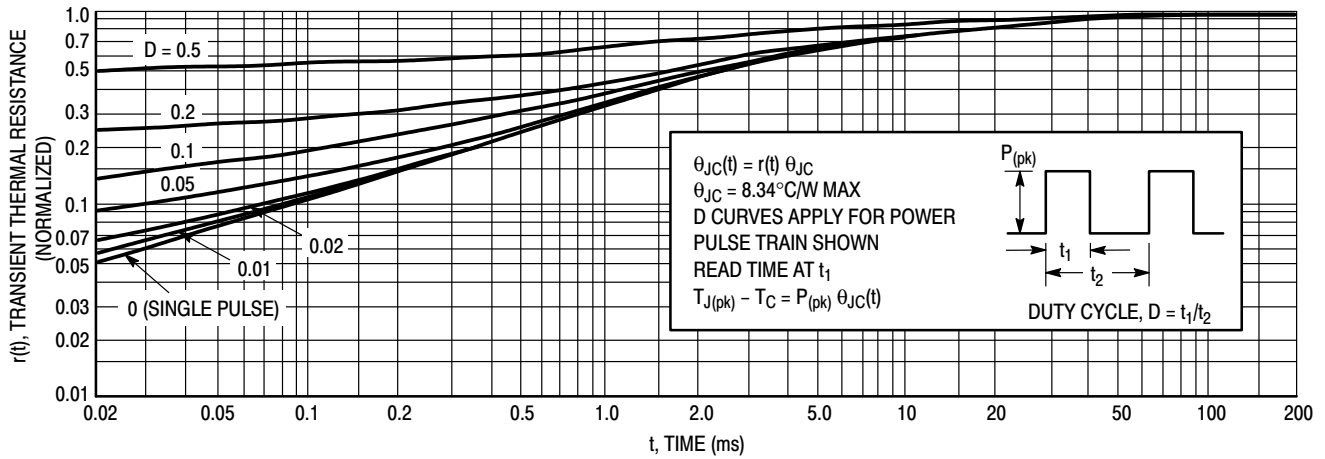
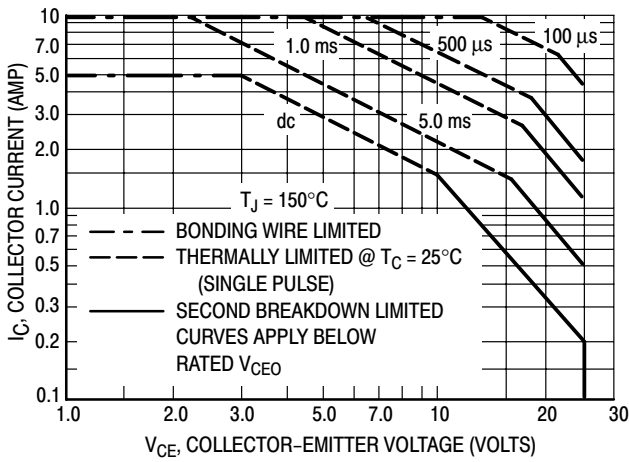


Figure 4. Thermal Response

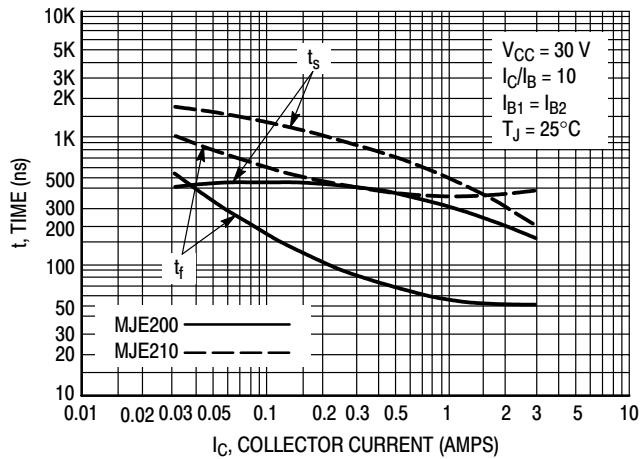
# MJE200 MJE210



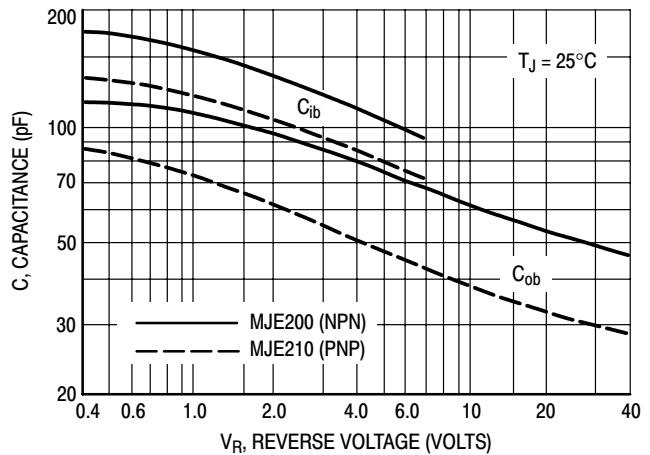
**Figure 5. Active Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 6. Turn-Off Time**



**Figure 7. Capacitance**



# MJE200 MJE210

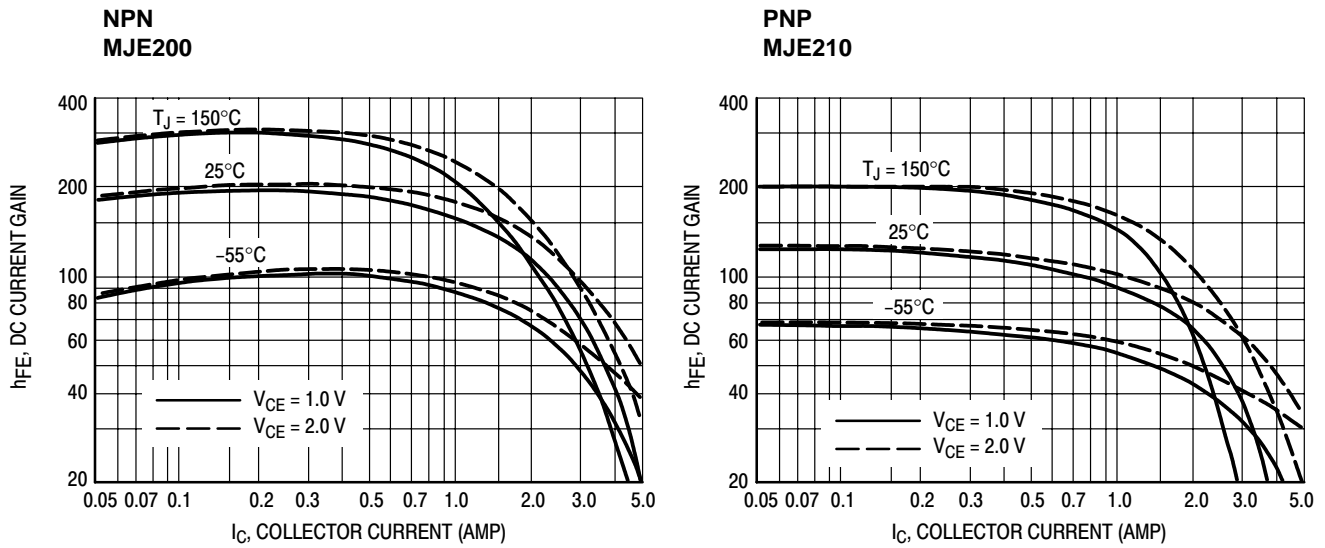


Figure 8. DC Current Gain

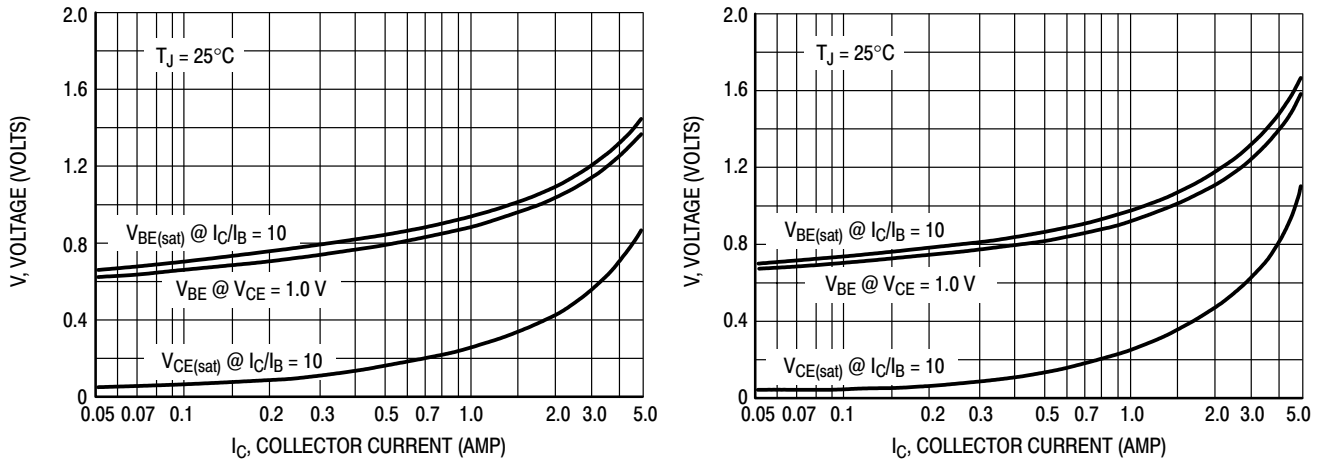


Figure 9. "On" Voltage

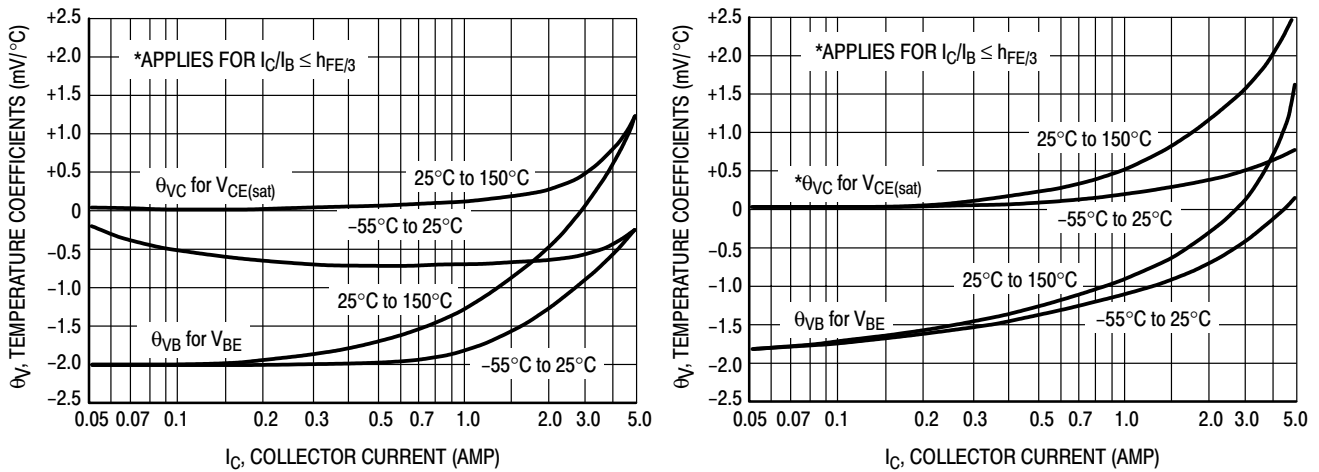


Figure 10. Temperature Coefficients

# Complementary Silicon Power Plastic Transistors

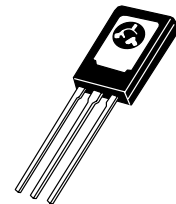
... designed for low power audio amplifier and low-current, high-speed switching applications.

- High Collector–Emitter Sustaining Voltage —  
 $V_{CE(sus)} = 100 \text{ Vdc (Min) — MJE243, MJE253}$
- High DC Current Gain @  $I_C = 200 \text{ mAdc}$   
 $h_{FE} = 40\text{--}200$   
 $= 40\text{--}120 \text{ — MJE243, MJE253}$
- Low Collector–Emitter Saturation Voltage —  
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$
- High Current Gain Bandwidth Product —  
 $f_T = 40 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakages  
 $I_{CBO} = 100 \text{ nAdc (Max) @ Rated } V_{CB}$

**NPN**  
**MJE243\***  
**PNP**  
**MJE253\***

\*ON Semiconductor Preferred Device

**4 AMPERE**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**100 VOLTS**  
**15 WATTS**



**CASE 77-09**  
**TO-225AA**

## MAXIMUM RATINGS

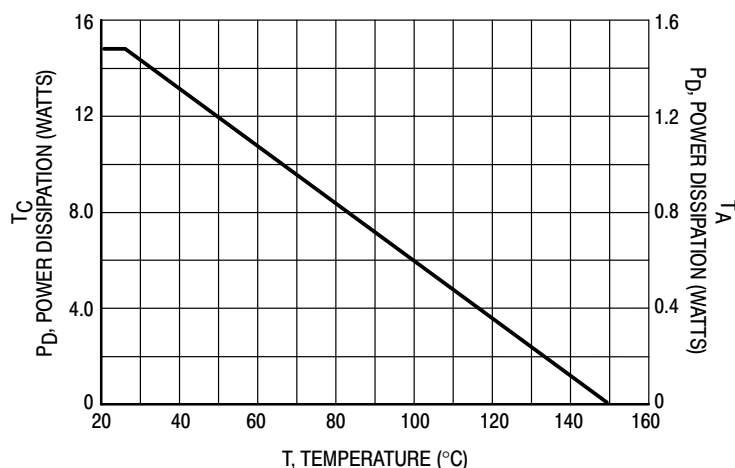
Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	100	Vdc
Collector–Base Voltage	$V_{CB}$	100	Vdc
Emitter–Base Voltage	$V_{EB}$	7.0	Vdc
Collector Current — Continuous Peak	$I_C$	4.0 8.0	Adc
Base Current	$I_B$	10	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	15 0.12	Watts W/ac
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate @ $25^\circ\text{C}$	$P_D$	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	°C

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	8.34	°C/W
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	83.4	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

## MJE243 MJE253



**Figure 1. Power Derating**

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage ( $I_C = 10\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CE} = 100\text{ Vdc}$ , $I_E = 0$ , $T_C = 125^\circ\text{C}$ )	$I_{CBO}$	—	0.1	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 7.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	0.1	$\mu\text{Adc}$
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = 200\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )	$h_{FE}$	40 15	180 —	—
Collector–Emitter Saturation Voltage ( $I_C = 500\text{ mAdc}$ , $I_B = 50\text{ mAdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $I_B = 100\text{ mAdc}$ )	$V_{CE(sat)}$	— —	0.3 0.6	Vdc
Base–Emitter Saturation Voltage ( $I_C = 2.0\text{ Adc}$ , $I_B = 200\text{ mAdc}$ )	$V_{BE(sat)}$	—	1.8	Vdc
Base–Emitter On Voltage ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ )	$V_{BE(on)}$	—	1.5	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain — Bandwidth Product ( $I_C = 100\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 10\text{ MHz}$ )	$f_T$	40	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	—	50	pF

# MJE243 MJE253

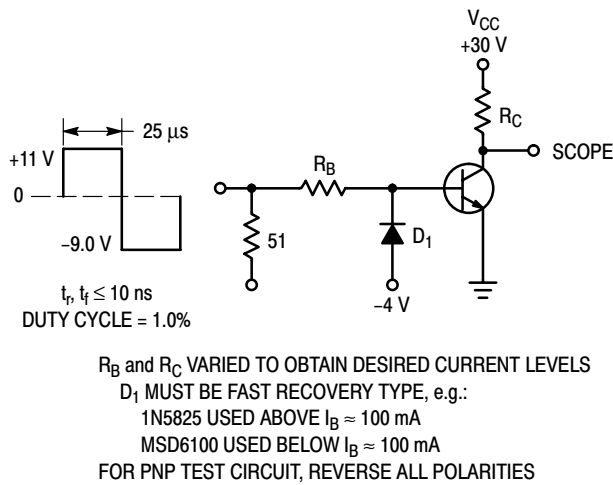


Figure 2. Switching Time Test Circuit

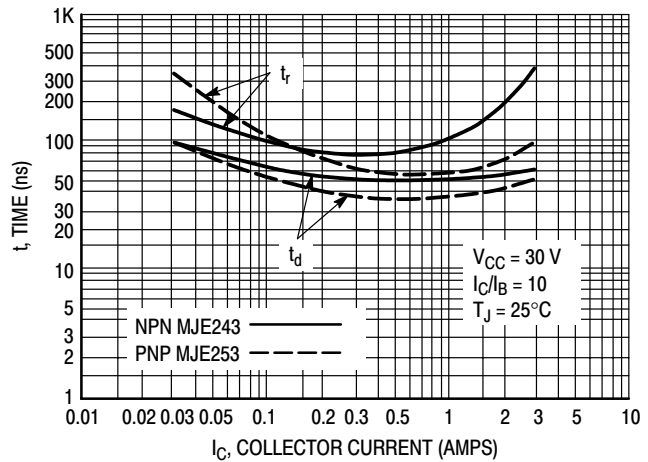


Figure 3. Turn-On Time

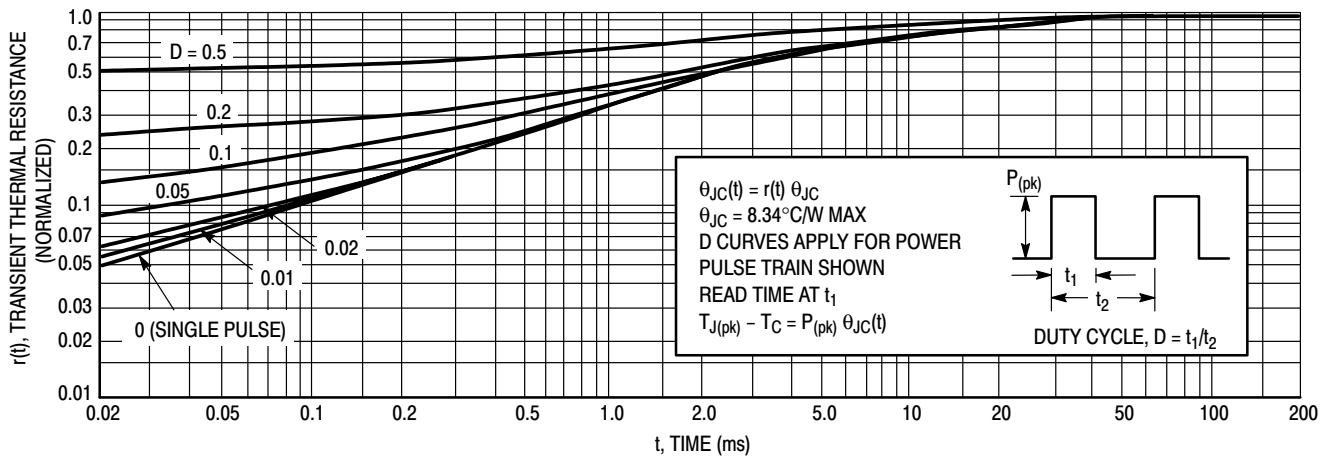


Figure 4. Thermal Response

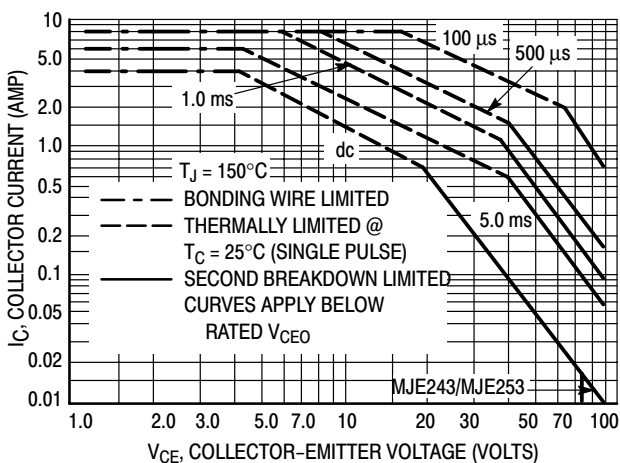


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# MJE243 MJE253

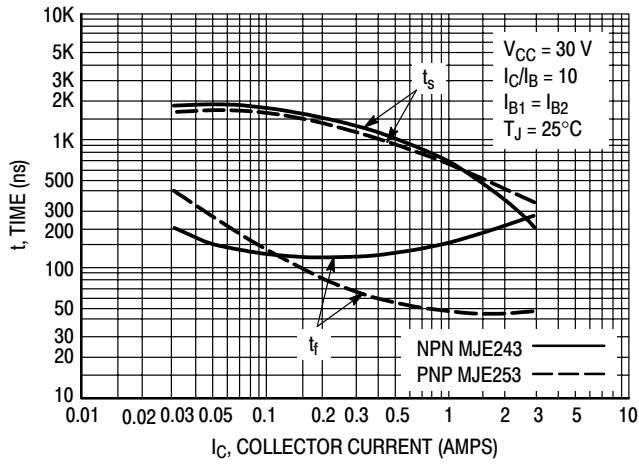


Figure 6. Turn-Off Time

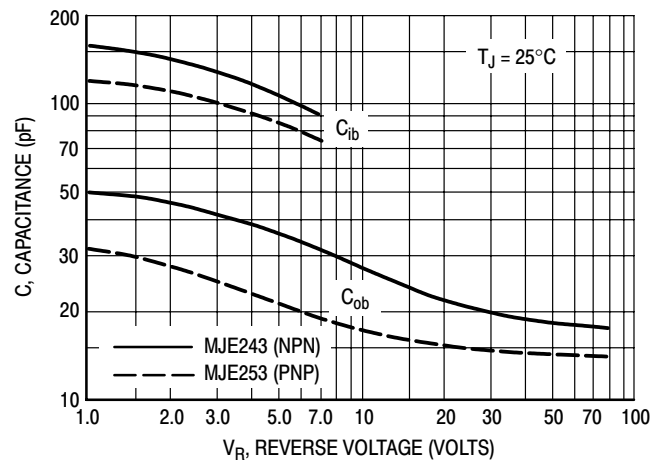


Figure 7. Capacitance

# MJE243 MJE253

**NPN  
MJE243**

**PNP  
MJE253**

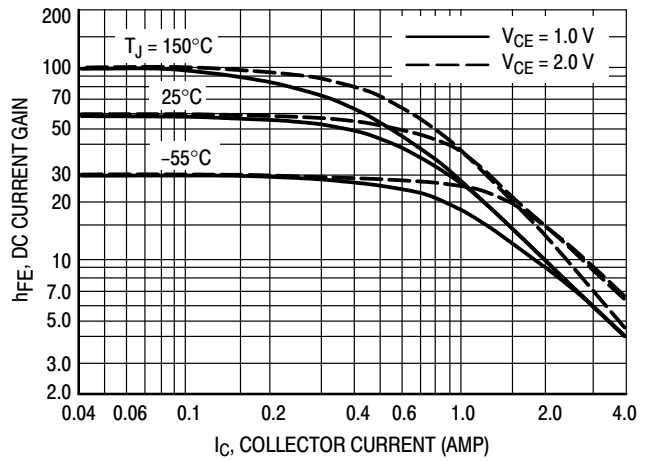
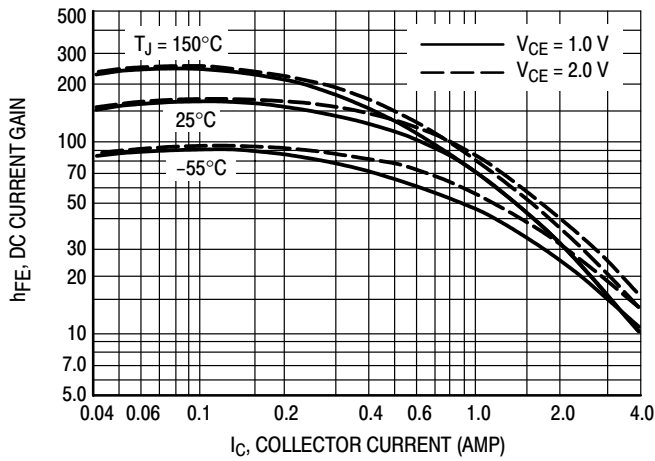


Figure 8. DC Current Gain

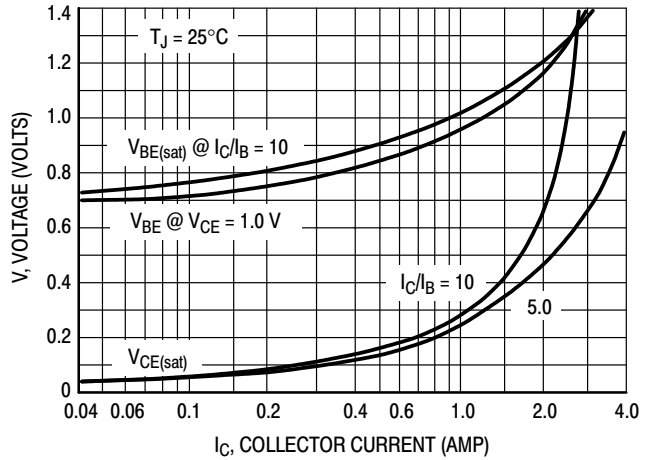
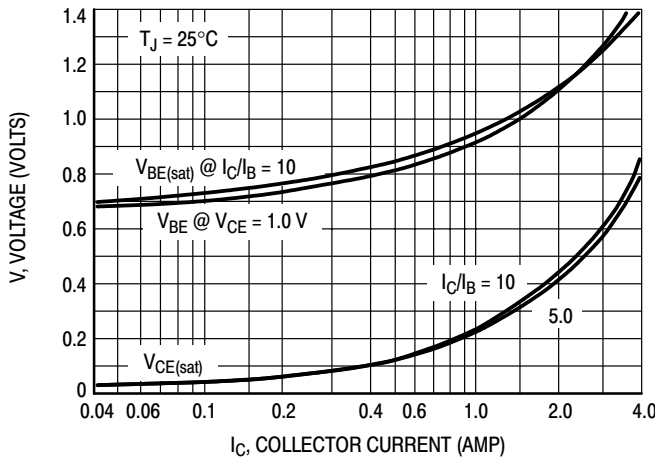


Figure 9. "On" Voltages

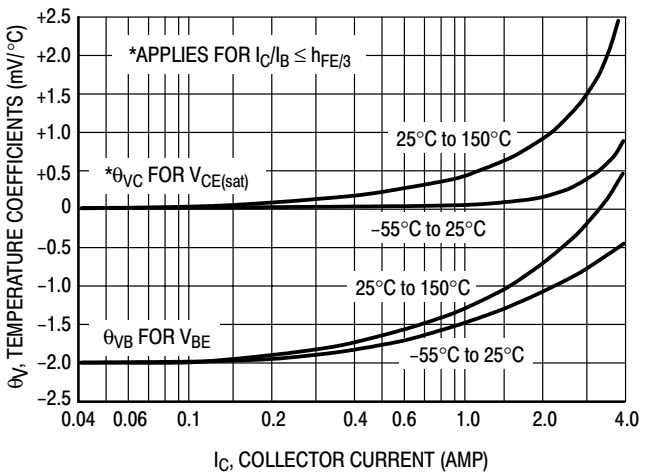
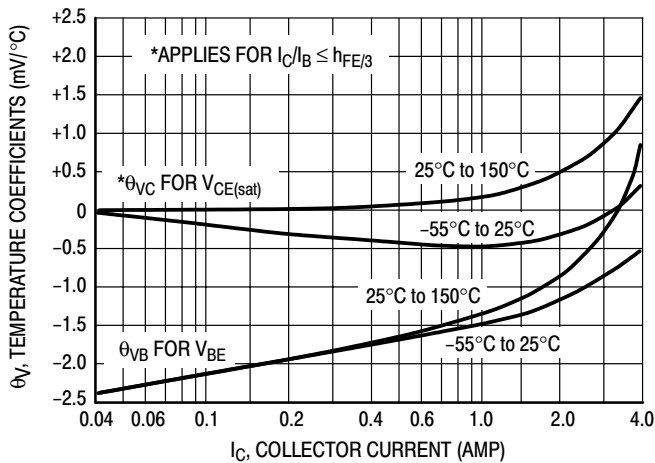


Figure 10. Temperature Coefficients

# Complementary Silicon Power Transistors

... designed specifically for use with the MC3419 Solid-State Subscriber Loop Interface Circuit (SLIC).

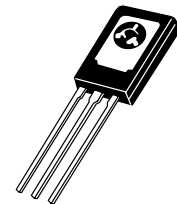
- High Safe Operating Area  
 $I_{S/B} @ 40 \text{ V}, 1.0 \text{ s} = 0.375 \text{ A} \text{ — TO-126}$
- Collector-Emitter Sustaining Voltage  
 $V_{CEO(sus)} = 100 \text{ Vdc (Min)}$
- High DC Current Gain  
 $h_{FE} @ 120 \text{ mA}, 10 \text{ V} = 1500 \text{ (Min)}$

**NPN  
MJE270  
PNP  
MJE271**

**2.0 AMPERE  
COMPLEMENTARY  
POWER DARLINGTON  
TRANSISTORS  
100 VOLTS  
15 WATTS**

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous — Peak	$I_C$	2.0 4.0	Adc
Base Current	$I_B$	0.1	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	15 0.12	Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.5 0.012	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$



**CASE 77-09  
TO-225AA TYPE**

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	$^\circ\text{C/W}$

# MJE270 MJE271

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Sustaining Voltage (1) ( $I_C = 10\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current ( $V_{CE} = 100\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	1.0	mAdc
Collector Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	0.3	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	0.1	mAdc

## SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 40\text{ Vdc}$ , $t = 1.0\text{ s}$ , non-repetitive)	$I_{S/b}$	375	—	Adc
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## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 20\text{ mAdc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 120\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ )	$h_{FE}$	500 1500	— —	—
Collector-Emitter Saturation Voltage ( $I_C = 20\text{ mAdc}$ , $I_B = 0.2\text{ mAdc}$ ) ( $I_C = 120\text{ mAdc}$ , $I_B = 1.2\text{ mAdc}$ )	$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base-Emitter On Voltage ( $I_C = 120\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ )	$V_{BE(on)}$	—	2.0	Vdc

## DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product (2) ( $I_C = 0.05\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	6.0	—	MHz
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### NOTES:

- (1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .
- (2)  $f_T = |h_{fe}| \cdot f_{test}$ .

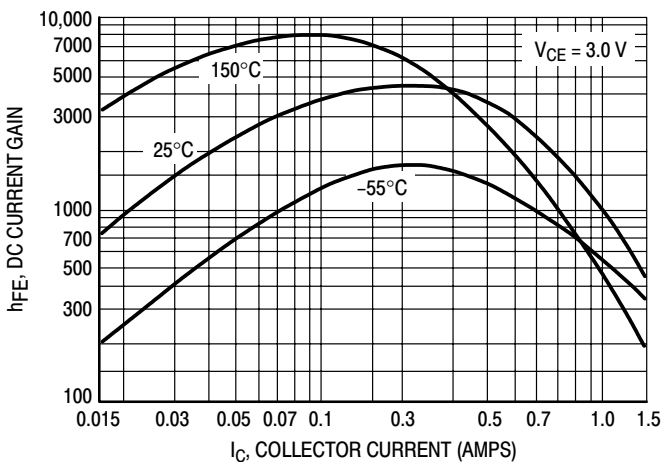


Figure 1. DC Current Gain

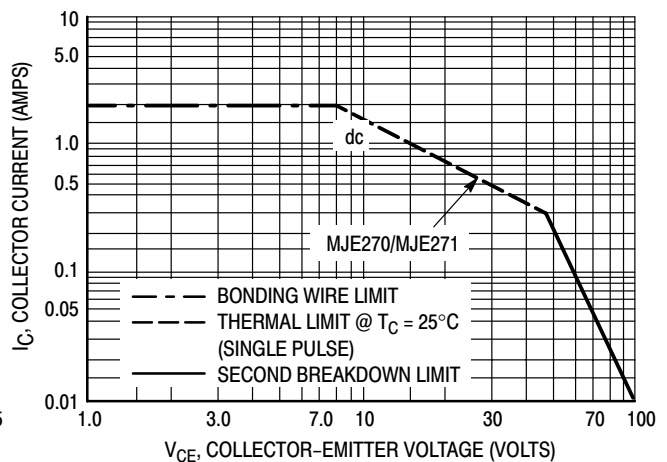


Figure 2. Safe Operating Area



# Complementary Silicon Plastic Power Transistors

... designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 10 Amperes
- High Current Gain — Bandwidth Product —  
 $f_T = 2.0 \text{ MHz (Min) @ } I_C = 500 \text{ mAdc}$

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	Vdc
Collector–Base Voltage	$V_{CB}$	70	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current	$I_C$	10	Adc
Base Current	$I_B$	6.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$ MJE3055T, MJE2955T	$P_{D†}$	75 0.6	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	1.67	$^\circ\text{C/W}$

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

**PNP  
MJE2955T\*  
NPN  
MJE3055T\***

\*ON Semiconductor Preferred Device

**10 AMPERE  
COMPLEMENTARY  
SILICON  
POWER TRANSISTORS  
60 VOLTS  
75 WATTS**

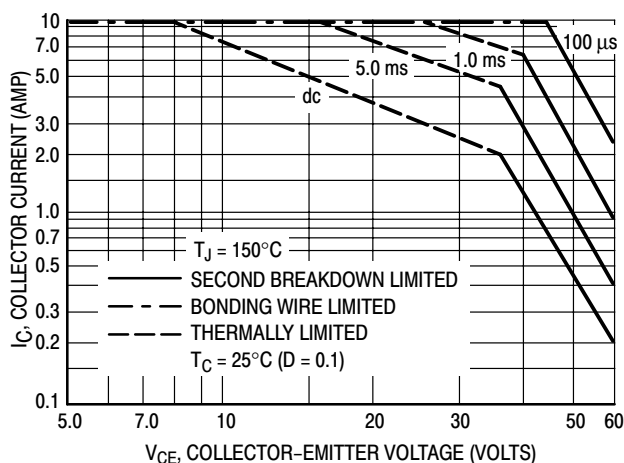
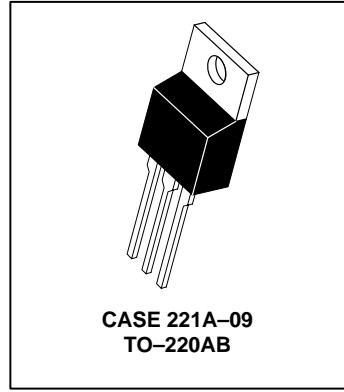


Figure 1. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on  $T_{J(pk)} = 150^\circ\text{C}$ .  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJE2955T MJE3055T

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	700	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 70\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 70\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	— —	1.0 5.0	mAdc
Collector Cutoff Current ( $V_{CB} = 70\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 70\text{ Vdc}$ , $I_E = 0$ , $T_C = 150^\circ\text{C}$ )	$I_{CBO}$	— —	1.0 10	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	5.0	mAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain (1) ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 10\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	20 5.0	100 —	—
Collector–Emitter Saturation Voltage (1) ( $I_C = 4.0\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 3.3\text{ Adc}$ )	$V_{CE(sat)}$	— —	1.1 8.0	Vdc
Base–Emitter On Voltage (1) ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	1.8	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain–Bandwidth Product ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 500\text{ kHz}$ )	$f_T$	2.0	—	MHz

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 20\%$ .

# MJE2955T MJE3055T

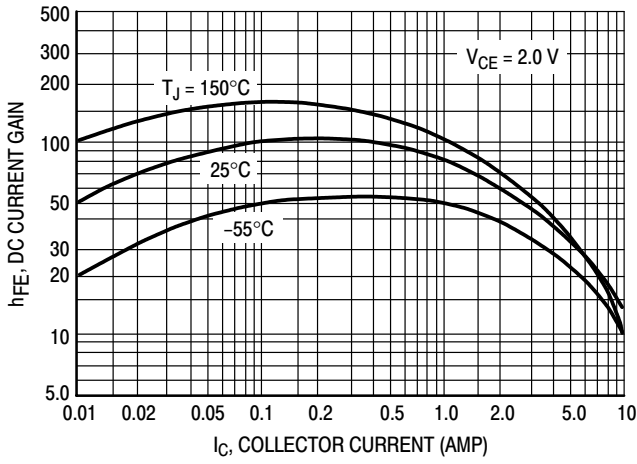


Figure 2. DC Current Gain

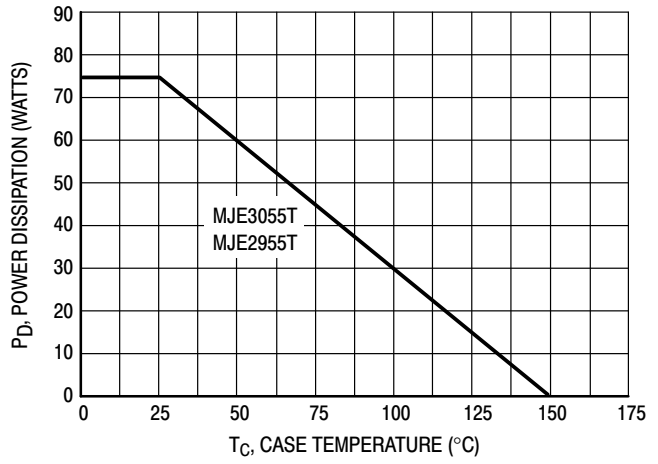


Figure 3. Power Derating

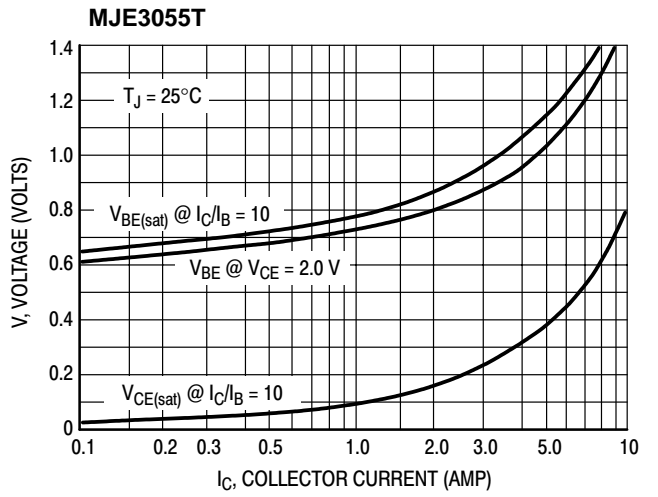
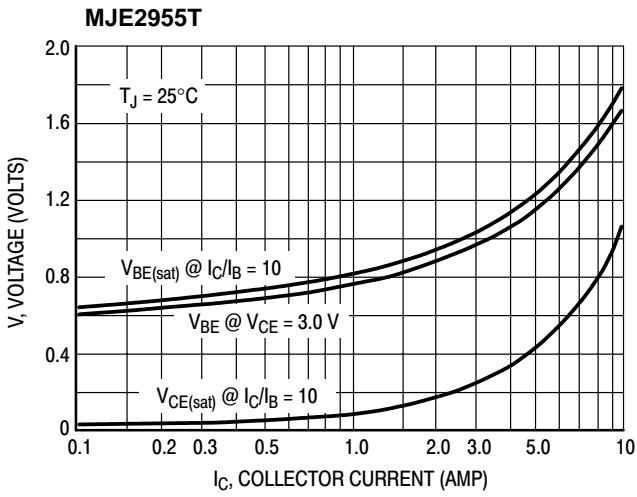


Figure 4. "On" Voltages

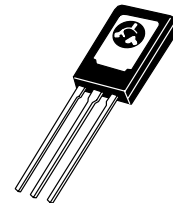
# Plastic Medium Power NPN Silicon Transistor

... useful for high-voltage general purpose applications.

- Suitable for Transformerless, Line-Operated Equipment
- Thermopad Construction Provides High Power Dissipation Rating for High Reliability

## MJE340

**0.5 AMPERE  
POWER TRANSISTOR  
NPN SILICON  
300 VOLTS  
20 WATTS**



**CASE 77-09  
TO-225AA TYPE**

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	300	Vdc
Emitter-Base Voltage	$V_{EB}$	3.0	Vdc
Collector Current — Continuous	$I_C$	500	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	6.25	$^\circ\text{C/W}$

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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#### OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ( $I_C = 1.0$ mAdc, $I_B = 0$ )	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current ( $V_{CB} = 300$ Vdc, $I_E = 0$ )	$I_{CBO}$	—	100	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = 3.0$ Vdc, $I_C = 0$ )	$I_{EBO}$	—	100	$\mu\text{Adc}$

#### ON CHARACTERISTICS

DC Current Gain ( $I_C = 50$ mAdc, $V_{CE} = 10$ Vdc)	$h_{FE}$	30	240	—
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## MJE340

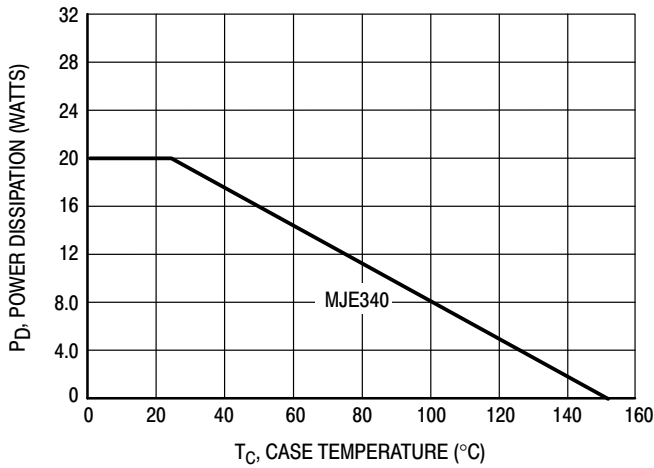


Figure 5. Power Temperature Derating

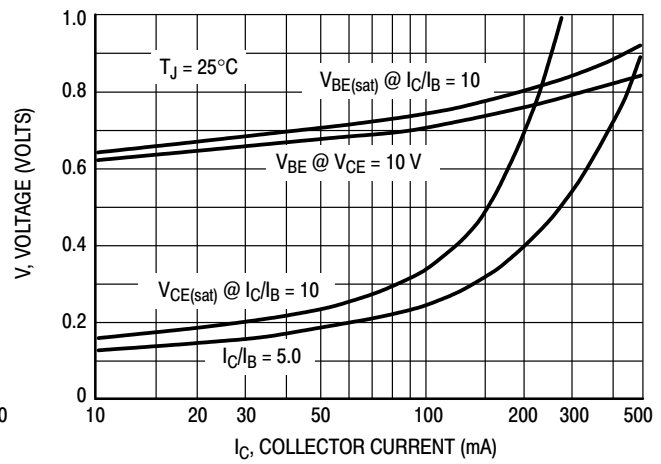


Figure 6. "On" Voltages

### ACTIVE-REGION SAFE OPERATING AREA

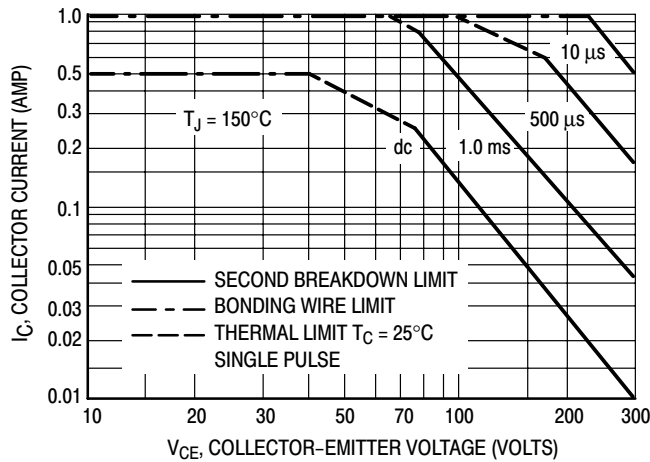


Figure 7. MJE340

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# MJE340

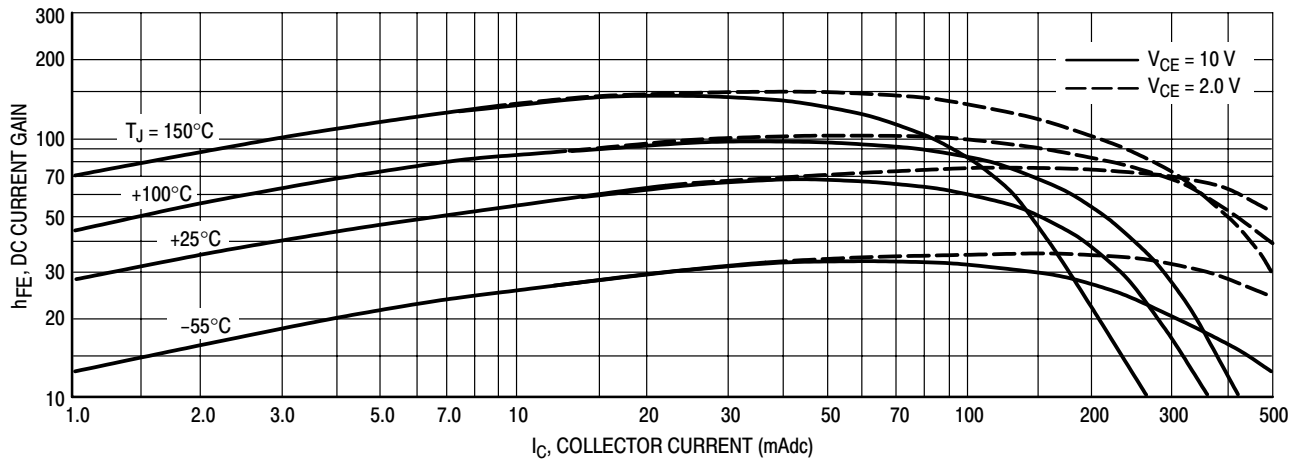


Figure 8. DC Current Gain

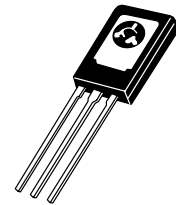
# NPN Silicon High-Voltage Power Transistors

... designed for use in line-operated equipment requiring high  $f_T$ .

- High DC Current Gain  
 $h_{FE} = 40-160 @ I_C$   
 $= 20 \text{ mAdc}$
- Current Gain Bandwidth Product —  
 $f_T = 15 \text{ MHz (Min) @ } I_C$   
 $= 10 \text{ mAdc}$
- Low Output Capacitance  
 $C_{ob} = 10 \text{ pF (Max) @ } f$   
 $= 1.0 \text{ MHz}$

**MJE3439**

**0.3 AMPERE  
POWER TRANSISTOR  
NPN SILICON  
350 VOLTS  
15 WATTS**



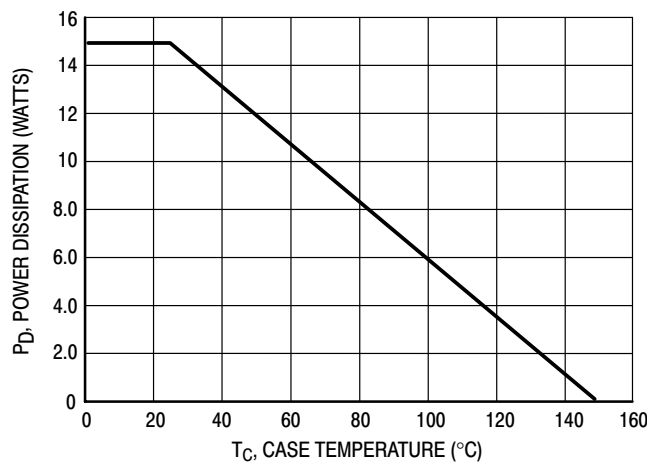
**CASE 77-09  
TO-225AA TYPE**

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	350	Vdc
Collector-Base Voltage	$V_{CB}$	450	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous	$I_C$	0.3	Adc
Base Current	$I_B$	150	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	15 0.12	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	8.33	$^\circ\text{C/W}$



**Figure 1. Power-Temperature Derating Curve**

# MJE3439

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage ( $I_C = 5.0\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	350	—	Vdc
Collector Cutoff Current ( $V_{CE} = 300\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	20	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 450\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ )	$I_{CEX}$	—	500	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CB} = 350\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	20	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	20	$\mu\text{Adc}$

## ON CHARACTERISTICS

DC Current Gain ( $I_C = 2.0\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ ) ( $I_C = 20\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ )	$h_{FE}$	30 15	— 200	—
Collector–Emitter Saturation Voltage ( $I_C = 50\text{ mAdc}$ , $I_B = 4.0\text{ mAdc}$ )	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter Saturation Voltage ( $I_C = 50\text{ mAdc}$ , $I_B = 4.0\text{ mAdc}$ )	$V_{BE(sat)}$	—	1.3	Vdc
Base–Emitter On Voltage ( $I_C = 50\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ )	$V_{BE(on)}$	—	0.8	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 10\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 5.0\text{ MHz}$ )	$f_T$	15	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	$C_{ob}$	—	10	pF
Small–Signal Current Gain ( $I_C = 5.0\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	25	—	—

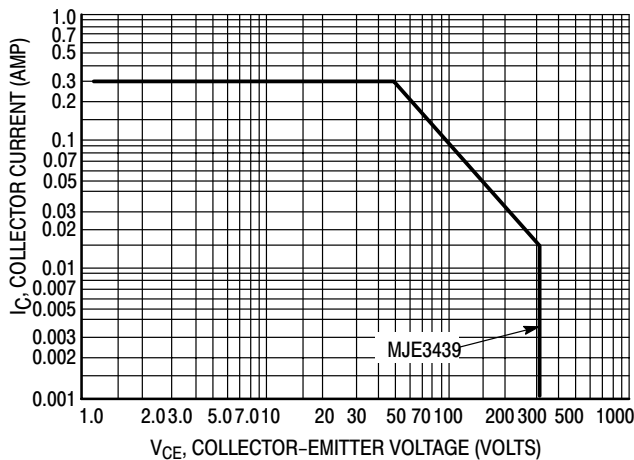


Figure 2. Active–Region Safe Operating Area

The Safe Operating Area Curves indicate  $I_C - V_{CE}$  limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum  $T_J$ , power–temperature derating must be observed for both steady state and pulse power conditions.



# Plastic NPN Silicon Medium-Power Transistor

... useful for medium voltage applications requiring high  $f_T$  such as converters and extended range amplifiers.

## MAXIMUM RATINGS

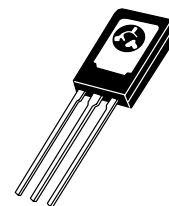
Rating	Symbol	MJE344	Unit
Collector–Emitter Voltage	$V_{CEO}$	200	Vdc
Collector–Base Voltage	$V_{CB}$	200	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous	$I_C$	500	mAdc
Base Current	$I_B$	250	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

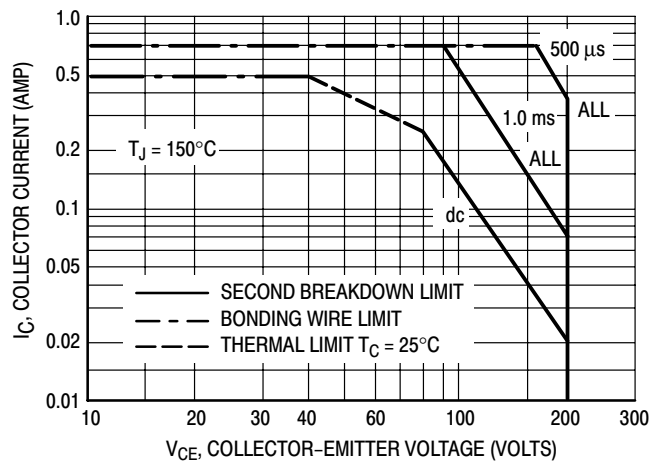
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	6.25	$^\circ\text{C}/\text{W}$

**MJE344**

**0.5 AMPERE  
POWER TRANSISTOR  
NPN SILICON  
150–200 VOLTS  
20 WATTS**



**CASE 77-09  
TO-225AA TYPE**



**Figure 1. Active Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# MJE344

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage ( $I_C = 1.0\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	200	—	Vdc
Collector Cutoff Current ( $V_{CE} = 200\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	1.0	mAdc
Collector Cutoff Current ( $V_{CB} = 200\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	0.1	mAdc
Emitter Cutoff Current ( $V_{EB} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	0.1	mAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = 50\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ )	$h_{FE}$	30	300	—
Collector–Emitter Saturation Voltage ( $I_C = 50\text{ mAdc}$ , $I_B = 5.0\text{ mAdc}$ )	$V_{CE(sat)}$	—	1.0	Vdc
Base–Emitter On Voltage ( $I_C = 50\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ )	$V_{BE(on)}$	—	1.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain — Bandwidth Product ( $I_C = 50\text{ mAdc}$ , $V_{CE} = 25\text{ Vdc}$ , $f = 10\text{ MHz}$ )	$f_T$	15	—	MHz
Output Capacitance ( $V_{CB} = 20\text{ Vdc}$ , $I_E = 0$ , $f = 100\text{ kHz}$ )	$C_{ob}$	—	15	pF
Small–Signal Current Gain ( $I_C = 50\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	25	—	—

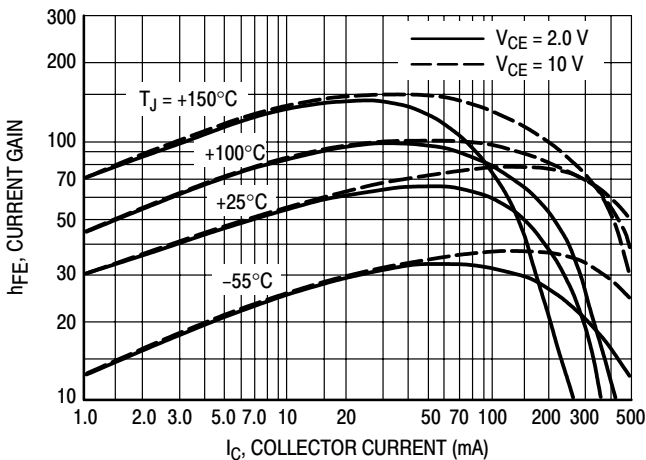


Figure 2. DC Current Gain

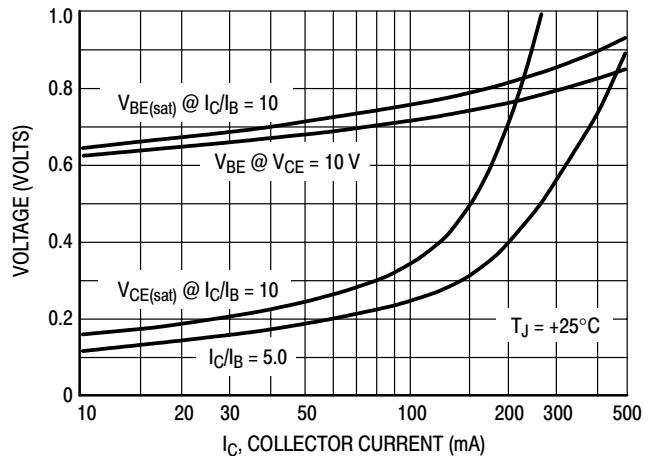


Figure 3. "On" Voltages

# Plastic Medium Power PNP Silicon Transistor

... designed for use in line-operated applications such as low power, line-operated series pass and switching regulators requiring PNP capability.

- High Collector–Emitter Sustaining Voltage —

$$V_{CEO(sus)} = 300 \text{ Vdc @ } I_C = 1.0 \text{ mAdc}$$

- Excellent DC Current Gain —

$$h_{FE} = 30\text{--}240 \text{ @ } I_C = 50 \text{ mAdc}$$

- Plastic Thermopad Package

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	300	Vdc
Emitter–Base Voltage	$V_{EB}$	3.0	Vdc
Collector Current — Continuous	$I_C$	500	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

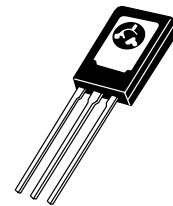
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	6.25	$^\circ\text{C/W}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage ( $I_C = 1.0 \text{ mAdc}, I_B = 0$ )	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current ( $V_{CB} = 300 \text{ Vdc}, I_E = 0$ )	$I_{CBO}$	—	100	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = 3.0 \text{ Vdc}, I_C = 0$ )	$I_{EBO}$	—	100	$\mu\text{Adc}$
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = 50 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$ )	$h_{FE}$	30	240	—

# MJE350

**0.5 AMPERE  
POWER TRANSISTOR  
PNP SILICON  
300 VOLTS  
20 WATTS**



**CASE 77–09  
TO–225AA TYPE**

# MJE350

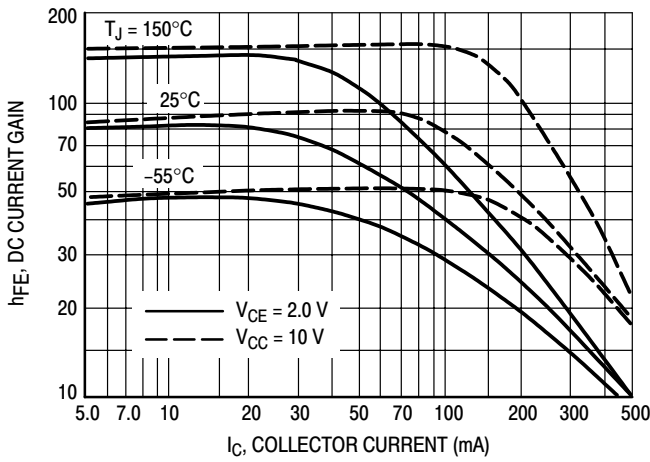


Figure 1. DC Current Gain

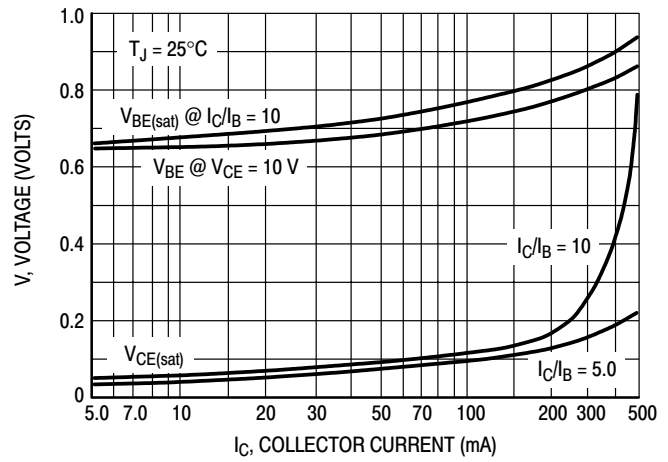


Figure 2. "On" Voltages

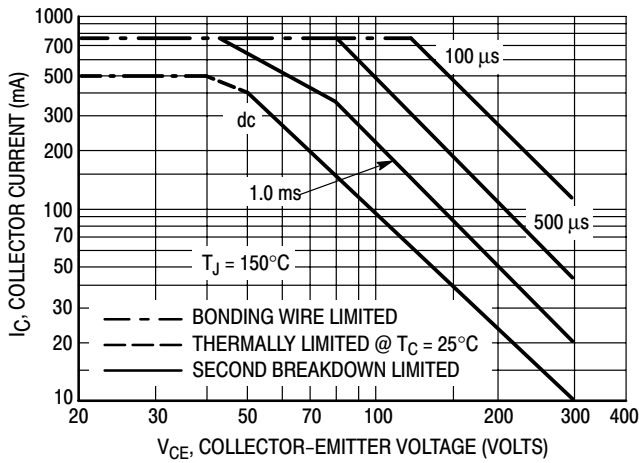


Figure 3. Active-Region Safe Operating Area

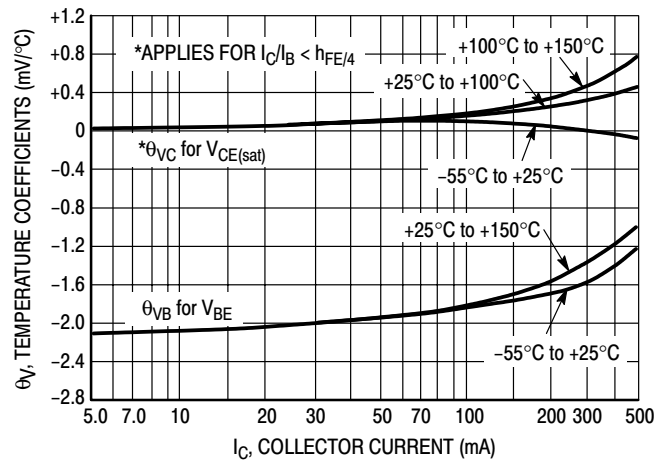


Figure 4. Temperature Coefficients

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

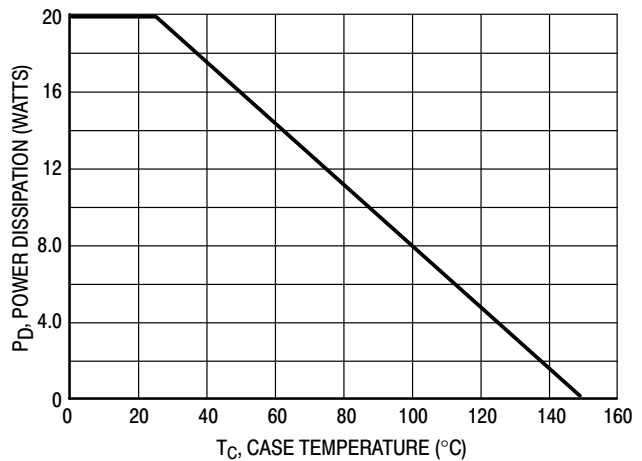


Figure 5. Power Derating

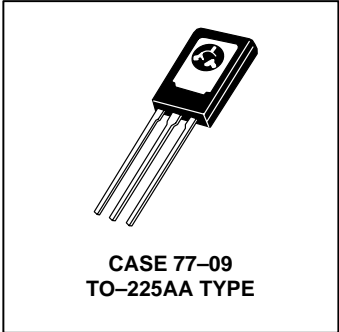
# Plastic Medium-Power PNP Silicon Transistors

... designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 20 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain —  
 $h_{FE} = 40 \text{ (Min) @ } I_C$   
 $= 1.0 \text{ Adc}$
- MJE371 is Complementary to NPN MJE521

**MJE371**

**4 AMPERE  
POWER TRANSISTOR  
PNP SILICON  
40 VOLTS  
40 WATTS**



## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	40	Vdc
Collector–Base Voltage	$V_{CB}$	40	Vdc
Emitter–Base Voltage	$V_{EB}$	4.0	Vdc
Collector Current — Continuous — Peak	$I_C$	4.0 8.0	Adc
Base Current — Continuous	$I_B$	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 320	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	3.12	$^\circ\text{C/W}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) ( $I_C = 100 \text{ mAdc}, I_B = 0$ )	$V_{CEO(sus)}$	40	—	Vdc
Collector–Base Cutoff Current ( $V_{CB} = 40 \text{ Vdc}, I_E = 0$ )	$I_{CBO}$	—	100	$\mu\text{Adc}$
Emitter–Base Cutoff Current ( $V_{EB} = 4.0 \text{ Vdc}, I_C = 0$ )	$I_{EBO}$	—	100	$\mu\text{Adc}$

### ON CHARACTERISTICS

DC Current Gain (1) ( $I_C = 1.0 \text{ Adc}, V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$	40	—	—
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(1) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

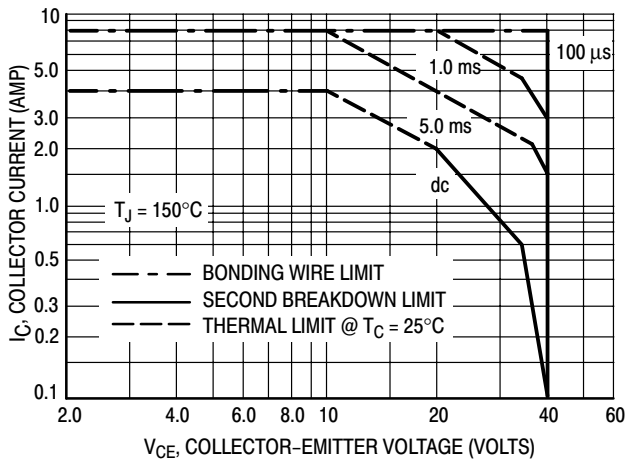


Figure 1. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

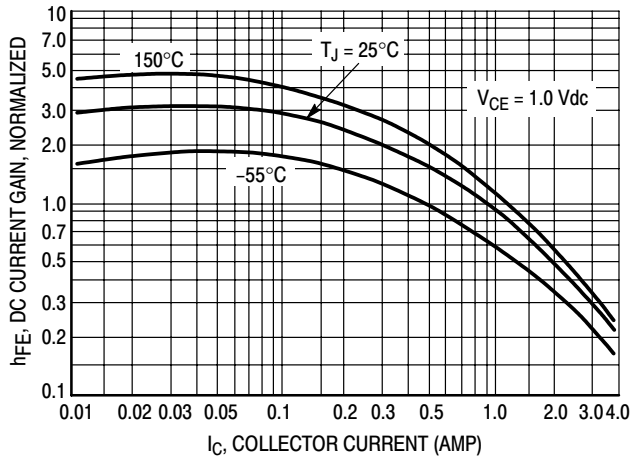


Figure 2. DC Current Gain

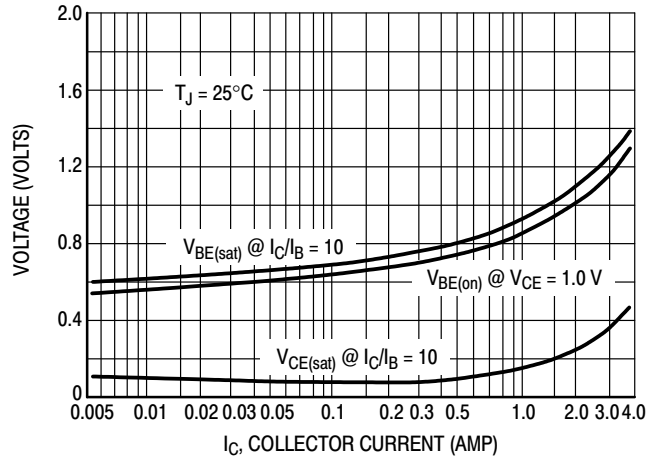


Figure 3. "On" Voltage

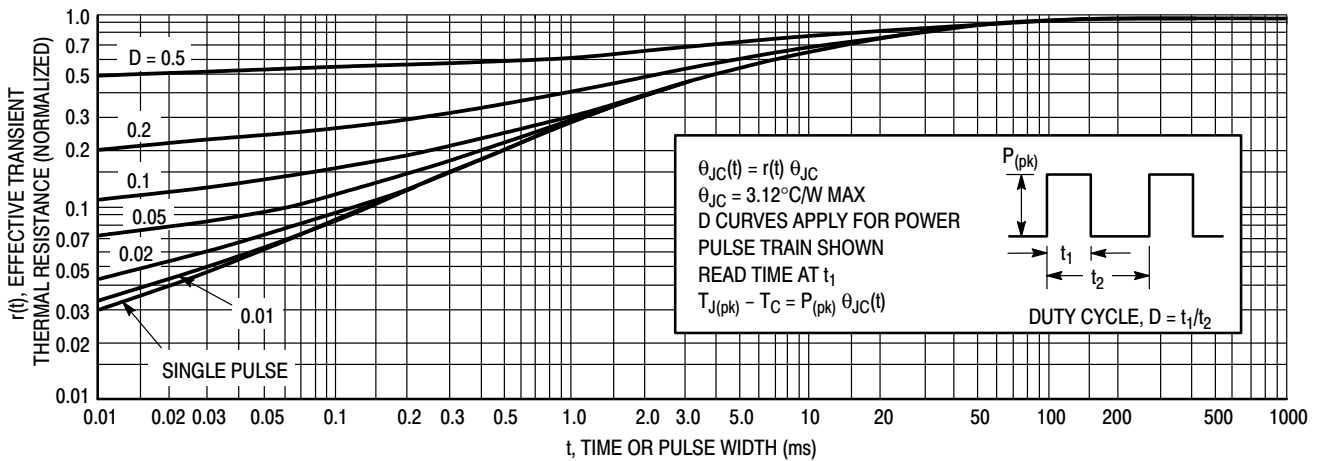


Figure 4. Thermal Response

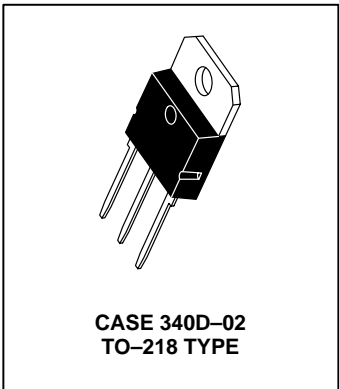
# High-Voltage — High Power Transistors

... designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector–Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 160 \text{ Vdc}$  — NPN MJE4343 PNP MJE4353
- High DC Current Gain — @  $I_C = 8.0 \text{ Adc}$   
 $h_{FE} = 35 \text{ (Typ)}$
- Low Collector–Emitter Saturation Voltage —  
 $V_{CE(sat)} = 2.0 \text{ Vdc (Max) @ } I_C = 8.0 \text{ Adc}$

**NPN  
MJE4343  
PNP  
MJE4353**

**16 AMPERE  
POWER TRANSISTORS  
COMPLEMENTARY  
SILICON  
160 VOLTS**



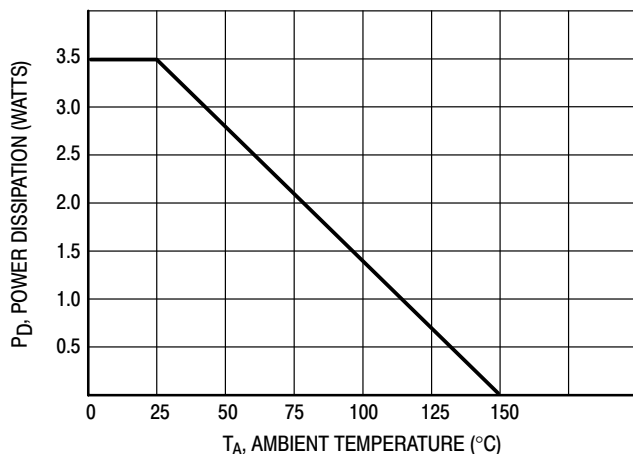
## MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	$V_{CEO}$	160	Vdc
Collector–Base Voltage	$V_{CB}$	160	Vdc
Emitter–Base Voltage	$V_{EB}$	7.0	Vdc
Collector Current — Continuous Peak (1)	$I_C$	16 20	A dc
Base Current — Continuous	$I_B$	5.0	A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	125	Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$

(1) Pulse Test: Pulse Width  $\leq 5.0 \mu\text{s}$ , Duty Cycle  $\geq 10\%$ .



**Figure 1. Power Derating  
Reference: Ambient Temperature**

# MJE4343 MJE4353

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	160	—	Vdc
Collector–Emitter Cutoff Current ( $V_{CE} = 80\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	750	$\mu\text{Adc}$
Collector–Emitter Cutoff Current ( $V_{CE} = \text{Rated } V_{CB}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CB}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	—	1.0 5.0	mAdc
Collector–Base Cutoff Current ( $V_{CB} = \text{Rated } V_{CB}$ , $I_E = 0$ )	$I_{CBO}$	—	750	$\mu\text{Adc}$
Emitter–Base Cutoff Current ( $V_{BE} = 7.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc

### ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 8.0\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ ) ( $I_C = 16\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	15 8.0	35 (Typ) 15 (Typ)	—
Collector–Emitter Saturation Voltage ( $I_C = 8.0\text{ Adc}$ , $I_B = 800\text{ mA}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 2.0\text{ Adc}$ )	$V_{CE(sat)}$	—	2.0 3.5	Vdc
Base–Emitter Saturation Voltage ( $I_C = 16\text{ Adc}$ , $I_B = 2.0\text{ Adc}$ )	$V_{BE(sat)}$	—	3.9	Vdc
Base–Emitter On Voltage ( $I_C = 16\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	3.9	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product (2) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 20\text{ Vdc}$ , $f_{test} = 0.5\text{ MHz}$ )	$f_T$	1.0	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	—	800	pF

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\geq 2.0\%$ .

(2)  $f_T = |h_{fe}| \cdot f_{test}$ .



# MJE4343 MJE4353

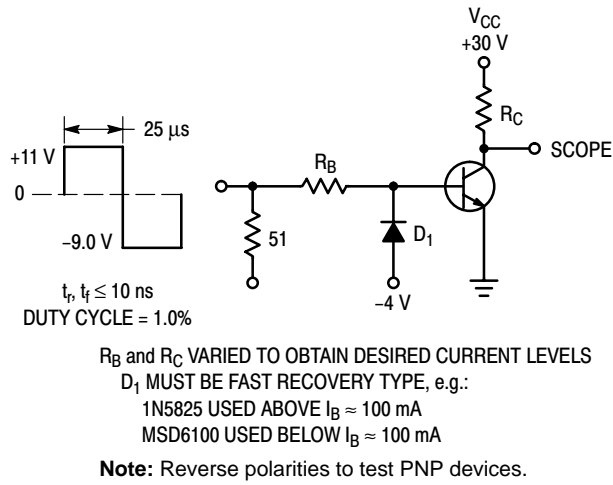


Figure 2. Switching Times Test Circuit

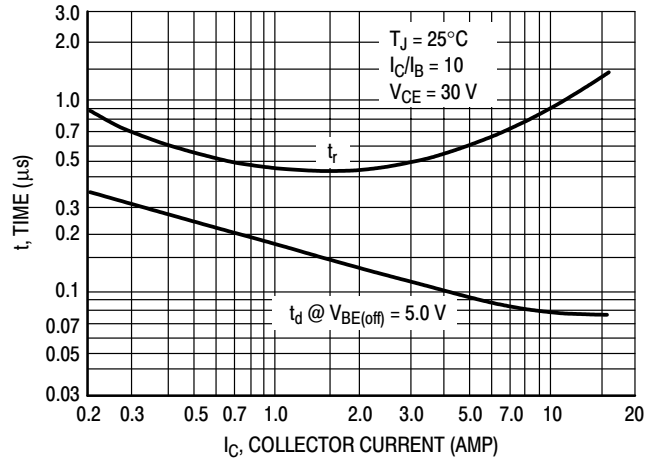


Figure 3. Typical Turn-On Time

## TYPICAL CHARACTERISTICS

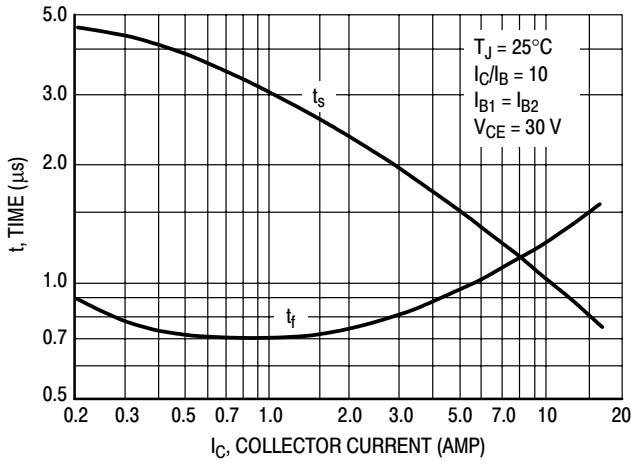


Figure 4. Turn-Off Time

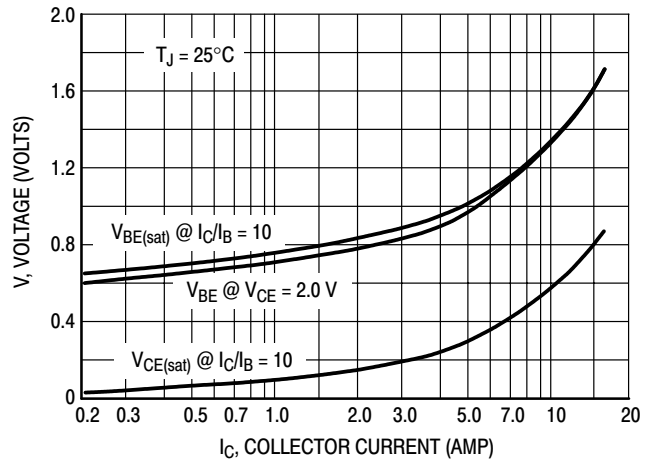


Figure 5. On Voltages

# MJE4343 MJE4353

## DC CURRENT GAIN

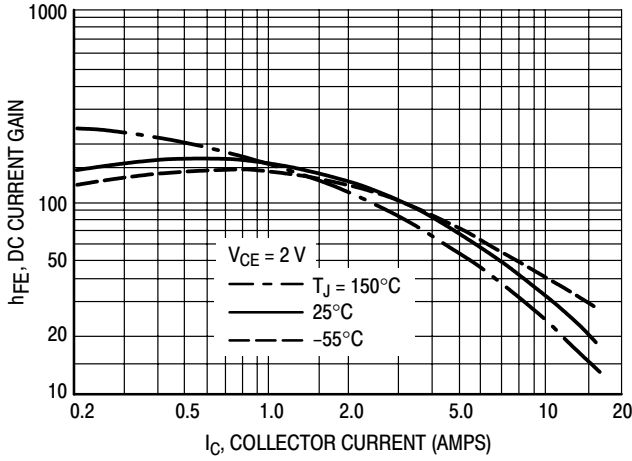


Figure 6. MJE4340 Series (NPN)

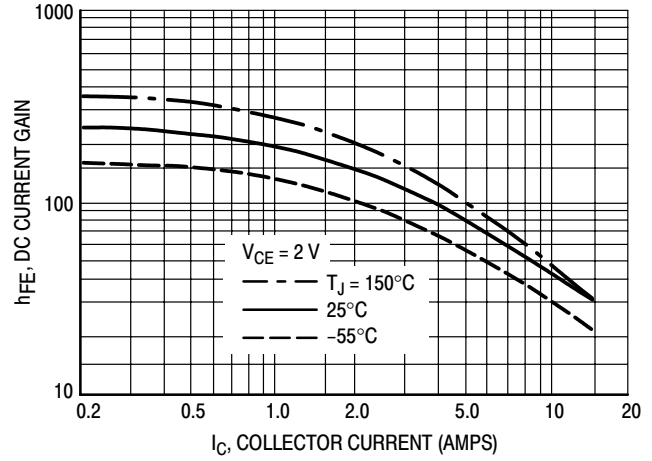


Figure 7. MJE4350 Series (PNP)

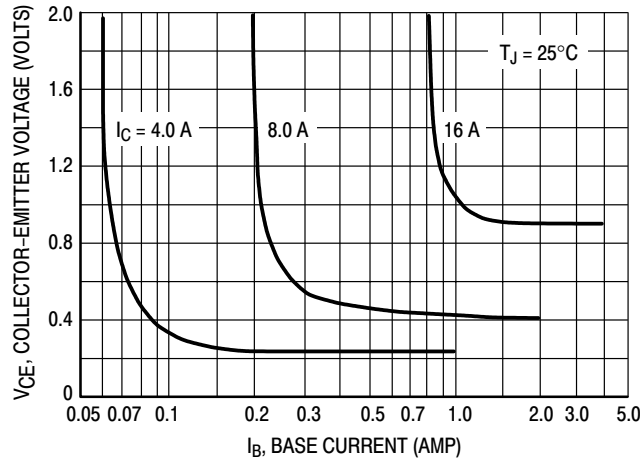


Figure 8. Collector Saturation Region

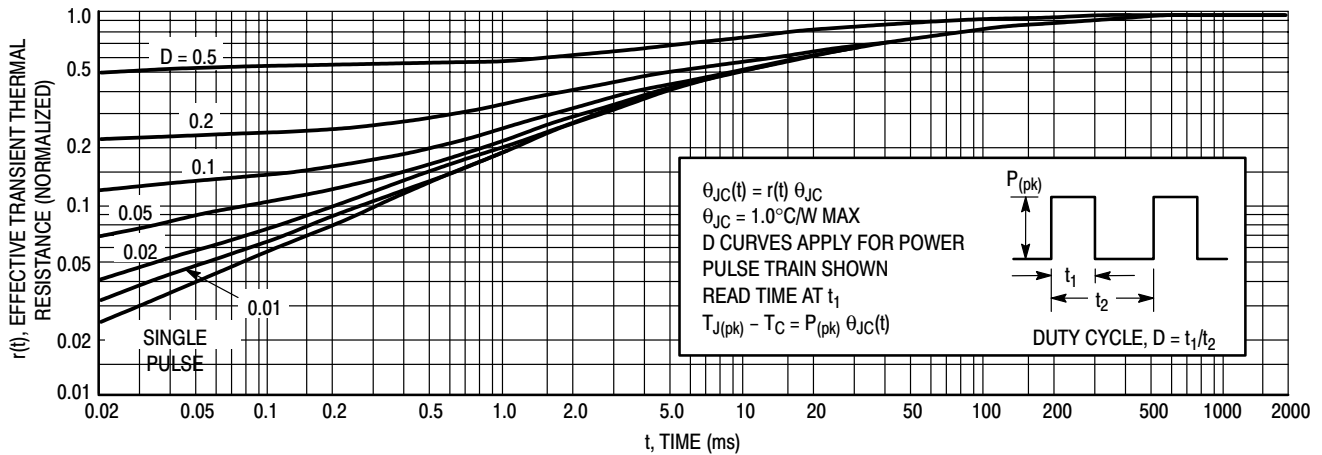


Figure 9. Thermal Response

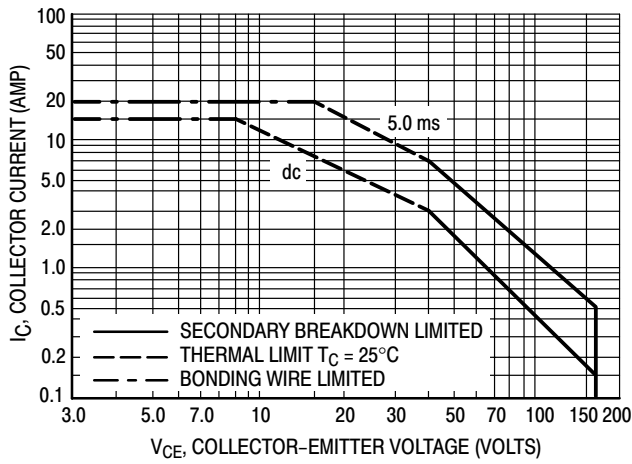


Figure 10. Maximum Forward Bias Safe Operating Area

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 11 gives RBSOA characteristics.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 9.

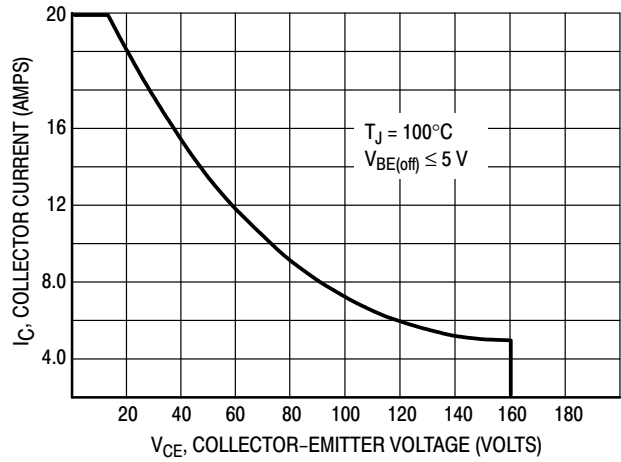


Figure 11. Maximum Reverse Bias Safe Operating Area

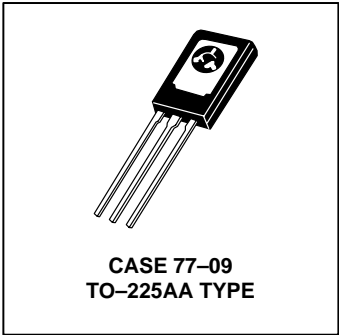
# Plastic Medium-Power NPN Silicon Transistor

... designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain —  
 $h_{FE} = 40 \text{ (Min) @ } I_C$   
 $= 1.0 \text{ Adc}$
- Complementary to PNP MJE371

**MJE521**

**4 AMPERE  
POWER TRANSISTOR  
NPN SILICON  
40 VOLTS  
40 WATTS**



## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	40	Vdc
Collector–Base Voltage	$V_{CB}$	40	Vdc
Emitter–Base Voltage	$V_{EB}$	4.0	Vdc
Collector Current — Continuous — Peak	$I_C$	4.0 8.0	Adc
Base Current — Continuous	$I_B$	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.32	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	3.12	$^\circ\text{C/W}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) ( $I_C = 100 \text{ mAdc}, I_B = 0$ )	$V_{CEO(sus)}$	40	—	Vdc
Collector–Base Cutoff Current ( $V_{CB} = 30 \text{ Vdc}, I_E = 0$ )	$I_{CBO}$	—	100	$\mu\text{Adc}$
Emitter–Base Cutoff Current ( $V_{EB} = 4.0 \text{ Vdc}, I_C = 0$ )	$I_{EBO}$	—	100	$\mu\text{Adc}$

### ON CHARACTERISTICS

DC Current Gain (1) ( $I_C = 1.0 \text{ Adc}, V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$	40	—	—
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(1) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

# MJE521

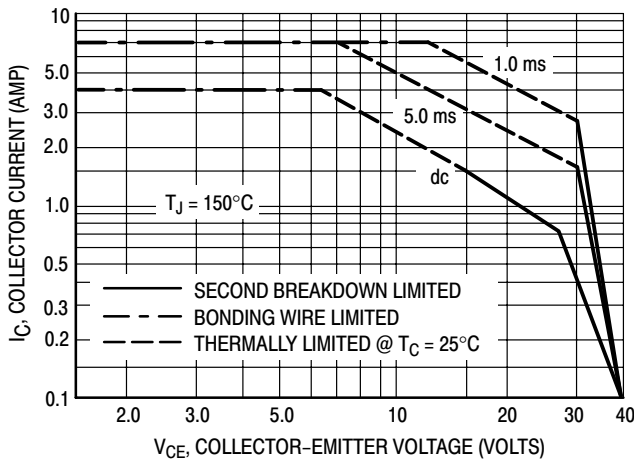


Figure 1. Active-Region Safe Operating Area

The data of Figure 1 based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $(T_{Jpk}) \leq 150^{\circ}\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

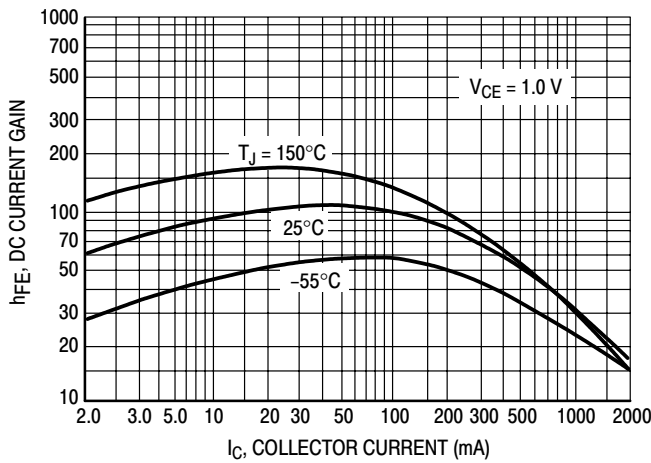


Figure 2. DC Current Gain

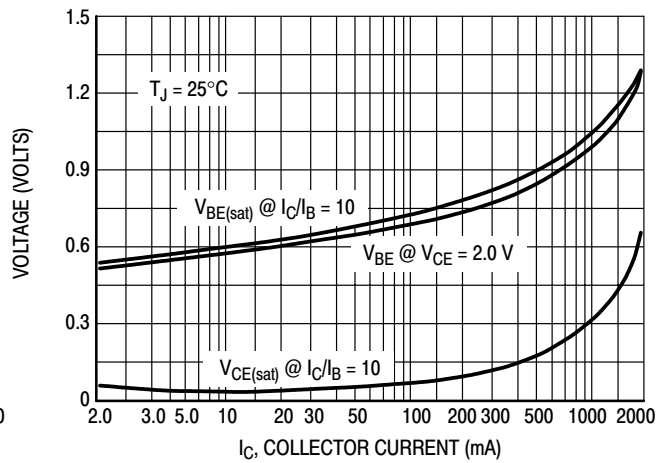


Figure 3. "On" Voltage

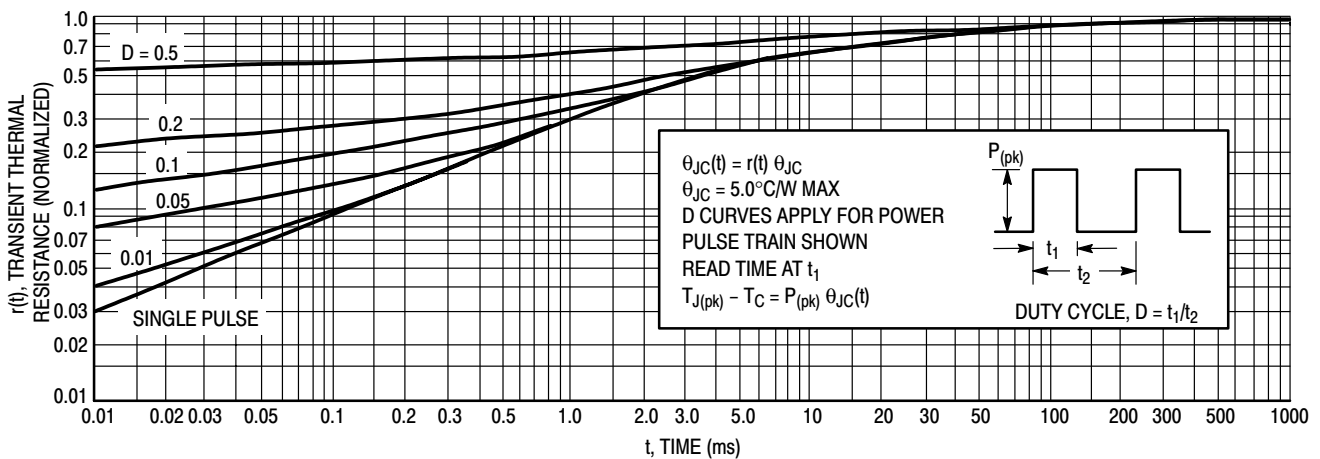


Figure 4. Thermal Response

# High Voltage PNP Silicon Power Transistors

... designed for line operated audio output amplifier, SWITCHMODE™ power supply drivers and other switching applications.

- 300 V to 400 V (Min) —  $V_{CEO(sus)}$
- 1.0 A Rated Collector Current
- Popular TO-220 Plastic Package
- PNP Complements to the TIP47 thru TIP50 Series

## MAXIMUM RATINGS

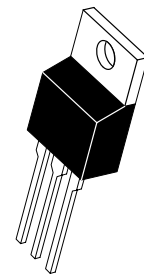
Rating	Symbol	MJE573 0	MJE573 1	MJE573 1A	Unit
Collector-Emitter Voltage	$V_{CEO}$	300	350	375	Vdc
Collector-Base Voltage	$V_{CB}$	300	350	375	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous Peak	$I_C$	1.0 3.0			Adc
Base Current	$I_B$	1.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.32			Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016			Watts W/ $^\circ\text{C}$
Unclamped Inducting Load Energy (See Figure 10)	E	20			mJ
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150			$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

**MJE5730**  
**MJE5731**  
**MJE5731A**

**1.0 AMPERE**  
**POWER TRANSISTORS**  
**PNP SILICON**  
**300-350-400 VOLTS**  
**40 WATTS**



**CASE 221A-09**  
**TO-220AB**

# MJE5730 MJE5731 MJE5731A

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	300 350 375	—	Vdc
Collector Cutoff Current ( $V_{CE} = 200\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 250\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 300\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— — —	1.0 1.0 1.0	mAdc
Collector Cutoff Current ( $V_{CE} = 300\text{ Vdc}$ , $V_{BE} = 0$ ) ( $V_{CE} = 350\text{ Vdc}$ , $V_{BE} = 0$ ) ( $V_{CE} = 400\text{ Vdc}$ , $V_{BE} = 0$ )	$I_{CES}$	— — —	1.0 1.0 1.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 0.3\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ )	$h_{FE}$	30 10	150 —	—
Collector–Emitter Saturation Voltage ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	$V_{CE(sat)}$	—	1.0	Vdc
Base–Emitter On Voltage ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ )	$V_{BE(on)}$	—	1.5	Vdc

## DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ( $I_C = 0.2\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 2.0\text{ MHz}$ )	$f_T$	10	—	MHz
Small–Signal Current Gain ( $I_C = 0.2\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	25	—	—

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

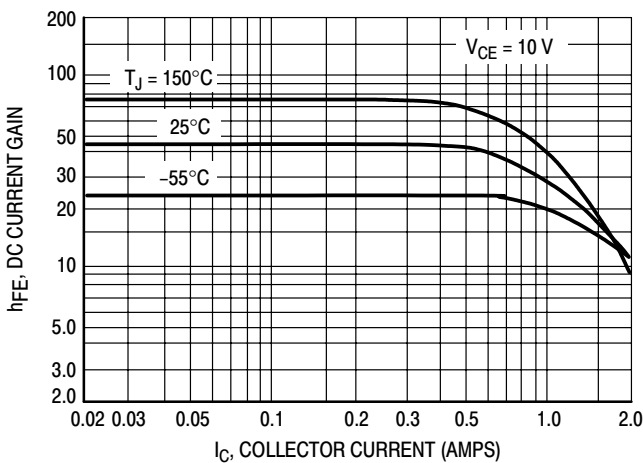


Figure 1. DC Current Gain

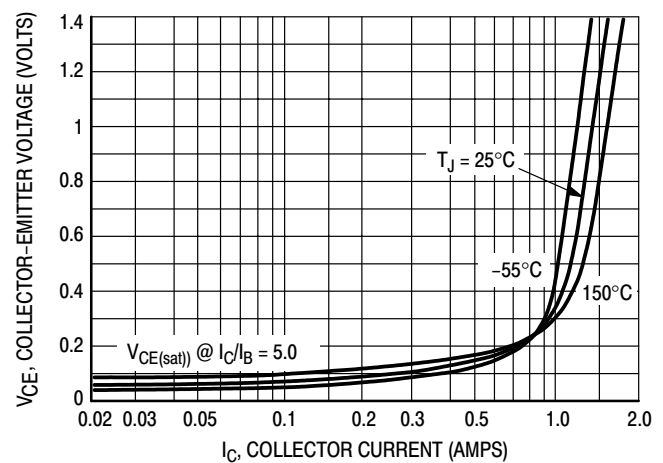


Figure 2. Collector–Emitter Saturation Voltage

# MJE5730 MJE5731 MJE5731A

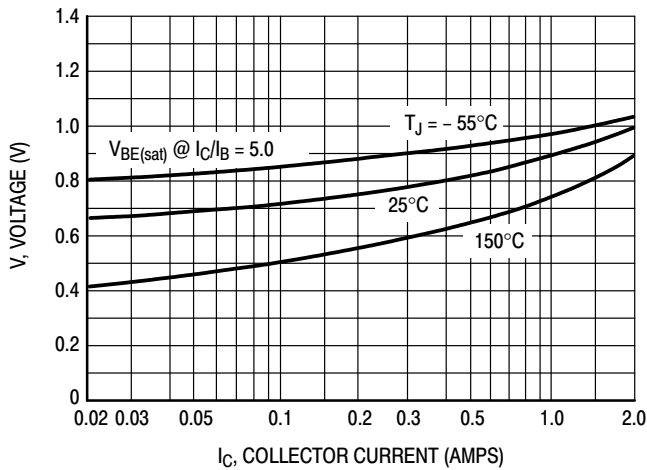


Figure 3. Base-Emitter Voltage

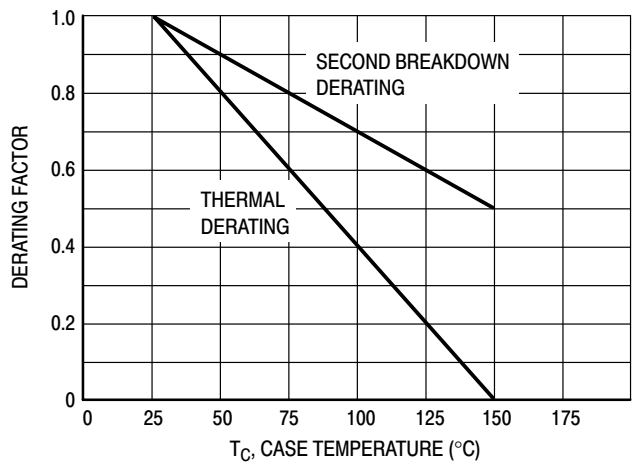


Figure 4. Normalized Power Derating

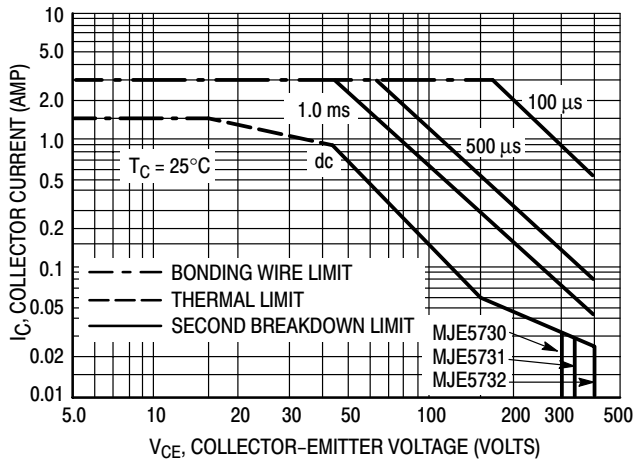


Figure 5. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

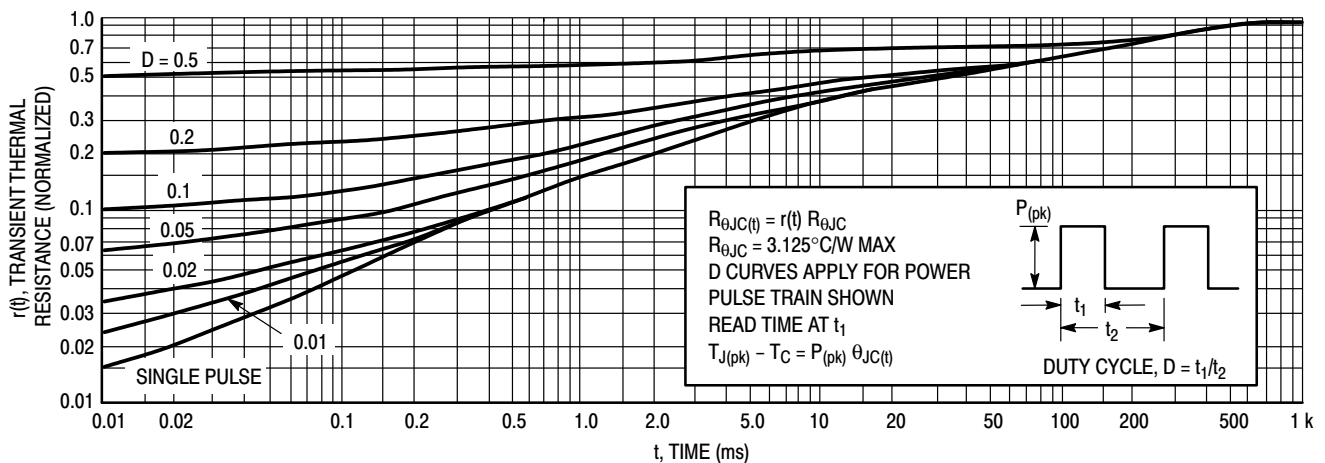


Figure 6. Thermal Response



# MJE5730 MJE5731 MJE5731A

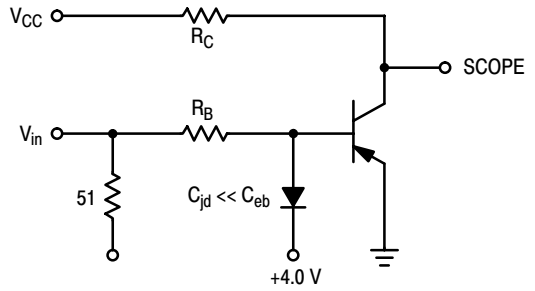
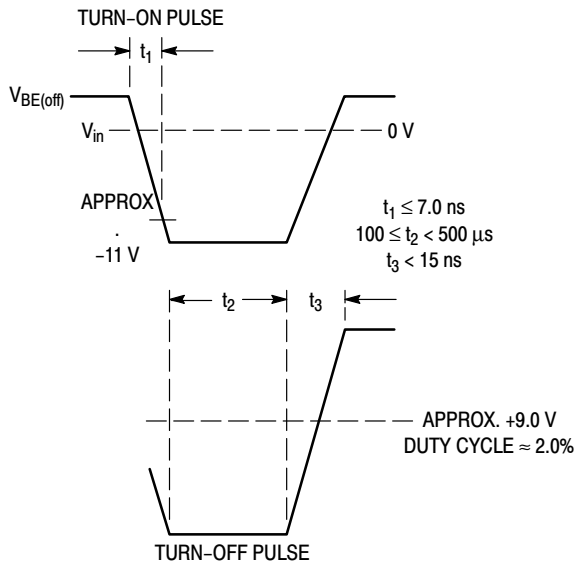


Figure 7. Switching Time Equivalent Circuit

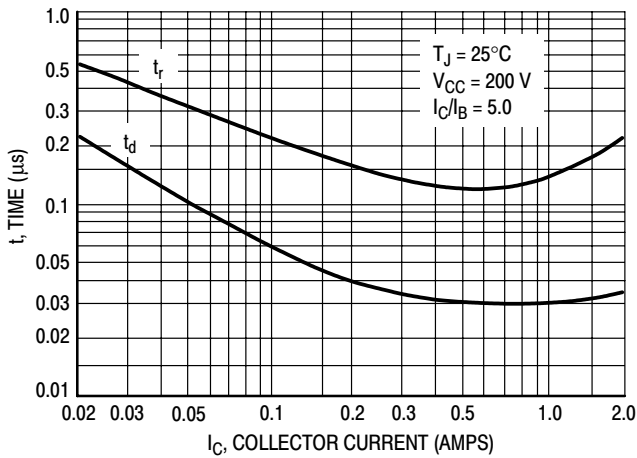


Figure 8. Turn-On Resistive Switching Times

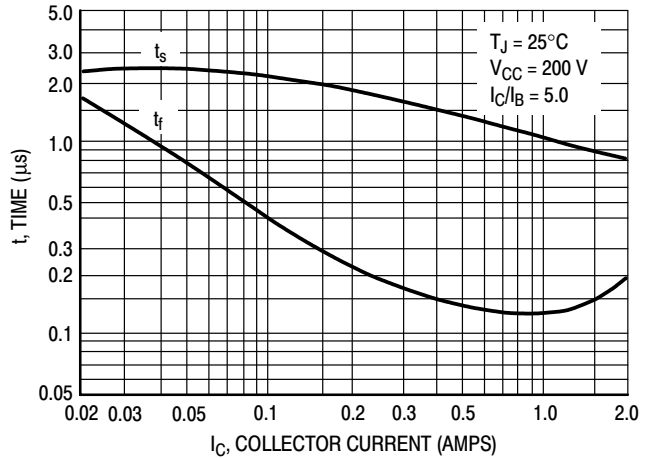


Figure 9. Resistive Turn-Off Switching Times

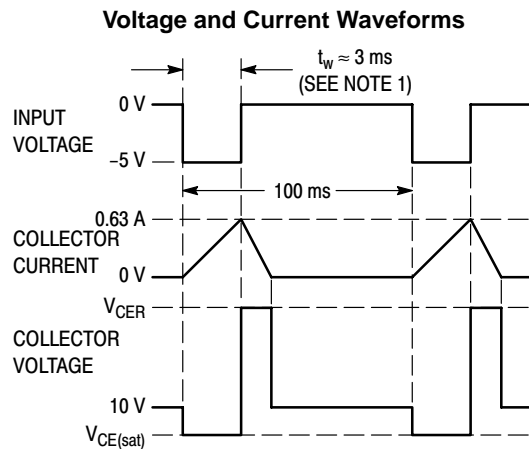
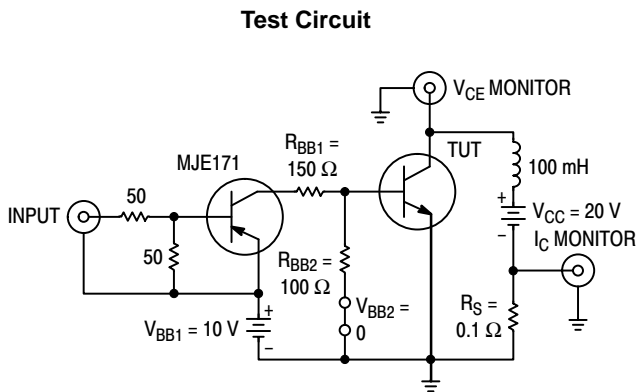


Figure 10. Inductive Load Switching

# NPN Silicon Power Darlington Transistors

The MJE5740 and MJE5742 Darlington transistors are designed for high-voltage power switching in inductive circuits. They are particularly suited for operation in applications such as:

- Small Engine Ignition
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

## MAXIMUM RATINGS

Rating	Symbol	MJE5740	MJE5742	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector–Emitter Voltage	$V_{CEV}$	600	800	Vdc
Emitter Base Voltage	$V_{EB}$	8		Vdc
Collector Current – Continuous	$I_C$	8		Adc
– Peak (1)	$I_{CM}$	16		
Base Current – Continuous	$I_B$	2.5		Adc
– Peak (1)	$I_{BM}$	5		
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2		Watts
		16		mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	80		Watts
		640		mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle = 10%.

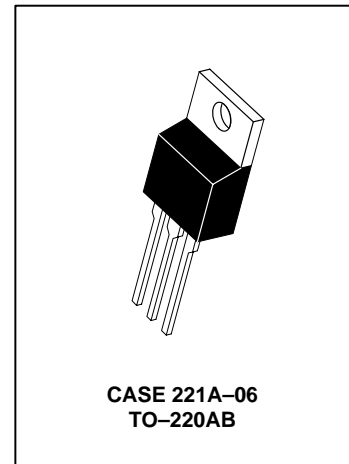
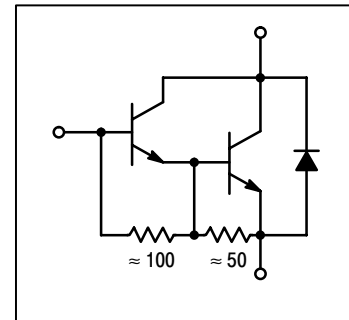
## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	$^\circ\text{C}$

# MJE5740 MJE5742\*

\*ON Semiconductor Preferred Device

**POWER DARLINGTON  
TRANSISTORS  
8 AMPERES  
300, 400 VOLTS  
80 WATTS**



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJE5740 MJE5742

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
<b>OFF CHARACTERISTICS (2)</b>						
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 50 mA, I <sub>B</sub> = 0)	MJE5740 MJE5742	V <sub>CEO(sus)</sub>	300 400	– –	– –	Vdc
Collector Cutoff Current (V <sub>CEV</sub> = Rated Value, V <sub>BE(off)</sub> = 1.5 Vdc) (V <sub>CEV</sub> = Rated Value, V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 100°C)	I <sub>CEV</sub>	– –	– –	1 5		mAdc
Emitter Cutoff Current (V <sub>EB</sub> = 8 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	75		mAdc

## SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I <sub>S/b</sub>	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 7			

Characteristic	Symbol	Min	Typ	Max	Unit	
<b>ON CHARACTERISTICS (3)</b>						
DC Current Gain (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 5 Vdc) (I <sub>C</sub> = 4 Adc, V <sub>CE</sub> = 5 Vdc)	h <sub>FE</sub>	50 200	100 400	– –	–	
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 4 Adc, I <sub>B</sub> = 0.2 Adc) (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 0.4 Adc) (I <sub>C</sub> = 4 Adc, I <sub>B</sub> = 0.2 Adc, T <sub>C</sub> = 100°C)	V <sub>CE(sat)</sub>	– – –	– – –	2 3 2.2		Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 4 Adc, I <sub>B</sub> = 0.2 Adc) (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 0.4 Adc) (I <sub>C</sub> = 4 Adc, I <sub>B</sub> = 0.2 Adc, T <sub>C</sub> = 100°C)	V <sub>BE(sat)</sub>	– – –	– – –	2.5 3.5 2.4		Vdc
Diode Forward Voltage (4) (I <sub>F</sub> = 5 Adc)	V <sub>f</sub>	–	–	2.5		Vdc

## SWITCHING CHARACTERISTICS

Typical Resistive Load (Table 1)						
Delay Time	(V <sub>CC</sub> = 250 Vdc, I <sub>C(pk)</sub> = 6 A I <sub>B1</sub> = I <sub>B2</sub> = 0.25 A, t <sub>p</sub> = 25 μs, Duty Cycle ≤ 1%)	t <sub>d</sub>	–	0.04	–	μs
Rise Time		t <sub>r</sub>	–	0.5	–	μs
Storage Time		t <sub>s</sub>	–	8	–	μs
Fall Time		t <sub>f</sub>	–	2	–	μs
Inductive Load, Clamped (Table 1)						
Voltage Storage Time	(I <sub>C(pk)</sub> = 6 A, V <sub>CE(pk)</sub> = 250 Vdc I <sub>B1</sub> = 0.06 A, V <sub>BE(off)</sub> = 5 Vdc)	t <sub>sv</sub>	–	4	–	μs
Crossover Time		t <sub>c</sub>	–	2	–	μs

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

(3) Pulse Test: Pulse Width 300 μs, Duty Cycle = 2%.

(4) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V<sub>f</sub>) of this diode is comparable to that of typical fast recovery rectifiers.

(continued)

TYPICAL CHARACTERISTICS

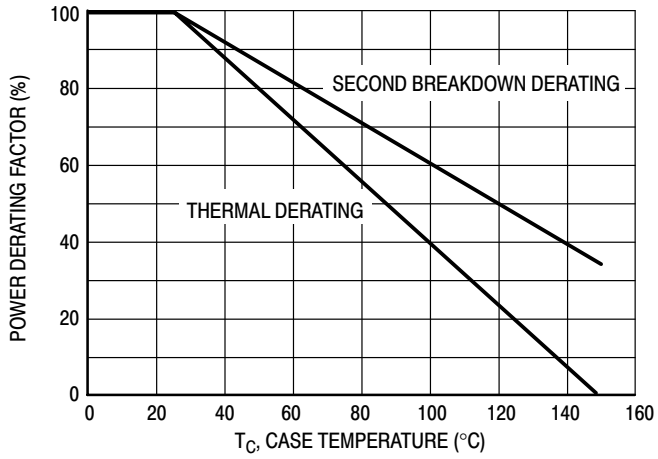


Figure 11. Power Derating

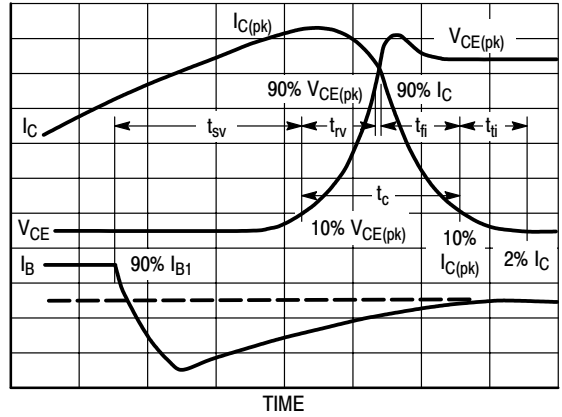


Figure 12. Inductive Switching Measurements

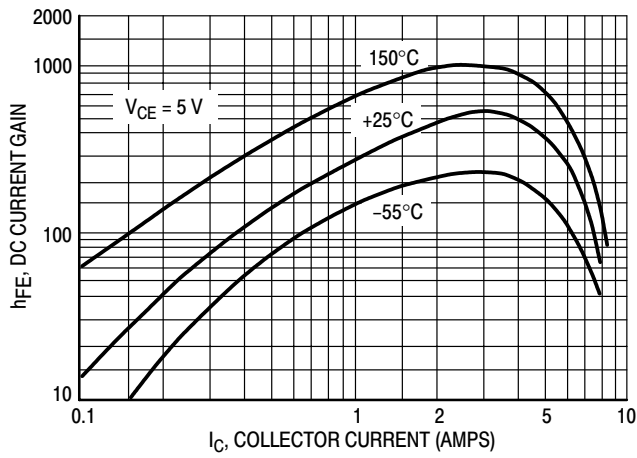


Figure 13. DC Current Gain

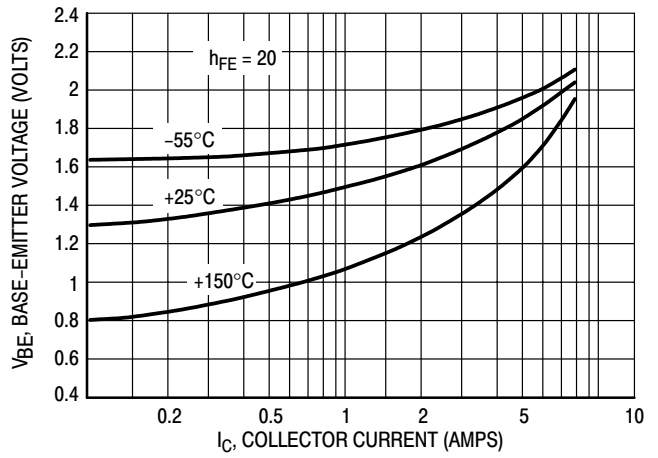


Figure 14. Base-Emitter Voltage

# MJE5740 MJE5742

Table 1. Test Conditions for Dynamic Performance

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
TEST CIRCUITS	<p>DUTY CYCLE <math>\leq 10\%</math>  <math>t_r, t_f \leq 10 \text{ ns}</math></p> <p>NOTE:  PW and <math>V_{CC}</math> Adjusted for Desired <math>I_C</math>  <math>R_B</math> Adjusted for Desired <math>I_{B1}</math></p>	
CIRCUIT VALUES	<p>COIL DATA:  FERROXCUBE CORE #6656  FULL BOBBIN (~16 TURNS) #16</p> <p>GAP FOR 200 <math>\mu\text{H}/20 \text{ A}</math>  <math>L_{\text{coil}} = 200 \mu\text{H}</math></p> <p><math>V_{CC} = 30 \text{ V}</math>  <math>V_{CE(\text{pk})} = 250 \text{ Vdc}</math>  <math>I_{C(\text{pk})} = 6 \text{ A}</math></p>	<p><math>V_{CC} = 250 \text{ V}</math>  <math>D1 = 1\text{N}5820 \text{ OR EQUIV.}</math></p>
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p><math>t_1</math> ADJUSTED TO OBTAIN <math>I_C</math></p> $t_1 \approx \frac{L_{\text{coil}} (I_{C(\text{pk})})}{V_{CC}}$ <p>TEST EQUIPMENT  SCOPE-TEKTRONICS  475 OR EQUIVALENT</p> $t_2 \approx \frac{L_{\text{coil}} (I_{C(\text{pk})})}{V_{\text{clamp}}}$	<p><math>t_r, t_f &lt; 10 \text{ ns}</math>  DUTY CYCLE = 1%  <math>R_B</math> AND <math>R_C</math> ADJUSTED FOR DESIRED <math>I_B</math> AND <math>I_C</math></p>

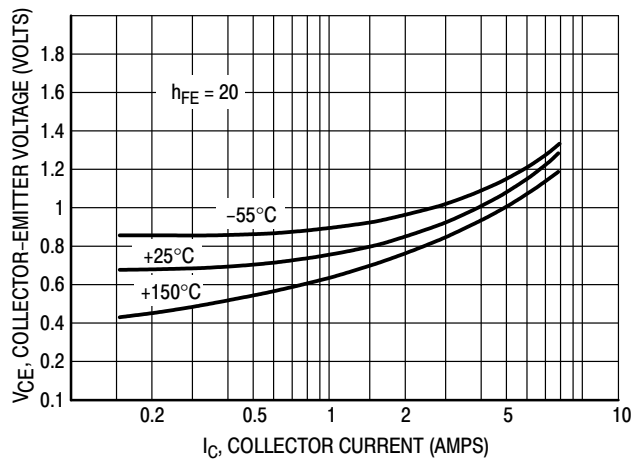


Figure 15. Inductive Switching Measurements

# MJE5740 MJE5742

## SAFE OPERATING AREA INFORMATION

### FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 16 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 11.

The Safe Operating Area figures shown in Figures 6 and 7 are specified ratings for these devices under the test conditions shown.

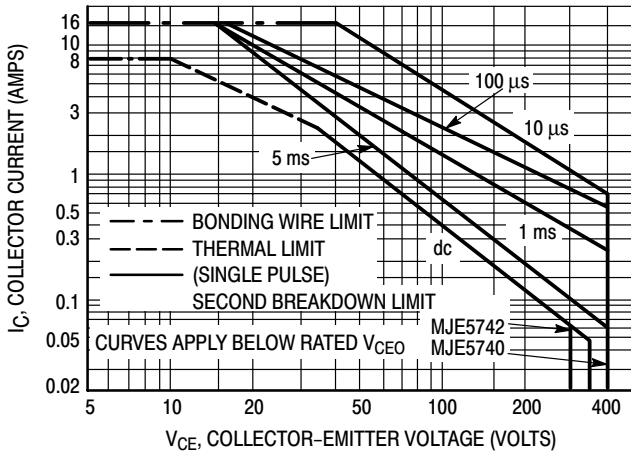


Figure 16. Forward Bias Safe Operating Area

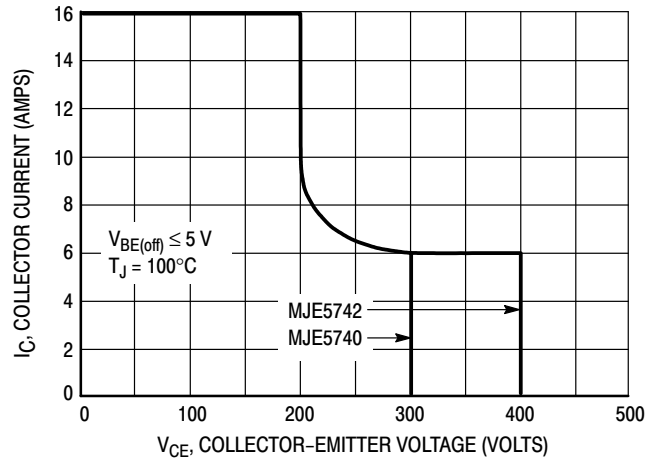


Figure 17. Reverse Bias Safe Operating Area

## RESISTIVE SWITCHING PERFORMANCE

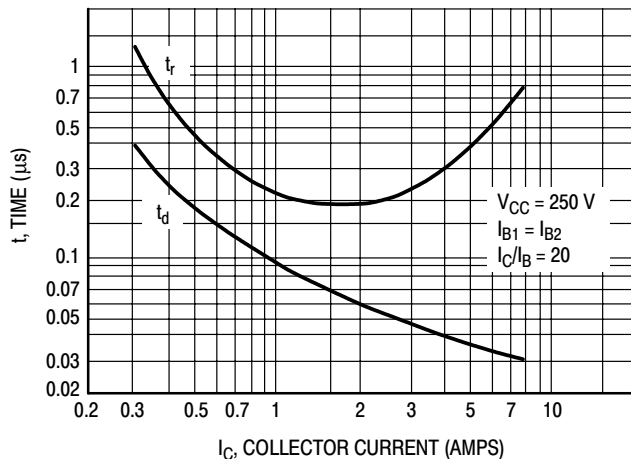


Figure 18. Turn-On Time

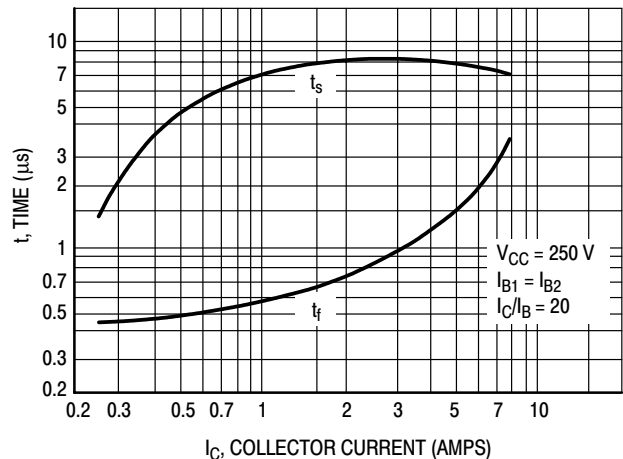


Figure 19. Turn-Off Time

# SWITCHMODE™ Series PNP Silicon Power Transistors

The MJE5850, MJE5851 and the MJE5852 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated SWITCHMODE applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

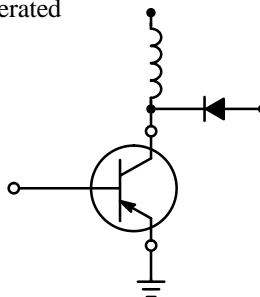
**Fast Turn-Off Times**

100 ns Inductive Fall Time @ 25°C (Typ)  
125 ns Inductive Crossover Time @ 25°C (Typ)

Operating Temperature Range -65 to +150°C

100°C Performance Specified for:

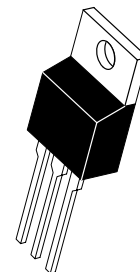
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



**MJE5850**  
**MJE5851\***  
**MJE5852\***

\*ON Semiconductor Preferred Device

**8 AMPERE  
PNP SILICON  
POWER TRANSISTORS  
300, 350, 400 VOLTS  
80 WATTS**



**CASE 221A-09  
TO-220AB**

**MAXIMUM RATINGS**

Rating	Symbol	MJE5850	MJE5851	MJE5852	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector-Emitter Voltage	$V_{CEV}$	350	400	450	Vdc
Emitter Base Voltage	$V_{EB}$	6.0			Vdc
Collector Current — Continuous	$I_C$	8.0			Adc
Peak (1)	$I_{CM}$	16			
Base Current — Continuous	$I_B$	4.0			Adc
Peak (1)	$I_{BM}$	8.0			
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	80			Watts
		0.640			W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to 150			°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJE5850 MJE5851 MJE5852

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0)	MJE5850 MJE5851 MJE5852	V <sub>CEO(sus)</sub>	300 350 400	— — —	— — —	Vdc
Collector Cutoff Current (V <sub>CEV</sub> = Rated Value, V <sub>BE(off)</sub> = 1.5 Vdc) (V <sub>CEV</sub> = Rated Value, V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 100°C)		I <sub>CEV</sub>	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEV</sub> , R <sub>BE</sub> = 50 Ω, T <sub>C</sub> = 100°C)		I <sub>CER</sub>	—	—	3.0	mAdc
Emitter Cutoff Current (V <sub>EB</sub> = 6.0 Vdc, I <sub>C</sub> = 0)		I <sub>EBO</sub>	—	—	1.0	mAdc

### SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	I <sub>S/b</sub>	See Figure 12			
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 13			

### \*ON CHARACTERISTICS

DC Current Gain (I <sub>C</sub> = 2.0 Adc, V <sub>CE</sub> = 5 Vdc) (I <sub>C</sub> = 5.0 Adc, V <sub>CE</sub> = 5 Vdc)	h <sub>FE</sub>	15 5	— —	— —	— —
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 4.0 Adc, I <sub>B</sub> = 1.0 Adc) (I <sub>C</sub> = 8.0 Adc, I <sub>B</sub> = 3.0 Adc) (I <sub>C</sub> = 4.0 Adc, I <sub>B</sub> = 1.0 Adc, T <sub>C</sub> = 100°C)	V <sub>CE(sat)</sub>	— — —	— — —	2.0 5.0 2.5	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 4.0 Adc, I <sub>B</sub> = 1.0 Adc) (I <sub>C</sub> = 4.0 Adc, I <sub>B</sub> = 1.0 Adc, T <sub>C</sub> = 100°C)	V <sub>BE(sat)</sub>	— —	— —	1.5 1.5	Vdc

### DYNAMIC CHARACTERISTICS

Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f <sub>test</sub> = 1.0 kHz)	C <sub>ob</sub>	—	270	—	pF
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### SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V <sub>CC</sub> = 250 Vdc, I <sub>C</sub> = 4.0 A, I <sub>B1</sub> = 1.0 A, t <sub>p</sub> = 50 μs, Duty Cycle ≤ 2%)	t <sub>d</sub>	—	0.025	0.1	μs
Rise Time		t <sub>r</sub>	—	0.100	0.5	μs
Storage Time	(V <sub>CC</sub> = 250 Vdc, I <sub>C</sub> = 4.0 A, I <sub>B1</sub> = 1.0 A, V <sub>BE(off)</sub> = 5 Vdc, t <sub>p</sub> = 50 μs, Duty Cycle ≤ 2%)	t <sub>s</sub>	—	0.60	2.0	μs
Fall Time		t <sub>f</sub>	—	0.11	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I <sub>CM</sub> = 4 A, V <sub>CEM</sub> = 250 V, I <sub>B1</sub> = 1.0 A, V <sub>BE(off)</sub> = 5 Vdc, T <sub>C</sub> = 100°C)	t <sub>sv</sub>	—	0.8	3.0	μs
Crossover Time		t <sub>c</sub>	—	0.4	1.5	μs
Fall Time		t <sub>fi</sub>	—	0.1	—	μs
Storage Time	(I <sub>CM</sub> = 4 A, V <sub>CEM</sub> = 250 V, I <sub>B1</sub> = 1.0 A, V <sub>BE(off)</sub> = 5 Vdc, T <sub>C</sub> = 25°C)	t <sub>sv</sub>	—	0.5	—	μs
Crossover Time		t <sub>c</sub>	—	0.125	—	μs
Fall Time		t <sub>fi</sub>	—	0.1	—	μs

\*Pulse Test: PW = 300 μs. Duty Cycle ≤ 2%



TYPICAL ELECTRICAL CHARACTERISTICS

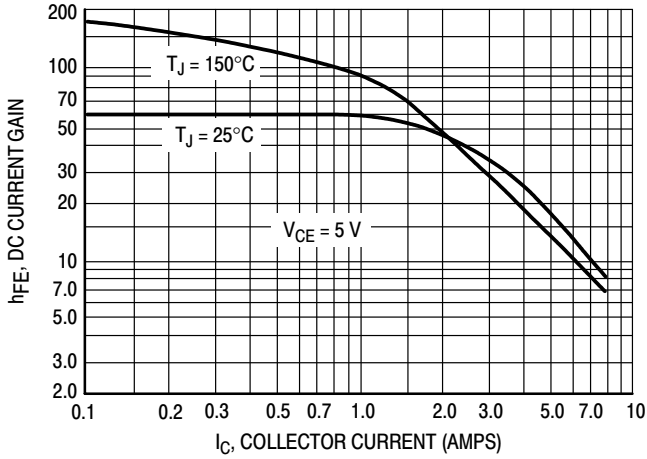


Figure 1. DC Current Gain

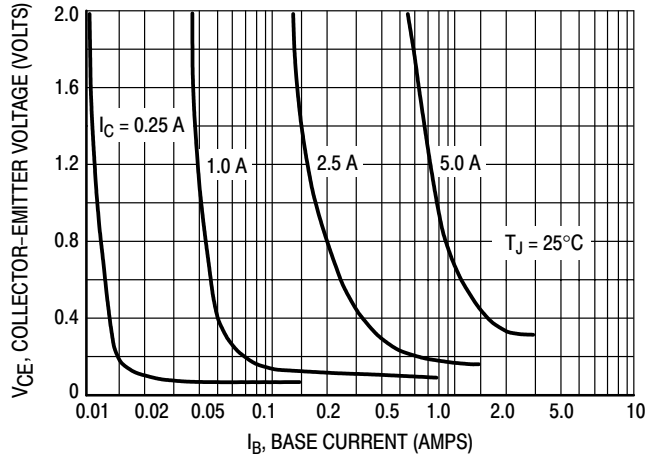


Figure 2. Collector Saturation Region

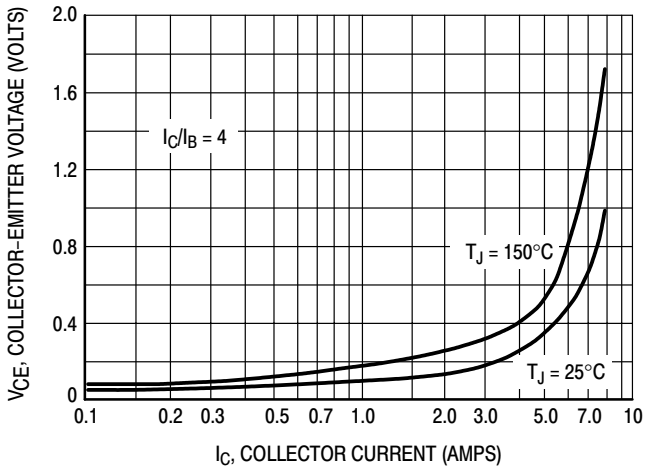


Figure 3. Collector-Emitter Saturation Voltage

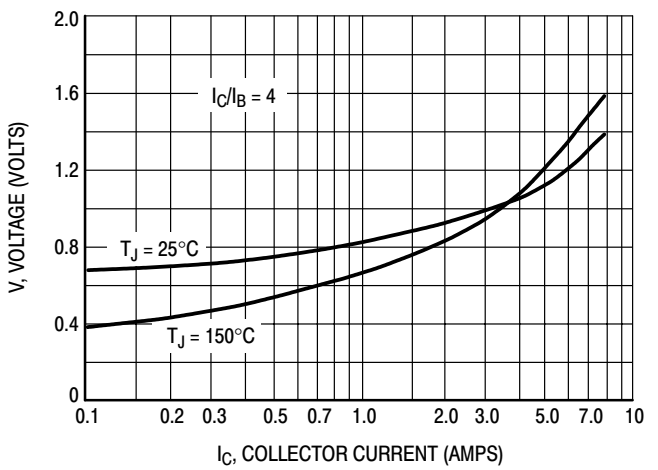


Figure 4. Base-Emitter Voltage

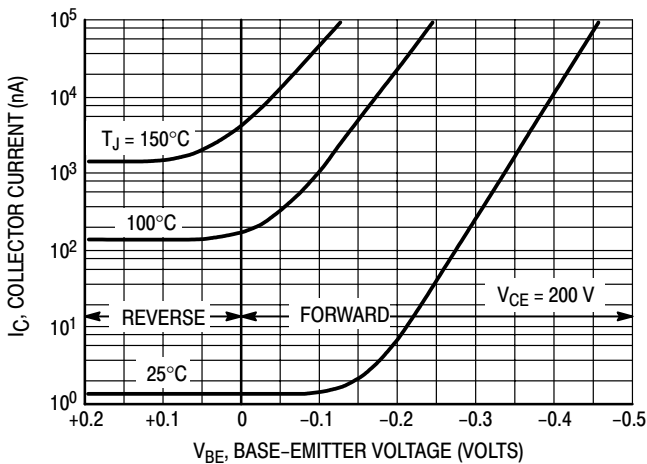


Figure 5. Collector Cutoff Region

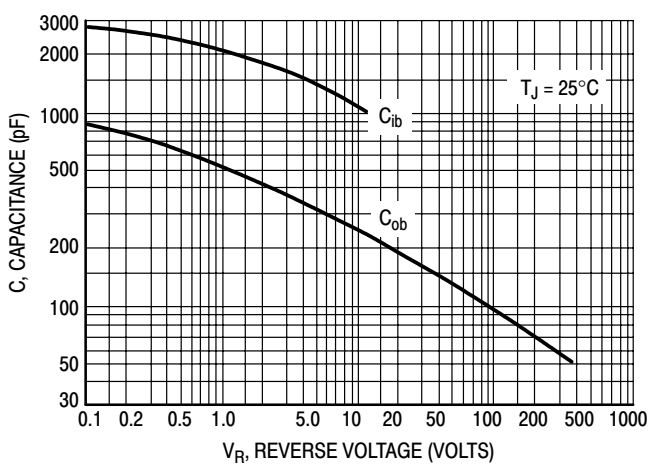


Figure 6. Capacitance

# MJE5850 MJE5851 MJE5852

Table 1. Test Conditions for Dynamic Performance

	$V_{CE(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain <math>I_C = 100 \text{ mA}</math></p>	<p><math>-V</math> adjusted to obtain desired <math>I_{B1}</math>  <math>+V</math> adjusted to obtain desired <math>V_{BE(off)}</math></p>	<p><b>TURN-ON TIME</b></p> <p><math>I_{B1}</math> adjusted to obtain the forced <math>h_{FE}</math> desired</p> <p><b>TURN-OFF TIME</b></p> <p>Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 80 \text{ mH}$ , $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 250 \text{ V}$ $R_B$ adjusted to attain desired $I_{B1}$	$V_{CC} = 250 \text{ V}$ $R_L = 62 \Omega$ Pulse Width = $10 \mu\text{s}$
TEST CIRCUITS	<p><b>INDUCTIVE TEST CIRCUIT</b></p> <p>SEE ABOVE FOR DETAILED CONDITIONS</p>	<p><b>OUTPUT WAVEFORMS</b></p> <p><math>t_1</math> Adjusted to Obtain <math>I_C</math></p> $t_1 \approx \frac{L_{coil} (I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{CM})}{V_{Clamp}}$ <p>Test Equipment  Scope — Tektronix 475 or Equivalent</p>	<p><b>RESISTIVE TEST CIRCUIT</b></p>

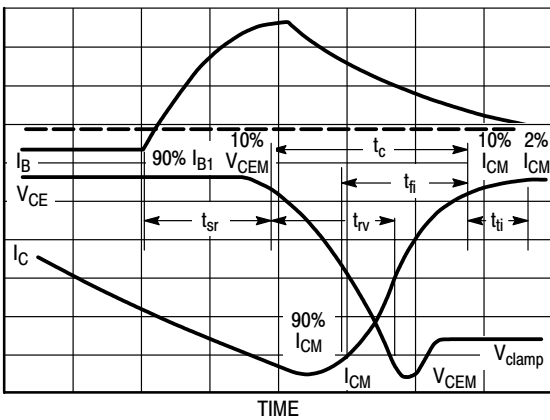


Figure 7. Inductive Switching Measurements

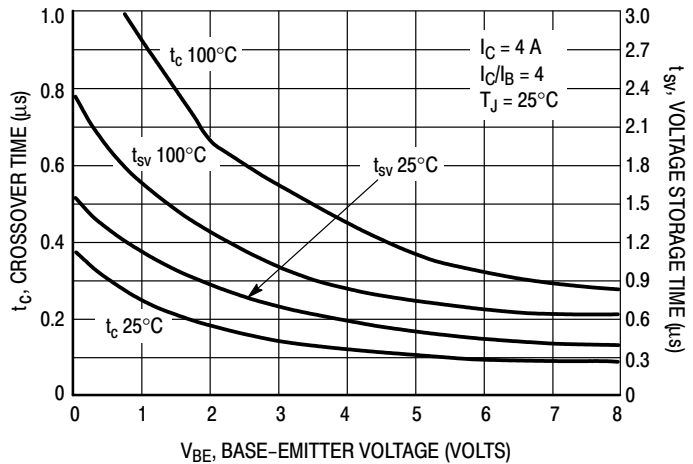


Figure 8. Inductive Switching Times

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- $t_{SV}$  = Voltage Storage Time, 90%  $I_{B1}$  to 10%  $V_{CEM}$
- $t_{RV}$  = Voltage Rise Time, 10–90%  $V_{CEM}$
- $t_{fi}$  = Current Fall Time, 90–10%  $I_{CM}$
- $t_{ti}$  = Current Tail, 10–2%  $I_{CM}$
- $t_c$  = Crossover Time, 10%  $V_{CEM}$  to 10%  $I_{CM}$

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general,  $t_{RV} + t_{fi} \approx t_c$ . However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds ( $t_c$  and  $t_{SV}$ ) which are guaranteed at 100°C.

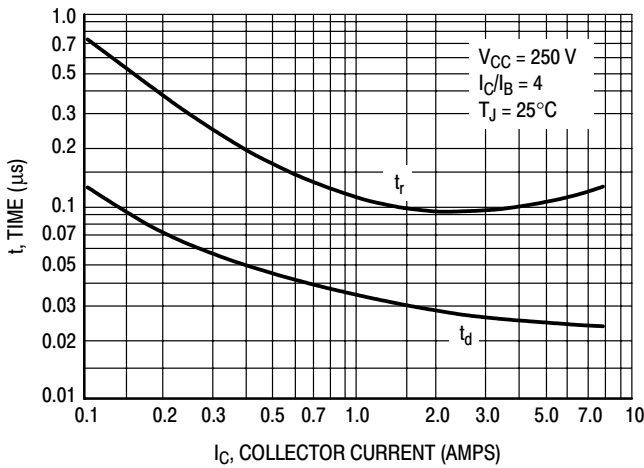


Figure 9. Turn-On Switching Times

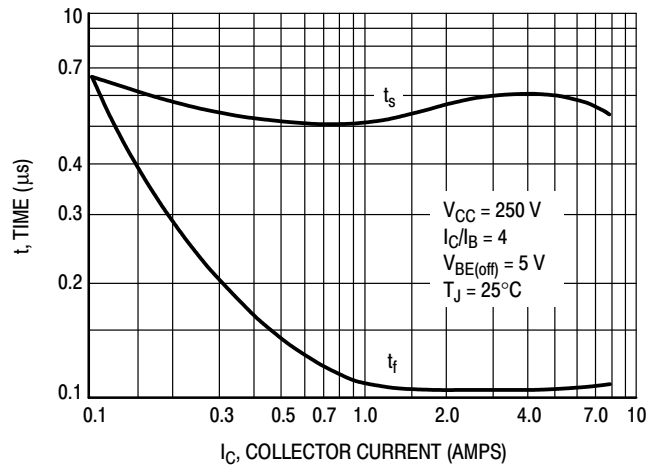


Figure 10. Turn-Off Switching Time

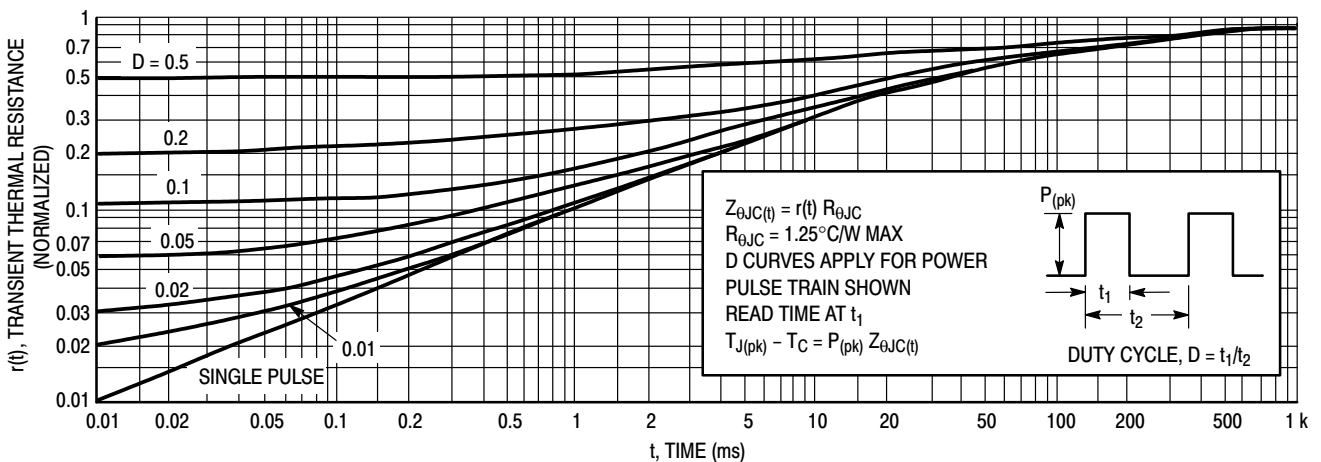


Figure 11. Typical Thermal Response [ $Z_{\theta JC}(t)$ ]

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

**SAFE OPERATING AREA INFORMATION**

**FORWARD BIAS**

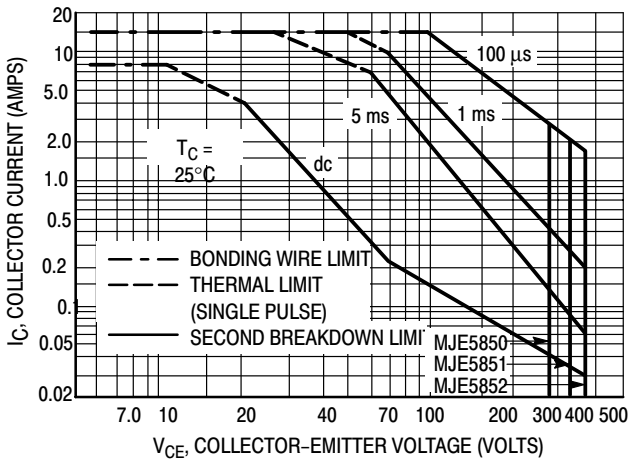
There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

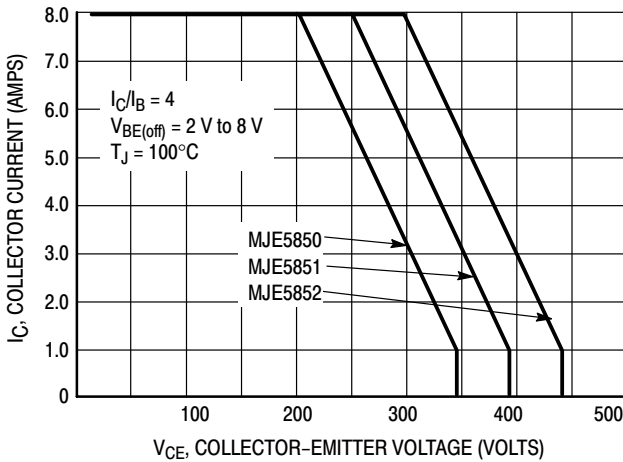
$T_{J(pk)}$  may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

**REVERSE BIAS**

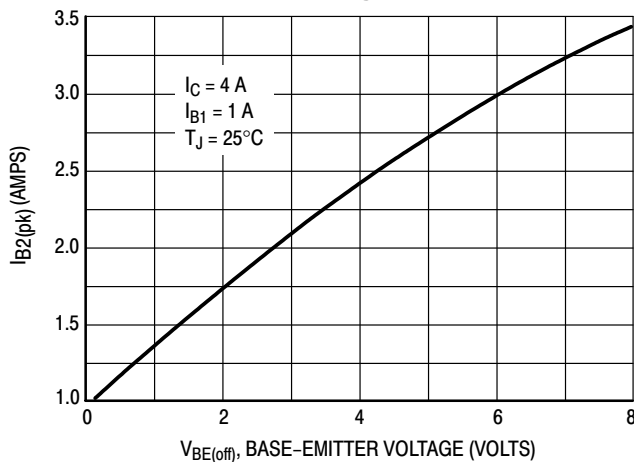
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.



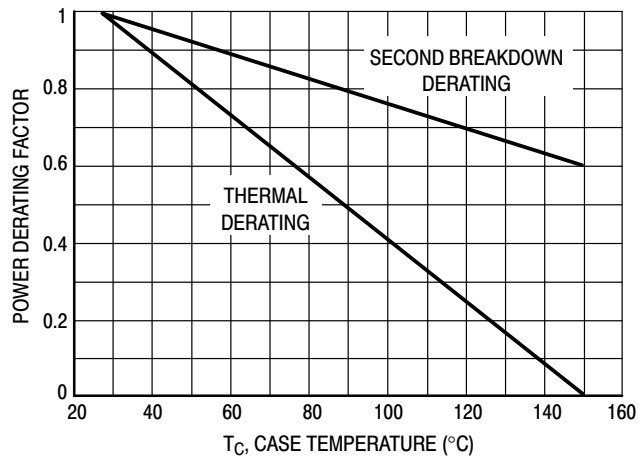
**Figure 12. Maximum Forward Bias Safe Operating Area**



**Figure 13. RBSOA, Maximum Reverse Bias Safe Operating Area**



**Figure 14. Peak Reverse Base Current**



**Figure 15. Forward Bias Power Derating**

# Plastic Darlington Complementary Silicon Power Transistors

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —  
 $h_{FE} = 2000$  (Typ) @  $I_C$   
 $= 2.0$  Adc
- Monolithic Construction with Built-in Base-Emitter Resistors to Limit Leakage Multiplication
- Choice of Packages —  
 MJE700 and MJE800 series

## MAXIMUM RATINGS

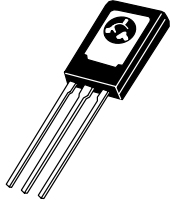
Rating	Symbol	MJE700 MJE800	MJE702 MJE703 MJE802 MJE803	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	80	Vdc
Collector-Base Voltage	$V_{CB}$	60	80	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current	$I_C$	4.0		Adc
Base Current	$I_B$	0.1		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	<b>CASE 77</b>		Watts W/ $^\circ\text{C}$
		40 0.32		
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case CASE 77 TO-220	$R_{\theta JC}$	3.13 2.50	$^\circ\text{C}/\text{W}$

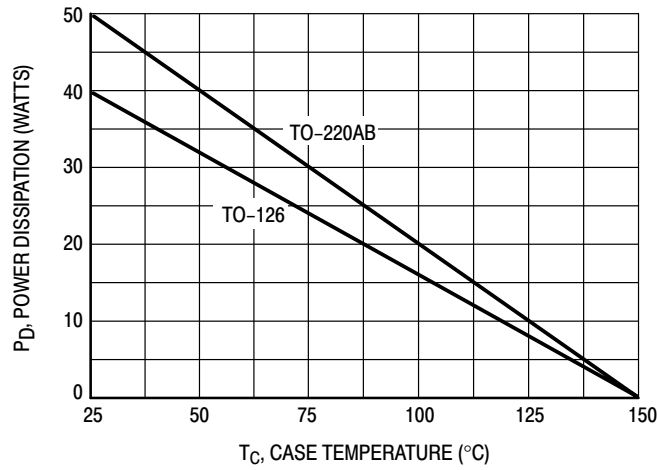
**PNP**  
**MJE700**  
**MJE702**  
**MJE703**  
**NPN**  
**MJE800**  
**MJE802**  
**MJE803**

**4.0 AMPERE**  
**DARLINGTON**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**40 WATT**  
**50 WATT**



**CASE 77-08**  
**TO-225AA TYPE**  
**MJE700-703**  
**MJE800-803**

**MJE700 MJE702 MJE703 MJE800 MJE802 MJE803**



**Figure 1. Power Derating**

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Breakdown Voltage (1) ( $I_C = 50\text{ mAdc}$ , $I_B = 0$ )	MJE700, MJE800 MJE702, MJE703, MJE802, MJE803	$V_{(BR)CEO}$	60 80	— — Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 80\text{ Vdc}$ , $I_B = 0$ )	MJE700, MJE800 MJE702, MJE703, MJE802, MJE803	$I_{CEO}$	— —	100 100 $\mu\text{Adc}$
Collector Cutoff Current ( $V_{CB} = \text{Rated } BV_{CEO}$ , $I_E = 0$ ) ( $V_{CB} = \text{Rated } BV_{CEO}$ , $I_E = 0$ , $T_C = 100^\circ\text{C}$ )		$I_{CBO}$	— —	100 500 $\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	2.0 mAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain (1) ( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	MJE700, MJE702, MJE800, MJE802 MJE703, MJE803 All devices	$h_{FE}$	750 750 100	— — —
Collector–Emitter Saturation Voltage (1) ( $I_C = 1.5\text{ Adc}$ , $I_B = 30\text{ mAdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $I_B = 40\text{ mAdc}$ ) ( $I_C = 4.0\text{ Adc}$ , $I_B = 40\text{ mAdc}$ )	MJE700, MJE702, MJE800, MJE802 MJE703, MJE803 All devices	$V_{CE(sat)}$	— — —	2.5 2.8 3.0 Vdc
Base–Emitter On Voltage (1) ( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	MJE700, MJE702, MJE800, MJE802 MJE703, MJE803 All devices	$V_{BE(on)}$	— — —	2.5 2.5 3.0 Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Small–Signal Current Gain ( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )		$h_{fe}$	1.0	— —

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

# MJE700 MJE702 MJE703 MJE800 MJE802 MJE803

$R_B$  &  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS  
 $D_1$ , MUST BE FAST RECOVERY TYPE, e.g.:  
 1N5825 USED ABOVE  $I_B \approx 100$  mA  
 MSD6100 USED BELOW  $I_B \approx 100$  mA

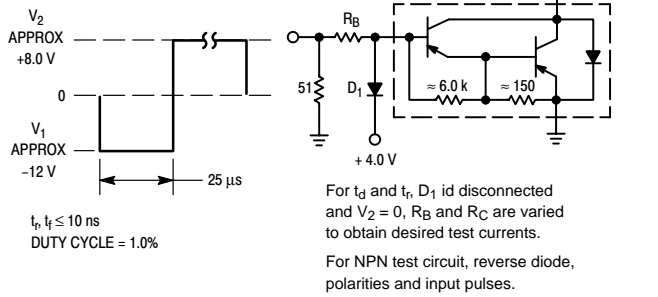


Figure 2. Switching Times Test Circuit

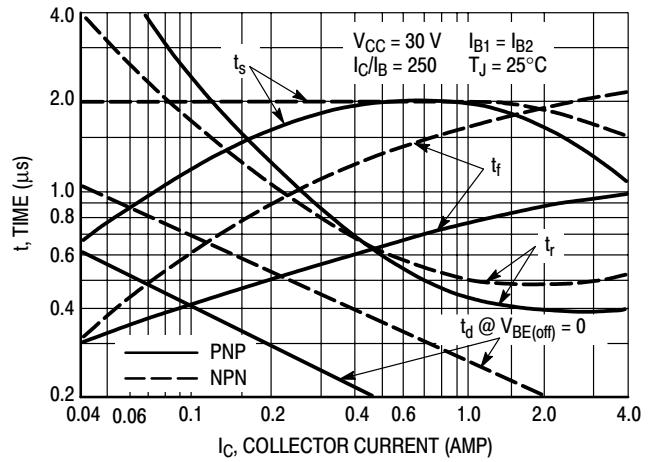


Figure 3. Switching Times

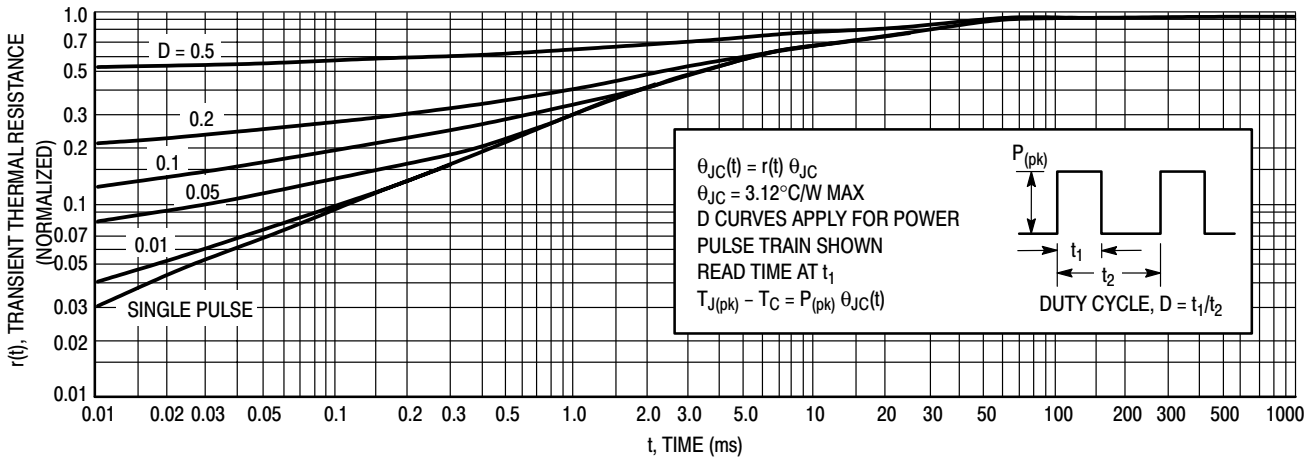


Figure 4. Thermal Response (MJE700, 800 Series)

ACTIVE-REGION SAFE-OPERATING AREA

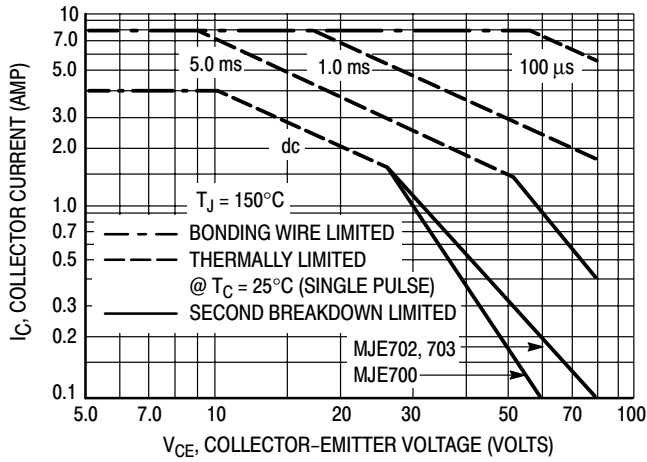


Figure 5. MJE700 Series

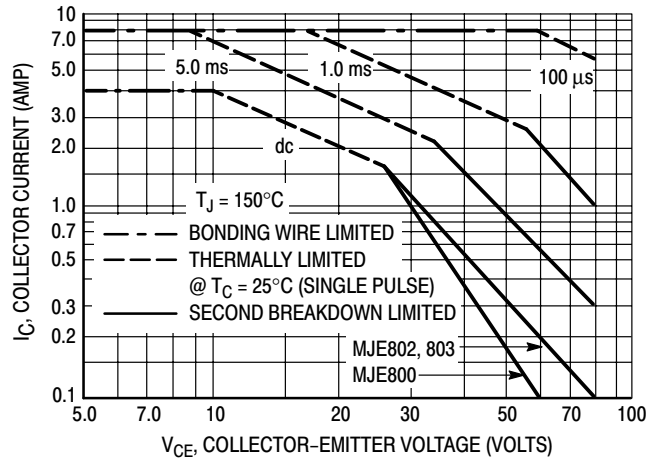


Figure 6. MJE800 Series

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 are based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown

pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



MJE700 MJE702 MJE703 MJE800 MJE802 MJE803

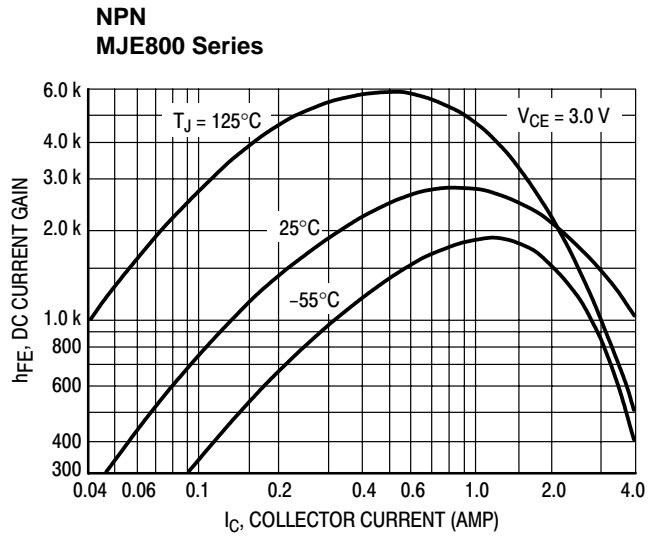
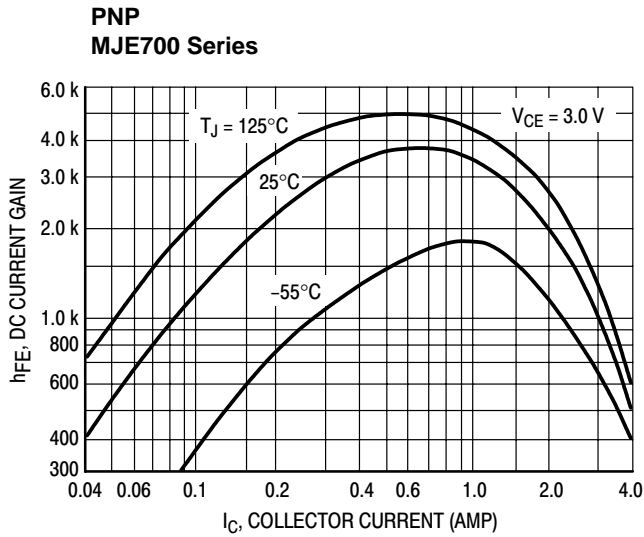


Figure 7. DC Current Gain

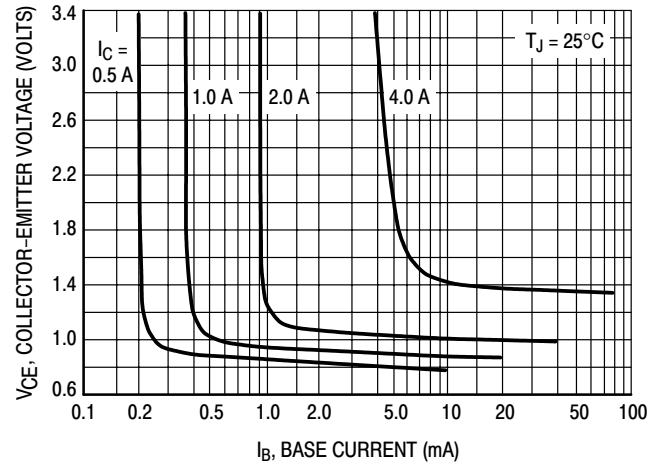
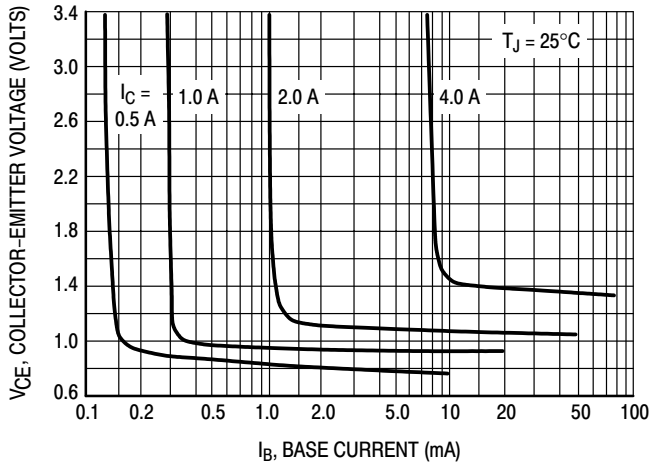


Figure 8. Collector Saturation Region

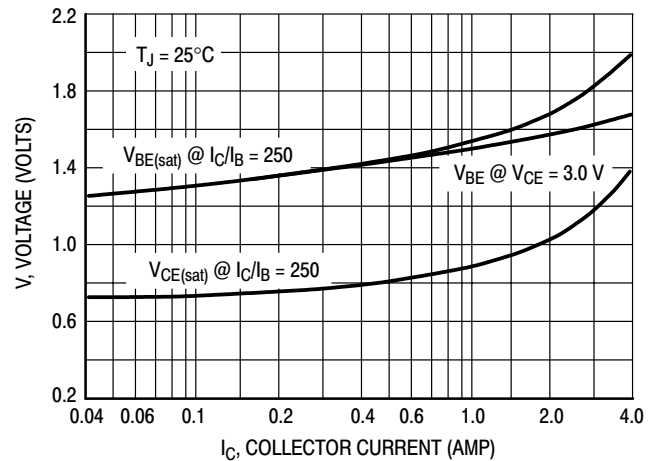
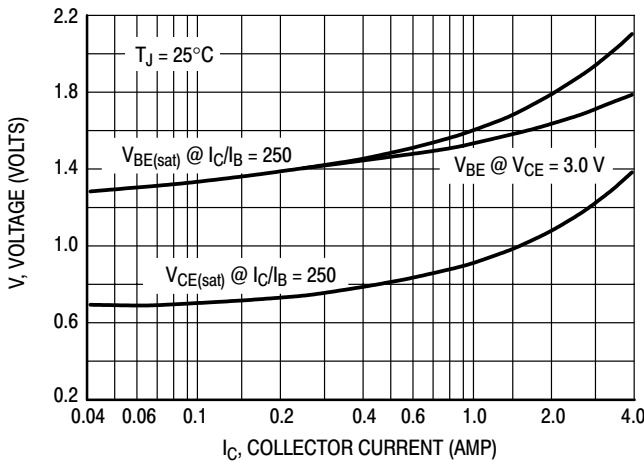


Figure 9. "On" Voltages

# Complementary Power Darlington

## For Isolated Package Applications

Designed for general-purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular TIP122 and TIP127
- 100  $V_{CEO(sus)}$
- 5 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain — 2000 (Min) @  $I_C = 3 A_{dc}$
- UL Recognized, File #E69369, to 3500  $V_{RMS}$  Isolation

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	100	Vdc
Collector–Base Voltage	$V_{CB}$	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, $T_A = 25^\circ C$ )	Test No. 1 Per Fig. 14 Test No. 2 Per Fig. 15 Test No. 3 Per Fig. 16 $V_{ISOL}$	4500 3500 1500	$V_{RMS}$
Collector Current — Continuous Peak	$I_C$	5 8	Adc
Base Current	$I_B$	0.12	Adc
Total Power Dissipation* @ $T_C = 25^\circ C$ Derate above $25^\circ C$	$P_D$	30 0.24	Watts W/ $^\circ C$
Total Power Dissipation @ $T_A = 25^\circ C$ Derate above $25^\circ C$	$P_D$	2 0.016	Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ C$

### THERMAL CHARACTERISTICS

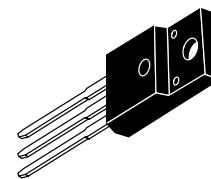
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	4.1	$^\circ C/W$
Lead Temperature for Soldering Purpose	$T_L$	260	$^\circ C$

\*Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of  $\geq 6$  in. lbs.

(1) Proper strike and creepage distance must be provided.

**NPN  
MJF122  
PNP  
MJF127**

**COMPLEMENTARY  
SILICON  
POWER DARLINGTONS  
5 AMPERES  
100 VOLTS  
30 WATTS**



**CASE 221D-02  
TO-220 TYPE**

# MJF122 MJF127

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 100\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	10	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	2	$\text{mA}$
<b>ON CHARACTERISTICS (1)</b>				
DC Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 3\text{ Vdc}$ ) ( $I_C = 3\text{ Adc}$ , $V_{CE} = 3\text{ Vdc}$ )	$h_{FE}$	1000 2000	—	—
Collector–Emitter Saturation Voltage ( $I_C = 3\text{ Adc}$ , $I_B = 12\text{ mA}$ ) ( $I_C = 5\text{ Adc}$ , $I_B = 20\text{ mA}$ )	$V_{CE(sat)}$	—	2 3.5	Vdc
Base–Emitter On Voltage ( $I_C = 3\text{ Adc}$ , $V_{CE} = 3\text{ Vdc}$ )	$V_{BE(on)}$	—	2.5	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Small–Signal Current Gain ( $I_C = 3\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$h_{fe}$	4	—	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	MJF127 MJF122 $C_{ob}$	—	300 200	$\text{pF}$

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

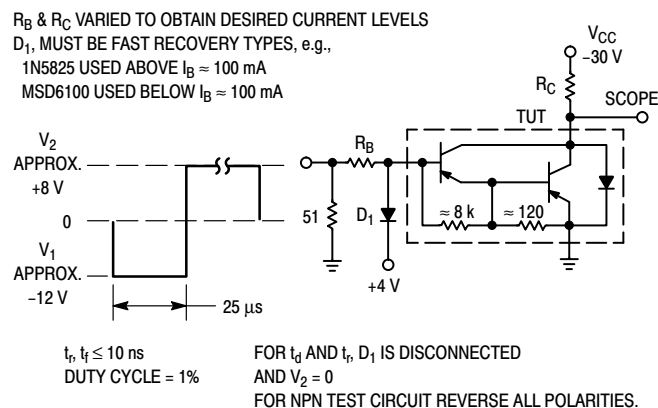


Figure 10. Switching Times Test Circuit

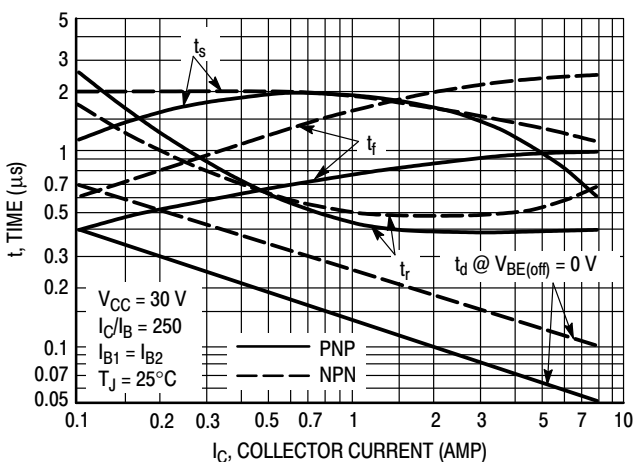


Figure 11. Typical Switching Times

# MJF122 MJF127

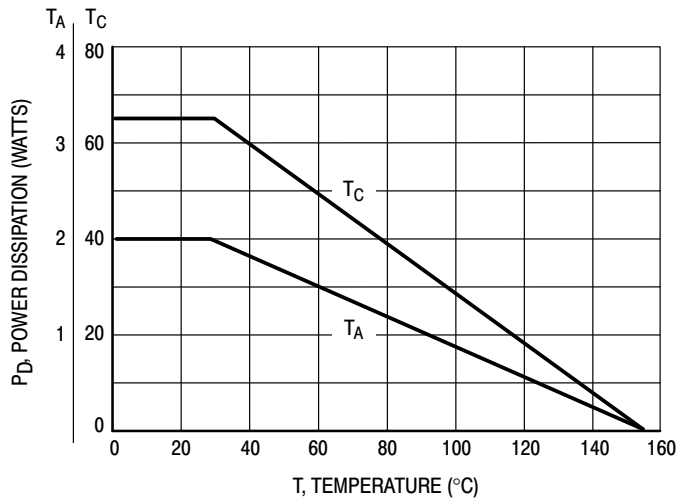


Figure 12. Maximum Power Derating

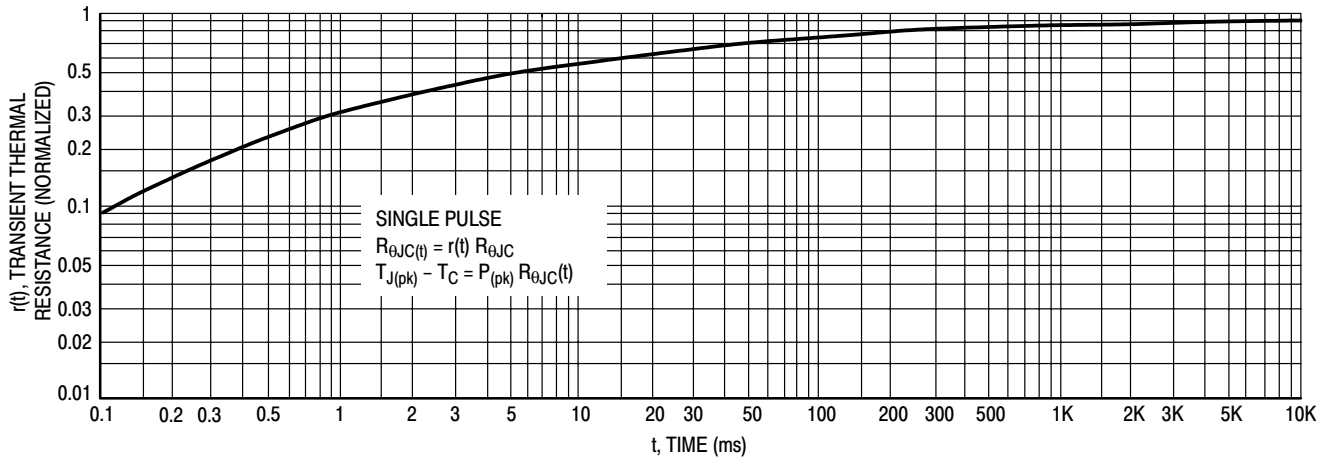


Figure 13. Thermal Response

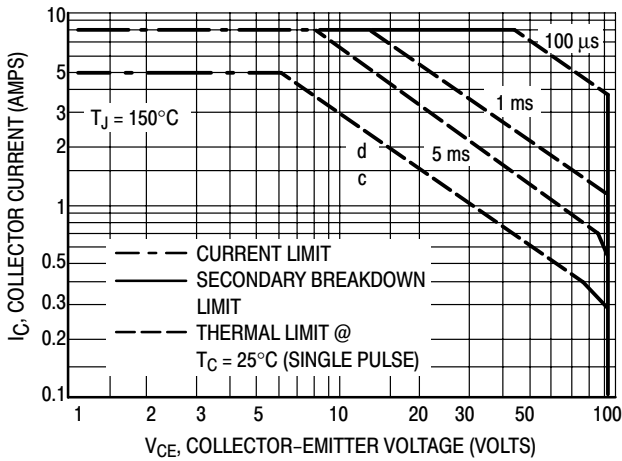


Figure 14. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 14 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

# MJF122 MJF127

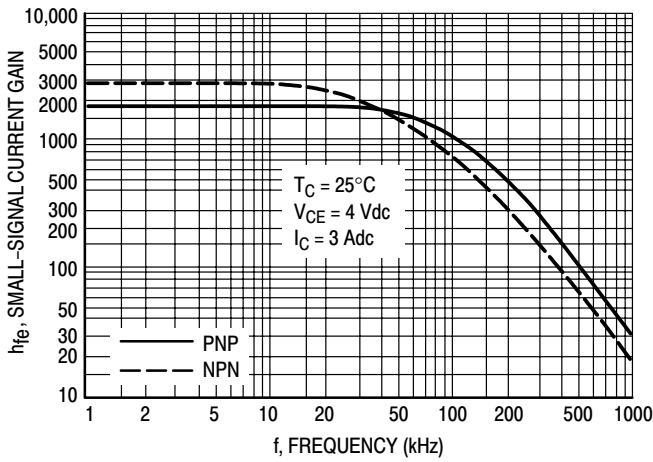


Figure 15. Typical Small-Signal Current Gain

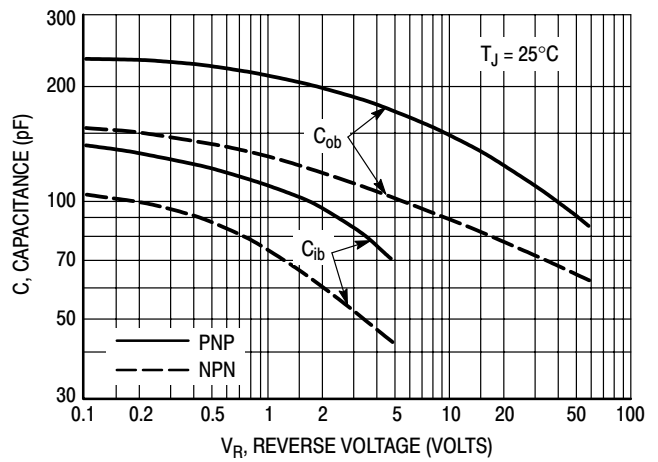


Figure 16. Typical Capacitance

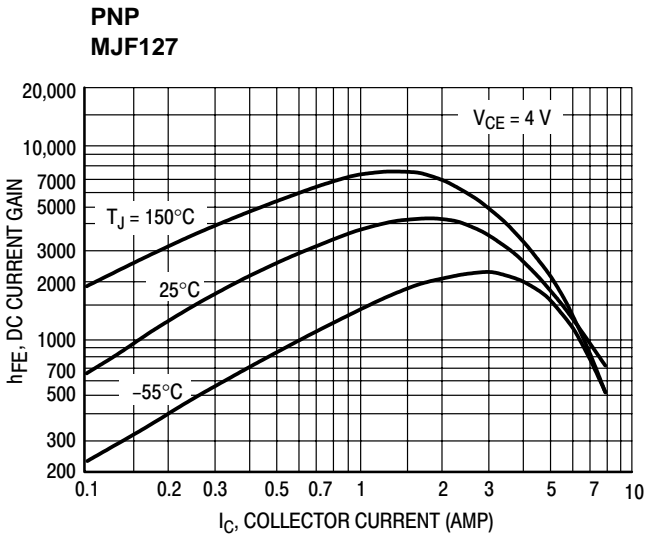
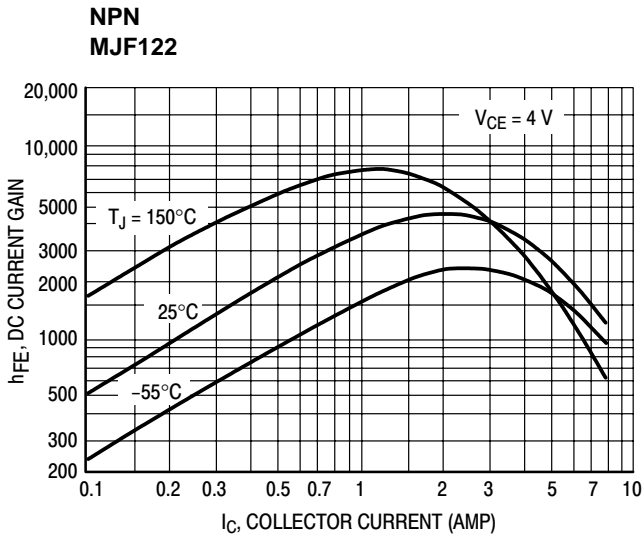


Figure 17. Typical DC Current Gain

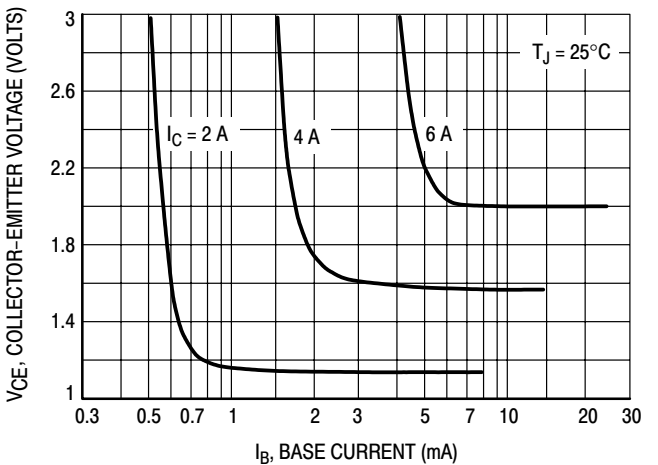
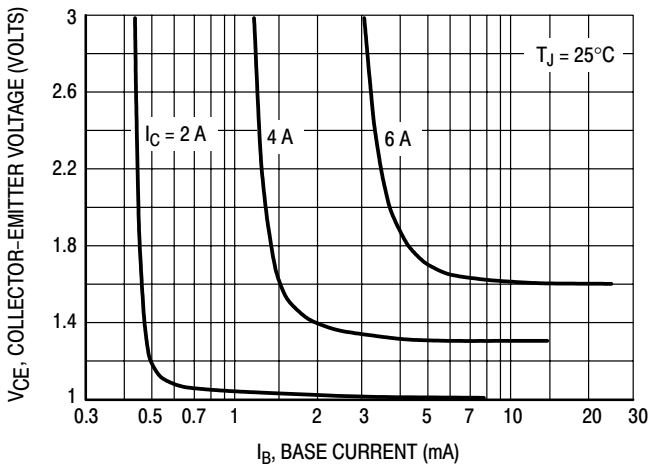
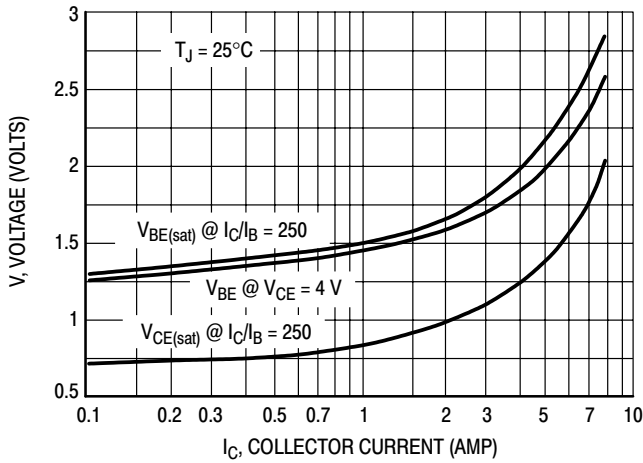


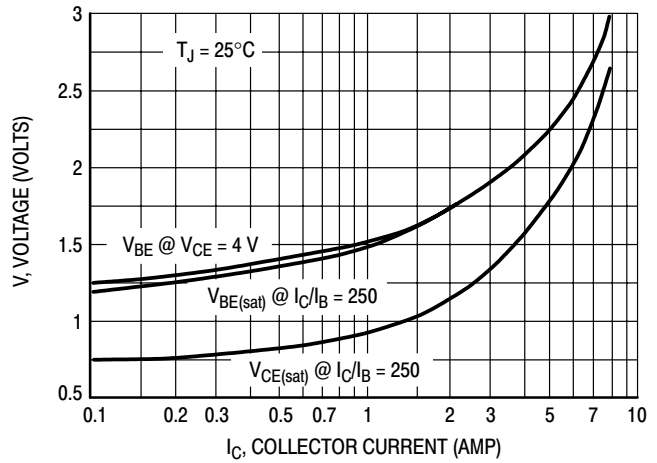
Figure 18. Typical Collector Saturation Region

# MJF122 MJF127

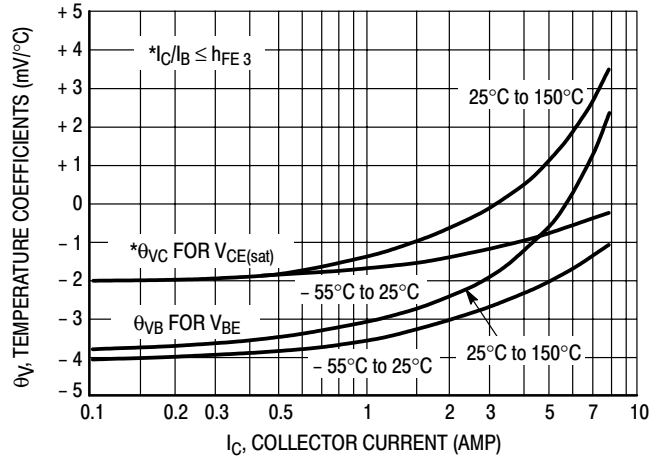
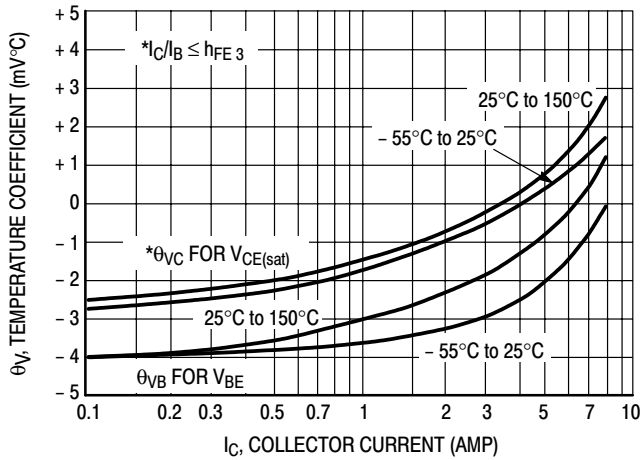
**NPN  
MJF122**



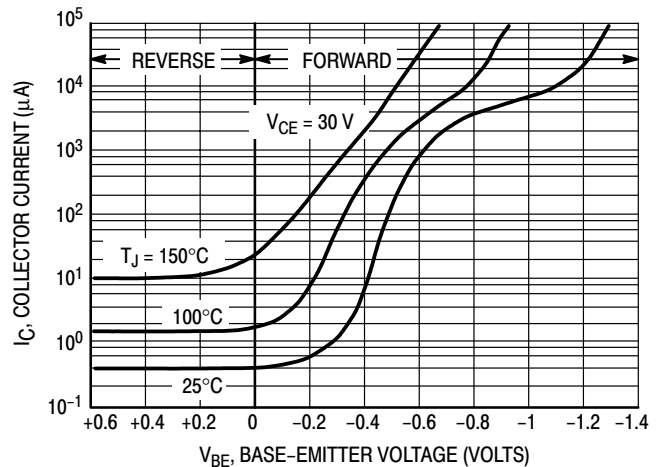
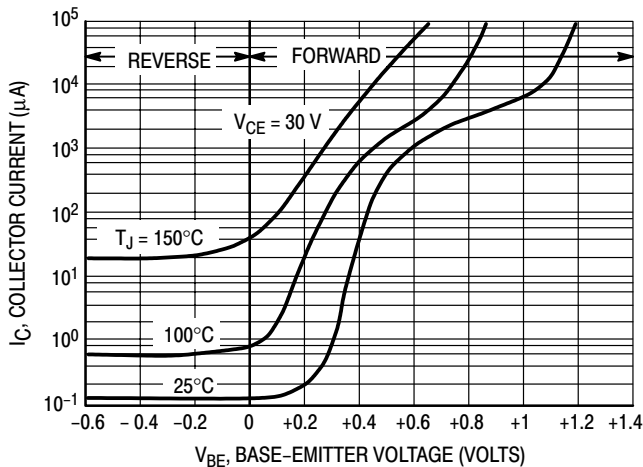
**PNP  
MJF127**



**Figure 19. Typical "On" Voltages**



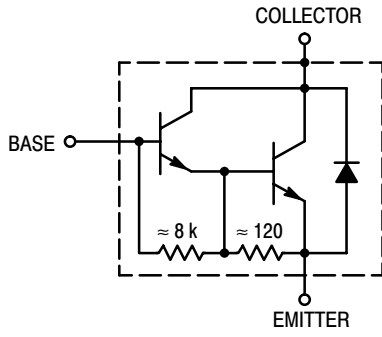
**Figure 20. Typical Temperature Coefficients**



**Figure 21. Typical Collector Cut-Off Region**

# MJF122 MJF127

NPN  
MJF122



PNP  
MJF127

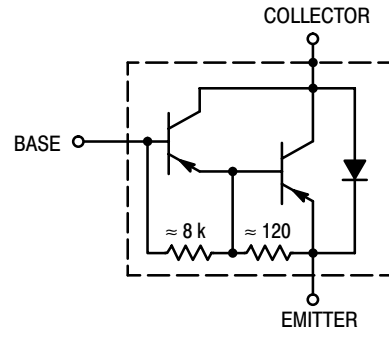


Figure 22. Darlington Schematic

TEST CONDITIONS FOR ISOLATION TESTS\*

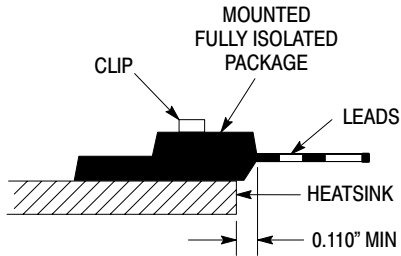


Figure 23. Clip Mounting Position for Isolation Test Number 1

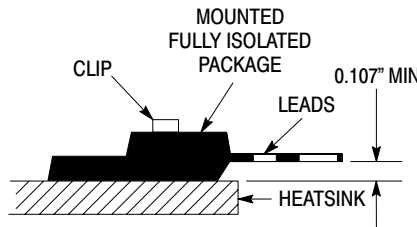


Figure 24. Clip Mounting Position for Isolation Test Number 2

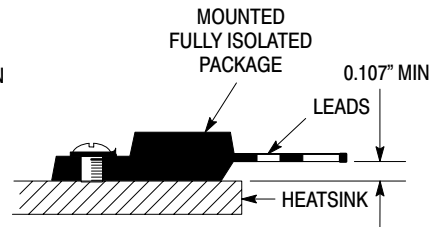


Figure 25. Screw Mounting Position for Isolation Test Number 3

\*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

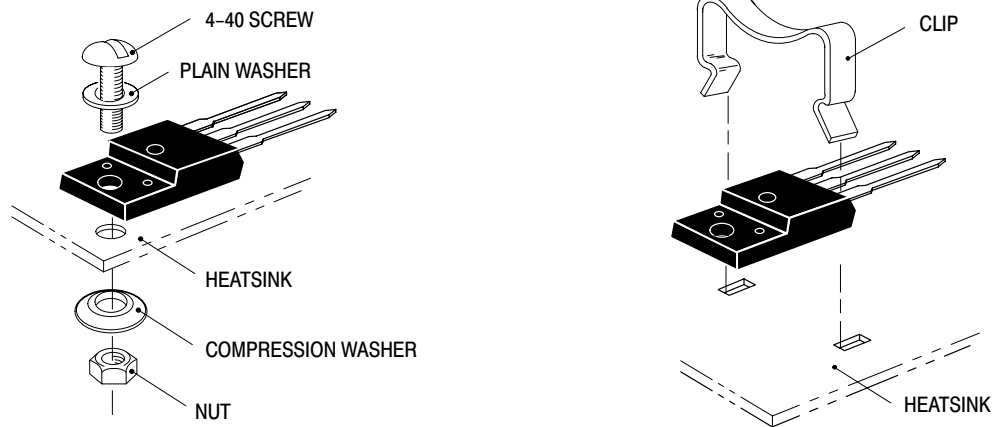


Figure 26. Typical Mounting Techniques\*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.



# Complementary Power Transistors

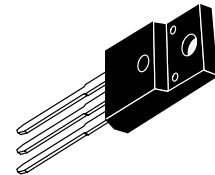
## For Isolated Package Applications

Designed for general-purpose amplifier and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular MJE15030 and MJE15031
- 150 V<sub>CEO(sus)</sub>
- 8 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High Current Gain-Bandwidth Product
$$f_T = 30 \text{ MHz (Min) @ } I_C = 500 \text{ mAdc}$$
- UL Recognized, File #E69369, to 3500 V<sub>RMS</sub> Isolation

**NPN**  
**MJF15030**  
**PNP**  
**MJF15031**

**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**8 AMPERES**  
**150 VOLTS**  
**36 WATTS**



**CASE 221D-02**  
**TO-220 TYPE**

# MJF15030 MJF15031

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	150	Vdc
Collector–Base Voltage	$V_{CB}$	150	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, $T_A = 25^\circ\text{C}$ )	$V_{ISOL}$	4500 3500 1500	$V_{RMS}$
Collector Current — Continuous — Peak	$I_C$	8 16	Adc
Base Current	$I_B$	2	Adc
Total Power Dissipation* @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	36 0.29	Watts $\text{W}/^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2 0.016	Watts $\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	3.5	$^\circ\text{C}/\text{W}$
Lead Temperature for Soldering Purpose	$T_L$	260	$^\circ\text{C}$

\*Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of  $\geq 6$  in. lbs.

(1) Proper strike and creepage distance must be provided.

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) ( $I_C = 10$ mAdc, $I_B = 0$ )	$V_{CEO(sus)}$	150	—	Vdc
Collector Cutoff Current ( $V_{CE} = 150$ Vdc, $I_B = 0$ )	$I_{CEO}$	—	10	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CB} = 150$ Vdc, $I_E = 0$ )	$I_{CBO}$	—	10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5$ Vdc, $I_C = 0$ )	$I_{EBO}$	—	10	$\mu\text{Adc}$

### ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 0.1$ Adc, $V_{CE} = 2$ Vdc) ( $I_C = 2$ Adc, $V_{CE} = 2$ Vdc) ( $I_C = 3$ Adc, $V_{CE} = 2$ Vdc) ( $I_C = 4$ Adc, $V_{CE} = 2$ Vdc)	$h_{FE}$	40 40 40 20	— — — —	—
DC Current Gain Linearity ( $V_{CE}$ from 2 V to 20 V, $I_C$ from 0.1 A to 3 A) (NPN to PNP)	$h_{FE}$	<b>Typ</b> 2 3		
Collector–Emitter Saturation Voltage ( $I_C = 1$ Adc, $I_B = 0.1$ Adc)	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter On Voltage ( $I_C = 1$ Adc, $V_{CE} = 2$ Vdc)	$V_{BE(on)}$	—	1	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain–Bandwidth Product (2) ( $I_C = 500$ mAdc, $V_{CE} = 10$ Vdc, $f_{test} = 10$ MHz)	$f_T$	30	—	MHz
--	-------	----	---	-----

#### NOTES:

- Pulse Test: Pulse Width  $\leq 300$   $\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- $f_T = |h_{fe}| \cdot f_{test}$ .

# MJF15030 MJF15031

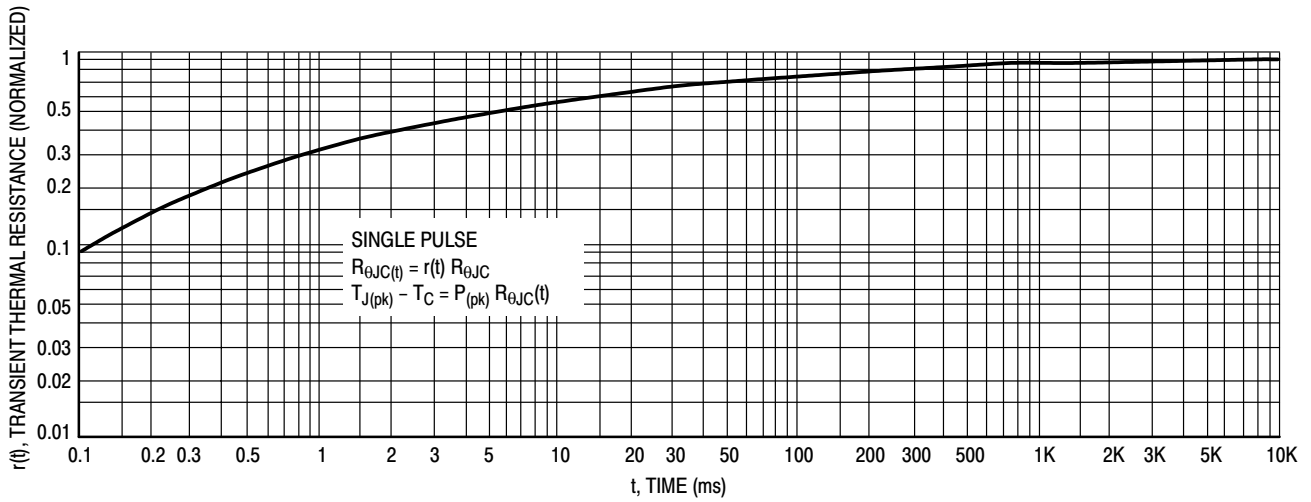


Figure 1. Thermal Response

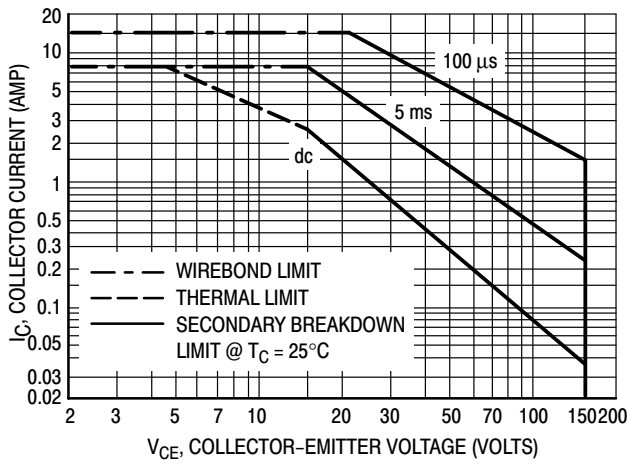
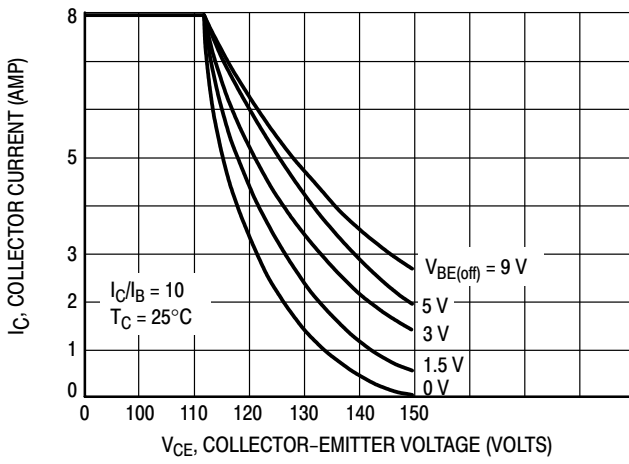


Figure 2. Forward Bias Safe Operating Area

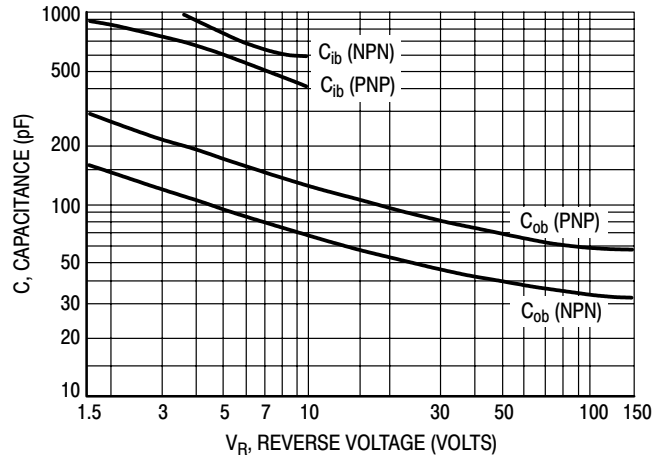
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 and 3 is based on  $T_{J(pk)} = 150^\circ C$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ C$ .  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

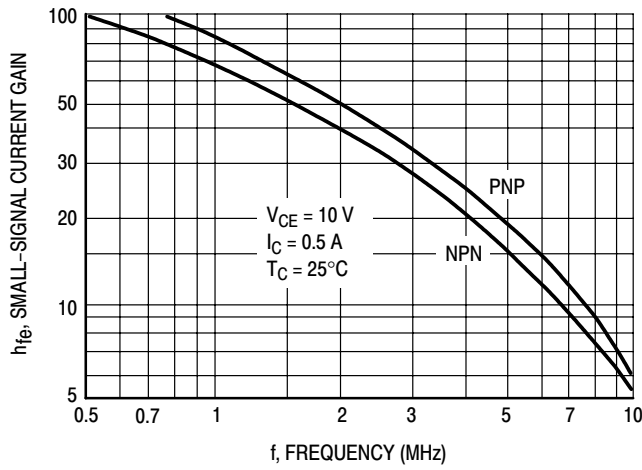
# MJF15030 MJF15031



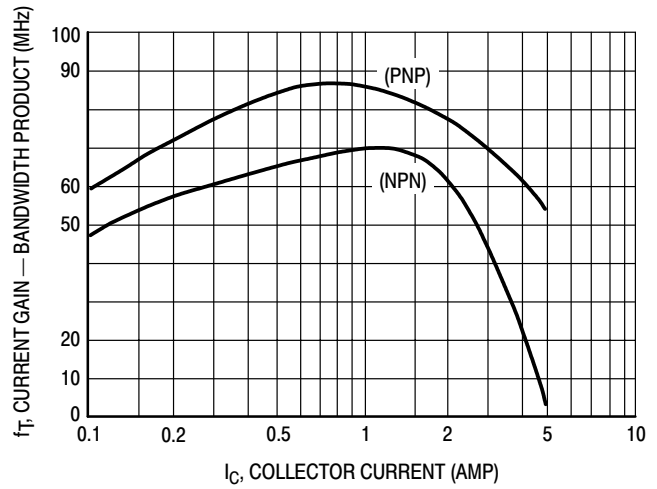
**Figure 3. Reverse Bias Switching Safe Operating Area**



**Figure 4. Capacitances**

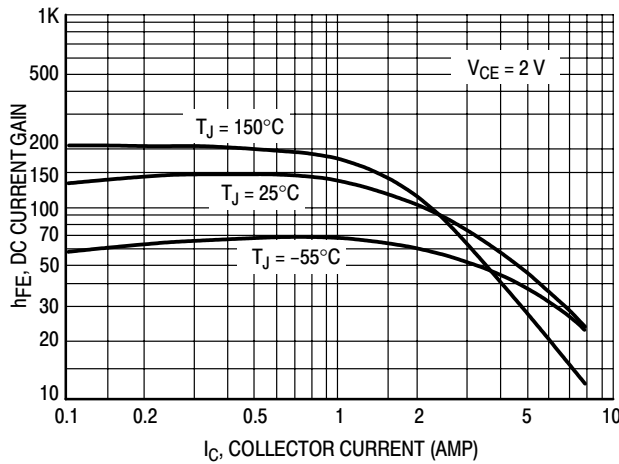


**Figure 5. Small-Signal Current Gain**

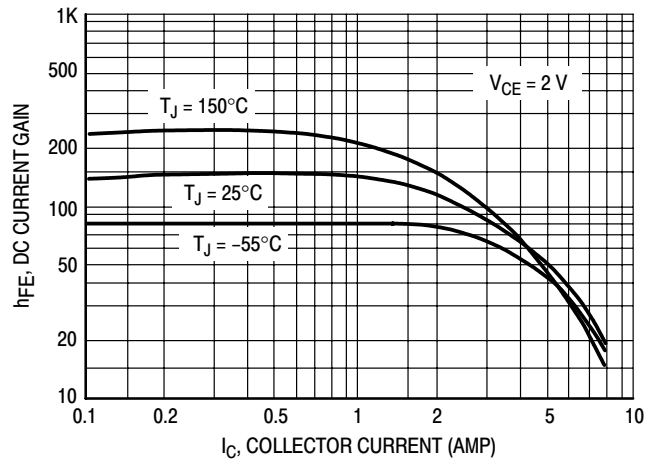


**Figure 6. Current Gain — Bandwidth Product**

## DC CURRENT GAIN



**Figure 7a. MJF15030 NPN**



**Figure 7b. MJF15031 PNP**

# MJF15030 MJF15031

## “ON” VOLTAGE

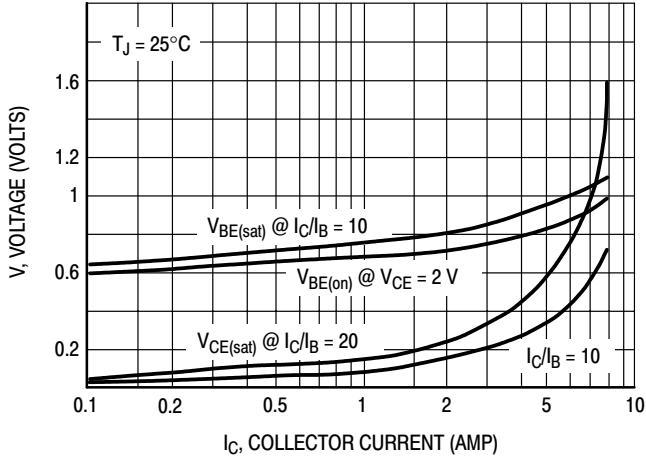


Figure 8a. MJF15030 NPN

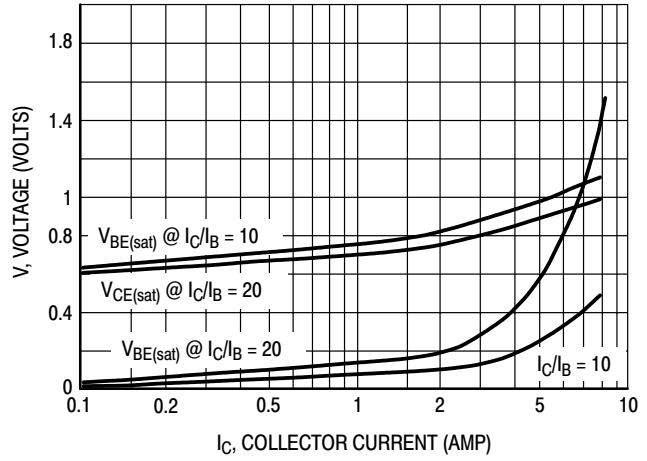


Figure 8b. MJF15031 PNP

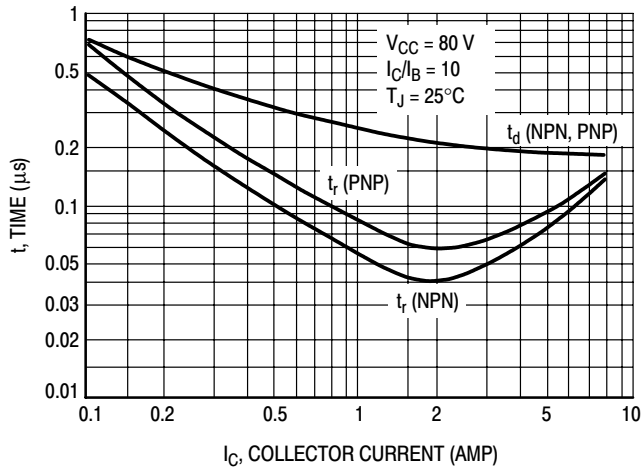


Figure 9. Turn-On Times

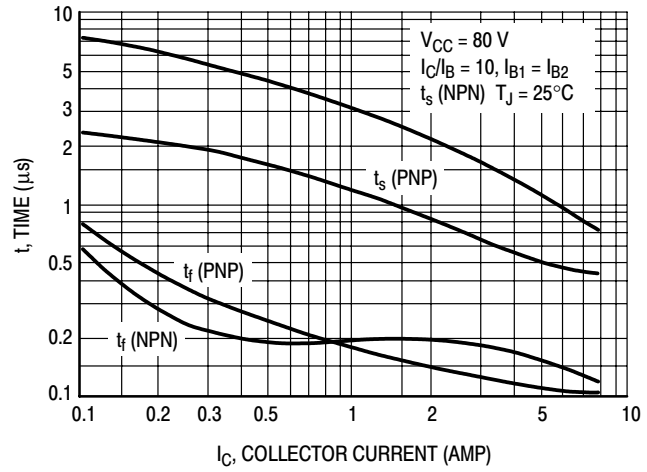
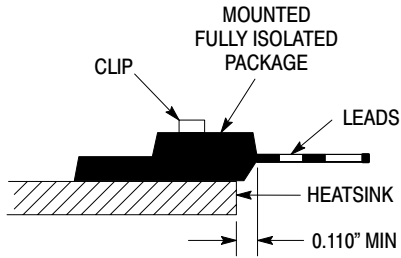


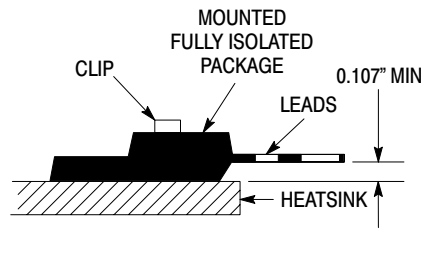
Figure 10. Turn-Off Times

# MJF15030 MJF15031

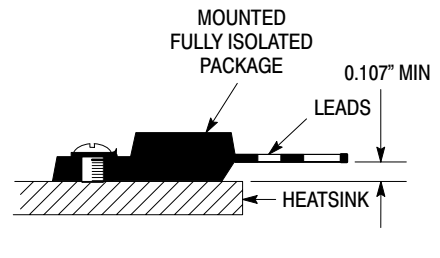
## TEST CONDITIONS FOR ISOLATION TESTS\*



**Figure 11. Clip Mounting Position for Isolation Test Number 1**



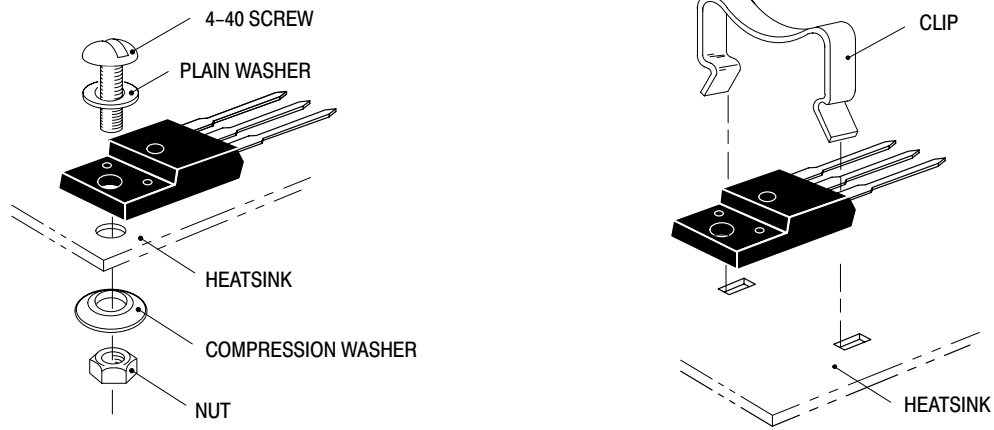
**Figure 12. Clip Mounting Position for Isolation Test Number 2**



**Figure 13. Screw Mounting Position for Isolation Test Number 3**

\*Measurement made between leads and heatsink with all leads shorted together

## MOUNTING INFORMATION



**Figure 14. Typical Mounting Techniques\***

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.

# Complementary Silicon Power Transistors

... specifically designed for general purpose amplifier and switching applications.

- Isolated Overmold Package (1500 Volts RMS Min)
- Electrically Similar to the Popular MJE3055T and MJE2955T
- Collector–Emitter Sustaining Voltage —  $V_{CEO(sus)}$  90 Volts
- 10 Amperes Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- UL Recognized, File #E69369, to 3500  $V_{RMS}$  Isolation

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	90	Vdc
Collector–Emitter Breakdown Voltage	$V_{CES}$	90	Vdc
Base–Emitter Voltage	$V_{EBO}$	5	Vdc
Collector Current — Continuous	$I_C$	10	Adc
Base Current — Continuous	$I_B$	6	Adc
RMS Isolation Voltage (3) (for 1 sec, R.H. < 30%, $T_A = 25^\circ\text{C}$ )	Test No. 1 Per Fig. 4 Test No. 2 Per Fig. 5 Test No. 3 Per Fig. 6 $V_{ISOL}$	4500 3500 1500	$V_{RMS}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ (2) Derate above $25^\circ\text{C}$	$P_D$	30 0.25	Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2 0.016	Watts W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case (2)	$R_{\theta JC}$	4	$^\circ\text{C}/\text{W}$
Thermal Resistance — Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Lead Temperature for Soldering Purposes	$T_L$	260	$^\circ\text{C}$

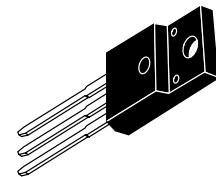
(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq$  10%.

(2) Measurement made with thermocouple contacting the bottom insulated surface (in a location beneath the die), the devices mounted on a heatsink with thermal grease and a mounting torque of  $\geq$  6 in. lbs.

(3) Proper strike and creepage distance must be provided.

**NPN**  
**MJF3055**  
**PNP**  
**MJF2955**

**COMPLEMENTARY**  
**SILICON**  
**POWER TRANSISTORS**  
**10 AMPERES**  
**90 VOLTS**  
**30 WATTS**



**CASE 221D-02**  
**TO-220 TYPE**

# MJF3055 MJF2955

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS (1)

Collector–Emitter Sustaining Voltage ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	90	—	Vdc
Collector Cutoff Current ( $V_{CE} = 90\text{ Vdc}$ , $V_{BE} = 0$ )	$I_{CES}$	—	1	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 90\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	1	$\mu\text{Adc}$
Emitter–Base Leakage ( $V_{EB} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1	$\mu\text{Adc}$

### ON CHARACTERISTICS (1)

DC Current Gain ( $I_{CE} = 4\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_{CE} = 10\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$h_{FE}$	20 5	100 —	—
Collector–Emitter Saturation Voltage ( $I_C = 4\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 3.3\text{ Adc}$ )	$V_{CE(sat)}$	— —	1 2.5	Vdc
Base–Emitter On Voltage ( $I_C = 4\text{ Adc}$ , $V_{BE} = 4\text{ Vdc}$ )	$V_{BE(on)}$	—	1.5	Vdc

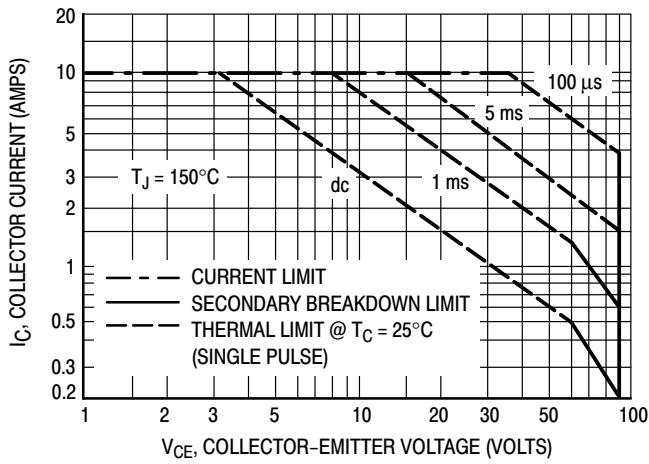
### DYNAMIC CHARACTERISTICS

Current–Gain–Bandwidth Product ( $V_{CE} = 10\text{ Vdc}$ , $I_C = 0.5\text{ Adc}$ , $f_{test} = 500\text{ kHz}$ )	$f_T$	2	—	MHz
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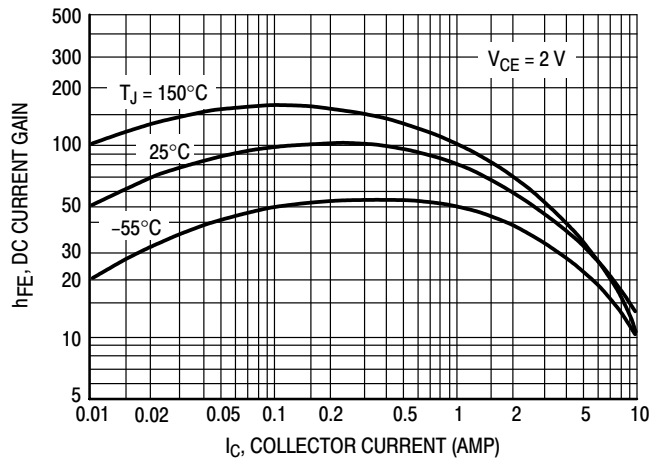
(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq 10\%$ .



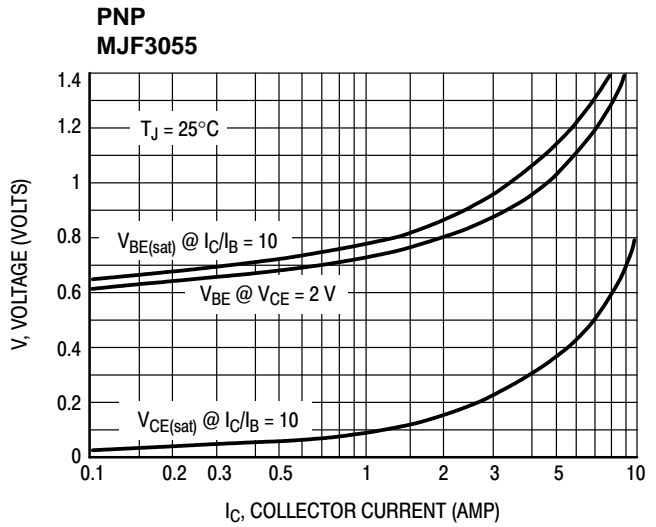
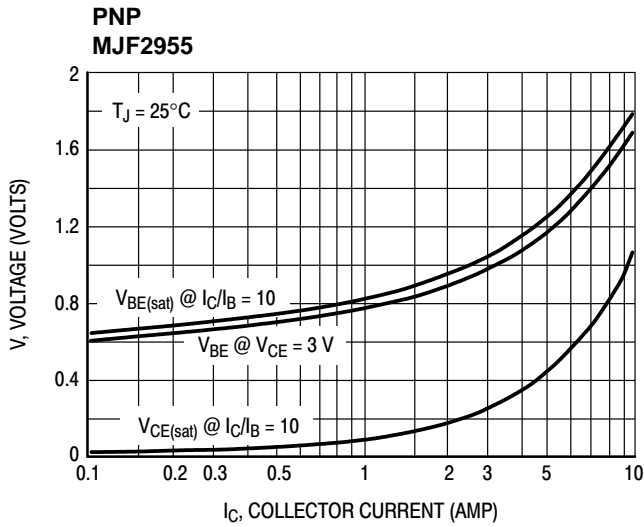
# MJF3055 MJF2955



**Figure 7. Maximum Forward Bias Safe Operating Area**



**Figure 8. DC Current Gain**



**Figure 9. "On" Voltages**

TEST CONDITIONS FOR ISOLATION TESTS\*

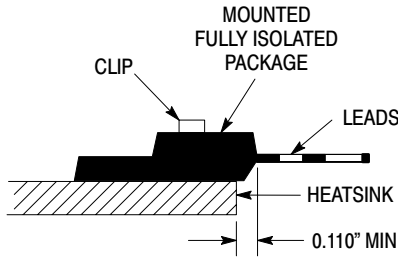


Figure 10. Clip Mounting Position for Isolation Test Number 1

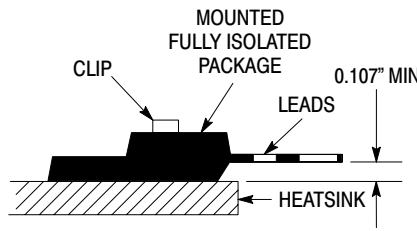


Figure 11. Clip Mounting Position for Isolation Test Number 2

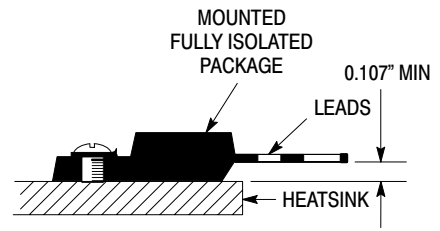


Figure 12. Screw Mounting Position for Isolation Test Number 3

\*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

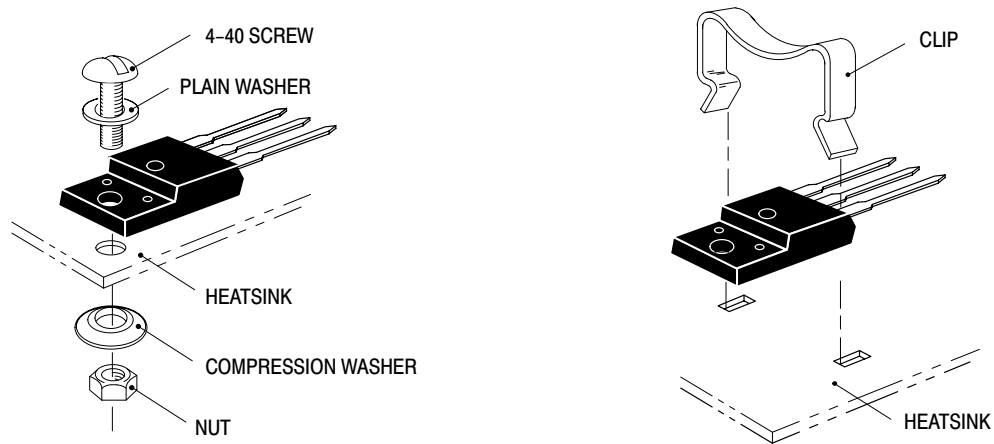


Figure 13. Typical Mounting Techniques\*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.

# MJF44H11 (NPN), MJF45H11 (PNP)

Preferred Devices

## Complementary Power Transistors

### For Isolated Package Applications

... for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector–Emitter Saturation Voltage –  
 $V_{CE(sat)} = 1.0 \text{ V (Max) @ } 8.0 \text{ A}$
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
Collector Current – Continuous – Peak	$I_C$	10 20	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	50 1.67	Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–55 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

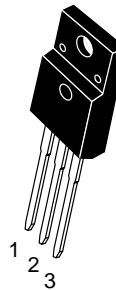
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$



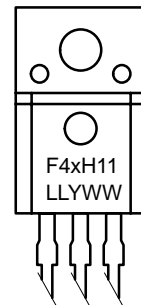
ON Semiconductor™

<http://onsemi.com>

**SILICON POWER  
TRANSISTORS  
10 AMPERES  
80 VOLTS  
50 WATTS**



#### MARKING DIAGRAM



**ISOLATED TO–220  
CASE 221D  
PLASTIC**

F4xH11 = Specific Device Code  
x = 4 or 5  
LL = Location Code  
Y = Year  
WW = Work Week

#### ORDERING INFORMATION

Device	Package	Shipping
MJF44H11	TO–220	50 Units/Rail
MJF45H11	TO–220	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

## MJF44H11 (NPN), MJF45H11 (PNP)

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CE(sus)}$	80	–	–	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CE0}$ , $V_{BE} = 0$ )	$I_{CES}$	–	–	1.0	$\mu\text{A}$
Emitter Cutoff Current ( $V_{EB} = 5\text{ Vdc}$ )	$I_{EBO}$	–	–	10	$\mu\text{A}$

### ON CHARACTERISTICS

Collector–Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )	$V_{CE(sat)}$	–	–	1.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.8\text{ Adc}$ )	$V_{BE(sat)}$	–	–	1.5	Vdc
DC Current Gain ( $V_{CE} = 1\text{ Vdc}$ , $I_C = 2\text{ Adc}$ )	$h_{FE}$	60	–	–	–
DC Current Gain ( $V_{CE} = 1\text{ Vdc}$ , $I_C = 4\text{ Adc}$ )		40	–	–	–

### DYNAMIC CHARACTERISTICS

Collector Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $f_{\text{test}} = 1\text{ MHz}$ )	MJF44H11 MJF45H11	$C_{cb}$	– –	130 230	– –	$\mu\text{F}$
Gain Bandwidth Product ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 20\text{ MHz}$ )	MJF44H11 MJF45H11	$f_T$	– –	50 40	– –	MHz

### SWITCHING TIMES

Delay and Rise Times ( $I_C = 5\text{ Adc}$ , $I_{B1} = 0.5\text{ Adc}$ )	MJF44H11 MJF45H11	$t_d + t_r$	– –	300 135	– –	ns
Storage Time ( $I_C = 5\text{ Adc}$ , $I_{B1} = I_{B2} = 0.5\text{ Adc}$ )	MJF44H11 MJF45H11	$t_s$	– –	500 500	– –	ns
Fall Time ( $I_C = 5\text{ Adc}$ , $I_{B1} = I_{B2} = 0.5\text{ Adc}$ )	MJF44H11 MJF45H11	$t_f$	– –	140 100	– –	ns

# MJF44H11 (NPN), MJF45H11 (PNP)

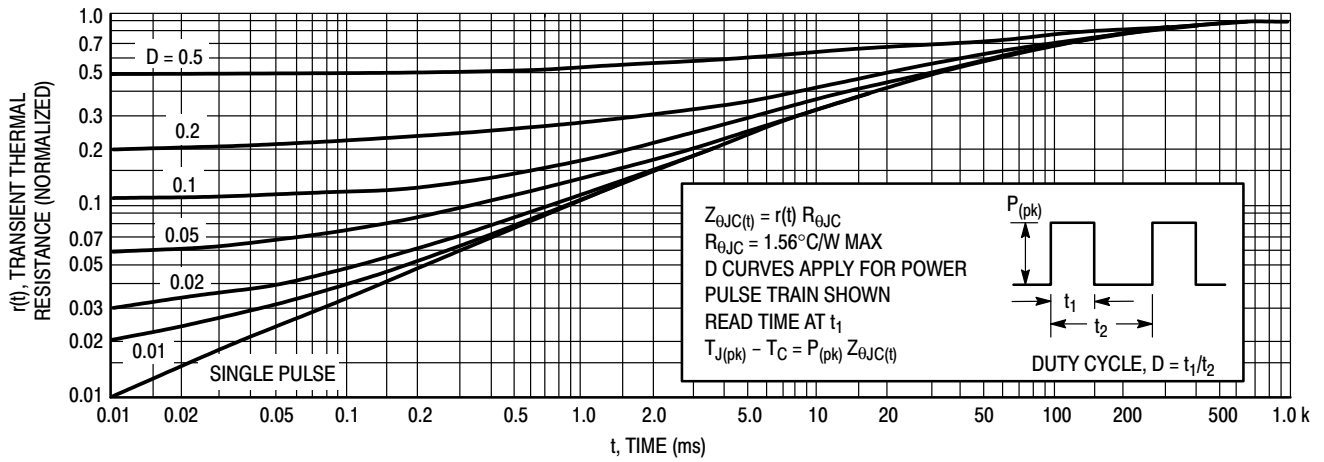


Figure 1. Thermal Response

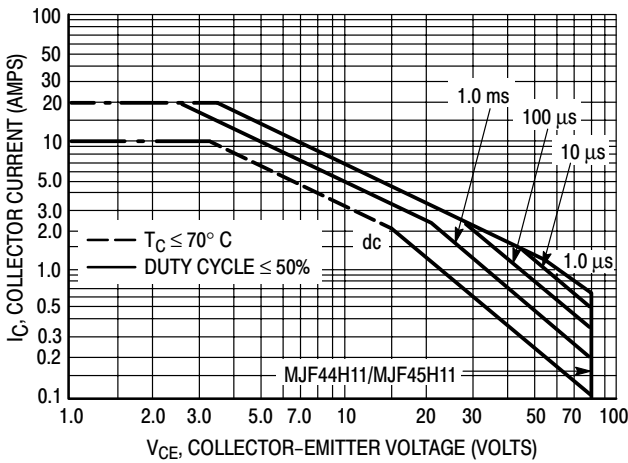


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

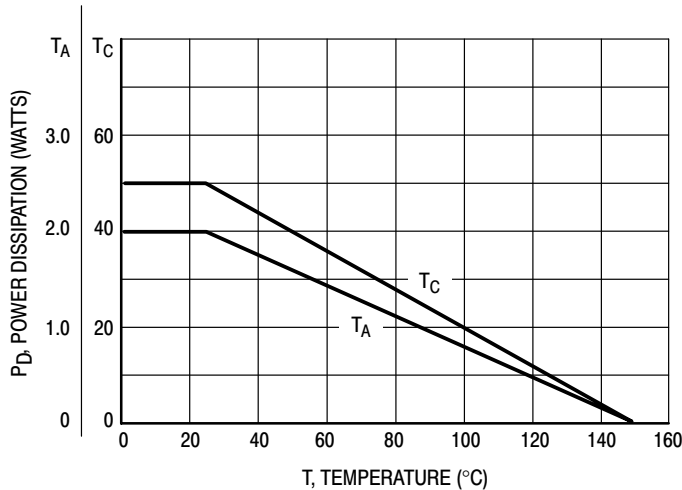


Figure 3. Power Derating

# MJF44H11 (NPN), MJF45H11 (PNP)

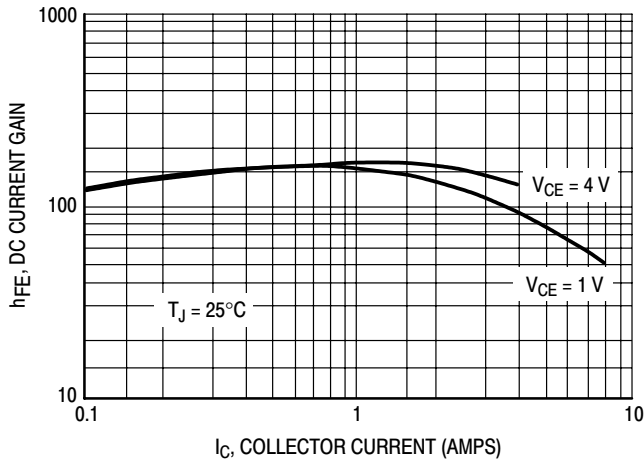


Figure 4. MJF44H11 DC Current Gain

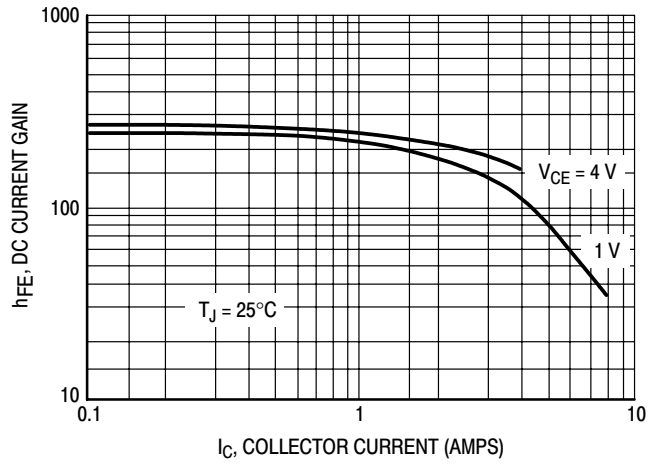


Figure 5. MJF45H11 DC Current Gain

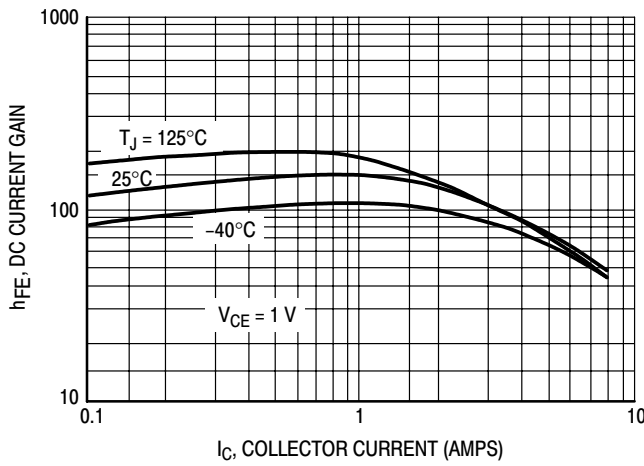


Figure 6. MJF44H11 Current Gain versus Temperature

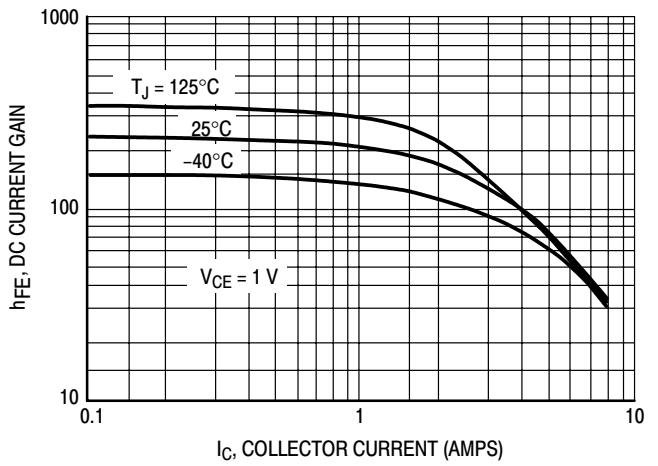


Figure 7. MJF45H11 Current Gain versus Temperature

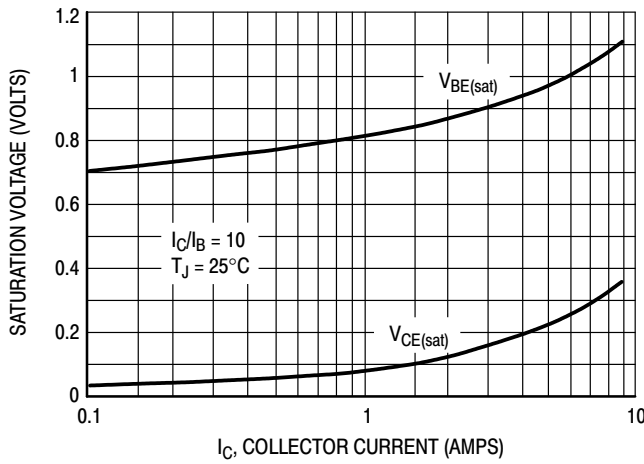


Figure 8. MJF44H11 On-Voltages

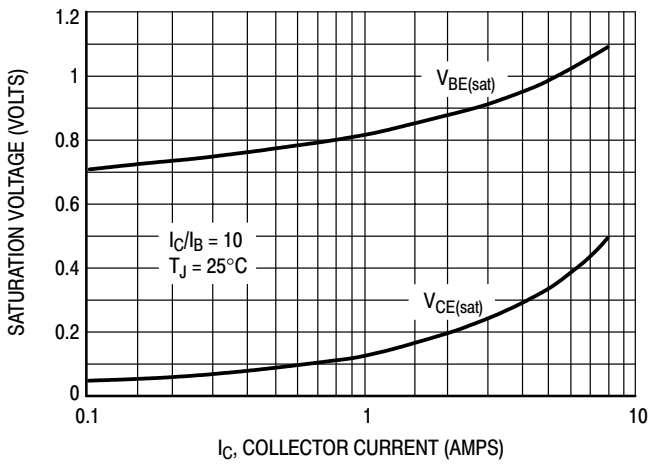


Figure 9. MJF45H11 On-Voltages

# High Voltage Power Transistor

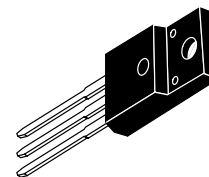
## Isolated Package Applications

Designed for line operated audio output amplifiers, switching power supply drivers and other switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular TIP47
- 250 V<sub>CEO(sus)</sub>
- 1 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- UL Recognized, File #E69369, to 3500 V<sub>RMS</sub> Isolation

# MJF47

**NPN SILICON  
POWER TRANSISTOR  
1 AMPERE  
250 VOLTS  
28 WATTS**



**CASE 221D-02  
TO-220 TYPE**

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V <sub>CEO</sub>	250	Vdc
Collector–Base Voltage	V <sub>CB</sub>	350	Vdc
Emitter–Base Voltage	V <sub>EB</sub>	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T <sub>A</sub> = 25°C)	V <sub>ISOL</sub>	4500 3500 1500	V <sub>RMS</sub>
Collector Current — Continuous Peak	I <sub>C</sub>	1 2	Adc
Base Current	I <sub>B</sub>	0.6	Adc
Total Power Dissipation* @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	28 0.23	Watts W/°C
Total Power Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	2 0.016	Watts W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–65 to +150	°C

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	62.5	°C/W
Thermal Resistance, Junction to Case*	R <sub>θJC</sub>	4.4	°C/W
Lead Temperature for Soldering Purpose	T <sub>L</sub>	260	°C

\*Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

(1) Proper strike and creepage distance must be provided.

# MJF47

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	250	—	Vdc
Collector Cutoff Current ( $V_{CE} = 150\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	0.2	mAdc
Collector Cutoff Current ( $V_{CE} = 350\text{ Vdc}$ , $V_{BE} = 0$ )	$I_{CES}$	—	0.1	mAdc
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1	mAdc

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 0.3\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ ) ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ )	$h_{FE}$	30 10	150 —	—
Collector–Emitter Saturation Voltage ( $I_C = 1\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	$V_{CE(sat)}$	—	1	Vdc
Base–Emitter On Voltage ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ )	$V_{BE(on)}$	—	1.5	Vdc

## DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ( $I_C = 0.2\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 2\text{ MHz}$ )	$f_T$	10	—	MHz
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(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

## TYPICAL CHARACTERISTICS

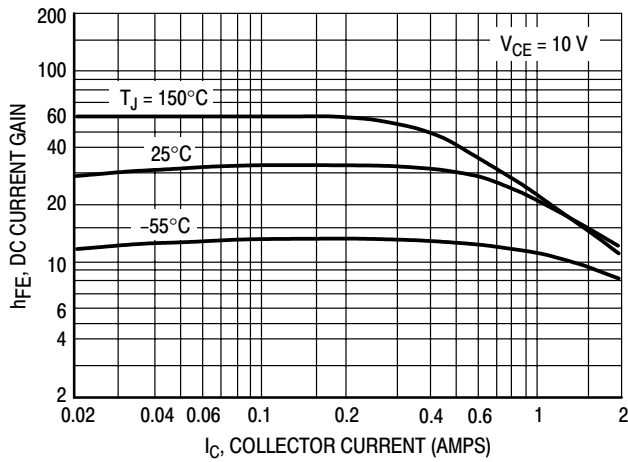


Figure 1. DC Current Gain

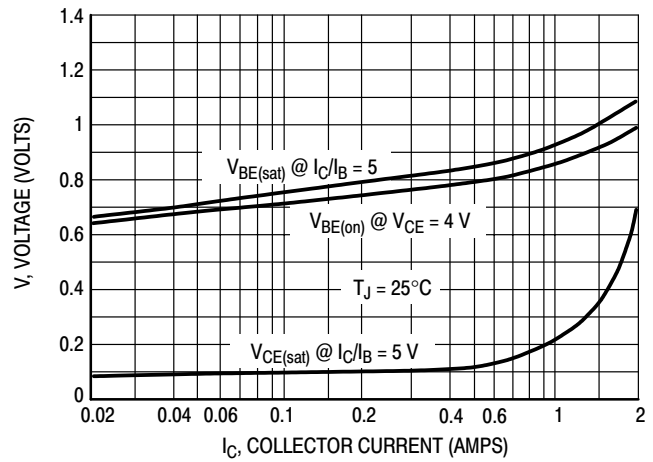


Figure 2. "On" Voltages



# MJF47

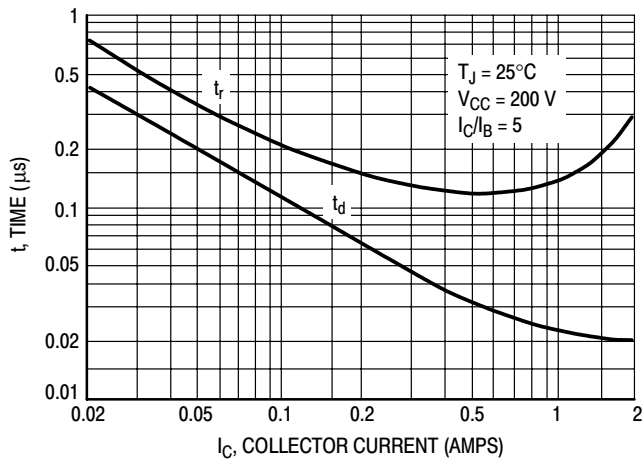


Figure 3. Turn-On Time

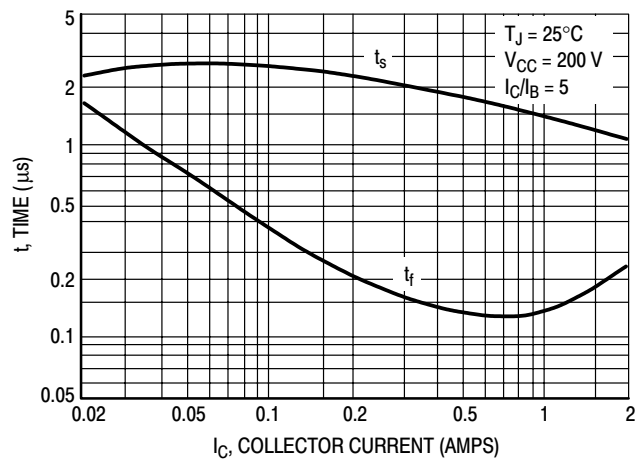


Figure 4. Turn-Off Time

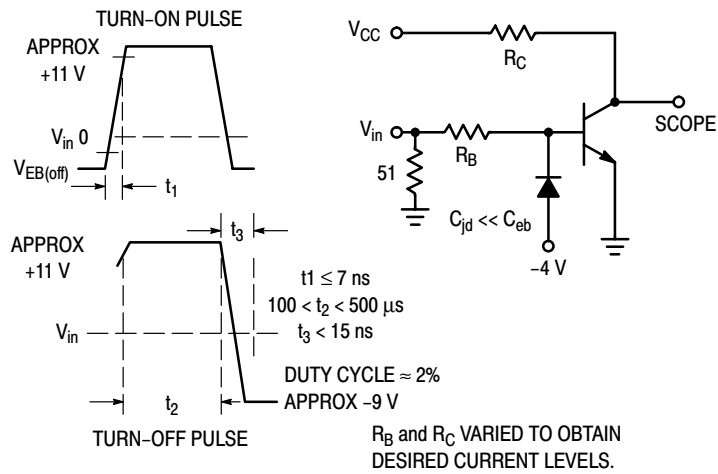


Figure 5. Switching Time Equivalent Circuit

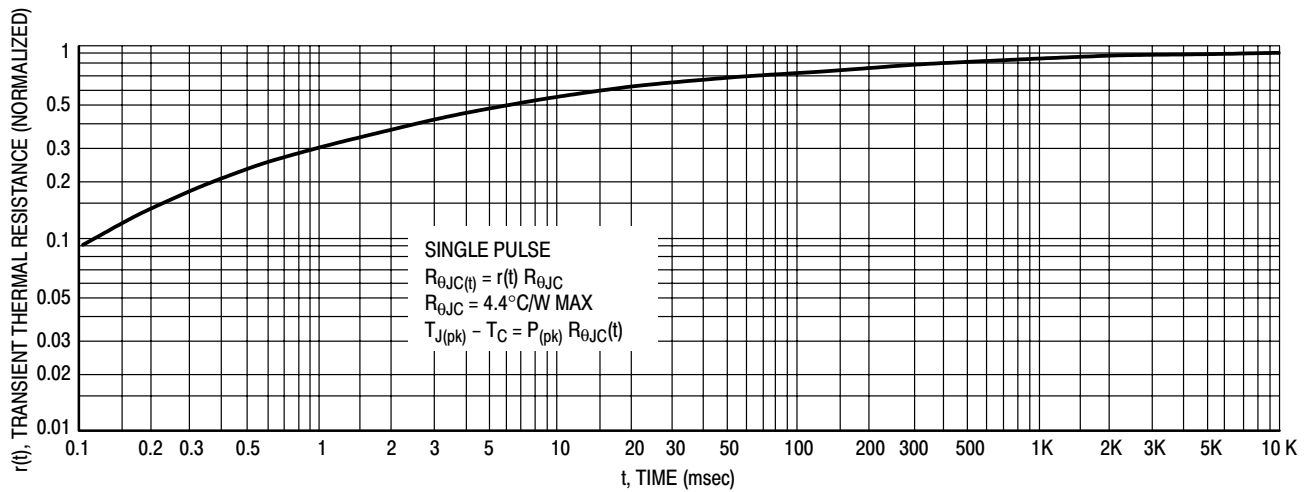
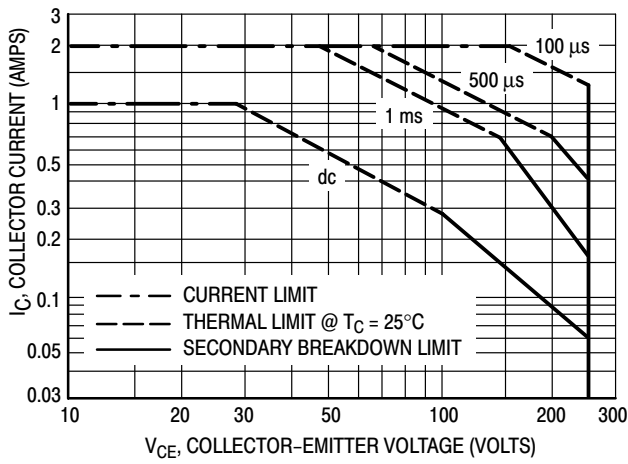


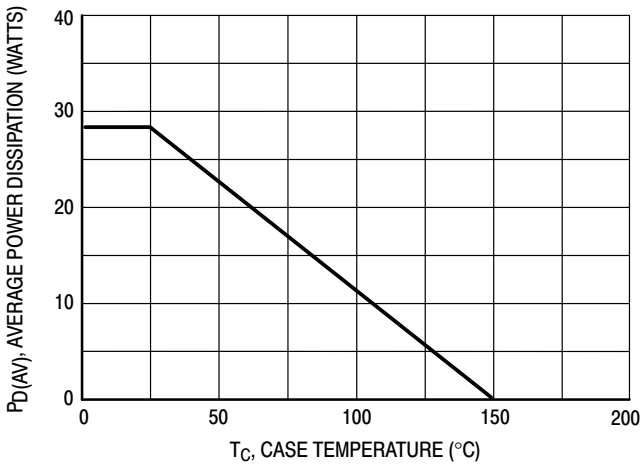
Figure 6. Thermal Response



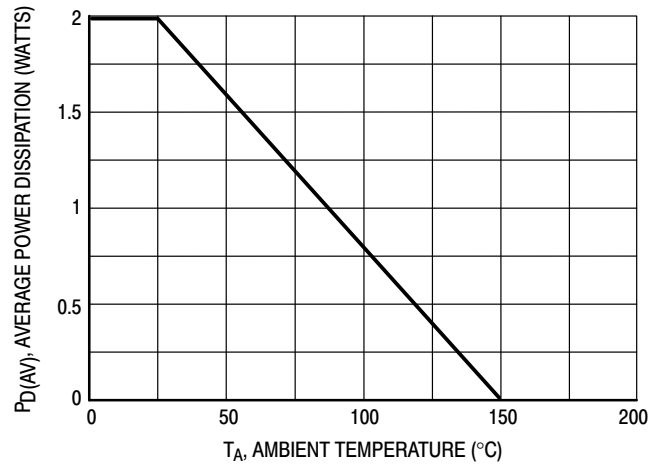
**Figure 7. Maximum Forward Bias Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 8. Power Derating**



**Figure 9. Power Derating**

# MJF47

## TEST CONDITIONS FOR ISOLATION TESTS\*

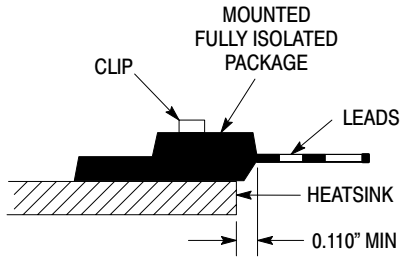


Figure 10. Clip Mounting Position for Isolation Test Number 1

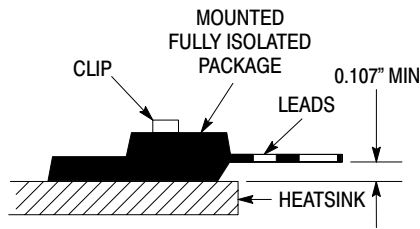


Figure 11. Clip Mounting Position for Isolation Test Number 2

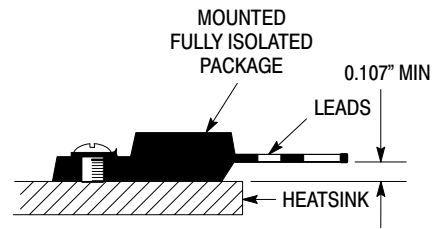


Figure 12. Screw Mounting Position for Isolation Test Number 3

\*Measurement made between leads and heatsink with all leads shorted together

## MOUNTING INFORMATION

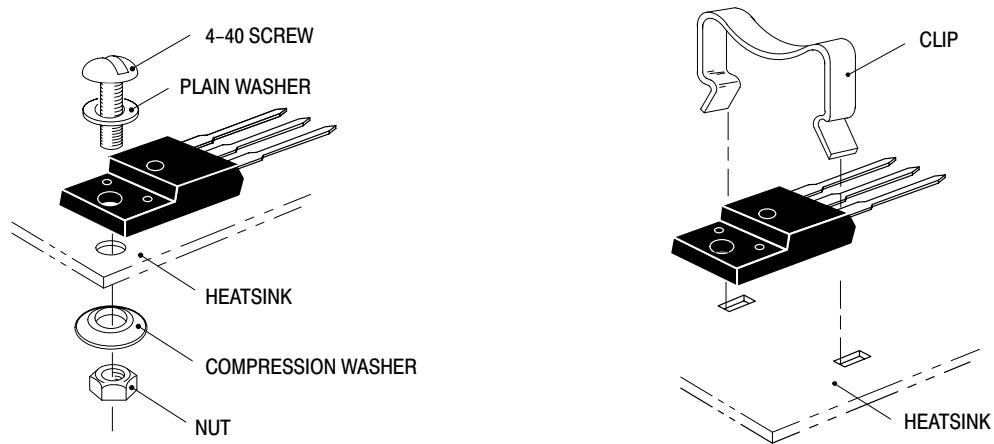


Figure 13. Typical Mounting Techniques\*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.

# Complementary Power Darlington

## For Isolated Package Applications

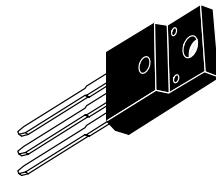
Designed for general-purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Isolated Overmold Package, TO-220 Type
- Electrically Similar to the Popular 2N6388, 2N6668, TIP102 and TIP107
- 100 V<sub>CEO(sus)</sub>
- 10 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain — 1000 (Min) @ I<sub>C</sub> = 5.0 Adc
- High Isolation Voltage (up to 4500 VRMS)
- Case 221D is UL Recognized at 3500 VRMS: File #E69369

**NPN**  
**MJF6388\***  
**PNP**  
**MJF6668\***

\*ON Semiconductor Preferred Devices

**COMPLEMENTARY  
SILICON  
POWER DARLINGTONS**  
**10 AMPERES**  
**100 VOLTS**  
**40 WATTS**



**CASE 221D-02  
UL RECOGNIZED**

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V <sub>CEO</sub>	100	Vdc
Collector–Base Voltage	V <sub>CB</sub>	100	Vdc
Emitter–Base Voltage	V <sub>EB</sub>	5.0	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T <sub>A</sub> = 25°C)	V <sub>ISOL</sub>	4500 3500 1500	V
Collector Current — Continuous — Peak(2)	I <sub>C</sub>	10 15	Adc
Base Current	I <sub>B</sub>	1.0	Adc
Total Power Dissipation* @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	40 0.31	Watts W/°C
Total Power Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	2.0 0.016	Watts W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–65 to +150	°C

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case*	R <sub>θJC</sub>	3.2	°C/W
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	62.5	°C/W
Lead Temperature for Soldering Purpose	T <sub>L</sub>	260	°C

(1) Proper strike and creepage distance must be provided.

(2) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

\*Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink, thermal grease applied and a mounting torque of 6 to 8 in•lbs.

**Preferred** devices are ON Semiconductor recommended choices for future use and best overall value.

# MJF6388 MJF6668

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CE(sus)}$	100	—	Vdc
Collector Cutoff Current ( $V_{CE} = 80\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	10	$\mu\text{A}$
Collector Cutoff Current ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$	—	10 3.0	$\mu\text{A}$ mA
Collector Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	10	$\mu\text{A}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	2.0	mA

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 3.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 5.0\text{ A}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 8.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 10\text{ A}$ , $V_{CE} = 3.0\text{ Vdc}$ )	$h_{FE}$	3000 1000 200 100	15000 — — —	—
Collector–Emitter Saturation Voltage ( $I_C = 3.0\text{ A}$ , $I_B = 6.0\text{ mA}$ ) ( $I_C = 5.0\text{ A}$ , $I_B = 0.01\text{ A}$ ) ( $I_C = 8.0\text{ A}$ , $I_B = 80\text{ mA}$ ) ( $I_C = 10\text{ A}$ , $I_B = 0.1\text{ A}$ )	$V_{CE(sat)}$	— — — —	2.0 2.0 2.5 3.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 5.0\text{ A}$ , $I_B = 0.01\text{ A}$ ) ( $I_C = 10\text{ A}$ , $I_B = 0.1\text{ A}$ )	$V_{BE(sat)}$	— —	2.8 4.5	Vdc
Base–Emitter On Voltage ( $I_C = 8.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	2.5	Vdc

## DYNAMIC CHARACTERISTICS

Small–Signal Current Gain ( $I_C = 1.0\text{ A}$ , $V_{CE} = 5.0\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$ h_{fe} $	20	—	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	MJF6388 MJF6668 $C_{ob}$	—	200 300	pF
Insulation Capacitance (Collector–to–External Heatsink)	$C_{c-hs}$	—	3.0 Typ	pF
Small–Signal Current Gain ( $I_C = 1.0\text{ A}$ , $V_{CE} = 5.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	1000	—	—

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

**NPN**  
**MJF6388**

**PNP**  
**MJF6668**

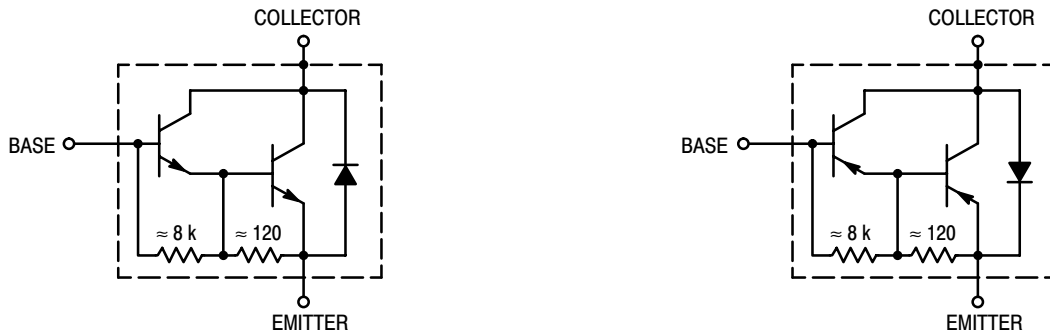
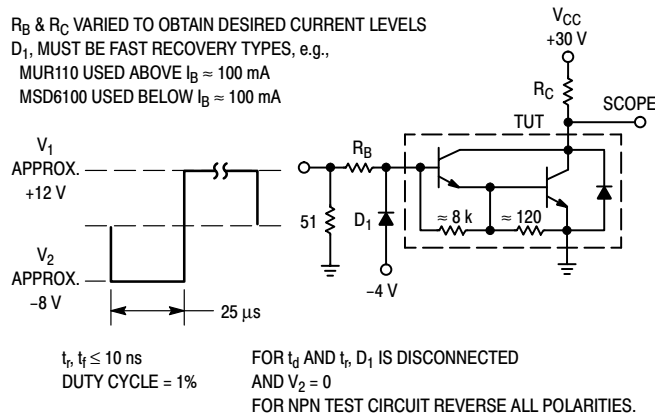


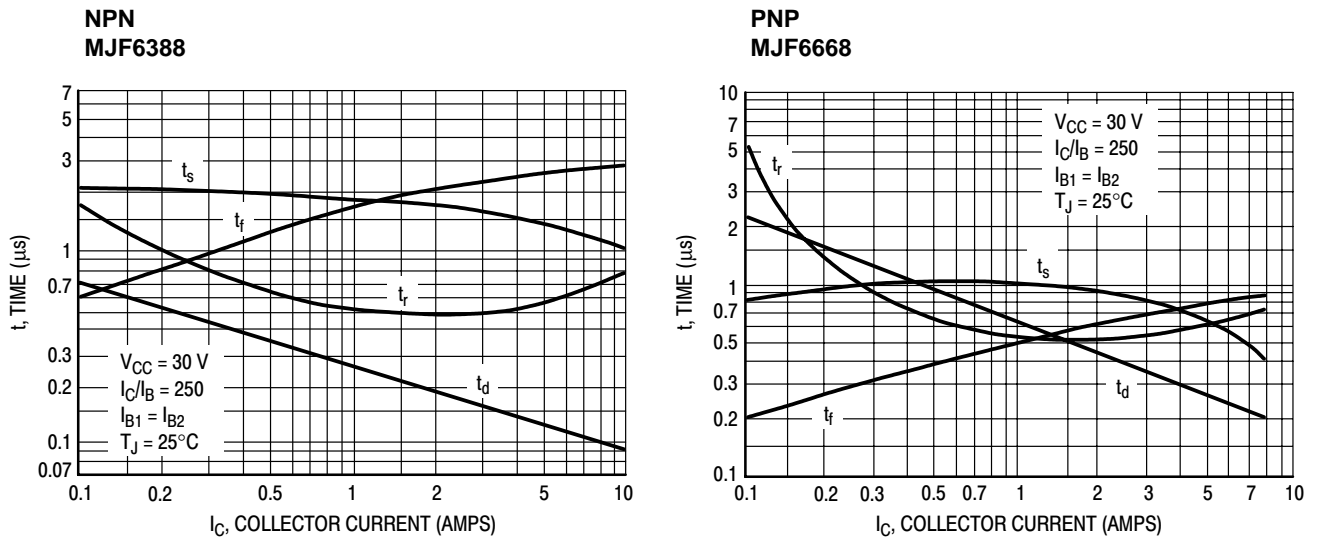
Figure 1. Darlington Schematic

# MJF6388 MJF6668

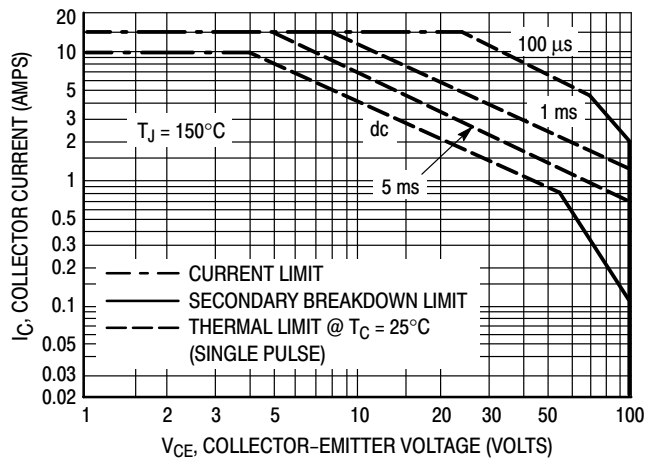
$R_B$  &  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS  
 $D_1$ , MUST BE FAST RECOVERY TYPES, e.g.,  
 MUR110 USED ABOVE  $I_B \approx 100$  mA  
 MSD6100 USED BELOW  $I_B \approx 100$  mA



**Figure 2. Switching Times Test Circuit**



**Figure 3. Typical Switching Times**



**Figure 4. Maximum Forward Bias Safe Operating Area**

# MJF6388 MJF6668

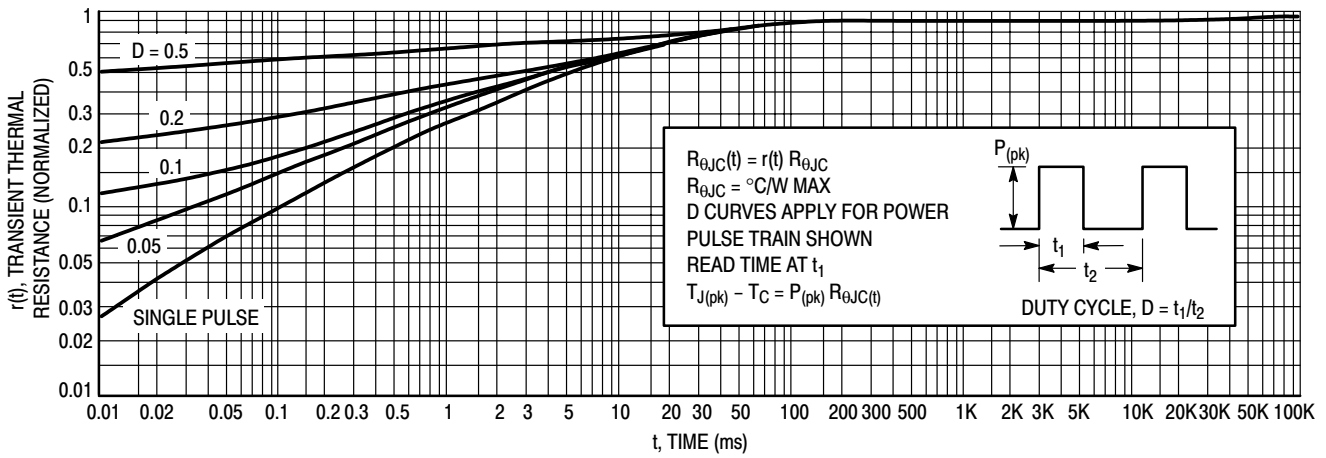


Figure 5. Thermal Response

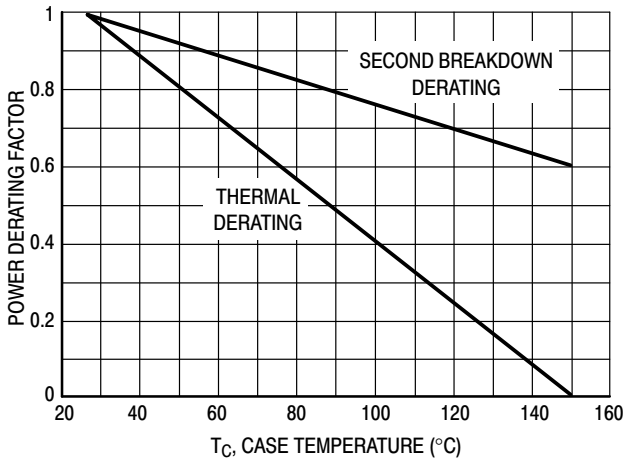


Figure 6. Maximum Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

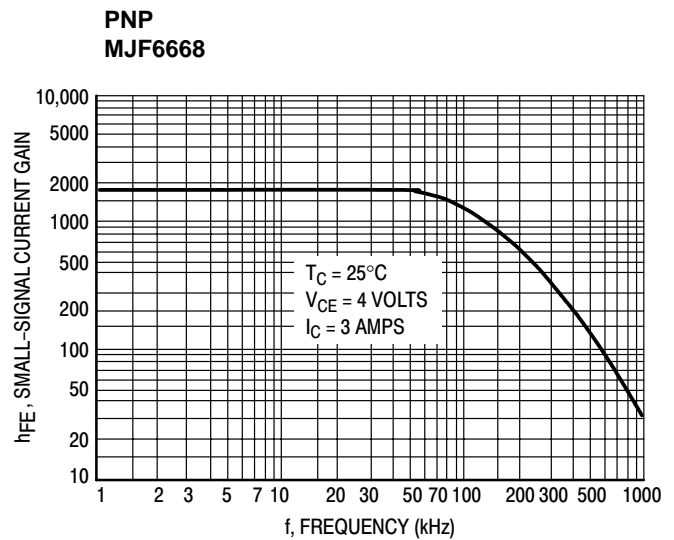
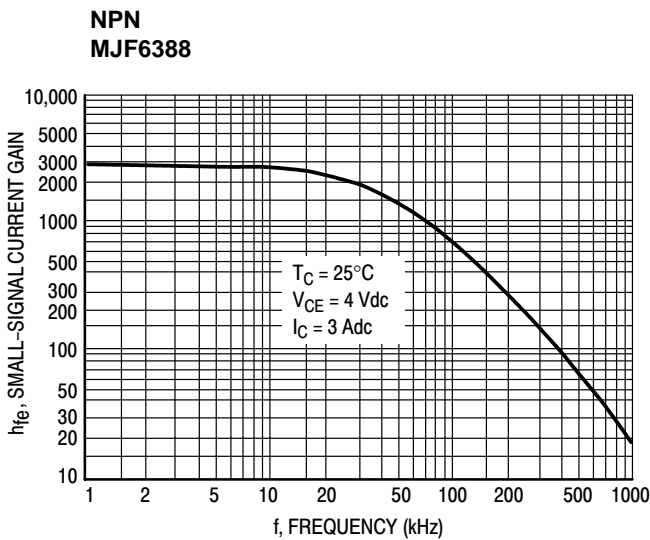


Figure 7. Typical Small-Signal Current Gain

# MJF6388 MJF6668

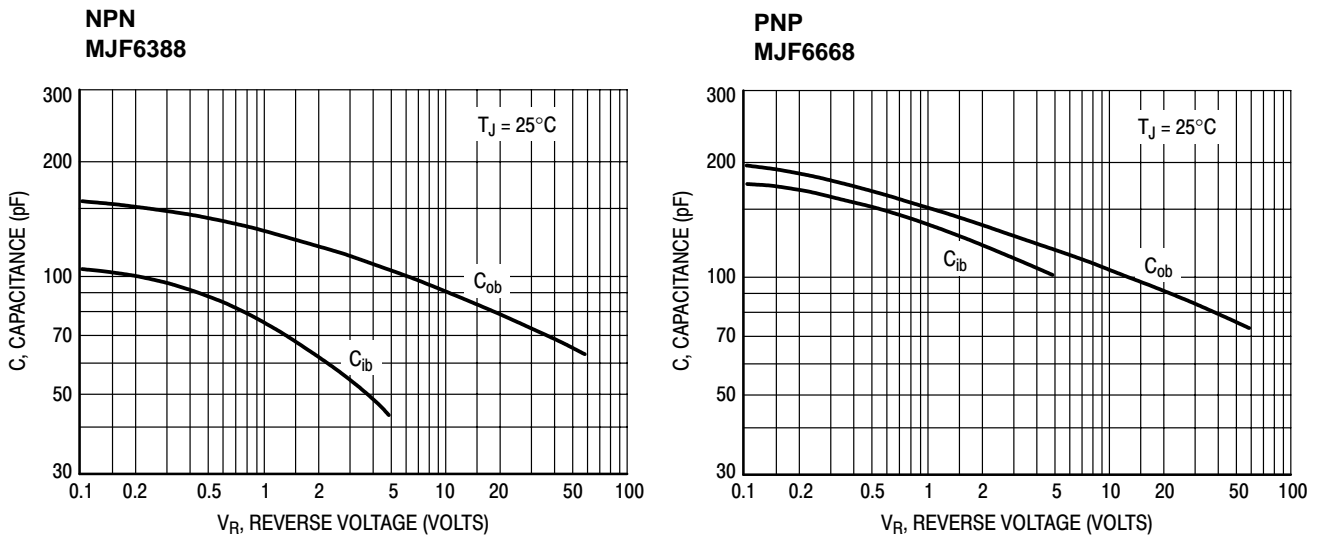


Figure 8. Typical Capacitance

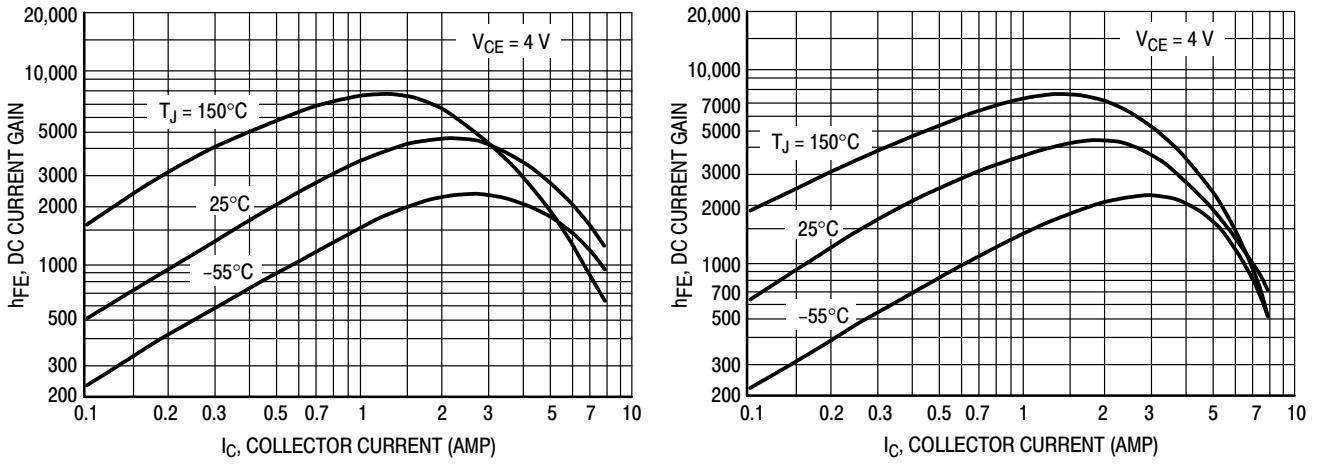


Figure 9. Typical DC Current Gain

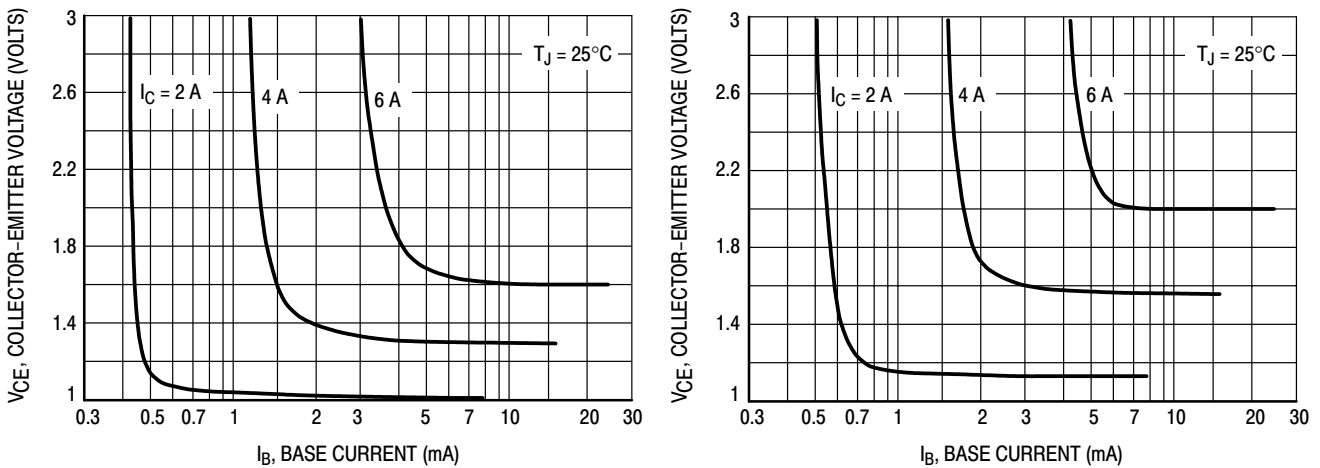
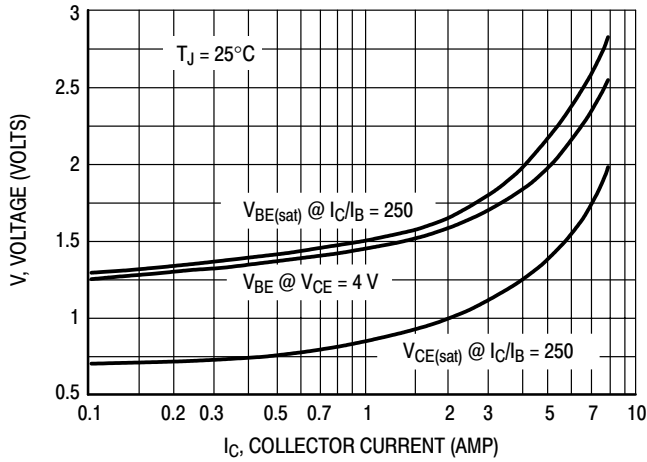


Figure 10. Typical Collector Saturation Region

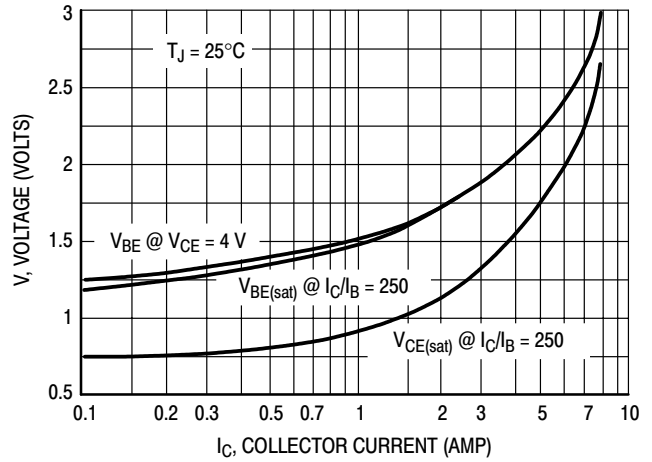


# MJF6388 MJF6668

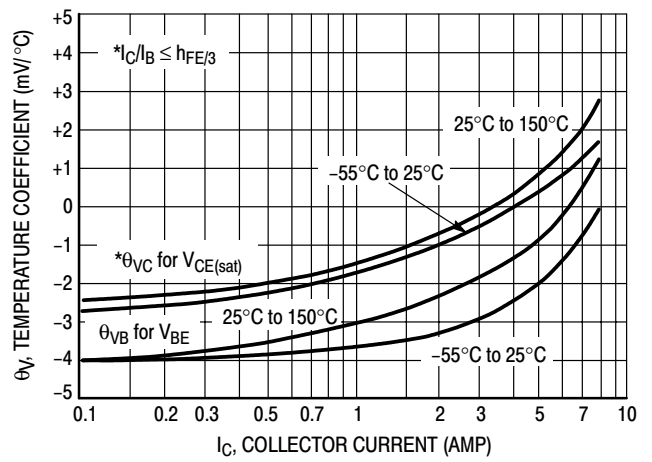
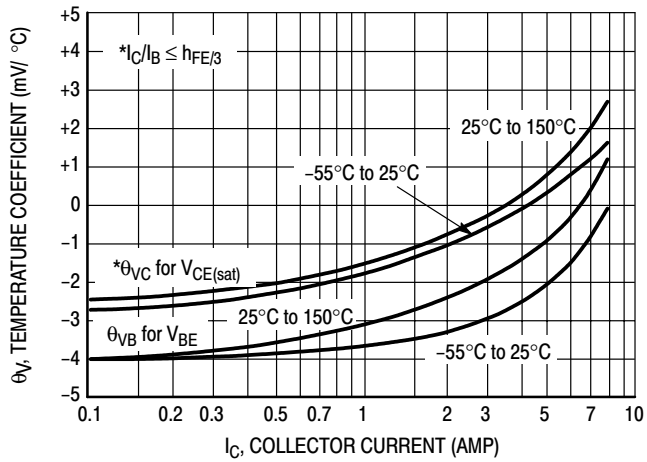
**NPN  
MJF6388**



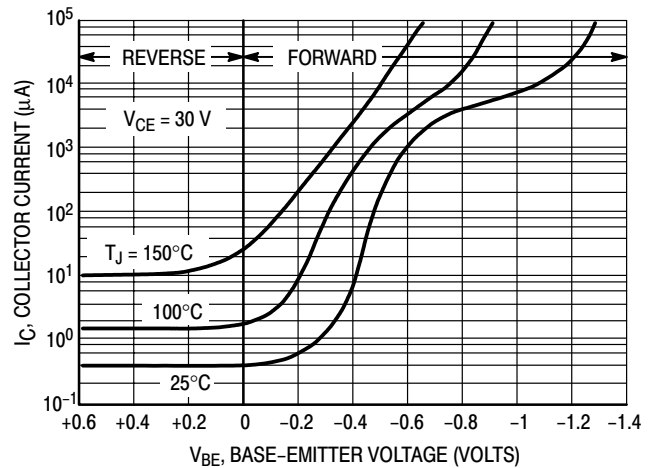
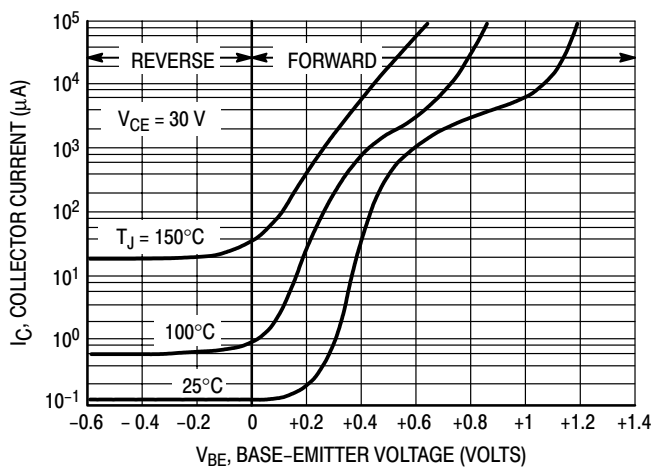
**PNP  
MJF6668**



**Figure 11. Typical "On" Voltages**



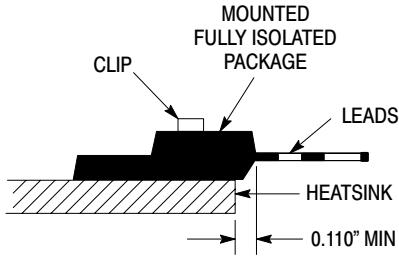
**Figure 12. Typical Temperature Coefficients**



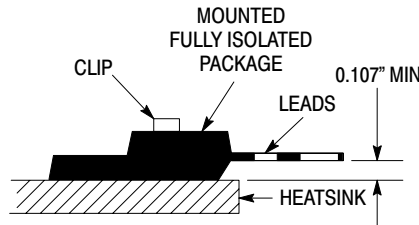
**Figure 13. Typical Collector Cut-Off Region**

# MJF6388 MJF6668

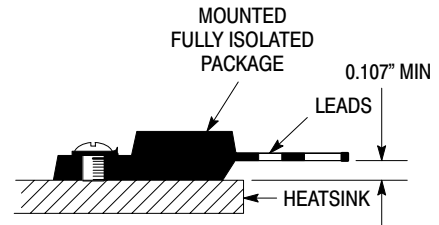
## TEST CONDITIONS FOR ISOLATION TESTS\*



**Figure 14. Clip Mounting Position for Isolation Test Number 1**



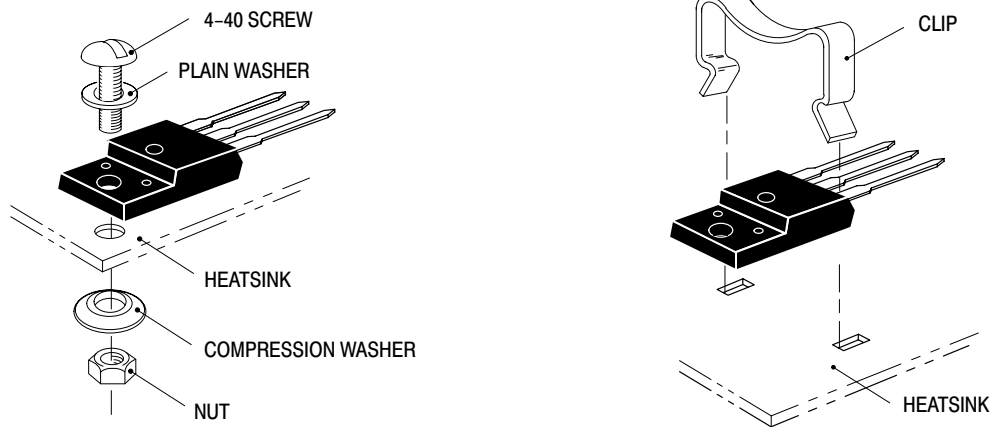
**Figure 15. Clip Mounting Position for Isolation Test Number 2**



**Figure 16. Screw Mounting Position for Isolation Test Number 3**

\*Measurement made between leads and heatsink with all leads shorted together

## MOUNTING INFORMATION



**Figure 17. Typical Mounting Techniques\***

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.

# Complementary Darlington Silicon Power Transistors

... designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High DC Current Gain @ 10 Adc —  
 $h_{FE} = 400$  Min (All Types)
- Collector–Emitter Sustaining Voltage  
 $V_{CEO(sus)} = 150$  Vdc (Min) — MJH11018, 17  
 $= 200$  Vdc (Min) — MJH11020, 19  
 $= 250$  Vdc (Min) — MJH11022, 21
- Low Collector–Emitter Saturation Voltage  
 $V_{CE(sat)} = 1.2$  V (Typ) @  $I_C = 5.0$  A  
 $= 1.8$  V (Typ) @  $I_C = 10$  A
- Monolithic Construction

## MAXIMUM RATINGS

Rating	Symbol	MJH			Unit
		11018 11017	11020 11019	11022 11021	
Collector–Emitter Voltage	$V_{CEO}$	150	200	250	Vdc
Collector–Base Voltage	$V_{CB}$	150	200	250	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous — Peak (1)	$I_C$	15 30			Adc
Base Current	$I_B$	0.5			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	150 1.2			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150			$^\circ\text{C}$

## THERMAL CHARACTERISTICS

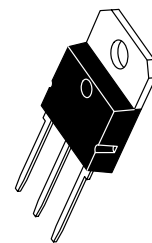
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.83	$^\circ\text{C}/\text{W}$

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle  $\leq 10\%$ .

**PNP**  
**MJH11017\***  
**MJH11019\***  
**MJH11021\***  
**NPN**  
**MJH11018\***  
**MJH11020\***  
**MJH11022\***

\*ON Semiconductor Preferred Device

**15 AMPERE  
 DARLINGTON  
 COMPLEMENTARY SILICON  
 POWER TRANSISTORS  
 150, 200, 250 VOLTS  
 150 WATTS**



CASE 340D–02

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

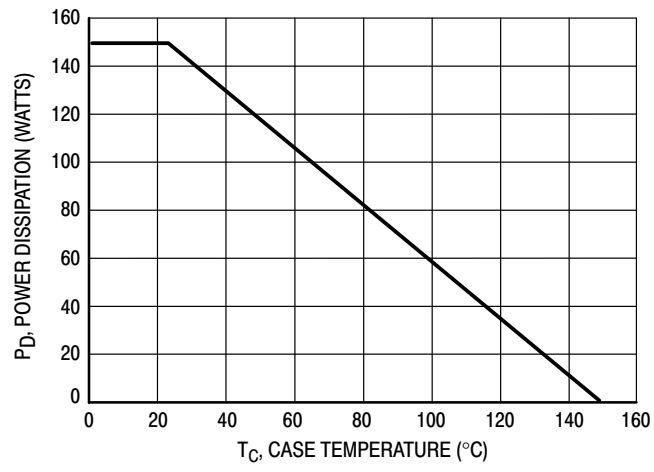


Figure 1. Power Derating

# MJH11017 MJH11019 MJH11021 MJH11018 MJH11020 MJH11022

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (1) (I <sub>C</sub> = 0.1 Adc, I <sub>B</sub> = 0)	MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	V <sub>CEO(sus)</sub>	150 200 250	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 75 Vdc, I <sub>B</sub> = 0) (V <sub>CE</sub> = 100 Vdc, I <sub>B</sub> = 0) (V <sub>CE</sub> = 125 Vdc, I <sub>B</sub> = 0)	MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	I <sub>CEO</sub>	— — —	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>J</sub> = 150°C)		I <sub>CEV</sub>	— —	0.5 5.0	mAdc
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc I <sub>C</sub> = 0)		I <sub>EBO</sub>	—	2.0	mAdc

### ON CHARACTERISTICS (1)

DC Current Gain (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 5.0 Vdc) (I <sub>C</sub> = 15 Adc, V <sub>CE</sub> = 5.0 Vdc)		h <sub>FE</sub>	400 100	15,000 —	—
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 10 Adc, I <sub>B</sub> = 100 mA) (I <sub>C</sub> = 15 Adc, I <sub>B</sub> = 150 mA)		V <sub>CE(sat)</sub>	— —	2.5 4.0	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 10 A, V <sub>CE</sub> = 5.0 Vdc)		V <sub>BE(on)</sub>	—	2.8	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 15 Adc, I <sub>B</sub> = 150 mA)		V <sub>BE(sat)</sub>	—	3.8	Vdc

### DYNAMIC CHARACTERISTICS

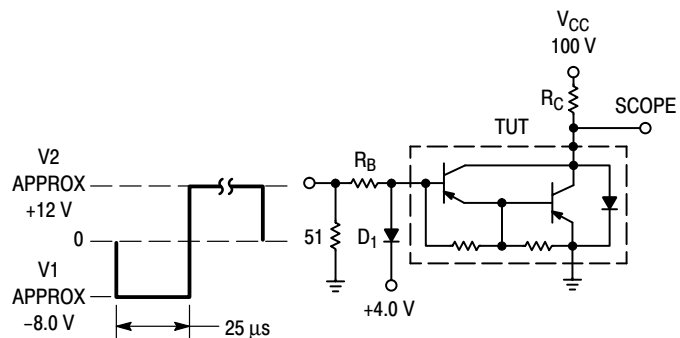
Current–Gain Bandwidth Product (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 MHz)		f <sub>T</sub>	3.0	—	—
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	MJH11018, MJH11020, MJH11022 MJH11017, MJH11019, MJH11021	C <sub>ob</sub>	— —	400 600	pF
Small–Signal Current Gain (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 kHz)		h <sub>fe</sub>	75	—	—

### SWITCHING CHARACTERISTICS

Characteristic	Symbol	Typical		Unit
		NPN	PNP	
Delay Time	t <sub>d</sub>	150	75	ns
Rise Time	t <sub>r</sub>	1.2	0.5	μs
Storage Time	t <sub>s</sub>	4.4	2.7	μs
Fall Time	t <sub>f</sub>	2.5	2.5	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

R<sub>B</sub> & R<sub>C</sub> varied to obtain desired current levels  
D<sub>1</sub>, must be fast recovery types, e.g.:  
1N5825 used above I<sub>B</sub> ≈ 100 mA  
MSD6100 used below I<sub>B</sub> ≈ 100 mA



t<sub>r</sub>, t<sub>f</sub> ≤ 10 ns  
Duty Cycle = 1.0%

For t<sub>d</sub> and t<sub>r</sub>, D<sub>1</sub> is disconnected and V<sub>2</sub> = 0  
For NPN test circuit, reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

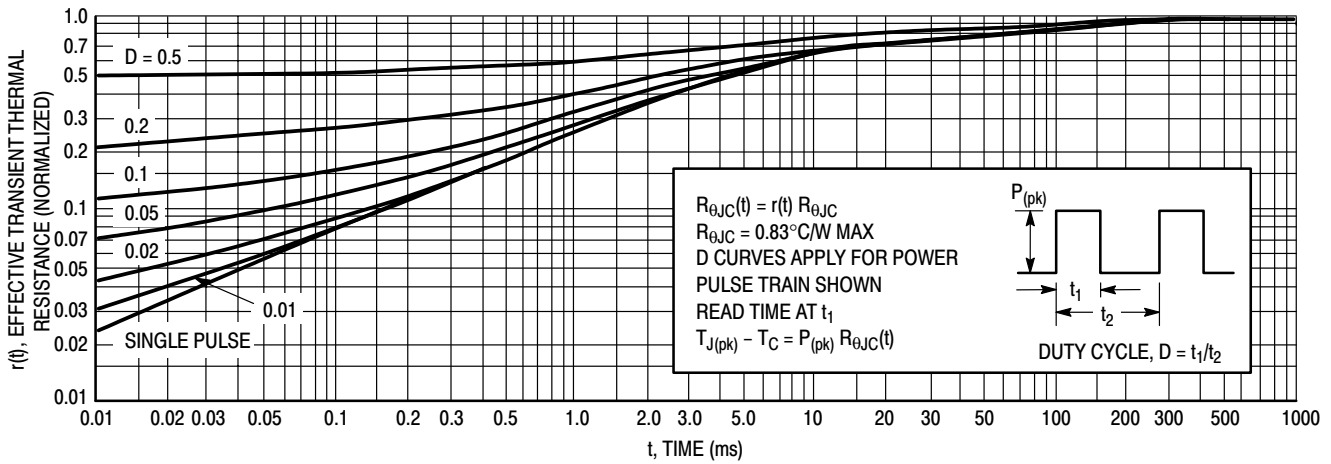


Figure 3. Thermal Response

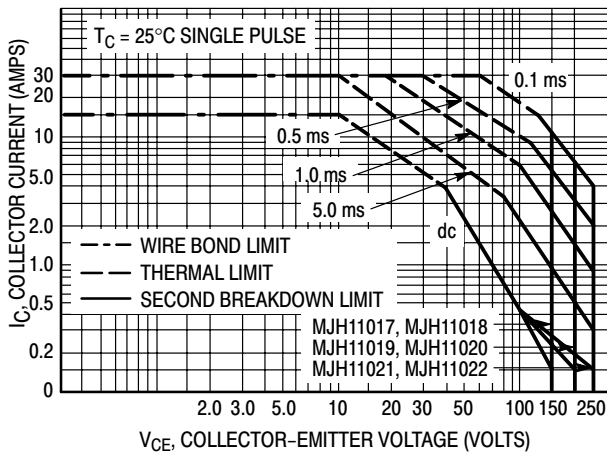


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

**FORWARD BIAS**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

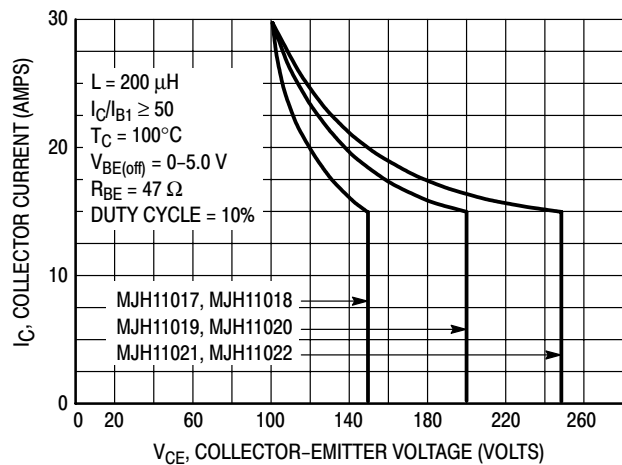


Figure 5. Maximum Rated Reverse Bias Safe Operating Area (RBSOA)

**REVERSE BIAS**

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives RBSOA characteristics.

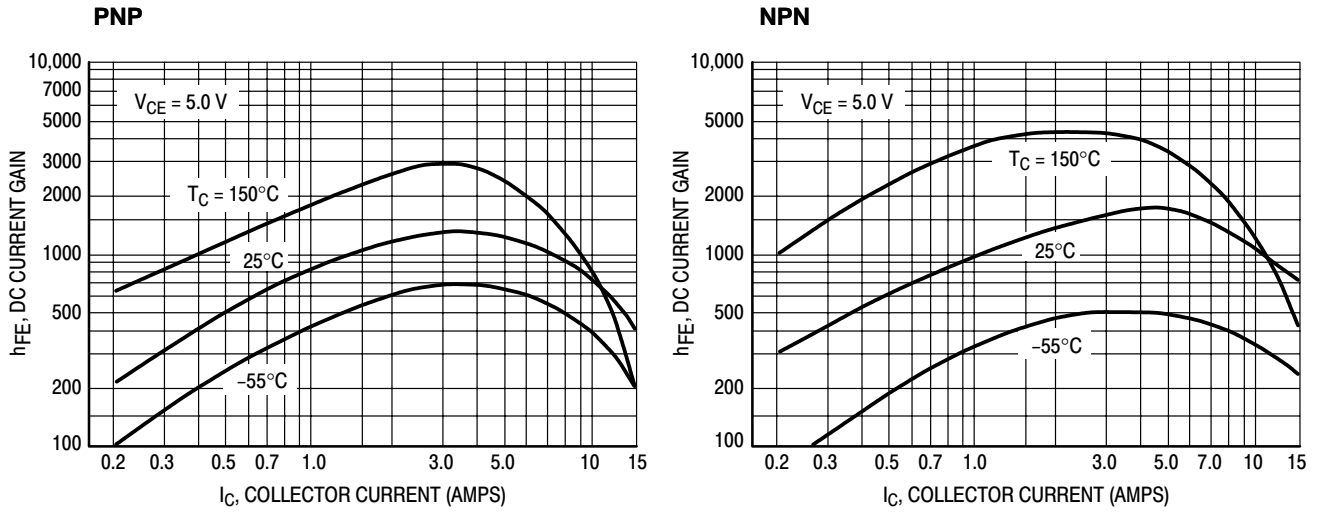


Figure 6. DC Current Gain

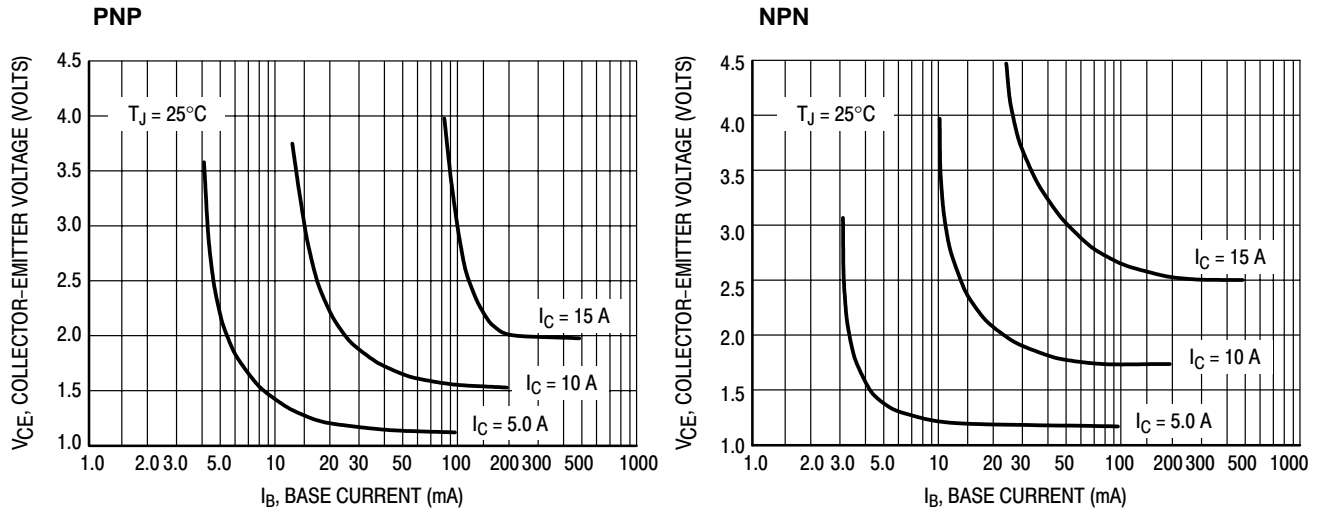


Figure 7. Collector Saturation Region

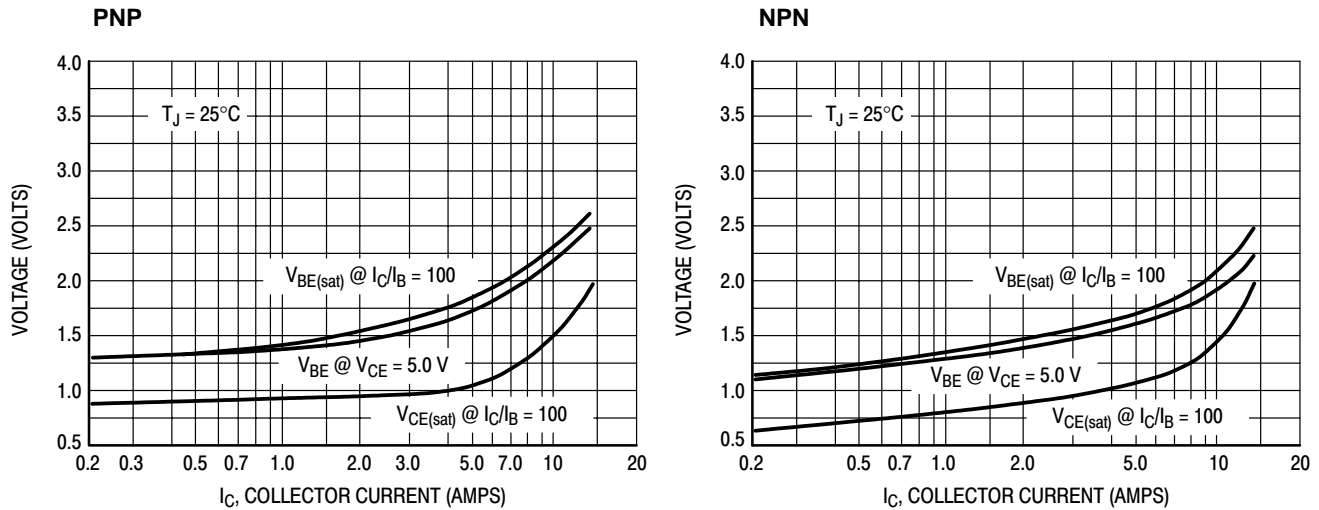
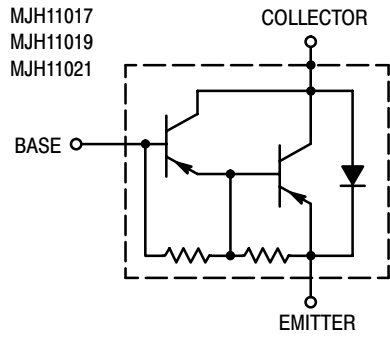


Figure 8. "On" Voltages

PNP



NPN

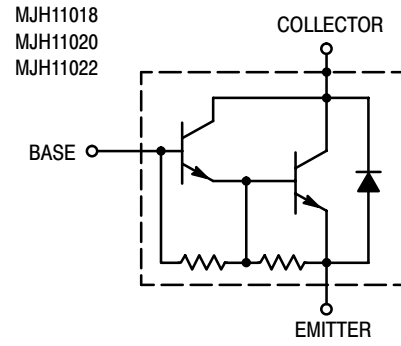


Figure 9. Darlington Schematic



# Darlington Complementary Silicon Power Transistors

... designed for general-purpose amplifier and low-speed switching motor control applications.

- Similar to the Popular NPN 2N6284 and the PNP 2N6287
- Rugged RBSOA Characteristics
- Monolithic Construction with Built-in Collector-Emitter Diode

## MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous Peak	$I_C$	20 40	Adc
Base Current	$I_B$	0.5	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	160 1.28	Watts $\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

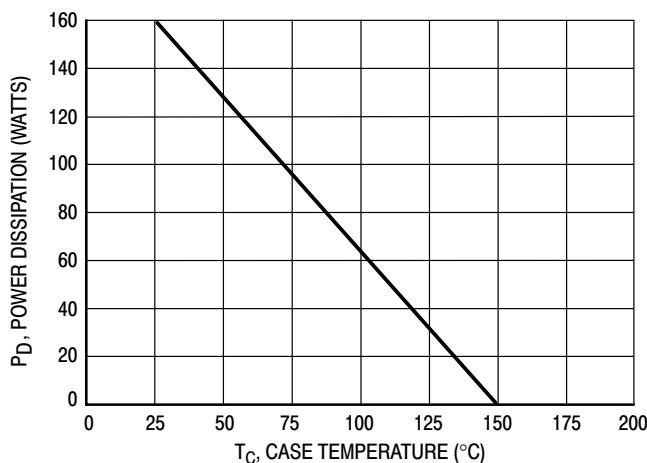
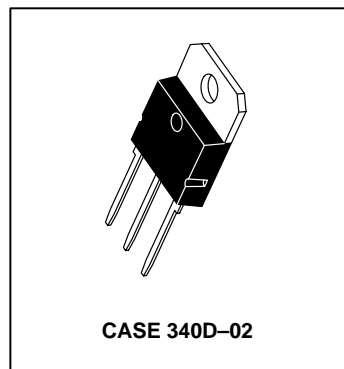
## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.78	$^\circ\text{C}/\text{W}$

**NPN  
MJH6284  
PNP  
MJH6287**

ON Semiconductor Preferred Devices

**DARLINGTON  
20 AMPERE  
COMPLEMENTARY SILICON  
POWER TRANSISTORS  
100 VOLTS  
160 WATTS**



**Figure 1. Power Derating**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJH6284 MJH6287

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 0.1 Adc, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	100	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 50 Vdc, I <sub>B</sub> = 0)	I <sub>CEO</sub>	—	1.0	mAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 150°C)	I <sub>CEX</sub>	—	0.5 5.0	mAdc
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	2.0	mAdc

## ON CHARACTERISTICS (1)

DC Current Gain (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc) (I <sub>C</sub> = 20 Adc, V <sub>CE</sub> = 3.0 Vdc)	h <sub>FE</sub>	750 100	18,000 —	—
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 10 Adc, I <sub>B</sub> = 40 mAdc) (I <sub>C</sub> = 20 Adc, I <sub>B</sub> = 200 mAdc)	V <sub>CE(sat)</sub>	—	2.0 3.0	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc)	V <sub>BE(on)</sub>	—	2.8	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 20 Adc, I <sub>B</sub> = 200 mAdc)	V <sub>BE(sat)</sub>	—	4.0	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain Bandwidth Product (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 MHz)	f <sub>T</sub>	4.0	—	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	C <sub>ob</sub>	—	400 600	pF
				MJH6284 MJH6287
Small–Signal Current Gain (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 kHz)	h <sub>fe</sub>	300	—	—

## SWITCHING CHARACTERISTICS

Resistive Load		Symbol	Typical		Unit
			NPN	PNP	
Delay Time	V <sub>CC</sub> = 30 Vdc, I <sub>C</sub> = 10 Adc I <sub>B1</sub> = I <sub>B2</sub> = 100 mA Duty Cycle = 1.0%	t <sub>d</sub>	0.1	0.1	μs
Rise Time		t <sub>r</sub>	0.3	0.3	
Storage Time		t <sub>s</sub>	1.0	1.0	
Fall Time		t <sub>f</sub>	3.5	2.0	

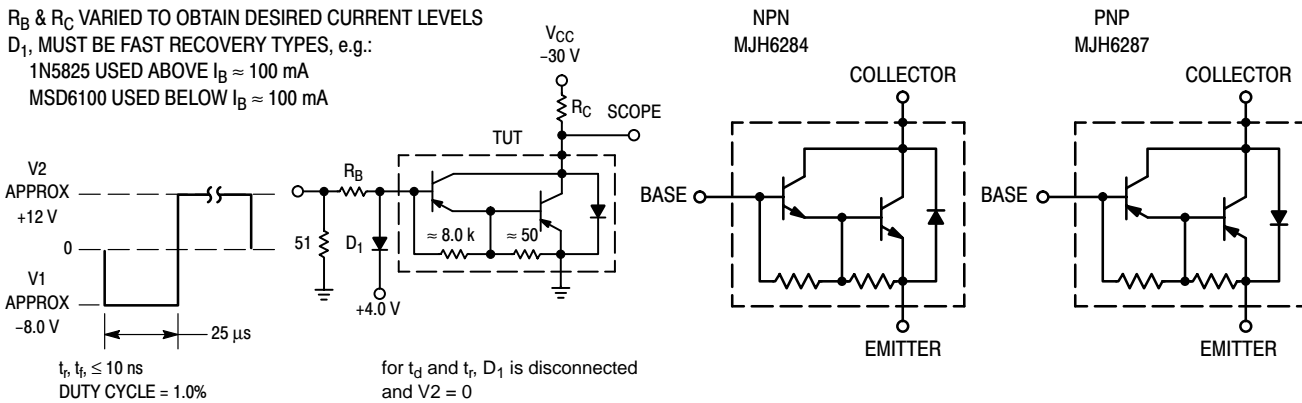
(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

R<sub>B</sub> & R<sub>C</sub> VARIED TO OBTAIN DESIRED CURRENT LEVELS

D<sub>1</sub>, MUST BE FAST RECOVERY TYPES, e.g.:

1N5825 USED ABOVE I<sub>B</sub> ≈ 100 mA

MSD6100 USED BELOW I<sub>B</sub> ≈ 100 mA



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

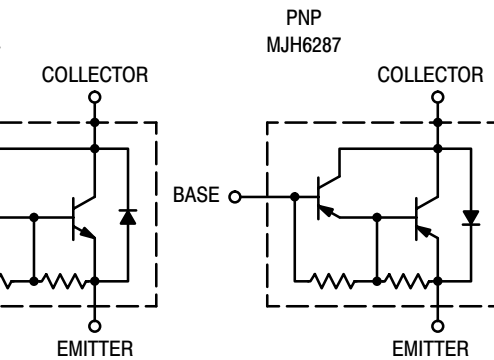


Figure 3. Darlington Schematic

# MJH6284 MJH6287

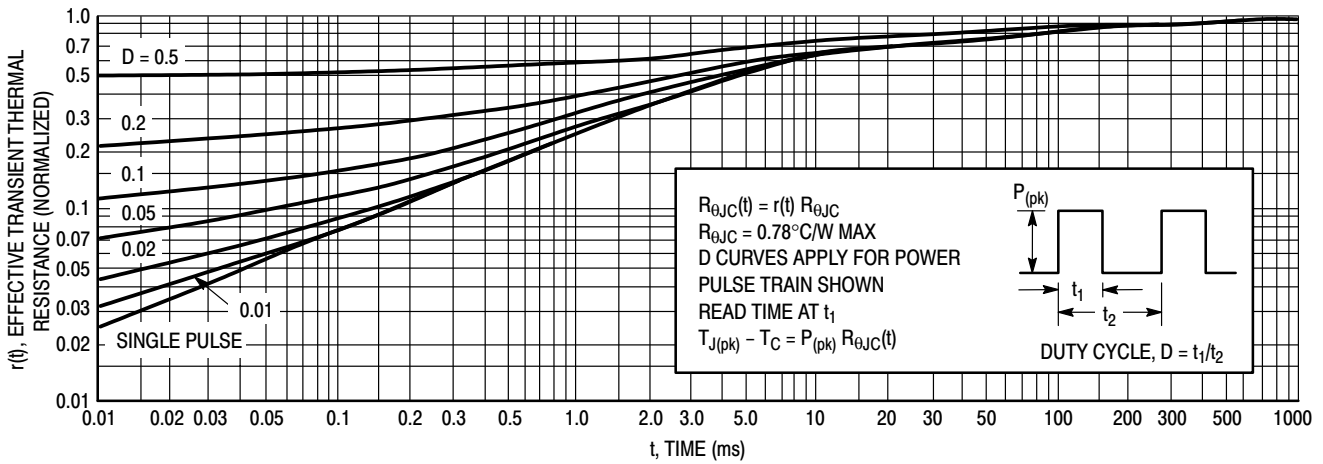


Figure 4. Thermal Response

## FBSOA, FORWARD BIAS SAFE OPERATING AREA

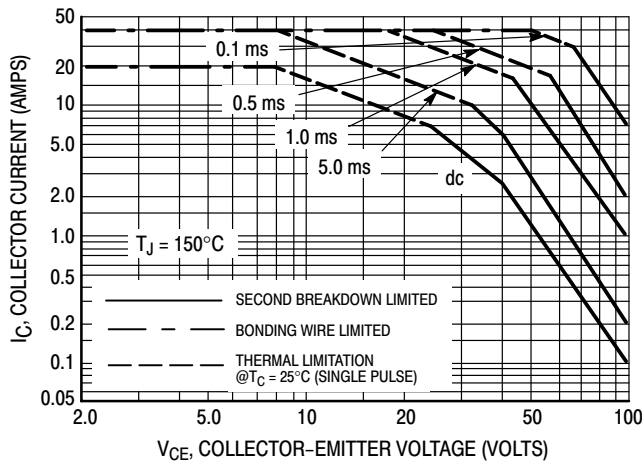


Figure 5. MJH6284, MJH6287

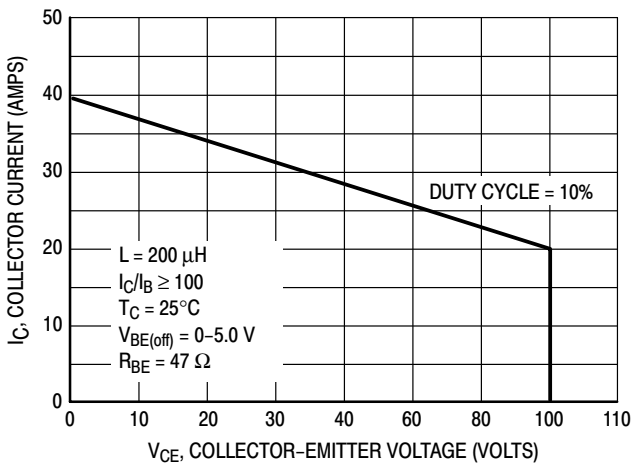


Figure 6. Maximum RBSOA, Reverse Bias Safe Operating Area

## FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# MJH6284 MJH6287

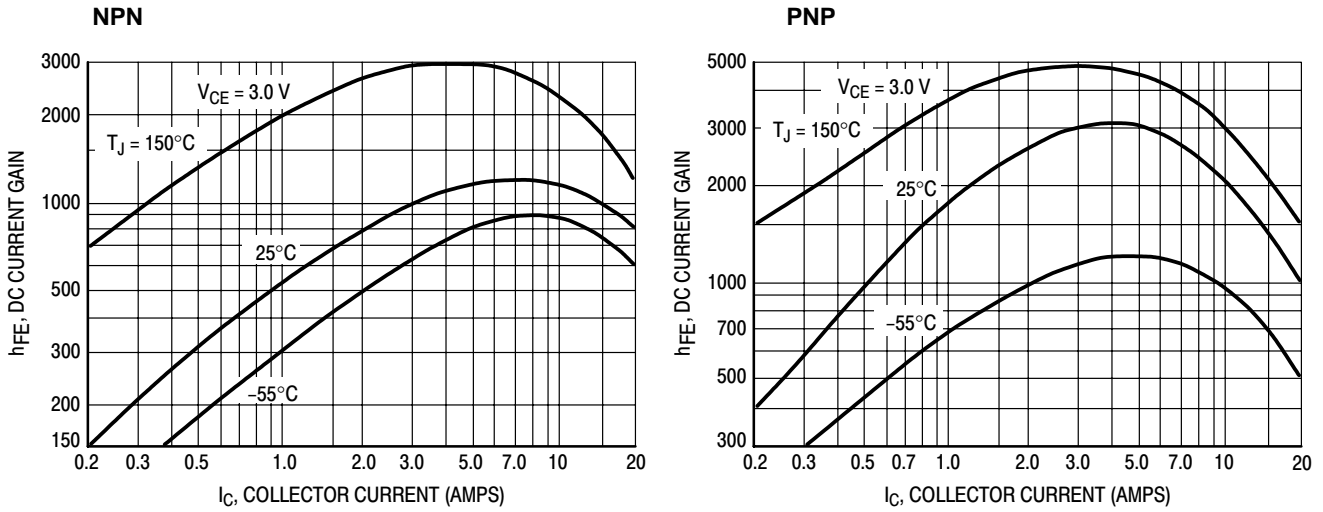


Figure 7. DC Current Gain

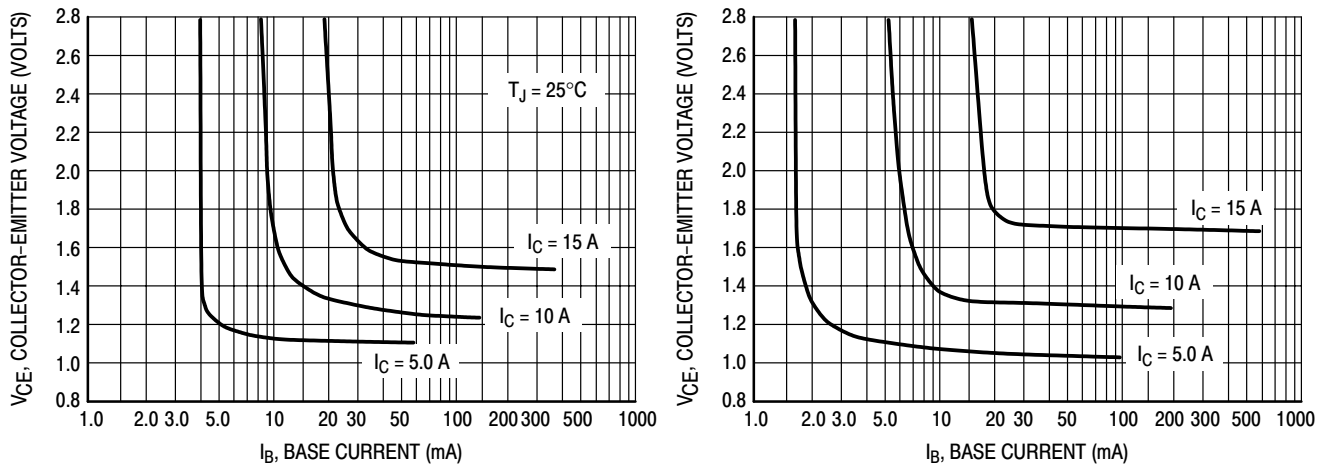


Figure 8. Collector Saturation Region

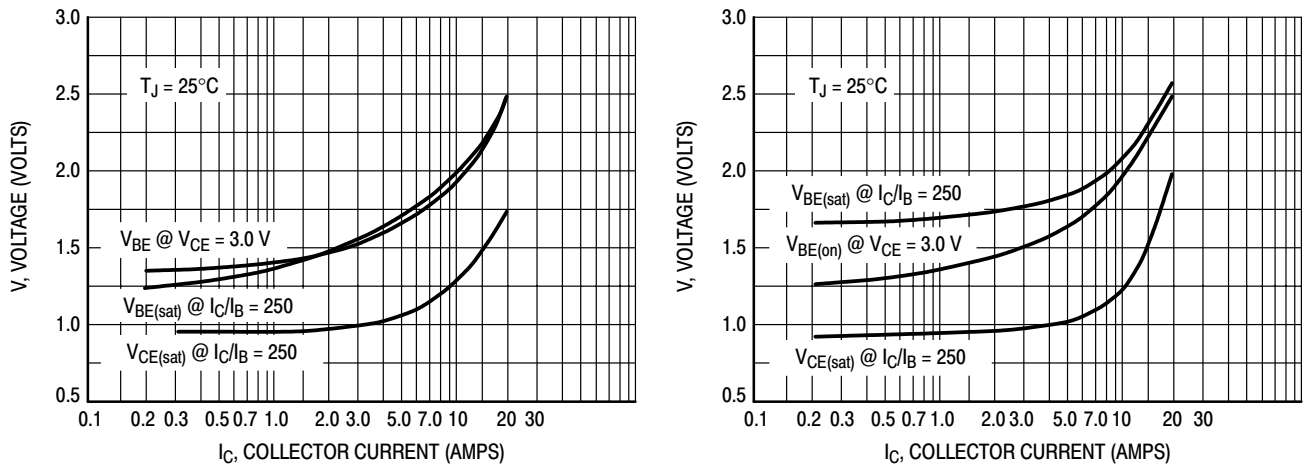


Figure 9. "On" Voltages



# Silicon Power Transistors

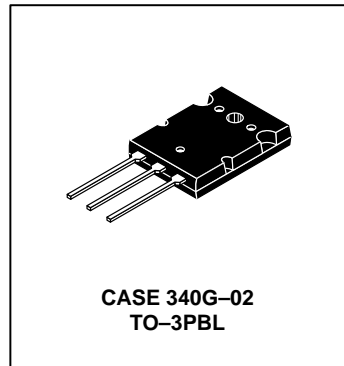
The MJL21193 and MJL21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –  
 $h_{FE} = 25 \text{ Min @ } I_C$   
 $= 8 \text{ Adc}$
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second

**PNP**  
**MJL21193\***  
**NPN**  
**MJL21194\***

\*ON Semiconductor Preferred Device

**16 AMPERE**  
**COMPLEMENTARY**  
**SILICON POWER**  
**TRANSISTORS**  
**250 VOLTS**  
**200 WATTS**



## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	Vdc
Collector–Base Voltage	$V_{CBO}$	400	Vdc
Emitter–Base Voltage	$V_{EBO}$	5	Vdc
Collector–Emitter Voltage – 1.5 V	$V_{CEX}$	400	Vdc
Collector Current — Continuous Peak (1)	$I_C$	16 30	Adc
Base Current – Continuous	$I_B$	5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	200 1.43	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J$ , $T_{stg}$	–65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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## OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100 \text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = 200 \text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	—	100	$\mu\text{Adc}$

(1) Pulse Test: Pulse Width = 5.0  $\mu\text{s}$ , Duty Cycle  $\leq 10\%$ .

(continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJL21193 MJL21194

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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### OFF CHARACTERISTICS

Emitter Cutoff Current ( $V_{CE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 250\text{ Vdc}$ , $V_{BE(\text{off})} = 1.5\text{ Vdc}$ )	$I_{CEX}$	—	—	100	$\mu\text{Adc}$

### SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 50\text{ Vdc}$ , $t = 1\text{ s}$ (non-repetitive)) ( $V_{CE} = 80\text{ Vdc}$ , $t = 1\text{ s}$ (non-repetitive))	$I_{S/b}$	4.0 2.25	— —	— —	A dc
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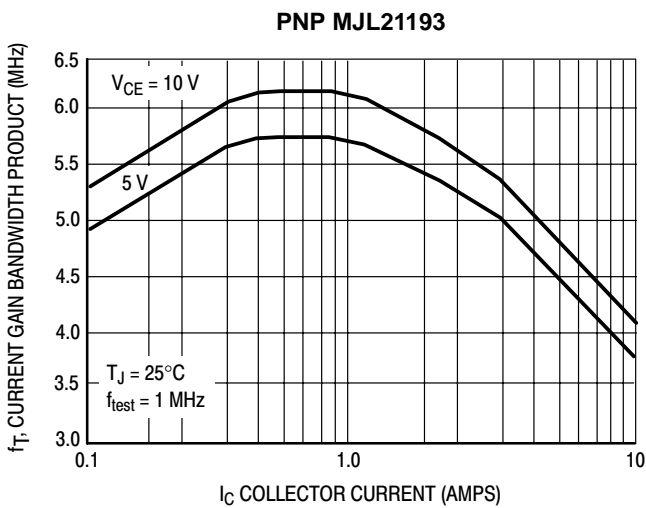
### ON CHARACTERISTICS

DC Current Gain ( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 5\text{ Adc}$ )	$h_{FE}$	25 8	— —	75 —	
Base-Emitter On Voltage ( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$V_{BE(\text{on})}$	—	—	2.2	V dc
Collector-Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.8\text{ Adc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 3.2\text{ Adc}$ )	$V_{CE(\text{sat})}$	— —	— —	1.4 4	V dc

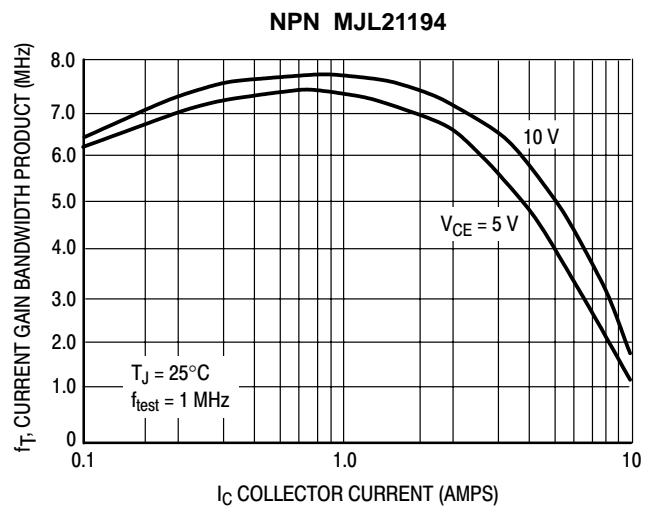
### DYNAMIC CHARACTERISTICS

Total Harmonic Distortion at the Output $V_{RMS} = 28.3\text{ V}$ , $f = 1\text{ kHz}$ , $P_{LOAD} = 100\text{ W}_{RMS}$ (Matched pair $h_{FE} = 50$ @ 5 A/5 V)	$T_{HD}$	—	0.8 0.08	—	%
Current Gain Bandwidth Product ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{\text{test}} = 1\text{ MHz}$ )	$f_T$	4	—	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{\text{test}} = 1\text{ MHz}$ )	$C_{ob}$	—	—	500	pF

(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$



**Figure 1. Typical Current Gain Bandwidth Product**

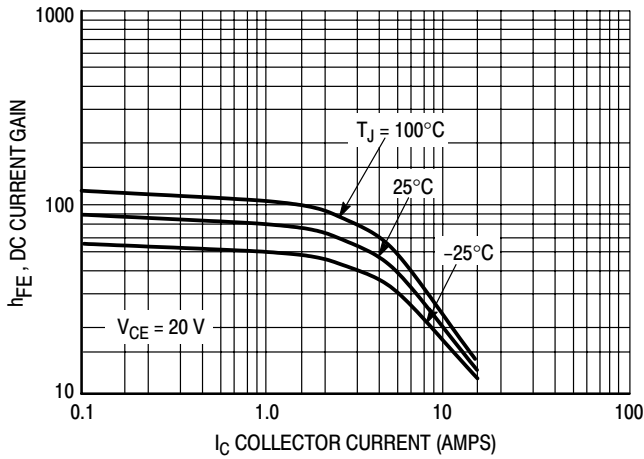


**Figure 2. Typical Current Gain Bandwidth Product**

# MJL21193 MJL21194

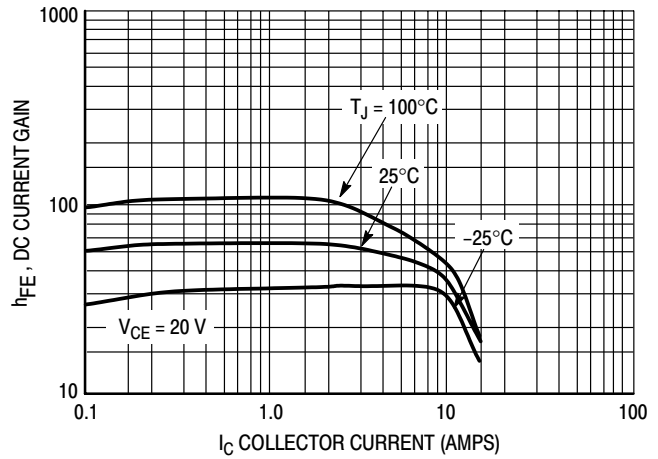
## TYPICAL CHARACTERISTICS

**PNP MJL21193**



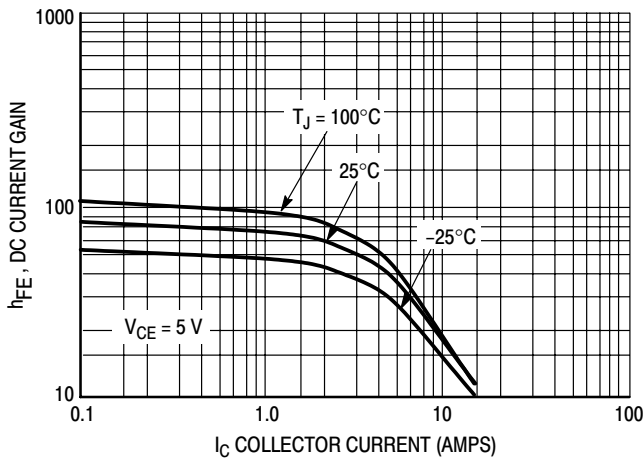
**Figure 3. DC Current Gain,  $V_{CE} = 20\text{ V}$**

**NPN MJL21194**



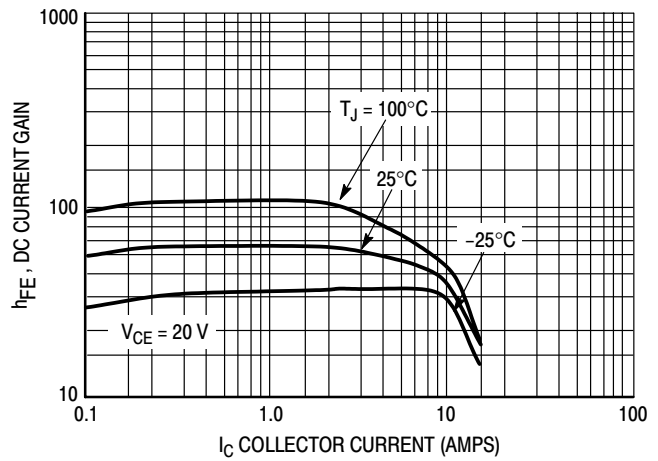
**Figure 4. DC Current Gain,  $V_{CE} = 20\text{ V}$**

**PNP MJL21193**



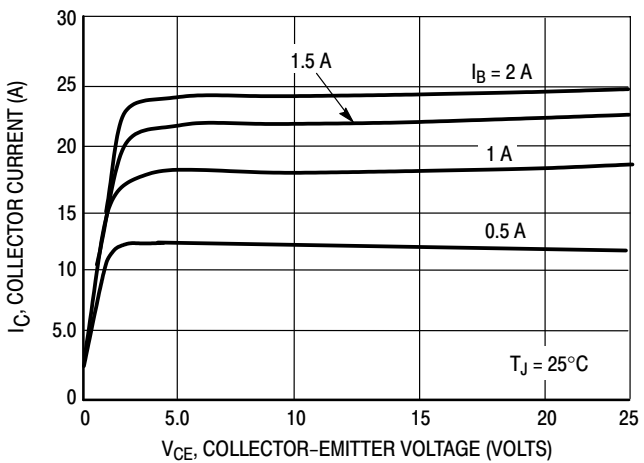
**Figure 5. DC Current Gain,  $V_{CE} = 5\text{ V}$**

**NPN MJL21194**

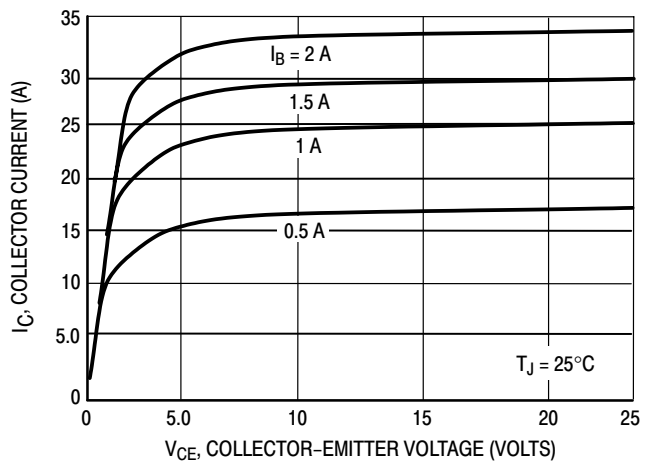


**Figure 6. DC Current Gain,  $V_{CE} = 5\text{ V}$**

**PNP MJL21193**



**NPN MJL21194**



TYPICAL CHARACTERISTICS

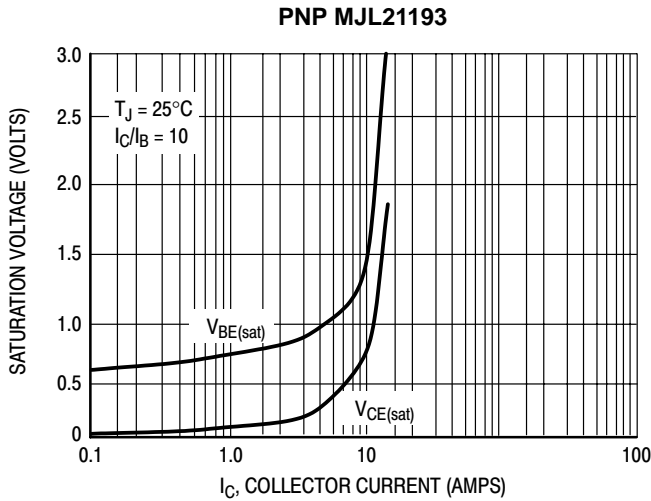


Figure 9. Typical Saturation Voltages

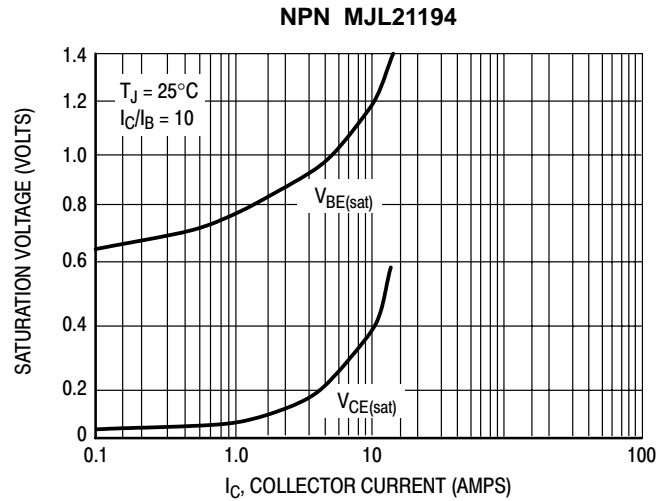


Figure 10. Typical Saturation Voltages

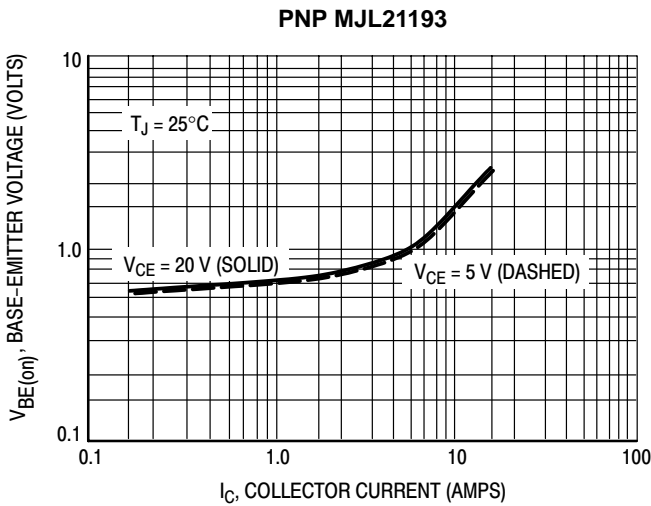


Figure 11. Typical Base-Emitter Voltage

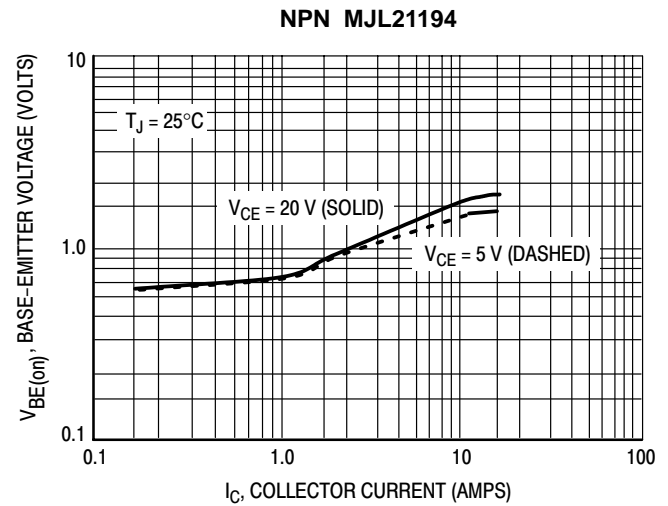


Figure 12. Typical Base-Emitter Voltage

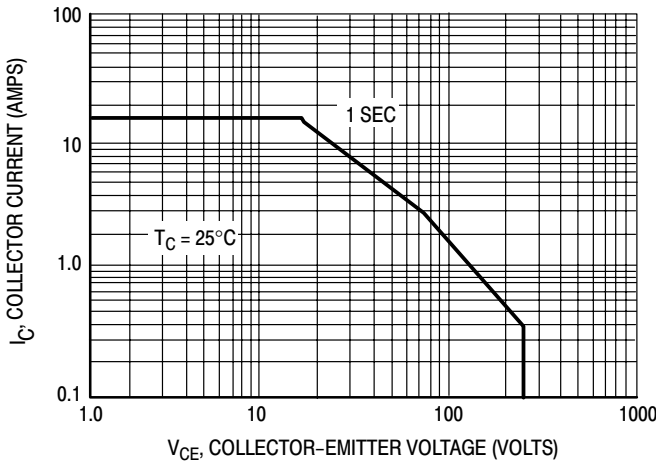


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.



# MJL21193 MJL21194

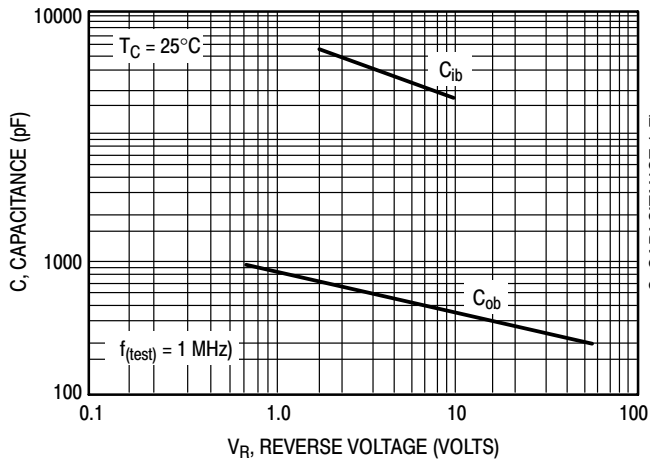


Figure 14. MJL21193 Typical Capacitance

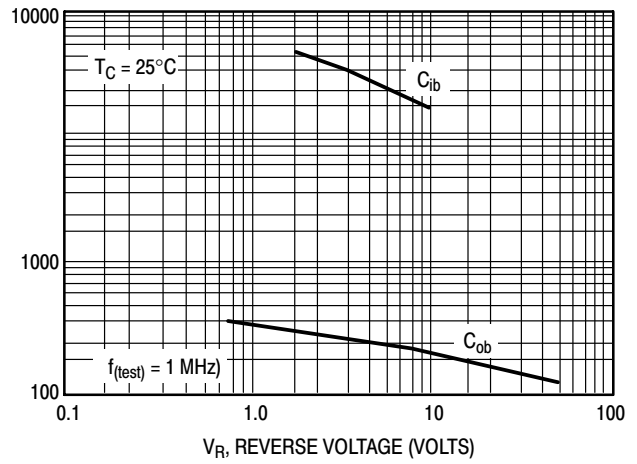


Figure 15. MJL21194 Typical Capacitance

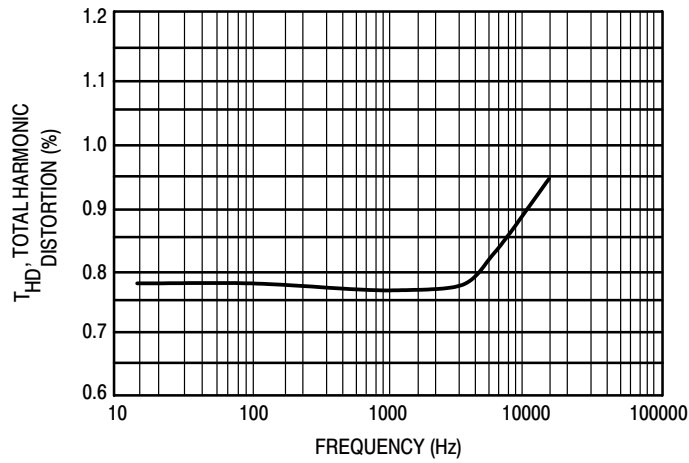


Figure 16. Typical Total Harmonic Distortion

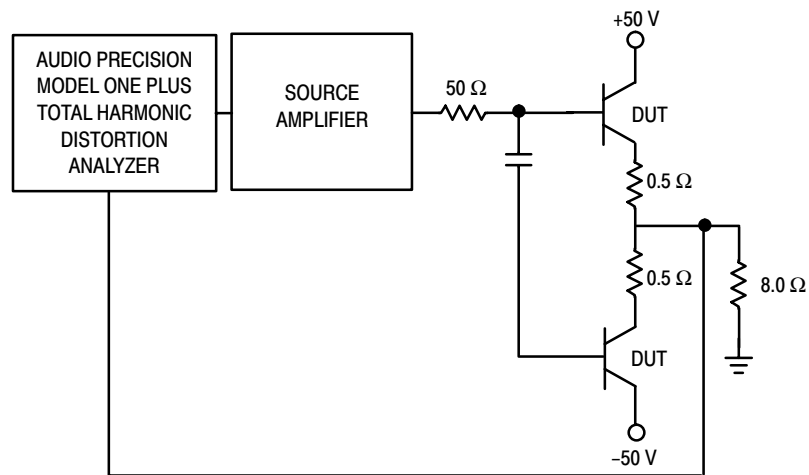


Figure 17. Total Harmonic Distortion Test Circuit

## Silicon Power Transistors

The MJL21195 and MJL21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –  $h_{FE} = 25$  Min @  $I_C = 8$  Adc
- Excellent Gain Linearity
- High SOA: 2.50 A, 80 V, 1 Second

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	Vdc
Collector–Base Voltage	$V_{CBO}$	400	Vdc
Emitter–Base Voltage	$V_{EBO}$	5	Vdc
Collector–Emitter Voltage – 1.5 V	$V_{CEX}$	400	Vdc
Collector Current — Continuous Peak <sup>(1)</sup>	$I_C$	16 30	Adc
Base Current – Continuous	$I_B$	5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	200 1.43	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

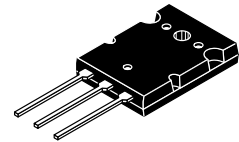
### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$

PNP  
**MJL21195\***  
NPN  
**MJL21196\***

\*ON Semiconductor Preferred Device

16 AMPERE  
COMPLEMENTARY  
SILICON POWER  
TRANSISTORS  
250 VOLTS  
200 WATTS



CASE 340G-02  
TO-3PBL

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MJL21195 MJL21196

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 100 mA <sub>dc</sub> , I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	250	—	—	V <sub>dc</sub>
Collector Cutoff Current (V <sub>CE</sub> = 200 V <sub>dc</sub> , I <sub>B</sub> = 0)	I <sub>CEO</sub>	—	—	100	μA <sub>dc</sub>

(1) Pulse Test: Pulse Width = 5.0 μs, Duty Cycle ≤10%.

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Emitter Cutoff Current (V <sub>CE</sub> = 5 V <sub>dc</sub> , I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	—	100	μA <sub>dc</sub>
Collector Cutoff Current (V <sub>CE</sub> = 250 V <sub>dc</sub> , V <sub>BE(off)</sub> = 1.5 V <sub>dc</sub> )	I <sub>CEX</sub>	—	—	100	μA <sub>dc</sub>

## SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased (V <sub>CE</sub> = 50 V <sub>dc</sub> , t = 1 s (non-repetitive) (V <sub>CE</sub> = 80 V <sub>dc</sub> , t = 1 s (non-repetitive)	I <sub>S/b</sub>	4.0 2.25	— —	— —	A <sub>dc</sub>
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## ON CHARACTERISTICS

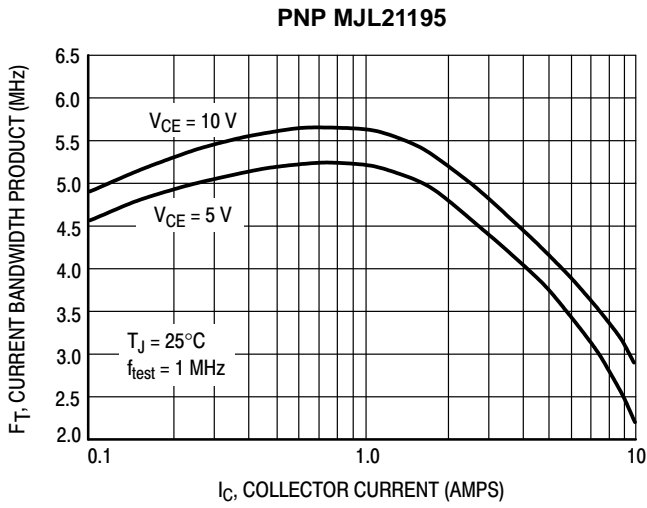
DC Current Gain (I <sub>C</sub> = 8 A <sub>dc</sub> , V <sub>CE</sub> = 5 V <sub>dc</sub> ) (I <sub>C</sub> = 16 A <sub>dc</sub> , I <sub>B</sub> = 5 A <sub>dc</sub> )	h <sub>FE</sub>	25 8	— —	100 —	
Base–Emitter On Voltage (I <sub>C</sub> = 8 A <sub>dc</sub> , V <sub>CE</sub> = 5 V <sub>dc</sub> )	V <sub>BE(on)</sub>	—	—	2.2	V <sub>dc</sub>
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 8 A <sub>dc</sub> , I <sub>B</sub> = 0.8 A <sub>dc</sub> ) (I <sub>C</sub> = 16 A <sub>dc</sub> , I <sub>B</sub> = 3.2 A <sub>dc</sub> )	V <sub>CE(sat)</sub>	— —	— —	1.4 4	V <sub>dc</sub>

## DYNAMIC CHARACTERISTICS

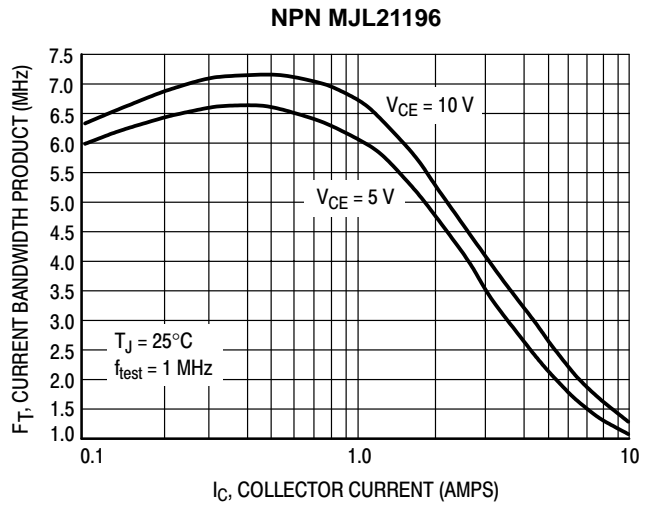
Total Harmonic Distortion at the Output V <sub>RMS</sub> = 28.3 V, f = 1 kHz, P <sub>LOAD</sub> = 100 W <sub>RMS</sub> (Matched pair h <sub>FE</sub> = 50 @ 5 A/5 V)	h <sub>FE</sub> unmatched h <sub>FE</sub> matched	T <sub>HD</sub>	— —	0.8 0.08	— —	%
Current Gain Bandwidth Product (I <sub>C</sub> = 1 A <sub>dc</sub> , V <sub>CE</sub> = 10 V <sub>dc</sub> , f <sub>test</sub> = 1 MHz)		f <sub>T</sub>	4	—	—	MHz
Output Capacitance (V <sub>CB</sub> = 10 V <sub>dc</sub> , I <sub>E</sub> = 0, f <sub>test</sub> = 1 MHz)		C <sub>ob</sub>	—	—	500	pF

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

# MJL21195 MJL21196



**Figure 1. Typical Current Gain Bandwidth Product**



**Figure 2. Typical Current Gain Bandwidth Product**

TYPICAL CHARACTERISTICS

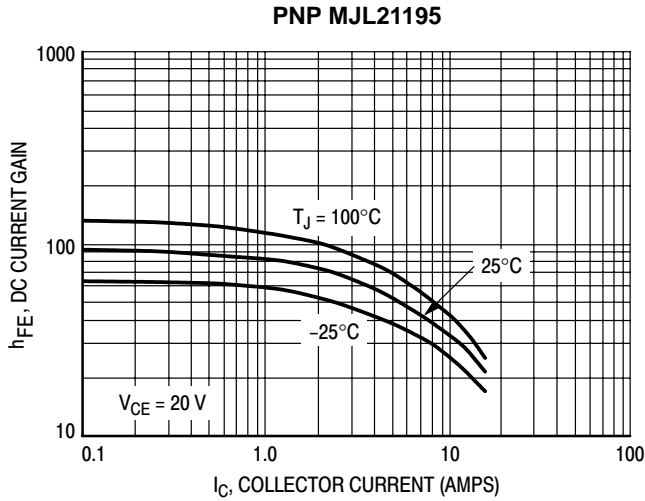


Figure 3. DC Current Gain,  $V_{CE} = 20\text{ V}$

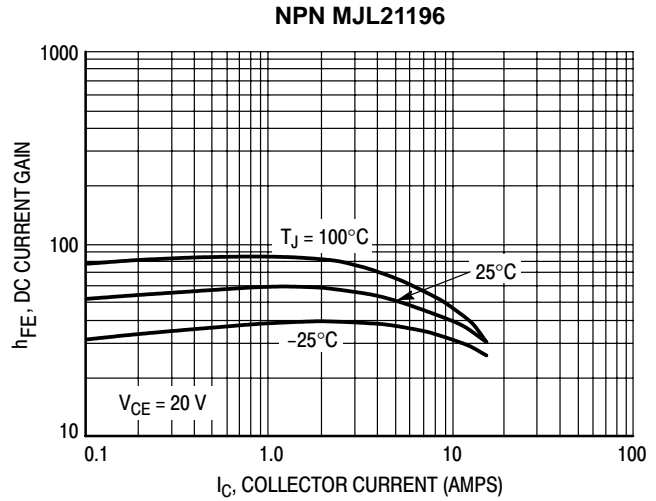


Figure 4. DC Current Gain,  $V_{CE} = 20\text{ V}$

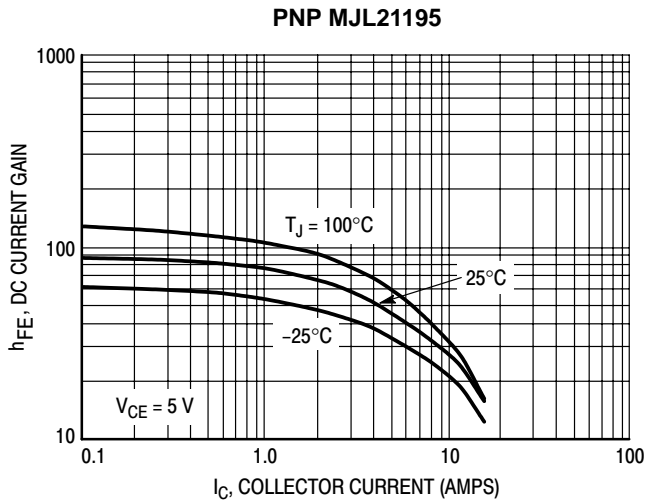


Figure 5. DC Current Gain,  $V_{CE} = 5\text{ V}$

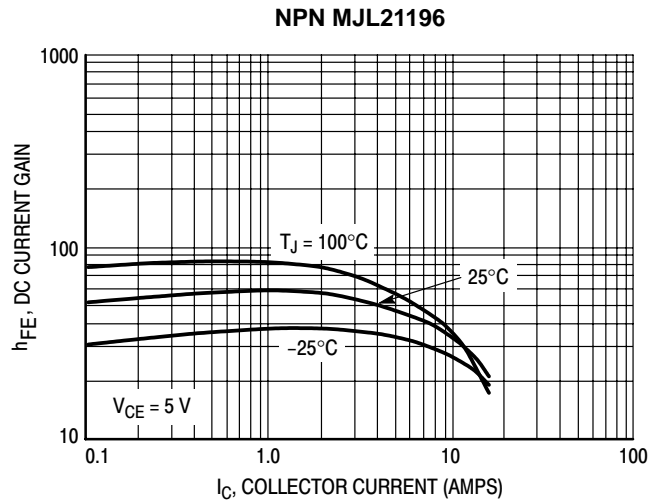


Figure 6. DC Current Gain,  $V_{CE} = 5\text{ V}$

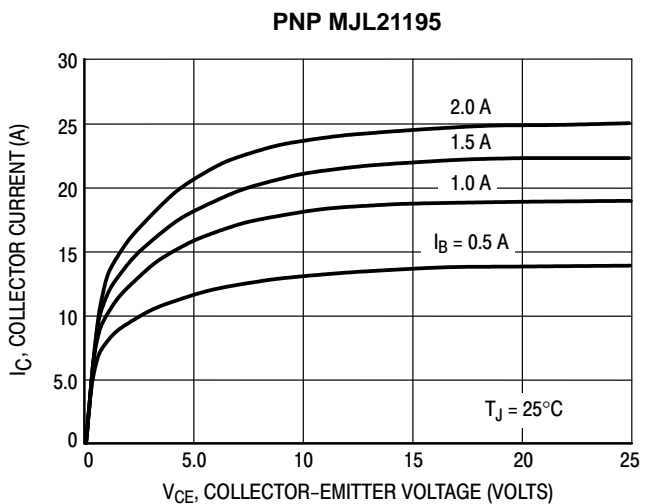


Figure 7. Typical Output Characteristics

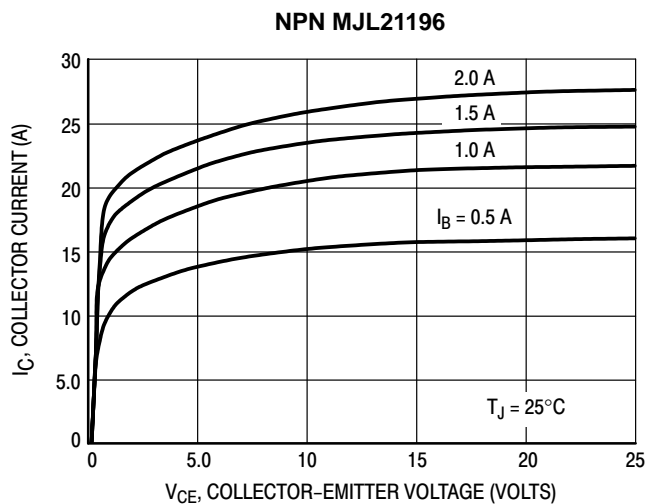


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJL21195

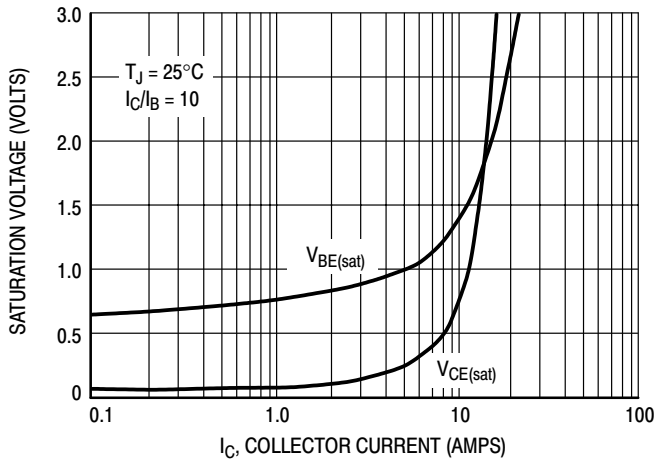


Figure 9. Typical Saturation Voltages

NPN MJL21196

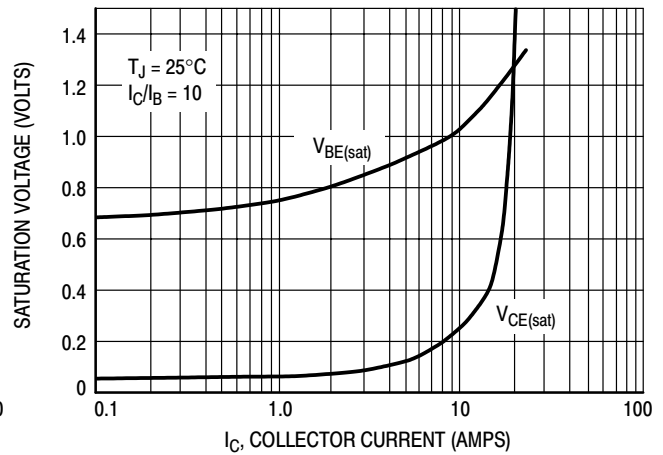


Figure 10. Typical Saturation Voltages

PNP MJL21195

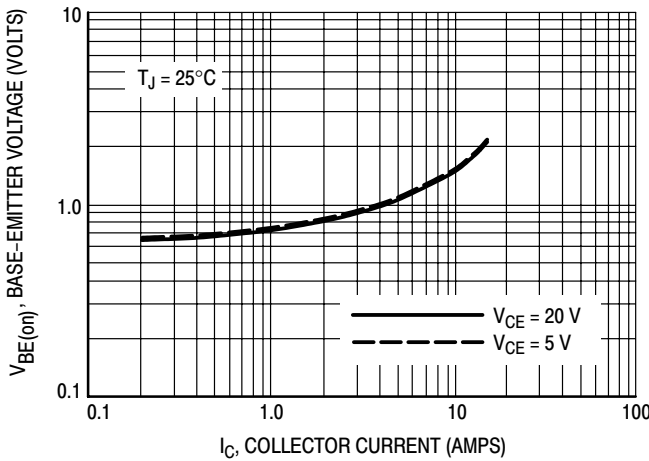


Figure 11. Typical Base-Emitter Voltage

NPN MJL21196

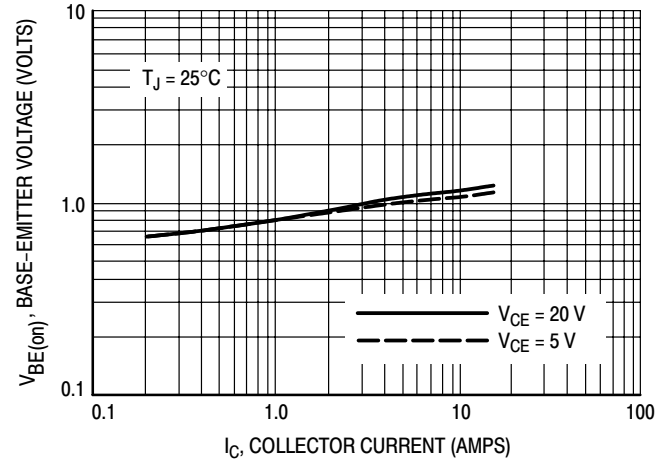


Figure 12. Typical Base-Emitter Voltage

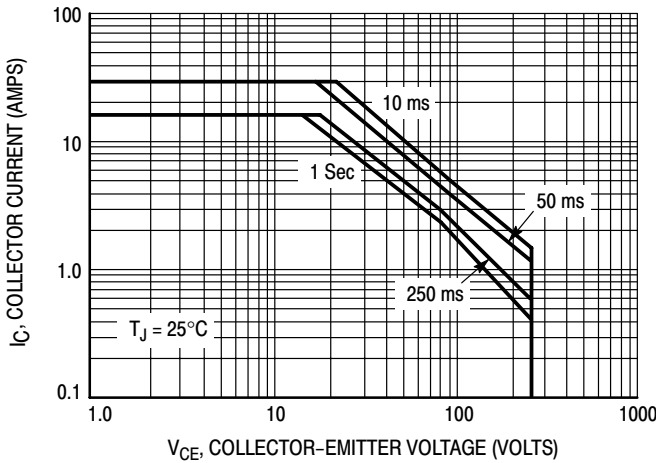


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

# MJL21195 MJL21196

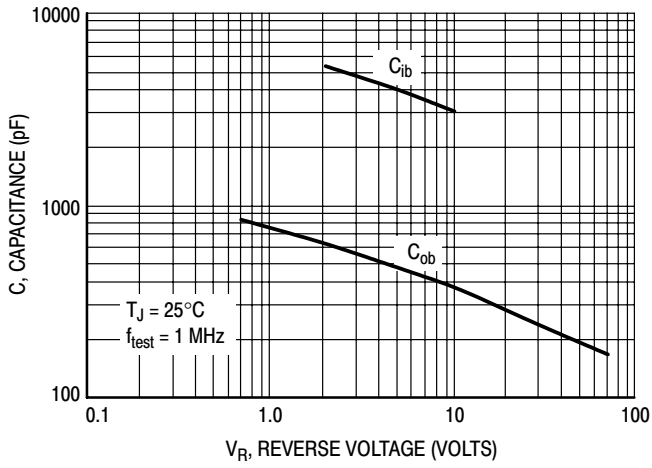


Figure 14. MJL21195 Typical Capacitance

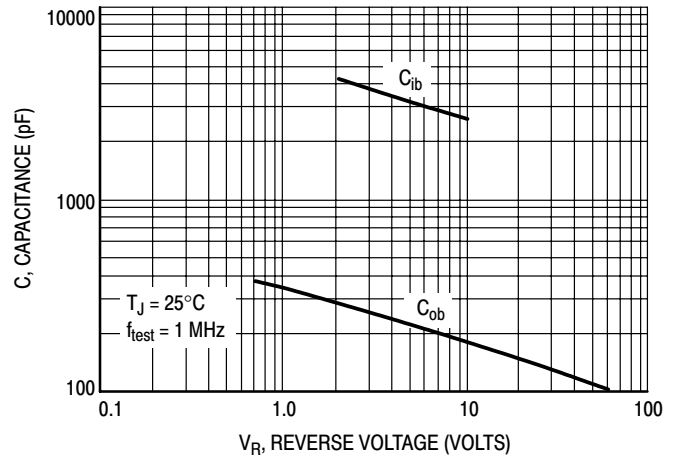


Figure 15. MJL21196 Typical Capacitance

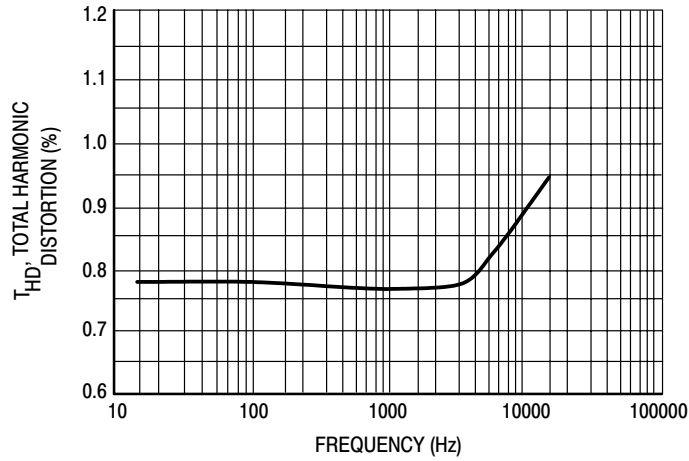


Figure 16. Typical Total Harmonic Distortion

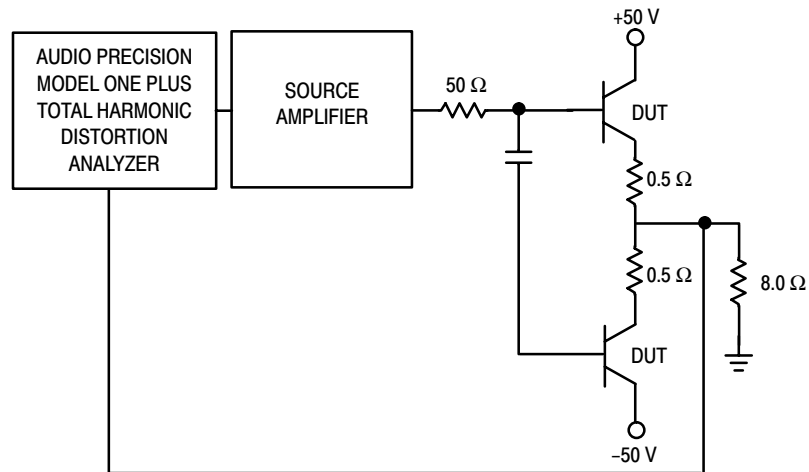


Figure 17. Total Harmonic Distortion Test Circuit

# Complementary NPN-PNP Silicon Power Bipolar Transistor

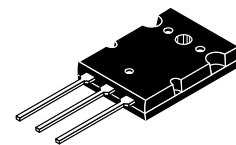
The MJL3281A and MJL1302A are PowerBase™ power transistors for high power audio, disk head positioners and other linear applications.

- Designed for 100 W Audio Frequency
- Gain Complementary:
  - Gain Linearity from 100 mA to 7 A
  - High Gain — 60 to 175
  - $h_{FE} = 45$  (Min) @  $I_C = 8$  A
- Low Harmonic Distortion
- High Safe Operation Area — 1 A/100 V @ 1 Second
- High  $f_T$  — 30 MHz Typical

**NPN**  
**MJL3281A\***  
**PNP**  
**MJL1302A\***

\*ON Semiconductor Preferred Device

**15 AMPERE  
COMPLEMENTARY  
SILICON POWER  
TRANSISTORS  
200 VOLTS  
200 WATTS**



**CASE 340G-02, STYLE 2  
TO-264**

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	200	Vdc
Collector–Base Voltage	$V_{CBO}$	200	Vdc
Emitter–Base Voltage	$V_{EBO}$	7	Vdc
Collector–Emitter Voltage – 1.5 V	$V_{CEX}$	200	Vdc
Collector Current — Continuous — Peak (1)	$I_C$	15 25	Adc
Base Current — Continuous	$I_B$	1.5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	°C

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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## OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100$ mAdc, $I_B = 0$ )	$V_{CEO(sus)}$	200	—	—	Vdc
Emitter–Base Voltage ( $I_E = 100$ $\mu$ Adc, $I_C = 0$ )	$V_{EBO}$	7	—	—	Vdc

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

(continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.



# MJL3281A MJL1302A

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector Cutoff Current ( $V_{CB} = 200\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	—	50	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	5	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = 7\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	25	$\mu\text{Adc}$

### SECOND BREAKDOWN

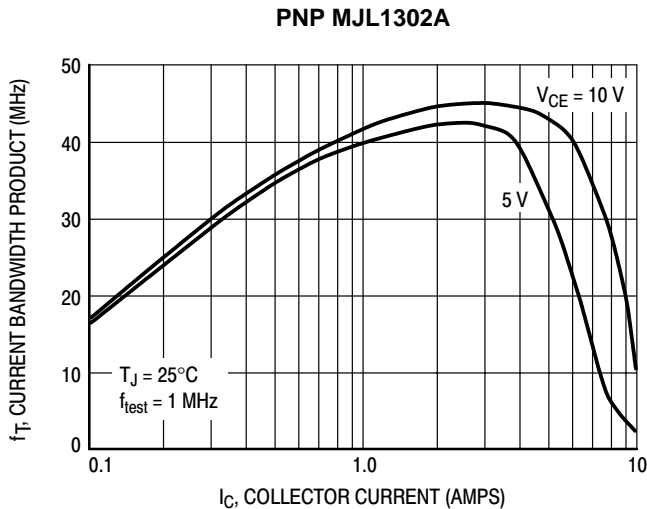
Second Breakdown Collector with Base Forward Biased ( $V_{CE} = 50\text{ Vdc}$ , $t = 1\text{ s}$ (non-repetitive)) ( $V_{CE} = 100\text{ Vdc}$ , $t = 1\text{ s}$ (non-repetitive))	$I_{S/b}$	4 1	— —	— —	A <sub>dc</sub>
--	-----------	--------	--------	--------	-----------------

### ON CHARACTERISTICS

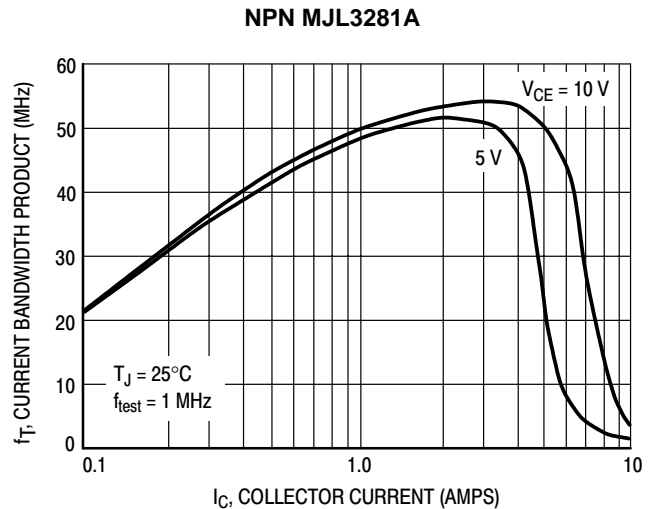
DC Current Gain ( $I_C = 100\text{ mAdc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 1\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 3\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 5\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 7\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 15\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$h_{FE}$	60 60 60 60 60 45 12	125 — — — 115 — 35	175 175 175 175 175 — —	
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ Adc}$ , $I_B = 1\text{ Adc}$ )	$V_{CE(sat)}$	—	—	3	V <sub>dc</sub>

### DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 1\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )	$f_T$	—	30	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ )	$C_{ob}$	—	—	600	pF



**Figure 18. Typical Current Gain Bandwidth Product**



**Figure 19. Typical Current Gain Bandwidth Product**

# MJL3281A MJL1302A

## TYPICAL CHARACTERISTICS

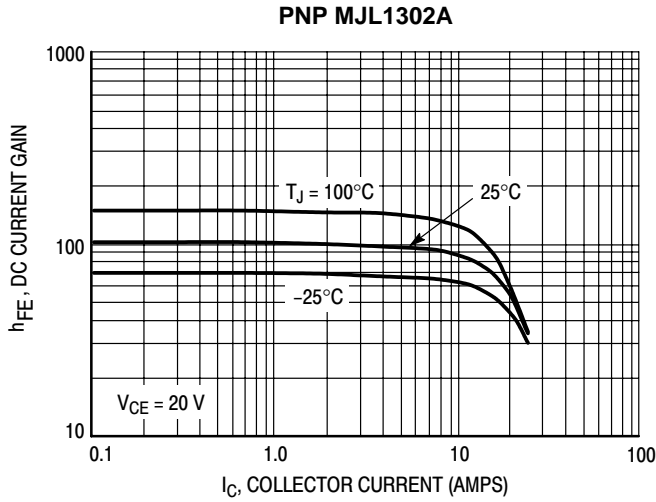


Figure 20. DC Current Gain,  $V_{CE} = 20\text{ V}$

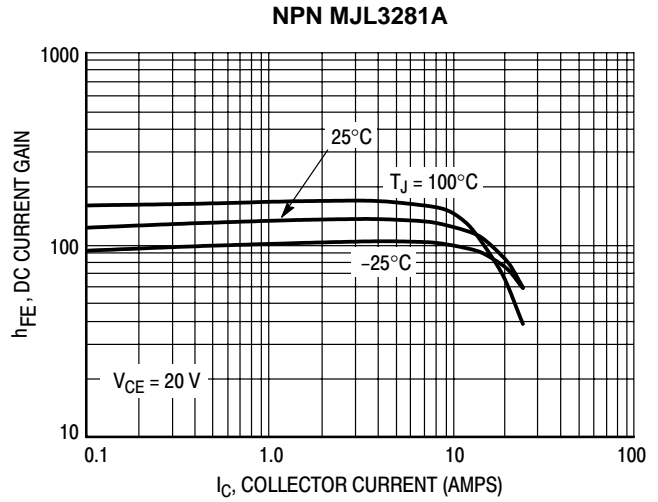


Figure 21. DC Current Gain,  $V_{CE} = 20\text{ V}$

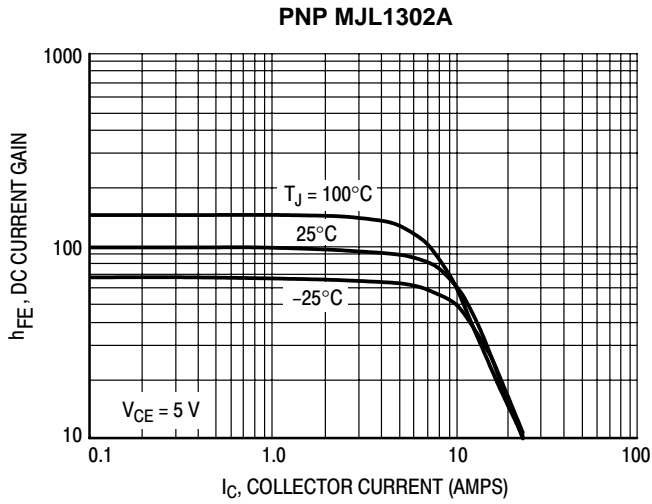


Figure 22. DC Current Gain,  $V_{CE} = 5\text{ V}$

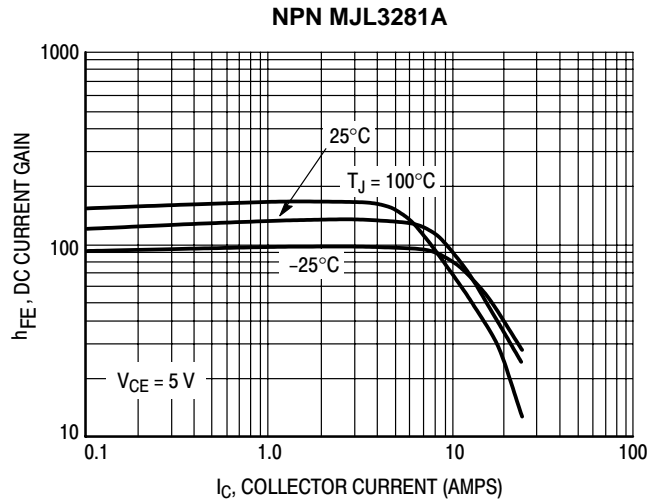


Figure 23. DC Current Gain,  $V_{CE} = 5\text{ V}$

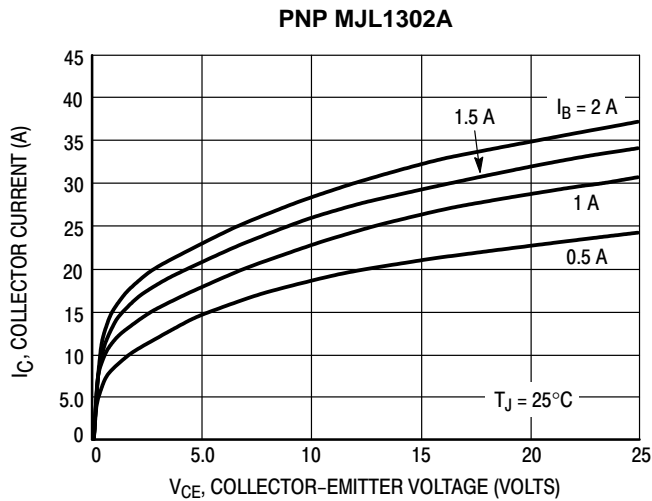


Figure 24. Typical Output Characteristics

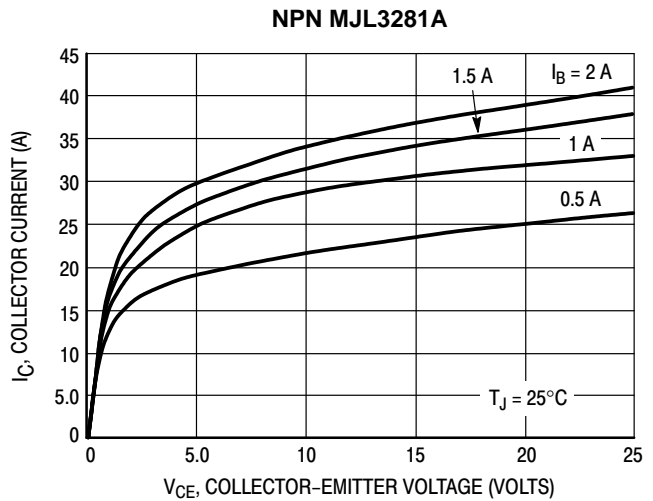


Figure 25. Typical Output Characteristics

# MJL3281A MJL1302A

## TYPICAL CHARACTERISTICS

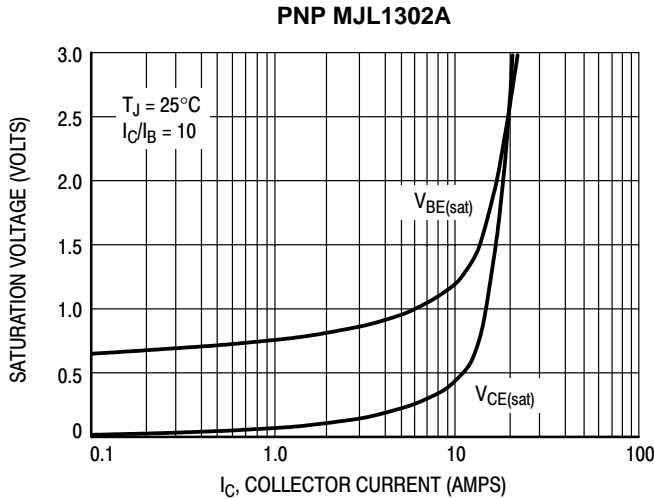


Figure 26. Typical Saturation Voltages

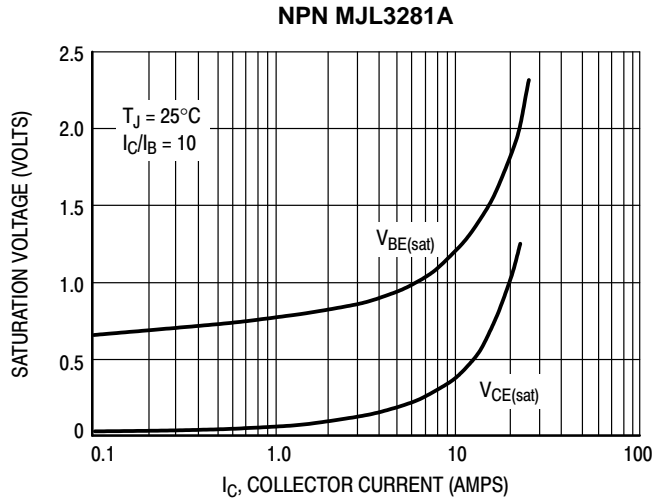


Figure 27. Typical Saturation Voltages

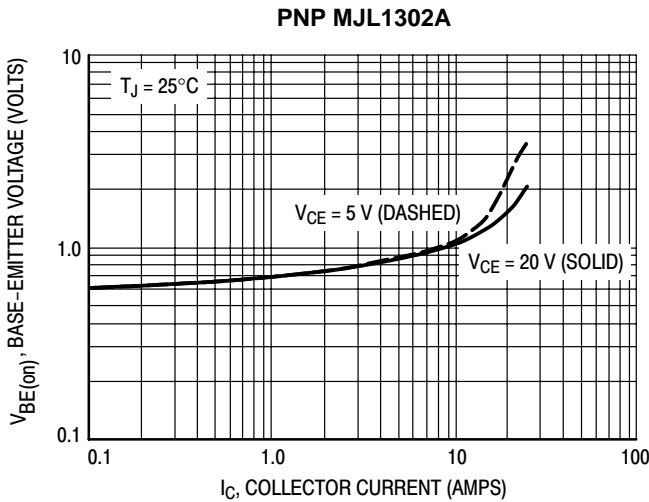


Figure 28. Typical Base-Emitter Voltage

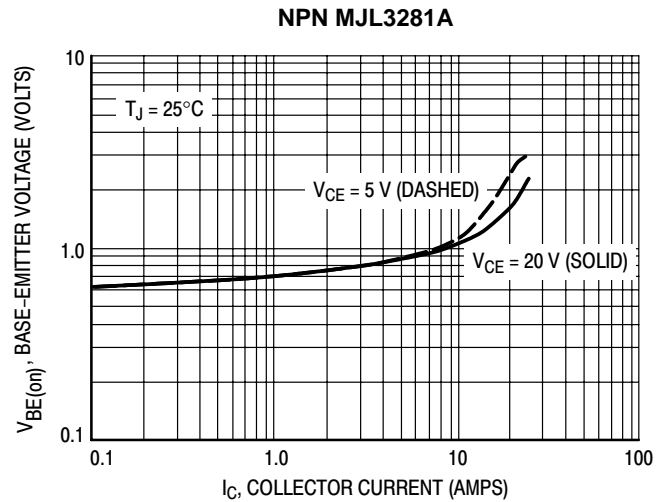


Figure 29. Typical Base-Emitter Voltage

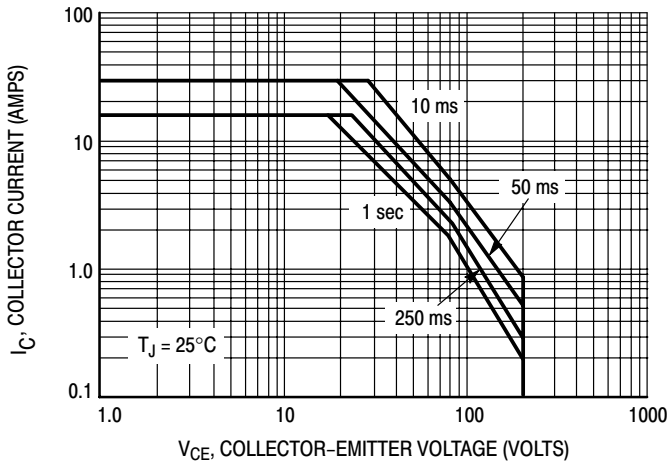


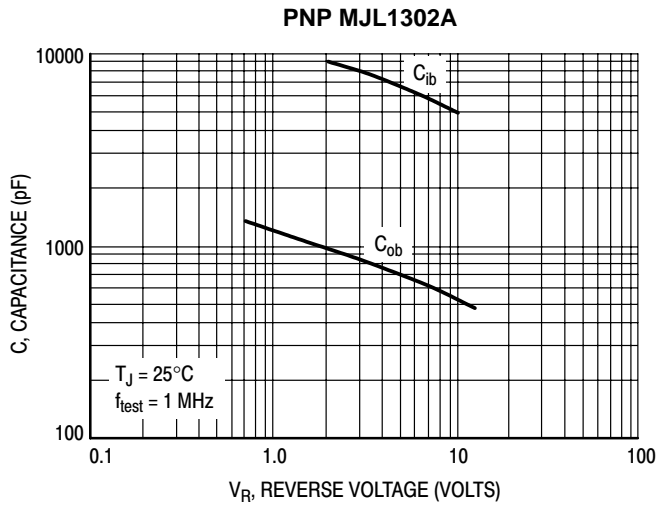
Figure 30. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

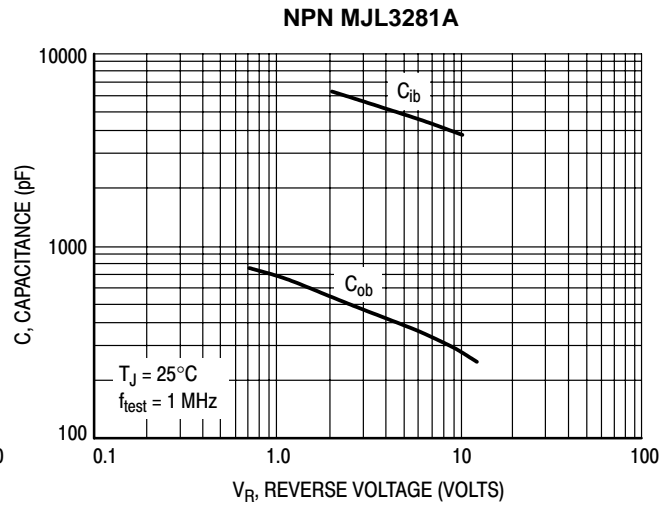
The data of Figure 30 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

# MJL3281A MJL1302A

## TYPICAL CHARACTERISTICS



**Figure 31. MJL1302A Typical Capacitance**



**Figure 32. MJL3281A Typical Capacitance**

# Complementary Silicon Plastic Power Transistors

Specifically designed for power audio output, or high power drivers in audio amplifiers.

- DC Current Gain Specified up to 8.0 Amperes at Temperature
- All On Characteristics at Temperature
- High SOA: 20 A, 18 V, 100 ms
- TO-247AE Package

## MAXIMUM RATINGS

Rating	Symbol	MJW21191 MJW21192	Unit
Collector–Emitter Voltage	$V_{CEO}$	150	Vdc
Collector–Base Voltage	$V_{CB}$	150	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous — Peak	$I_C$	8.0 16	Adc
Base Current	$I_B$	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	125 0.65	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

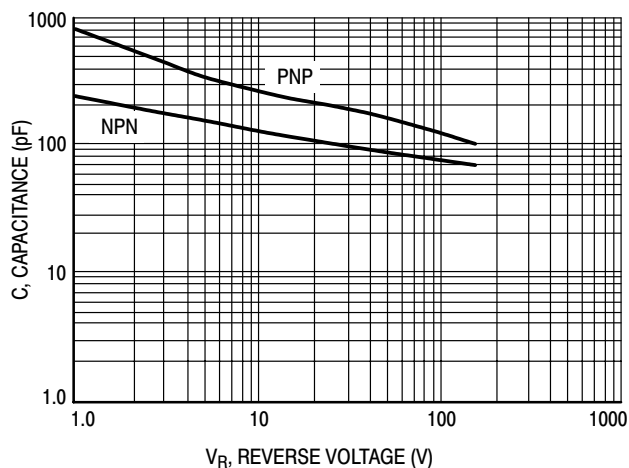


Figure 1. Typical Capacitance @ 25°C

**NPN  
MJW21192**

**PNP  
MJW21191**

**8.0 AMPERES  
POWER TRANSISTORS  
COMPLEMENTARY SILICON  
150 VOLTS  
125 WATTS**

**TO-247  
CASE 340K  
STYLE 3**

**MARKING DIAGRAM**

1 BASE  
2 COLLECTOR  
3 EMITTER

MJW2119x = Device Code  
x = 1 or 2  
LL = Location Code  
Y = Year  
WW = Work Week

# MJW21192 MJW21191

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 10\text{ mA dc}$ , $I_B = 0$ )	$V_{CE(sus)}$	150	—	Vdc
Collector Cutoff Current ( $V_{CB} = 250\text{ Vdc}$ , $I_E = 0$ )	$I_{CES}$	—	10	$\mu\text{A dc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	10	$\mu\text{A dc}$
<b>ON CHARACTERISTICS (1)</b>				
DC Current Gain ( $I_C = 4.0\text{ A dc}$ , $V_{CE} = 2.0\text{ Vdc}$ ) ( $I_C = 8.0\text{ A dc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$h_{FE}$	15 5.0	— —	— 100
Collector–Emitter Saturation Voltage ( $I_C = 4.0\text{ A dc}$ , $I_B = 0.4\text{ A dc}$ ) ( $I_C = 8.0\text{ A dc}$ , $I_B = 1.6\text{ A dc}$ )	$V_{CE(sat)}$	— —	1.0 2.0	Vdc
Base–Emitter On Voltage ( $I_C = 4.0\text{ A dc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$V_{BE(on)}$	—	2.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current Gain — Bandwidth Product (2) ( $I_C = 1.0\text{ A dc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	4.0	—	MHz

- (1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .  
 (2)  $f_T = |h_{fe}| \cdot f_{test}$ .

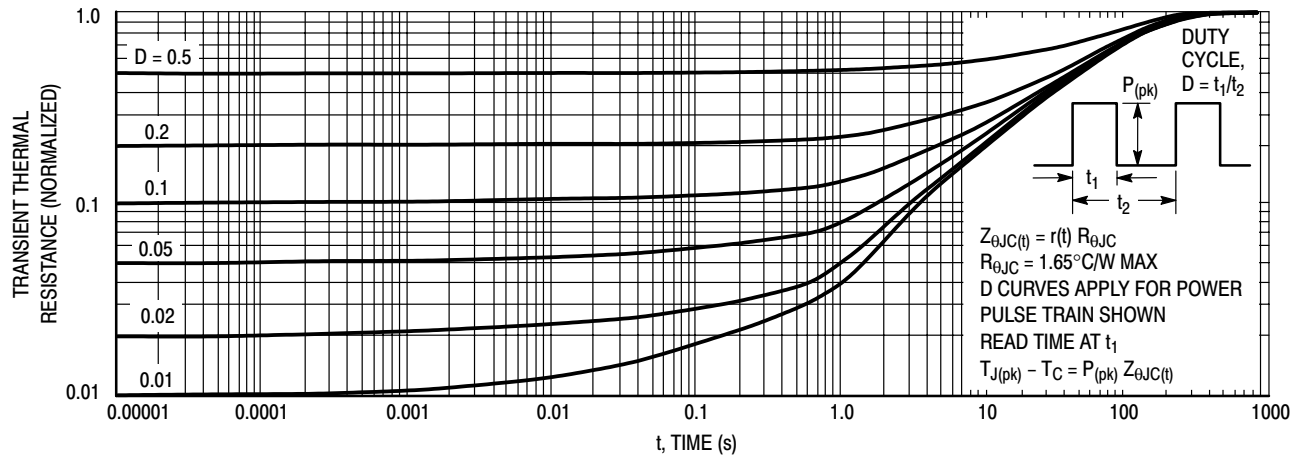


Figure 2. Thermal Response

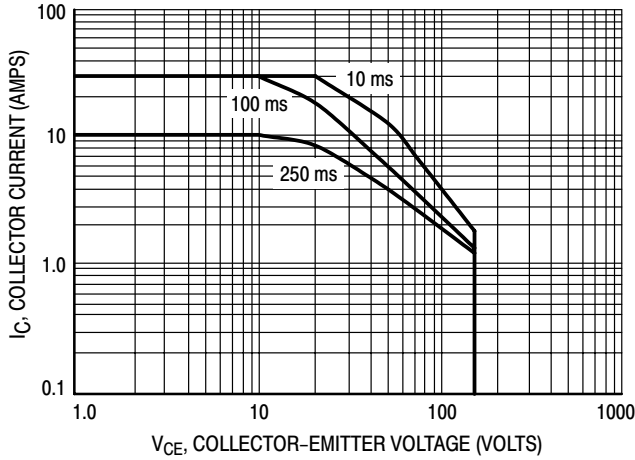
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 3 and 4 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown

pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

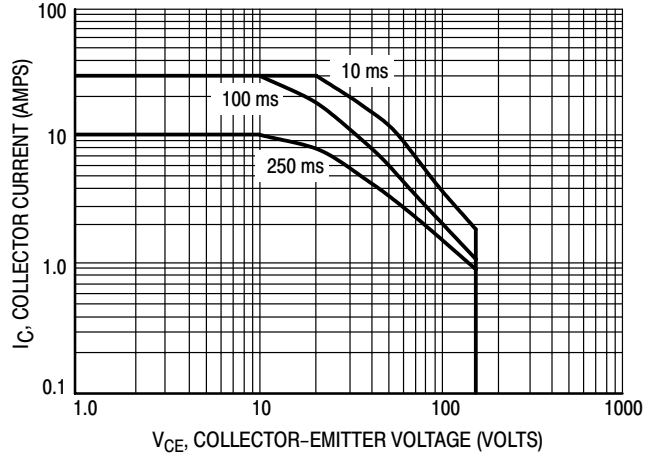
# MJW21192 MJW21191

**NPN — MJW21192**



**Figure 3. NPN — MJW21192  
Safe Operating Area**

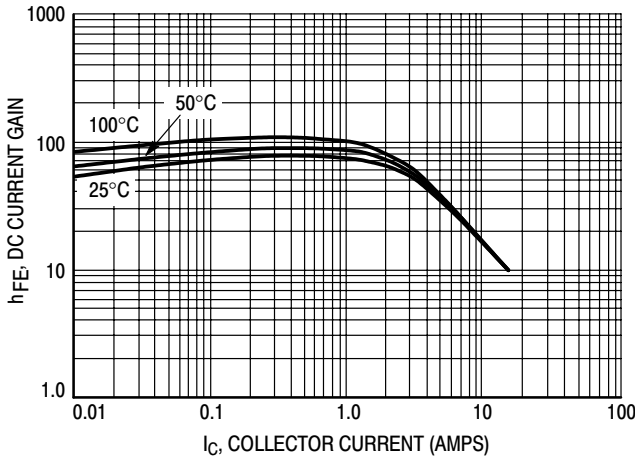
**PNP — MJW21191**



**Figure 4. PNP — MJW21191  
Safe Operating Area**

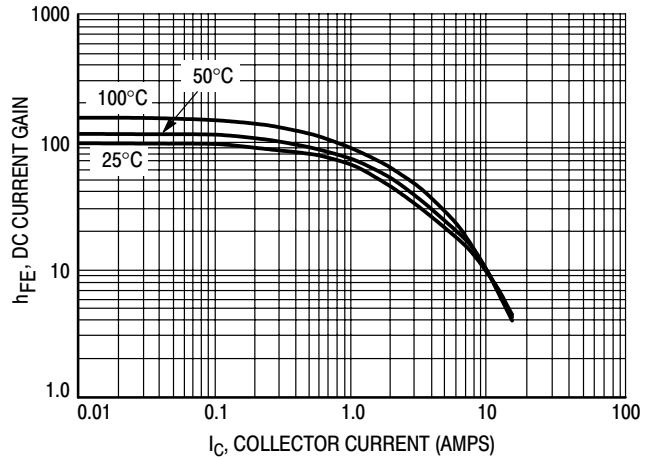
## TYPICAL CHARACTERISTICS

**NPN — MJW21192**



**Figure 5. NPN — MJW21192  
V<sub>CE</sub> = 2.0 V DC Current Gain**

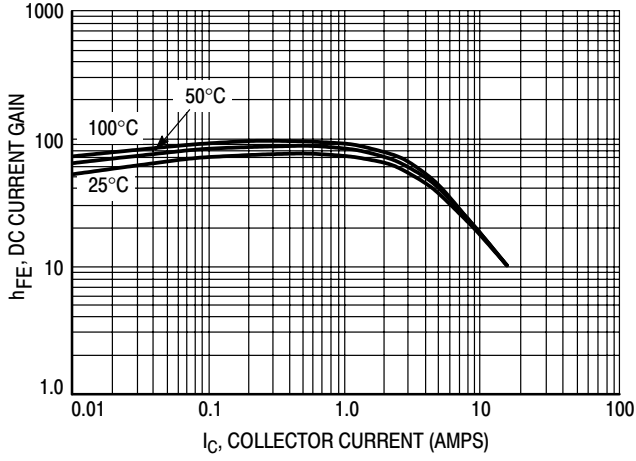
**PNP — MJW21191**



**Figure 6. PNP — MJW21191  
V<sub>CE</sub> = 2.0 V DC Current Gain**

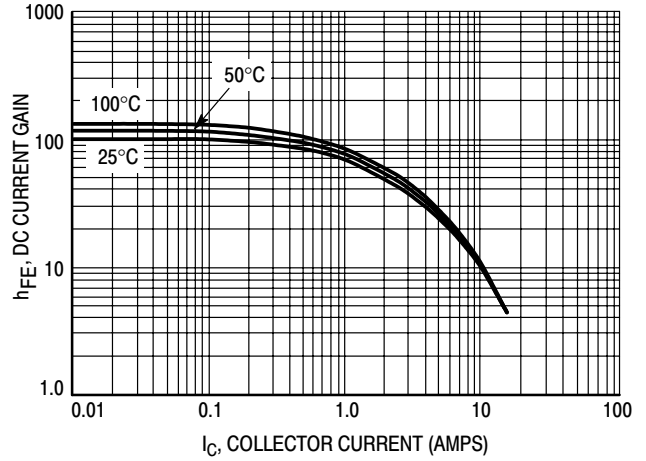
# MJW21192 MJW21191

**NPN — MJW21192**

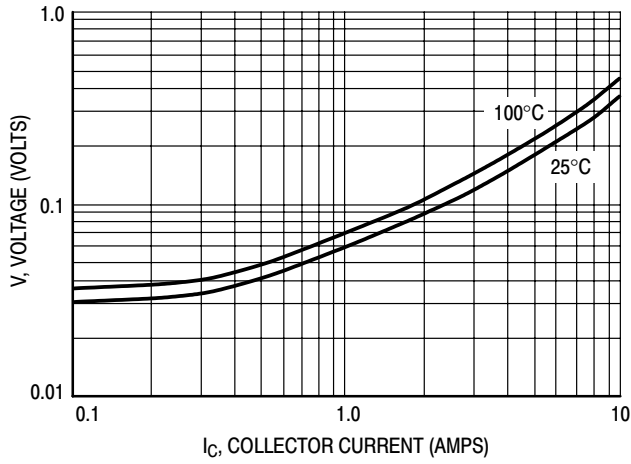


**Figure 7. NPN — MJW21192**  
 $V_{CE} = 5.0 \text{ V DC Current Gain}$

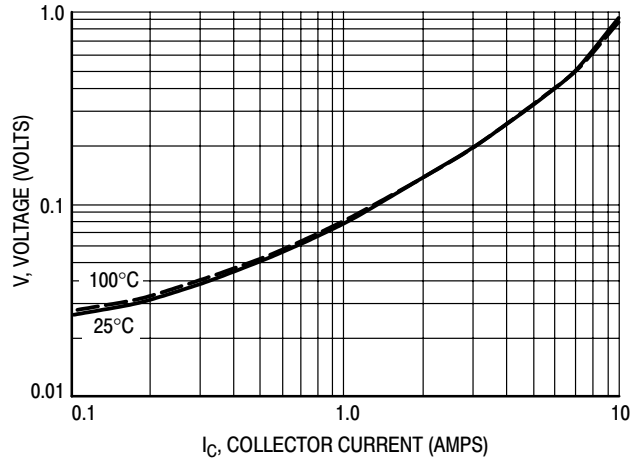
**PNP — MJW21191**



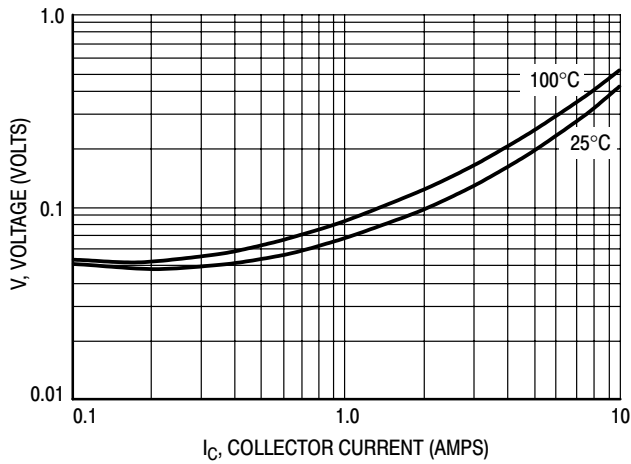
**Figure 8. PNP — MJW21191**  
 $V_{CE} = 5.0 \text{ V DC Current Gain}$



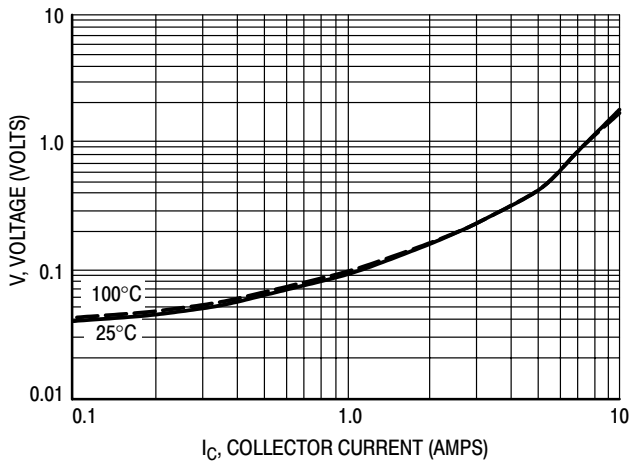
**Figure 9. NPN — MJW21192**  
 $V_{CE(sat)} I_C/I_B = 5.0$



**Figure 10. PNP — MJW21191**  
 $V_{CE(sat)} I_C/I_B = 5.0$



**Figure 11. NPN — MJW21192**  
 $V_{CE(sat)} I_C/I_B = 10$



**Figure 12. PNP — MJW21191**  
 $V_{CE(sat)} I_C/I_B = 10$



# MJW21192 MJW21191

NPN — MJW21192

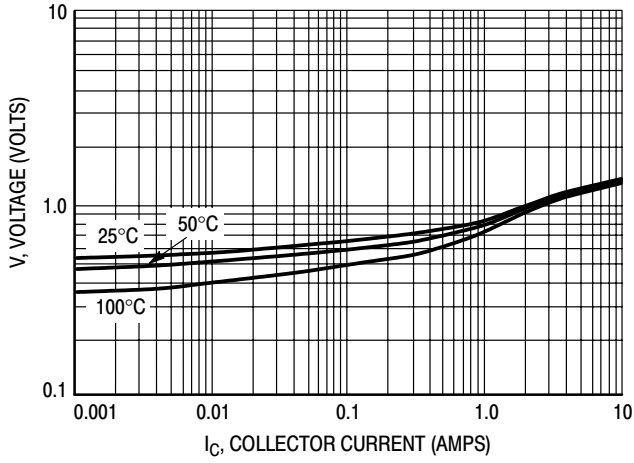


Figure 13. NPN — MJW21192  
 $V_{CE} = 2.0 \text{ V } V_{BE(on)}$  Curve

PNP — MJW21191

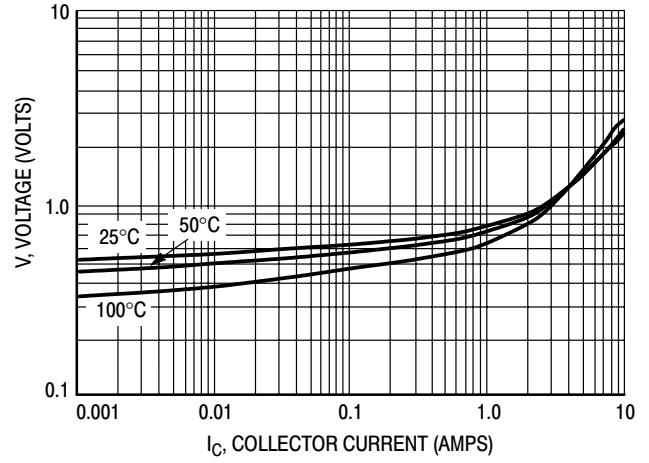


Figure 14. PNP — MJW21191  
 $V_{CE} = 2.0 \text{ V } V_{BE(on)}$  Curve

# MJW21193 (PNP) MJW21194 (NPN)

Preferred Devices

## Silicon Power Transistors

The MJW21193 and MJW21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –  
 $h_{FE} = 20 \text{ Min @ } I_C = 8 \text{ A dc}$
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	Vdc
Collector–Base Voltage	$V_{CBO}$	400	Vdc
Emitter–Base Voltage	$V_{EBO}$	5.0	Vdc
Collector–Emitter Voltage – 1.5 V	$V_{CEX}$	400	Vdc
Collector Current – Continuous – Peak (Note 1.)	$I_C$	16 30	Adc
Base Current – Continuous	$I_B$	5.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	200 1.43	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	$^\circ\text{C/W}$

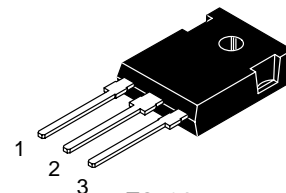
1. Pulse Test: Pulse Width = 5  $\mu\text{s}$ , Duty Cycle  $\leq 10\%$ .



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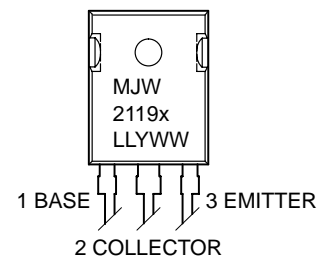
<http://onsemi.com>

**16 AMPERES  
COMPLEMENTARY  
SILICON POWER  
TRANSISTORS  
250 VOLTS  
200 WATTS**



TO-247  
CASE 340K  
STYLE 3

### MARKING DIAGRAM



MJW2119x = Device Code  
x = 3 or 4  
LL = Location Code  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MJW21193	TO-247	30 Units/Rail
MJW21194	TO-247	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

# MJW21193 (PNP) MJW21194 (NPN)

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	250	–	–	Vdc
Collector Cutoff Current ( $V_{CE} = 200\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	–	100	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{CE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	–	100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 250\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ )	$I_{CEX}$	–	–	100	$\mu\text{Adc}$

### SECOND BREAKDOWN

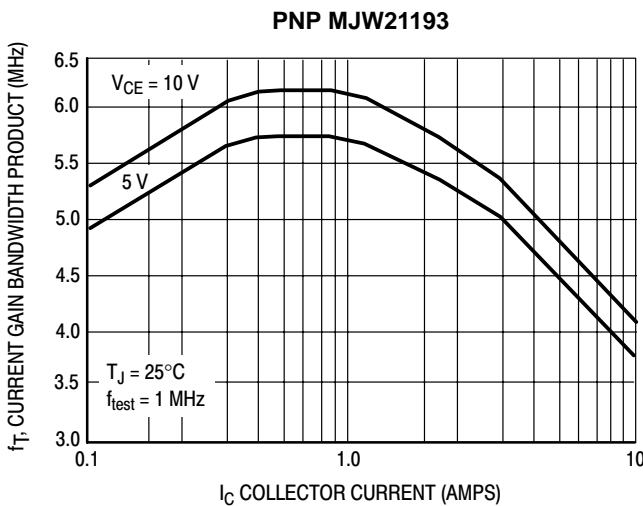
Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 50\text{ Vdc}$ , $t = 1\text{ s}$ (non–repetitive)) ( $V_{CE} = 80\text{ Vdc}$ , $t = 1\text{ s}$ (non–repetitive))	$I_{S/b}$	4.0 2.25	– –	– –	A dc
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### ON CHARACTERISTICS

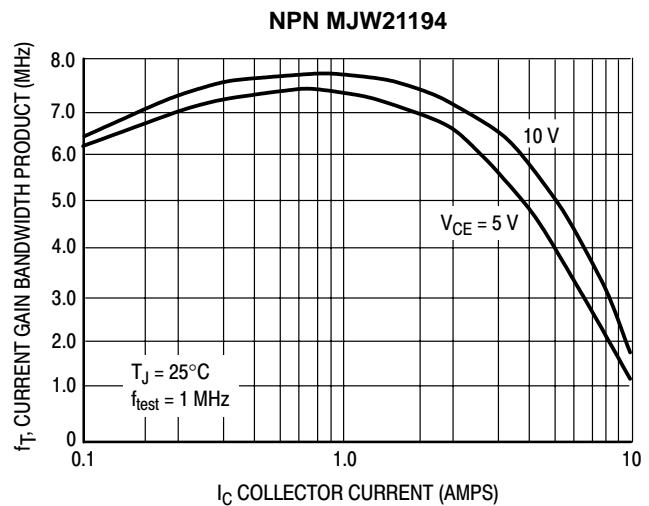
DC Current Gain ( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 5\text{ Adc}$ )	$h_{FE}$	20 8	– –	60 –	
Base–Emitter On Voltage ( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$V_{BE(on)}$	–	–	2.2	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.8\text{ Adc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 3.2\text{ Adc}$ )	$V_{CE(sat)}$	– –	– –	1.4 4	Vdc

### DYNAMIC CHARACTERISTICS

Total Harmonic Distortion at the Output $V_{RMS} = 28.3\text{ V}$ , $f = 1\text{ kHz}$ , $P_{LOAD} = 100\text{ W}_{RMS}$  (Matched pair $h_{FE} = 50 @ 5\text{ A}/5\text{ V}$ )	$h_{FE}$ unmatched $h_{FE}$ matched	$T_{HD}$	– –	0.8 0.08	– –	%
Current Gain Bandwidth Product ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )		$f_T$	4	–	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ )		$C_{ob}$	–	–	500	pF



**Figure 1. Typical Current Gain Bandwidth Product**



**Figure 2. Typical Current Gain Bandwidth Product**

# MJW21193 (PNP) MJW21194 (NPN)

## TYPICAL CHARACTERISTICS

PNP MJW21193

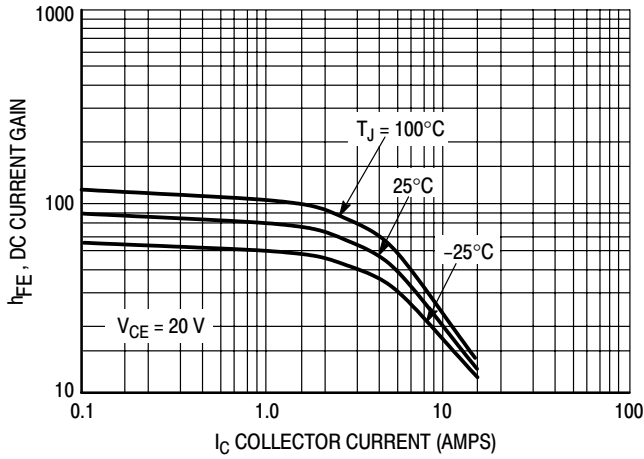


Figure 3. DC Current Gain,  $V_{CE} = 20\text{ V}$

NPN MJW21194

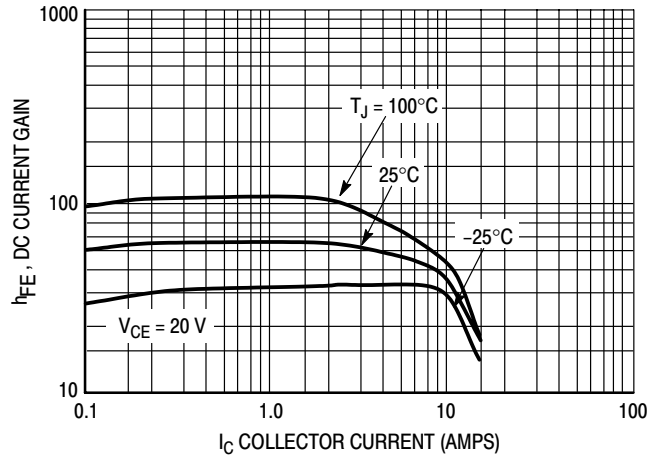


Figure 4. DC Current Gain,  $V_{CE} = 20\text{ V}$

PNP MJW21193

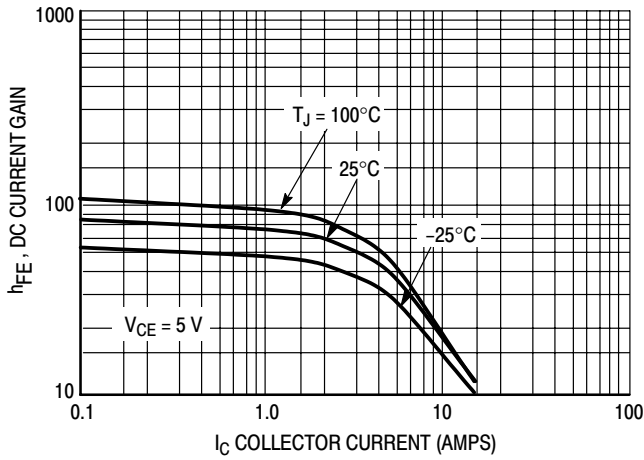


Figure 5. DC Current Gain,  $V_{CE} = 5\text{ V}$

NPN MJW21194

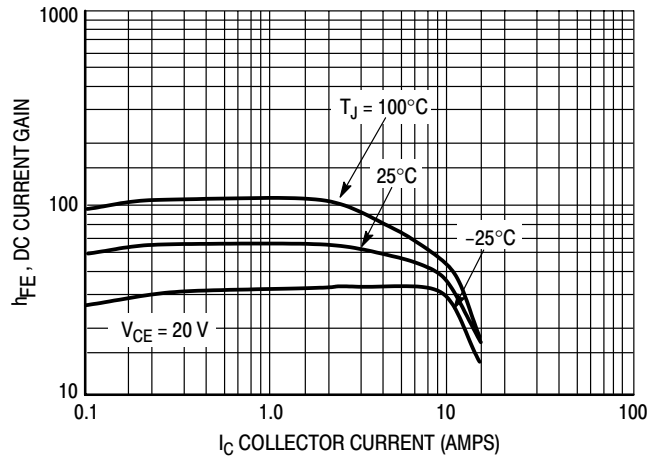


Figure 6. DC Current Gain,  $V_{CE} = 5\text{ V}$

PNP MJW21193

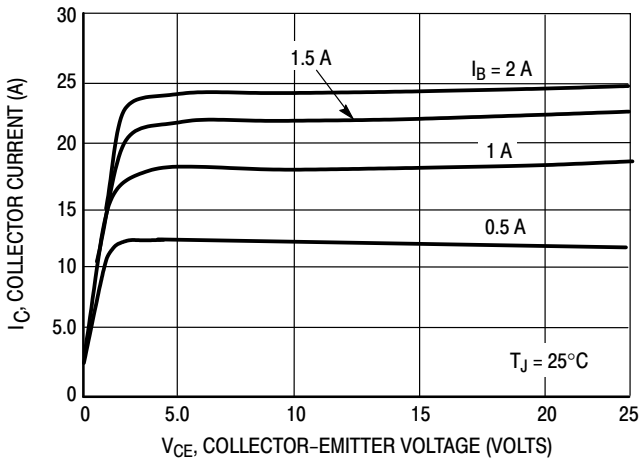


Figure 7. Typical Output Characteristics

NPN MJW21194

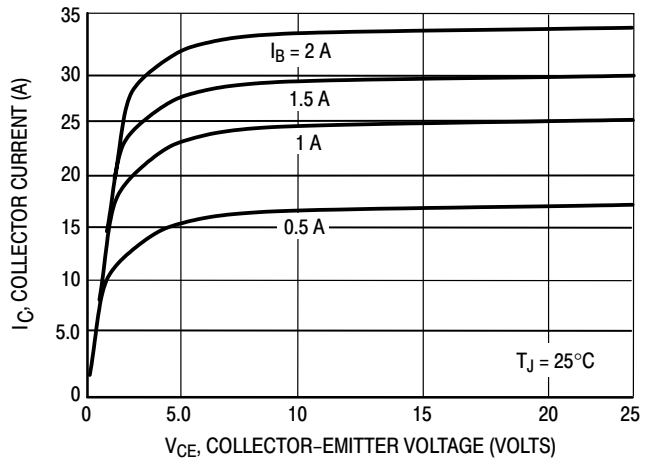


Figure 8. Typical Output Characteristics

# MJW21193 (PNP) MJW21194 (NPN)

## TYPICAL CHARACTERISTICS

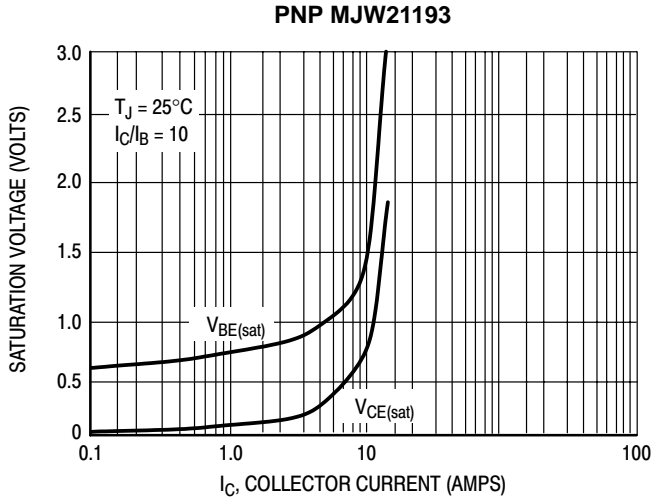


Figure 9. Typical Saturation Voltages

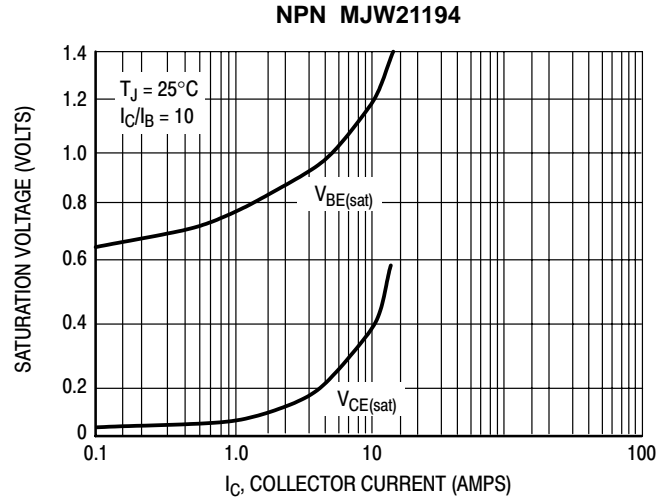


Figure 10. Typical Saturation Voltages

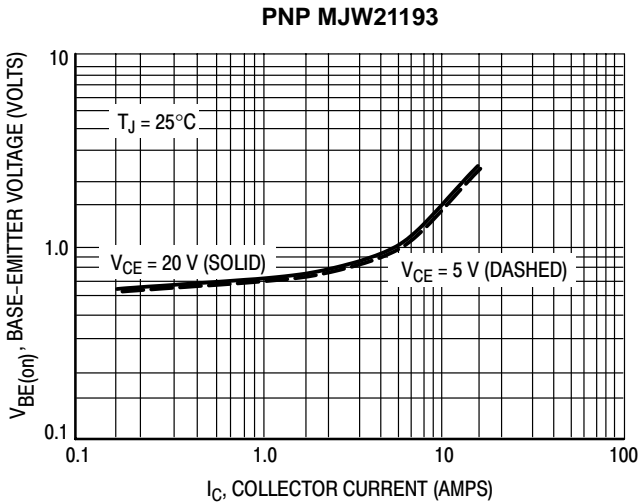


Figure 11. Typical Base-Emitter Voltage

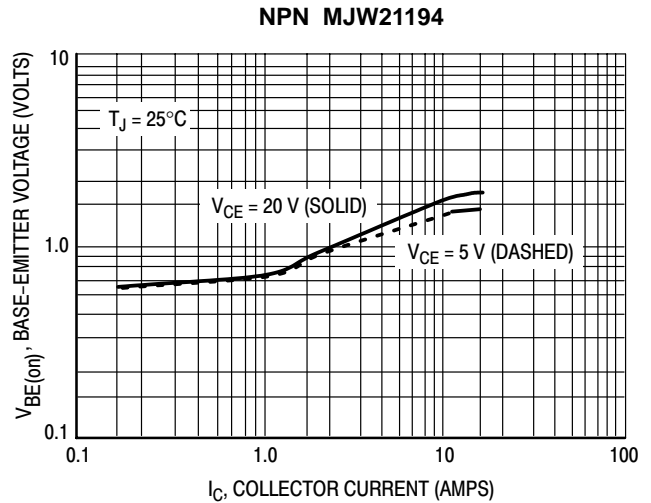


Figure 12. Typical Base-Emitter Voltage

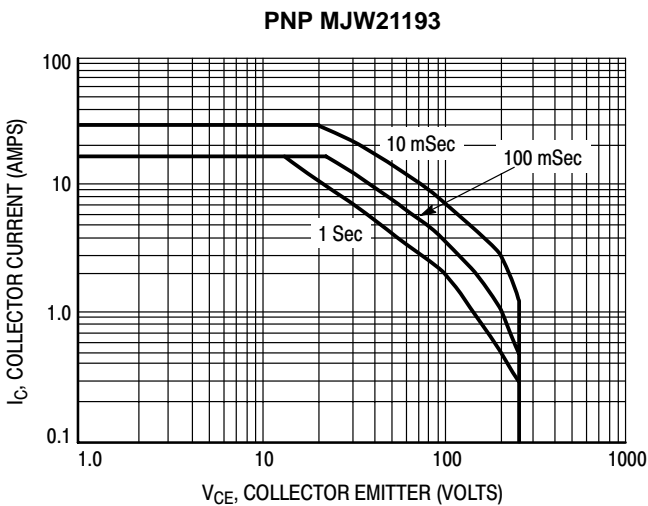


Figure 13. Active Region Safe Operating Area

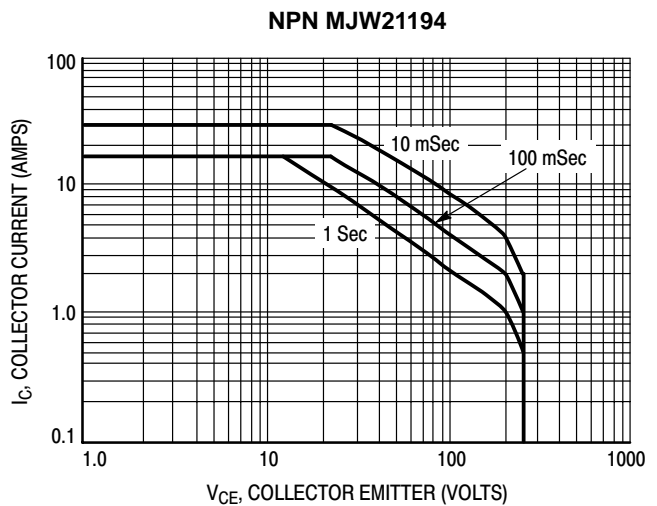


Figure 14. Active Region Safe Operating Area

## MJW21193 (PNP) MJW21194 (NPN)

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

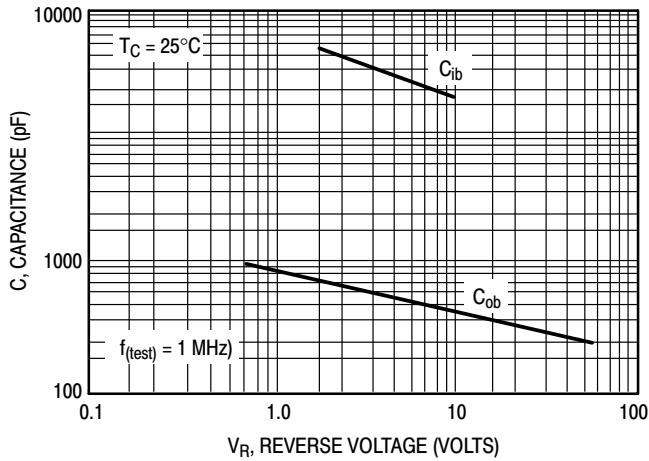


Figure 15. MJW21193 Typical Capacitance

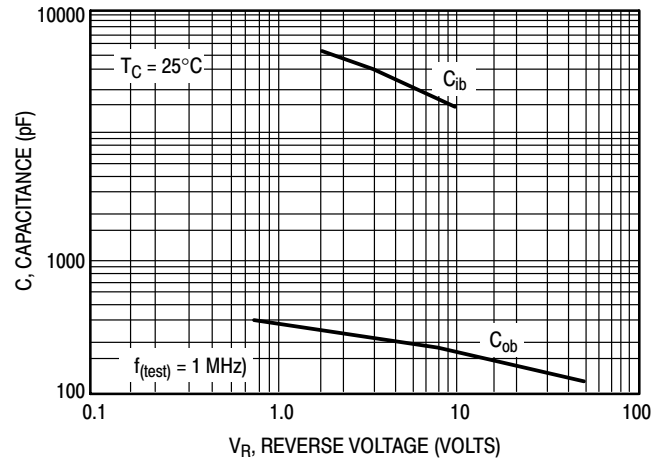


Figure 16. MJW21194 Typical Capacitance

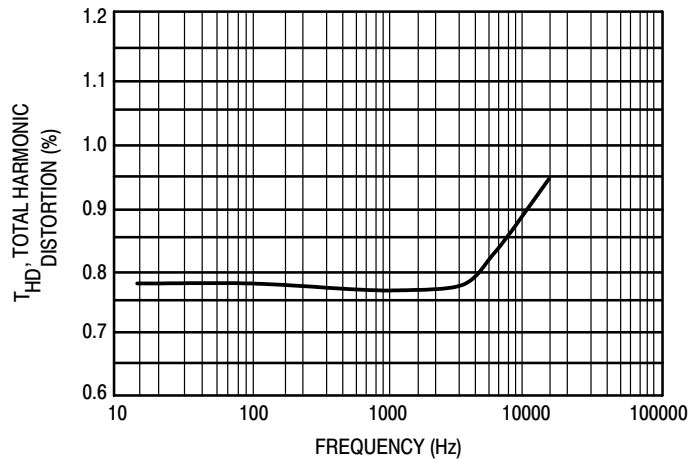


Figure 17. Typical Total Harmonic Distortion

# MJW21193 (PNP) MJW21194 (NPN)

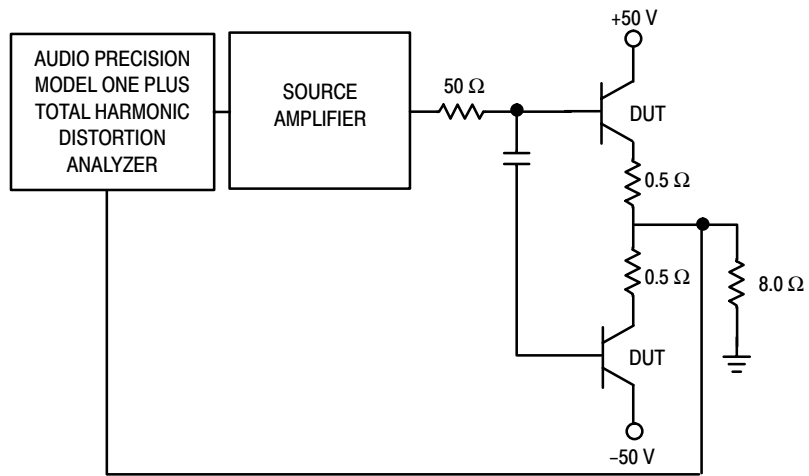


Figure 18. Total Harmonic Distortion Test Circuit

# MJW21195 (PNP) MJW21196 (NPN)

Preferred Devices

## Silicon Power Transistors

The MJW21195 and MJW21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –  
 $h_{FE} = 20 \text{ Min @ } I_C = 8 \text{ A dc}$
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	Vdc
Collector–Base Voltage	$V_{CBO}$	400	Vdc
Emitter–Base Voltage	$V_{EBO}$	5.0	Vdc
Collector–Emitter Voltage – 1.5 V	$V_{CEX}$	400	Vdc
Collector Current – Continuous – Peak (Note 1.)	$I_C$	16 30	Adc
Base Current – Continuous	$I_B$	5.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	200 1.43	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	$^\circ\text{C/W}$

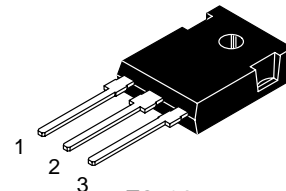
1. Pulse Test: Pulse Width = 5  $\mu\text{s}$ , Duty Cycle  $\leq 10\%$ .



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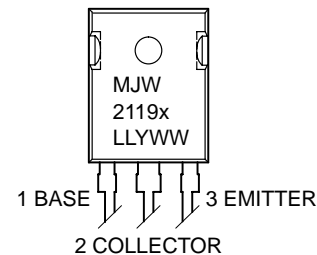
<http://onsemi.com>

**16 AMPERES  
COMPLEMENTARY  
SILICON POWER  
TRANSISTORS  
250 VOLTS  
200 WATTS**



TO–247  
CASE 340K  
STYLE 3

### MARKING DIAGRAM



MJW2119x = Device Code  
x = 5 or 6  
LL = Location Code  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MJW21195	TO–247	30 Units/Rail
MJW21196	TO–247	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.



# MJW21195 (PNP) MJW21196 (NPN)

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 100 mAdc, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	250	–	–	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 200 Vdc, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	100	μAdc

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
----------------	--------	-----	---------	-----	------

### OFF CHARACTERISTICS

Emitter Cutoff Current (V <sub>CE</sub> = 5 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	50	μAdc
Collector Cutoff Current (V <sub>CE</sub> = 250 Vdc, V <sub>BE(off)</sub> = 1.5 Vdc)	I <sub>CEx</sub>	–	–	50	μAdc

### SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased (V <sub>CE</sub> = 50 Vdc, t = 1 s (non-repetitive)) (V <sub>CE</sub> = 80 Vdc, t = 1 s (non-repetitive))	I <sub>S/b</sub>	4.0 2.25	– –	– –	Adc
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### ON CHARACTERISTICS

DC Current Gain (I <sub>C</sub> = 8 Adc, V <sub>CE</sub> = 5 Vdc) (I <sub>C</sub> = 16 Adc, I <sub>B</sub> = 5 Adc)	h <sub>FE</sub>	20 8	– –	80 –	
Base–Emitter On Voltage (I <sub>C</sub> = 8 Adc, V <sub>CE</sub> = 5 Vdc)	V <sub>BE(on)</sub>	–	–	2.0	Vdc
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 0.8 Adc) (I <sub>C</sub> = 16 Adc, I <sub>B</sub> = 3.2 Adc)	V <sub>CE(sat)</sub>	– –	– –	1.0 3	Vdc

### DYNAMIC CHARACTERISTICS

Total Harmonic Distortion at the Output V <sub>RMS</sub> = 28.3 V, f = 1 kHz, P <sub>LOAD</sub> = 100 W <sub>RMS</sub> (Matched pair h <sub>FE</sub> = 50 @ 5 A/5 V)	T <sub>HD</sub>	– –	0.8 0.08	– –	%
Current Gain Bandwidth Product (I <sub>C</sub> = 1 Adc, V <sub>CE</sub> = 10 Vdc, f <sub>test</sub> = 1 MHz)	f <sub>T</sub>	4	–	–	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f <sub>test</sub> = 1 MHz)	C <sub>ob</sub>	–	–	500	pF

PNP MJW21195

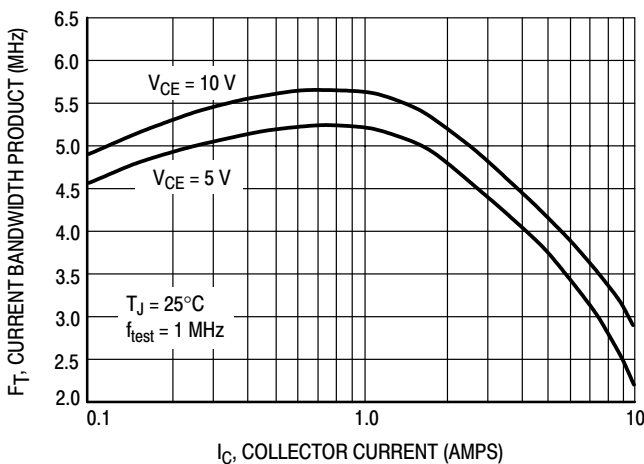


Figure 1. Typical Current Gain Bandwidth Product

NPN MJW21196

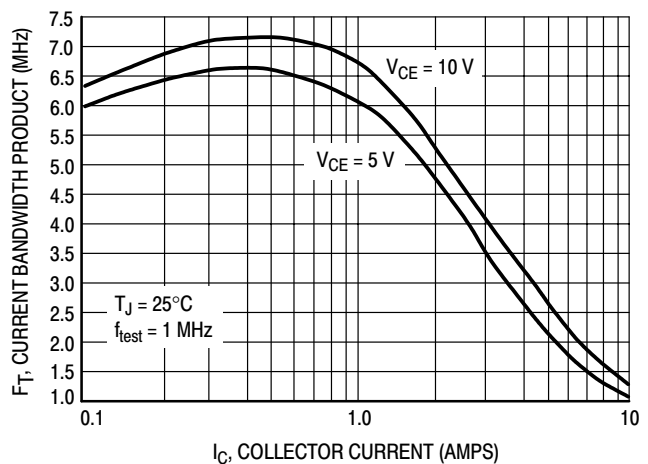
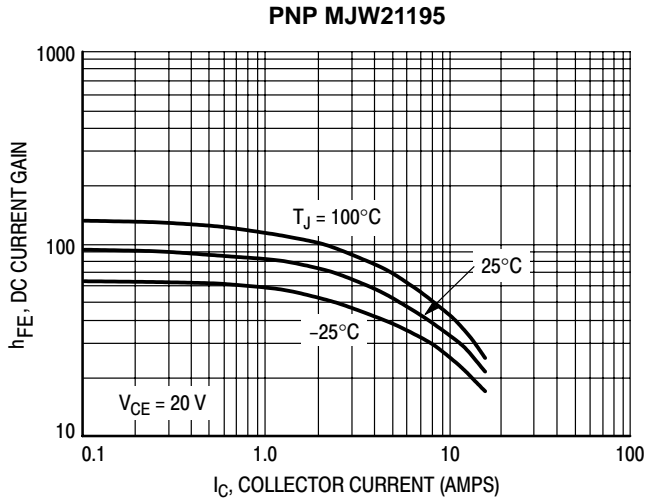


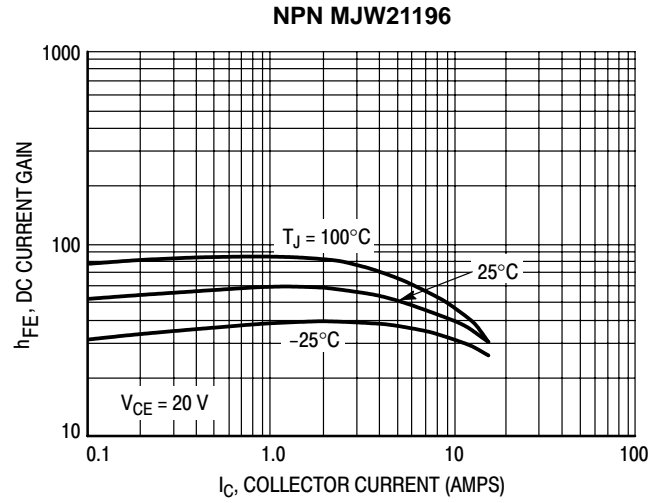
Figure 2. Typical Current Gain Bandwidth Product

# MJW21195 (PNP) MJW21196 (NPN)

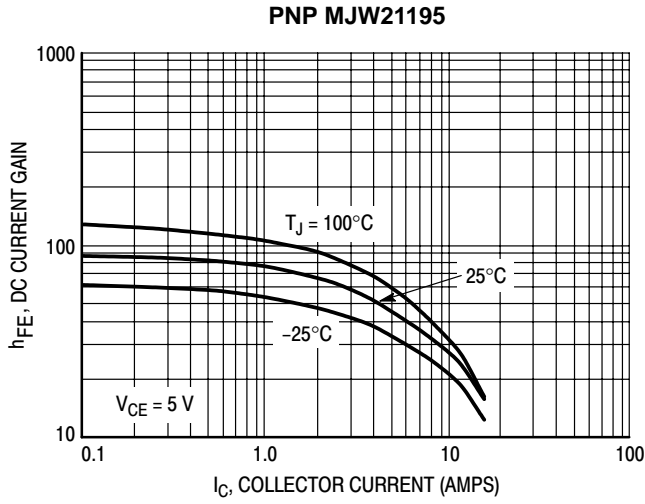
## TYPICAL CHARACTERISTICS



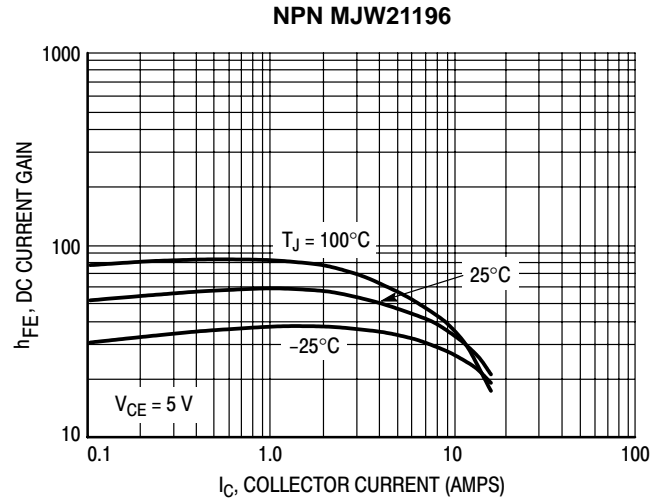
**Figure 3. DC Current Gain,  $V_{CE} = 20\text{ V}$**



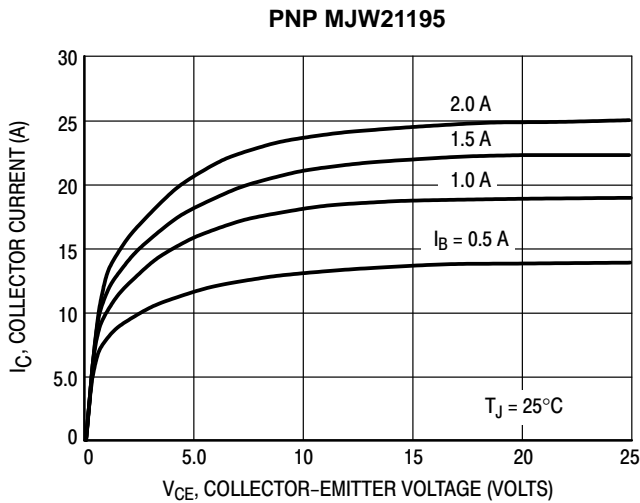
**Figure 4. DC Current Gain,  $V_{CE} = 20\text{ V}$**



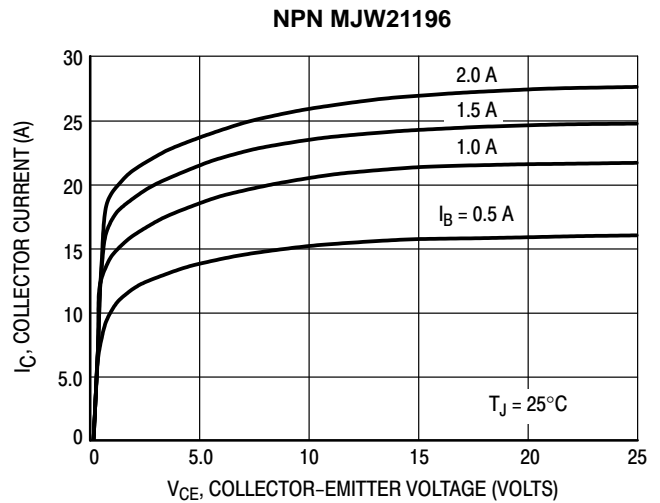
**Figure 5. DC Current Gain,  $V_{CE} = 5\text{ V}$**



**Figure 6. DC Current Gain,  $V_{CE} = 5\text{ V}$**



**Figure 7. Typical Output Characteristics**

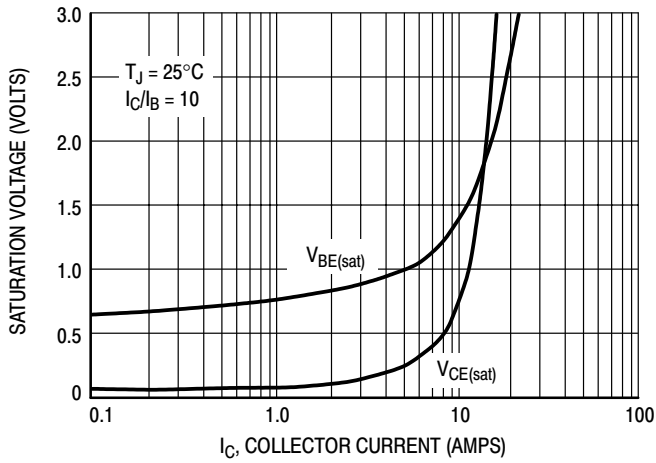


**Figure 8. Typical Output Characteristics**

# MJW21195 (PNP) MJW21196 (NPN)

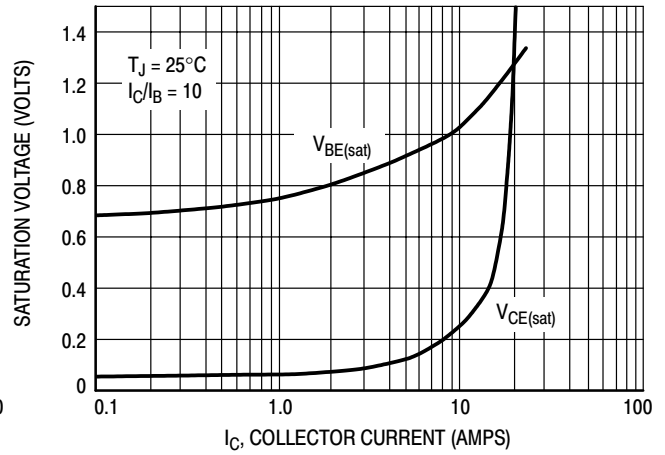
## TYPICAL CHARACTERISTICS

**PNP MJW21195**



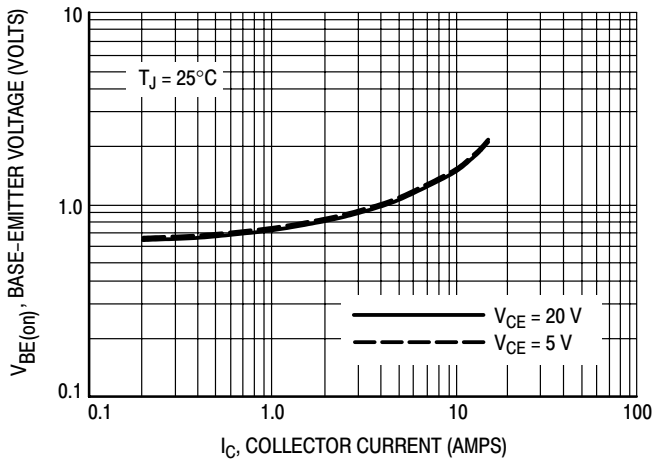
**Figure 9. Typical Saturation Voltages**

**NPN MJW21196**



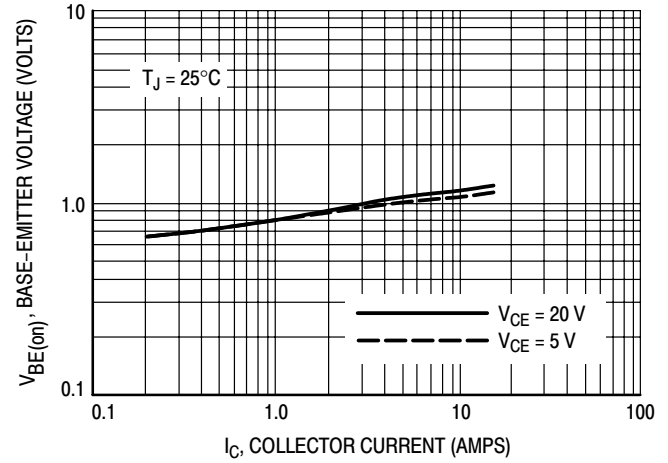
**Figure 10. Typical Saturation Voltages**

**PNP MJW21195**



**Figure 11. Typical Base-Emitter Voltage**

**NPN MJW21196**



**Figure 12. Typical Base-Emitter Voltage**

## MJW21195 (PNP) MJW21196 (NPN)

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

### TYPICAL CHARACTERISTICS

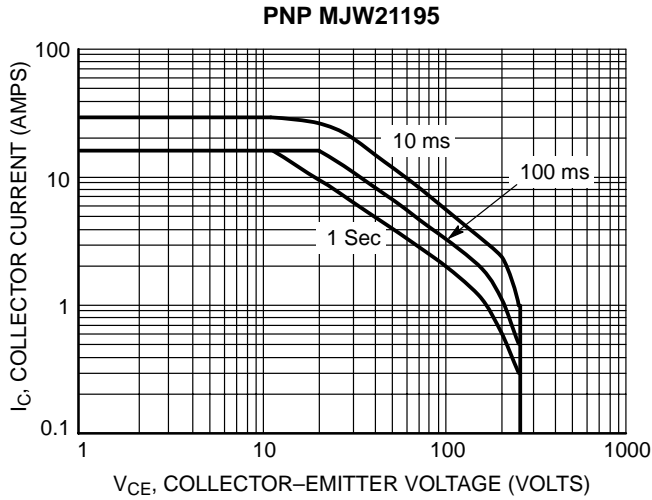


Figure 13. Active Region Safe Operating Area

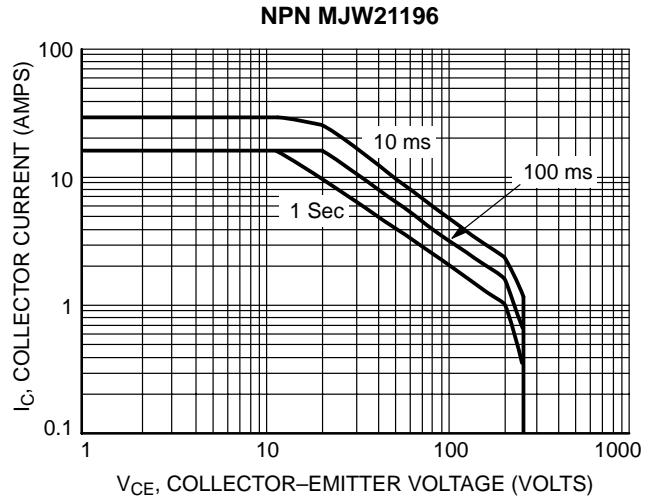


Figure 14. Active Region Safe Operating Area

## MJW21195 (PNP) MJW21196 (NPN)

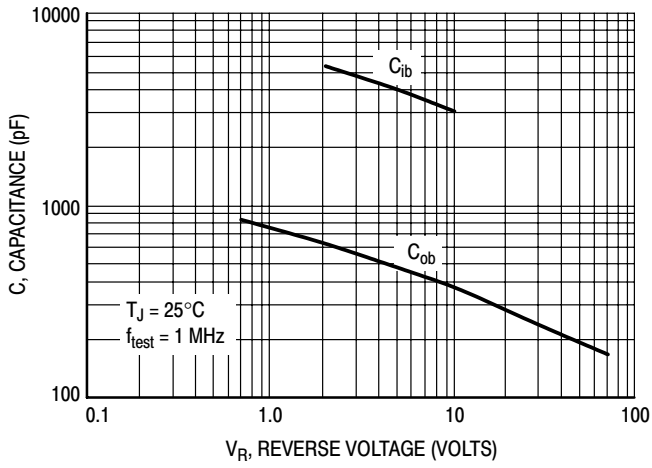


Figure 15. MJW21195 Typical Capacitance

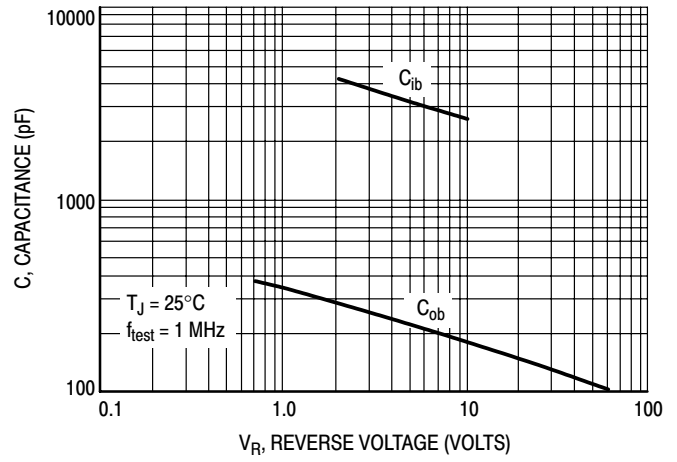


Figure 16. MJW21196 Typical Capacitance

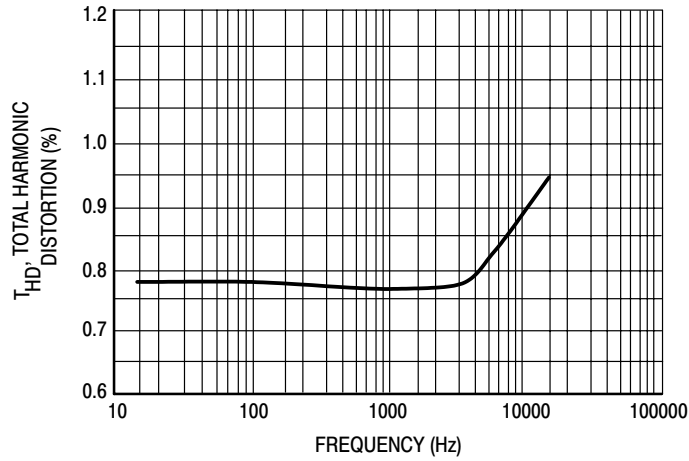


Figure 17. Typical Total Harmonic Distortion

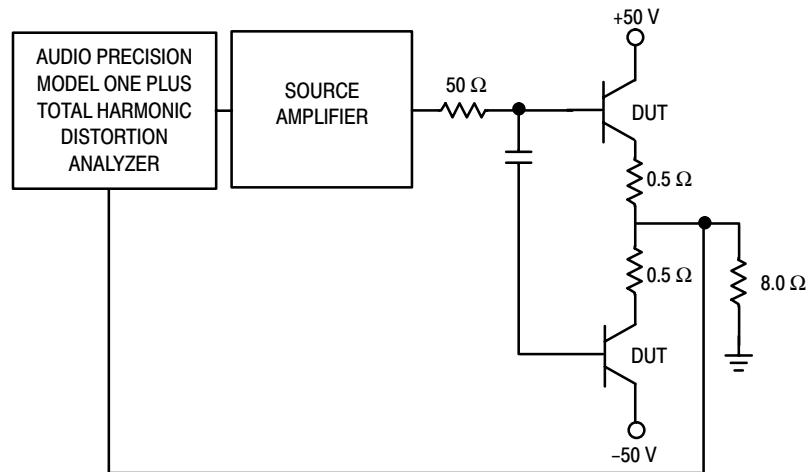


Figure 18. Total Harmonic Distortion Test Circuit

# MJW3281A (NPN) MJW1302A (PNP)

Preferred Devices

## Complementary NPN-PNP Silicon Power Bipolar Transistors

The MJW3281A and MJW1302A are PowerBase™ power transistors for high power audio, disk head positioners and other linear applications.

- Designed for 100 W Audio Frequency
- Gain Complementary:  
Gain Linearity from 100 mA to 7 A  
 $h_{FE} = 45$  (Min) @  $I_C = 8$  A
- Low Harmonic Distortion
- High Safe Operation Area – 1 A/100 V @ 1 Second
- High  $f_T$  – 30 MHz Typical

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	230	Vdc
Collector–Base Voltage	$V_{CBO}$	230	Vdc
Emitter–Base Voltage	$V_{EBO}$	5.0	Vdc
Collector–Emitter Voltage – 1.5 V	$V_{CEX}$	230	Vdc
Collector Current – Continuous – Peak (Note 1.)	$I_C$	15 25	Adc
Base Current – Continuous	$I_B$	1.5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	200 1.43	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	$^\circ\text{C}/\text{W}$

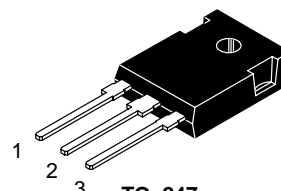
1. Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.



ON Semiconductor™

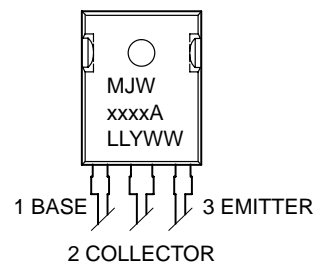
<http://onsemi.com>

**15 AMPERES  
COMPLEMENTARY  
SILICON POWER  
TRANSISTORS  
230 VOLTS  
200 WATTS**



**TO-247  
CASE 340K  
STYLE 3**

### MARKING DIAGRAM



MJWxxxxA = Device Code  
xxxx = 3281 OR 1302  
LL = Location Code  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MJW3281A	TO-247	30 Units/Rail
MJW1302A	TO-247	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

# MJW3281A (NPN) MJW1302A (PNP)

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	230	–	–	Vdc
Collector Cutoff Current ( $V_{CB} = 230\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	–	50	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	–	5	$\mu\text{Adc}$

### SECOND BREAKDOWN

Second Breakdown Collector with Base Forward Biased ( $V_{CE} = 50\text{ Vdc}$ , $t = 1\text{ s}$ (non–repetitive)) ( $V_{CE} = 100\text{ Vdc}$ , $t = 1\text{ s}$ (non–repetitive))	$I_{S/b}$	4 1	– –	– –	Adc
--	-----------	--------	--------	--------	-----

### ON CHARACTERISTICS

DC Current Gain ( $I_C = 100\text{ mAdc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 1\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 3\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 5\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 7\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 15\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$h_{FE}$	50 50 50 50 50 45 12	125 – – – 115 – 35	200 200 200 200 200 – –	–
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ Adc}$ , $I_B = 1\text{ Adc}$ )	$V_{CE(sat)}$	–	0.4	2	Vdc
Base–Emitter On Voltage ( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$V_{BE(on)}$	–	–	2	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product ( $I_C = 1\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )	$f_T$	–	30	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ )	$C_{ob}$	–	–	600	pF

PNP MJW1302A

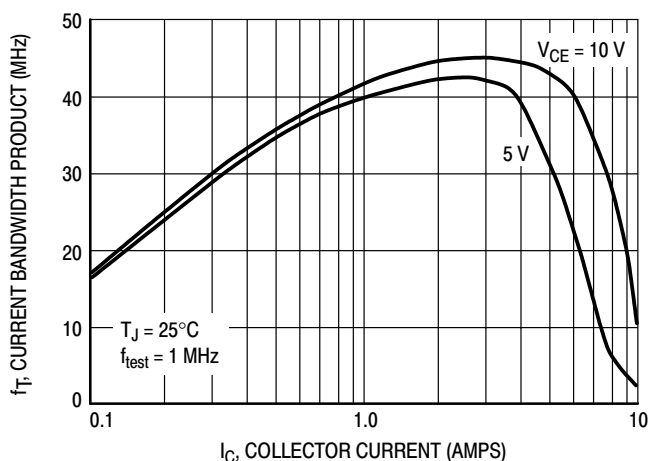


Figure 19. Typical Current Gain Bandwidth Product

NPN MJW3281A

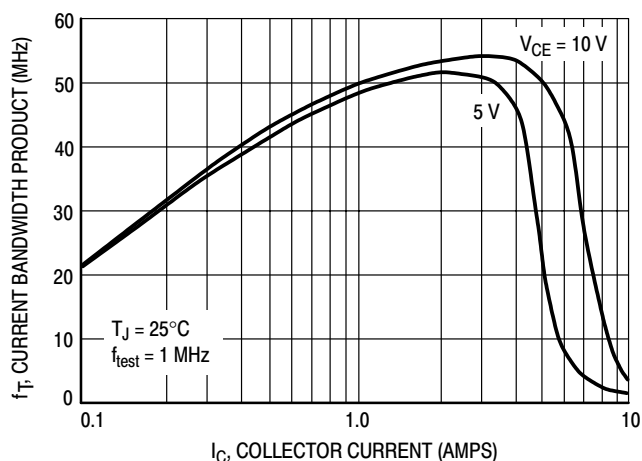
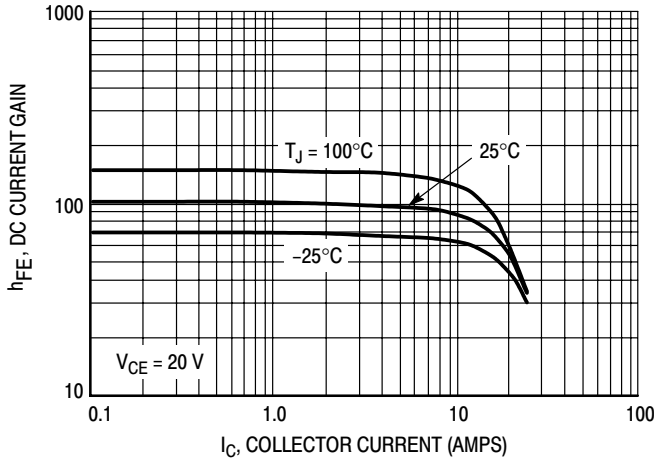


Figure 20. Typical Current Gain Bandwidth Product

# MJW3281A (NPN) MJW1302A (PNP)

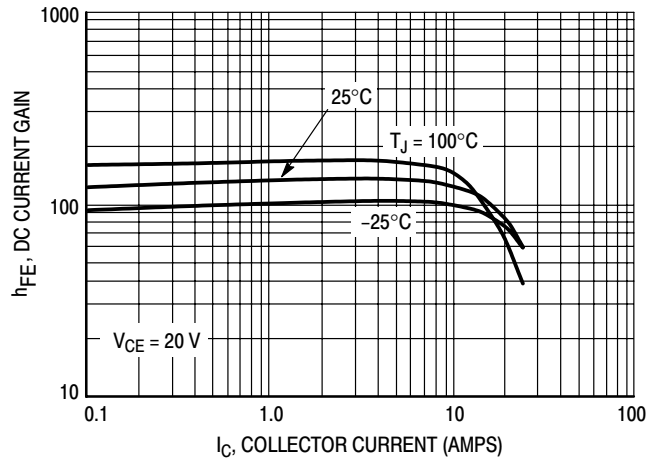
## TYPICAL CHARACTERISTICS

**PNP MJW1302A**



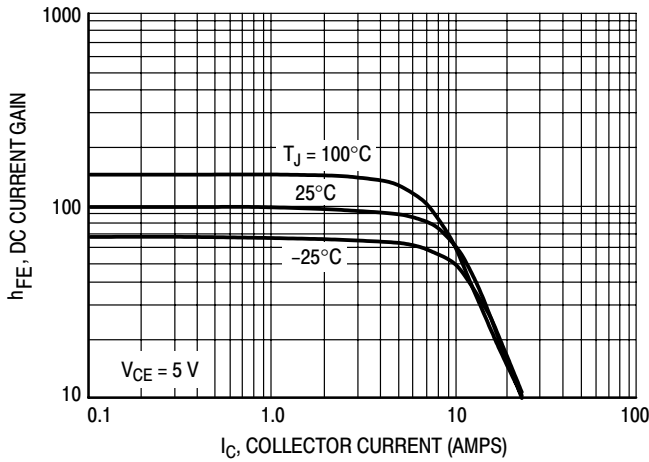
**Figure 21. DC Current Gain,  $V_{CE} = 20\text{ V}$**

**NPN MJW3281A**



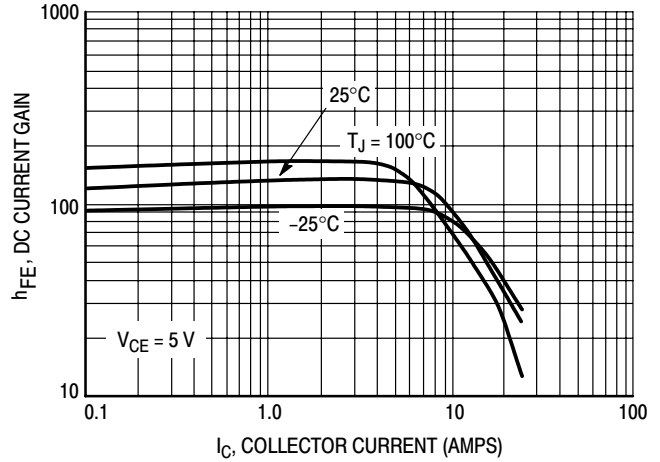
**Figure 22. DC Current Gain,  $V_{CE} = 20\text{ V}$**

**PNP MJW1302A**



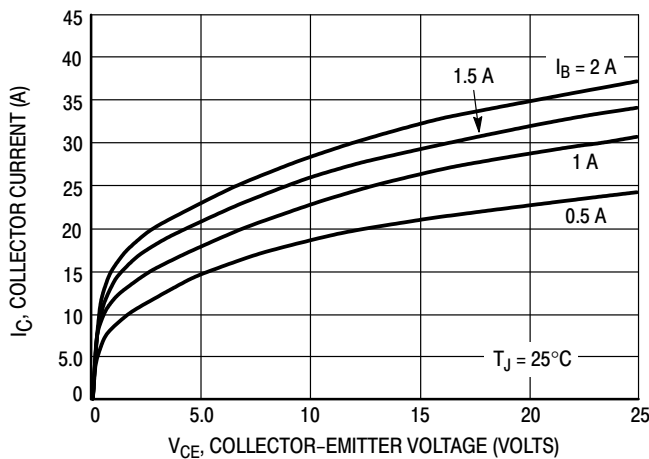
**Figure 23. DC Current Gain,  $V_{CE} = 5\text{ V}$**

**NPN MJW3281A**



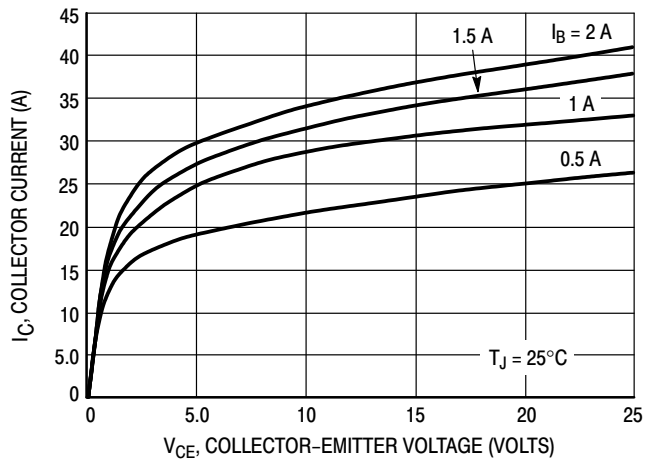
**Figure 24. DC Current Gain,  $V_{CE} = 5\text{ V}$**

**PNP MJW1302A**



**Figure 25. Typical Output Characteristics**

**NPN MJW3281A**



**Figure 26. Typical Output Characteristics**



# MJW3281A (NPN) MJW1302A (PNP)

## TYPICAL CHARACTERISTICS

PNP MJW1302A

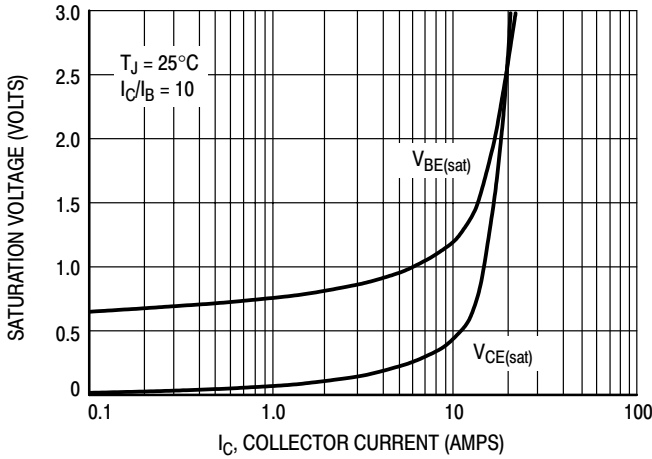


Figure 27. Typical Saturation Voltages

NPN MJW3281A

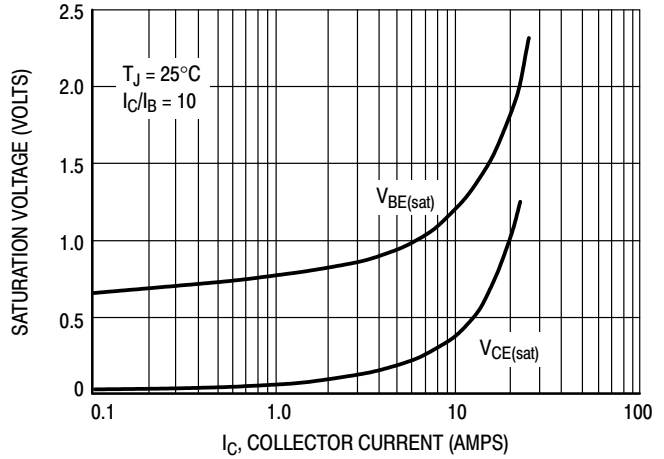


Figure 28. Typical Saturation Voltages

PNP MJW1302A

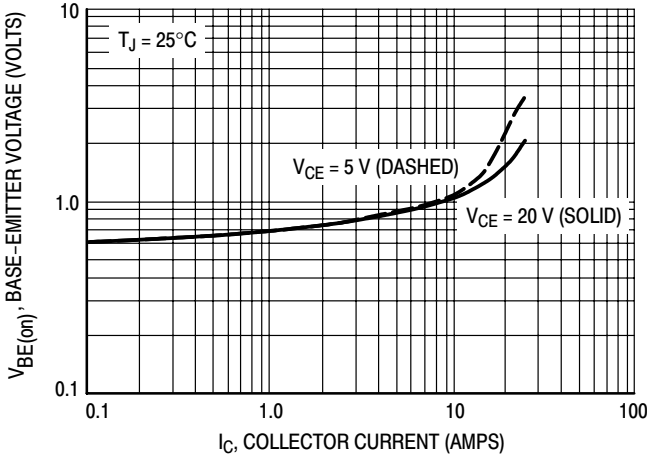


Figure 29. Typical Base-Emitter Voltage

NPN MJW3281A

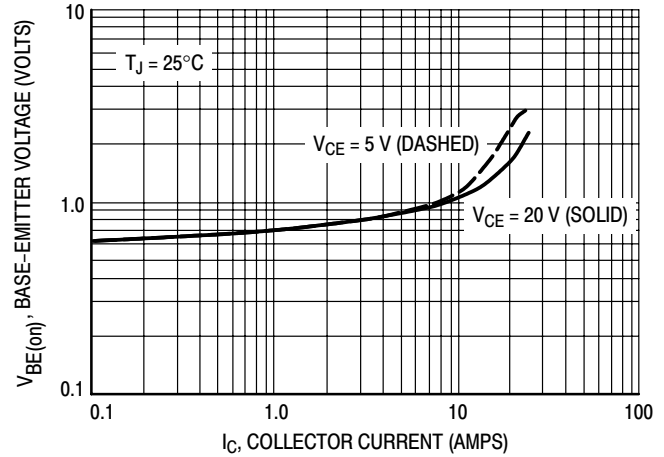


Figure 30. Typical Base-Emitter Voltage

PNP MJW1302A

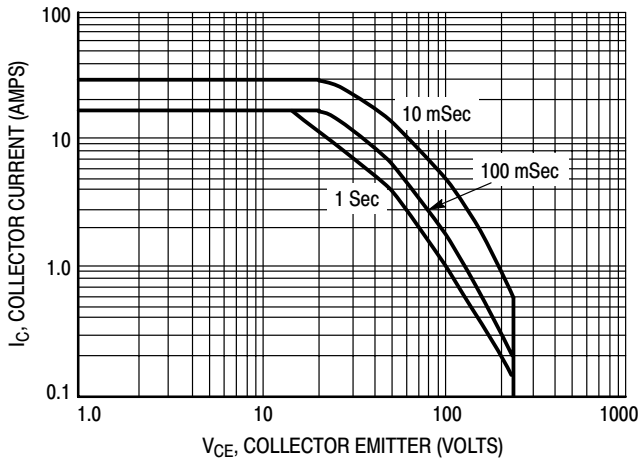


Figure 31. Active Region Safe Operating Area

NPN MJW3281A

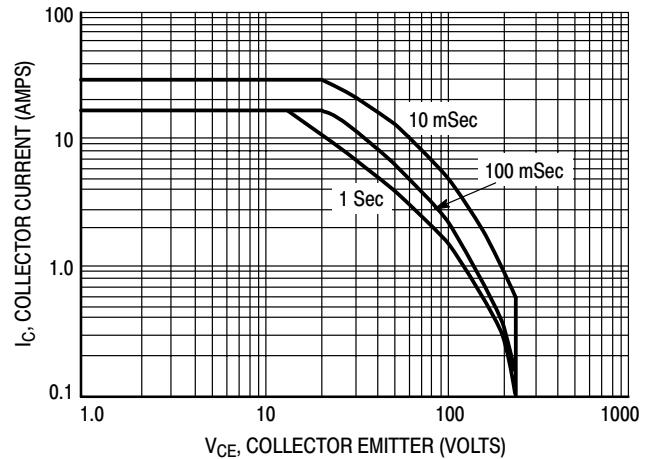


Figure 32. Active Region Safe Operating Area

## MJW3281A (NPN) MJW1302A (PNP)

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 31 and 32 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

### TYPICAL CHARACTERISTICS

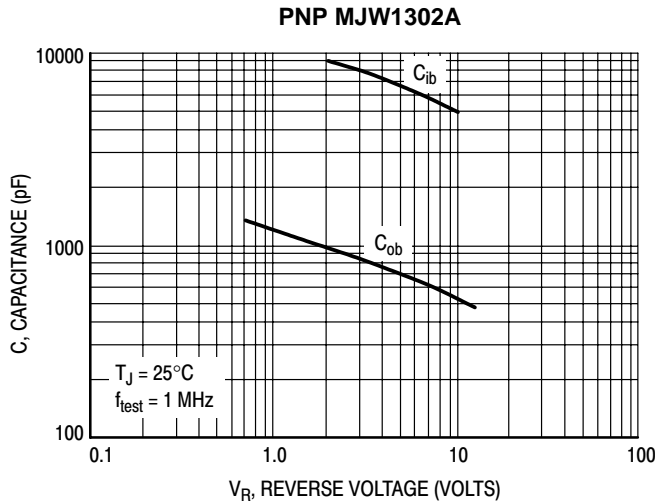


Figure 33. MJW1302A Typical Capacitance

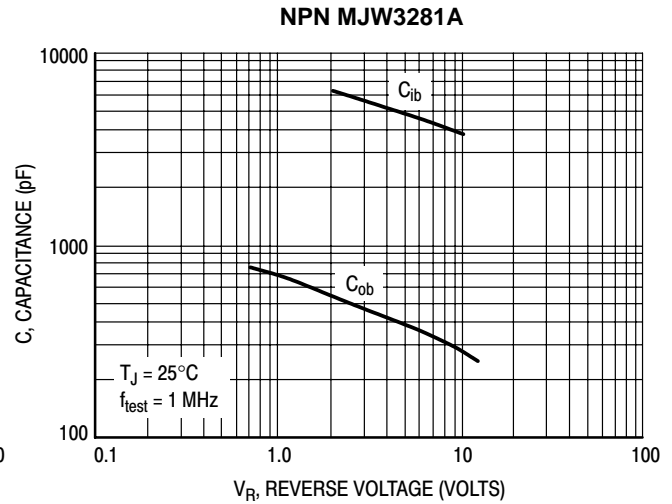
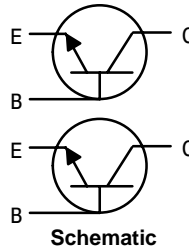


Figure 34. MJW3281A Typical Capacitance

# Plastic Power Transistors SO-8 for Surface Mount Applications

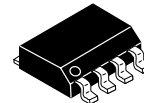
- Collector–Emitter Sustaining Voltage —  $V_{CEO(sus)}$   
= 30 Vdc (Min) @  $I_C = 10$  mAdc
- High DC Current Gain —  
 $h_{FE} = 85$  (Min) @  $I_C = 0.8$  Adc  
= 60 (Min) @  $I_C = 3.0$  Adc
- Low Collector–Emitter Saturation Voltage —  
 $V_{CE(sat)} = 0.18$  Vdc (Max) @  $I_C = 1.2$  Adc  
= 0.45 Vdc (Max) @  $I_C = 3.0$  Adc
- Miniature SO-8 Surface Mount Package – Saves Board Space



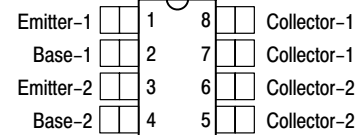
## MMDJ3N03BJT

ON Semiconductor Preferred Device

**DUAL BIPOLAR  
POWER TRANSISTOR  
NPN SILICON  
30 VOLTS  
3 AMPERES**



**CASE 751-07, Style 16  
(SO-8)**



Top View  
Pinout

### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Base Voltage	$V_{CB}$	45	Vdc
Collector–Emitter Voltage	$V_{CEO}$	30	Vdc
Emitter–Base Voltage	$V_{EB}$	$\pm 6.0$	Vdc
Collector Current — Continuous — Peak	$I_C$	3.0 5.0	Adc
Base Current — Continuous	$I_B$	1.0	Adc
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Ambient on 1" sq. (645 sq. mm) Collector pad on FR-4 board material with one die operating.	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 board material with one die operating.		185	
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ mounted on 1" sq. (645 sq. mm) Collector pad on FR-4 board material with one die operating. Derate above $25^\circ\text{C}$	$P_D$	1.25 10	Watts $\text{mW}/^\circ\text{C}$
Maximum Temperature for Soldering	$T_L$	260	$^\circ\text{C}$

**Preferred** devices are ON Semiconductor recommended choices for future use and best overall value.

# MMDJ3N03BJT

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0 A)	V <sub>CEO(sus)</sub>	30	—	—	Vdc
Emitter–Base Voltage (I <sub>E</sub> = 50 μA, I <sub>C</sub> = 0 A)	V <sub>EBO</sub>	6.0	—	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 25 Vdc, R <sub>BE</sub> = 200 Ω) (V <sub>CE</sub> = 25 Vdc, R <sub>BE</sub> = 200 Ω, T <sub>J</sub> = 125°C)	I <sub>CER</sub>	—	—	20 200	μA
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc)	I <sub>EBO</sub>	—	—	10	μA

### ON CHARACTERISTICS<sup>(1)</sup>

Collector–Emitter Saturation Voltage (I <sub>C</sub> = 0.8 A, I <sub>B</sub> = 20 mA) (I <sub>C</sub> = 1.2 A, I <sub>B</sub> = 20 mA) (I <sub>C</sub> = 3.0 A, I <sub>B</sub> = 0.3 A)	V <sub>CE(sat)</sub>	—	0.105	0.15 0.18 0.45	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 3.0 A, I <sub>B</sub> = 0.3 A)	V <sub>BE(sat)</sub>	—	—	1.25	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 1.2 A, V <sub>CE</sub> = 4.0 Vdc)	V <sub>BE(on)</sub>	—	—	1.10	Vdc
DC Current Gain (I <sub>C</sub> = 0.8 A, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 1.2 A, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 3.0 A, V <sub>CE</sub> = 1.0 Vdc)	h <sub>FE</sub>	85 80 60	195 — —	— — —	—

### DYNAMIC CHARACTERISTICS

Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0 A, f = 1.0 MHz)	C <sub>ob</sub>	—	85	135	pF
Input Capacitance (V <sub>EB</sub> = 8.0 Vdc)	C <sub>ib</sub>	—	200	—	pF
Current–Gain — Bandwidth Product <sup>(2)</sup> (I <sub>C</sub> = 500 mA, V <sub>CE</sub> = 10 Vdc, F <sub>test</sub> = 1.0 MHz)	f <sub>T</sub>	—	72	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) f<sub>T</sub> = |h<sub>FE</sub>| • f<sub>test</sub>

# MMDJ3N03BJT

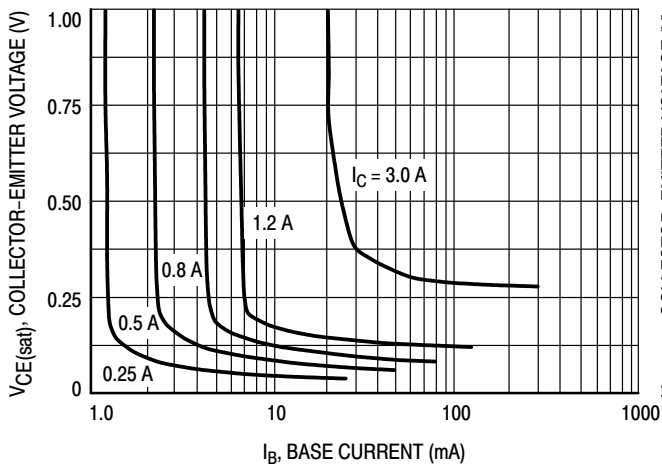


Figure 1. Collector Saturation Region

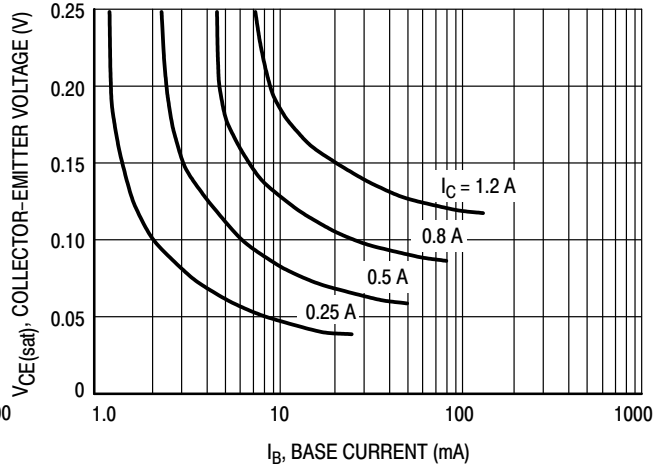


Figure 2. Collector Saturation Region

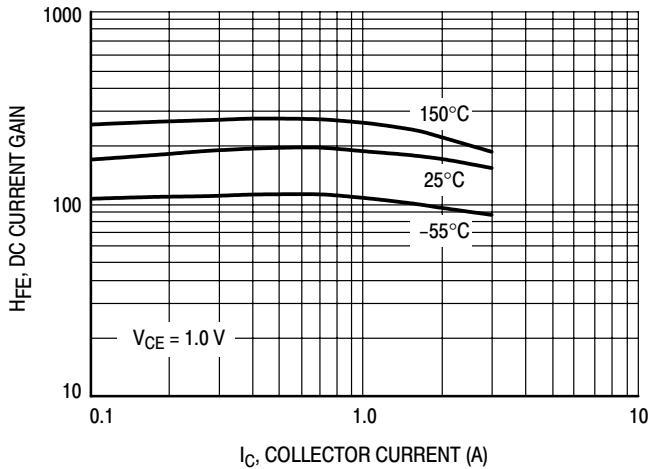


Figure 3. DC Current Gain

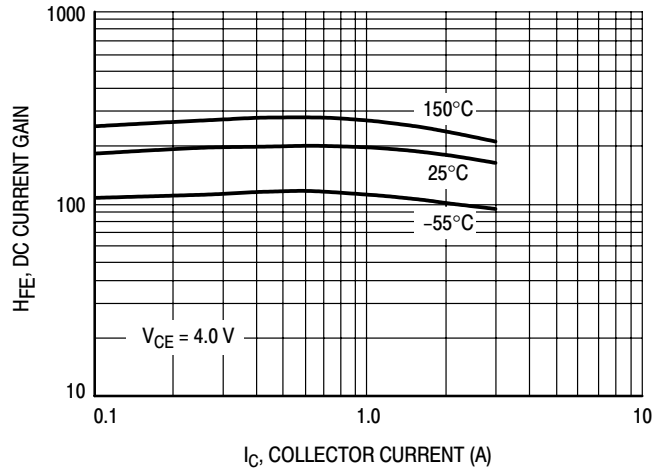


Figure 4. DC Current Gain

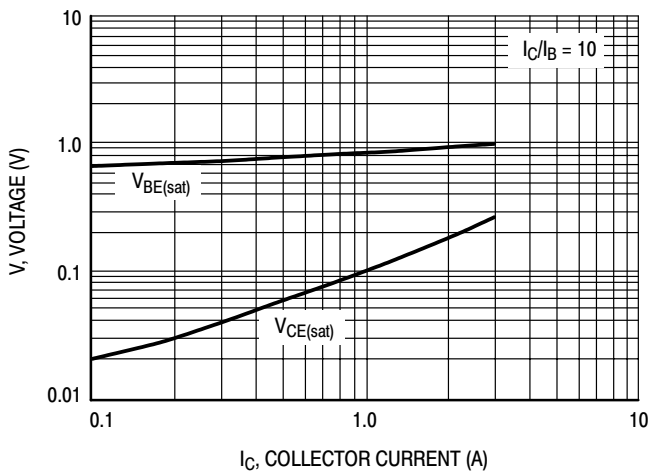


Figure 5. "On" Voltages

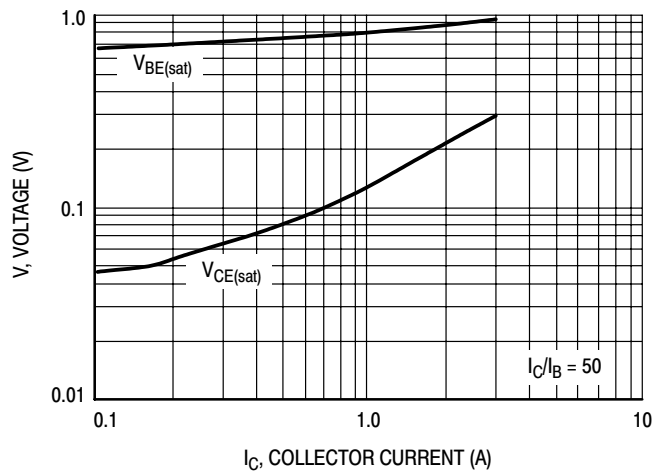


Figure 6. "On" Voltages

# MMDJ3N03BJT

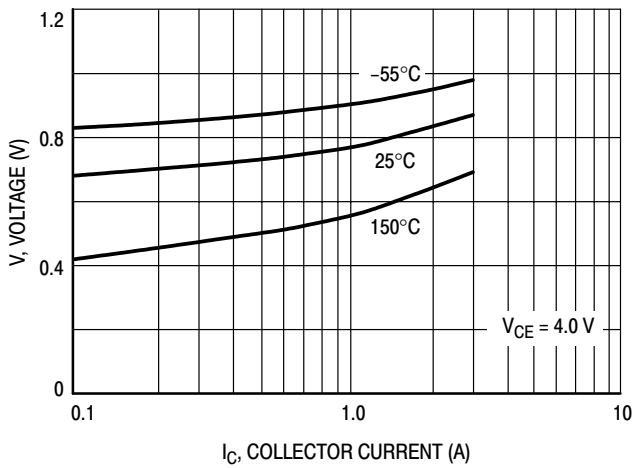


Figure 7.  $V_{BE(on)}$  Voltage

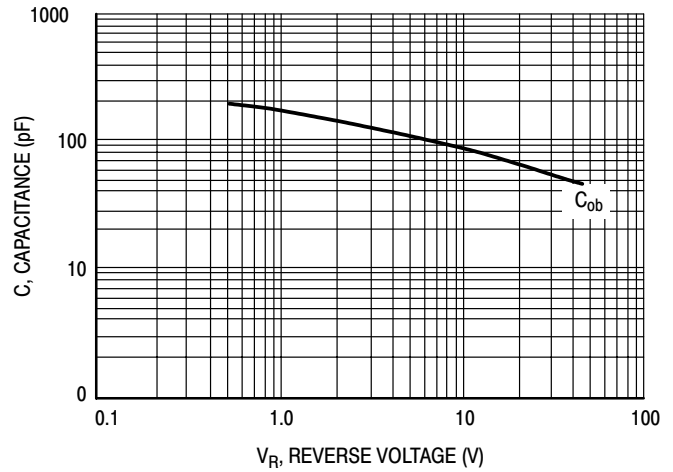


Figure 8. Capacitance

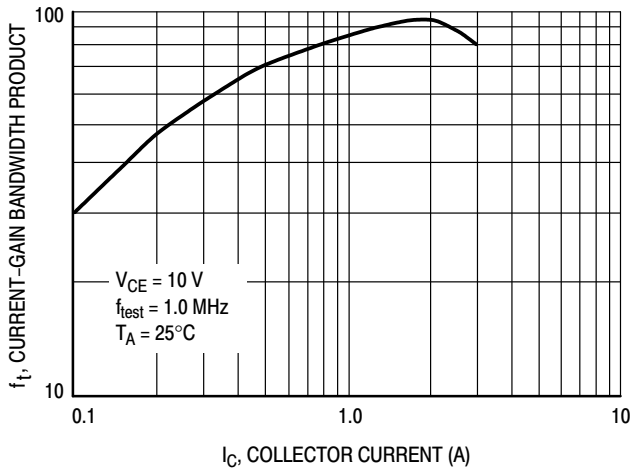


Figure 9. Current-Gain Bandwidth Product

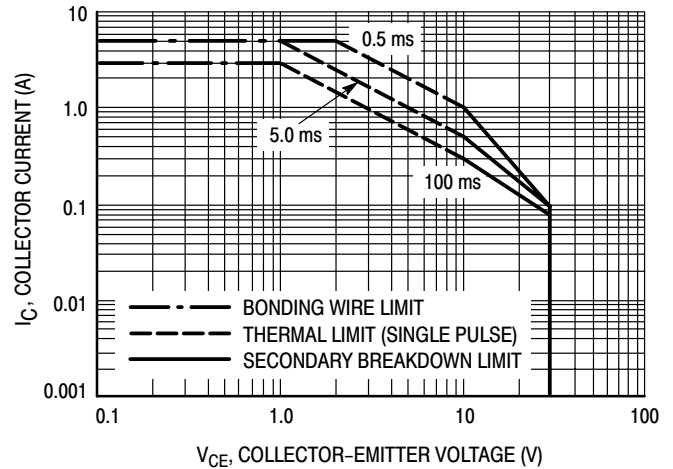


Figure 10. Active Region Safe Operating Area

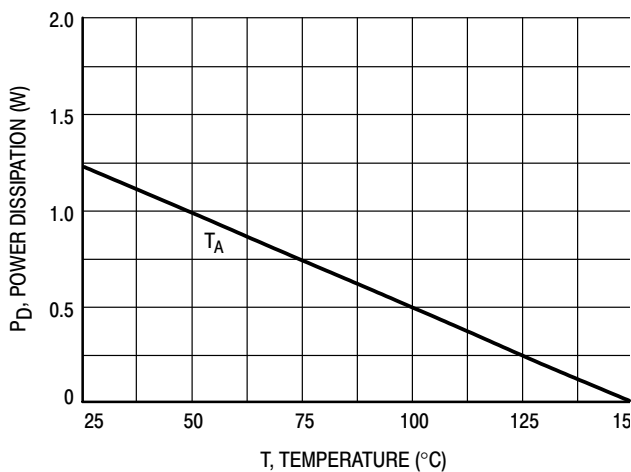


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

# MMDJ3N03BJT

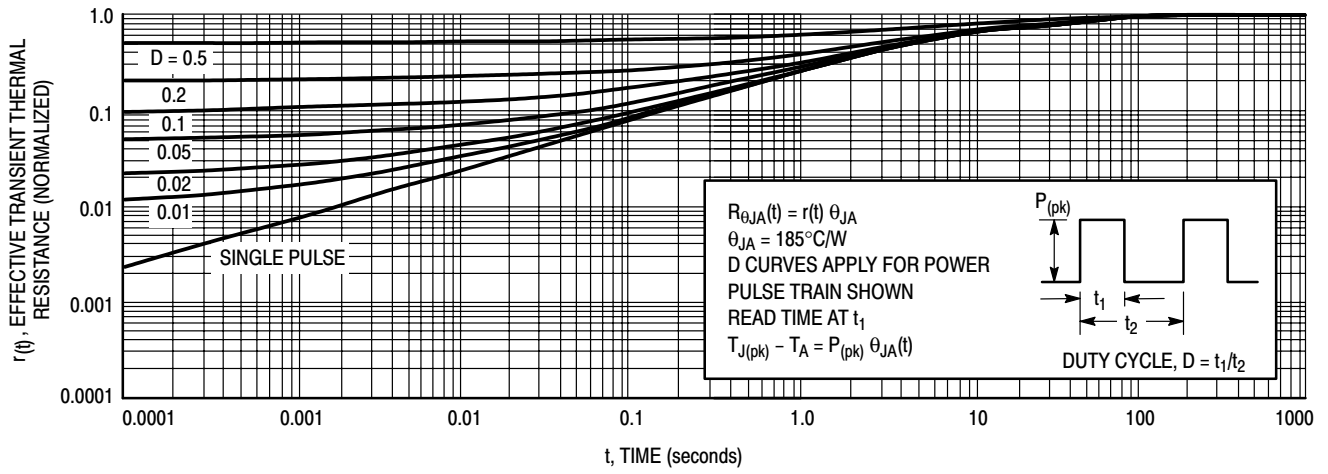
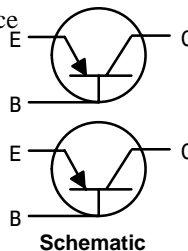


Figure 12. Thermal Response

# Plastic Power Transistors SO-8 for Surface Mount Applications

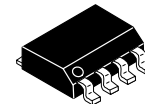
- Collector–Emitter Sustaining Voltage —  
 $V_{CE(sus)} = 30 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain —  
 $h_{FE} = 125 \text{ (Min) @ } I_C = 0.8 \text{ Adc}$   
 $= 90 \text{ (Min) @ } I_C = 3.0 \text{ Adc}$
- Low Collector–Emitter Saturation Voltage —  
 $V_{CE(sat)} = 0.24 \text{ Vdc (Max) @ } I_C = 1.2 \text{ Adc}$   
 $= 0.55 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- Miniature SO-8 Surface Mount Package – Saves Board Space



## MMDJ3P03BJT

ON Semiconductor Preferred Device

**DUAL BIPOLAR  
POWER TRANSISTOR  
PNP SILICON  
30 VOLTS  
3 AMPERES**



**CASE 751-07, Style 16  
(SO-8)**

Emitter-1	1	8	Collector-1
Base-1	2	7	Collector-1
Emitter-2	3	6	Collector-2
Base-2	4	5	Collector-2

Top View  
Pinout

### MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Base Voltage	V <sub>CB</sub>	45	Vdc
Collector–Emitter Voltage	V <sub>CEO</sub>	30	Vdc
Emitter–Base Voltage	V <sub>EB</sub>	±6.0	Vdc
Collector Current — Continuous — Peak	I <sub>C</sub>	3.0 5.0	Adc
Base Current — Continuous	I <sub>B</sub>	1.0	Adc
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–55 to +150	°C

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Ambient on 1" sq. (645 sq. mm) Collector pad on FR-4 board material with one die operating.	R <sub>θJA</sub>	100	°C/W
Thermal Resistance – Junction to Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 board material with one die operating.		185	
Total Power Dissipation @ T <sub>A</sub> = 25°C mounted on 1" sq. (645 sq. mm) Collector pad on FR-4 board material with one die operating. Derate above 25°C	P <sub>D</sub>	1.25 10	Watts mW/°C
Maximum Temperature for Soldering	T <sub>L</sub>	260	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.



# MMDJ3P03BJT

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 10\text{ mA}$ , $I_B = 0\text{ A}$ )	$V_{CE(sus)}$	30	—	—	Vdc
Emitter–Base Voltage ( $I_E = 50\text{ }\mu\text{A}$ , $I_C = 0\text{ A}$ )	$V_{EBO}$	6.0	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = 25\text{ Vdc}$ , $R_{BE} = 200\text{ }\Omega$ ) ( $V_{CE} = 25\text{ Vdc}$ , $R_{BE} = 200\text{ }\Omega$ , $T_J = 125^\circ\text{C}$ )	$I_{CER}$	— —	— —	20 200	$\mu\text{A}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ )	$I_{EBO}$	—	—	10	$\mu\text{A}$

### ON CHARACTERISTICS<sup>(1)</sup>

Collector–Emitter Saturation Voltage ( $I_C = 0.8\text{ A}$ , $I_B = 20\text{ mA}$ ) ( $I_C = 1.2\text{ A}$ , $I_B = 20\text{ mA}$ ) ( $I_C = 3.0\text{ A}$ , $I_B = 0.3\text{ A}$ )	$V_{CE(sat)}$	— — —	0.15 — —	0.21 0.24 0.55	Vdc
Base–Emitter Saturation Voltage ( $I_C = 3.0\text{ A}$ , $I_B = 0.3\text{ A}$ )	$V_{BE(sat)}$	—	—	1.25	Vdc
Base–Emitter On Voltage ( $I_C = 1.2\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	—	1.10	Vdc
DC Current Gain ( $I_C = 0.8\text{ A}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 1.2\text{ A}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ A}$ , $V_{CE} = 1.0\text{ Vdc}$ )	$h_{FE}$	125 110 90	260 — —	— — —	—

### DYNAMIC CHARACTERISTICS

Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0\text{ A}$ , $f = 1.0\text{ MHz}$ )	$C_{ob}$	—	100	150	pF
Input Capacitance ( $V_{EB} = 8.0\text{ Vdc}$ )	$C_{ib}$	—	135	—	pF
Current–Gain — Bandwidth Product <sup>(2)</sup> ( $I_C = 500\text{ mA}$ , $V_{CE} = 10\text{ V}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	—	110	—	MHz

(1) Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

(2)  $f_T = |h_{FE}| \cdot f_{test}$

# MMDJ3P03BJT

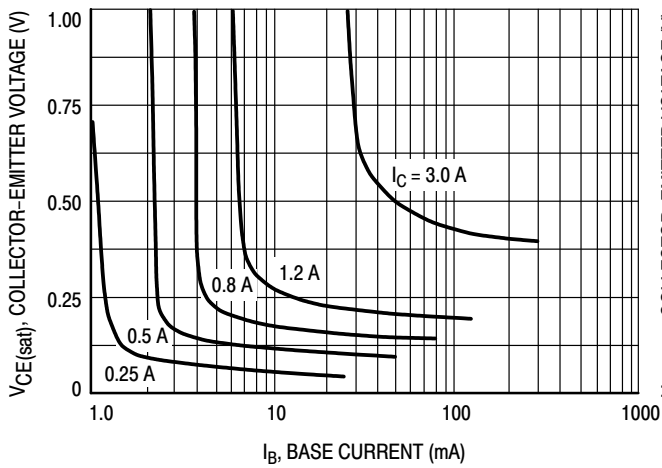


Figure 1. Collector Saturation Region

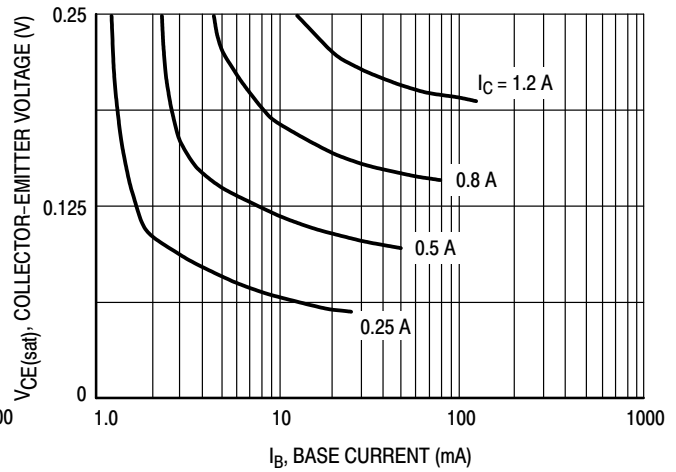


Figure 2. Collector Saturation Region

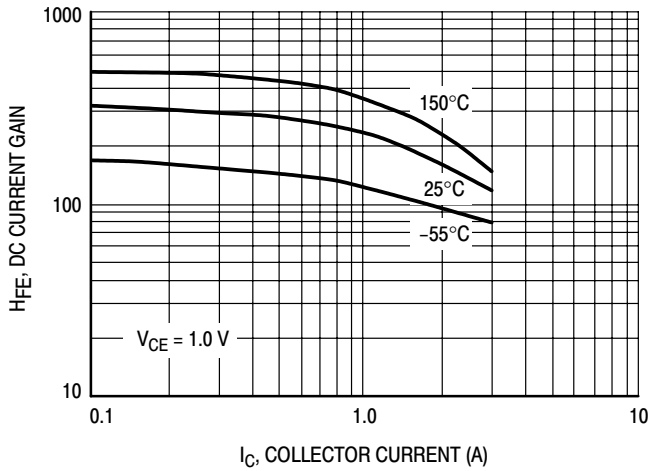


Figure 3. DC Current Gain

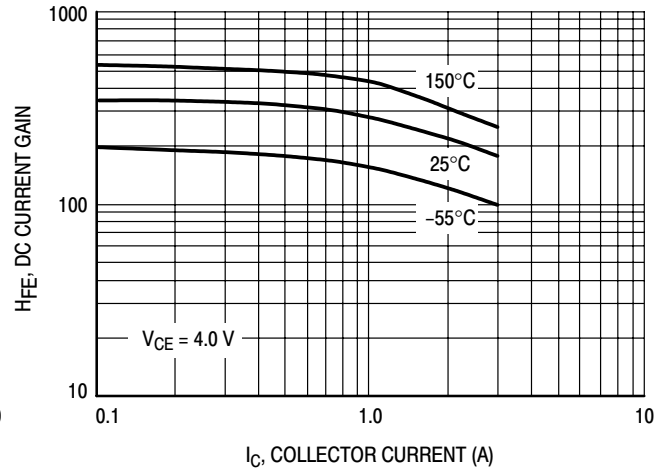


Figure 4. DC Current Gain

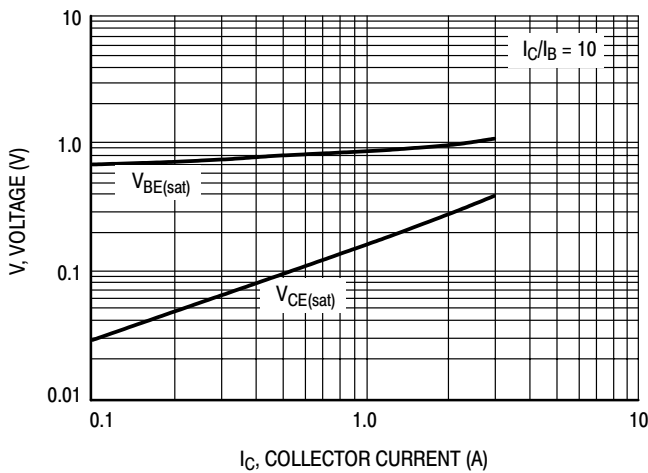


Figure 5. "On" Voltages

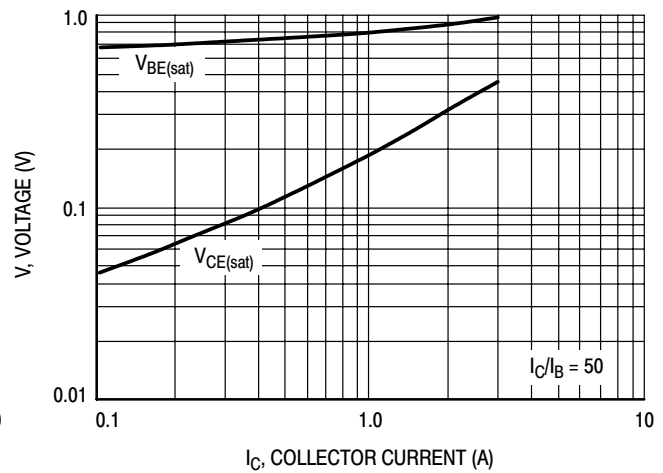


Figure 6. "On" Voltages

# MMDJ3P03BJT

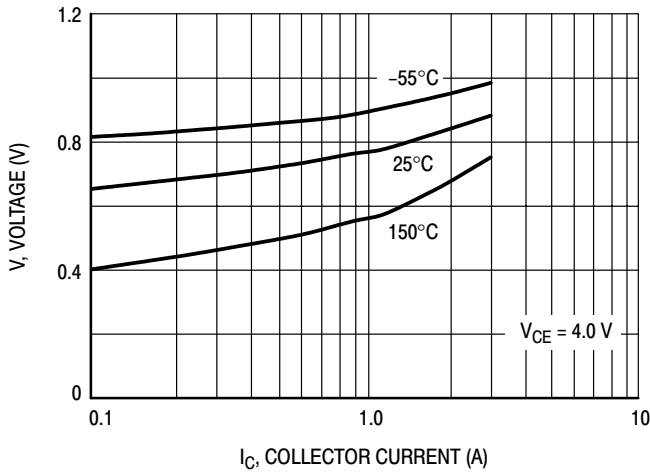


Figure 7.  $V_{BE(on)}$  Voltage

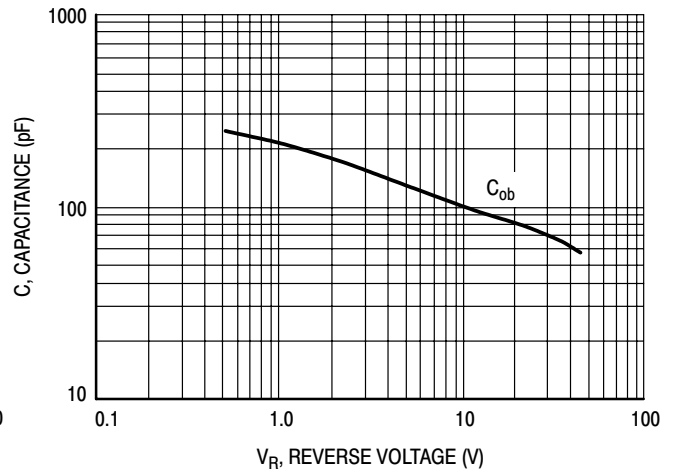


Figure 8. Output Capacitance

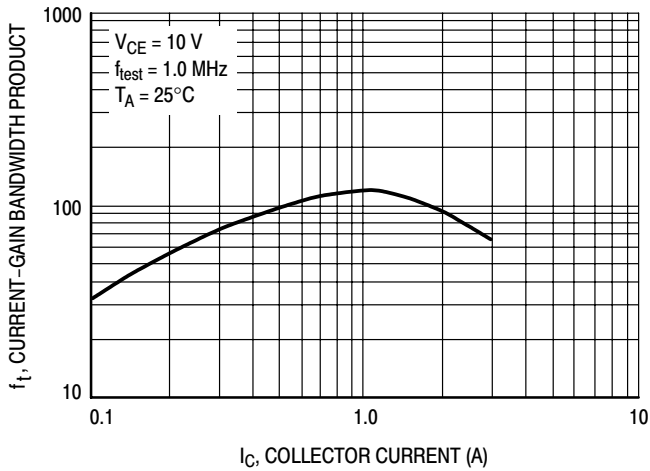


Figure 9. Current-Gain Bandwidth Product

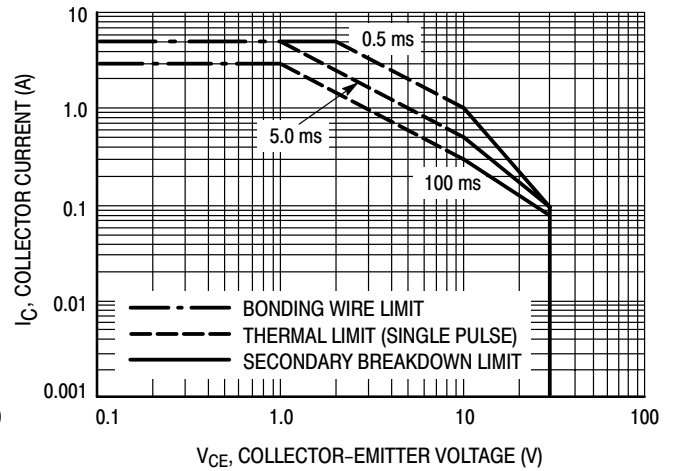


Figure 10. Active Region Safe Operating Area

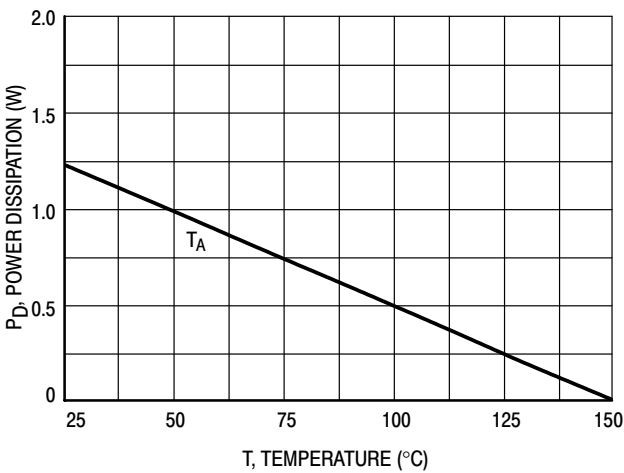


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

# MMDJ3P03BJT

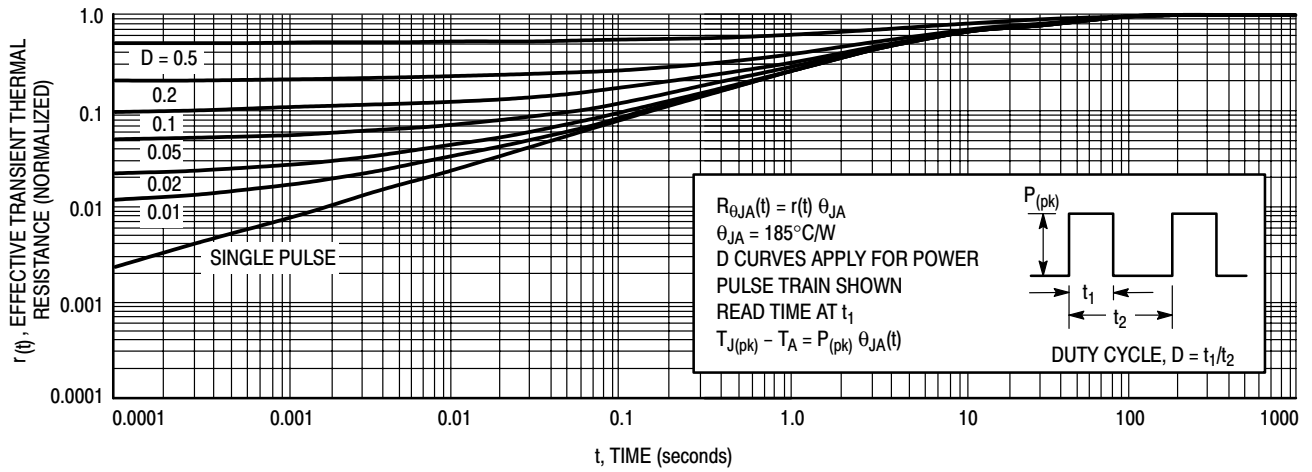


Figure 12. Thermal Response

# Bipolar Power Transistors

## PNP Silicon

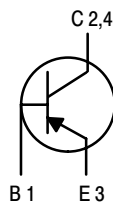
... designed for use in line-operated applications such as low power, line-operated series pass and switching regulators requiring PNP capability.

- High Collector–Emitter Sustaining Voltage —

$$V_{CEO(sus)} = 300 \text{ Vdc @ } I_C = 1.0 \text{ mAdc}$$

- Excellent DC Current Gain —

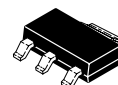
$$h_{FE} = 30\text{--}240 @ I_C = 50 \text{ mAdc}$$



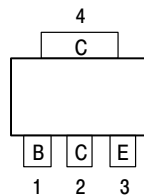
Schematic

# MMJT350T1

**0.5 AMPERE  
POWER TRANSISTOR  
PNP SILICON  
300 VOLTS  
2.75 WATTS**



CASE 318E-04, Style 1



Top View Pinout

### MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V <sub>CEO</sub>	300	Vdc
Collector–Base Voltage	V <sub>CB</sub>	300	Vdc
Emitter–Base Voltage	V <sub>EB</sub>	3.0	Vdc
Collector Current — Continuous — Peak	I <sub>C</sub>	0.5 0.75	Adc
Total Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C Total P <sub>D</sub> @ T <sub>A</sub> = 25°C mounted on 1" sq. (645 sq. mm) Collector pad on FR-4 bd material Total P <sub>D</sub> @ T <sub>A</sub> = 25°C mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 bd material	P <sub>D</sub>	2.75 22 1.40 0.65	Watts mW/°C Watts Watts
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Case – Junction to Ambient on 1" sq. (645 sq. mm) Collector pad on FR-4 bd material – Junction to Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 bd material	R <sub>θJC</sub> R <sub>θJA</sub> R <sub>θJA</sub>	45 85 190	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T <sub>L</sub>	260	°C

# MMJT350T1

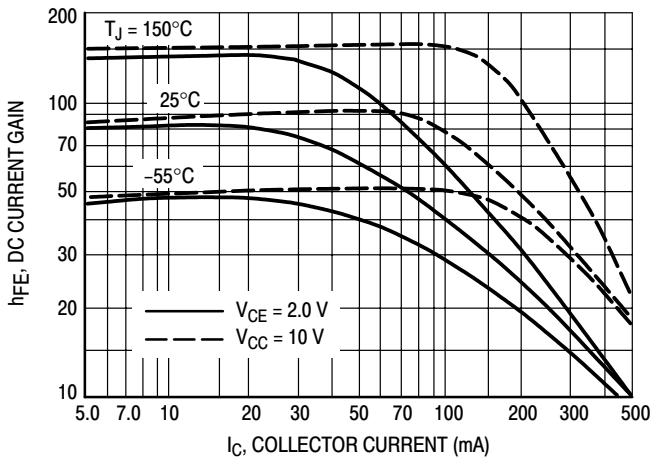


Figure 1. DC Current Gain

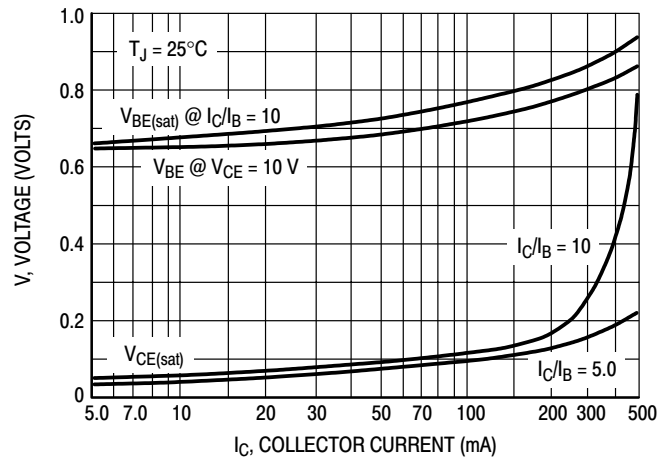


Figure 2. "On" Voltages

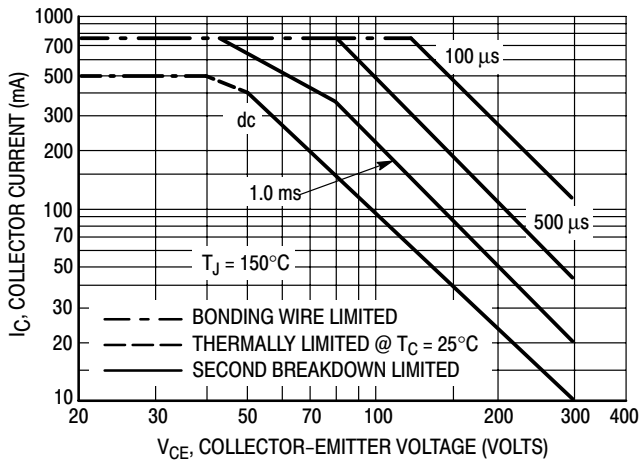


Figure 3. Active-Region Safe Operating Area

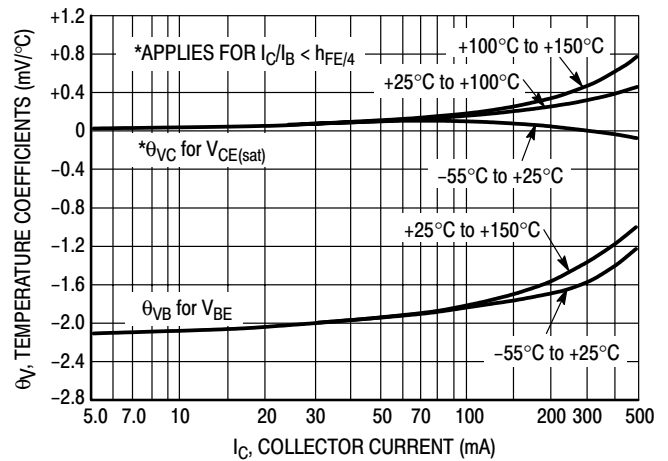


Figure 4. Temperature Coefficients

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

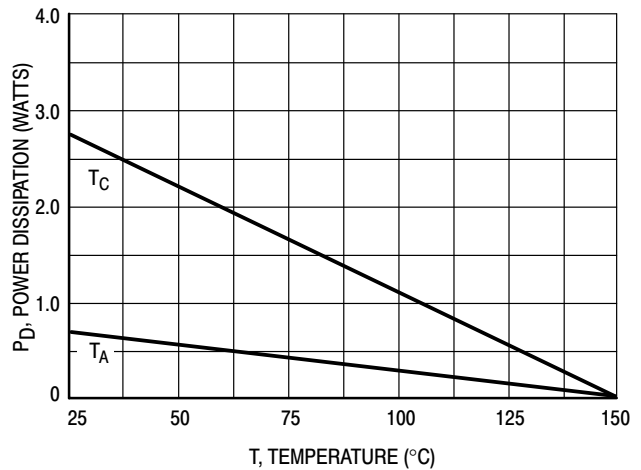


Figure 5. Power Derating

# Bipolar Power Transistors

## NPN Silicon

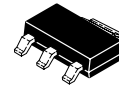
- Collector–Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 30 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain —  
 $h_{FE} = 85 \text{ (Min) @ } I_C = 0.8 \text{ Adc}$   
 $= 60 \text{ (Min) @ } I_C = 3.0 \text{ Adc}$
- Low Collector–Emitter Saturation Voltage —  
 $V_{CE(sat)} = 0.2 \text{ Vdc (Max) @ } I_C = 1.2 \text{ Adc}$   
 $= 0.45 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- SOT–223 Surface Mount Packaging



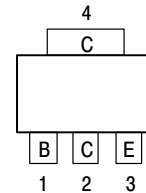
# MMJT9410

ON Semiconductor Preferred Device

**POWER BJT**  
 $I_C = 3.0 \text{ AMPERES}$   
 $BV_{CEO} = 30 \text{ VOLTS}$   
 $V_{CE(sat)} = 0.2 \text{ VOLTS}$



CASE 318E–04, Style 1



### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	30	Vdc
Collector–Base Voltage	$V_{CB}$	45	Vdc
Emitter–Base Voltage	$V_{EB}$	$\pm 6.0$	Vdc
Base Current — Continuous	$I_B$	1.0	Adc
Collector Current — Continuous — Peak	$I_C$	3.0 5.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$ Total $P_D$ @ $T_A = 25^\circ\text{C}$ mounted on 1" sq. (645 sq. mm) Collector pad on FR–4 bd material Total $P_D$ @ $T_A = 25^\circ\text{C}$ mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR–4 bd material	$P_D$	3.0 24 1.7 0.75	Watts mW/°C Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–55 to +150	°C

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Case – Junction to Ambient on 1" sq. (645 sq. mm) Collector pad on FR–4 bd material – Junction to Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR–4 bd material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	42 75 165	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	$T_L$	260	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MMJT9410

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0 A)	V <sub>CEO(sus)</sub>	30	—	—	Vdc
Emitter–Base Voltage (I <sub>E</sub> = 50 μA, I <sub>C</sub> = 0 A)	V <sub>EBO</sub>	6.0	—	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 25 Vdc, R <sub>BE</sub> = 200 Ω) (V <sub>CE</sub> = 25 Vdc, R <sub>BE</sub> = 200 Ω, T <sub>J</sub> = 125°C)	I <sub>CER</sub>	—	—	20 200	μA
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc)	I <sub>EBO</sub>	—	—	10	μA

### ON CHARACTERISTICS<sup>(1)</sup>

Collector–Emitter Saturation Voltage (I <sub>C</sub> = 0.8 A, I <sub>B</sub> = 20 mA) (I <sub>C</sub> = 1.2 A, I <sub>B</sub> = 20 mA) (I <sub>C</sub> = 3.0 A, I <sub>B</sub> = 0.3 A)	V <sub>CE(sat)</sub>	—	0.105 0.150 —	0.150 0.200 0.450	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 3.0 A, I <sub>B</sub> = 0.3 A)	V <sub>BE(sat)</sub>	—	—	1.25	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 1.2 A, V <sub>CE</sub> = 4.0 Vdc)	V <sub>BE(on)</sub>	—	—	1.10	Vdc
DC Current Gain (I <sub>C</sub> = 0.8 A, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 1.2 A, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 3.0 A, V <sub>CE</sub> = 1.0 Vdc)	h <sub>FE</sub>	85 80 60	200 — —	— — —	—

### DYNAMIC CHARACTERISTICS

Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0 A, f = 1.0 MHz)	C <sub>ob</sub>	—	85	135	pF
Input Capacitance (V <sub>EB</sub> = 8.0 Vdc)	C <sub>ib</sub>	—	200	—	pF
Current–Gain — Bandwidth Product <sup>(2)</sup> (I <sub>C</sub> = 500 mA, V <sub>CE</sub> = 10 Vdc, F <sub>test</sub> = 1.0 MHz)	f <sub>T</sub>	—	72	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) f<sub>T</sub> = |h<sub>FE</sub>| • f<sub>test</sub>



# MMJT9410

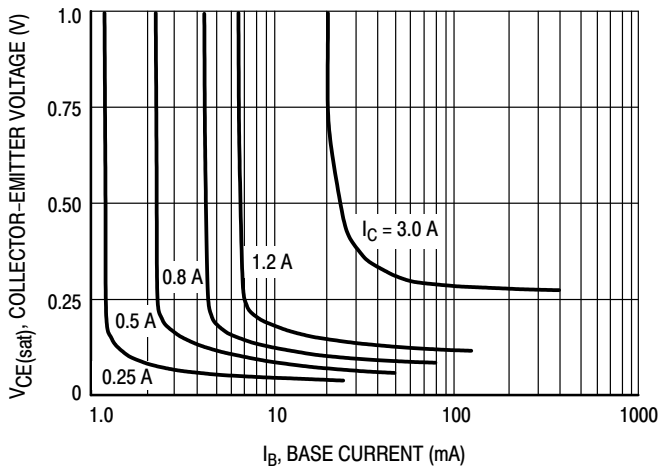


Figure 1. Collector Saturation Region

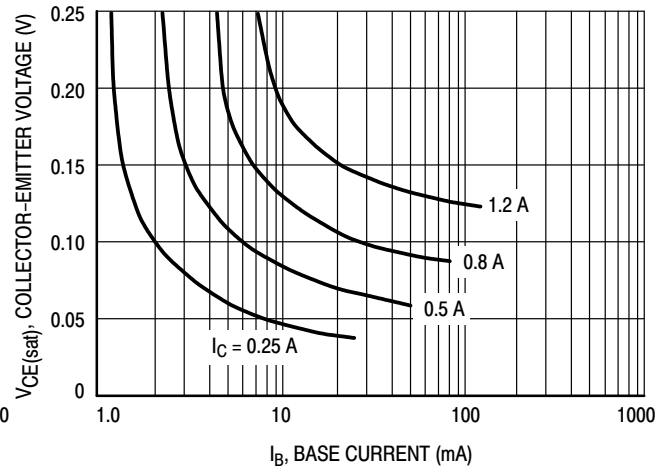


Figure 2. Collector Saturation Region

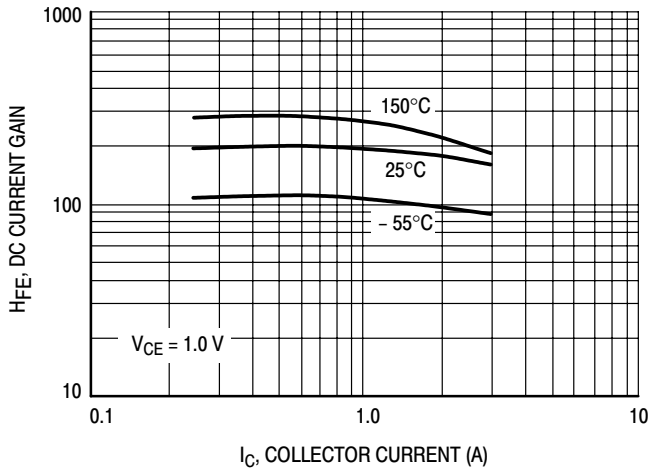


Figure 3. DC Current Gain

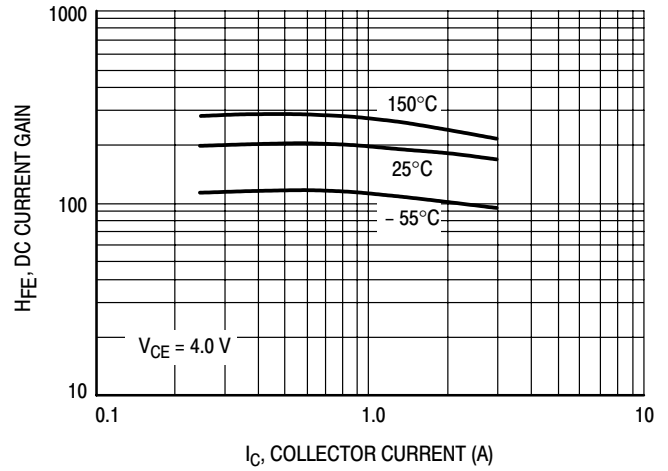


Figure 4. DC Current Gain

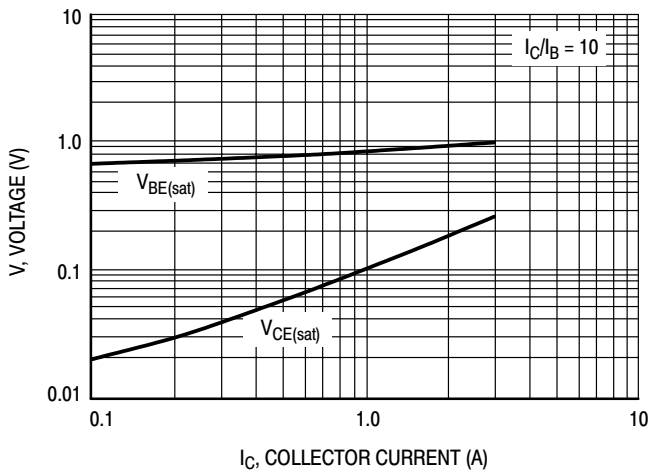


Figure 5. "On" Voltages

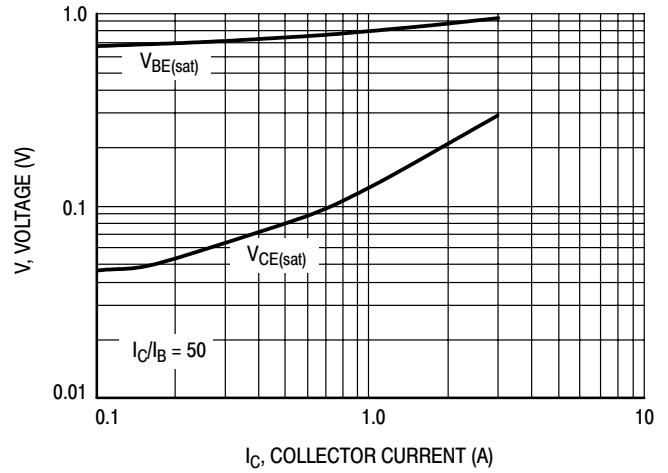


Figure 6. "On" Voltages

# MMJT9410

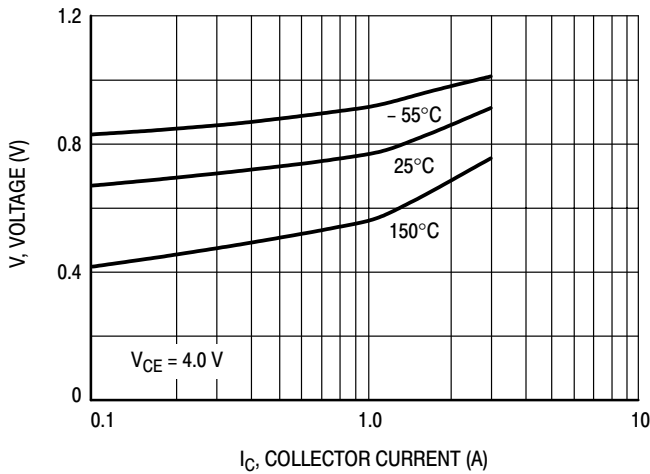


Figure 7.  $V_{BE(on)}$  Voltage

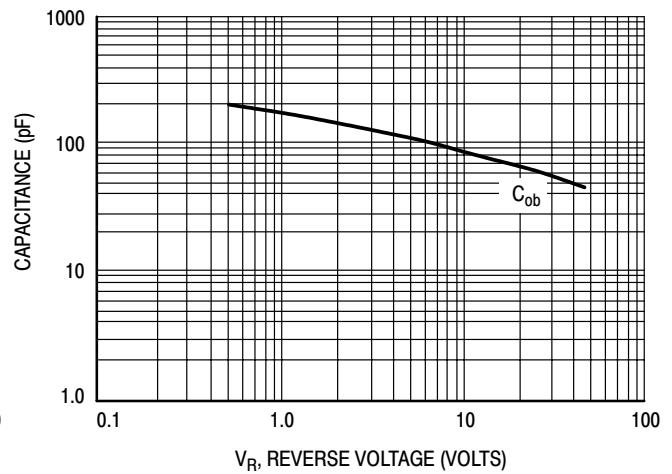


Figure 8. Capacitance

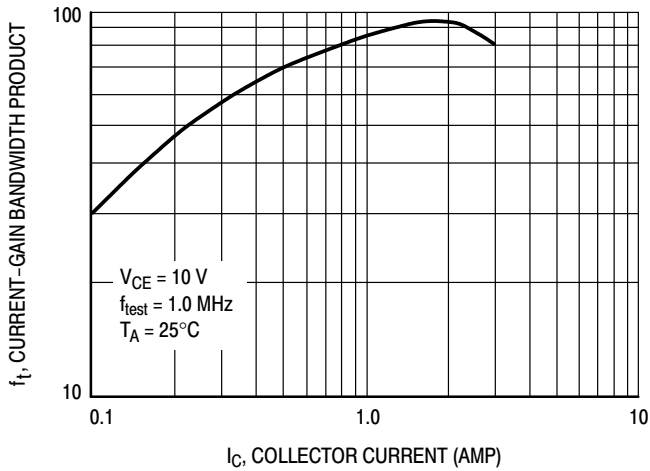


Figure 9. Current-Gain Bandwidth Product

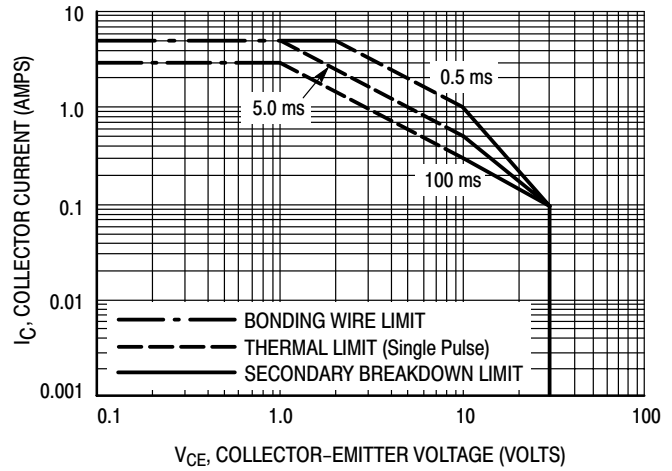


Figure 10. Active Region Safe Operating Area

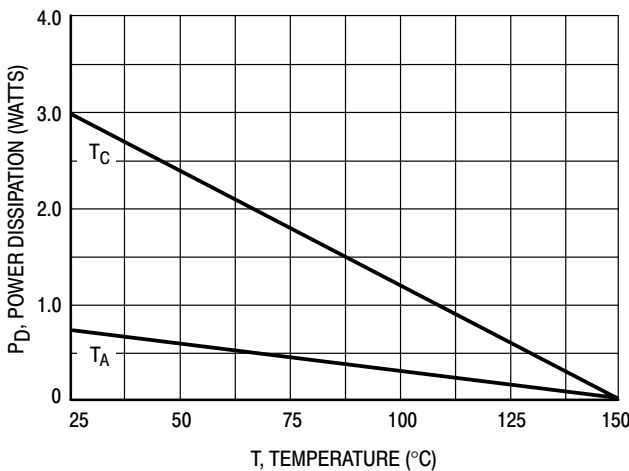


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

# MMJT9410

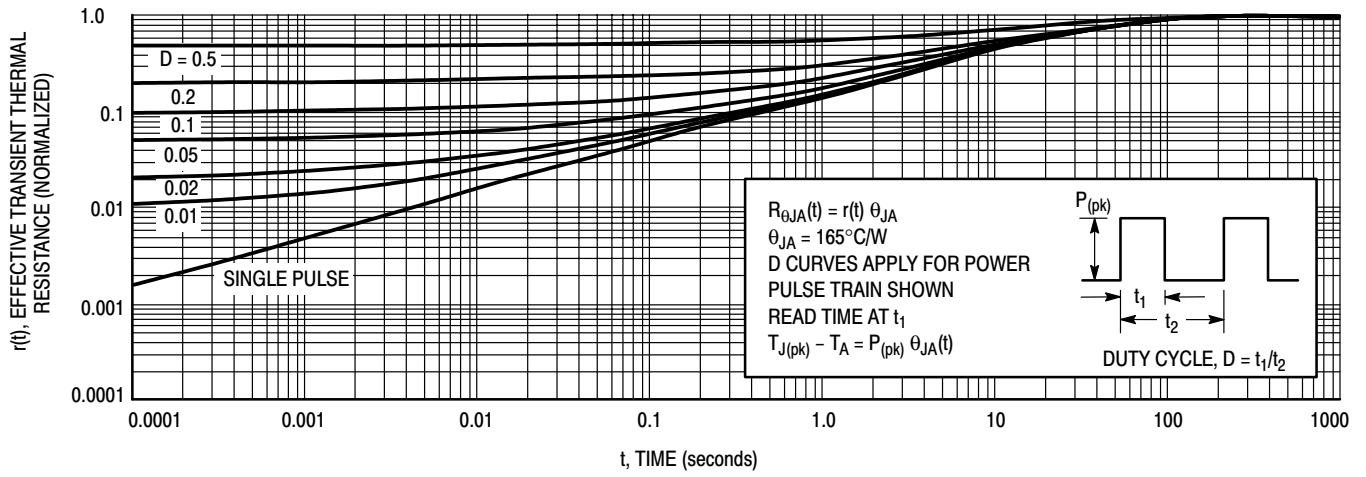


Figure 12. Thermal Response

# Bipolar Power Transistors

## PNP Silicon

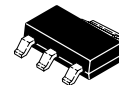
- Collector–Emitter Sustaining Voltage —  
 $V_{CE(sus)} = 30 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain —  
 $h_{FE} = 125 \text{ (Min) @ } I_C = 0.8 \text{ Adc}$   
 $= 90 \text{ (Min) @ } I_C = 3.0 \text{ Adc}$
- Low Collector–Emitter Saturation Voltage —  
 $V_{CE(sat)} = 0.275 \text{ Vdc (Max) @ } I_C = 1.2 \text{ Adc}$   
 $= 0.55 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- SOT–223 Surface Mount Packaging



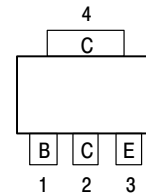
# MMJT9435

ON Semiconductor Preferred Device

**POWER BJT**  
 $I_C = 3.0 \text{ AMPERES}$   
 $BV_{CEO} = 30 \text{ VOLTS}$   
 $V_{CE(sat)} = 0.275 \text{ VOLTS}$



CASE 318E–04, Style 1



### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	30	Vdc
Collector–Base Voltage	$V_{CB}$	45	Vdc
Emitter–Base Voltage	$V_{EB}$	$\pm 6.0$	Vdc
Base Current — Continuous	$I_B$	1.0	Adc
Collector Current — Continuous — Peak	$I_C$	3.0 5.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$ Total $P_D$ @ $T_A = 25^\circ\text{C}$ mounted on 1" sq. (645 sq. mm) Collector pad on FR–4 bd material Total $P_D$ @ $T_A = 25^\circ\text{C}$ mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR–4 bd material	$P_D$	3.0 24 1.56 0.72	Watts mW/ $^\circ\text{C}$ Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	$-55$ to $+150$	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Case – Junction to Ambient on 1" sq. (645 sq. mm) Collector pad on FR–4 bd material – Junction to Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR–4 bd material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	42 80 174	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	$T_L$	260	$^\circ\text{C}$

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# MMJT9435

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0 A)	V <sub>CEO(sus)</sub>	30	—	—	Vdc
Emitter–Base Voltage (I <sub>E</sub> = 50 μA, I <sub>C</sub> = 0 A)	V <sub>EBO</sub>	6.0	—	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 25 Vdc, R <sub>BE</sub> = 200 Ω) (V <sub>CE</sub> = 25 Vdc, R <sub>BE</sub> = 200 Ω, T <sub>J</sub> = 125°C)	I <sub>CER</sub>	—	—	20 200	μA
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc)	I <sub>EBO</sub>	—	—	10	μA

### ON CHARACTERISTICS<sup>(1)</sup>

Collector–Emitter Saturation Voltage (I <sub>C</sub> = 0.8 A, I <sub>B</sub> = 20 mA) (I <sub>C</sub> = 1.2 A, I <sub>B</sub> = 20 mA) (I <sub>C</sub> = 3.0 A, I <sub>B</sub> = 0.3 A)	V <sub>CE(sat)</sub>	—	0.155	0.210 0.275 0.550	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 3.0 A, I <sub>B</sub> = 0.3 A)	V <sub>BE(sat)</sub>	—	—	1.25	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 1.2 A, V <sub>CE</sub> = 4.0 Vdc)	V <sub>BE(on)</sub>	—	—	1.10	Vdc
DC Current Gain (I <sub>C</sub> = 0.8 A, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 1.2 A, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 3.0 A, V <sub>CE</sub> = 1.0 Vdc)	h <sub>FE</sub>	125 110 90	220 — —	— — —	—

### DYNAMIC CHARACTERISTICS

Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0 A, f = 1.0 MHz)	C <sub>ob</sub>	—	100	150	pF
Input Capacitance (V <sub>EB</sub> = 8.0 Vdc)	C <sub>ib</sub>	—	135	—	pF
Current–Gain — Bandwidth Product <sup>(2)</sup> (I <sub>C</sub> = 500 mA, V <sub>CE</sub> = 10 V, F <sub>test</sub> = 1.0 MHz)	f <sub>T</sub>	—	110	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) f<sub>T</sub> = |h<sub>FE</sub>| • f<sub>test</sub>

# MMJT9435

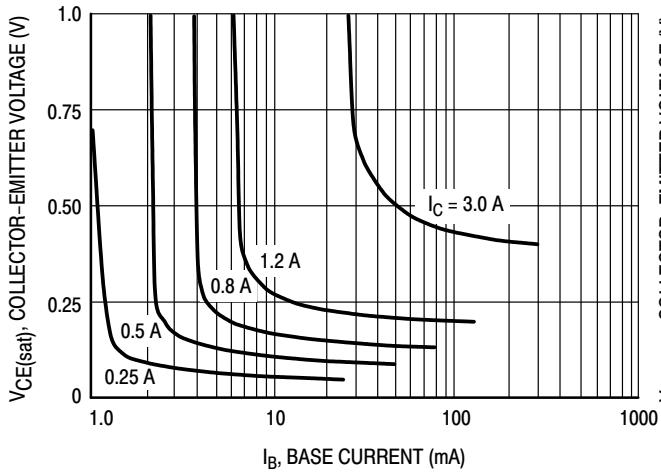


Figure 1. Collector Saturation Region

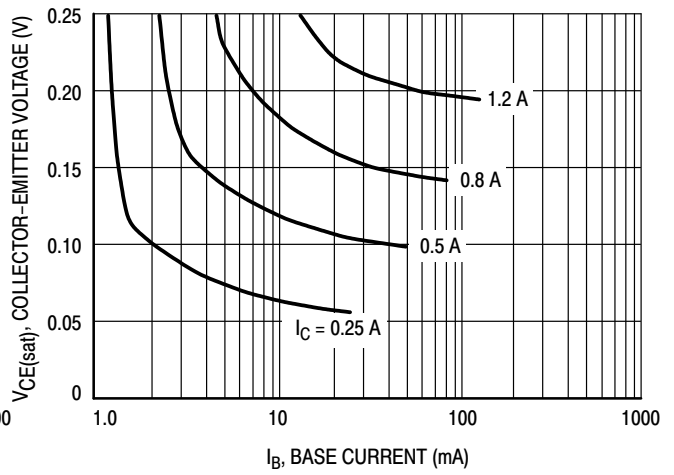


Figure 2. Collector Saturation Region

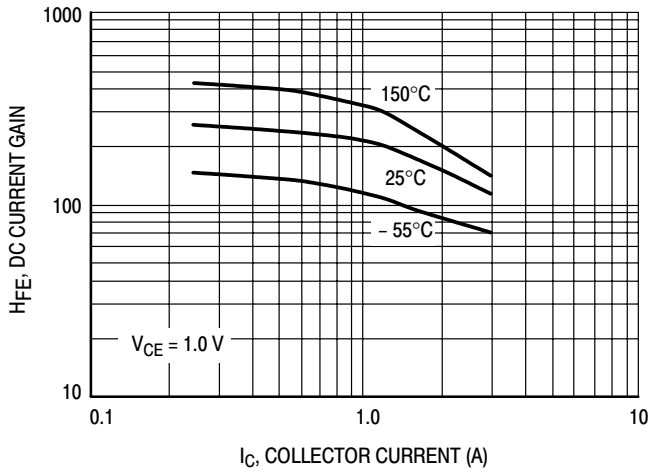


Figure 3. DC Current Gain

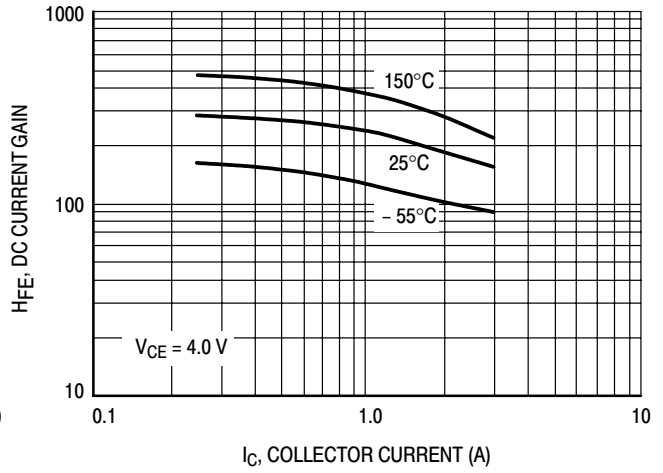


Figure 4. DC Current Gain

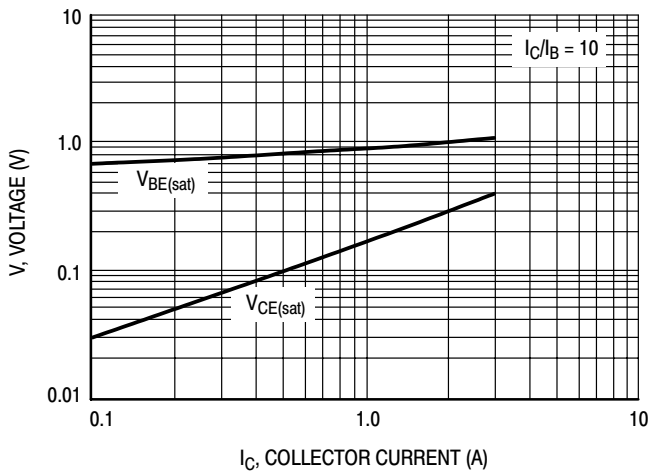


Figure 5. "On" Voltages

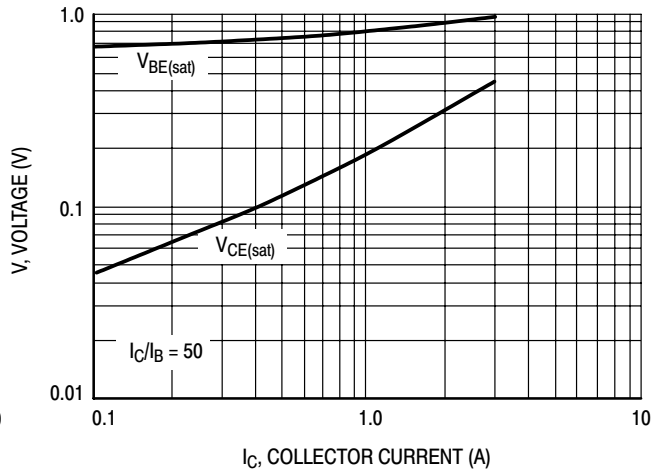


Figure 6. "On" Voltages

# MMJT9435

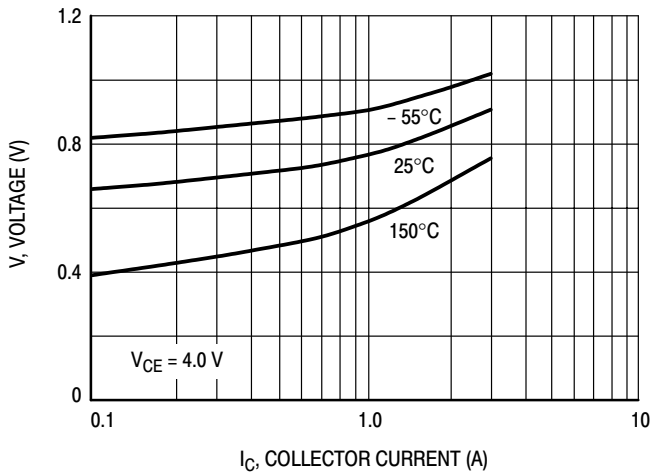


Figure 7.  $V_{BE(on)}$  Voltage

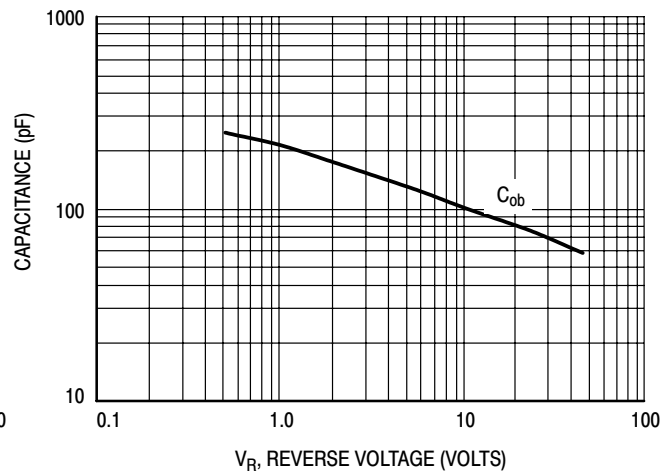


Figure 8. Output Capacitance

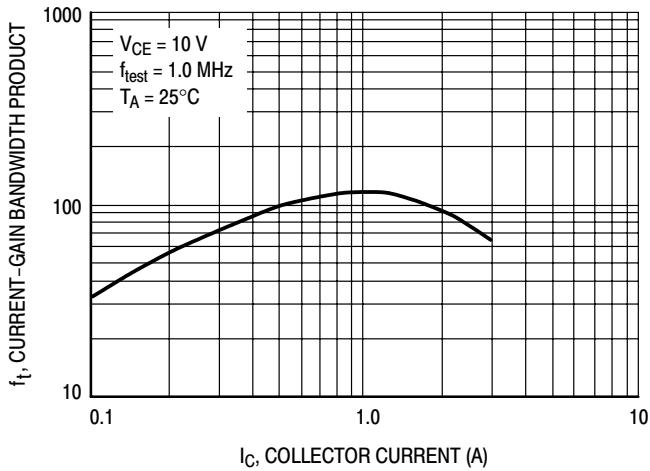


Figure 9. Current-Gain Bandwidth Product

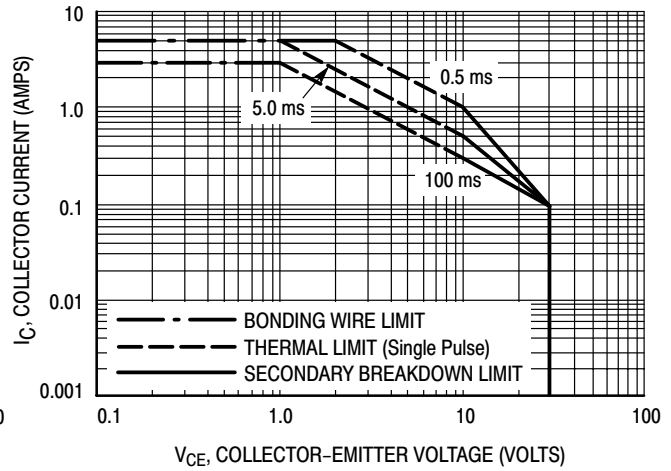


Figure 10. Active Region Safe Operating Area

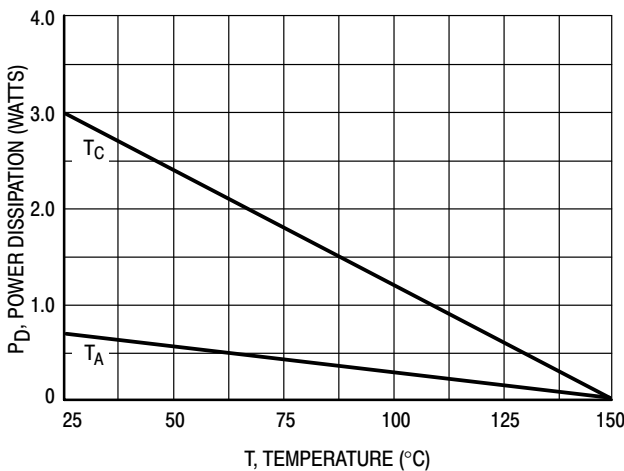


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

# MMJT9435

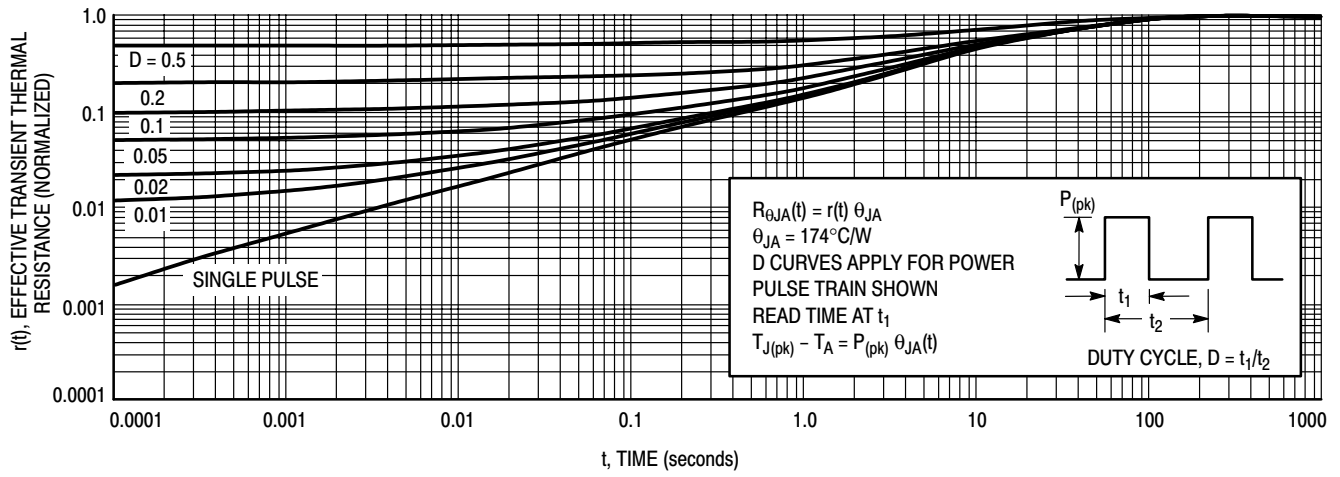


Figure 12. Thermal Response



# Plastic Medium-Power Complementary Silicon Transistors

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —  
 $h_{FE} = 2500$  (Typ) @  $I_C$   
 $= 4.0$  Adc
- Collector-Emitter Sustaining Voltage — @ 30 mA dc  
 $V_{CEO(sus)} = 60$  Vdc (Min) — TIP100, TIP105  
 $= 80$  Vdc (Min) — TIP101, TIP106  
 $= 100$  Vdc (Min) — TIP102, TIP107
- Low Collector-Emitter Saturation Voltage —  
 $V_{CE(sat)} = 2.0$  Vdc (Max) @  $I_C$   
 $= 3.0$  Adc  
 $= 2.5$  Vdc (Max) @  $I_C = 8.0$  Adc
- Monolithic Construction with Built-in Base-Emitter Shunt Resistors
- TO-220AB Compact Package

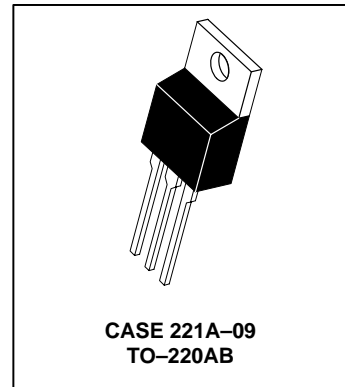
**NPN**  
**TIP100**  
**TIP101\***  
**TIP102\***  
**PNP**  
**TIP105**  
**TIP106\***  
**TIP107\***

\*ON Semiconductor Preferred Device

**DARLINGTON**  
**8 AMPERE**  
**COMPLEMENTARY SILICON**  
**POWER TRANSISTORS**  
**60-80-100 VOLTS**  
**80 WATTS**

### \*MAXIMUM RATINGS

Rating	Symbol	TIP100, TIP105	TIP101, TIP106	TIP102, TIP107	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	80	100	Vdc
Collector-Base Voltage	$V_{CB}$	60	80	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous Peak	$I_C$	8.0 15			A dc
Base Current	$I_B$	1.0			A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	80 0.64			Watts W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (1)	E	30			mJ
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150			$^\circ\text{C}$



### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

(1)  $I_C = 1.1$  A,  $L = 50$  mH, P.R.F. = 10 Hz,  $V_{CC} = 20$  V,  $R_{BE} = 100$   $\Omega$ .

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

TIP100 TIP101 TIP102 TIP105 TIP106 TIP107

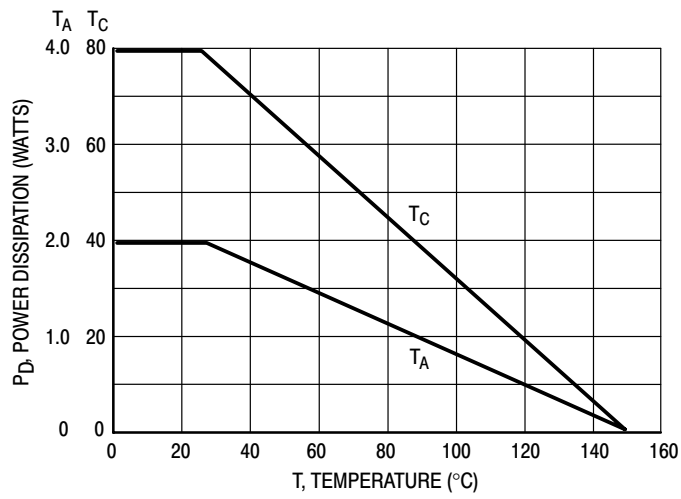


Figure 1. Power Derating

# TIP100 TIP101 TIP102 TIP105 TIP106 TIP107

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	60 80 100	—	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— — —	50 50 50	$\mu\text{A}$ dc
Collector Cutoff Current ( $V_{CB} = 60\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	— — —	50 50 50	$\mu\text{A}$ dc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	8.0	mAdc

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 8.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	1000 200	20,000 —	—
Collector–Emitter Saturation Voltage ( $I_C = 3.0\text{ Adc}$ , $I_B = 6.0\text{ mA}$ ) ( $I_C = 8.0\text{ Adc}$ , $I_B = 80\text{ mA}$ )	$V_{CE(sat)}$	— —	2.0 2.5	Vdc
Base–Emitter On Voltage ( $I_C = 8.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	2.8	Vdc

## DYNAMIC CHARACTERISTICS

Small–Signal Current Gain ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$h_{fe}$	4.0	—	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	— —	300 200	pF

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

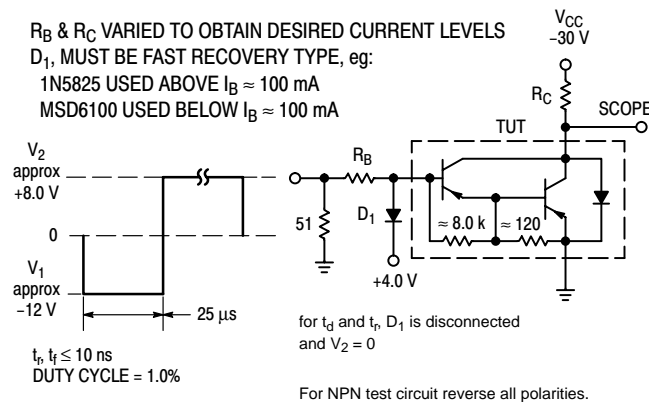


Figure 2. Switching Times Test Circuit

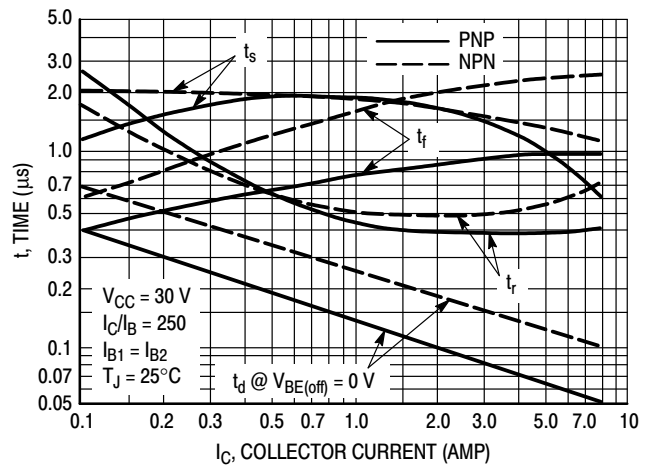


Figure 3. Switching Times

TIP100 TIP101 TIP102 TIP105 TIP106 TIP107

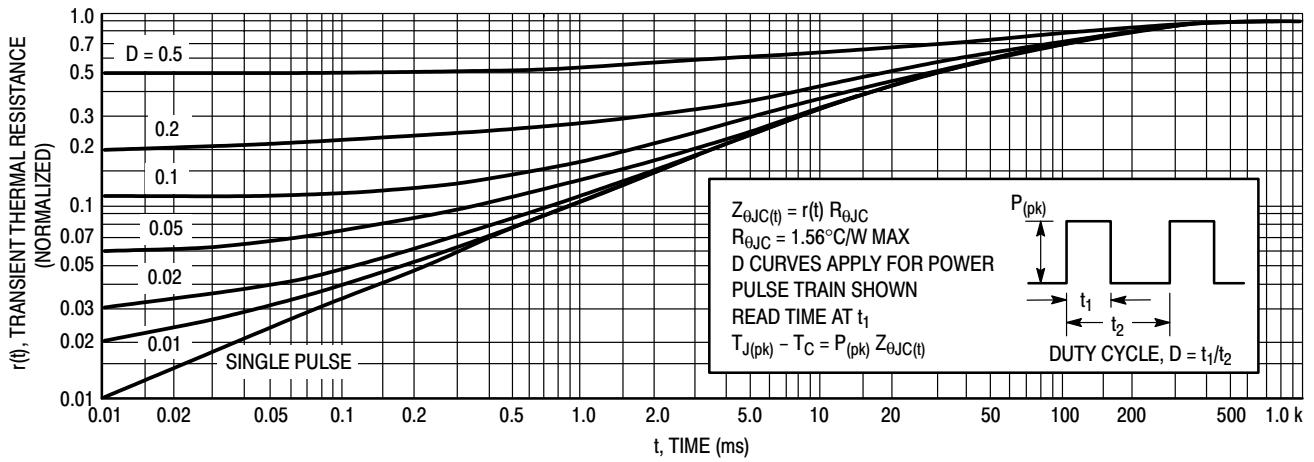


Figure 4. Thermal Response

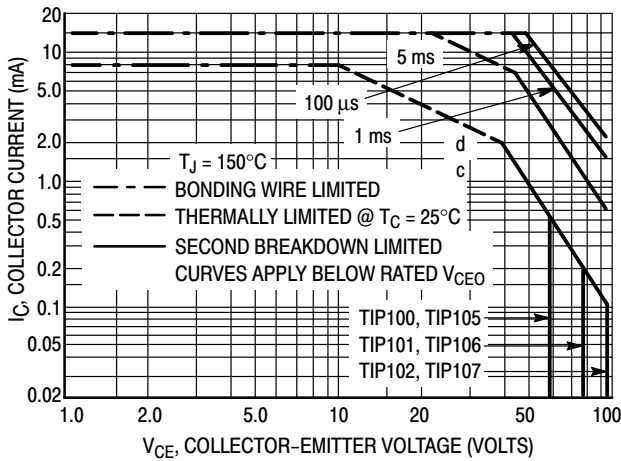


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

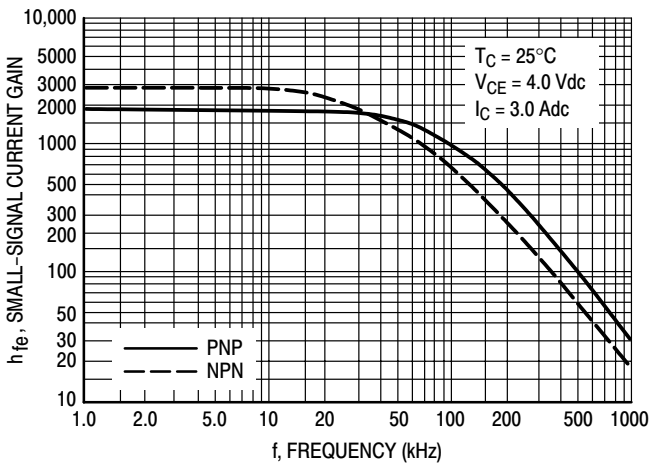


Figure 6. Small-Signal Current Gain

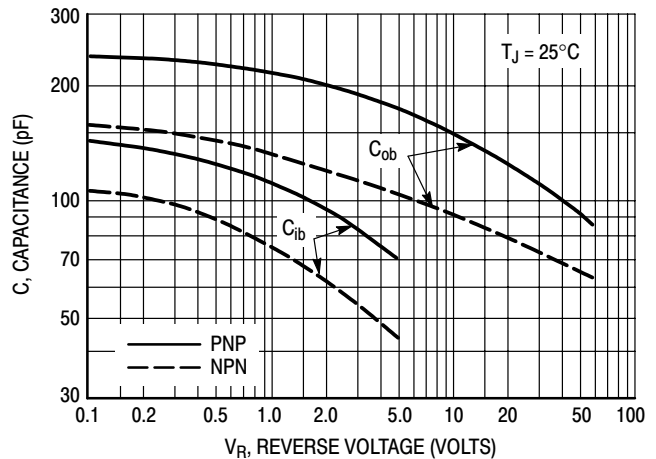


Figure 7. Capacitance

TIP100 TIP101 TIP102 TIP105 TIP106 TIP107

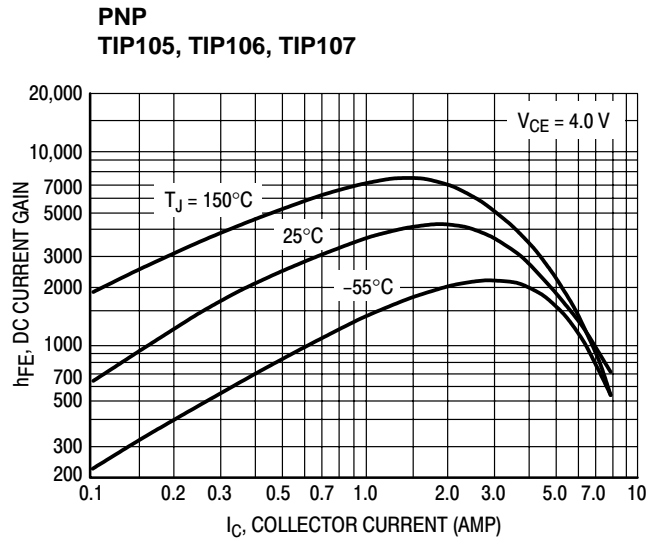
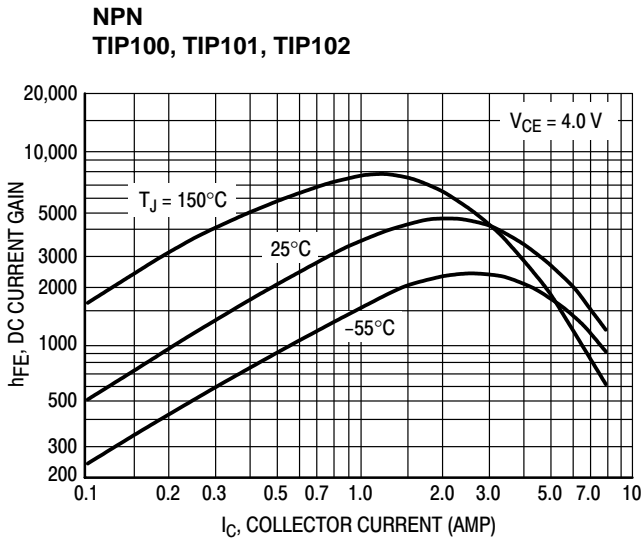


Figure 8. DC Current Gain

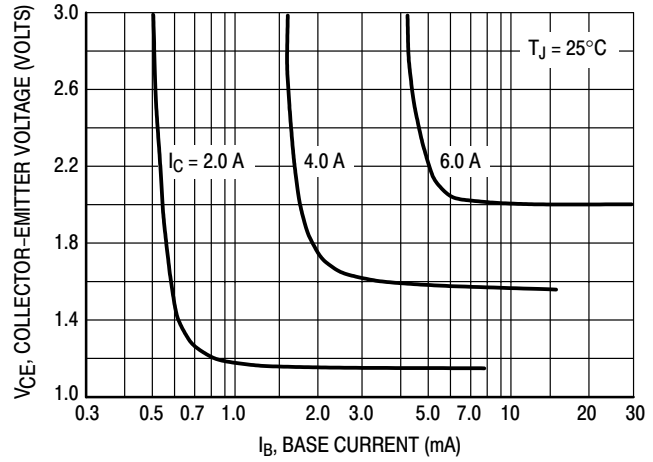
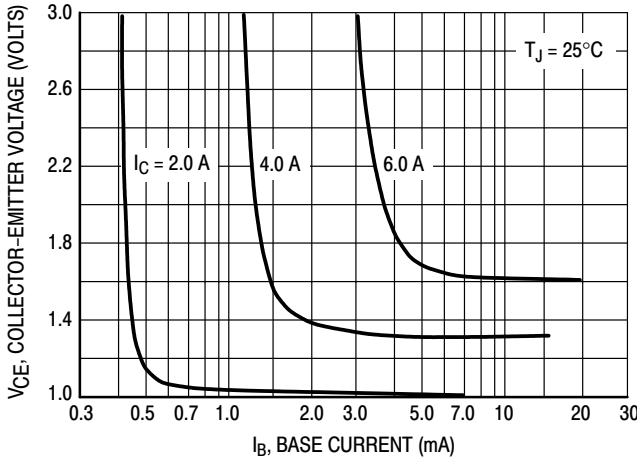


Figure 9. Collector Saturation Region

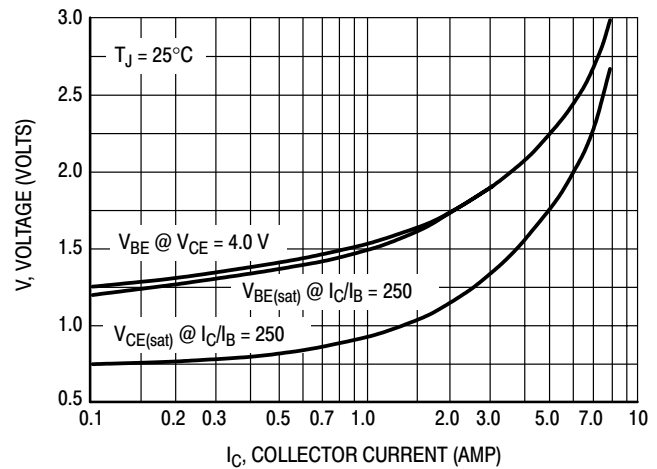
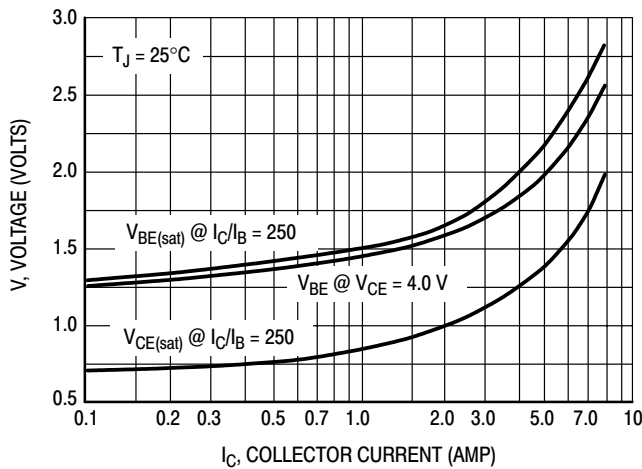


Figure 10. "On" Voltages

# Plastic Medium-Power Complementary Silicon Transistors

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —  
 $h_{FE} = 2500$  (Typ) @  $I_C$   
 $= 1.0$  Adc
- Collector-Emitter Sustaining Voltage — @ 30 mAdc  
 $V_{CEO(sus)} = 60$  Vdc (Min) — TIP110, TIP115  
 $= 80$  Vdc (Min) — TIP111, TIP116  
 $= 100$  Vdc (Min) — TIP112, TIP117
- Low Collector-Emitter Saturation Voltage —  
 $V_{CE(sat)} = 2.5$  Vdc (Max) @  $I_C$   
 $= 2.0$  Adc
- Monolithic Construction with Built-in Base-Emitter Shunt Resistors
- TO-220AB Compact Package

**\*MAXIMUM RATINGS**

Rating	Symbol	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	80	100	Vdc
Collector-Base Voltage	$V_{CB}$	60	80	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous Peak	$I_C$	2.0 4.0			A dc
Base Current	$I_B$	50			mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	50 0.4			Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016			Watts W/ $^\circ\text{C}$
Unclamped Inductive Load Energy — Figure 13	E	25			mJ
Operating and Storage Junction	$T_J, T_{stg}$	-65 to +150			$^\circ\text{C}$

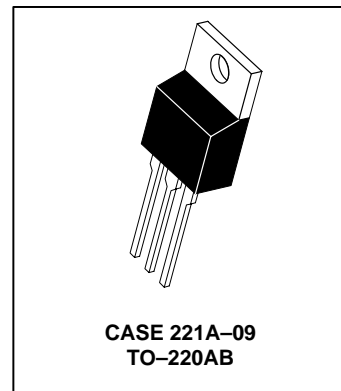
**THERMAL CHARACTERISTICS**

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

**NPN**  
**TIP110**  
**TIP111\***  
**TIP112\***  
**PNP**  
**TIP115**  
**TIP116\***  
**TIP117\***

\*ON Semiconductor Preferred Device

**DARLINGTON**  
**2 AMPERE**  
**COMPLEMENTARY SILICON**  
**POWER TRANSISTORS**  
**60-80-100 VOLTS**  
**50 WATTS**



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

TIP110 TIP111 TIP112 TIP115 TIP116 TIP117

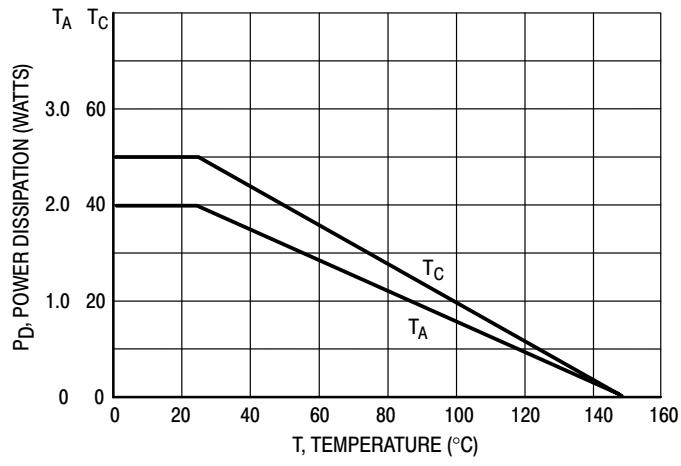


Figure 1. Power Derating

# TIP110 TIP111 TIP112 TIP115 TIP116 TIP117

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	60 80 100	—	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— — —	2.0 2.0 2.0	mAdc
Collector Cutoff Current ( $V_{CB} = 60\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	— — —	1.0 1.0 1.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	2.0	mAdc

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	1000 500	— —	—
Collector–Emitter Saturation Voltage ( $I_C = 2.0\text{ Adc}$ , $I_B = 8.0\text{ mAdc}$ )	$V_{CE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	2.8	Vdc

## DYNAMIC CHARACTERISTICS

Small–Signal Current Gain ( $I_C = 0.75\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$h_{fe}$	25	—	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	— —	200 100	pF

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

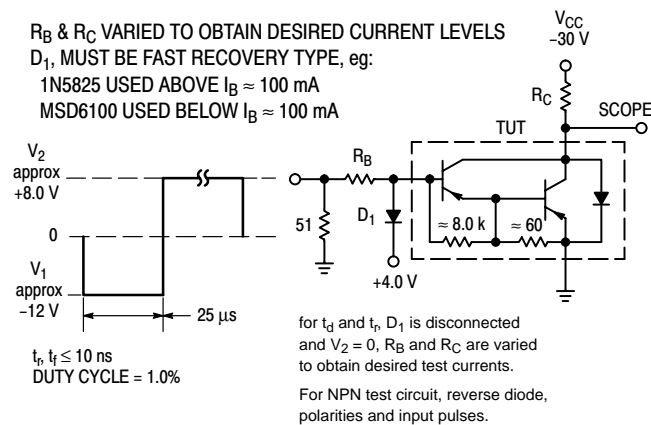


Figure 2. Switching Times Test Circuit

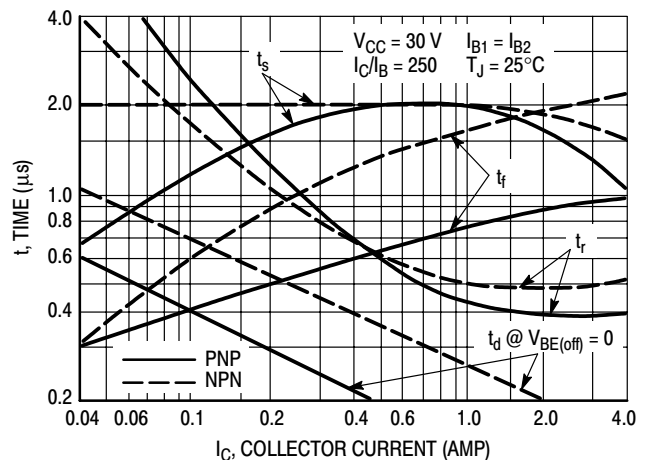


Figure 3. Switching Times



TIP110 TIP111 TIP112 TIP115 TIP116 TIP117

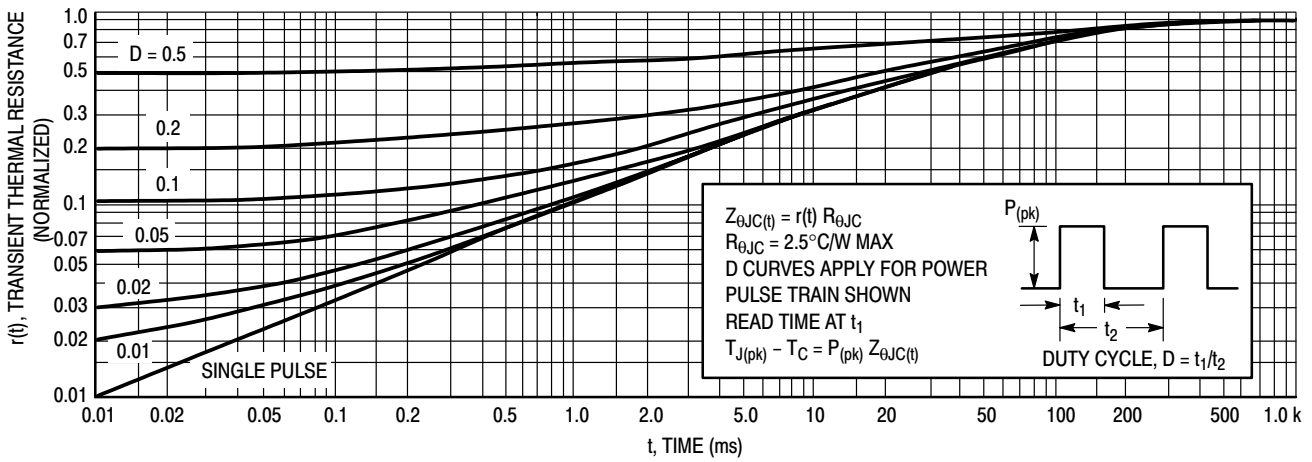


Figure 4. Thermal Response

ACTIVE-REGION SAFE-OPERATING AREA

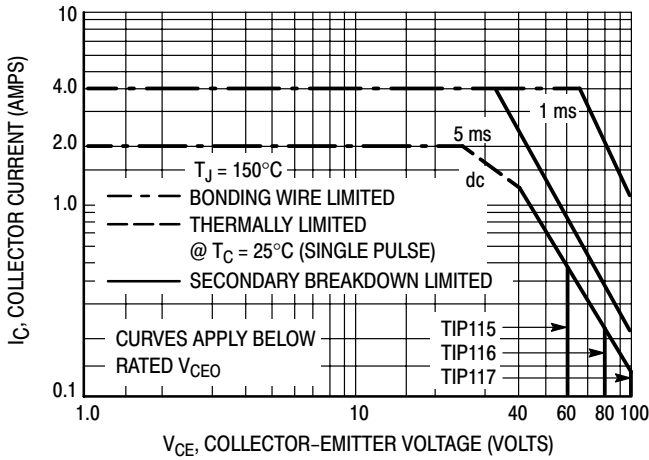


Figure 5. TIP115, 116, 117

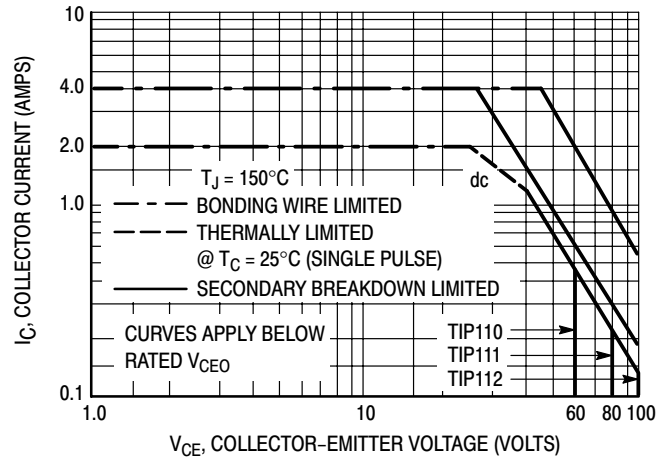


Figure 6. TIP110, 111, 112

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

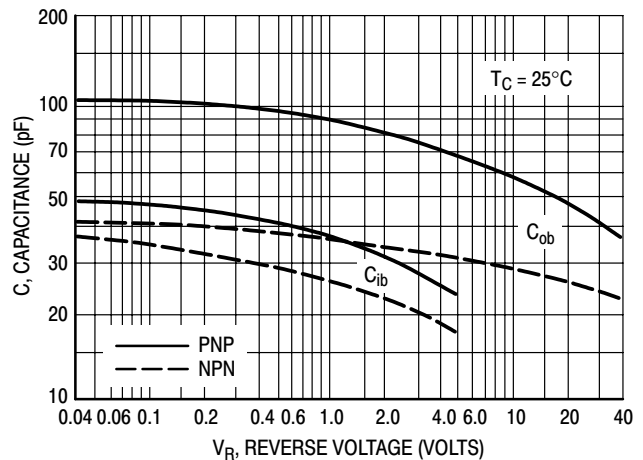


Figure 7. Capacitance

TIP110 TIP111 TIP112 TIP115 TIP116 TIP117

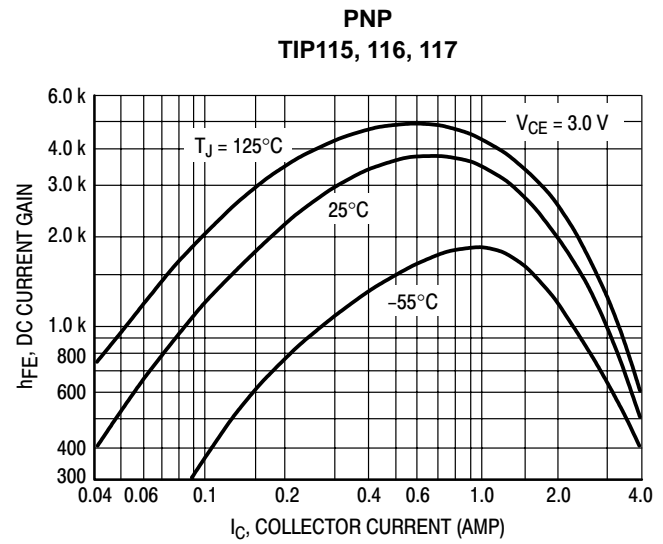
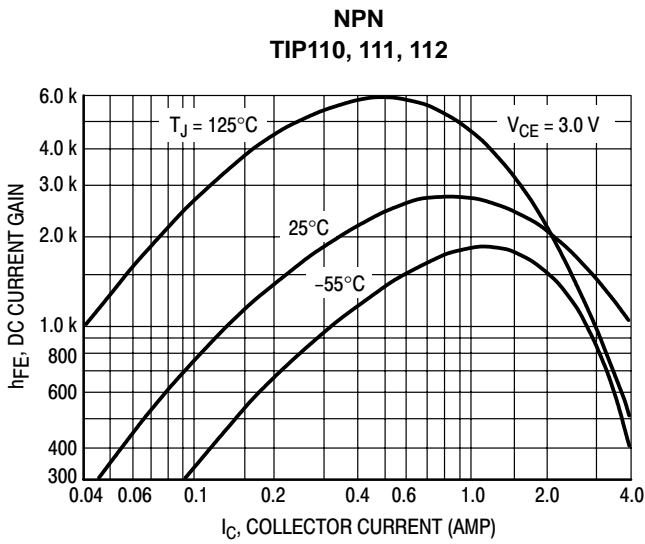


Figure 8. DC Current Gain

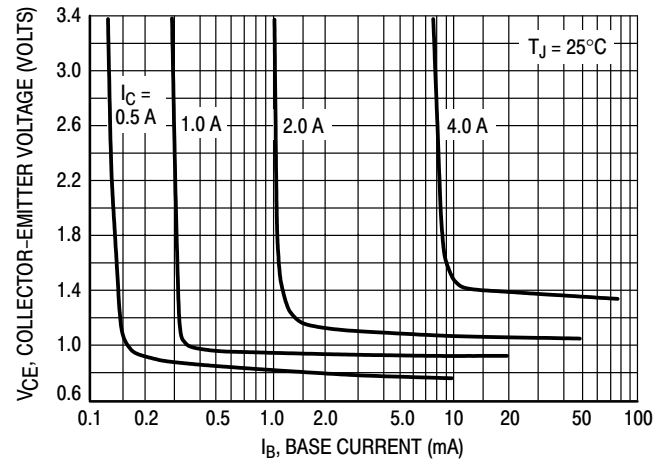
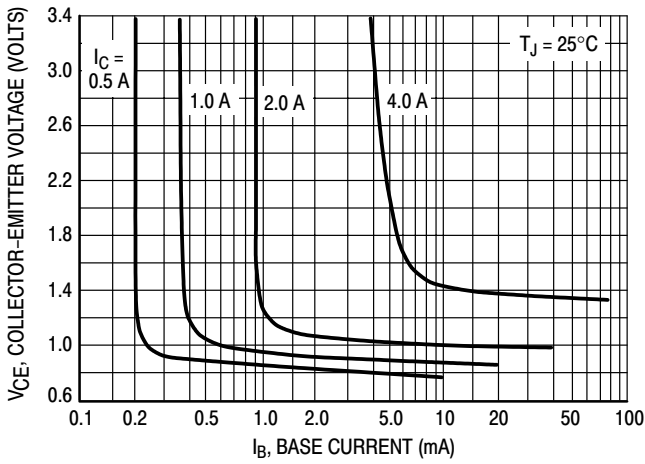


Figure 9. Collector Saturation Region

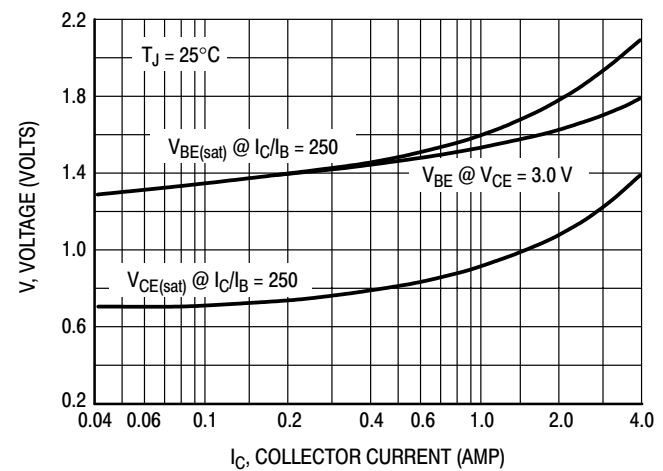
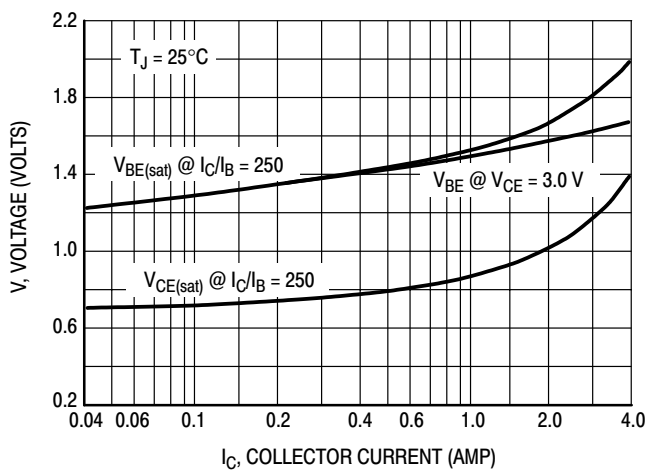


Figure 10. "On" Voltages

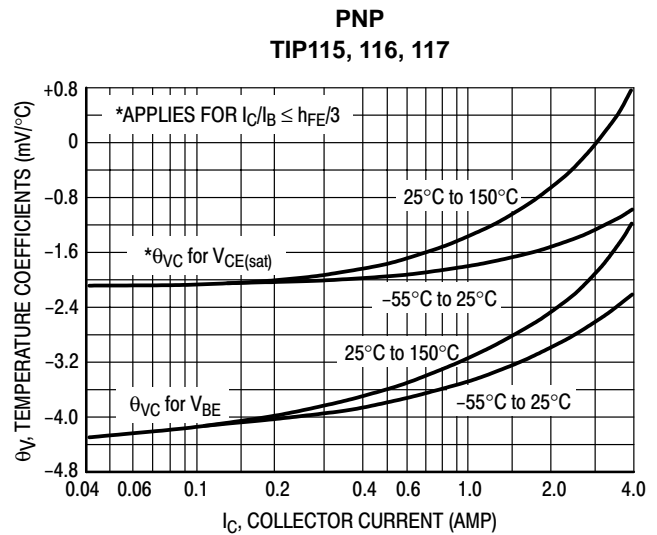
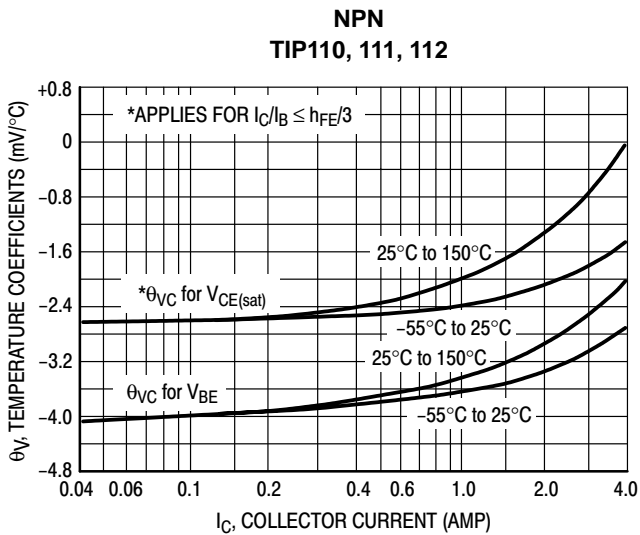


Figure 11. Temperature Coefficients

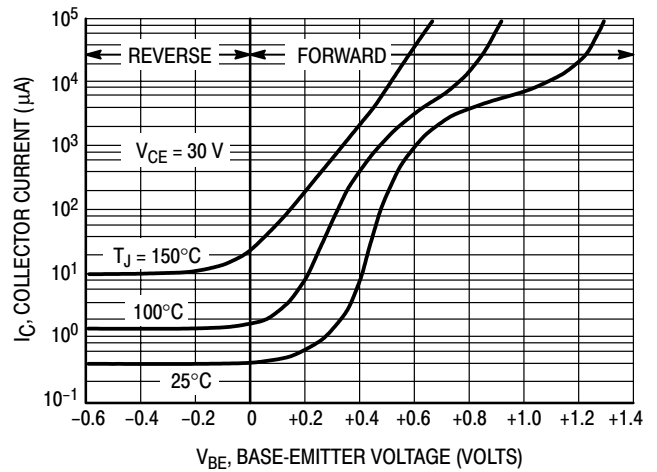
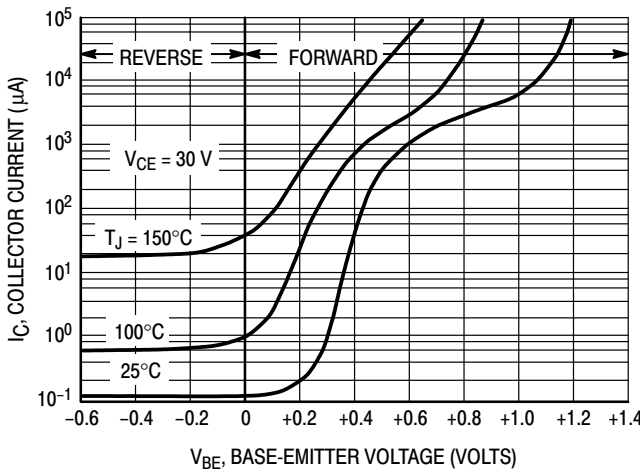
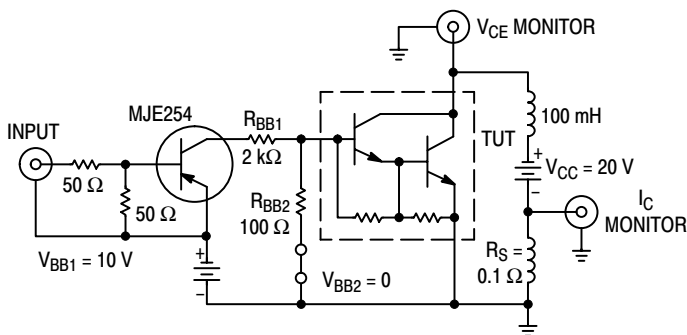
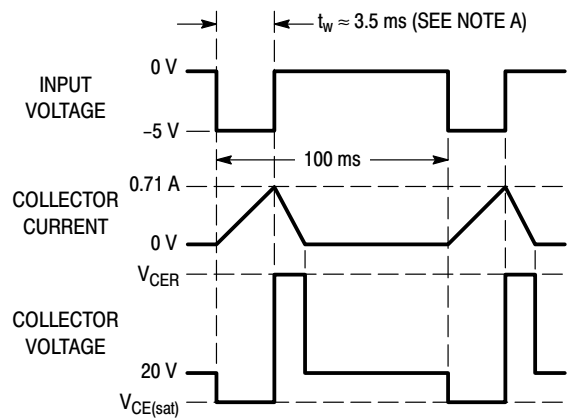


Figure 12. Collector Cut-Off Region

**TEST CIRCUIT**



**VOLTAGE AND CURRENT WAVEFORMS**



Note A: Input pulse width is increased until  $I_{CM} = 0.71$  A, NPN test shown; for PNP test reverse all polarity and use MJE224 driver.

Figure 13. Inductive Load Switching

# Plastic Medium-Power Complementary Silicon Transistors

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —  
 $h_{FE} = 2500$  (Typ) @  $I_C$   
 $= 4.0$  Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc  
 $V_{CEO(sus)} = 60$  Vdc (Min) — TIP120, TIP125  
 $= 80$  Vdc (Min) — TIP121, TIP126  
 $= 100$  Vdc (Min) — TIP122, TIP127
- Low Collector-Emitter Saturation Voltage —  
 $V_{CE(sat)} = 2.0$  Vdc (Max) @  $I_C = 3.0$  Adc  
 $= 4.0$  Vdc (Max) @  $I_C = 5.0$  Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package

**\*MAXIMUM RATINGS**

Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	80	100	Vdc
Collector-Base Voltage	$V_{CB}$	60	80	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous Peak	$I_C$	5.0 8.0			Adc
Base Current	$I_B$	120			mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	65 0.52			Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016			Watts W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (1)	E	50			mJ
Operating and Storage Junction, Temperature Range	$T_J, T_{stg}$	-65 to +150			$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

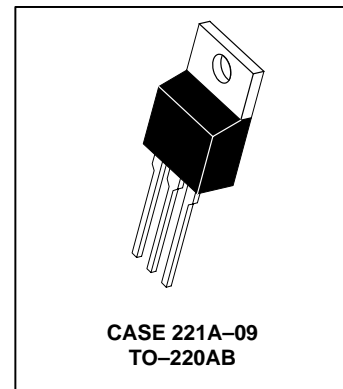
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

(1)  $I_C = 1$  A,  $L = 100$  mH, P.R.F. = 10 Hz,  $V_{CC} = 20$  V,  $R_{BE} = 100 \Omega$ .

**NPN**  
**TIP120\***  
**TIP121\***  
**TIP122\***  
**PNP**  
**TIP125\***  
**TIP126\***  
**TIP127\***

\*ON Semiconductor Preferred Device

**DARLINGTON**  
**5 AMPERE**  
**COMPLEMENTARY SILICON**  
**POWER TRANSISTORS**  
**60-80-100 VOLTS**  
**65 WATTS**



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

TIP120 TIP121 TIP122 TIP125 TIP126 TIP127

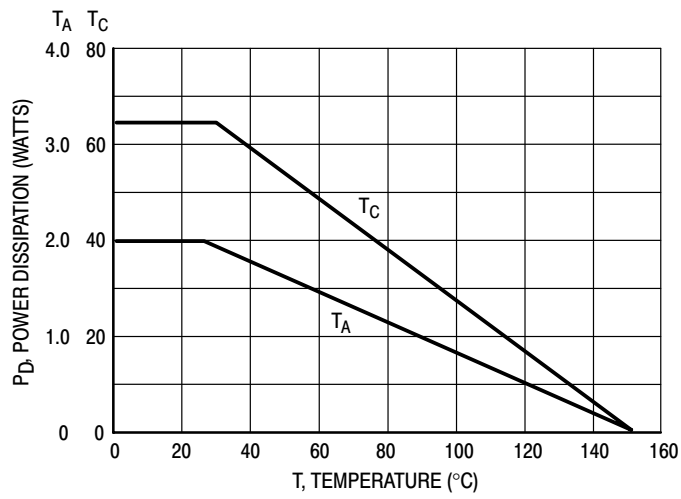


Figure 1. Power Derating

# TIP120 TIP121 TIP122 TIP125 TIP126 TIP127

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	$V_{CE(sus)}$	60 80 100	—	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— — —	0.5 0.5 0.5	mAdc
Collector Cutoff Current ( $V_{CB} = 60\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	— — —	0.2 0.2 0.2	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	2.0	mAdc

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	$h_{FE}$	1000 1000	— —	—
Collector–Emitter Saturation Voltage ( $I_C = 3.0\text{ Adc}$ , $I_B = 12\text{ mAdc}$ ) ( $I_C = 5.0\text{ Adc}$ , $I_B = 20\text{ mAdc}$ )	$V_{CE(sat)}$	— —	2.0 4.0	Vdc
Base–Emitter On Voltage ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	$V_{BE(on)}$	—	2.5	Vdc

## DYNAMIC CHARACTERISTICS

Small–Signal Current Gain ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$h_{fe}$	4.0	—	—
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	— —	300 200	pF

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

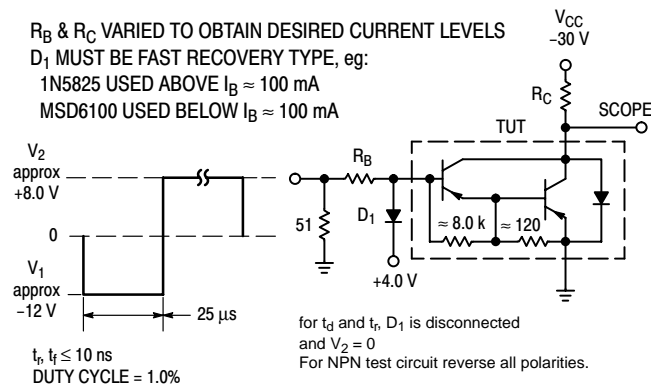


Figure 2. Switching Times Test Circuit

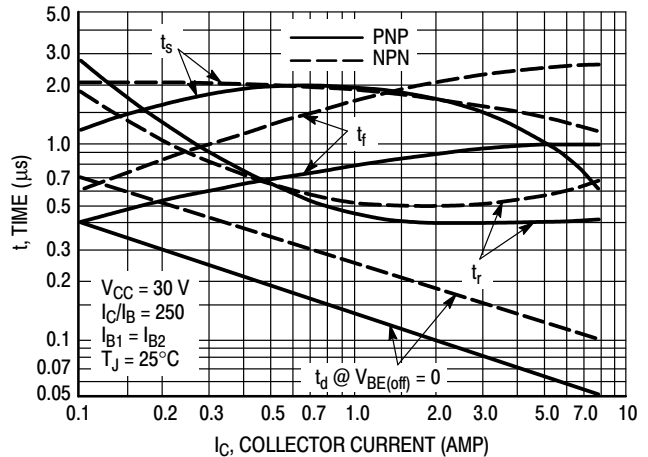


Figure 3. Switching Times

TIP120 TIP121 TIP122 TIP125 TIP126 TIP127

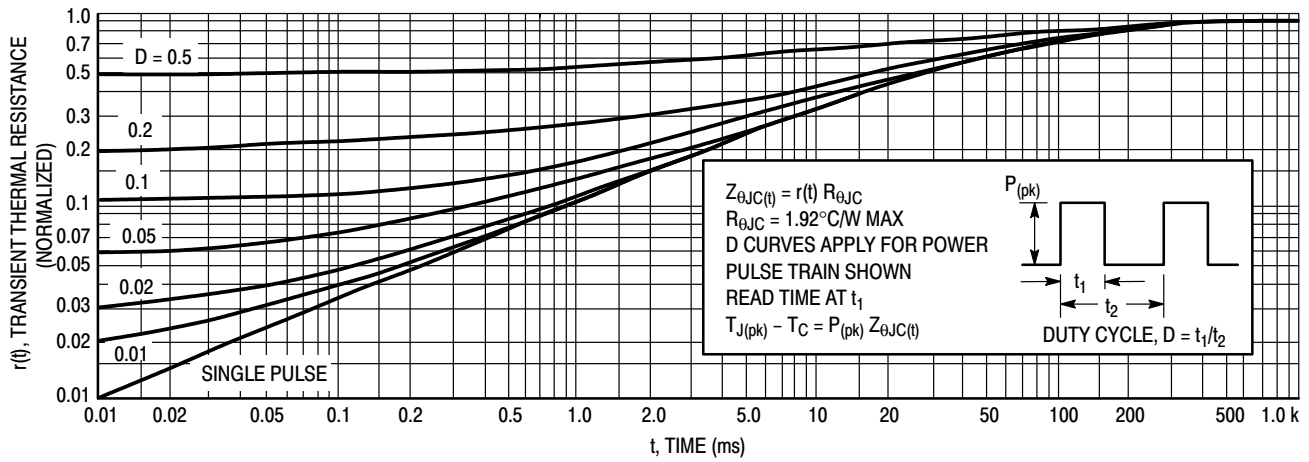


Figure 4. Thermal Response

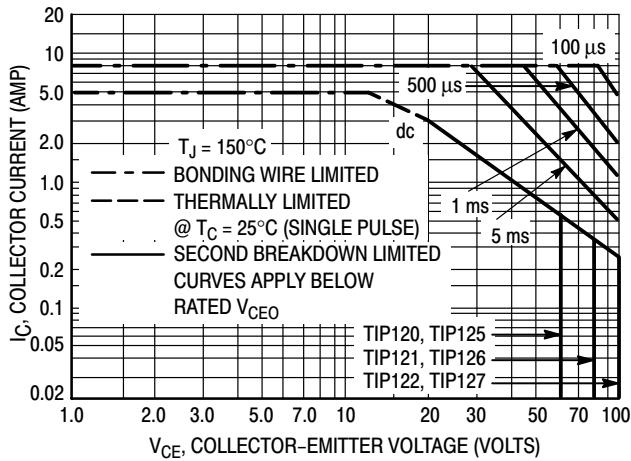


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

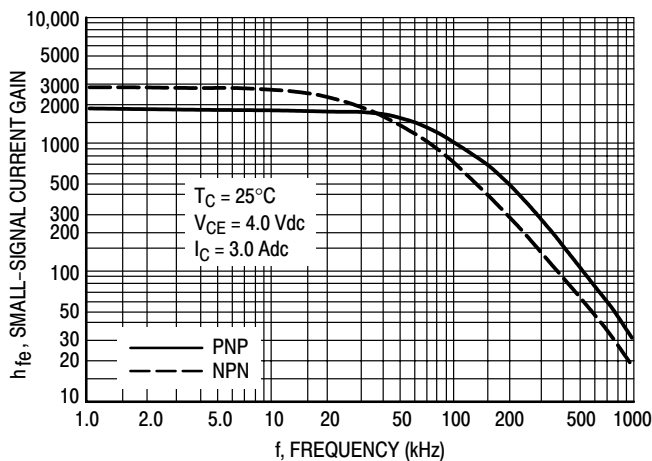


Figure 6. Small-Signal Current Gain

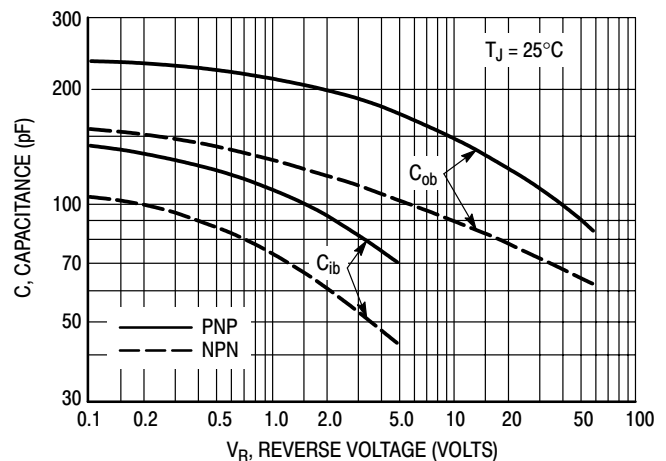
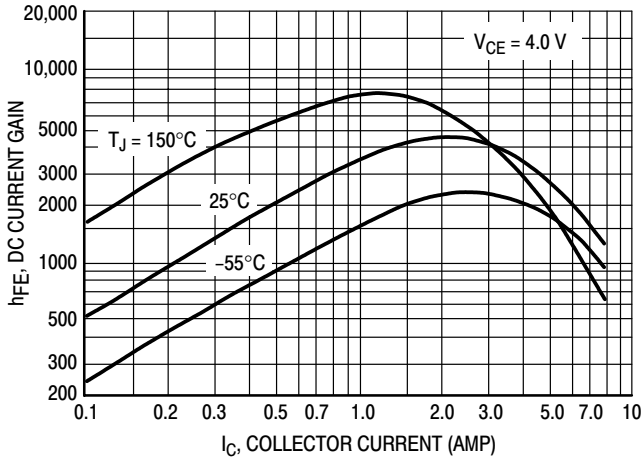


Figure 7. Capacitance

TIP120 TIP121 TIP122 TIP125 TIP126 TIP127

**NPN**  
TIP120, TIP121, TIP122



**PNP**  
TIP125, TIP126, TIP127

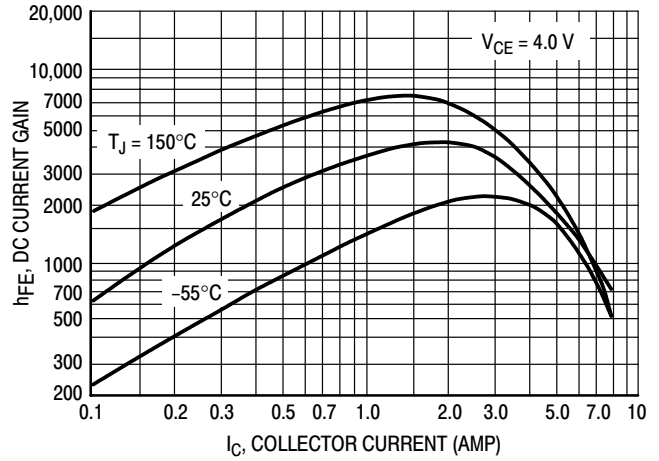


Figure 8. DC Current Gain

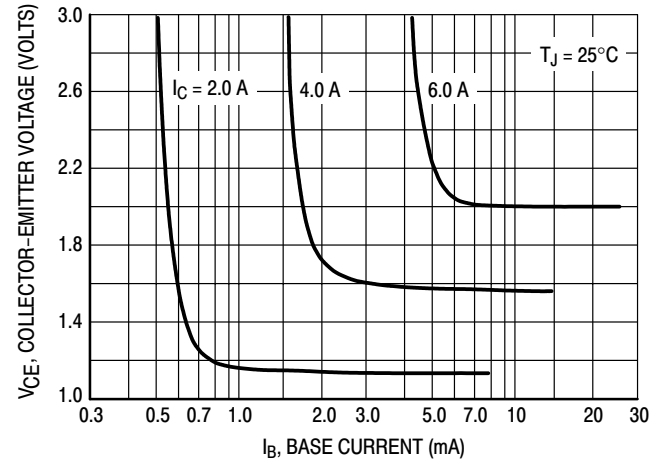
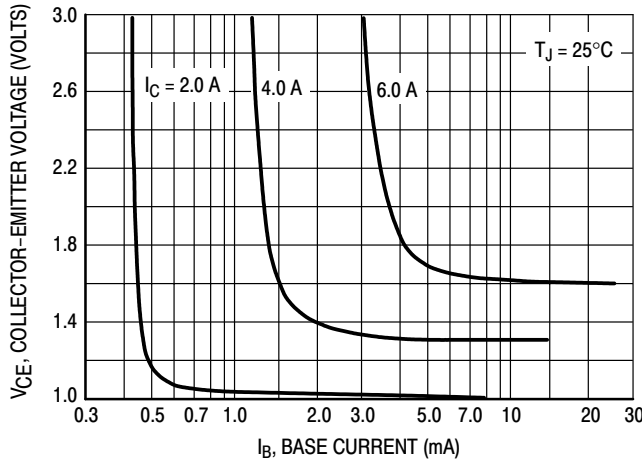


Figure 9. Collector Saturation Region

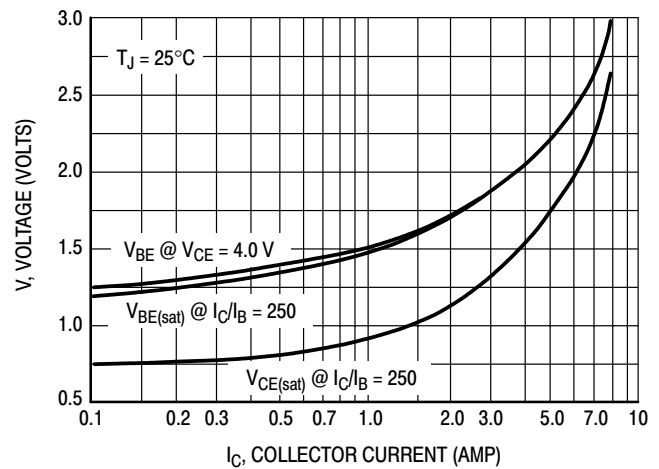
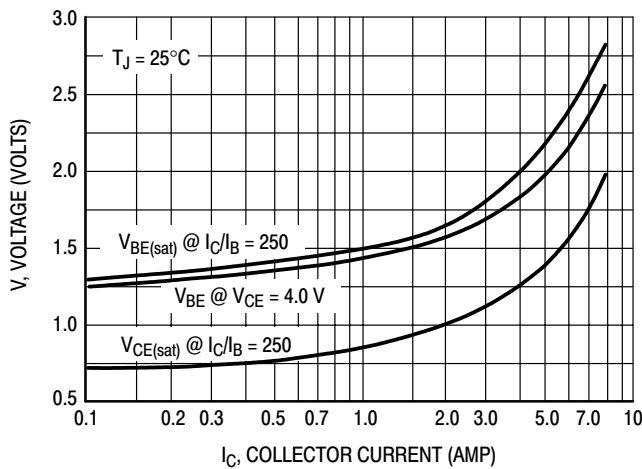


Figure 10. "On" Voltages



# Darlington Complementary Silicon Power Transistors

... designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain —  
 $\text{Min } h_{FE} = 1000 @ I_C$   
 $= 5 \text{ A, } V_{CE} = 4 \text{ V}$
- Collector–Emitter Sustaining Voltage — @ 30 mA  
 $V_{CEO(sus)} = 60 \text{ Vdc (Min) — TIP140, TIP145}$   
 $80 \text{ Vdc (Min) — TIP141, TIP146}$   
 $100 \text{ Vdc (Min) — TIP142, TIP147}$
- Monolithic Construction with Built–In Base–Emitter Shunt Resistor

## MAXIMUM RATINGS

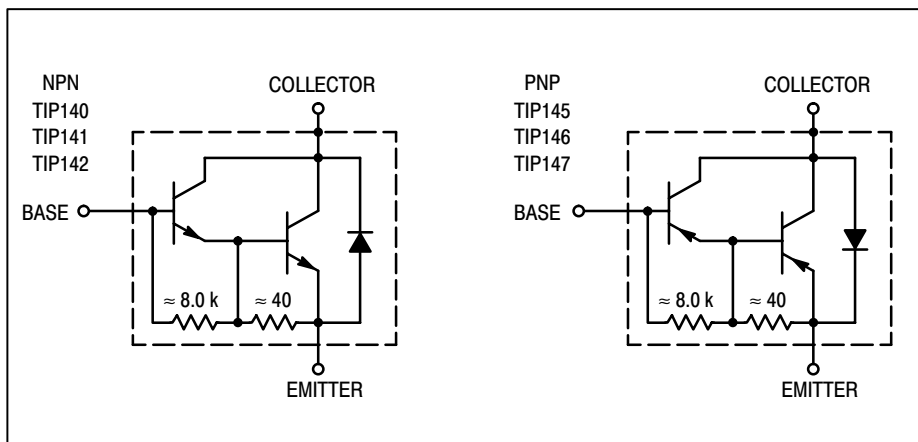
Rating	Symbol	TIP140 TIP145	TIP141 TIP146	TIP142 TIP147	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	80	100	Vdc
Collector–Base Voltage	$V_{CB}$	60	80	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous Peak (1)	$I_C$	10 15			A <sub>dc</sub>
Base Current — Continuous	$I_B$	0.5			A <sub>dc</sub>
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	125			Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150			$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
Thermal Resistance, Case to Ambient	$R_{\theta JA}$	35.7	$^\circ\text{C/W}$

(1) 5 ms,  $\leq 10\%$  Duty Cycle.

## DARLINGTON SCHEMATICS

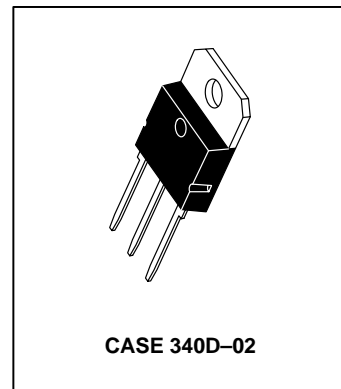


Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**NPN**  
**TIP140**  
**TIP141\***  
**TIP142\***  
**PNP**  
**TIP145**  
**TIP146\***  
**TIP147\***

\*ON Semiconductor Preferred Device

**10 AMPERE**  
**DARLINGTON**  
**COMPLEMENTARY SILICON**  
**POWER TRANSISTORS**  
**60–100 VOLTS**  
**125 WATTS**



# TIP140 TIP141 TIP142 TIP145 TIP146 TIP147

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	60 80 100	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— — —	— — —	2.0 2.0 2.0	mA
Collector Cutoff Current ( $V_{CB} = 60\text{ V}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ V}$ , $I_E = 0$ ) ( $V_{CB} = 100\text{ V}$ , $I_E = 0$ )	$I_{CBO}$	— — —	— — —	1.0 1.0 1.0	mA
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ V}$ )	$I_{EBO}$	—	—	2.0	mA

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 5.0\text{ A}$ , $V_{CE} = 4.0\text{ V}$ ) ( $I_C = 10\text{ A}$ , $V_{CE} = 4.0\text{ V}$ )	$h_{FE}$	1000 500	— —	— —	—
Collector–Emitter Saturation Voltage ( $I_C = 5.0\text{ A}$ , $I_B = 10\text{ mA}$ ) ( $I_C = 10\text{ A}$ , $I_B = 40\text{ mA}$ )	$V_{CE(sat)}$	— —	— —	2.0 3.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 10\text{ A}$ , $I_B = 40\text{ mA}$ )	$V_{BE(sat)}$	—	—	3.5	Vdc
Base–Emitter On Voltage ( $I_C = 10\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	—	3.0	Vdc

## SWITCHING CHARACTERISTICS

Resistive Load (See Figure 1)						
Delay Time	$(V_{CC} = 30\text{ V}$ , $I_C = 5.0\text{ A}$ , $I_B = 20\text{ mA}$ , Duty Cycle $\leq 2.0\%$ , $I_{B1} = I_{B2}$ , $R_C$ & $R_B$ Varied, $T_J = 25^\circ\text{C}$ )	$t_d$	—	0.15	—	$\mu\text{s}$
Rise Time		$t_r$	—	0.55	—	$\mu\text{s}$
Storage Time		$t_s$	—	2.5	—	$\mu\text{s}$
Fall Time		$t_f$	—	2.5	—	$\mu\text{s}$

(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

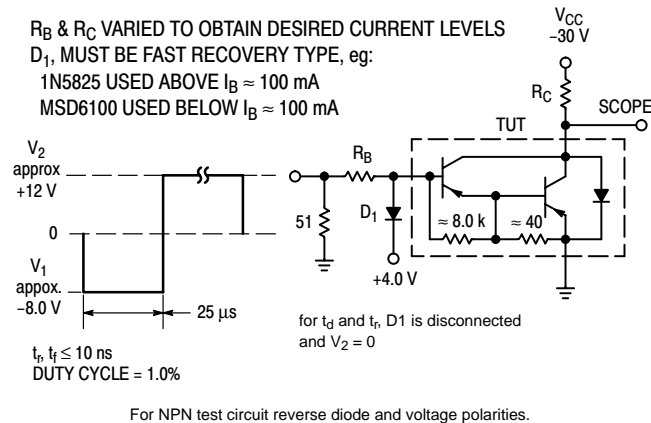


Figure 11. Switching Times Test Circuit

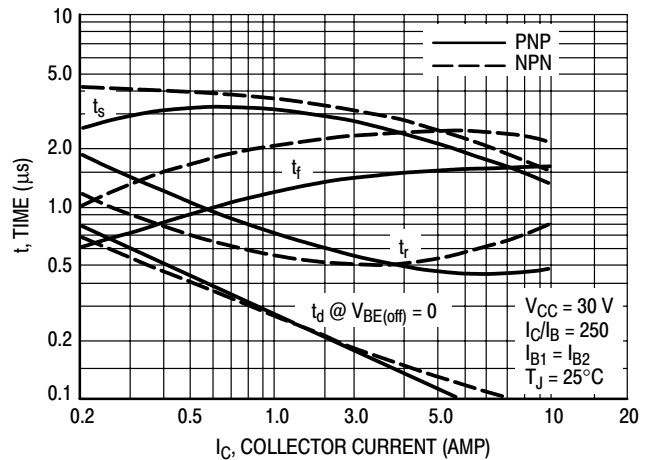


Figure 12. Switching Times

TYPICAL CHARACTERISTICS

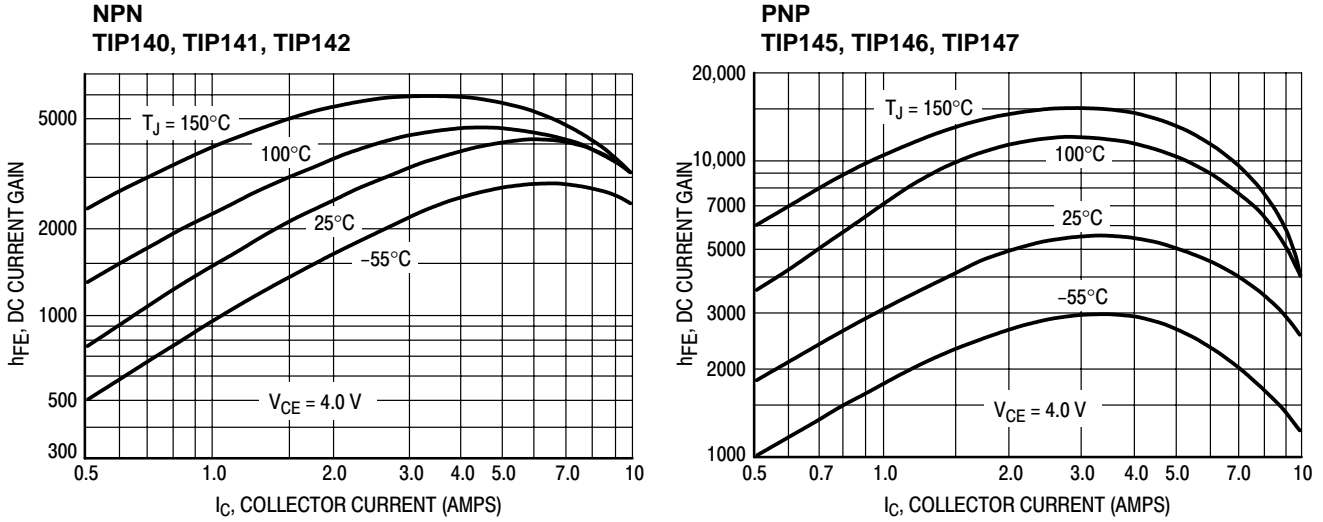


Figure 13. DC Current Gain versus Collector Current

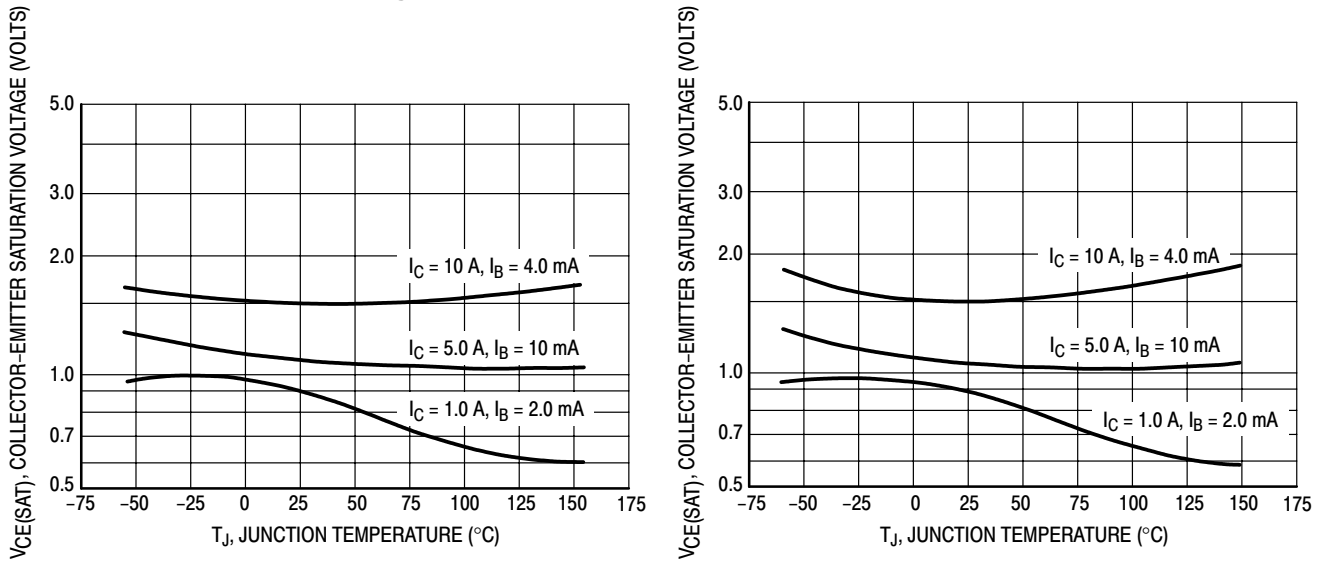


Figure 14. Collector-Emitter Saturation Voltage

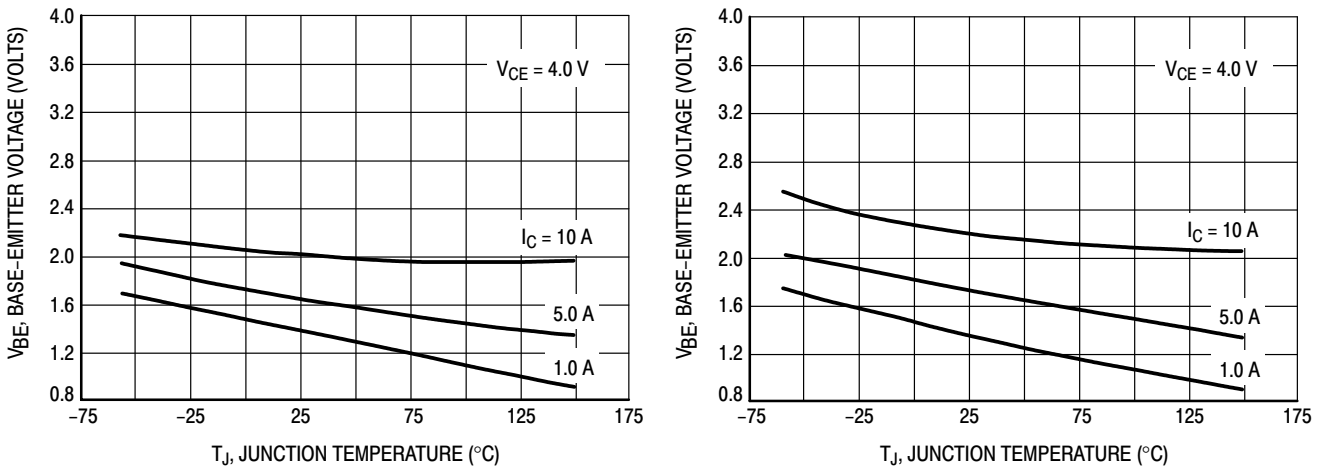


Figure 15. Base-Emitter Voltage

ACTIVE-REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 16 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

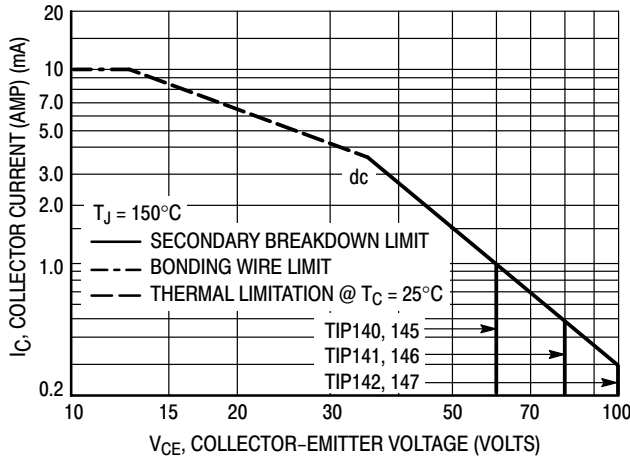


Figure 16. Active-Region Safe Operating Area

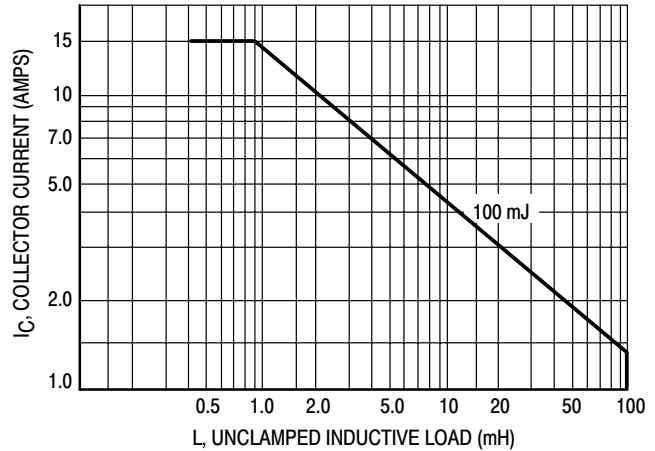
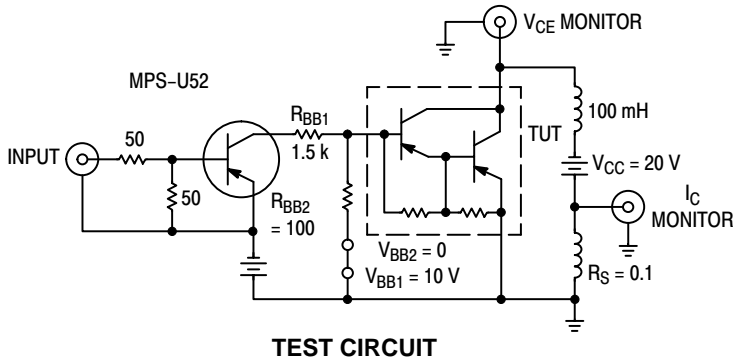
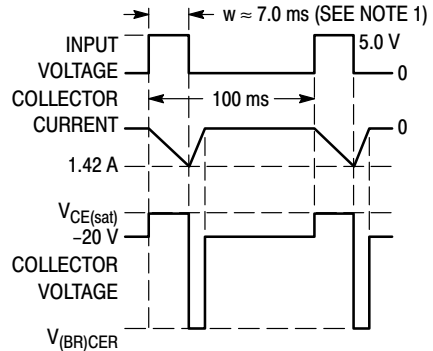


Figure 17. Unclamped Inductive Load



TEST CIRCUIT

NOTE 1: Input pulse width is increased until  $I_{CM} = 1.42\text{ A}$ .  
NOTE 2: For NPN test circuit reverse polarities.



VOLTAGE AND CURRENT WAVEFORMS

Figure 18. Inductive Load

TIP140 TIP141 TIP142 TIP145 TIP146 TIP147

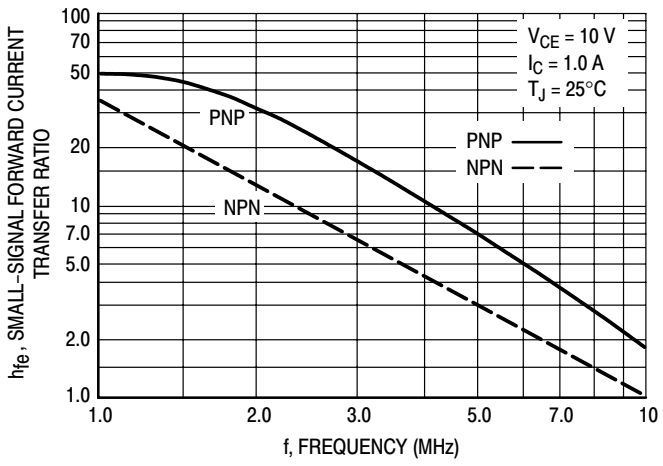


Figure 19. Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio

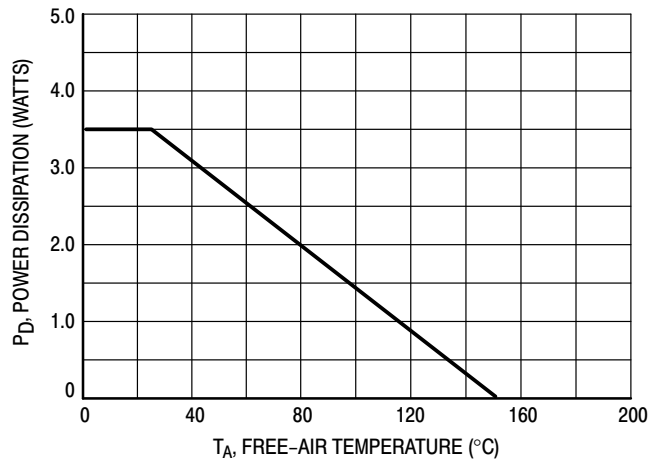


Figure 20. Free-Air Temperature Power Derating

# Complementary Silicon Plastic Power Transistors

... designed for use in general purpose amplifier and switching applications. Compact TO-220 AB package.

## MAXIMUM RATINGS

Rating	Symbol	TIP29B TIP30B	TIP29C TIP30C	Unit
Collector-Emitter Voltage	$V_{CEO}$	80	100	Vdc
Collector-Base Voltage	$V_{CB}$	80	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current — Continuous Peak	$I_C$	1.0 3.0		Adc
Base Current	$I_B$	0.4		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	30 0.24		Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016		Watts W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (See Note 3)	E	32		mJ
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	$^\circ\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mAdc}, I_B = 0$ )	TIP29B, TIP30B TIP29C, TIP30C	$V_{CEO(sus)}$	80 100	— — Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}, I_B = 0$ )		$I_{CEO}$	—	0.3 mAdc
Collector Cutoff Current ( $V_{CE} = 80\text{ Vdc}, V_{EB} = 0$ ) ( $V_{CE} = 100\text{ Vdc}, V_{EB} = 0$ )	TIP29B, TIP30B TIP29C, TIP30C	$I_{CES}$	— —	200 200 $\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}, I_C = 0$ )		$I_{EBO}$	—	1.0 mAdc

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 0.2\text{ Adc}, V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 1.0\text{ Adc}, V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	40 15	— 75	—
Collector-Emitter Saturation Voltage ( $I_C = 1.0\text{ Adc}, I_B = 125\text{ mAdc}$ )	$V_{CE(sat)}$	—	0.7	Vdc
Base-Emitter On Voltage ( $I_C = 1.0\text{ Adc}, V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	1.3	Vdc

## DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product (2) ( $I_C = 200\text{ mAdc}, V_{CE} = 10\text{ Vdc}, f_{test} = 1.0\text{ MHz}$ )	$f_T$	3.0	—	MHz
Small-Signal Current Gain ( $I_C = 0.2\text{ Adc}, V_{CE} = 10\text{ Vdc}, f = 1.0\text{ kHz}$ )	$h_{fe}$	20	—	—

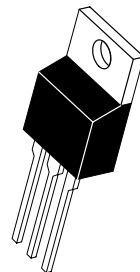
(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

(2)  $f_T = |h_{fe}| \cdot f_{test}$ .

(3) This rating based on testing with  $L_C = 20\text{ mH}$ ,  $R_{BE} = 100\ \Omega$ ,  $V_{CC} = 10\text{ V}$ ,  $I_C = 1.8\text{ A}$ , P.R.F = 10 Hz.

**NPN  
TIP29B  
TIP29C  
PNP  
TIP30B  
TIP30C**

**1 AMPERE  
POWER TRANSISTORS  
COMPLEMENTARY  
SILICON  
80-100 VOLTS  
30 WATTS**



**CASE 221A-06  
TO-220AB**

# TIP29B TIP29C TIP30B TIP30C

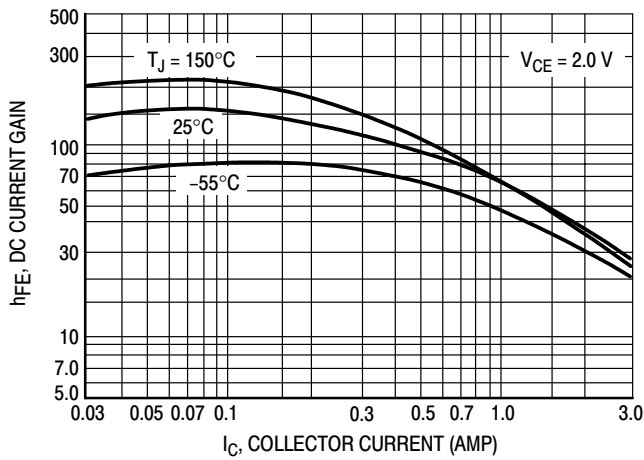


Figure 21. DC Current Gain

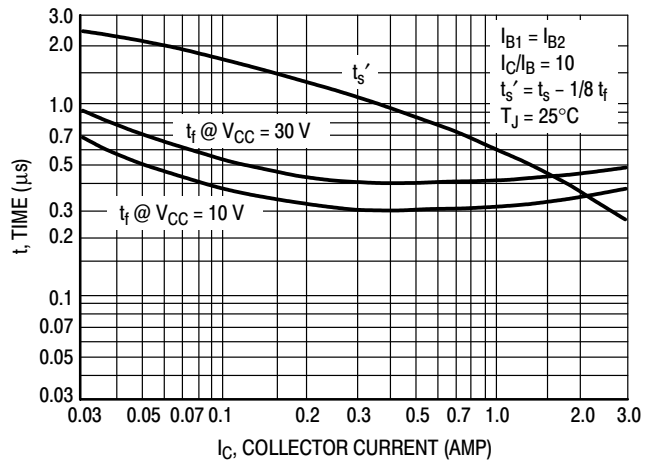


Figure 22. Turn-Off Time

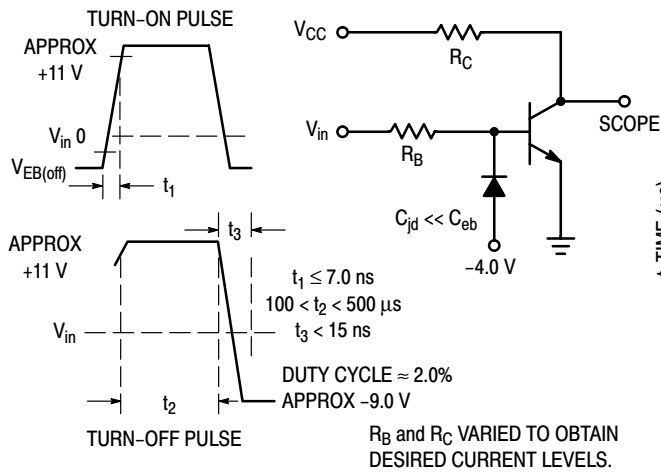


Figure 23. Switching Time Equivalent Circuit

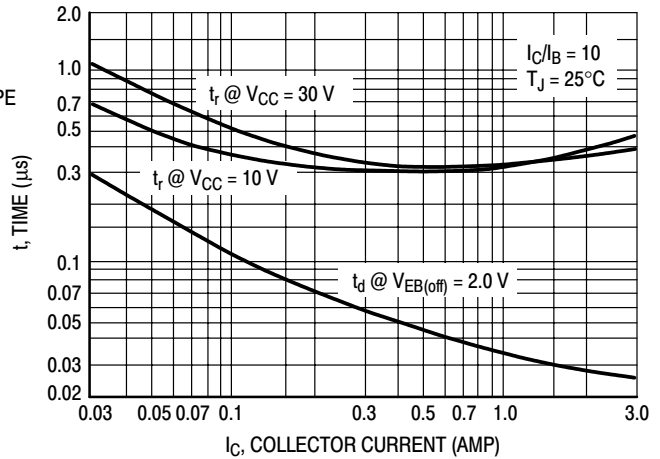


Figure 24. Turn-On Time

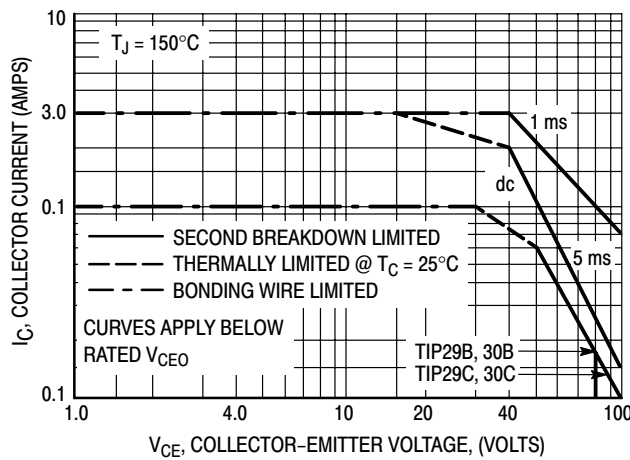


Figure 25. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 25 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

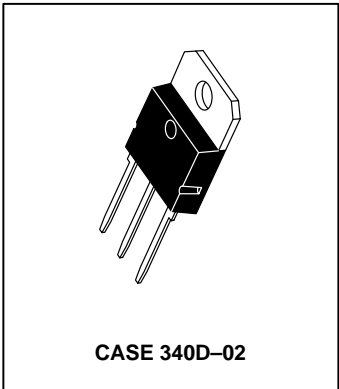
# Complementary Silicon Power Transistors

... designed for general-purpose switching and amplifier applications.

- DC Current Gain —  
 $h_{FE} = 20-70 @ I_C$   
 $= 4.0 A_{dc}$
- Collector-Emitter Saturation Voltage —  
 $V_{CE(sat)} = 1.1 V_{dc} (Max) @ I_C$   
 $= 4.0 A_{dc}$
- Excellent Safe Operating Area

**NPN  
TIP3055  
PNP  
TIP2955**

**15 AMPERE  
POWER TRANSISTORS  
COMPLEMENTARY  
SILICON  
60 VOLTS  
90 WATTS**



## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	Vdc
Collector-Emitter Voltage	$V_{CER}$	70	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	7.0	Vdc
Collector Current — Continuous	$I_C$	1.5	A <sub>dc</sub>
Base Current	$I_B$	7.0	A <sub>dc</sub>
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	$P_D$	90 0.72	Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ C$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.39	$^\circ C/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	35.7	$^\circ C/W$

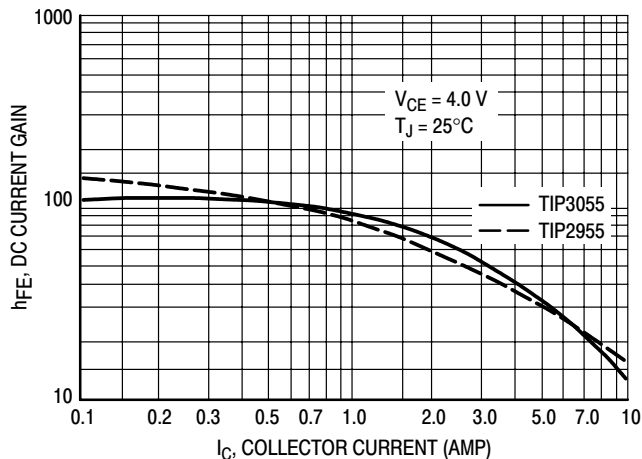


Figure 1. DC Current Gain



# TIP3055 TIP2955

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current ( $V_{CE} = 70\text{ Vdc}$ , $R_{BE} = 100\text{ Ohms}$ )	$I_{CER}$	—	1.0	mAdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	0.7	mAdc
Collector Cutoff Current ( $V_{CE} = 100\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ )	$I_{CEV}$	—	5.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 7.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	5.0	mAdc

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 10\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	20 5.0	70 —	—
Collector–Emitter Saturation Voltage ( $I_C = 4.0\text{ Adc}$ , $I_B = 400\text{ mAdc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 3.3\text{ Adc}$ )	$V_{CE(sat)}$	— —	1.1 3.0	Vdc
Base–Emitter On Voltage ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	1.8	Vdc

## SECOND BREAKDOWN

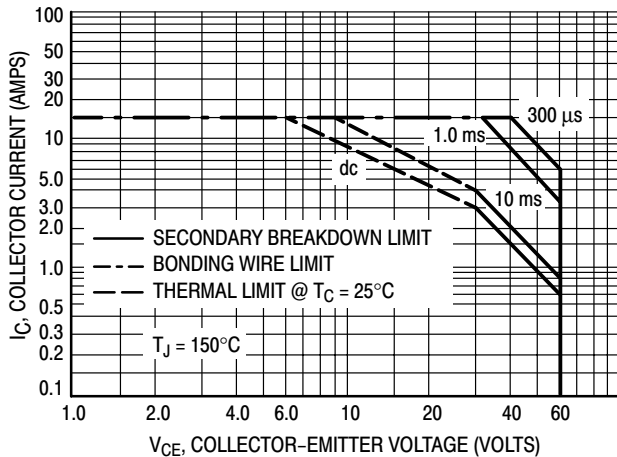
Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 30\text{ Vdc}$ , $t = 1.0\text{ s}$ ; Nonrepetitive)	$I_{s/b}$	3.0	—	Adc
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## DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	2.5	—	MHz
Small–Signal Current Gain ( $V_{CE} = 4.0\text{ Vdc}$ , $I_C = 1.0\text{ Adc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	15	—	kHz

(1) Pulse Test: Pulse Width =  $300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

NOTE: For additional design curves, refer to electrical characteristics curves of 2N3055.



**Figure 2. Maximum Rated Forward Bias Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature.

# Complementary Silicon Plastic Power Transistors

... designed for use in general purpose amplifier and switching applications.

- Collector–Emitter Saturation Voltage —  
 $V_{CE(sat)} = 1.2 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- Collector–Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 60 \text{ Vdc (Min) — TIP31A, TIP32A}$   
 $= 80 \text{ Vdc (Min) — TIP31B, TIP32B}$   
 $= 100 \text{ Vdc (Min) — TIP31C, TIP32C}$
- High Current Gain — Bandwidth Product  
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 500 \text{ mA}$
- Compact TO–220 AB Package

**\*MAXIMUM RATINGS**

Rating	Symbol	TIP31A TIP32A	TIP31B TIP32B	TIP31C TIP32C	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	80	100	Vdc
Collector–Base Voltage	$V_{CB}$	60	80	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous Peak	$I_C$	3.0 5.0			A
Base Current	$I_B$	1.0			A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.32			Watts W/°C
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy (1)	E	32			mJ
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150			°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

(1)  $I_C = 1.8 \text{ A}$ ,  $L = 20 \text{ mH}$ , P.R.F. = 10 Hz,  $V_{CC} = 10 \text{ V}$ ,  $R_{BE} = 100 \Omega$ .

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**NPN**  
**TIP31A**  
**TIP31B\***  
**MJF31C\***  
**PNP**  
**TIP31C**  
**TIP32A\***  
**TIP32B\***  
**TIP32C**  
**MJF32C**

\*ON Semiconductor Preferred Device

**3 AMPERE**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**60–80–100 VOLTS**  
**40 WATTS**

**CASE 221A–09**  
**TO–220AB**

# TIP31A TIP31B MJF31C TIP31C TIP32A TIP32B TIP32C MJF32C

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	TIP31A, TIP32A TIP31B, TIP32B TIP31C, TIP32C	$V_{CE(sus)}$	60 80 100	— — —	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	TIP31A, TIP32A TIP31B, TIP31C TIP32B, TIP32C	$I_{CEO}$	— — —	0.3 0.3 0.3	mAdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB} = 0$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB} = 0$ ) ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB} = 0$ )	TIP31A, TIP32A TIP31B, TIP32B TIP31C, TIP32C	$I_{CES}$	— — —	200 200 200	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	1.0	mAdc
<b>ON CHARACTERISTICS (1)</b>					
DC Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )		$h_{FE}$	25 10	— 50	—
Collector–Emitter Saturation Voltage ( $I_C = 3.0\text{ Adc}$ , $I_B = 375\text{ mAdc}$ )		$V_{CE(sat)}$	—	1.2	Vdc
Base–Emitter On Voltage ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )		$V_{BE(on)}$	—	1.8	Vdc
<b>DYNAMIC CHARACTERISTICS</b>					
Current–Gain — Bandwidth Product ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )		$f_T$	3.0	—	MHz
Small–Signal Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )		$h_{fe}$	20	—	—

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

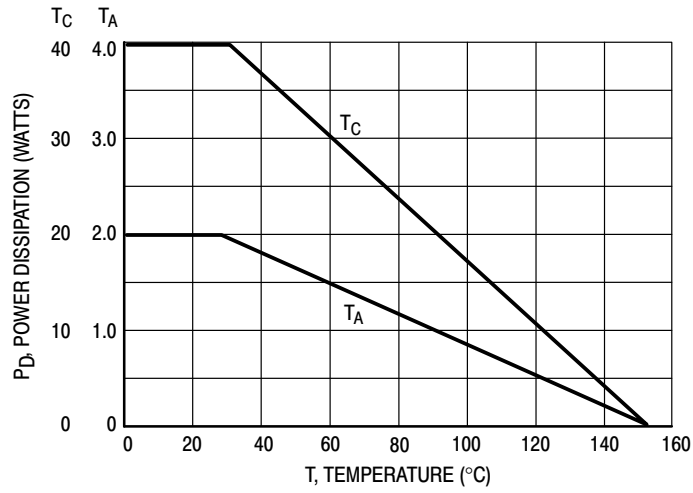
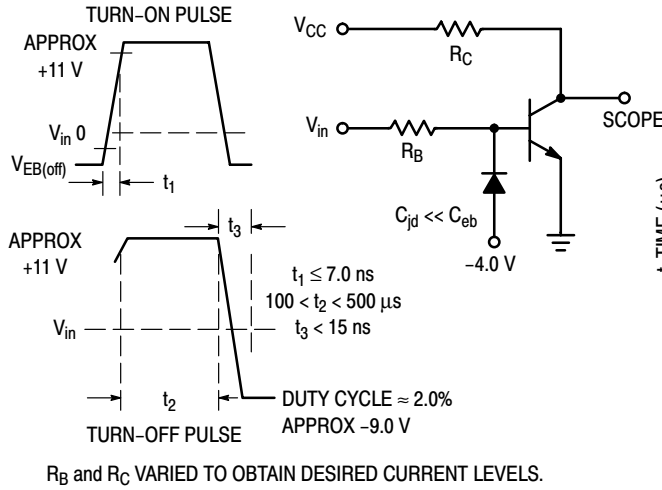


Figure 1. Power Derating



$R_B$  and  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS.

Figure 2. Switching Time Equivalent Circuit

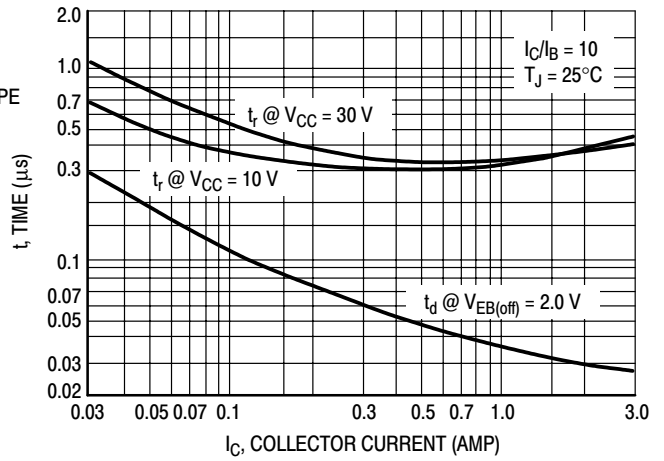


Figure 3. Turn-On Time

TIP31A TIP31B MJF31C TIP31C TIP32A TIP32B TIP32C MJF32C

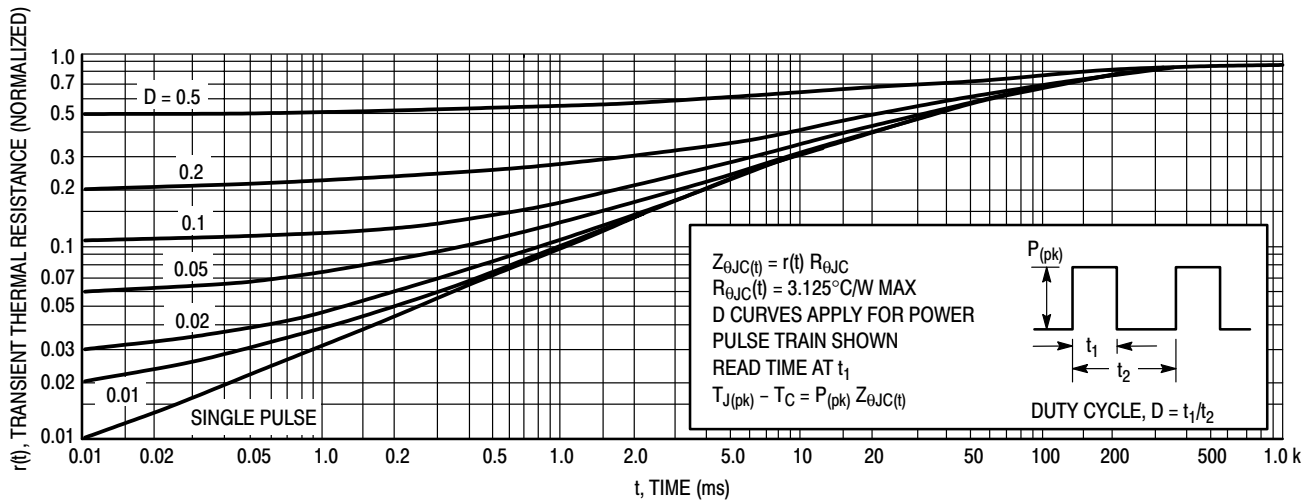


Figure 4. Thermal Response

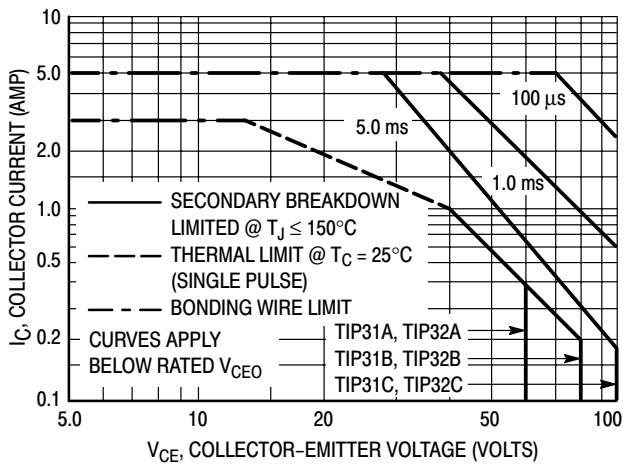


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ}C$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}C$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

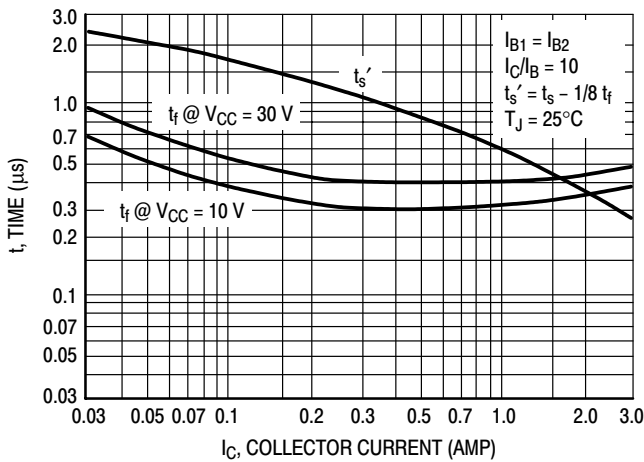


Figure 6. Turn-Off Time

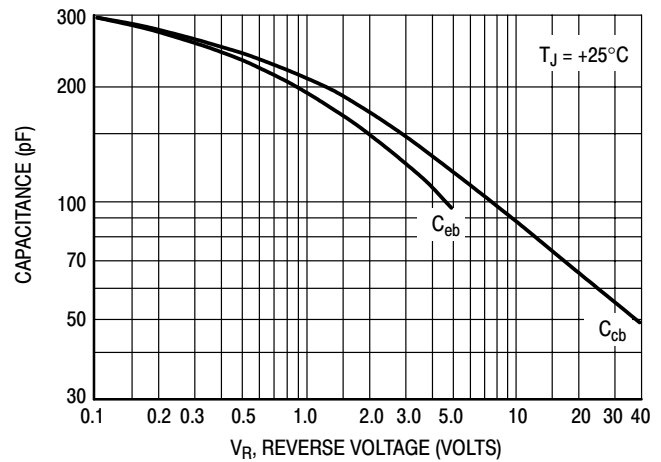


Figure 7. Capacitance

TIP31A TIP31B MJF31C TIP31C TIP32A TIP32B TIP32C MJF32C

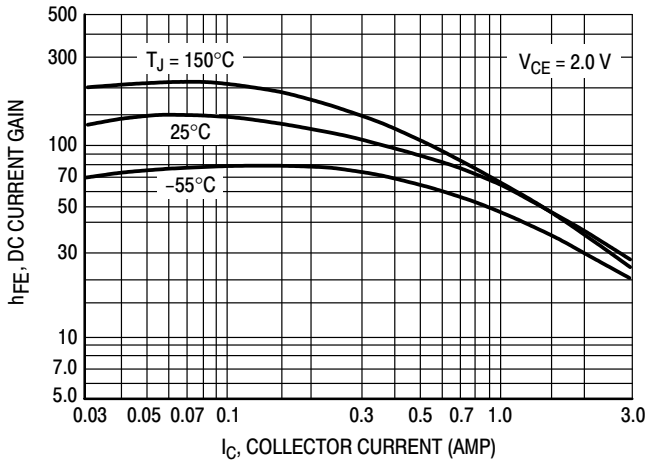


Figure 8. DC Current Gain

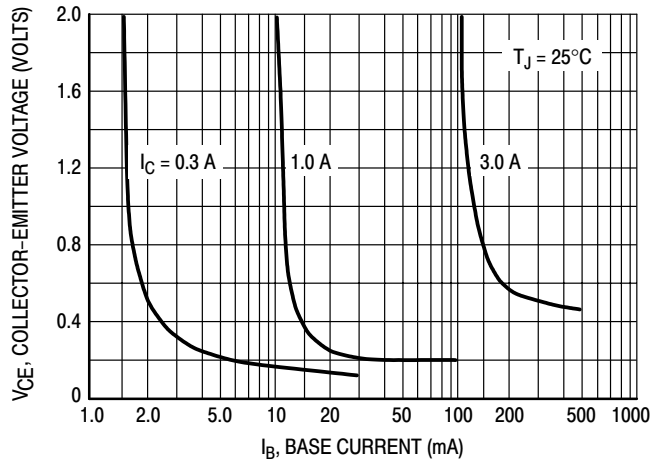


Figure 9. Collector Saturation Region

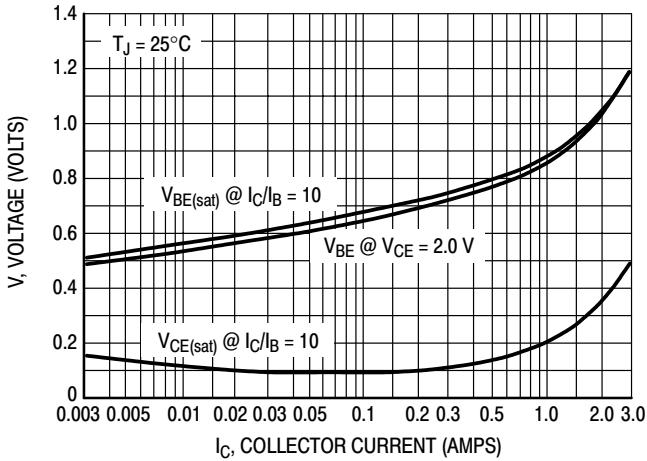


Figure 10. "On" Voltages

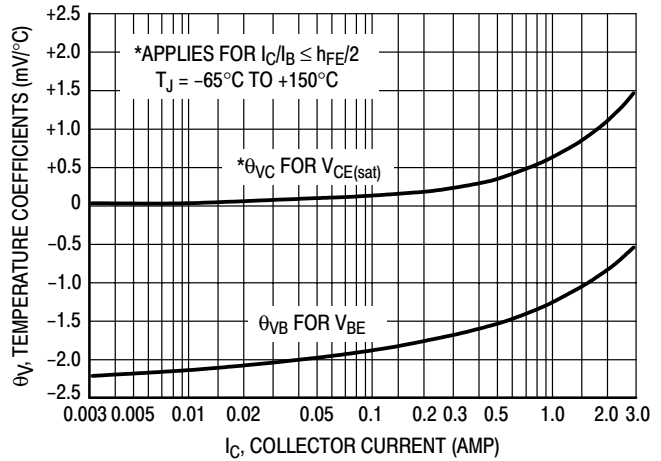


Figure 11. Temperature Coefficients

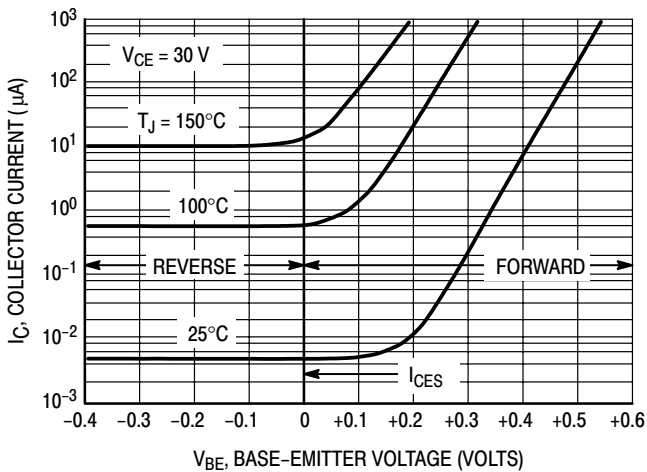


Figure 12. Collector Cut-Off Region

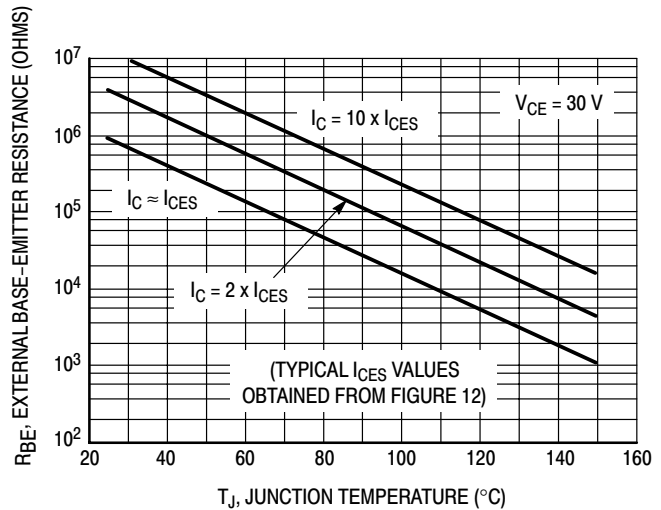


Figure 13. Effects of Base-Emitter Resistance

## Complementary Silicon High-Power Transistors

... for general-purpose power amplifier and switching applications.

- 10 A Collector Current
- Low Leakage Current —  
 $I_{CEO} = 0.7 \text{ mA @ } 60 \text{ V}$
- Excellent dc Gain —  
 $h_{FE} = 40 \text{ Typ @ } 3.0 \text{ A}$
- High Current Gain Bandwidth Product —  
 $h_{fe} = 3.0 \text{ min @ } I_C$   
 $= 0.5 \text{ A,}$   
 $f = 1.0 \text{ MHz}$

### MAXIMUM RATINGS

Rating	Symbol	TIP33C TIP34C	Unit
Collector–Emitter Voltage	$V_{CEO}$	100 V	Vdc
Collector–Base Voltage	$V_{CB}$	100 V	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous Peak (1)	$I_C$	10 15	Adc
Base Current — Continuous	$I_B$	3.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	80 0.64	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

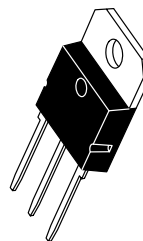
### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^\circ\text{C/W}$
Junction–To–Free–Air Thermal Resistance	$R_{\theta JA}$	35.7	$^\circ\text{C/W}$

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle  $\leq$  10%.

**NPN  
TIP33C  
PNP  
TIP34C**

**10 AMPERE  
COMPLEMENTARY  
SILICON  
POWER TRANSISTORS  
100 VOLTS  
80 WATTS**



**CASE 340D–02  
TO–218AC**

# TIP33C TIP34C

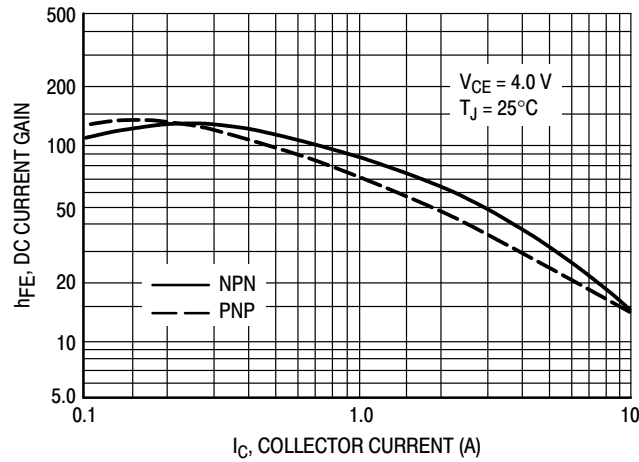


Figure 1. DC Current Gain

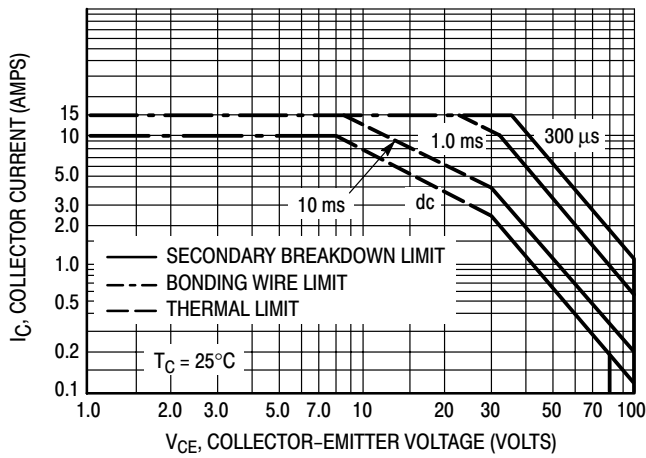
## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30$ mA, $I_B = 0$ )	$V_{CEO(sus)}$	100	—	Vdc
Collector–Emitter Cutoff Current ( $V_{CE} = 60$ V, $I_B = 0$ )	$I_{CEO}$	—	0.7	mA
Collector–Emitter Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB} = 0$ )	$I_{CES}$	—	0.4	mA
Emitter–Base Cutoff Current ( $V_{EB} = 5.0$ V, $I_C = 0$ )	$I_{EBO}$	—	1.0	mA
<b>ON CHARACTERISTICS (1)</b>				
DC Current Gain ( $I_C = 1.0$ A, $V_{CE} = 4.0$ V) ( $I_C = 3.0$ A, $V_{CE} = 4.0$ V)	$h_{FE}$	40 20	— 100	—
Collector–Emitter Saturation Voltage ( $I_C = 3.0$ A, $I_B = 0.3$ A) ( $I_C = 10$ A, $I_B = 2.5$ A)	$V_{CE(sat)}$	— —	1.0 4.0	Vdc
Base–Emitter On Voltage ( $I_C = 3.0$ A, $V_{CE} = 4.0$ V) ( $I_C = 10$ A, $V_{CE} = 4.0$ V)	$V_{BE(on)}$	— —	1.6 3.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Small–Signal Current Gain ( $I_C = 0.5$ A, $V_{CE} = 10$ V, $f = 1.0$ kHz)	$h_{fe}$	20	—	—
Current–Gain — Bandwidth Product ( $I_C = 0.5$ A, $V_{CE} = 10$ V, $f = 1.0$ MHz)	$f_T$	3.0	—	MHz

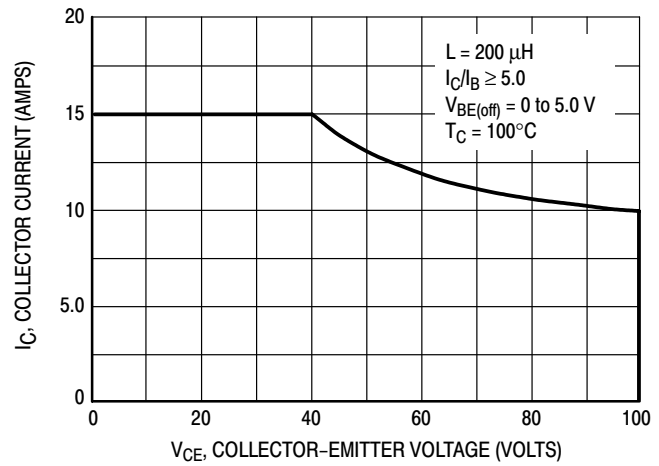
(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



## TIP33C TIP34C



**Figure 2. Maximum Rated Forward Bias Safe Operating Area**



**Figure 3. Maximum Rated Forward Bias Safe Operating Area**

### FORWARD BIAS

The Forward Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during forward bias. The data is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%, and must be derated thermally for  $T_C > 25^\circ\text{C}$ .

### REVERSE BIAS

The Reverse Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during reverse biased turn-off. This rating is verified under clamped conditions so the device is never subjected to an avalanche mode.

## Complementary Silicon High-Power Transistors

... for general-purpose power amplifier and switching applications.

- 25 A Collector Current
- Low Leakage Current —  
 $I_{CEO} = 1.0 \text{ mA @ } 30 \text{ and } 60 \text{ V}$
- Excellent DC Gain —  
 $h_{FE} = 40 \text{ Typ @ } 15 \text{ A}$
- High Current Gain Bandwidth Product —  
 $|h_{fe}| = 3.0 \text{ min @ } I_C$   
 $= 1.0 \text{ A, } f = 1.0 \text{ MHz}$

### MAXIMUM RATINGS

Rating	Symbol	TIP35A TIP36A	TIP35B TIP36B	TIP35C TIP36C	Unit
Collector–Emitter Voltage	$V_{CEO}$	60 V	80 V	100 V	Vdc
Collector–Base Voltage	$V_{CB}$	60 V	80 V	100 V	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous Peak (1)	$I_C$	25 40			Adc
Base Current — Continuous	$I_B$	5.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	125 1.0			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150			$^\circ\text{C}$
Unclamped Inductive Load	$E_{SB}$	90			mJ

### THERMAL CHARACTERISTICS

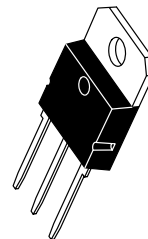
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
Junction–To–Free–Air Thermal Resistance	$R_{\theta JA}$	35.7	$^\circ\text{C/W}$

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle  $\leq 10\%$ .

**NPN**  
**TIP35A**  
**TIP35B\***  
**TIP35C\***  
**PNP**  
**TIP36A**  
**TIP36B\***  
**TIP36C\***

\*ON Semiconductor Preferred Device

**25 AMPERE  
 COMPLEMENTARY  
 SILICON  
 POWER TRANSISTORS  
 60–100 VOLTS  
 125 WATTS**



**CASE 340D–02  
 TO–218AC**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

TIP35A TIP35B TIP35C TIP36A TIP36B TIP36C

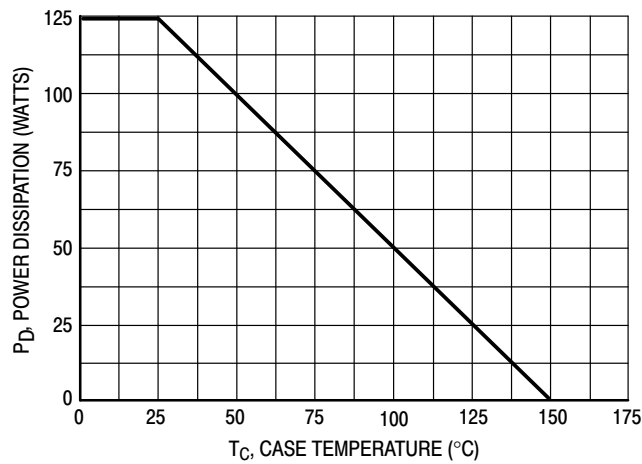


Figure 1. Power Derating

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CE(sus)}$	60 80 100	—	Vdc
Collector–Emitter Cutoff Current ( $V_{CE} = 30\text{ V}$ , $I_B = 0$ ) ( $V_{CE} = 60\text{ V}$ , $I_B = 0$ )	$I_{CEO}$	— —	1.0 1.0	mA
Collector–Emitter Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB} = 0$ )	$I_{CES}$	—	0.7	mA
Emitter–Base Cutoff Current ( $V_{EB} = 5.0\text{ V}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mA
<b>ON CHARACTERISTICS (1)</b>				
DC Current Gain ( $I_C = 1.5\text{ A}$ , $V_{CE} = 4.0\text{ V}$ ) ( $I_C = 15\text{ A}$ , $V_{CE} = 4.0\text{ V}$ )	$h_{FE}$	25 15	— 75	—
Collector–Emitter Saturation Voltage ( $I_C = 15\text{ A}$ , $I_B = 1.5\text{ A}$ ) ( $I_C = 25\text{ A}$ , $I_B = 5.0\text{ A}$ )	$V_{CE(sat)}$	— —	1.8 4.0	Vdc
Base–Emitter On Voltage ( $I_C = 15\text{ A}$ , $V_{CE} = 4.0\text{ V}$ ) ( $I_C = 25\text{ A}$ , $V_{CE} = 4.0\text{ V}$ )	$V_{BE(on)}$	— —	2.0 4.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Small–Signal Current Gain ( $I_C = 1.0\text{ A}$ , $V_{CE} = 10\text{ V}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	25	—	—
Current–Gain — Bandwidth Product ( $I_C = 1.0\text{ A}$ , $V_{CE} = 10\text{ V}$ , $f = 1.0\text{ MHz}$ )	$f_T$	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

TIP35A TIP35B TIP35C TIP36A TIP36B TIP36C

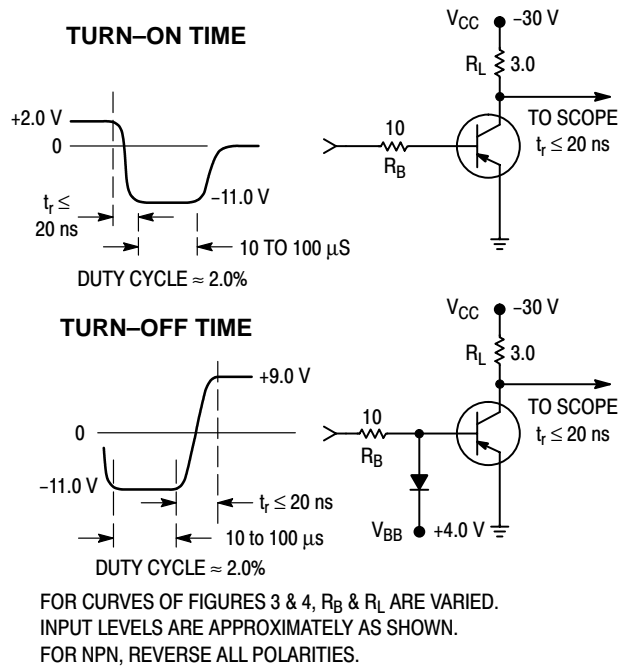


Figure 2. Switching Time Equivalent Test Circuits

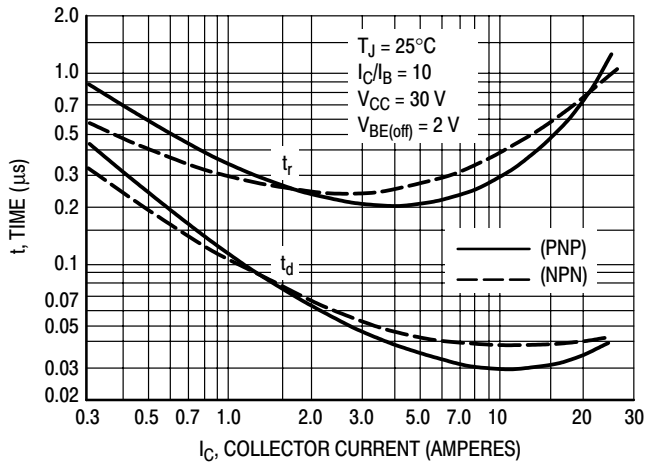


Figure 3. Turn-On Time

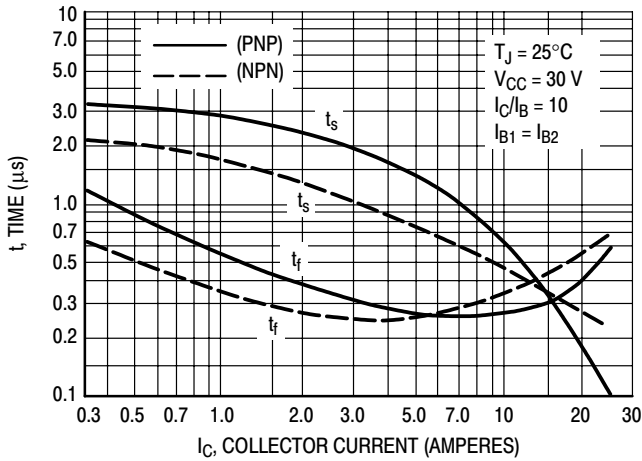


Figure 4. Turn-Off Time

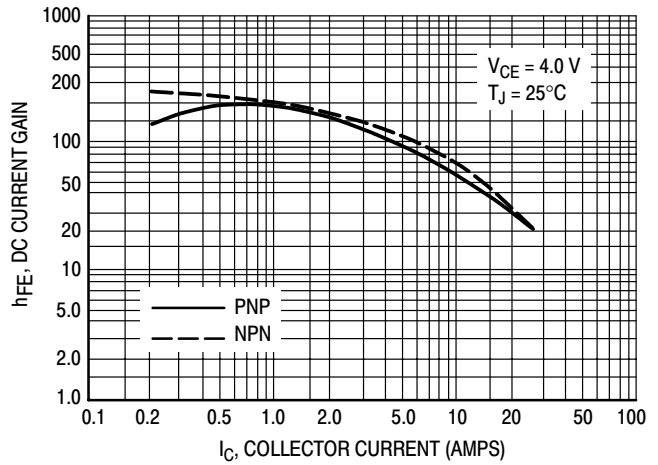


Figure 5. DC Current Gain

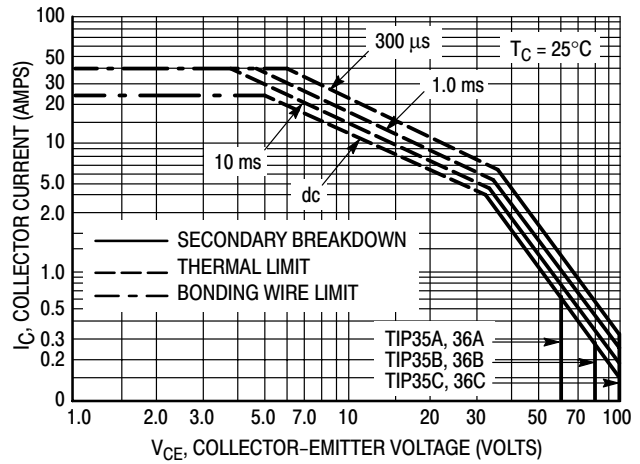
**FORWARD BIAS**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

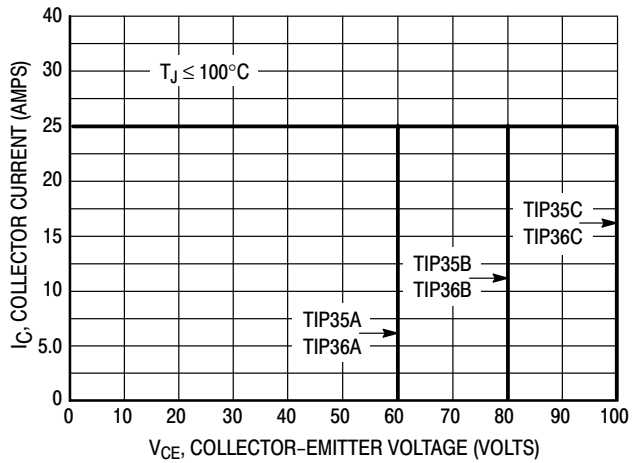
The data of Figure 6 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations.

**REVERSE BIAS**

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.



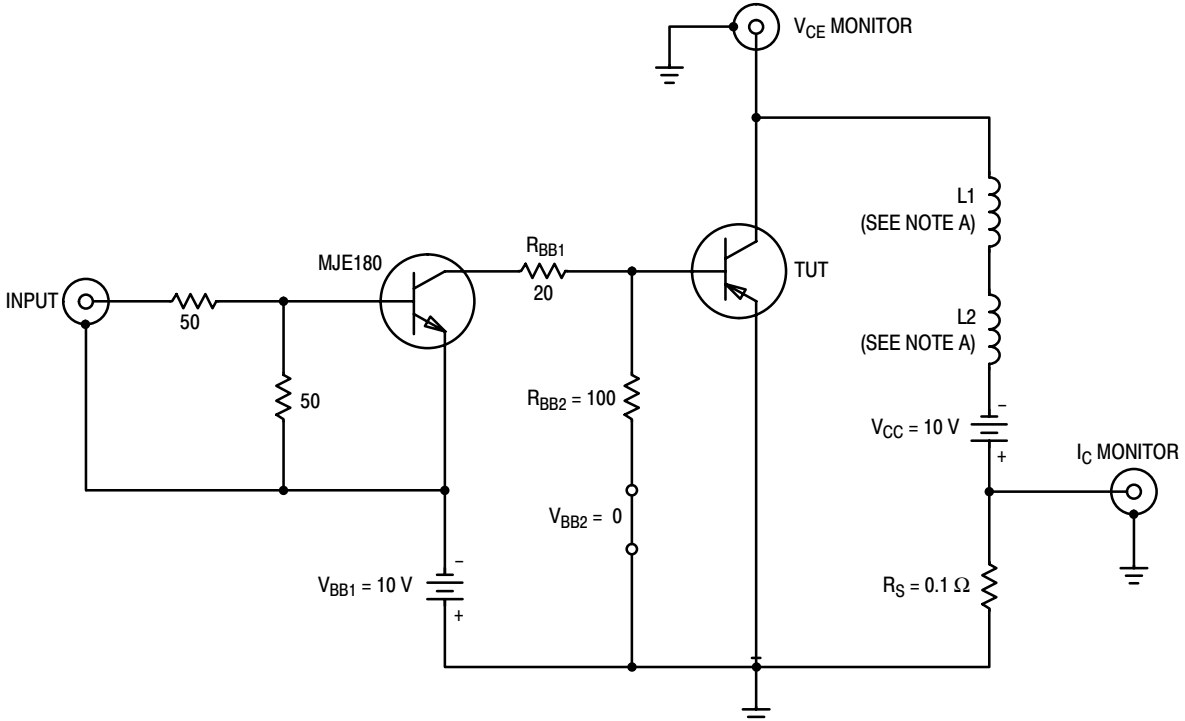
**Figure 6. Maximum Rated Forward Bias Safe Operating Area**



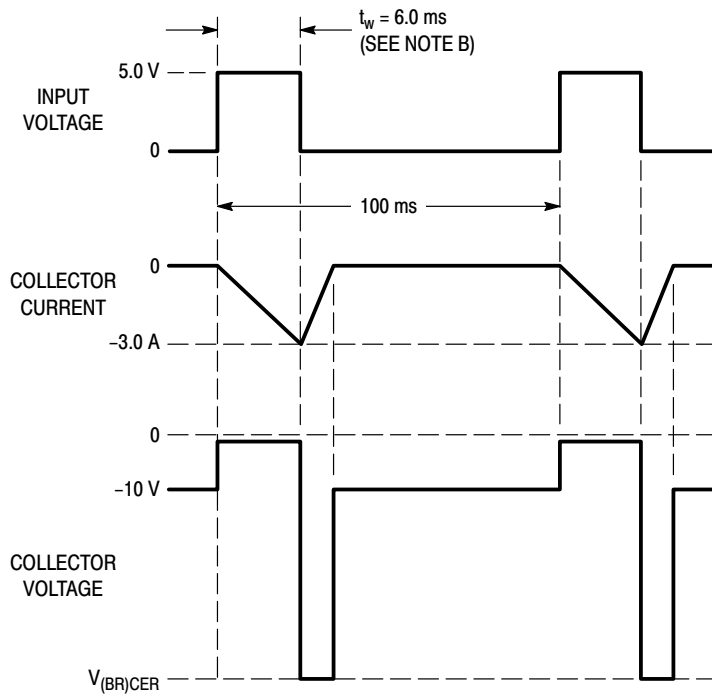
**Figure 7. Maximum Rated Forward Bias Safe Operating Area**

TIP35A TIP35B TIP35C TIP36A TIP36B TIP36C

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



NOTES:

- A. L1 and L2 are 10 mH, 0.11  $\Omega$ , Chicago Standard Transformer Corporation C-2688, or equivalent.
- B. Input pulse width is increased until  $I_{CM} = -3.0$  A.
- C. For NPN, reverse all polarities.

Figure 8. Inductive Load Switching

# Complementary Silicon Plastic Power Transistors

... designed for use in general purpose amplifier and switching applications.

- Collector–Emitter Saturation Voltage —  
 $V_{CE(sat)} = 1.5 \text{ Vdc (Max) @ } I_C = 6.0 \text{ Adc}$
- Collector–Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 60 \text{ Vdc (Min) — TIP41A, TIP42A}$   
 $= 80 \text{ Vdc (Min) — TIP41B, TIP42B}$   
 $= 100 \text{ Vdc (Min) — TIP41C, TIP42C}$
- High Current Gain — Bandwidth Product  
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 500 \text{ mAdc}$
- Compact TO–220 AB Package

**\*MAXIMUM RATINGS**

Rating	Symbol	TIP41A TIP42A	TIP41B TIP42B	TIP41C TIP42C	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	80	100	Vdc
Collector–Base Voltage	$V_{CB}$	60	80	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous Peak	$I_C$	6 10			Adc
Base Current	$I_B$	2.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	65 0.52			Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016			Watts W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (1)	E	62.5			mJ
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150			$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

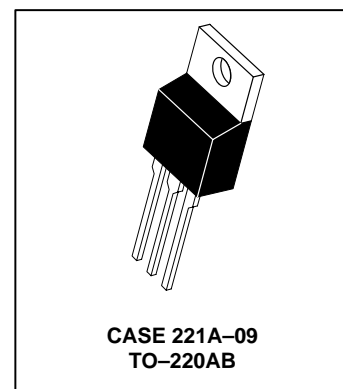
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C/W}$

(1)  $I_C = 2.5 \text{ A, } L = 20 \text{ mH, P.R.F.} = 10 \text{ Hz, } V_{CC} = 10 \text{ V, } R_{BE} = 100 \Omega.$

**NPN**  
**TIP41A**  
**TIP41B\***  
**TIP41C\***  
**PNP**  
**TIP42A**  
**TIP42B\***  
**TIP42C\***

\*ON Semiconductor Preferred Device

**6 AMPERE**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**60–80–100 VOLTS**  
**65 WATTS**



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

# TIP41A TIP41B TIP41C TIP42A TIP42B TIP42C

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) (I <sub>C</sub> = 30 mAdc, I <sub>B</sub> = 0)	TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	V <sub>CEO(sus)</sub>	60 80 100	— — — Vdc
Collector Cutoff Current (V <sub>CE</sub> = 30 Vdc, I <sub>B</sub> = 0) (V <sub>CE</sub> = 60 Vdc, I <sub>B</sub> = 0)	TIP41A, TIP42A TIP41B, TIP41C TIP42B, TIP42C	I <sub>CEO</sub>	— — —	0.7 0.7 0.7 mAdc
Collector Cutoff Current (V <sub>CE</sub> = 60 Vdc, V <sub>EB</sub> = 0) (V <sub>CE</sub> = 80 Vdc, V <sub>EB</sub> = 0) (V <sub>CE</sub> = 100 Vdc, V <sub>EB</sub> = 0)	TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	I <sub>CES</sub>	— — —	400 400 400 μAdc
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)		I <sub>EBO</sub>	—	1.0 mAdc
<b>ON CHARACTERISTICS (1)</b>				
DC Current Gain (I <sub>C</sub> = 0.3 Adc, V <sub>CE</sub> = 4.0 Vdc) (I <sub>C</sub> = 3.0 Adc, V <sub>CE</sub> = 4.0 Vdc)		h <sub>FE</sub>	30 15	— 75 —
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 6.0 Adc, I <sub>B</sub> = 600 mAdc)		V <sub>CE(sat)</sub>	—	1.5 Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 6.0 Adc, V <sub>CE</sub> = 4.0 Vdc)		V <sub>BE(on)</sub>	—	2.0 Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain — Bandwidth Product (I <sub>C</sub> = 500 mAdc, V <sub>CE</sub> = 10 Vdc, f <sub>test</sub> = 1.0 MHz)		f <sub>T</sub>	3.0	— MHz
Small–Signal Current Gain (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1.0 kHz)		h <sub>fe</sub>	20	— —

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



TIP41A TIP41B TIP41C TIP42A TIP42B TIP42C

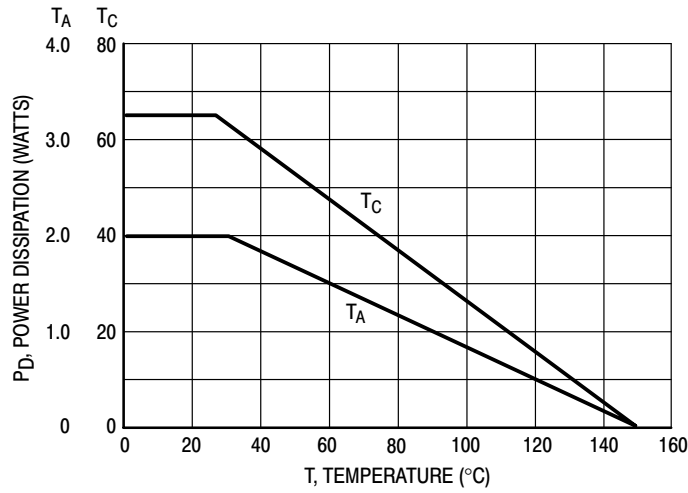


Figure 1. Power Derating

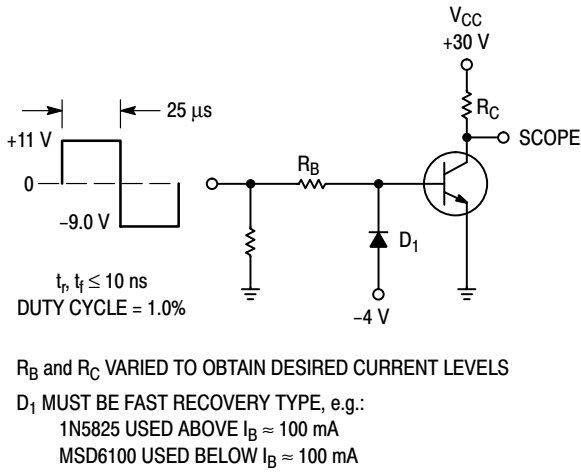


Figure 2. Switching Time Test Circuit

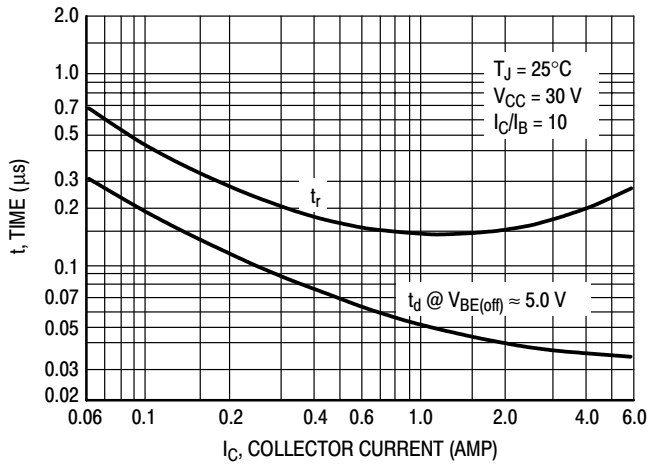


Figure 3. Turn-On Time

TIP41A TIP41B TIP41C TIP42A TIP42B TIP42C

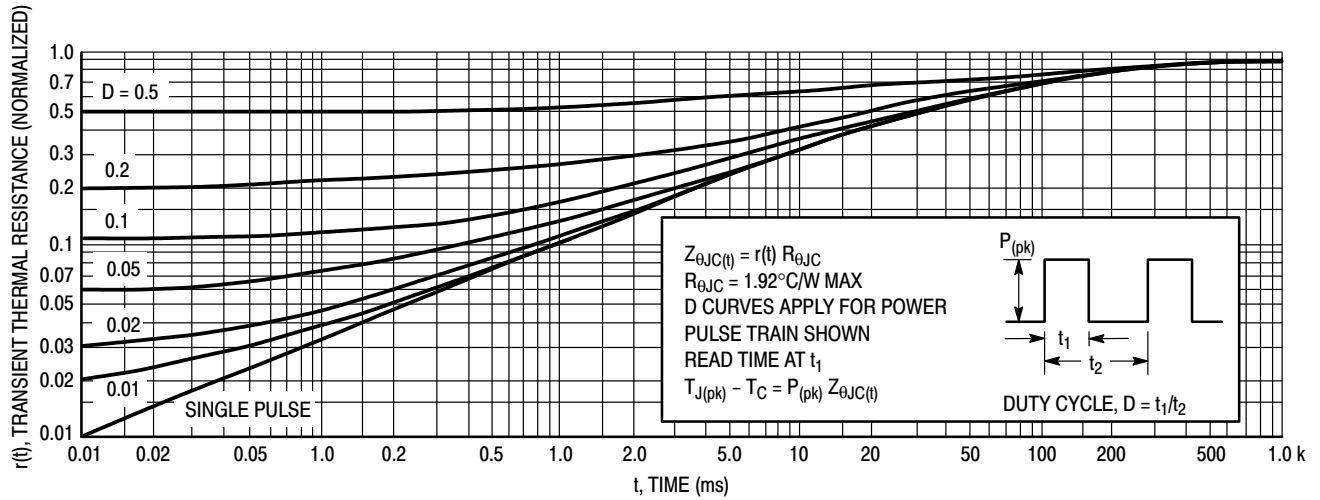


Figure 4. Thermal Response

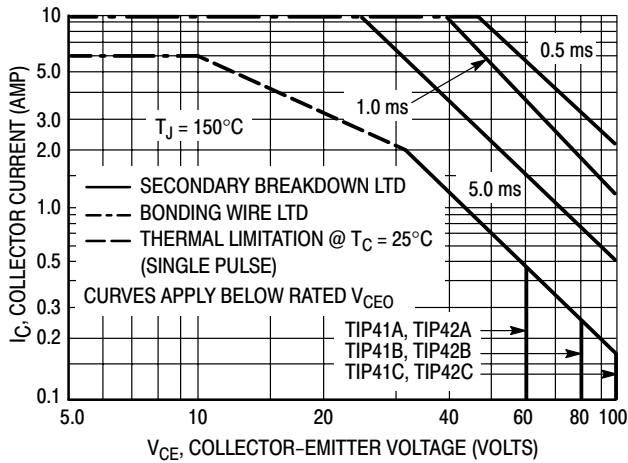


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

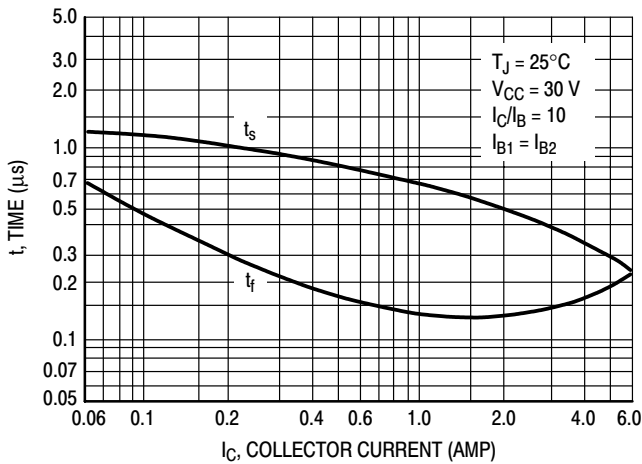


Figure 6. Turn-Off Time

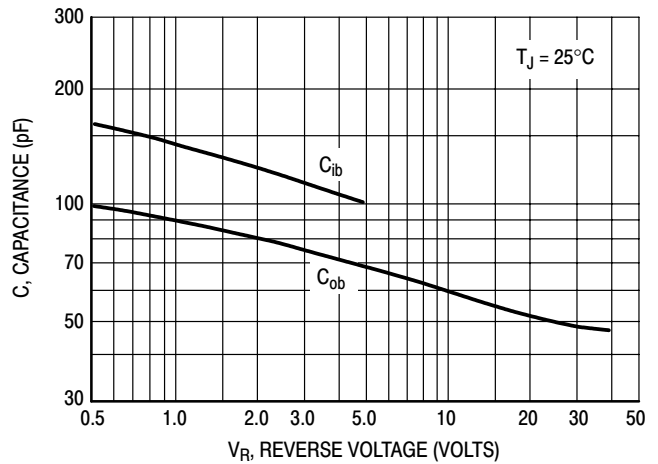


Figure 7. Capacitance

TIP41A TIP41B TIP41C TIP42A TIP42B TIP42C

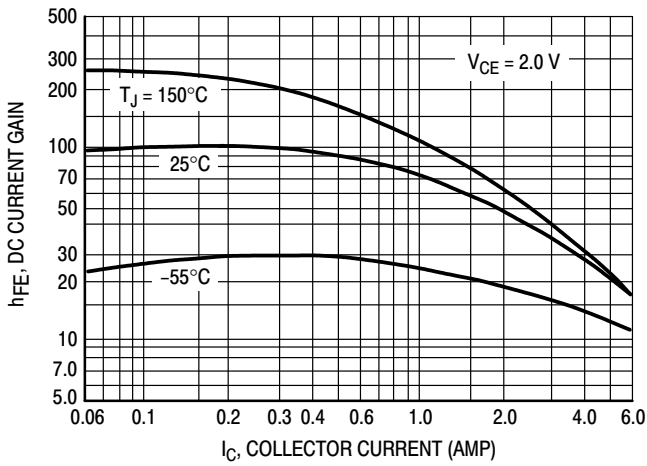


Figure 8. DC Current Gain

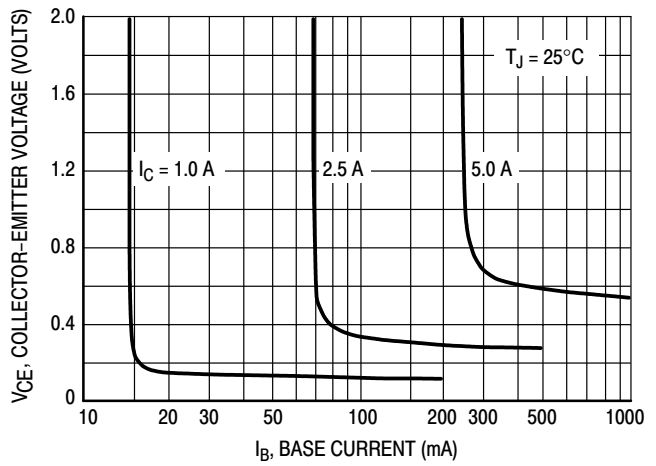


Figure 9. Collector Saturation Region

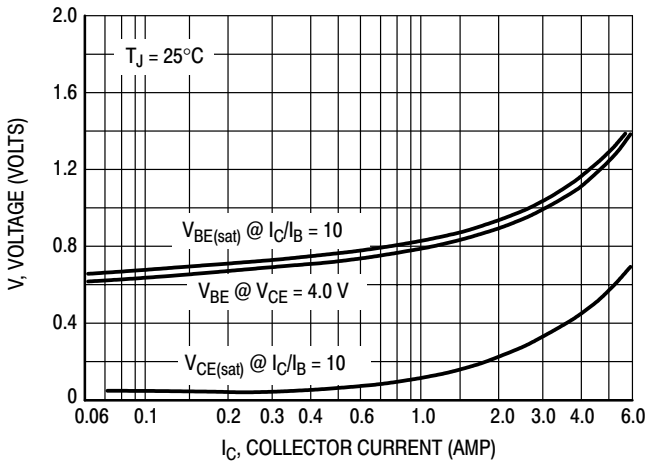


Figure 10. "On" Voltages

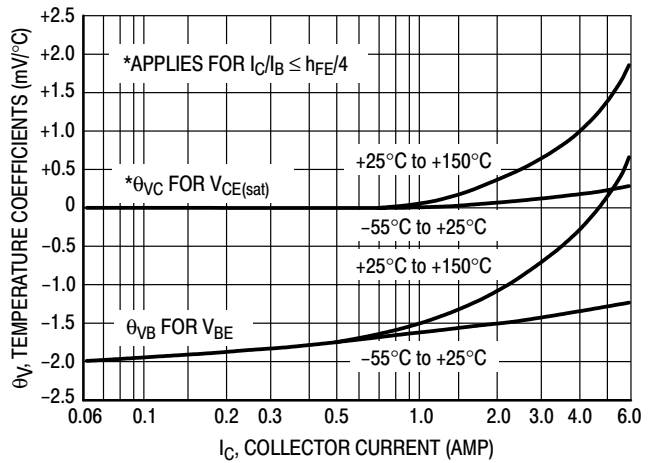


Figure 11. Temperature Coefficients

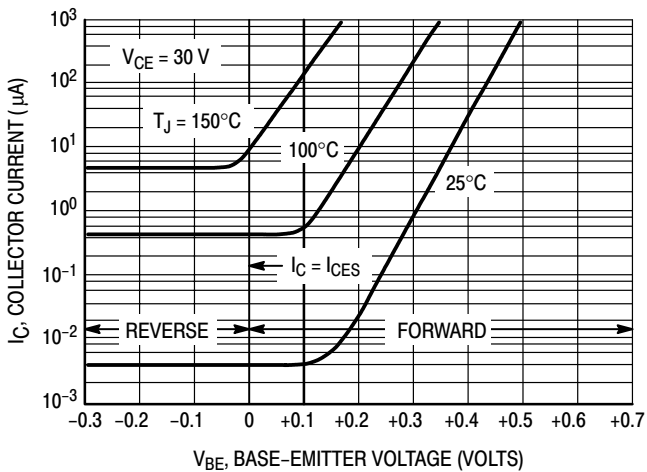


Figure 12. Collector Cut-Off Region

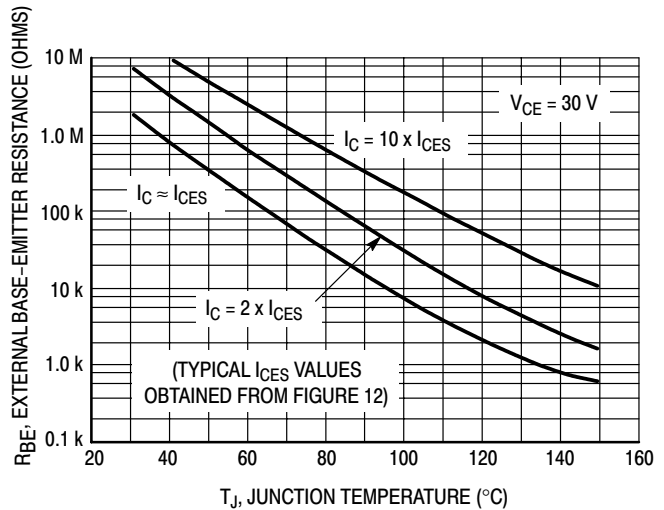


Figure 13. Effects of Base-Emitter Resistance

# High Voltage NPN Silicon Power Transistors

... designed for line operated audio output amplifier, SWITCHMODE™ power supply drivers and other switching applications.

- 250 V to 400 V (Min) —  $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Popular TO-220 Plastic Package

## MAXIMUM RATINGS

Rating	Symbol	TIP47	TIP48	TIP50	Unit
Collector–Emitter Voltage	$V_{CEO}$	250	300	400	Vdc
Collector–Base Voltage	$V_{CB}$	350	400	500	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous	$I_C$	1.0			Adc
Peak		2.0			
Base Current	$I_B$	0.6			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40			Watts
		0.32			W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0			Watts
		0.016			W/ $^\circ\text{C}$
Unclamped Inducting Load Energy (See Figure 8)	E	20			mJ
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150			$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

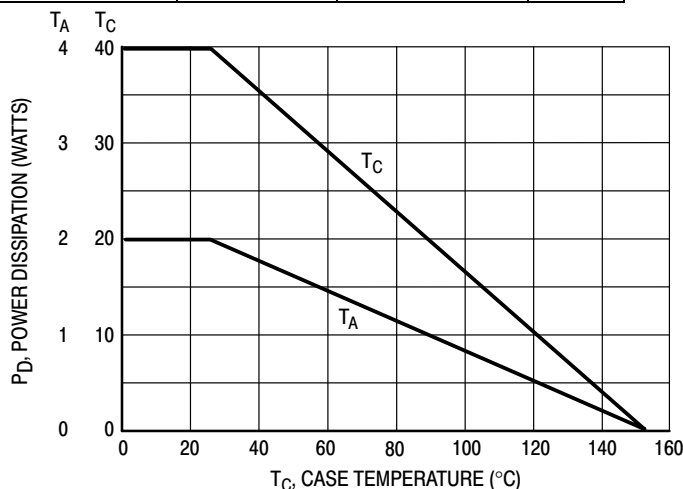


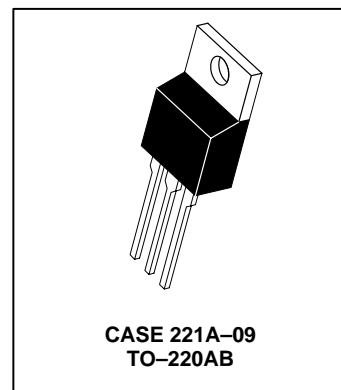
Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

**TIP47\***  
**TIP48\***  
**TIP50\***

\*ON Semiconductor Preferred Device

**1.0 AMPERE  
 POWER TRANSISTORS  
 NPN SILICON  
 250–300–350–400 VOLTS  
 40 WATTS**



# TIP47 TIP48 TIP50

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	TIP47 TIP48 TIP50	$V_{CEO(sus)}$	250 300 400	— — —	Vdc
Collector Cutoff Current ( $V_{CE} = 150\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 200\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 300\text{ Vdc}$ , $I_B = 0$ )	TIP47 TIP48 TIP50	$I_{CEO}$	— — —	1.0 1.0 1.0	mAdc
Collector Cutoff Current ( $V_{CE} = 350\text{ Vdc}$ , $V_{BE} = 0$ ) ( $V_{CE} = 400\text{ Vdc}$ , $V_{BE} = 0$ ) ( $V_{CE} = 500\text{ Vdc}$ , $V_{BE} = 0$ )	TIP47 TIP48 TIP50	$I_{CES}$	— — —	1.0 1.0 1.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	—	1.0	mAdc

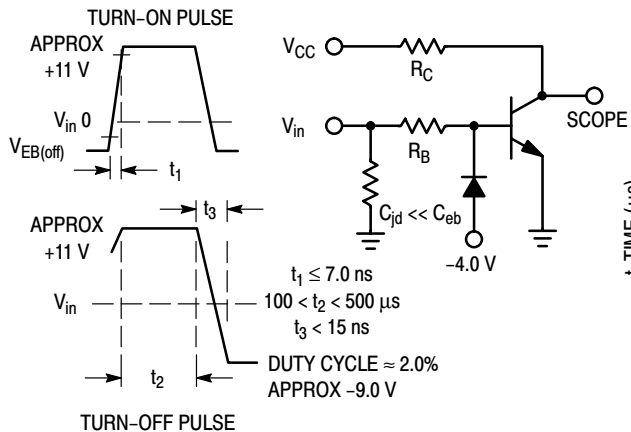
## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 0.3\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ )	$h_{FE}$	30 10	150 —	—
Collector–Emitter Saturation Voltage ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	$V_{CE(sat)}$	—	1.0	Vdc
Base–Emitter On Voltage ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ )	$V_{BE(on)}$	—	1.5	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 0.1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 2.0\text{ MHz}$ )	$f_T$	10	—	MHz
Small–Signal Current Gain ( $I_C = 0.2\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	25	—	—

(1) Pulse Test: Pulse width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



$R_B$  and  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS.

Figure 2. Switching Time Equivalent Circuit

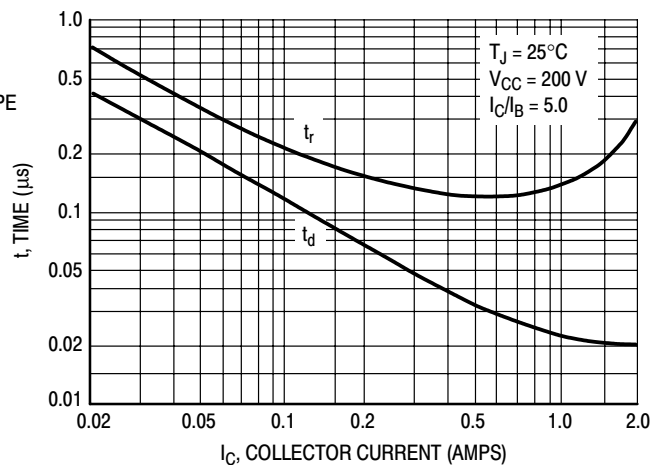


Figure 3. Turn-On Time

# TIP47 TIP48 TIP50

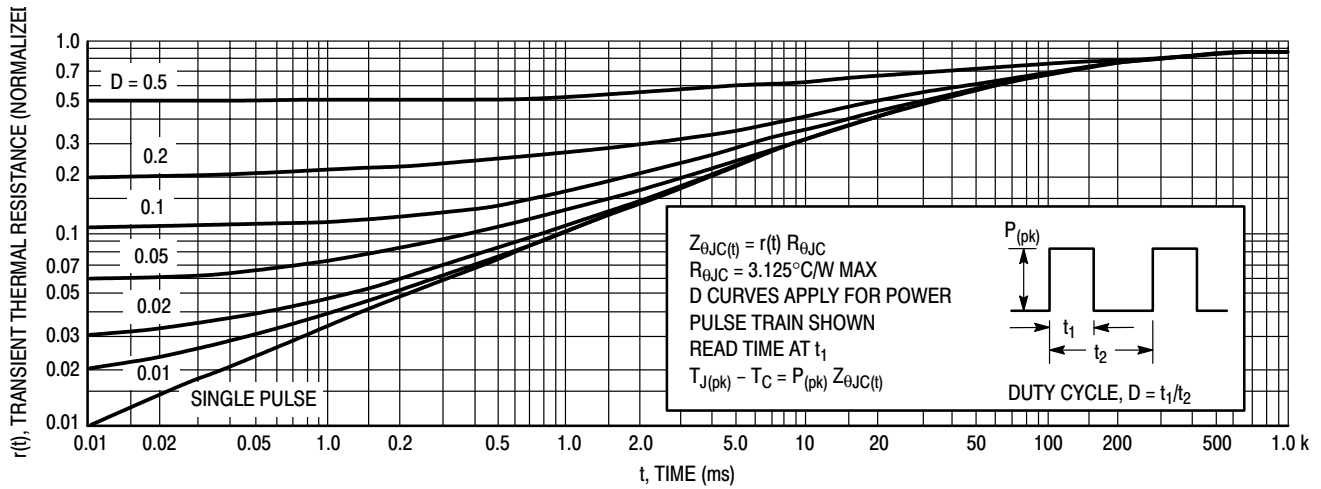


Figure 4. Thermal Response

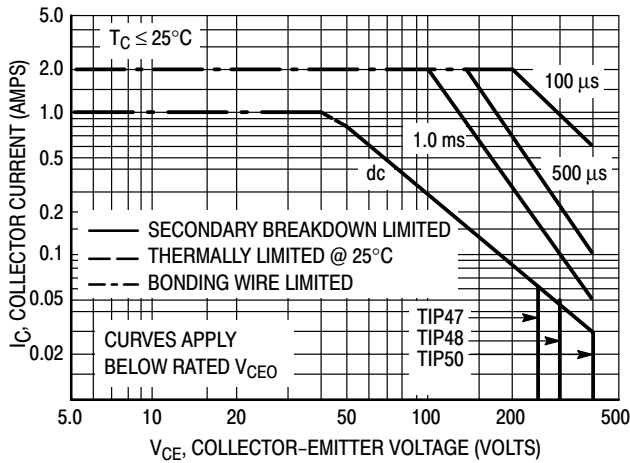


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

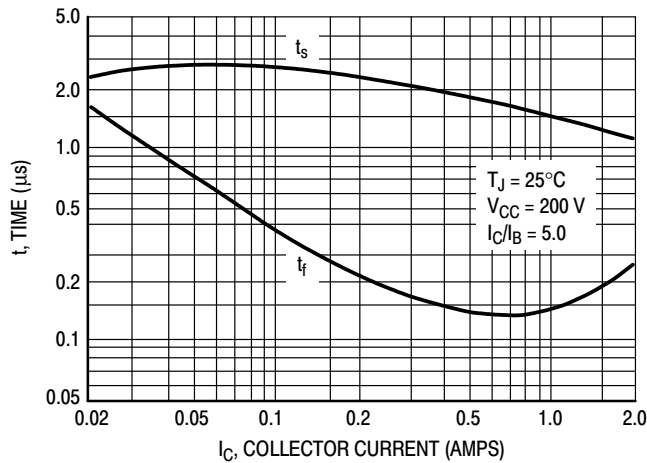


Figure 6. Turn-Off Time

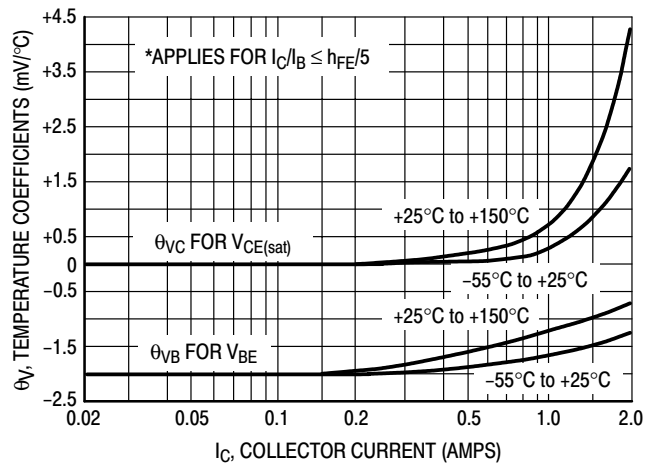
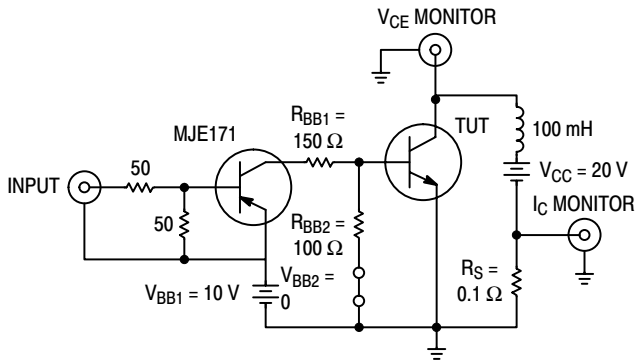


Figure 7. Temperature Coefficients

TIP47 TIP48 TIP50



Note A: Input pulse width is increased until  $I_{CM} = 0.63$  A.

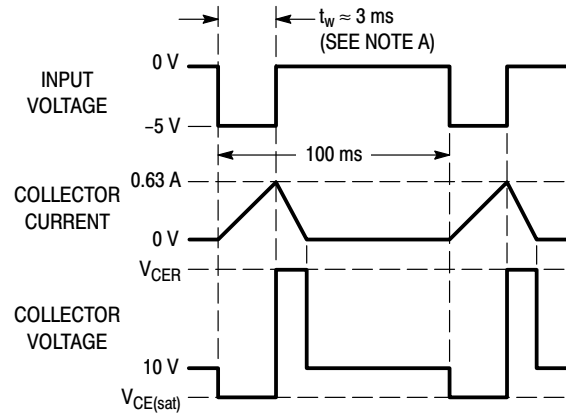


Figure 8. Inductive Load Switching

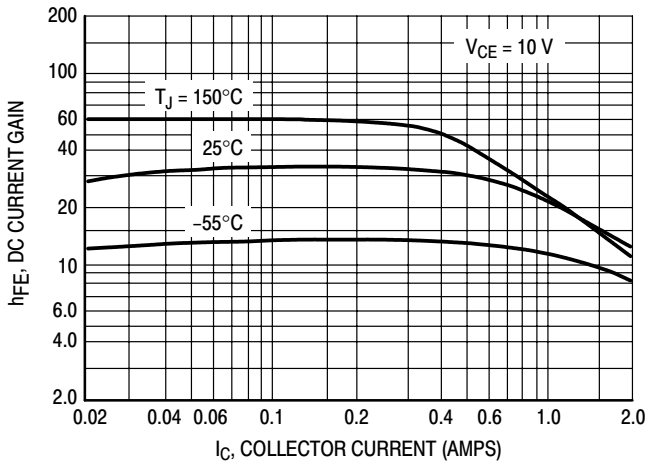


Figure 9. DC Current Gain

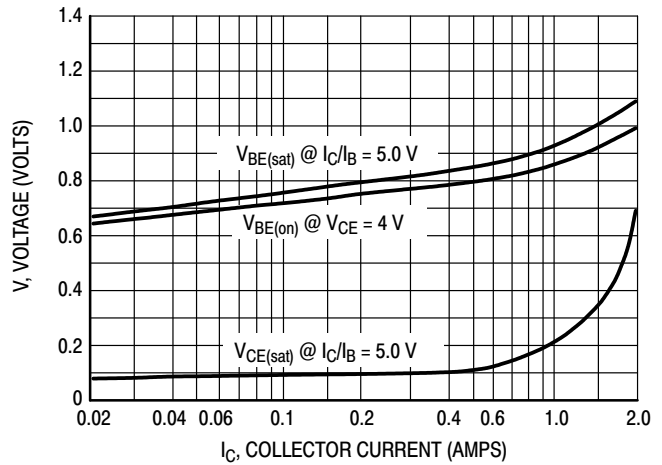


Figure 10. "On" Voltages

# **CHAPTER 3**

## **Applications Information and Case Outlines**

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## A High-Performance Video Amplifier for High Resolution CRT Applications



ON Semiconductor™

<http://onsemi.com>

### APPLICATION NOTE

Prepared by: Bill Roehr

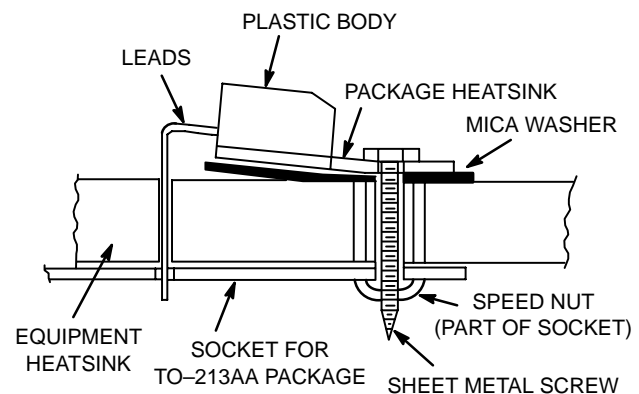
#### INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one-half for a decrease in junction temperature from 160°C to 135°C.<sup>(1)</sup> Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.<sup>(2)</sup> Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic-packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

Figure 1 shows an example of doing nearly everything wrong. A tab mount TO-220 package is shown being used as a replacement for a TO-213AA (TO-66) part which was socket mounted. To use the socket, the leads are bent – an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet-metal screw through a 1/4" hole containing a fiber-insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition, the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than

expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all, poor mounting practices would be covered.



**Figure 1. Extreme Case of Improperly Mounting a Semiconductor (Distortion Exaggerated)**

In many situations, the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

- Stud Mount
- Flange Mount
- Pressfit
- Plastic Body Mount
- Tab Mount
- Surface Mount

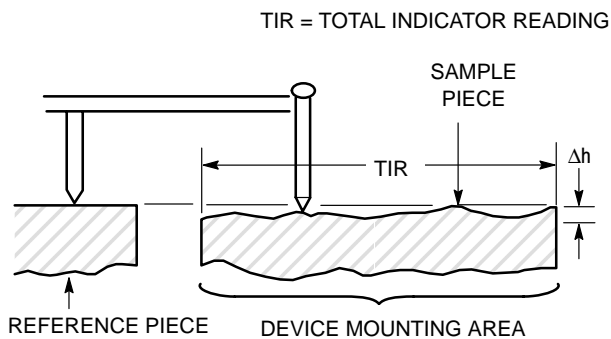
Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests. Appendix C indicates the type of accessories supplied by a number of manufacturers.

### MOUNTING SURFACE PREPARATION

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

#### Surface Flatness

Surface flatness is determined by comparing the variance in height ( $\Delta h$ ) of the test specimen to that of a reference standard as indicated in Figure 2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e.,  $\Delta h/TIR$ , if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.



**Figure 2. Surface Flatness Measurement**

#### Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy, Inc., using a copper TO-204 (TO-3) package with a typical 32-microinch finish, showed that heatsink finishes between 16 and 64  $\mu$ -in caused less than  $\pm 2.5\%$  difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.<sup>(3)</sup> Most commercially available cast or extruded heatsinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

#### Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO-3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

#### Surface Treatment

Many aluminum heatsinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical, but negligible thermal insulation; it need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromateacid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

### INTERFACE DECISIONS

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise, the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock-marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal, therefore, they partially fill voids when under pressure.

#### Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well-mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct, a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range is less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

### Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a

greased bare joint and a joint using Grafoil®, a dry graphite compound, is shown in the data of Figure 3 through Figure 6. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called Kon-Dux™. It is made with a unique, grain oriented, flake-like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

**Table 1. Approximate Values for Interface Thermal Resistance Data from Measurements Performed in ON Semiconductor Applications Engineering Laboratory**

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions.

Unless otherwise noted, the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						See Note
		Test Torque In-Lb	Metal-to-Metal		With Insulator			
JEDEC Outlines	Description			Dry	Lubed	Dry	Lubed	Type
DO-203AA, TO-210AA TO-208AB	10-32 Stud 7/16" Hex	15	0.3	0.2	1.6	0.8	3 mil Mica	
DO-203AB, TO-210AC TO-208	1/4-28 Stud 11/16" Hex	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO-208AA	Pressfit, 1/2"	–	0.15	0.1	–	–	–	
TO-204AA (TO-3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO-213AA (TO-66)	Diamond Flange	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO-126	Thermopad 1/4" x 3/8"	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO-220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figure 3 through Figure 7 for additional data on TO-3 and TO-220 packages.

2. Screw not insulated. See Figure 20.

### INSULATION CONSIDERATIONS

Since most power semiconductors use vertical device construction, it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non-isolated packages. In

these situations, insulators are used to isolate the individual components from the heatsink. Newer packages, such as the ON Semiconductor FULLPAK™ and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

### Insulator Thermal Resistance

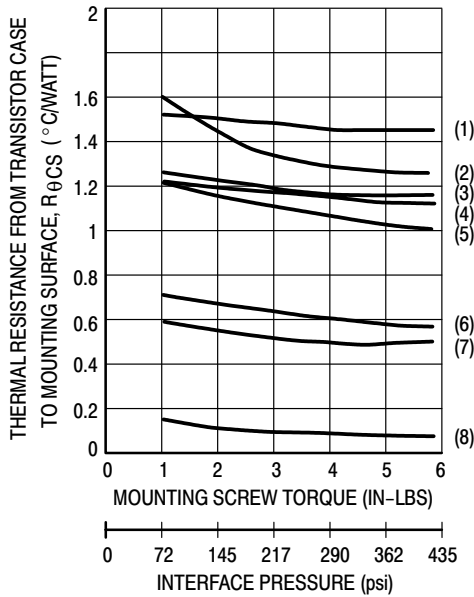
When an insulator is used, thermal grease is of greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials, reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO-204 (TO-3) and TO-220 packages, are shown in Figure 3 through Figure 6, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 3 through Figure 6, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraded, as the dust is

highly toxic.) Thermafilm® is a filled polyimide material which is used for isolation (variation of Kapton®). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost, but it certainly should be used with grease.



- (1) Thermafilm, .002 (.05) thick.
  - (2) Mica, .003 (.08) thick.
  - (3) Mica, .002 (.05) thick.
  - (4) Hard anodized, .020 (.51) thick.
  - (5) Aluminum oxide, .062 (1.57) thick.
  - (6) Beryllium oxide, .062 (1.57) thick.
  - (7) Bare joint – no finish.
  - (8) Grafoil, .005 (.13) thick.\*
- \*Grafoil is not an insulating material.

Figure 3. TO-204AA (TO-3) Without Thermal Grease

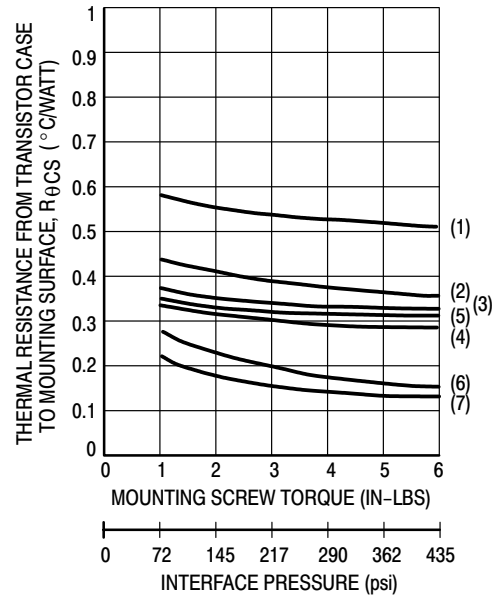
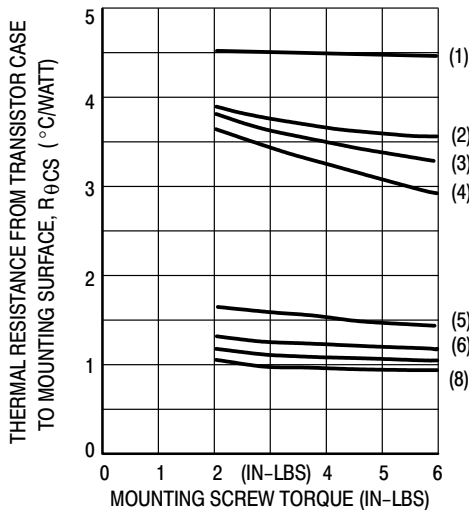


Figure 4. TO-204AA (TO-3) With Thermal Grease



- (1) Thermafilm, .002 (.05) thick.
  - (2) Mica, .003 (.08) thick.
  - (3) Mica, .002 (.05) thick.
  - (4) Hard anodized, .020 (.51) thick.
  - (5) Thermasil II, .009 (.23) thick.
  - (6) Thermasil III, .0076 (.15) thick.
  - (7) Bare joint – no finish.
  - (8) Grafoil, .005 (.13) thick.\*
- \*Grafoil is not an insulating material.

Figure 5. TO-220 Without Thermal Grease

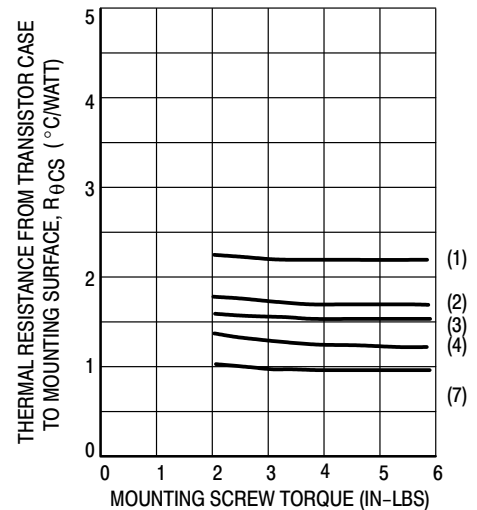


Figure 6. TO-220 With Thermal Grease

INTERFACE THERMAL RESISTANCE FOR TO-204, TO-3, AND TO-220 PACKAGES USING DIFFERENT INSULATING MATERIALS AS A FUNCTION OF MOUNTING SCREW TORQUE (DATA COURTESY THERMALLOY)

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut-through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By comparing Figure 5 and Figure 6, it can be noted that Thermasil™, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica for the TO-220 package.

A number of manufacturers offer silicone rubber insulators. Table 2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out-of-flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K-10® pad, for example, is described as having about 2/3 the interface resistance of the Sil-Pad® 1000 which would place its performance close to the Chomerics 1671 pad. Aavid also offers an isolated pad called Rubber-Duc™, however, it is only available vulcanized to a heatsink and, therefore, was not included in the comparison. Published data from Aavid shows  $R_{\theta CS}$  below  $0.3^{\circ}\text{C}/\text{W}$  for pressures above 500 psi. However, surface flatness and other details are not specified, so a comparison cannot be made with other data in this note.

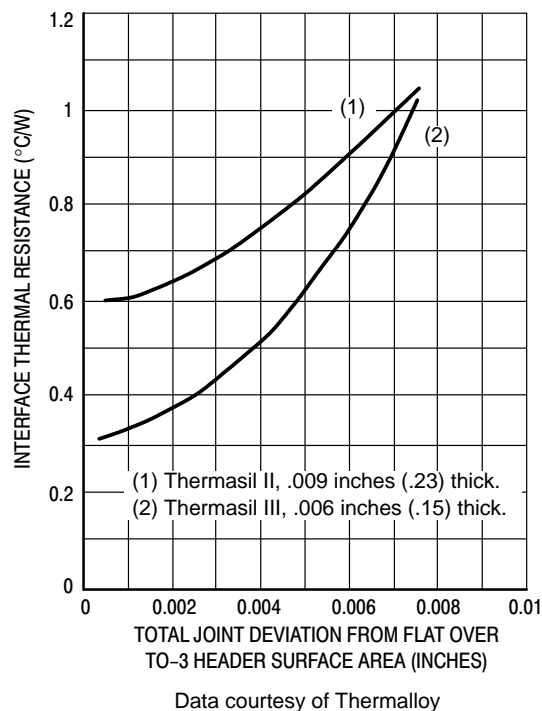
**Table 2. Thermal Resistance of Silicone Rubber Pads**

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173-7	.790	1.175
Bergquist	Sil-Pad K-4®	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil-Pad 400-9®	.735	1.205
Thermalloy	Thermasil II	.680	1.045
Shin-Etsu	TC-30AG	.664	1.260
Bergquist	Sil-Pad 400-7®	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174-9	.574	.755
Bergquist	Sil-Pad 1000®	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermasil III	.440	1.035
Chomerics	1671	.367	.655

\*Test Fixture Deviation from flat from Thermalloy EIR86-1010.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO-204AA (TO-3) package insulated with Thermasil is shown in Figure 7. Observe that the “worst case” encountered (7.5 mils) yields results having about twice the thermal resistance of the “typical case” (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased

mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.



**Figure 7. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators**

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the CHO-THERM® 1688 pad thermal interface impedance dropped from  $0.90^{\circ}\text{C}/\text{W}$  to  $0.70^{\circ}\text{C}/\text{W}$  at the end of 1000 hours. Most of the change occurred during the first 200 hours where  $R_{\theta CS}$  measured  $0.74^{\circ}\text{C}/\text{W}$ . The torque on the conventional mounting hardware had decreased to 3 in-lb from an initial 6 in-lb. With nonconformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing, ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will outperform the commonly used mica with grease. Cost may be a determining factor in making a selection.

**Table 3. Performance of Silicon Rubber Insulators Tested Per MIL-I-49456**

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data <sup>(1)</sup>	Bergquist Data <sup>(2)</sup>
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	–
CHO-THERM, 1617	0.233	–
Q Pad (non-insulated)	–	0.009
Sil-Pad, K-10	0.263	0.200
Thermasil III	0.267	–
Mica, greased	0.329	0.400
Sil-Pad 1000	0.400	0.300
CHO-THERM 1674	0.433	–
Thermasil II	0.500	–
Sil-Pad 400	0.533	0.440
Sil-Pad K-4	0.583	0.440

(1) From Thermalloy EIR 87-1030

(2) From Bergquist Data Sheet

### Insulation Resistance

When using insulators, care must be taken to keep the matting surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system, but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed.

### Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost-effective insulated packages since the 1950's. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late 80's, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The Energy Management Series (EMS) modules, shown in Figure 16, Case 806 (ICePAK™) and Case 388A (TO-258AA) (see Figure 16) are examples of parts in this category. The second category contains parts which have a plastic overmold covering the metal mounting base. The isolated, Case 221C, illustrated in 21, is an example of parts in the second category.

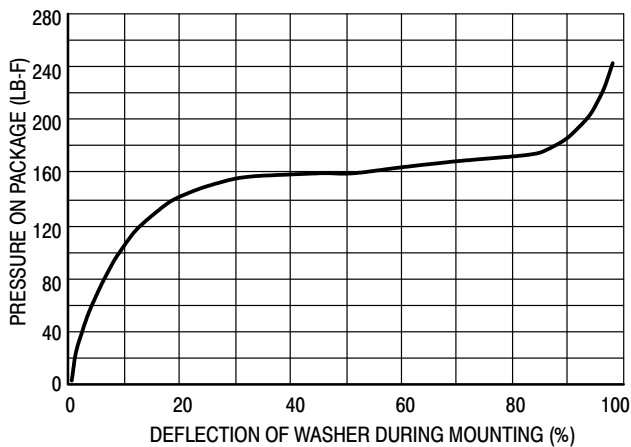
Parts in the first category (those with an exposed metal flange or tab) are mounted the same as their non-insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

## FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

### Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 8, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection – generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a “sync nut,” the patented device can be soldered to a PC board and the semiconductor mounted with a 6-32 machine screw.<sup>(4)</sup>



**Figure 8. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors**

### Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board-mounted or free-standing heat dissipaters with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO-220 and TO-126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO-220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

### Machine Screws

Machine screws, conical washers, and nuts (or sync nuts) can form a trouble-free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case could occur.

### Self-Tapping Screws

Under carefully controlled conditions, sheet-metal screws are acceptable. However, during the tapping process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; an unacceptable

surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speednut. If a self-tapping process is desired, the screw type must be used which roll-forms machine screw threads.

### Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange-mount package or EMS module is being mounted directly to a heatsink, rivets can be used provided press-riveting is used. Crimping force must be applied slowly and evenly. Pop-riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

### Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt-furnace, irons, vapor-phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

### Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.<sup>(5)</sup> Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non-field serviceable systems or low strength types for field serviceable systems. Adhesive bonding is attractive when case-mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

### Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.



**FASTENING TECHNIQUES**

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in the following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper-based part is rigidly mounted to an aluminum heatsink, a bi-metallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws, the semiconductor chip could be damaged.

Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some can slip between surfaces as the temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

**Stud Mount**

Parts which fall into the stud-mount classification are shown in Figure 8 through Figure 11. Mounting errors with non-insulated stud-mounted parts are generally confined to application of excessive torque or tapping the stud into a threaded heatsink hole. Both of these practices may cause a warpage of the hex base which may crack the semiconductor die. The only recommended fastening method is to use a nut and washer. The details are shown in Figure 12.

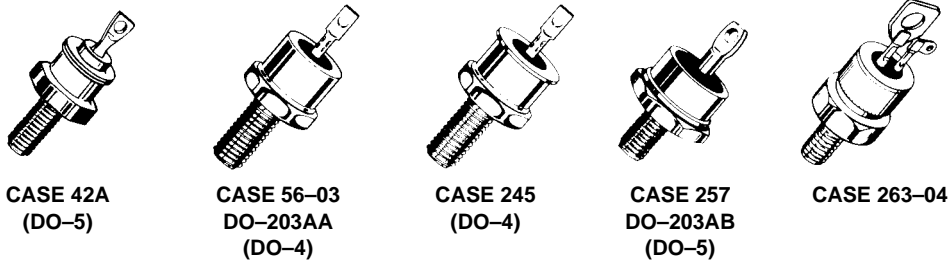


Figure 9. Standard Non-Isolated Types

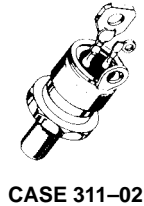


Figure 10. Isolated Type

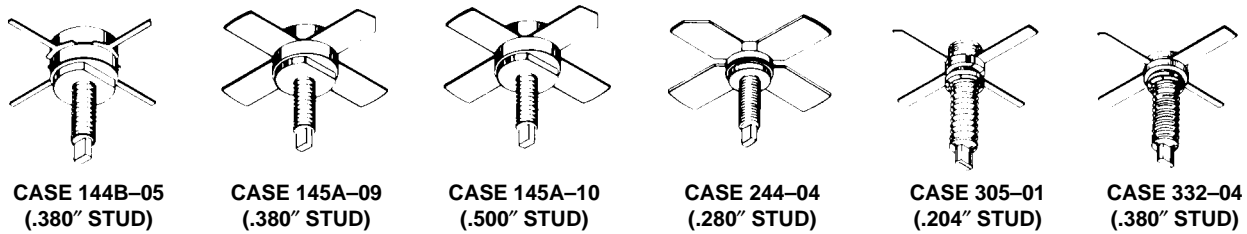
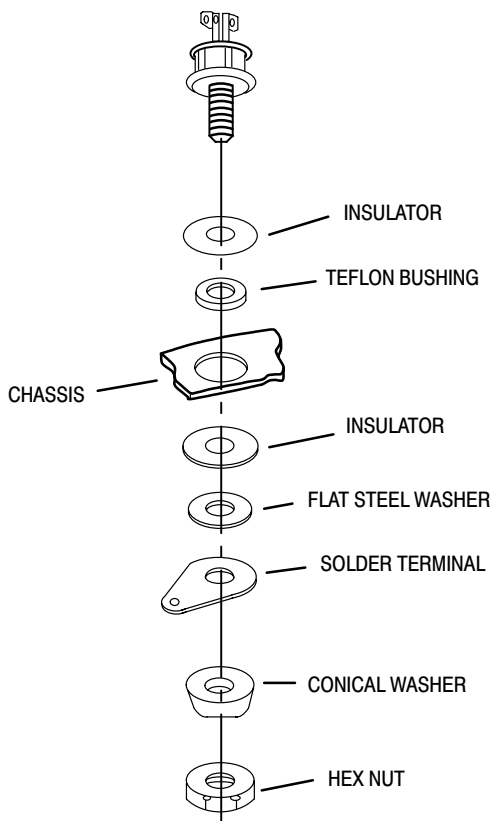


Figure 11. RF Stripline Opposed Emitter (SOE) Series

**A VARIETY OF STUD-MOUNT PARTS**



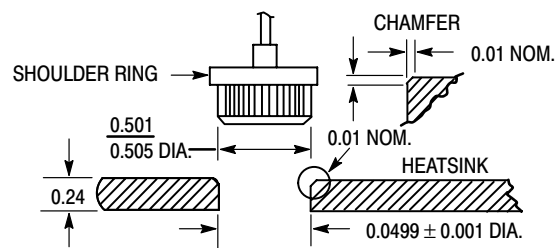
**Figure 12. Isolating Hardware Used for a Non-Isolated Stud-Mount Package**

Insulated electrode packages on a stud mount base require less hardware. They are mounted the same as their non-insulated counterparts, but care must be exercised to avoid applying a shear or tension stress to the insulation layer, usually a beryllium oxide (BeO) ceramic. This requirement dictates that the leads must be attached to the circuit with flexible wire. In addition, the stud hex should be used to hold the part while the nut is torqued.

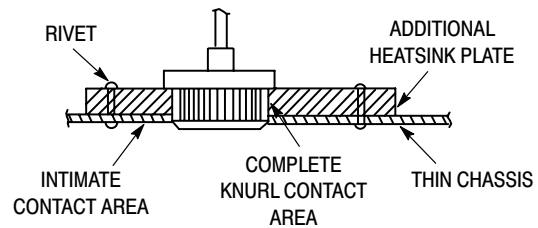
RF transistors in the stud-mount Stripline Opposed Emitter (SOE) package impose some additional constraints because of the unique construction of the package. Special techniques to make connections to the stripline leads and to mount the part so no tension or shear forces are applied to any ceramic – metal interface are discussed in the section entitled, “Connecting and Handling Terminals.”

#### Press Fit

For most applications, the press-fit case should be mounted according to the instructions shown in Figure 13. A special fixture, meeting the necessary requirements, must be used.



**HEATSINK MOUNTING**



**THIN-CHASSIS MOUNTING**

The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heatsink material. Recommended hardnesses are: copper—less than 50 on the Rockwell F scale; aluminum—less than 65 on the Brinell scale. A heatsink as thin as 1/8" may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

**Figure 13. Press-Fit Package**

#### Flange Mount

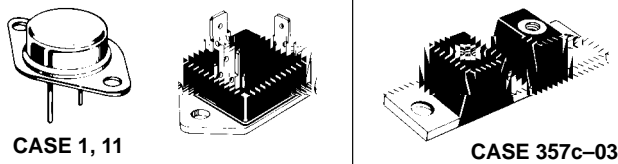
A large variety of parts fit into the flange mount category as shown in Figure 14 through Figure 17. Few known mounting difficulties exist with the smaller flange mount packages, such as the TO-204 (TO-3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is, therefore, good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger-tight, the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 18. Machine screws (preferred), self-tapping screws, eyelets, or rivets may be used to secure the package using guidelines in the previous section, “Fastener and Hardware Characteristics.”

The copper flange of the Energy Management Series (EMS) modules is very thick. Consequently, the parts are rugged and indestructible for all practical purposes. No special precautions are necessary when fastening these parts to a heatsink.

Some packages specify a tightening procedure. For example, with the Power Tap package, 15, final torque should be applied first to the center position.

The RF power modules (MHW series) are more sensitive to the flatness of the heatsink than other packages because

a ceramic (BeO) substrate is attached to a relatively thin, fairly long, flange. The maximum allowable flange bending to avoid mechanical damage has been determined and presented in detail in Engineering Bulletin EB107/D, "Mounting Considerations for ON Semiconductor RF Power Modules." Many of the parts can handle a combined heatsink and flange deviation from flat of 7 to 8 mils which is commonly available. Others must be held to 1.5 mils, which requires that the heatsink have nearly perfect flatness.



CASE 1, 11 TO-204AA (TO-3)  
CASE 383-01  
CASE 357c-03

Figure 14. TO-3 Variations

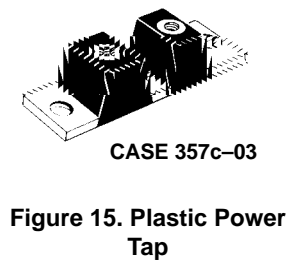


Figure 15. Plastic Power Tap



Figure 16. Energy Management Series (Isolated Base Plate)

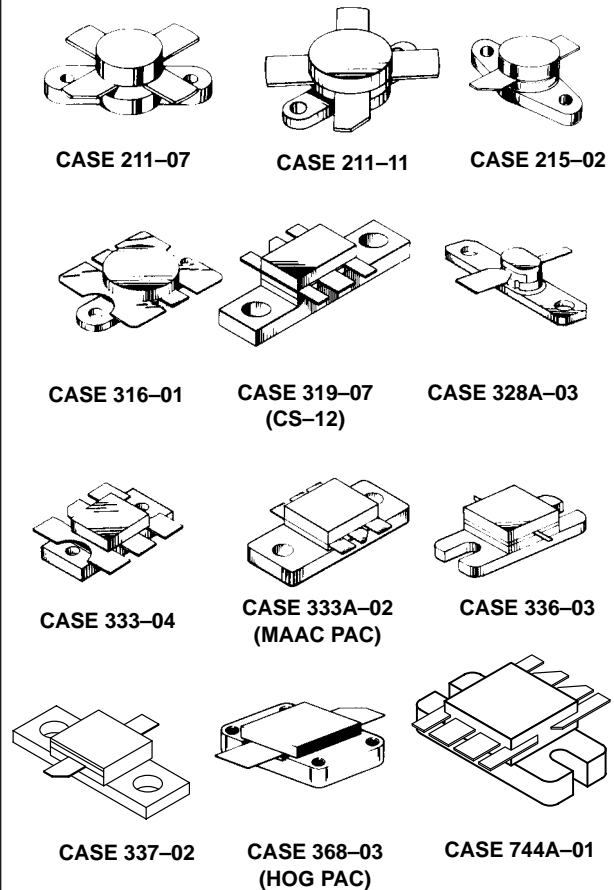


Figure 17. RF Stripline Isolated Output Opposed Emitter (SOE) Series

**A LARGE ARRAY OF PARTS FIT INTO THE FLANGE-MOUNT CLASSIFICATION**

Specific mounting recommendations are critical to RF devices in isolated packages because of the internal ceramic substrate. The large area, Case 368-03 (HOG PAC), will be used to illustrate problem areas. It is more sensitive to proper mounting techniques than most other RF power devices.

Although the data sheets contain information on recommended mounting procedures, experience indicates that they are often ignored. For example, the recommended maximum torque on the 4-40 mounting screws is 5 in./lbs. Spring and flat washers are recommended. Over-torquing

is a common problem. In some parts returned for failure analysis, indentions up to 10 mils deep in the mounting screw areas, have been observed.

Calculations indicate that the length of the flange increases in excess of two mils with a temperature change of 75°C. In such cases, if the mounting screw torque is excessive, the flange is prevented from expanding in length; instead, it bends upward in the mid-section, cracking the BeO and the die. A similar result can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied. With

sufficient torque, the thermal compound will squeeze out of the mounting hole areas, but will remain under the center of the flange, deforming it. Deformations of 2 – 3 mils have been measured between the center and the ends under such conditions (enough to crack internal ceramic).

Another problem arises because the thickness of the flange changes with temperature. For the 75°C temperature excursion mentioned, the increased amount is around 0.25 mils which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. With a decrease in temperature, the opposite effect occurs. Therefore, thermal cycling not only causes risk of structural damage but often causes the assembly to loosen which raises the interface resistance. Use of compression hardware can eliminate this problem.

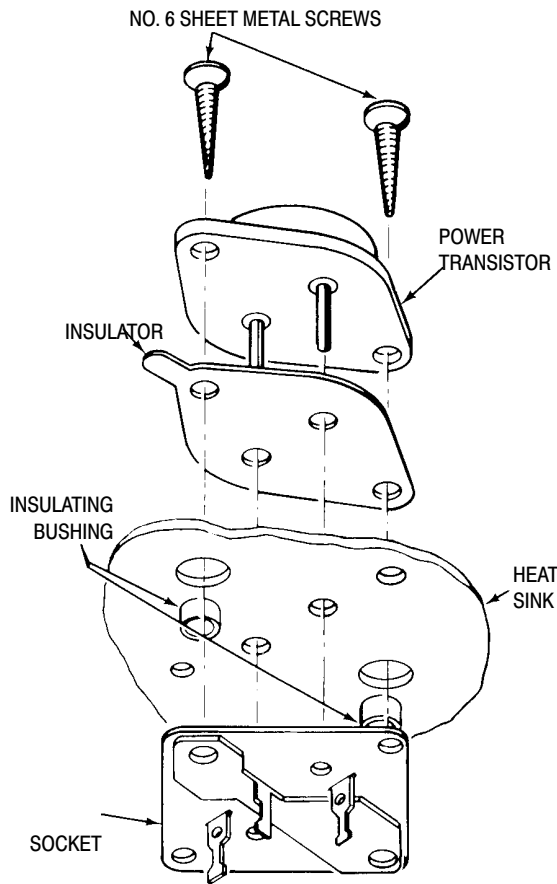


Figure 18. Hardware Used for a TO-204AA (TO-3) Flange Mount Part

**Tab Mount**

The tab mount class is composed of a wide array of packages as illustrated in Figure 19. Mounting considerations for all varieties are similar to that for the popular TO-220 package, whose suggested mounting arrangements and hardware are shown in Figure 20. The rectangular washer shown in Figure 20a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip.

Use of the washer is only important when the size of the mounting hole exceeds 0.140 in. (6-32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 in./lbs is suggested when using a 6-32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, ON Semiconductor TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

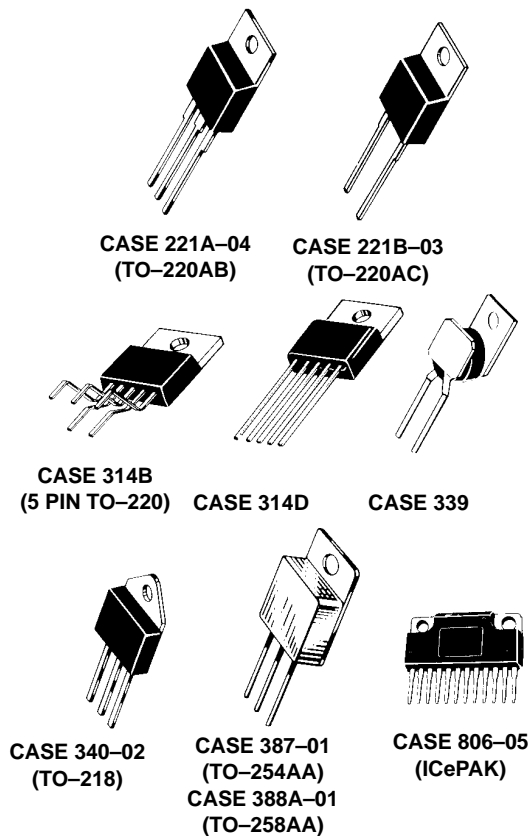


Figure 19. Several Types of Tab-Mount Parts

The popular TO-220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure 36.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.<sup>(6)</sup> In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 27.

To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

The ICePAK (Case 806-05) is basically an elongated TO-220 package with isolated chips. The mounting precautions for the TO-220 consequently apply. In addition, since two mounting screws are required, the alternate tightening procedure described for the flange mount package should be used.

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.

- a) Preferred Arrangement for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.
- b) Alternate Arrangement for Isolated Mounting when Screw must be at Heatsink Potential. 4-40 Hardware is Used.

Choose from Parts Listed Below

Use Parts Listed Below

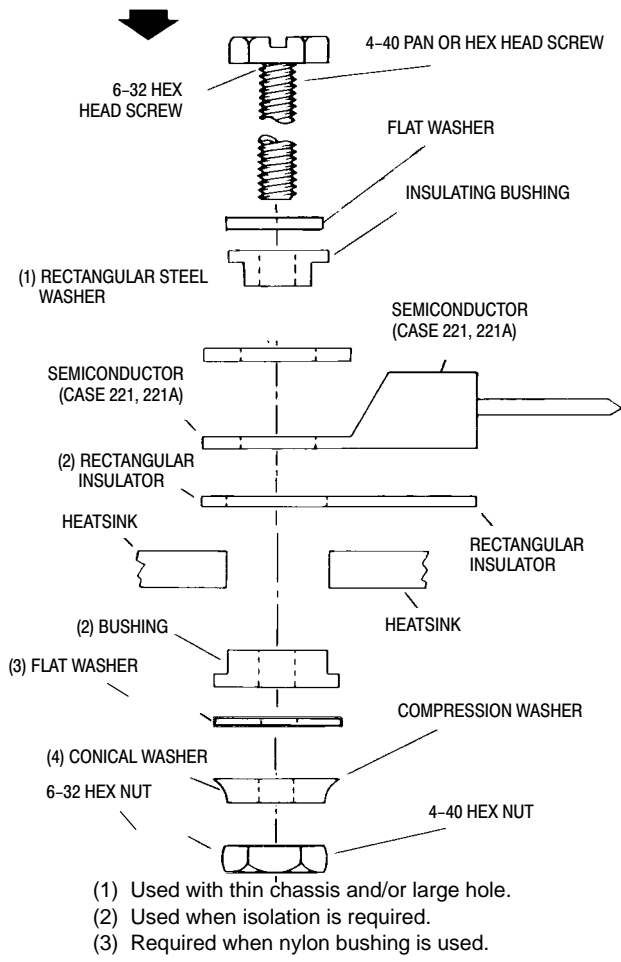


Figure 20. Mounting Arrangements for Tab Mount TO-220

**Plastic Body Mount**

The Thermopad™ and isolated plastic power packages shown in Figure 21 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad (Case 77) parts, this is accomplished by die-bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The isolated (Case 221C-02) is similar to a TO-220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO-220 and is similar to that of the Thermopad.

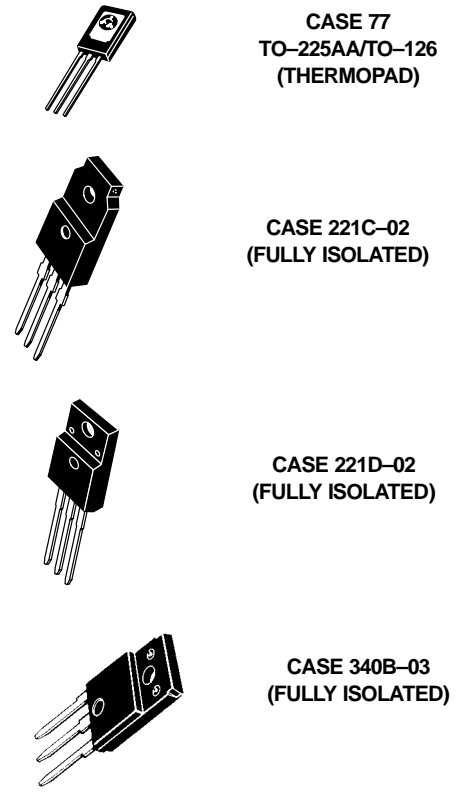


Figure 21. Plastic Body-Mount Packages

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 8.

Figure 22 through Figure 24 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

The isolated, (Case 221C, 221D, and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO-220. As shown in Figure 27, one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure 36 of Appendix B.) The interface should consist of a layer of thermal grease or

a highly conductive thermal pad. Of course, screw mounting shown in Figure 26 may also be used, but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO-220 package which is shown in Figure 25.

### **Surface Mount**

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 28, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

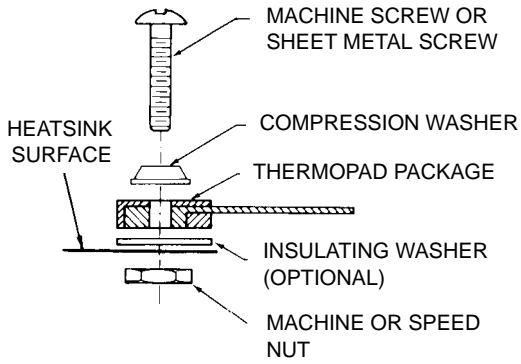


Figure 22. Machine Screw Mounting

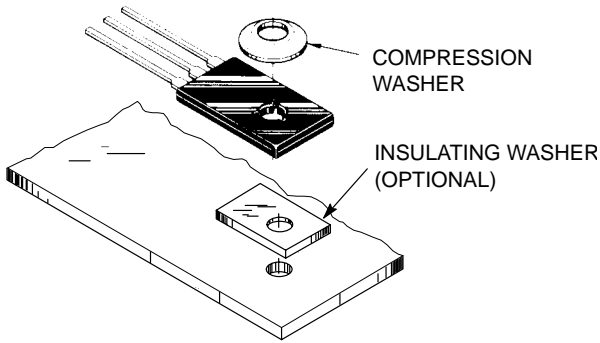
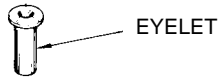


Figure 23. Eyelet Mounting

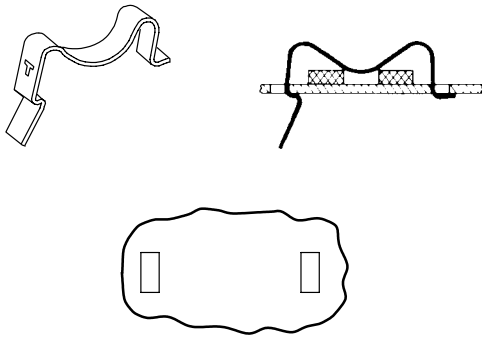


Figure 24. Clips

RECOMMENDED MOUNTING ARRANGEMENTS FOR TO-225AA (TO-126) THERMOPAD PACKAGES

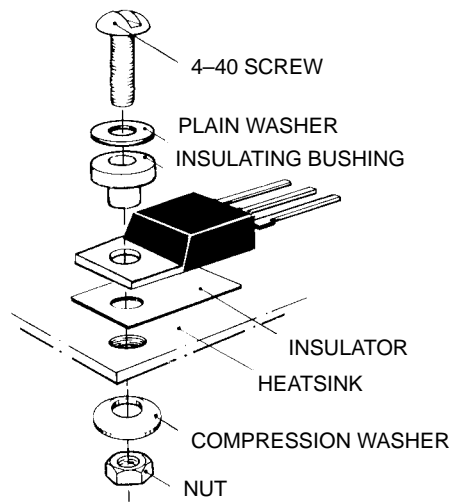


Figure 25. Screw-Mounted TO-220

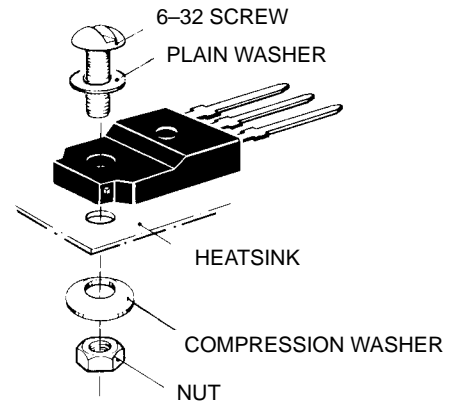


Figure 26. Screw-Mounted Isolated Package

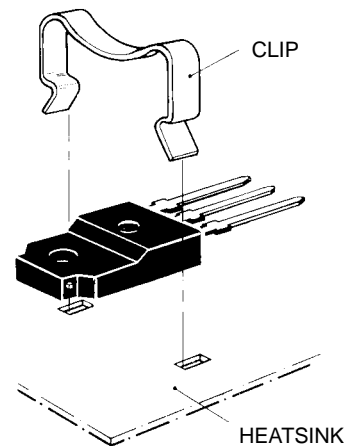


Figure 27. Clip-Mounted Isolated Package

MOUNTING ARRANGEMENTS FOR THE ISOLATED PACKAGE AS COMPARED TO A CONVENTIONAL

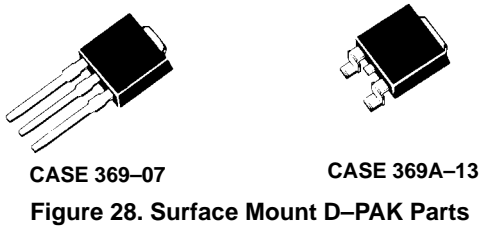


Figure 28. Surface Mount D-PAK Parts

Standard Glass-Epoxy 2-ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 29 shows, thermal resistance asymptotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlaid with one- or two-ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.<sup>(7)</sup> The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

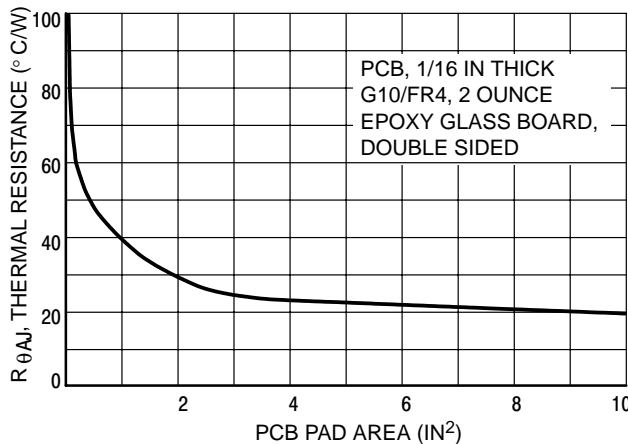


Figure 29. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass-Epoxy Board

**FREE AIR AND SOCKET MOUNTING**

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are

not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice, however, it is better to support the package. A plastic support for the TO-220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the Case 77 (TO-225AA) (TO-127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 30 and Figure 31. The arrangement of Figure 30 could be used with any plastic package, but the scheme of Figure 31 is more practical with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.

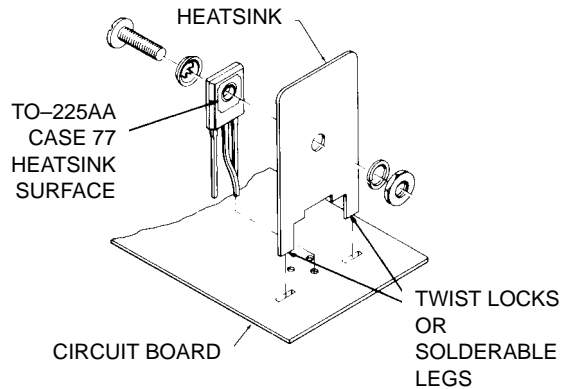


Figure 30. Simple Plate, Vertically Mounted

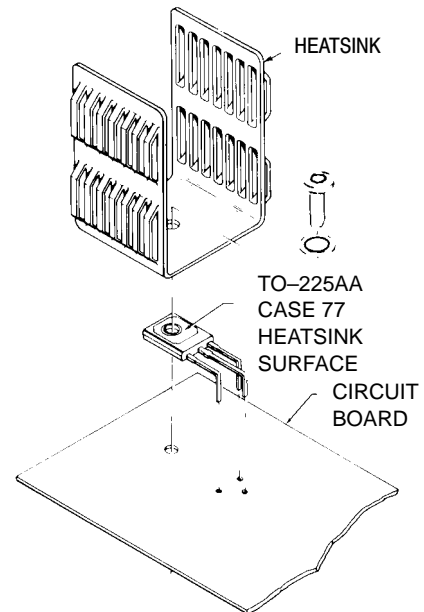


Figure 31. Commercial Sink, Horizontally Mounted

**METHODS OF USING SMALL HEATSINKS WITH PLASTIC SEMICONDUCTOR PACKAGES**



In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from ON Semiconductor. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

### CONNECTING AND HANDLING TERMINALS

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions, as a result of thermal cycling over operating temperature extremes, must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

#### Metal Packages

The pins and lugs of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

#### EMS Modules

The screw terminals of the EMS modules look deceptively rugged. Since the flange base is mounted to a rigid heatsink, the connection to the terminals must allow some flexibility. A rigid buss bar should not be bolted to terminals. Lugs with braid are preferred.

#### Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped, although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead-bending unnecessary. Numerous lead and tab-forming options are available from ON Semiconductor on large quantity orders. Preformed leads remove the users' risk of device damage caused by bending.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/16 inch is advisable for TO-225AA (CASE 77) and 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.

3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire-wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

#### Stripline Packages

The leads of stripline packages normally are soldered into a board while the case is recessed to contact a heatsink as shown in Figure 32 through Figure 34. The following rules should be observed:

1. The device should never be mounted in such a manner as to place ceramic-to-metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud and BeO portion of the header passing through a hole in the circuit boards, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.
4. Some clearance must be allowed between the leads and the circuit board when the device is secured to the heatsink.
5. The device should be properly secured into the heatsinks before its leads are attached into the circuit.
6. The leads on stud type devices must not be used to prevent device rotation during stud torque application. A wrench flat is provided for this purpose.

Figure 33 shows a cross-section of a printed circuit board and heatsink assembly for mounting a stud-type stripline device. H is the distance from the top surface of the printed circuit board to the D-flat heatsink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud - BeO ceramic joint. If, however, H is greater than the package

dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurrences are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead-soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heatsink surface will occur as the differences between H and the package dimension become larger; this may result in device failure as power is applied.

Figure 34 shows a typical mounting technique for flange-type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heatsink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur.

**CLEANING CIRCUIT BOARDS**

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free-standing without support.

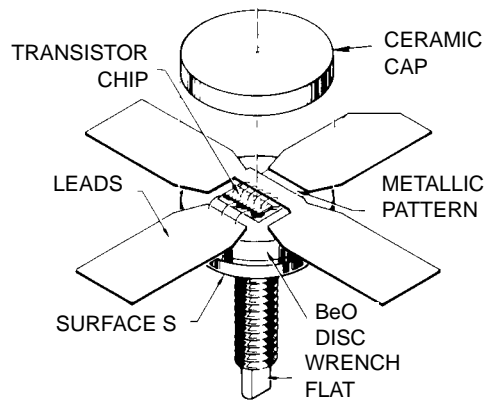
**THERMAL SYSTEM EVALUATION**

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

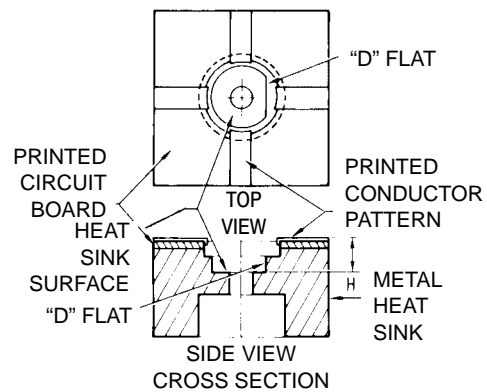
In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see ON Semiconductor Application Note, AN569/D.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating

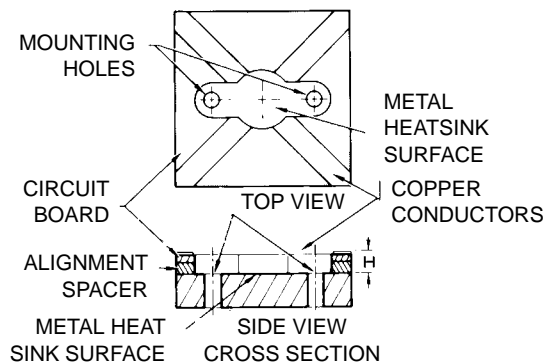
area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.



**Figure 32. Component Parts of a Stud Mount Stripline Package. Flange Mounted Packages are Similarly Constructed**



**Figure 33. Typical Stud Type SOE Transistor Mounting Method**



**Figure 34. Flange Type SOE Transistor Mounting Method**  
**MOUNTING DETAILS FOR SOE TRANSISTORS**

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where  $T_J$  = junction temperature ( $^{\circ}\text{C}$ )  
 $T_C$  = case temperature ( $^{\circ}\text{C}$ )  
 $R_{\theta JC}$  = thermal resistance junction-to case as specified on the data sheet ( $^{\circ}\text{C}/\text{W}$ )  
 $P_D$  = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

#### **Graphical Integration**

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a

suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

#### **Substitution**

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

## APPENDIX A THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where  $q$  = rate of heat transfer or power dissipation ( $P_D$ )  
 $h$  = heat transfer coefficient,  
 $A$  = area involved in heat transfer,  
 $\Delta T$  = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance,  $R_{\theta}$ , is

$$R_{\theta} = \Delta T/q = 1/hA \quad (2)$$

The coefficient ( $h$ ) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that  $T$  could be thought of as a voltage thermal resistance corresponds to electrical resistance ( $R$ ); and, power ( $q$ ) is analogous to current ( $I$ ). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure 35.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where  $T_J$  = junction temperature,

$P_D$  = power dissipation

$R_{\theta JC}$  = semiconductor thermal resistance (junction to case),

$R_{\theta CS}$  = interface thermal resistance (case to heat-sink),

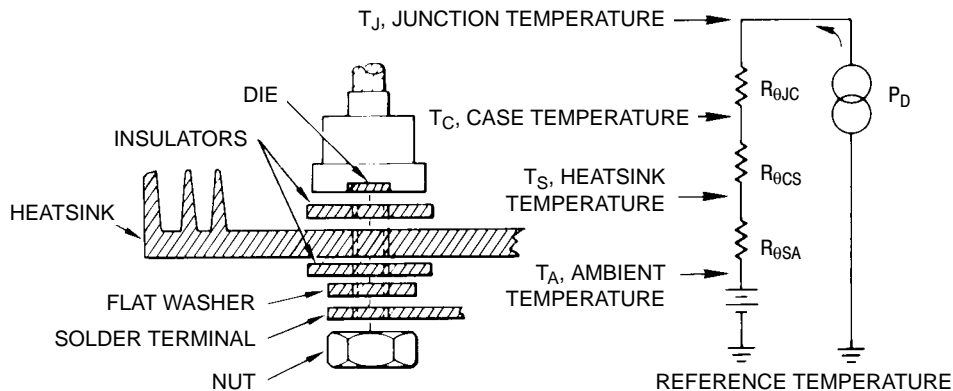
$R_{\theta SA}$  = heat sink thermal resistance (heatsink to ambient),

$T_A$  = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance,  $R_{\theta CS}$ , may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize  $R_{\theta CS}$ .

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications, such as in RF power amplifiers and short-pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.



**Figure 35. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor**

## APPENDIX B MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance  $R_{\theta CS}$  appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However,  $R_{\theta CS}$  is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO-3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL-I-49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

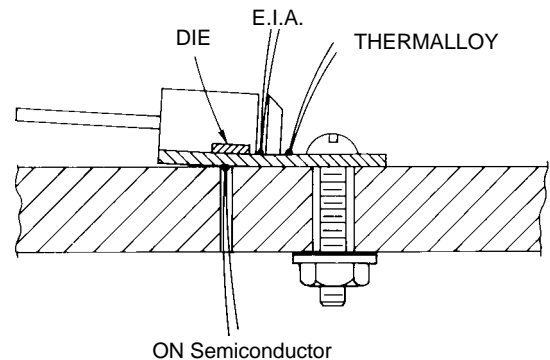
Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The ON Semiconductor fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO-220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in  $R_{\theta CS}$  can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO-220 package shown in 36. The mounting pressure at one end causes the other end – where the die is located – to lift off the mounting surface slightly. To improve contact, ON Semiconductor TO-220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

1. The ON Semiconductor location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

2. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.
3. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.



**Figure 36. JEDEC TO-220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End**

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the ON Semiconductor location is even hotter. Since junction-to-sink thermal resistance must be constant for a given test setup, the calculated junction-to-case thermal resistance values decrease and case-to-sink values increase as the "case" temperature thermocouple readings become warmer. Thus, the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower, but close to the temperature at the EIA location as the lateral heat flow is generally small. The ON Semiconductor location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The ON Semiconductor location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink, to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO-220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified

junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ-inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is, therefore, application-oriented. It is also easy to use, but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction-to-case thermal resistance while testing for interface thermal resistance. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

### APPENDIX C Sources of Accessories

Manufacturer	Joint Compound	Adhesives	Insulators						Heatsinks	Clips	
			BeO	AlO <sub>2</sub>	Anodize	Mica	Plastic Film	Silicone Rubber			
Aavid	–	–	–	–	–	–	–	X	X	X	X
AHAM-TOR	–	–	–	–	–	–	–	–	–	X	–
Asheville-Schoonmaker	–	–	–	–	–	–	X	–	–	–	–
Astrodynamicis	X	–	–	–	–	–	–	–	–	X	–
Delbert Blinn	–	–	X	–	X	X	X	X	X	X	–
IERC	X	–	–	–	–	–	–	–	–	X	–
Staver	–	–	–	–	–	–	–	–	–	X	–
Thermalloy	X	X	X	X	X	X	X	X	X	X	X
Tran-tec	X	–	X	X	X	X	X	–	X	X	–
Wakefield	X	X	X	–	X	–	–	–	X	X	X

Other Sources for silicone rubber pads: Chomerics, Bergquist

#### Suppliers Addresses

Aavid Engineering, Inc., P.O. Box 400, Laconia, New Hampshire 03247	(603) 524-1478
AHAM-TOR Heatsinks, 27901 Front Street, Rancho, California 92390	(714) 676-4151
Asheville-Schoonmaker, 900 Jefferson Ave., Newport News, VA 23607	(804) 244-7311
Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801	(617) 935-4944
Bergquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435	(612) 835-2322
Chomerics, Inc., 16 Flagstone Drive, Hudson, New Hampshire 03051	1-800-633-8800
Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769	(714) 623-1257
International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502	(213) 849-2481
The Staver Company, Inc., 41-51 Saxon Avenue, Bay Shore, Long Island, New York 11706	(516) 666-8000
Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234	(214) 243-4321
Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601	(402) 564-2748
Wakefield Engineering, Inc., Wakefield, Massachusetts 01880	(617) 245-5900

## PACKAGE INDEX

## PREFACE

When the JEDEC registration system for package outlines started in 1957, numbers were assigned sequentially whenever manufacturers wished to establish a package as an industry standard. As minor variations developed from these industry standards, either a new, non-related number was issued by JEDEC or manufacturers would attempt to relate the part to an industry standard via some appended description.

In an attempt to ease confusion, JEDEC established the present system in late 1968 in which new packages are assigned into a category, based on their general physical appearance. Differences between specific packages in a

category are denoted by suffix letters. The older package designations were re-registered to the new system as time permitted.

For example the venerable TO-3 has many variations. Can heights differ and it is available with 30, 40, 50, and 60 mil pins, with and without lugs. It is now classified in the TO-204 family. The TO-204AA conforms to the original outline for the TO-3 having 40 mil pins while the TO-204AE has 60 mil pins, for example.

The new numbers for the old parts really haven't caught on very well. It seems that the DO-4, DO-5 and TO-3 still convey sufficient meaning for general verbal communication.

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
001	TO-3	TO-204AA		Flange
003	TO-3		2	Flange
009	TO-61	TO-210AC		Stud
011	TO-3	TO-204AA	–	Flange
011A	TO-3	–	2	Flange
012	TO-3	–	2	Flange
036	TO-60	TO-210AB	–	Stud
042A	DO-5	DO-203AB	–	Stud
044	DO-4	DO-203AA	–	Stud
054	TO-3	–	2	Flange
056	DO-4	–	–	Stud
058	DO-5	–	2	Stud
61-04				Flange
63-02	TO-64	TO-208AB		Stud
63-03	TO-64	TO-2088AB		Stud
077	TO-126	TO-225AA	–	Plastic
080	TO-66	TO-213AA	–	Flange
086	–	TO-208	1	Stud
086L	–	TO-298	1	Stud
144B-05				Stud
145A-09				Stud
145A-10				Stud
145C	TO-232		1	Stud
157	–	DO-203	1	Stud
160-03	TO-59	TO-210AA	–	Stud
167	–	DO-203	1	Stud
174-04				Pressfit

Notes: 1. Would fit within this family outline if registered with JEDEC.  
2. Not within all JEDEC dimensions.

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
175-03				Stud
197	–	TO-204AE	–	Flange
211-07				Flange
211-11				Flange
215-02				Flange
221	–	TO-220AB	–	Tab
221C-02				Plastic
221D-02	–	–	Isolated TO-220	Plastic
235	–	TO-208	1	Stud
235-03				Stud
238	–	TO-208	1	Stud
239	–	TO-208	–	Stud
244-04				Stud
245	DO-4	–	–	Stud
257-01	DO-5	–	–	Stud
263	–	TO-208	–	Stud
263-04				Stud
283	DO-4	–	–	Stud
289	–	TO-209	1	Stud
305-01				Stud
310-02				Pressfit
311-02			Isolated	Stud
311-02				Pressfit
311-02				Stud
314B-03				Tab

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
314D-03				Tab
316-01				Flange
319-06				Flange
328A-03				Flange
332-04				Stud
333-04				Flange
333A-02				Flange
336-03				Flange
337-02				Flange
340		TO-218AC		Tab
340A-02				Plastic
340B-03			Isolated TO-218	Plastic
342-01				Flange
357B-01				Flange
361-01				Flange
368-02				Flange
369-06		TO-251		Insertion
369A-12		TO-252		Surface
373-01			Isolated	Flange
383-01			Isolated	Flange
387-01		TO-254AA	Isolated 2	Tab
388A-01		TO-258AA	Isolated 2	Tab
744-02				Flange
744A-01				Flange
043-07	DO-21	DO-208AA		Pressfit

- (1) MIL-HANDBOOK – 2178, SECTION 2.2.
- (2) "Navy Power Supply Reliability – Design and Manufacturing Guidelines" NAVMAT P4855-1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.
- (3) Catalog #87-HS-9, (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381-0839.
- (4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.
- (5) Robert Batson, Elliot Fraunglass and James P Moran, "Heat Dissipation Through Thermalloy Conductive Adhesives," EMTAS '83. Conference, February 1 – 3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

- (6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.
- (7) Herb Fick, "Thermal Management of Surface Mount Power Devices," Powerconversion and Intelligent Motion, August 1987.

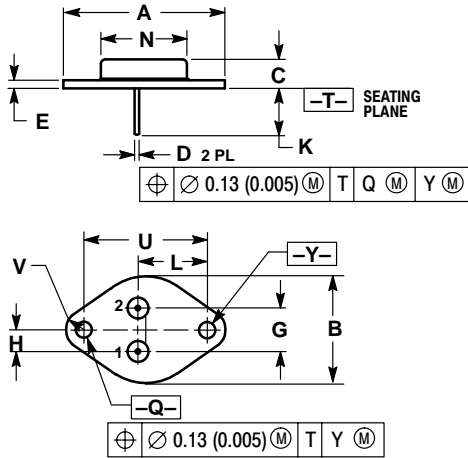
# Case Outlines

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# Case Outlines

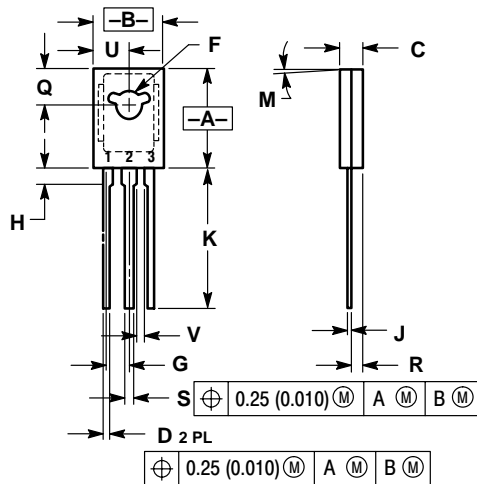
## TO-204 CASE 1-07 ISSUE Z



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

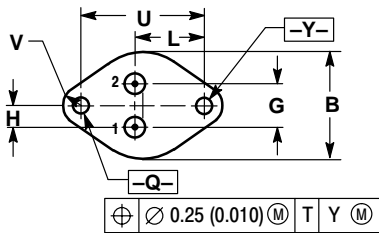
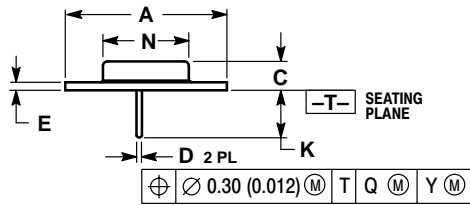
## TO-225 CASE 77-09 ISSUE W



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

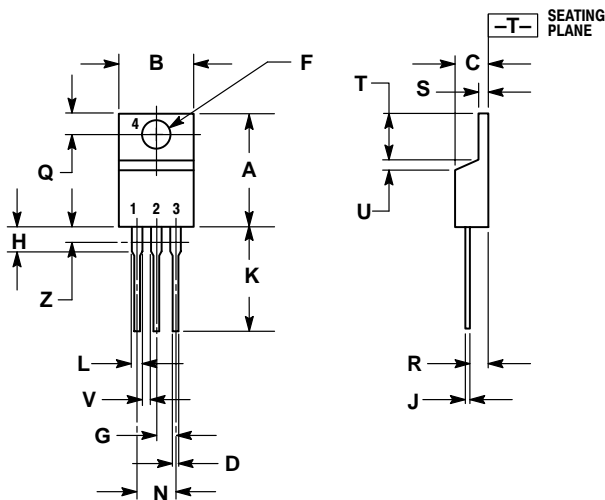
**TO-204**  
CASE 197A-05  
ISSUE J



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

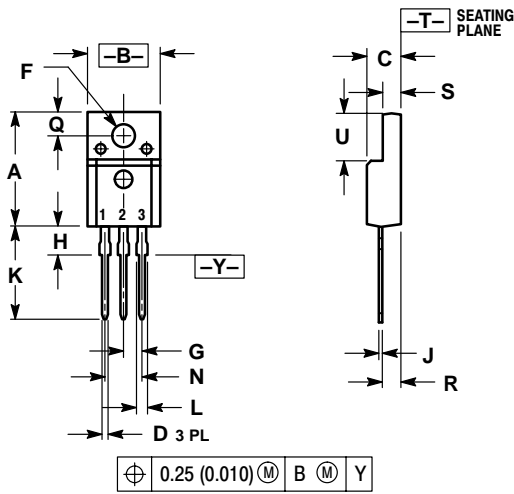
**TO-220**  
CASE 221A-09  
ISSUE AA



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.  
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

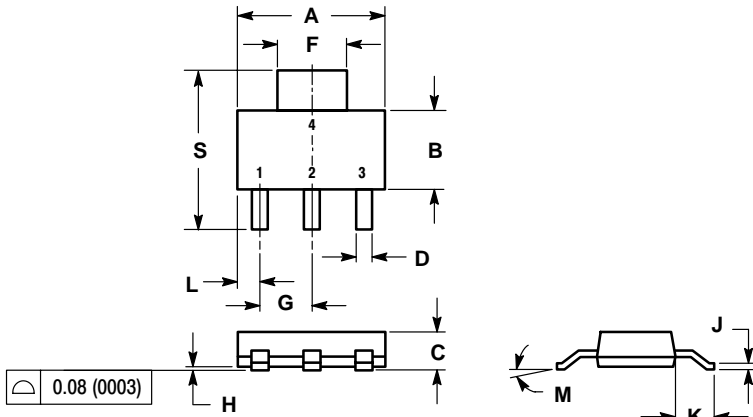
TO-220  
CASE 221D-02  
ISSUE D



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

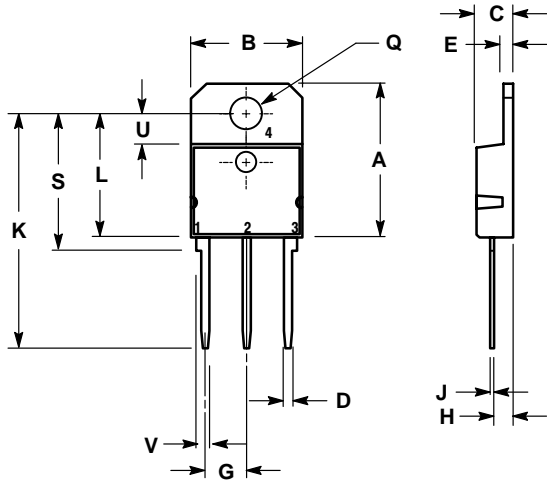
TO-261  
CASE 318E-04  
ISSUE K



- NOTES:  
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
5. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0°	10°	0°	10°
S	0.264	0.287	6.70	7.30

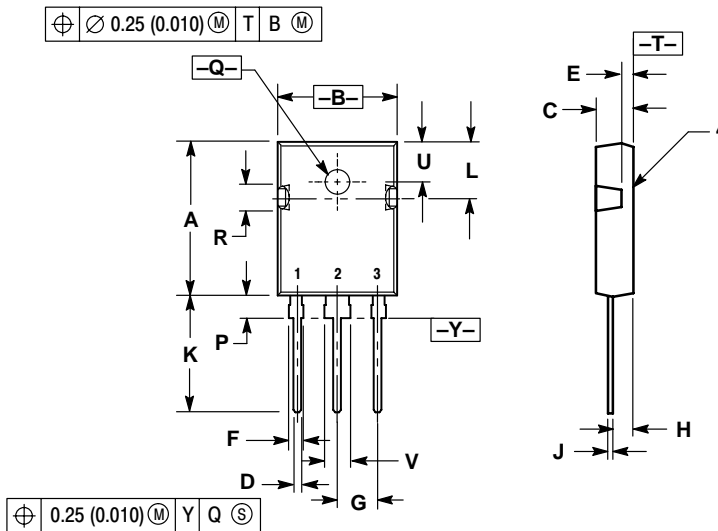
TO-218  
CASE 340D-02  
ISSUE B



NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

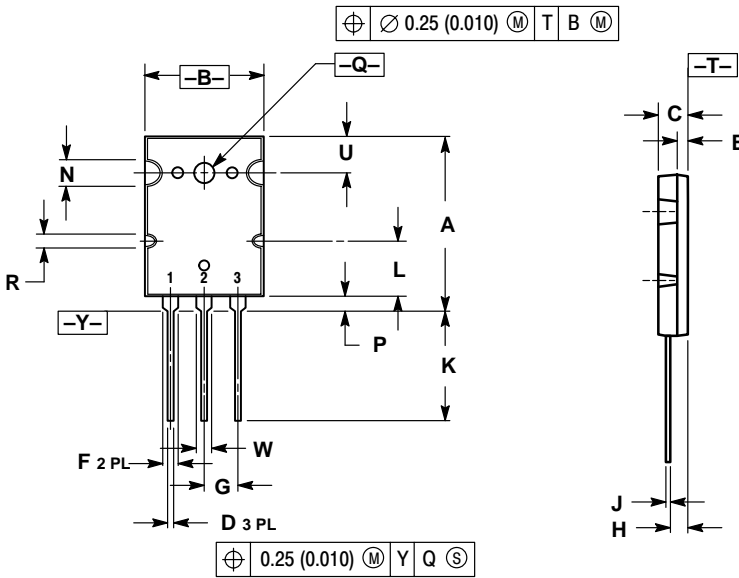
TO-207  
CASE 340F-03  
ISSUE G



NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.40	20.90	0.803	0.823
B	15.44	15.95	0.608	0.628
C	4.70	5.21	0.185	0.205
D	1.09	1.30	0.043	0.051
E	1.50	1.63	0.059	0.064
F	1.80	2.18	0.071	0.086
G	5.45 BSC		0.215 BSC	
H	2.56	2.87	0.101	0.113
J	0.48	0.68	0.019	0.027
K	15.57	16.08	0.613	0.633
L	7.26	7.50	0.286	0.295
P	3.10	3.38	0.122	0.133
Q	3.50	3.70	0.138	0.145
R	3.30	3.80	0.130	0.150
U	5.30 BSC		0.209 BSC	
V	3.05	3.40	0.120	0.134

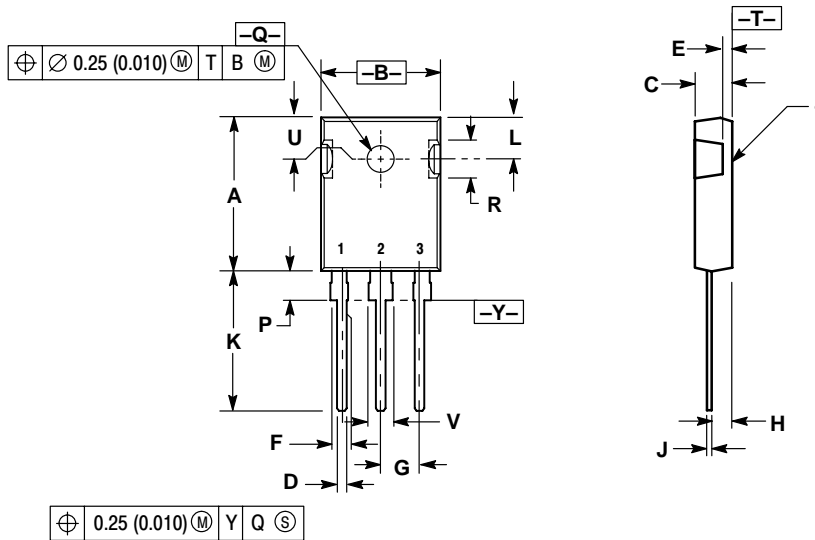
TO-264  
CASE 340G-02  
ISSUE H



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	28.0	29.0	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

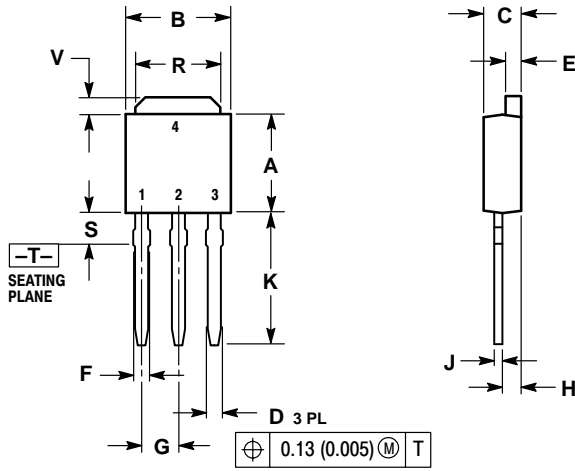
TO-247  
CASE 340K-01  
ISSUE C



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.7	20.3	0.776	0.799
B	15.3	15.9	0.602	0.626
C	4.7	5.3	0.185	0.209
D	1.0	1.4	0.039	0.055
E	1.27 REF		0.050 REF	
F	2.0	2.4	0.079	0.094
G	5.5 BSC		0.216 BSC	
H	2.2	2.6	0.087	0.102
J	0.4	0.8	0.016	0.031
K	14.2	14.8	0.559	0.583
L	5.5 NOM		0.217 NOM	
P	3.7	4.3	0.146	0.169
Q	3.55	3.65	0.140	0.144
R	5.0 NOM		0.197 NOM	
U	5.5 BSC		0.217 BSC	
V	3.0	3.4	0.118	0.134

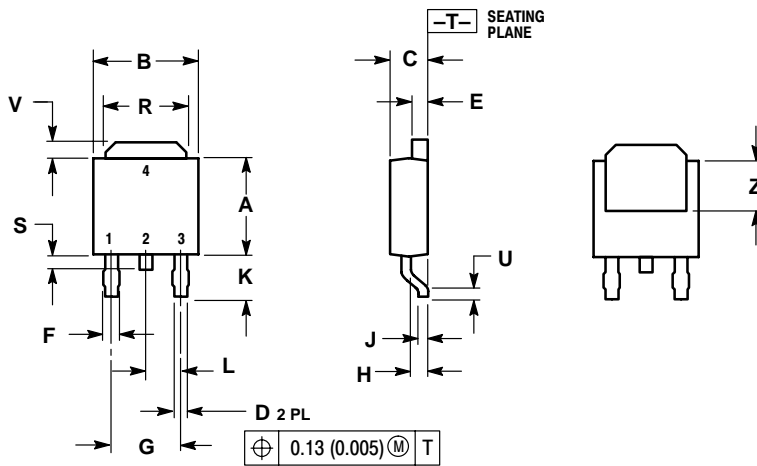
**DPAK**  
CASE 369-07  
ISSUE M



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

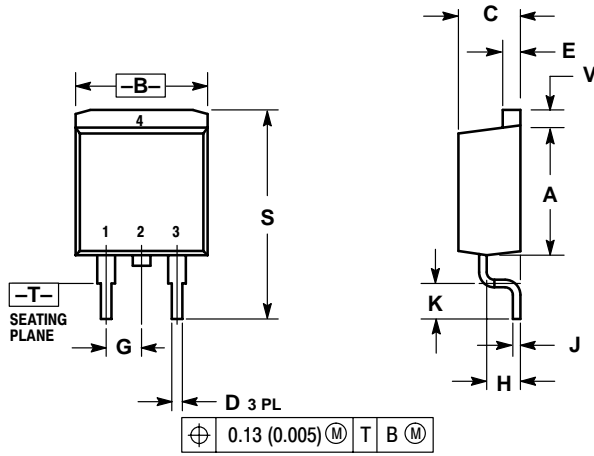
**DPAK**  
CASE 369A-13  
ISSUE AA



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

**D<sup>2</sup>PAK**  
CASE 418B-03  
ISSUE D

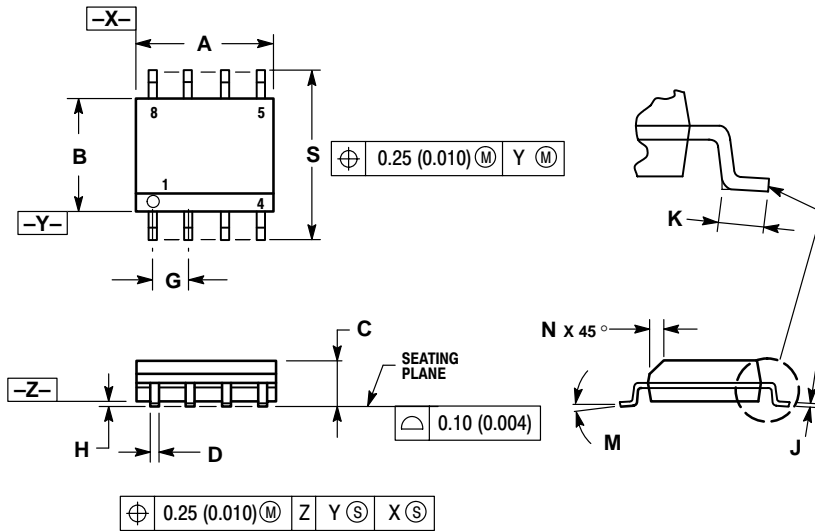


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

**SOIC-8 NB**  
CASE 751-07  
ISSUE W



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: MILLIMETER.  
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.  
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.  
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## **CHAPTER 4**

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