Compal confidential

Schematics Document
Intel portability uFCBGA/uFCPGA
with ATI-RC300M+SB200 core logic

2003-07-10

REV:0.4

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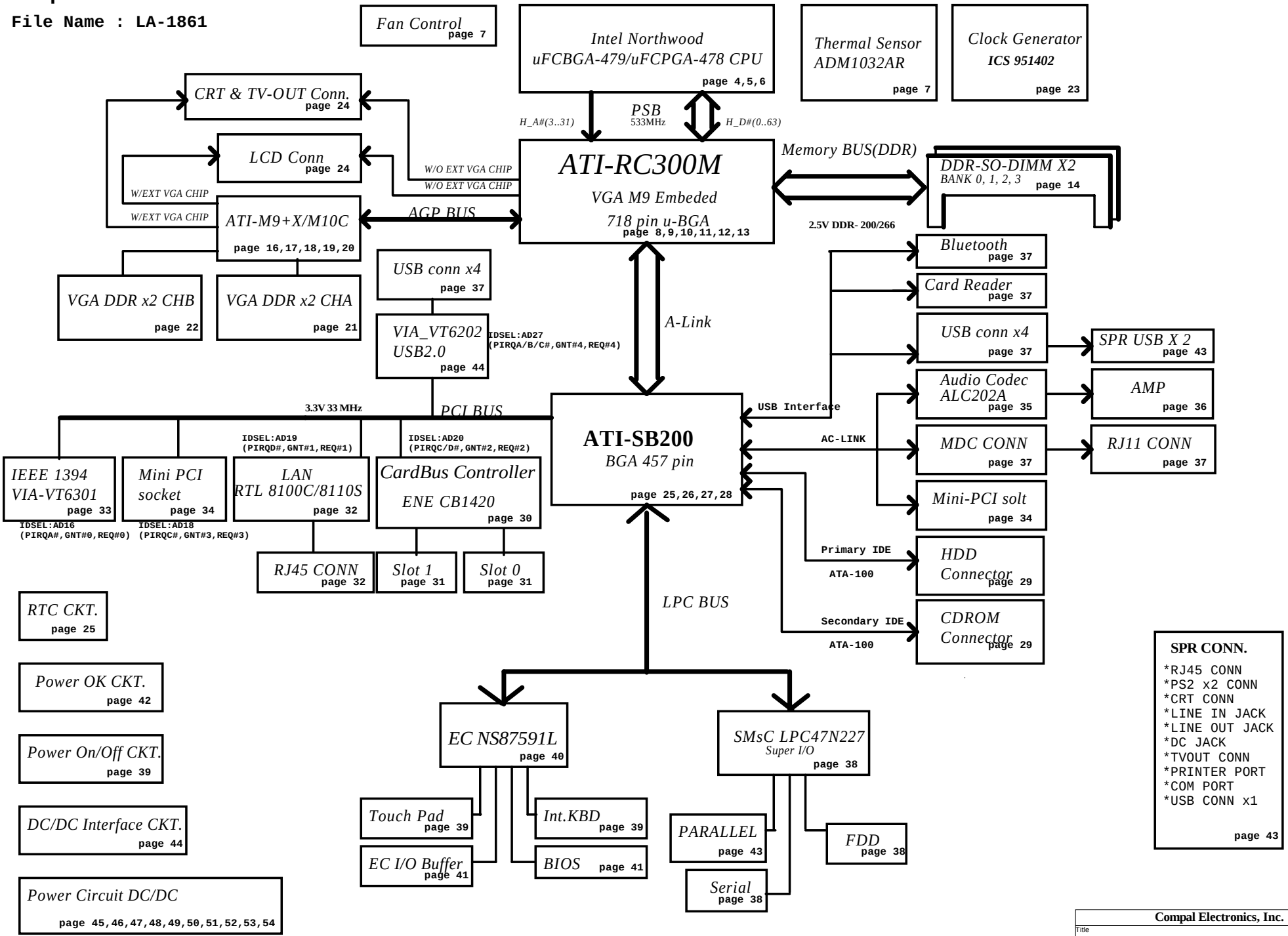
File Name : LA-1861



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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCVID	The voltage for Processor VID select	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+1.2VS_VGA	1.2V I/O power rail for ATI-VGA M9+X/M10P.	ON	OFF	OFF
+1.5VS	1.5V I/O power rail for ATI-RS300M/RC300M NB AGP.	ON	OFF	OFF
+1.8VS	1.8V switched power rail for ATI-RS300M/RC300M NB.	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V system power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+3V	3.3V system power rail for SB,LAN,CardReader and HUB.	ON	ON	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12Vswitched power rail on power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
AGP BUS	AGP_DEVSEL	N/A	A
SOUTHBRIDGE	AD31 (INT.)	N/A	N/A
USB	AD30 (INT.)	N/A	D
AC97	AD31 (INT.)	N/A	B
ATA 100	AD31 (INT.)	N/A	A
ETHERNET	AD24 (INT.)	N/A	C
1394	AD16	0	A
LAN	AD19	1	D
CARD BUS	AD20	2	A/B
Wireless LAN	AD18	3	C
VIA6202 USB20	AD27	4	A/B/C

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1010000X
DDR SO-DIMM 1	A2	1010001X
CLOCK GENERATOR (EXT.)	D2	1101001X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build

M9@ : means just build when no external AGP VGA chip build in .

M9+/M10@ : means just build when M9+XC or M10 build in

M9+@ : means just build when M9+XC chip build in .

M10@ : means just build when M10 chip build in .

NSPR@ : means just build when no SPR build in .

SPR@ : means just build when SPR build in .

8100S@ : means just build when 8100S build in .

1394@ : means just build when 1394 build in .

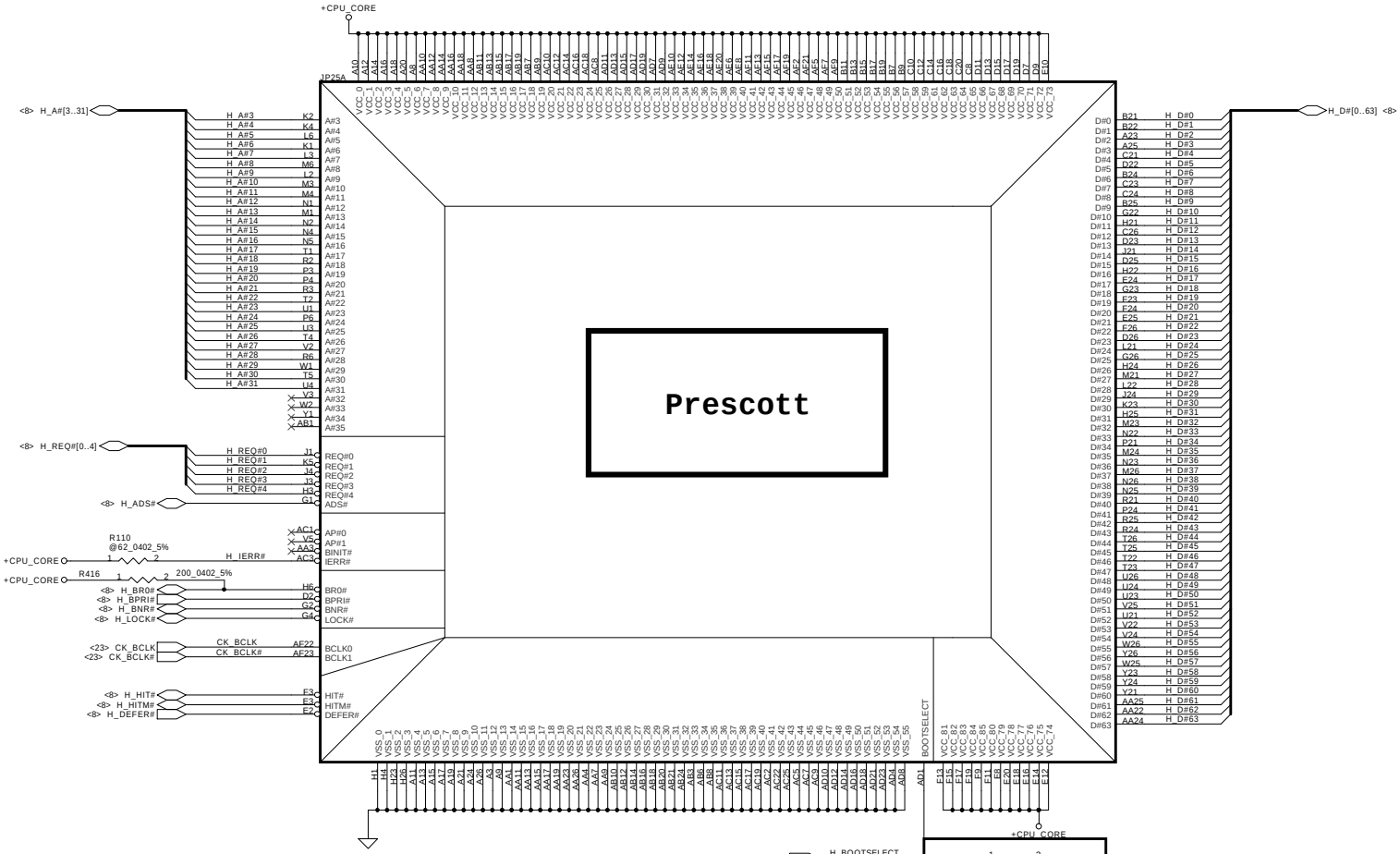
MDC@ : means just build when MDC build in .

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	



Reference Intel document
Desktop P4 Spec.: 10988 P4 0.13u 512KB L2 EMTS Rev.2.0
Desktop Prescott Spec.: 11910 Prescott EMTS Rev.0.5

Pin number	Northwood Pin name	Commend	Prescott Pin name	Commend	Northwood MT Pin name	Commend	Northwood	Prescott	Northwood MT
A6	TESTHI11	Pull-up 200ohm to +VCC_CORE	TESTHI11	Pull-up 62ohm to +VCC_CORE	GHI	Connect to PLD CPUPREF through 0ohm	Pop	Pop	Pop
B6	FERR#	Pull-up 62ohm to +VCC_CORE	FERR#/PBE#	Pull-up 62ohm to +VCC_CORE	FERR#	Pull-up 62ohm to +VCC_CORE	Pop	Pop	Pop
AA20	ITPCLKOUT0	Pull-up56ohm to +VCC_CORE	TESTHI6	Pull-up 62ohm to +VCC_CORE	ITPCLKOUT0	Pull-up56ohm to +VCC_CORE	Pop	Pop	Pop
AB22	ITPCLKOUT1	Pull-up 56ohm to +VCC_CORE	TESTHI7	Pull-up 62ohm to +VCC_CORE	ITPCLKOUT1	Pull-up 56ohm to +VCC_CORE	Pop	Pop	Pop
AD2	NC	float	VIDPWRGD	Pull-up 2.43K ohm to +VCCVID	NC	float	Depop	Pop	Depop
AD3	NC	float	VID5	Pull-up1Kohm to +3VRUN & connect to PWRIC	NC	float	Depop	Pop	Depop
AF3	NC	float	VCCVIDLB	Connect to +VCCVID	NC	float	Depop	Pop	Depop
AD20	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter			
AE23	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter			
AD1	VSS	Connect to GND	BOOTSELECT	CPU determine	VSS	Connect to GND	Pop	Depop	Pop
AE26	VSS	Connect to GND	OPTIMIZED/ COMPAT#	float	VSS	Connect to GND	Pop	Depop	Pop
AD25	TESTHI12	Pull-up 200ohm to +VCC_CORE	TESTHI12	Pull-up 62ohm to +VCC_CORE	DPSLP	Connect to PLD through 0ohm	Pop	Pop	Pop

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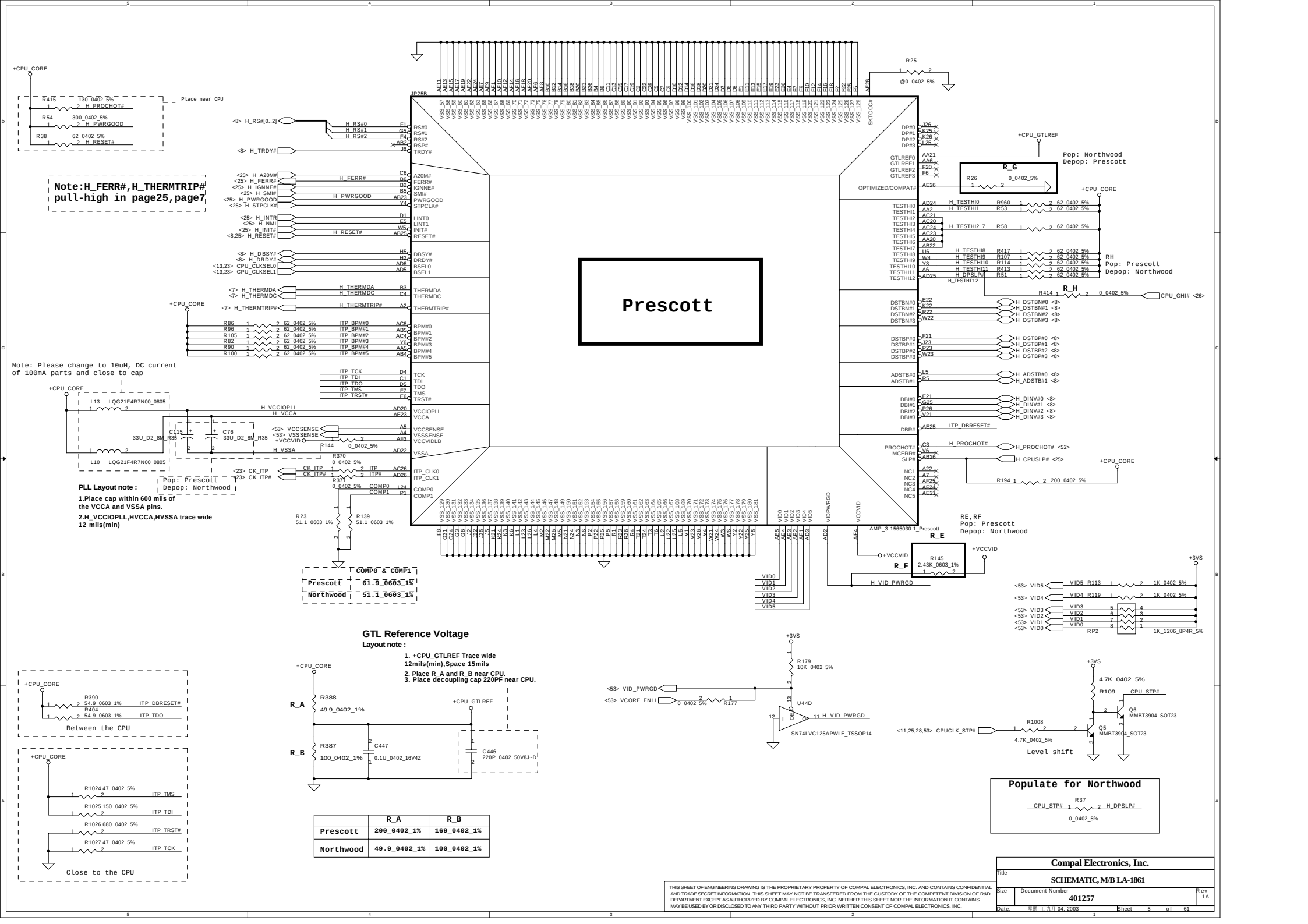
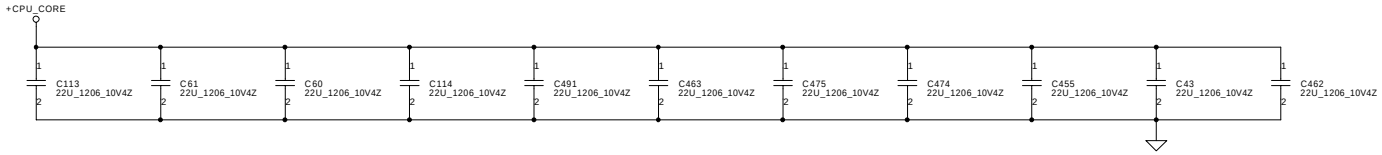


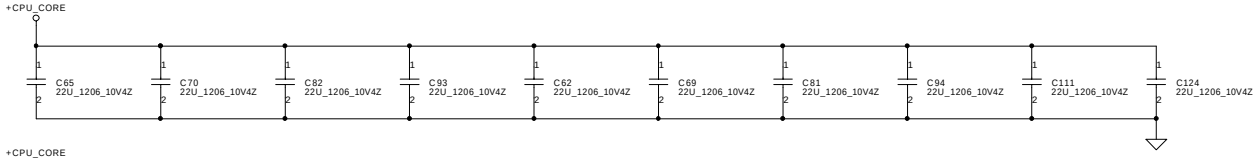
	R_A	R_B
Prescott	200_0402_1%	169_0402_1%
Northwood	49.9_0402_1%	100_0402_1%

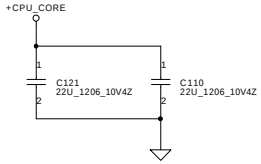
Place 11 North of Socket(Stuff 6)



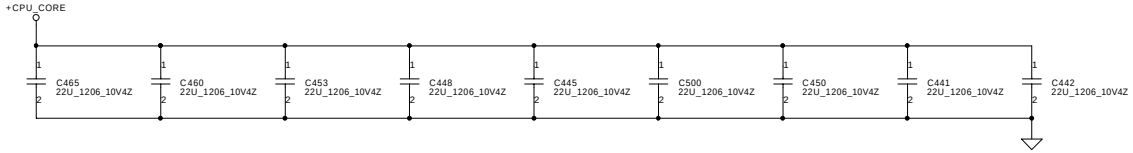
22uF depop reference
Springdale Chipset Platform Design Guide Rev1.11(12474)

Place 12 Inside Socket(Stuff all)

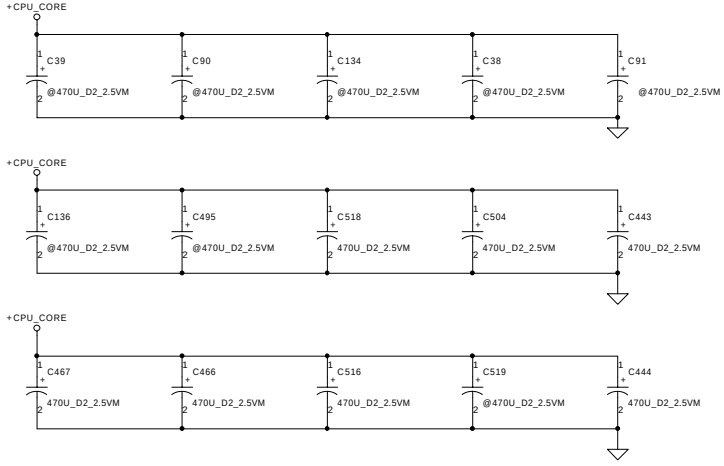


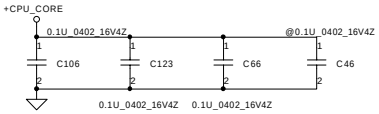


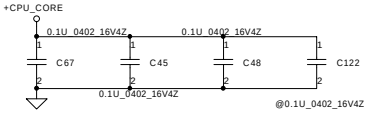
Place 9 South of Socket(Unstuff all)



470uF _ERS10m ohm* 15







Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11 (12474)page239

Decoupling Reference Requirement:
560uF Polymer, ESR:5m ohm(each) * 10
22uF X5R * 32

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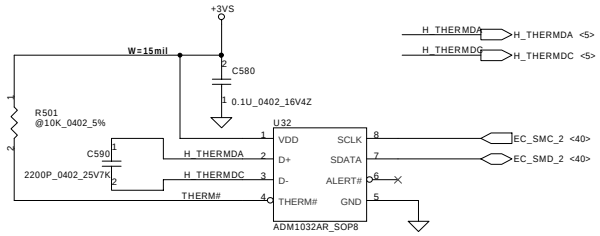
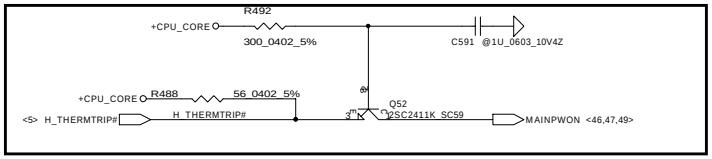
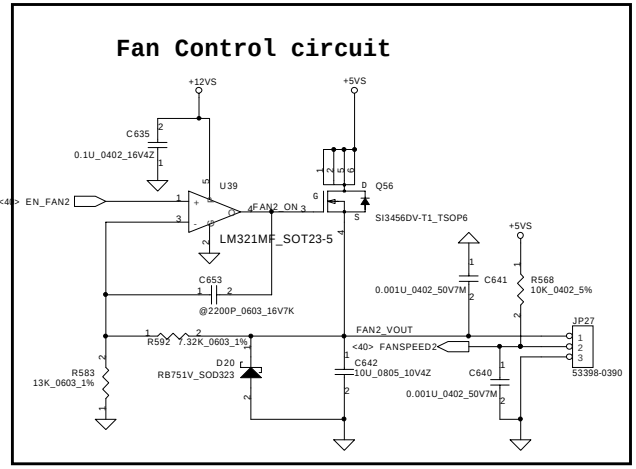
Thermal Sensor ADM1032AR



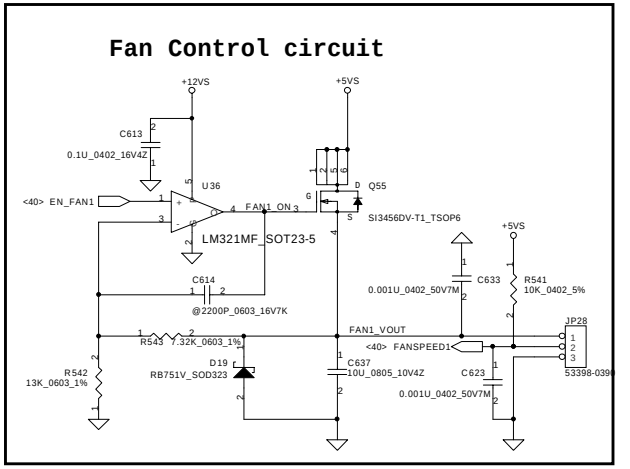
Address:1001_100X

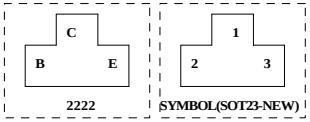


Fan Control circuit



Fan Control circuit





2222 SYMBOL(SOT23-NEW)

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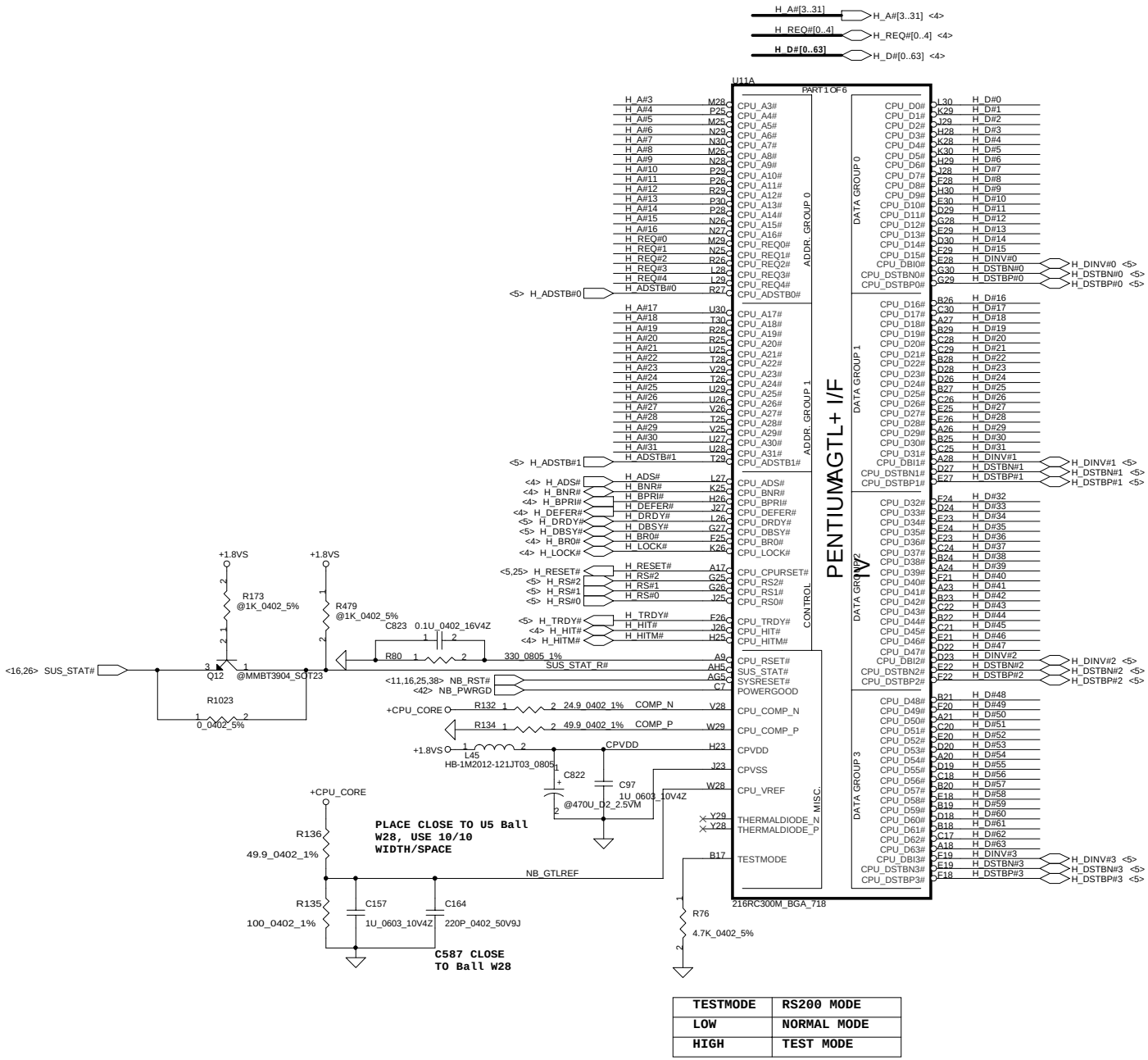

TESTMODE	RS200 MODE
LOW	NORMAL MODE
HIGH	TEST MODE

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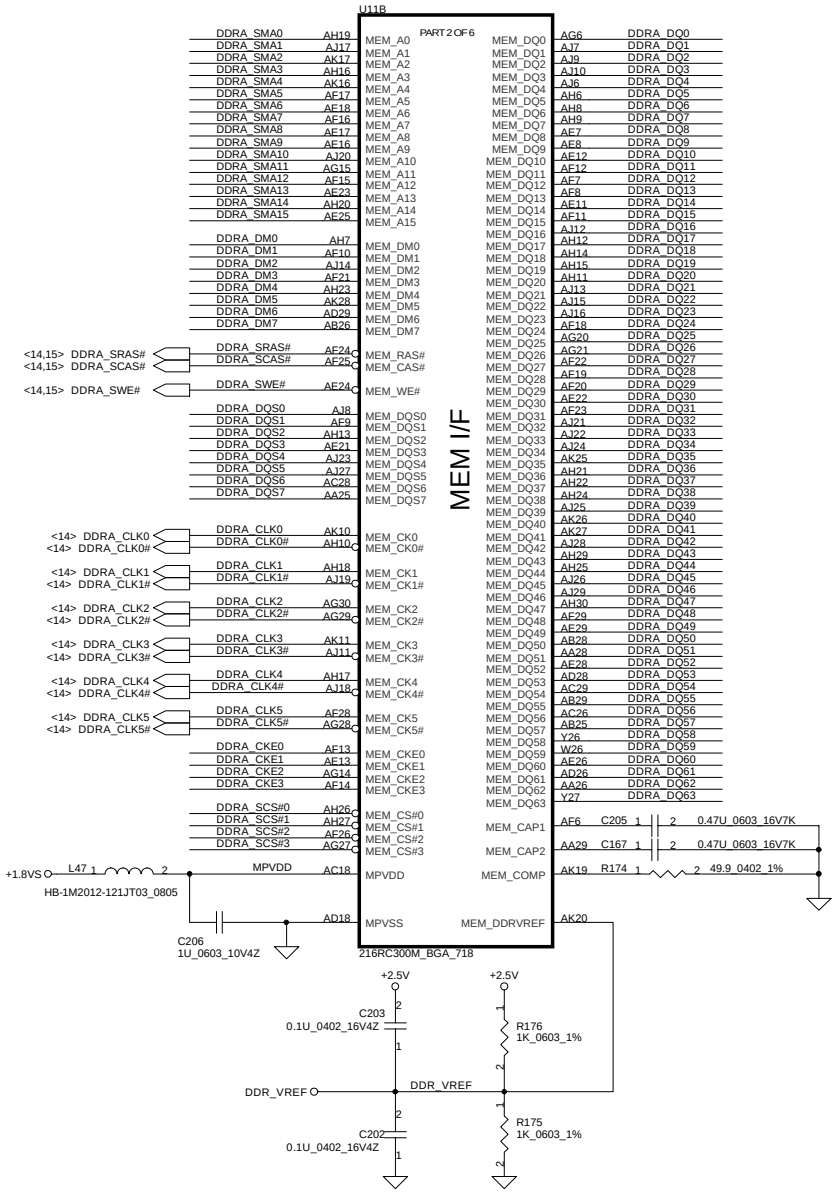

DDR_VREF trace width of 12mils and space 12mils(min)

DDRA_SDM[0..7] DDRA_SDM[0..7] <14,15>
DDRA_SDQ[0..63] DDRA_SDQ[0..63] <14,15>
DDRA_SDQS[0..7] DDRA_SDQS[0..7] <14,15>
DDRA_SMA[0..15] DDRA_SMA[0..15] <14,15>
DDRA_CKE[0..3] DDRA_CKE[0..3] <14,15>
DDRA_SCS#[0..3] DDRA_SCS#[0..3] <14,15>

As close as to DIMM

RP70: DDRA_DQ7 DDRA_DQ0 DDRA_DM0 DDRA_DQ5 — DDRA_SDQ7 DDRA_SDQ0 DDRA_SDM0 DDRA_SDQ5 — 0_0804_8P4R_5%
RP78: DDRA_DQ33 DDRA_DQ36 DDRA_DQ32 DDRA_DQ37 — DDRA_SDQ33 DDRA_SDQ36 DDRA_SDQ32 DDRA_SDQ37 — 0_0804_8P4R_5%
RP69: DDRA_DQ4 DDRA_DQ6 DDRA_DQ1 DDRA_DQ2 — DDRA_SDQ4 DDRA_SDQ6 DDRA_SDQ1 DDRA_SDQ2 — 0_0804_8P4R_5%
RP77: DDRA_DQS4 DDRA_DQ34 DDRA_DM4 DDRA_DQ38 — DDRA_SDQS4 DDRA_SDQ34 DDRA_SDM4 DDRA_SDQ38 — 0_0804_8P4R_5%
DDRA_DQ3 R621 0_0402_5% DDRA_SDQ3
DDRA_DQS0 R620 0_0402_5% DDRA_SDQS0
DDRA_DQ39 R629 0_0402_5% DDRA_SDQ39
DDRA_DQ35 R628 0_0402_5% DDRA_SDQ35
RP68: DDRA_DQ9 DDRA_DQ8 DDRA_DQ14 DDRA_DM1 — DDRA_SDQ9 DDRA_SDQ8 DDRA_SDQ14 DDRA_SDM1 — 0_0804_8P4R_5%
RP76: DDRA_DQ40 DDRA_DQ45 DDRA_DQ44 DDRA_DQS5 — DDRA_SDQ40 DDRA_SDQ45 DDRA_SDQ44 DDRA_SDQS5 — 0_0804_8P4R_5%
RP67: DDRA_DQ12 DDRA_DQ13 DDRA_DQ10 DDRA_DQS1 — DDRA_SDQ12 DDRA_SDQ13 DDRA_SDQ10 DDRA_SDQS1 — 0_0804_8P4R_5%
RP75: DDRA_DQ41 DDRA_DQ42 DDRA_DQ46 DDRA_DM5 — DDRA_SDQ41 DDRA_SDQ42 DDRA_SDQ46 DDRA_SDM5 — 0_0804_8P4R_5%
DDRA_DQ15 R619 0_0402_5% DDRA_SDQ15
DDRA_DQ11 R618 0_0402_5% DDRA_SDQ11
DDRA_DQ47 R627 0_0402_5% DDRA_SDQ47
DDRA_DQ43 R626 0_0402_5% DDRA_SDQ43
RP80: DDRA_DQ20 DDRA_DQS2 DDRA_DQ17 DDRA_DQ16 — DDRA_SDQ20 DDRA_SDQS2 DDRA_SDQ17 DDRA_SDQ16 — 0_0804_8P4R_5%
RP74: DDRA_DQ53 DDRA_DQ52 DDRA_DM6 DDRA_DQS6 — DDRA_SDQ53 DDRA_SDQ52 DDRA_SDM6 DDRA_SDQS6 — 0_0804_8P4R_5%
RP79: DDRA_DQ21 DDRA_DQ18 DDRA_DM2 DDRA_DQ22 — DDRA_SDQ21 DDRA_SDQ18 DDRA_SDM2 DDRA_SDQ22 — 0_0804_8P4R_5%
RP73: DDRA_DQ54 DDRA_DQ49 DDRA_DQ48 DDRA_DQ50 — DDRA_SDQ54 DDRA_SDQ49 DDRA_SDQ48 DDRA_SDQ50 — 0_0804_8P4R_5%
DDRA_DQ19 R630 0_0402_5% DDRA_SDQ19
DDRA_DQ23 R633 0_0402_5% DDRA_SDQ23
DDRA_DQ55 R625 0_0402_5% DDRA_SDQ55
DDRA_DQ51 R624 0_0402_5% DDRA_SDQ51
RP82: DDRA_DQ30 DDRA_DQ27 DDRA_DQ28 DDRA_DQS3 — DDRA_SDQ30 DDRA_SDQ27 DDRA_SDQ28 DDRA_SDQS3 — 0_0804_8P4R_5%
RP72: DDRA_DQ60 DDRA_DQ61 DDRA_DQ57 DDRA_DQ56 — DDRA_SDQ60 DDRA_SDQ61 DDRA_SDQ57 DDRA_SDQ56 — 0_0804_8P4R_5%
RP81: DDRA_DQ24 DDRA_DQ25 DDRA_DQ29 DDRA_DM3 — DDRA_SDQ24 DDRA_SDQ25 DDRA_SDQ29 DDRA_SDM3 — 0_0804_8P4R_5%
RP71: DDRA_DQS7 DDRA_DQ62 DDRA_DM7 DDRA_DQ63 — DDRA_SDQS7 DDRA_SDQ62 DDRA_SDM7 DDRA_SDQ63 — 0_0804_8P4R_5%
DDRA_DQ26 R632 0_0402_5% DDRA_SDQ26
DDRA_DQ31 R631 0_0402_5% DDRA_SDQ31
DDRA_DQ58 R623 0_0402_5% DDRA_SDQ58
DDRA_DQ59 R622 0_0402_5% DDRA_SDQ59

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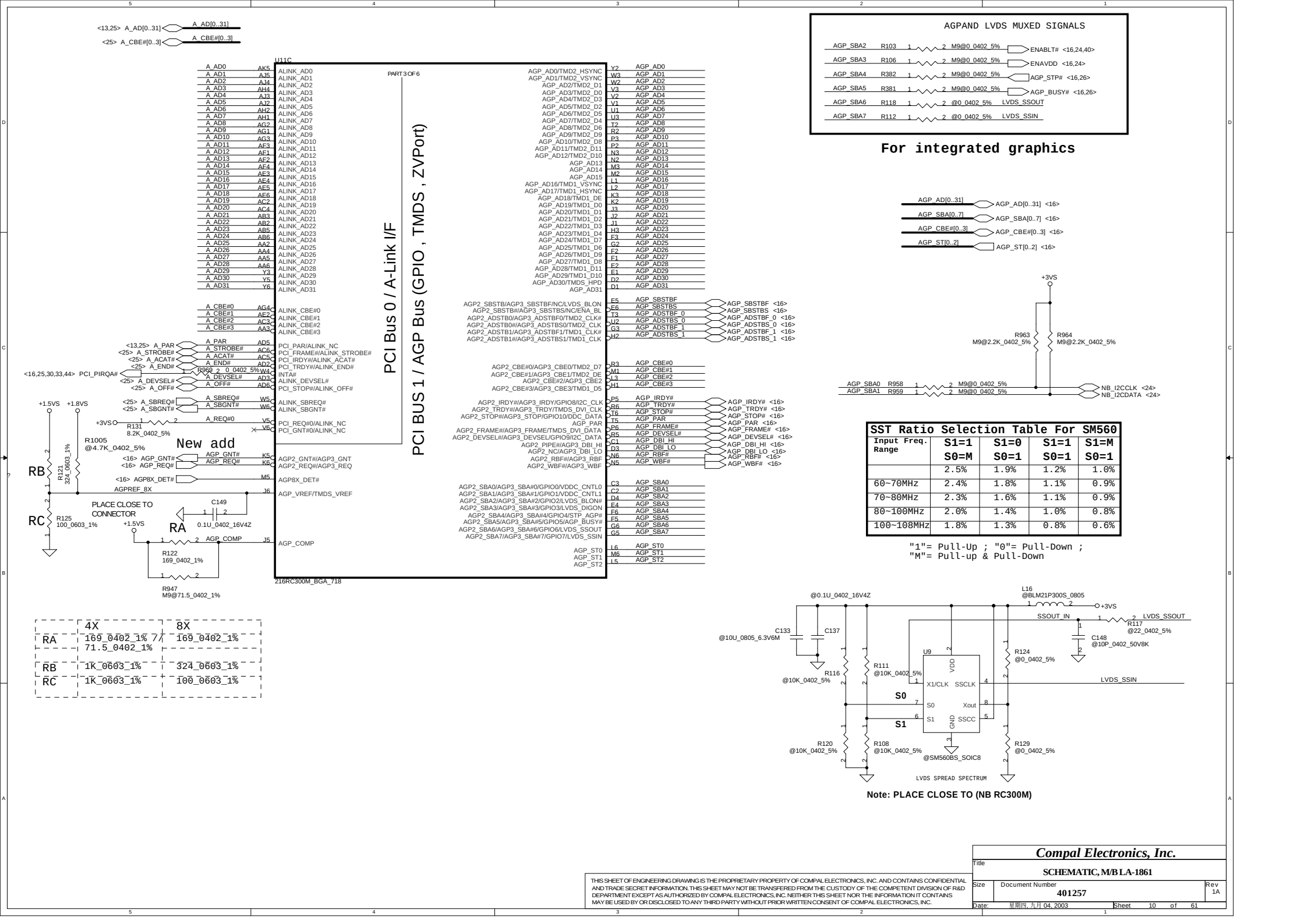
AGPAND LVDS MUXED SIGNALS
AGP_SBA2 R103 M9@0_0402_5% ENABLT# <16,24,40>
AGP_SBA3 R106 M9@0_0402_5% ENAVDD <16,24>
AGP_SBA4 R382 M9@0_0402_5% AGP_STP# <16,26>
AGP_SBA5 R381 M9@0_0402_5% AGP_BUSY# <16,26>
AGP_SBA6 R118 @0_0402_5% LVDS_SSOUT
AGP_SBA7 R112 @0_0402_5% LVDS_SSIN
For integrated graphics
U11C
PART 3 OF 6
PCI Bus 0 / A-Link I/F
PCI BUS 1 / AGP Bus (GPIO , TMDS , ZVPort)
216RC300M_BGA_718
New add
PLACE CLOSE TO CONNECTOR
SST Ratio Selection Table For SM560
Input Freq. Range
S1=1 S0=M
S1=0 S0=1
S1=1 S0=1
S1=M S0=1
2.5% 1.9% 1.2% 1.0%
60~70MHz 2.4% 1.8% 1.1% 0.9%
70~80MHz 2.3% 1.6% 1.1% 0.9%
80~100MHz 2.0% 1.4% 1.0% 0.8%
100~108MHz 1.8% 1.3% 0.8% 0.6%
"1"= Pull-Up ; "0"= Pull-Down ;
"M"= Pull-up & Pull-Down
4X 8X
RA 169_0402_1% / 71.5_0402_1% 169_0402_1%
RB 1K_0603_1% 324_0603_1%
RC 1K_0603_1% 100_0603_1%
SM560BS_SOIC8
LVDS SPREAD SPECTRUM
Note: PLACE CLOSE TO (NB RC300M)
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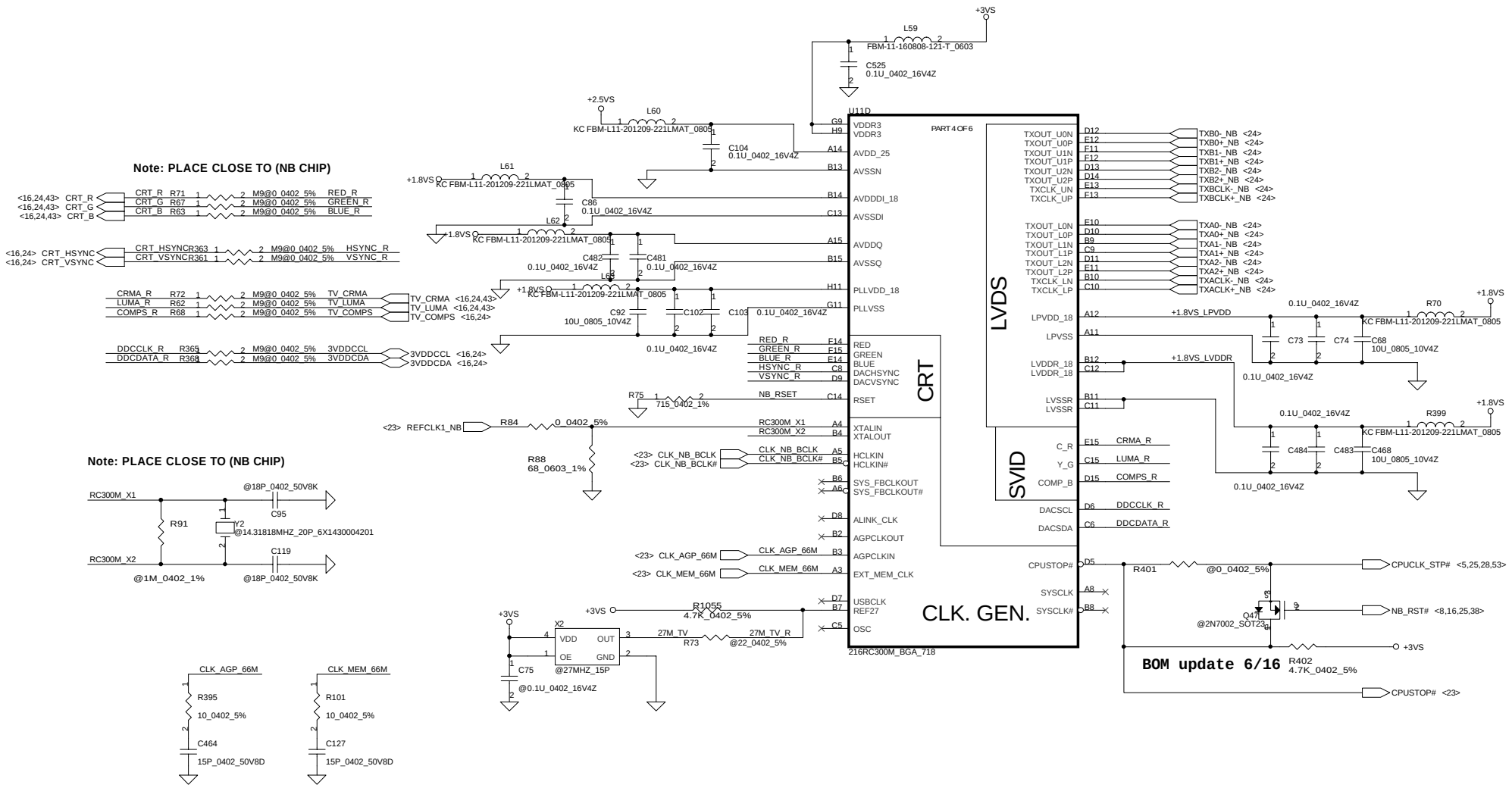

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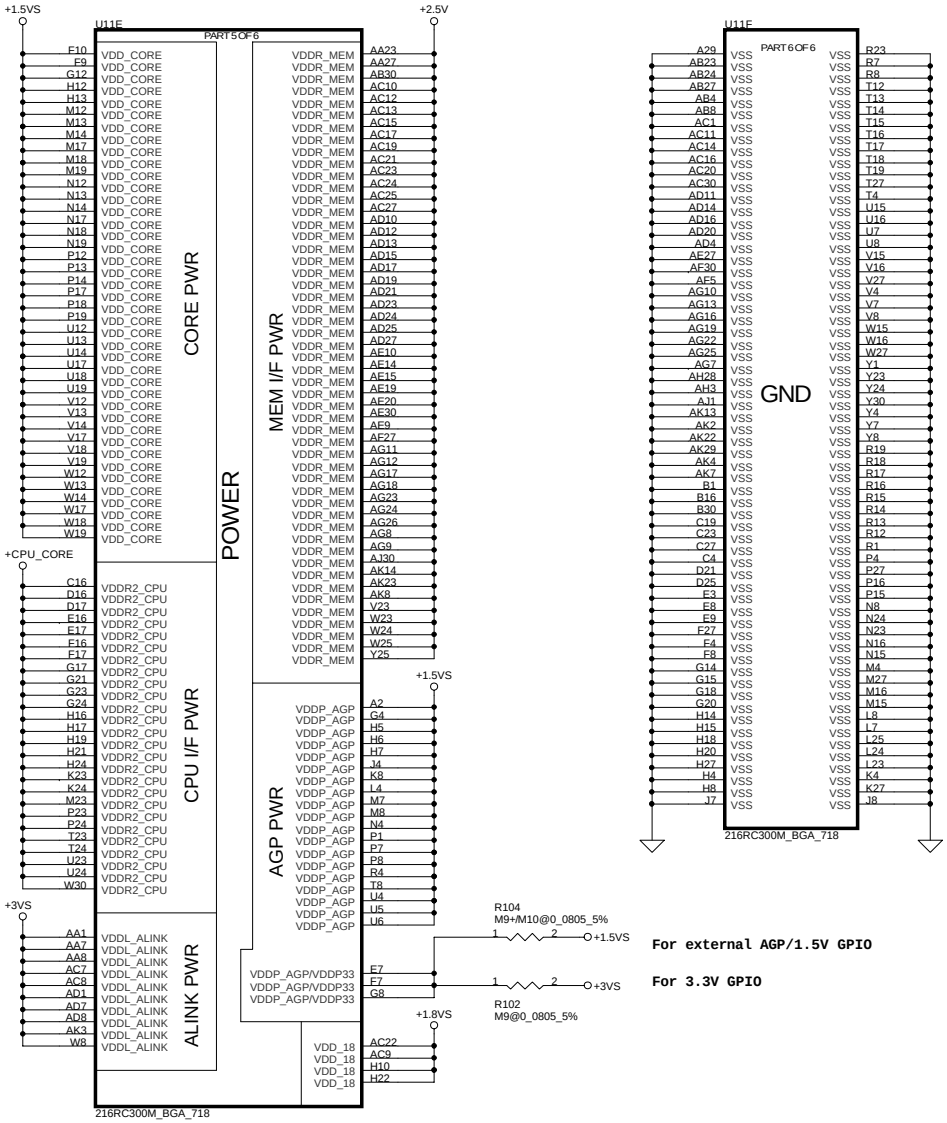
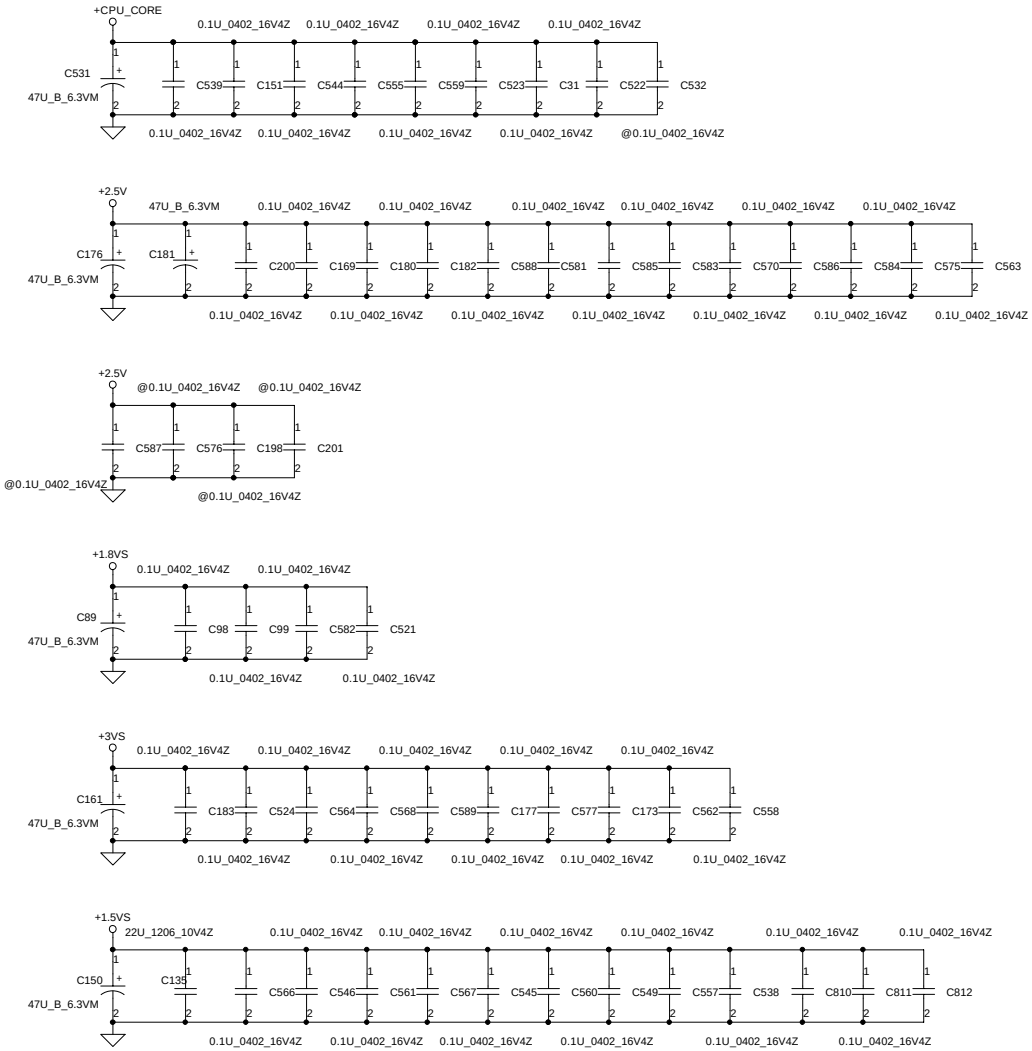


For external AGP/1.5V GPIO

For 3.3V GPIO



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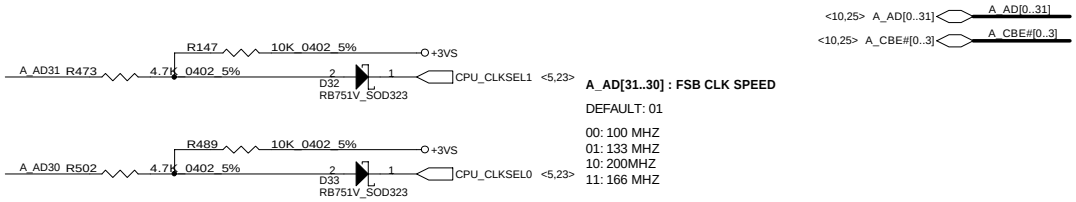
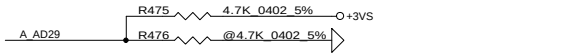


A_AD[31..30] : FSB CLK SPEED

DEFAULT: 01

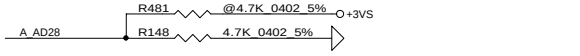
00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11: 166 MHZ



A_AD29: STRAP CONFIGURATION

DEFAULT:1

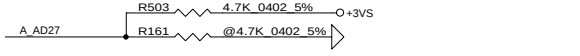
0: REDUCEDE SET
1: FULL SET



A_AD28: SPREAD SPECTRUM ENABLE

DEFAULT:0

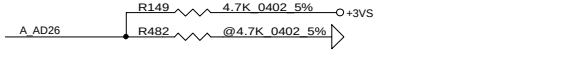
0: DISABLE
1: ENABLE



A_AD27: FrcShortReset#

DEFAULT: 1

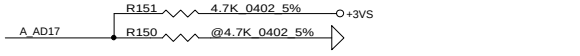
0: TEST MODE
1: NORMAL MODE

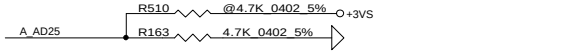


A_AD26 : ENABLE IOQ

DEFAULT: 1

0: IOQ=1
1: IOQ=12

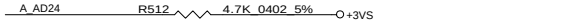




A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 00

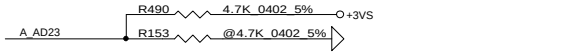
00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V



A_AD24 : MOBILE CPU SELECT

DEFAULT: 1

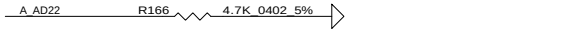
0: BANIAS CPU
1: OTHER CPU



A_AD23 : CLOCK BYPASS DISABLE

DEFAULT: 1

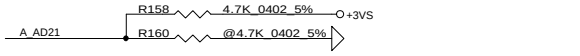
0: TEST MODE
1: NORMAL



A_AD22 : OSC PAD OUTPUT PCICLK

DEFAULT : 1

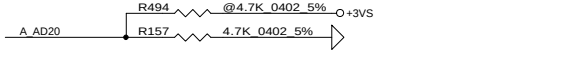
0: OSC CLK OUT
1: PCICLK OUT



A_AD21 : AUTO_CAL ENABLE

DEFAULT : 1

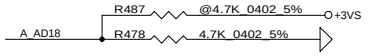
0: DISABLE
1: ENABLE



A_AD20 : INTERNAL CLK GEN ENABLE

DEFAULT : 0

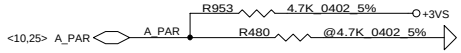
0: DISABLE
1: ENABLE



A_AD18 : ENABLE PHASE CALIBRATION

DEFAULT: 0

0: ENABLE
1: DISABLE



PAR: EXTENDED DEBUG MODE

DEFAULT : 1

0: DEBUG MODE
1: NORMAL

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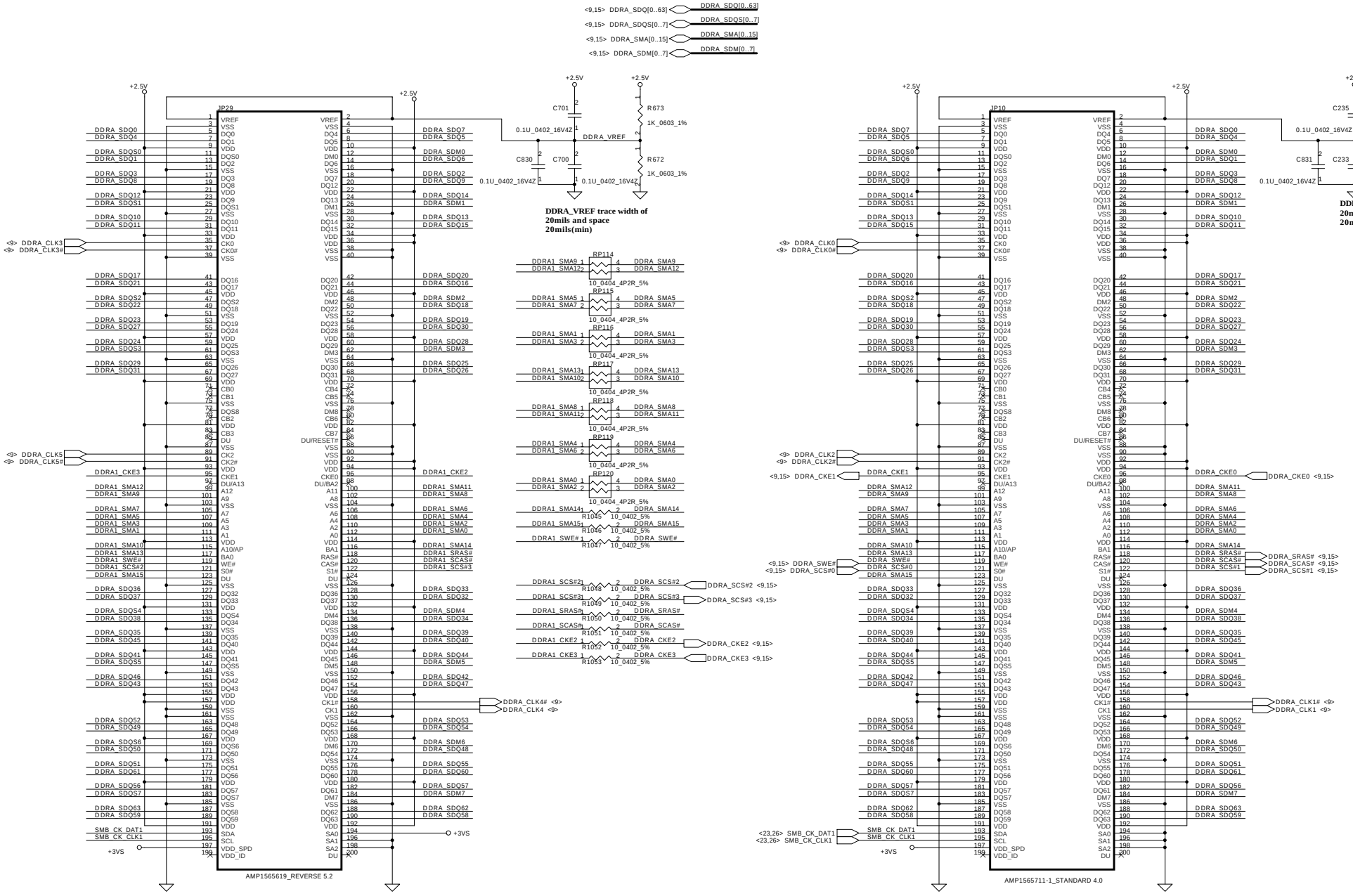

DIMM1 REVERSE

DIMM0 STANDARD

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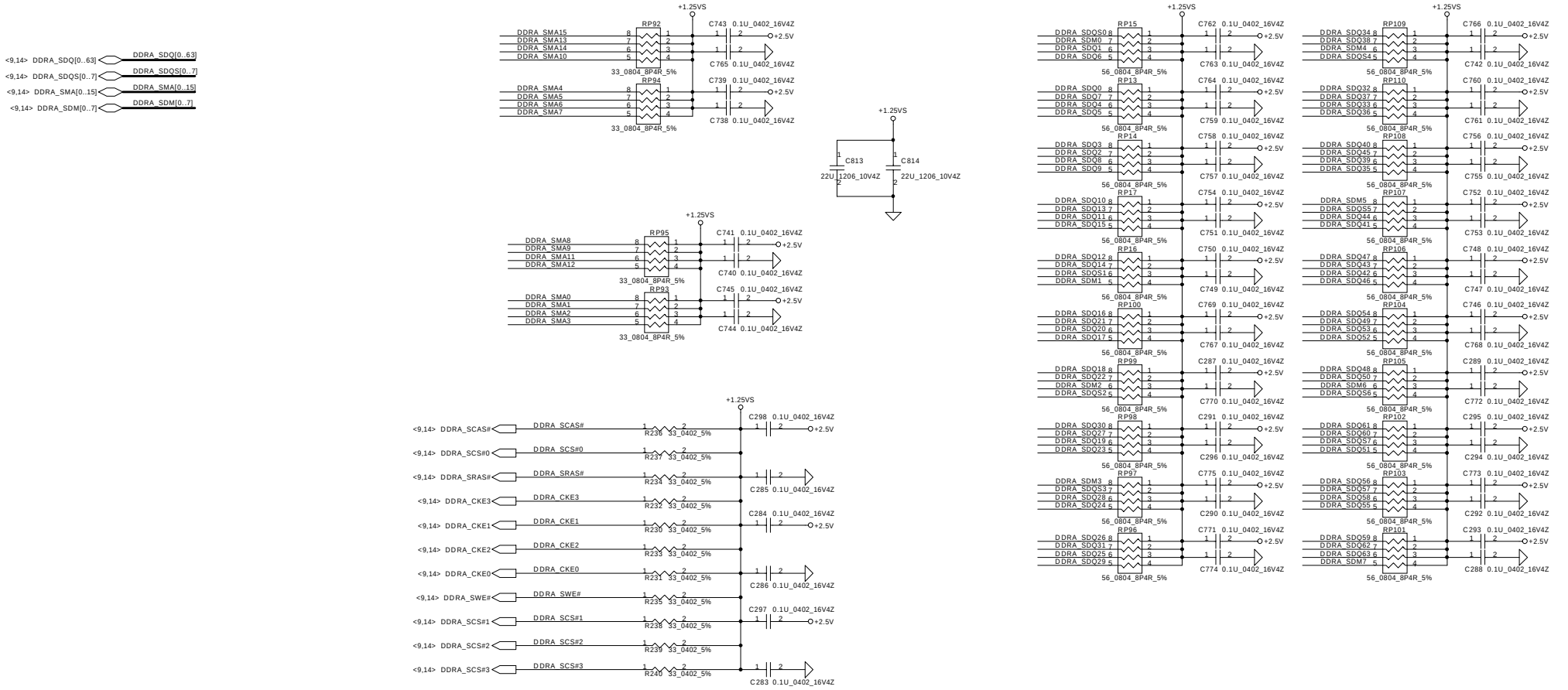
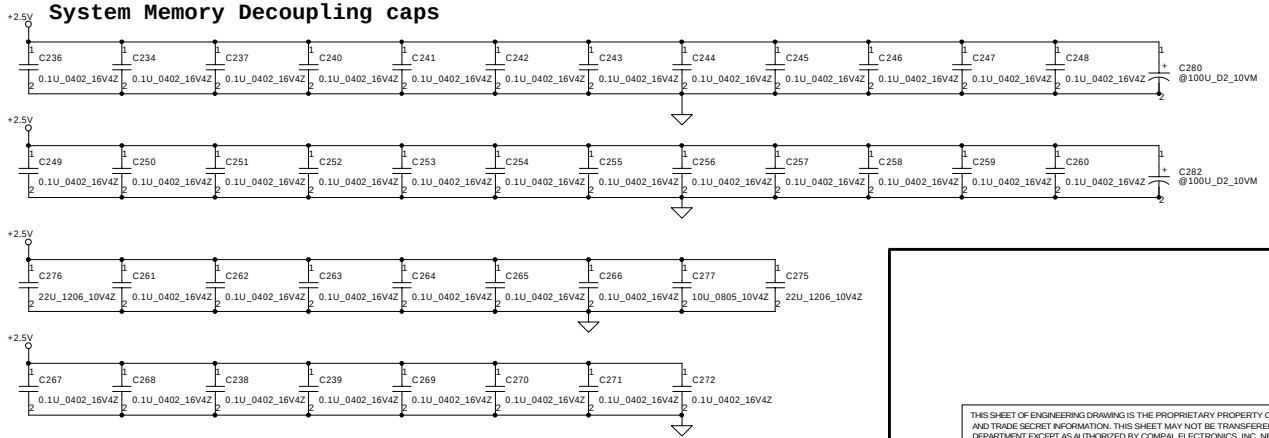
DDR Termination resistors & Decoupling caps



System Memory Decoupling caps



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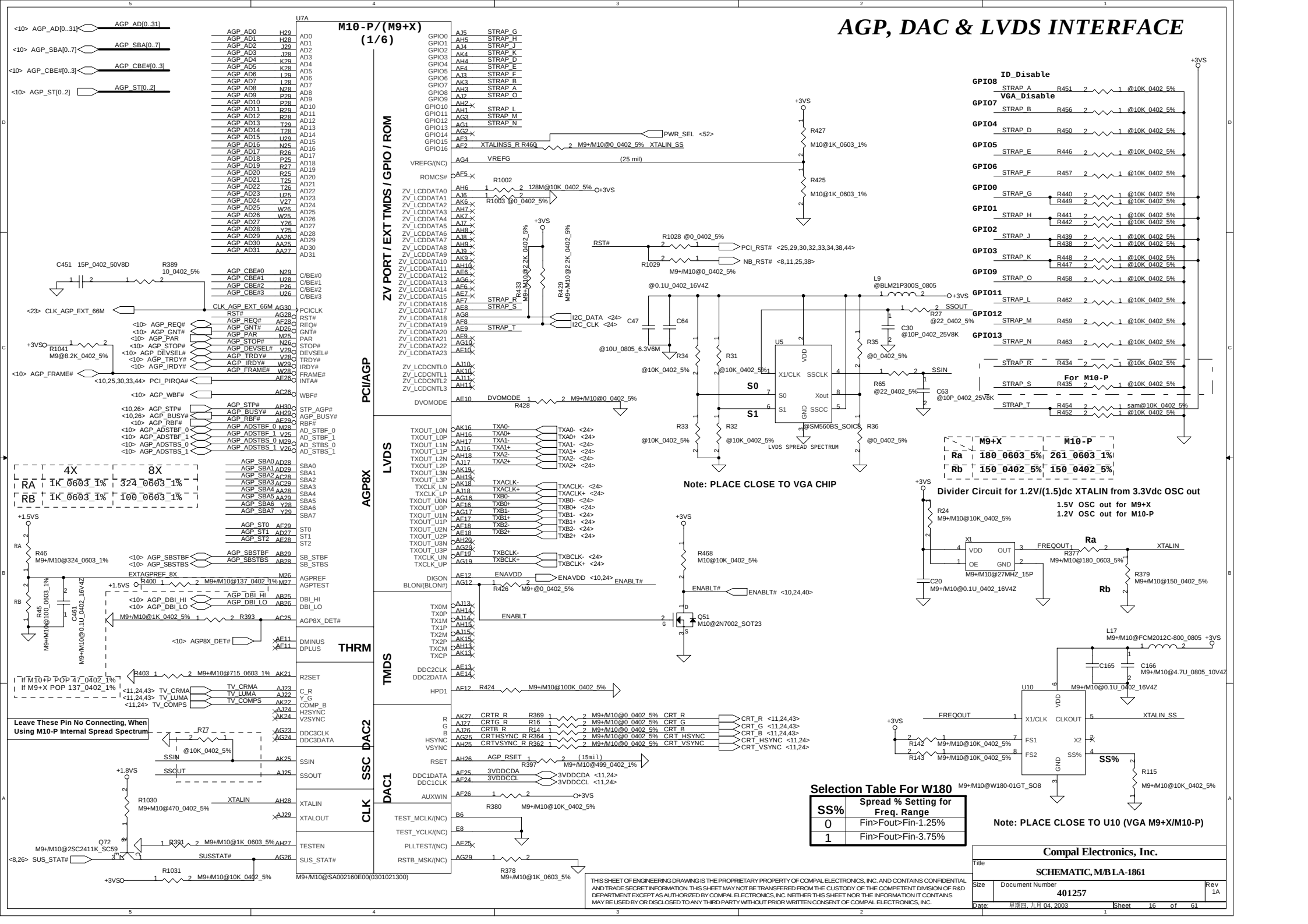
AGP, DAC & LVDS INTERFACE



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MEMORY INTERFACE A

<21> R_NMDA[0..63] — R_NMDA[0..63]
<21> NMAA[0..13] — NMAA[0..13]
<21> NDQMA[0..7] — NDQMA[0..7]
<21> NDQSA[0..7] — NDQSA[0..7]

U7B

M10-P/(M9+X) (2/6)

MEMORY INTERFACE A

R_NMDA0	L25	DQA0	
R_NMDA1	L26	DQA1	
R_NMDA2	K25	DQA2	
R_NMDA3	K26	DQA3	
R_NMDA4	J26	DQA4	
R_NMDA5	H25	DQA5	
R_NMDA6	H26	DQA6	
R_NMDA7	G26	DQA7	
R_NMDA8	G30	DQA8	
R_NMDA9	D29	DQA9	
R_NMDA10	D28	DQA10	
R_NMDA11	E28	DQA11	
R_NMDA12	E29	DQA12	
R_NMDA13	G29	DQA13	
R_NMDA14	G28	DQA14	
R_NMDA15	F28	DQA15	
R_NMDA16	G25	DQA16	
R_NMDA17	F26	DQA17	
R_NMDA18	E26	DQA18	
R_NMDA19	F25	DQA19	
R_NMDA20	E24	DQA20	
R_NMDA21	F23	DQA21	
R_NMDA22	E23	DQA22	
R_NMDA23	D22	DQA23	
R_NMDA24	B29	DQA24	
R_NMDA25	C29	DQA25	
R_NMDA26	C25	DQA26	
R_NMDA27	C27	DQA27	
R_NMDA28	B28	DQA28	
R_NMDA29	B25	DQA29	
R_NMDA30	C26	DQA30	
R_NMDA31	B26	DQA31	
R_NMDA32	F17	DQA32	
R_NMDA33	E17	DQA33	
R_NMDA34	D16	DQA34	
R_NMDA35	F16	DQA35	
R_NMDA36	E15	DQA36	
R_NMDA37	F14	DQA37	
R_NMDA38	E14	DQA38	
R_NMDA39	F13	DQA39	
R_NMDA40	C17	DQA40	
R_NMDA41	B18	DQA41	
R_NMDA42	B17	DQA42	
R_NMDA43	B15	DQA43	
R_NMDA44	C13	DQA44	
R_NMDA45	B14	DQA45	
R_NMDA46	C14	DQA46	
R_NMDA47	C16	DQA47	
R_NMDA48	A13	DQA48	
R_NMDA49	A12	DQA49	
R_NMDA50	C12	DQA50	
R_NMDA51	B12	DQA51	
R_NMDA52	C10	DQA52	
R_NMDA53	C9	DQA53	
R_NMDA54	B9	DQA54	
R_NMDA55	B10	DQA55	
R_NMDA56	E13	DQA56	
R_NMDA57	E12	DQA57	
R_NMDA58	E10	DQA58	
R_NMDA59	F12	DQA59	
R_NMDA60	F11	DQA60	
R_NMDA61	F9	DQA61	
R_NMDA62	F9	DQA62	
R_NMDA63	F8	DQA63	

AA0	E22	NMAA0	
AA1	B22	NMAA1	
AA2	B23	NMAA2	
AA3	B24	NMAA3	
AA4	C23	NMAA4	
AA5	C22	NMAA5	
AA6	F22	NMAA6	
AA7	F21	NMAA7	
AA8	C21	NMAA8	
AA9	A24	NMAA9	
AA10	C24	NMAA10	
AA11	A25	NMAA11	
AA12/(AA13)	E21	NMAA12	
AA13/(AA12)	B20	NMAA13	
AA14/(NC)	C19		
DQMA#0	J25	NDQMA0	
DQMA#1	E29	NDQMA1	
DQMA#2	E25	NDQMA2	
DQMA#3	A27	NDQMA3	
DQMA#4	F15	NDQMA4	
DQMA#5	C15	NDQMA5	
DQMA#6	C11	NDQMA6	
DQMA#7	E11	NDQMA7	
QSA0	J27	NDQSA0	
QSA1	F30	NDQSA1	
QSA2	F24	NDQSA2	
QSA3	B27	NDQSA3	
QSA4	E16	NDQSA4	
QSA5	B16	NDQSA5	
QSA6	B11	NDQSA6	
QSA7	F10	NDQSA7	
RASA#	A19	NMRASA#	NMRASA# <21>
CASA#	E18	NMCASA#	NMCASA# <21>
WEA#	E19	NMWEA#	NMWEA# <21>
CSA0#	E20	NMCSA0#	NMCSA0# <21>
CSA1#	E20	NMCSA1#	NMCSA1# <21>
CKEA	B19	NMCKEA	NMCKEA <21>
CLKA0	B21	NMCLKA0	NMCLKA0 <21>
CLKA0#	C20	NMCLKA0#	NMCLKA0# <21>
CLKA1	C18	NMCLKA1	NMCLKA1 <21>
CLKA1#	A18	NMCLKA1#	NMCLKA1# <21>
DIMA0	D30		
DIMA1	B13		
MVREFD	B7	MVREFD	
MVREFS/(NC)	B8	MVREFS	

M9+/M10@SA002160E00(0301021300)

+2.5VS
R431 M9+/M10@1K_0402_1%
MVREFD (25 mil)
C543 M9+/M10@0.1U_0402_16V4Z
R430 M9+/M10@1K_0402_1%

+2.5VS
R437 M10@1K_0402_1%
MVREFS (25 mil)
C542 M10@0.1U_0402_16V4Z
R436 M10@1K_0402_1%

Poped for M10-P
Depoped for M9+X

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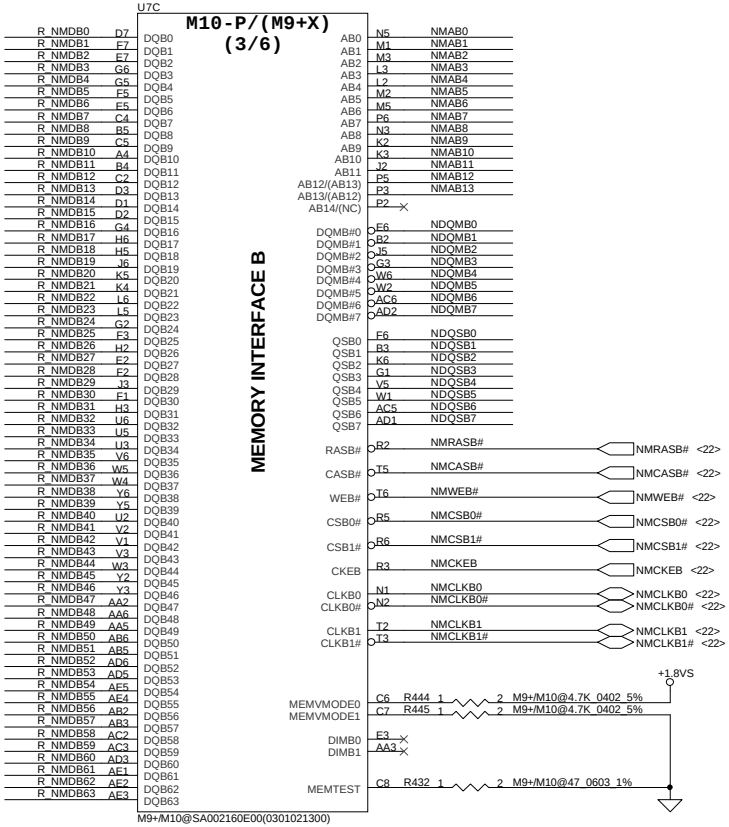
MEMORY INTERFACE B

<22> R_NMDB[0..63] → R_NMDB[0..63]

<22> NMAB[0..13] → NMAB[0..13]

<22> NDQMB[0..7] → NDQMB[0..7]

<22> NDQSB[0..7] → NDQSB[0..7]



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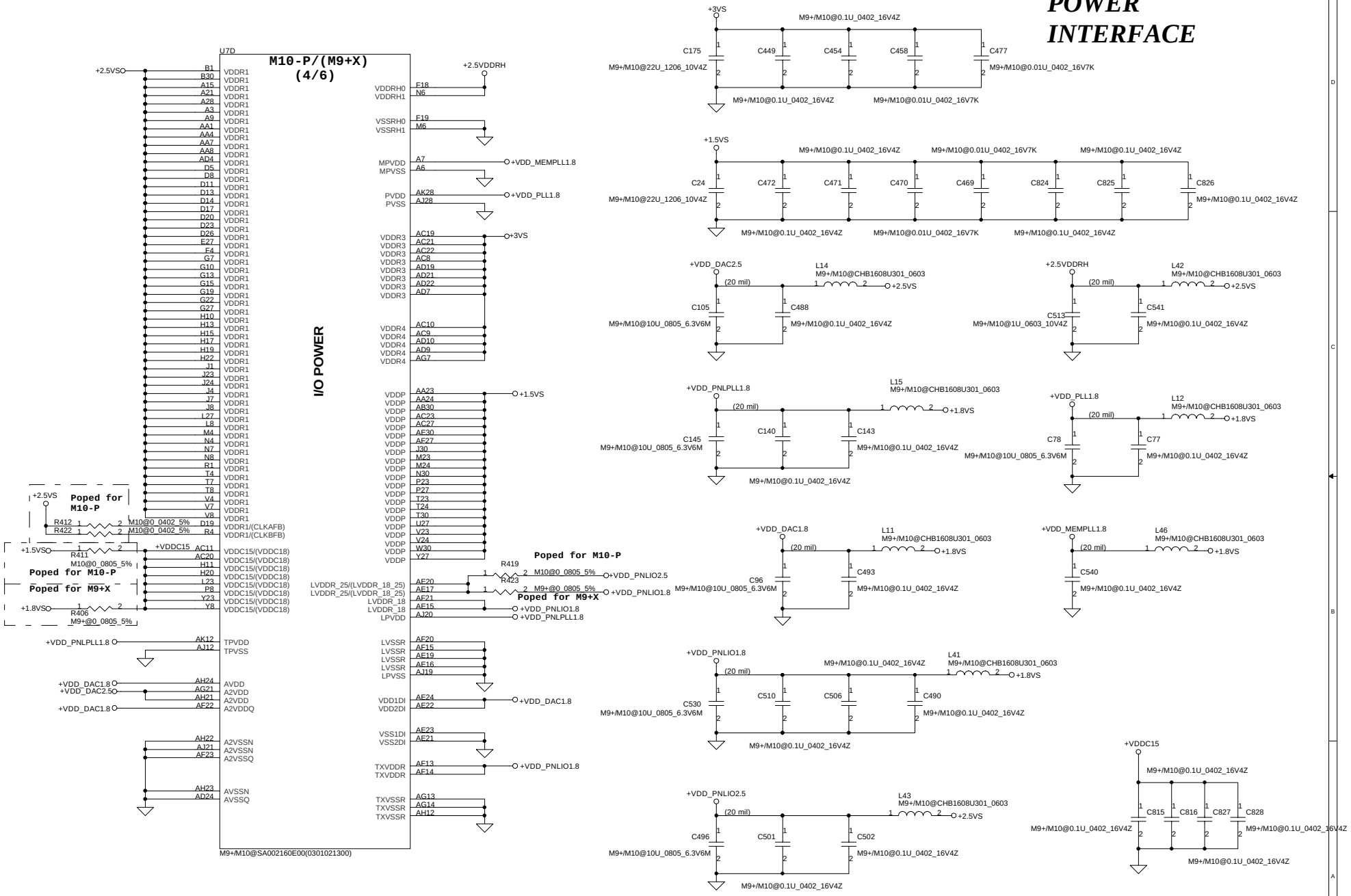
POWER INTERFACE



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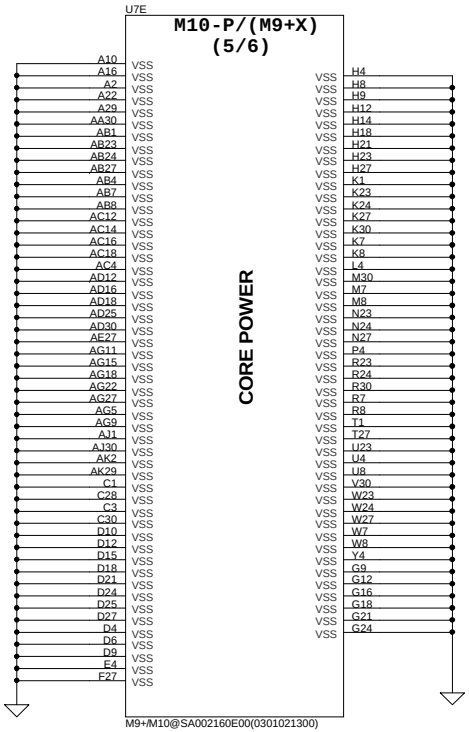
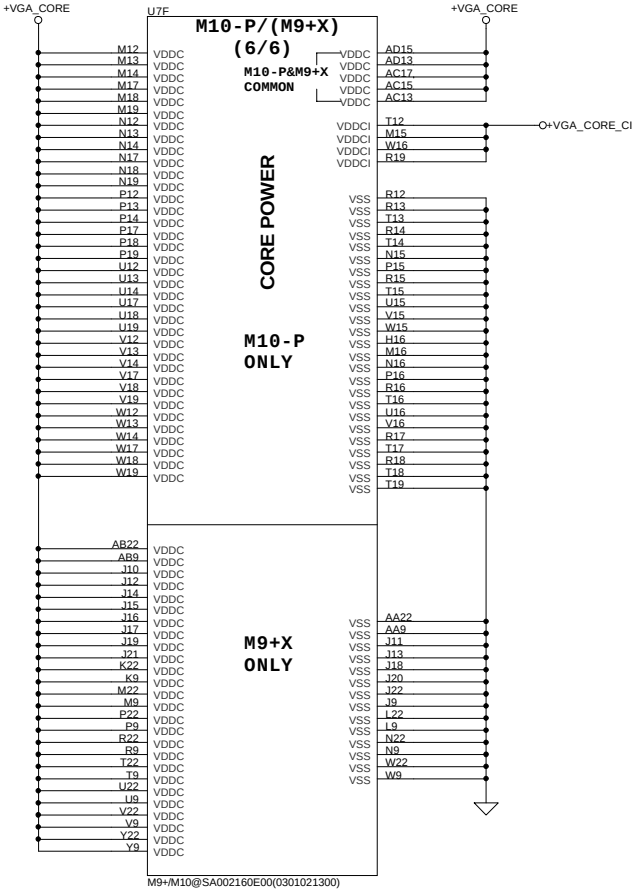
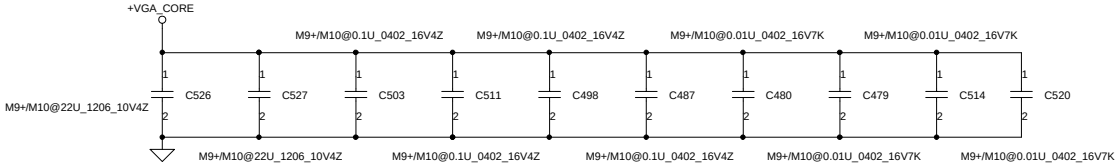
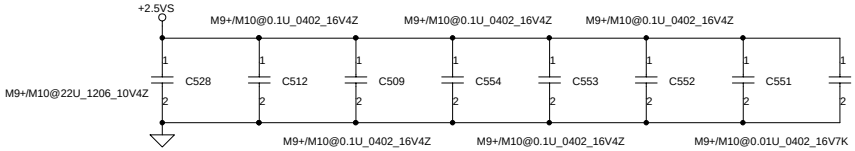
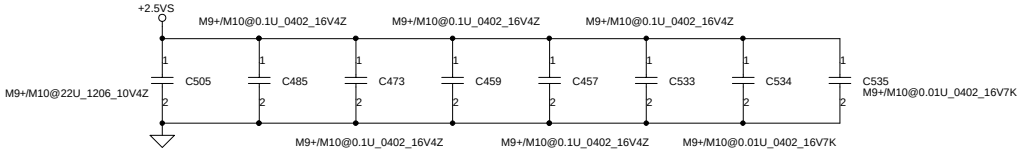
POWER INTERFACE



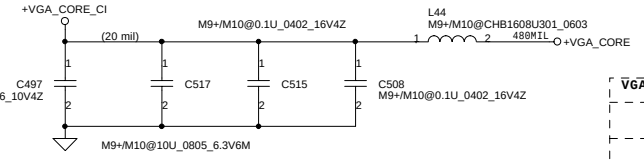








As close as possible to related pin



As close as possible to related pin

VGA_CORE for M10P	VGA_CORE for M9+
1.2	1.5V
1.0	1.25V

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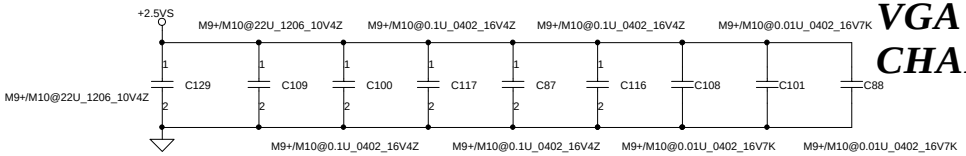
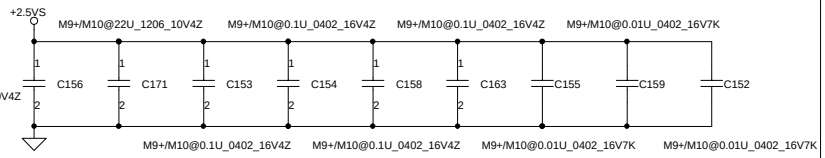
VGA DDR FOR CHANNEL A

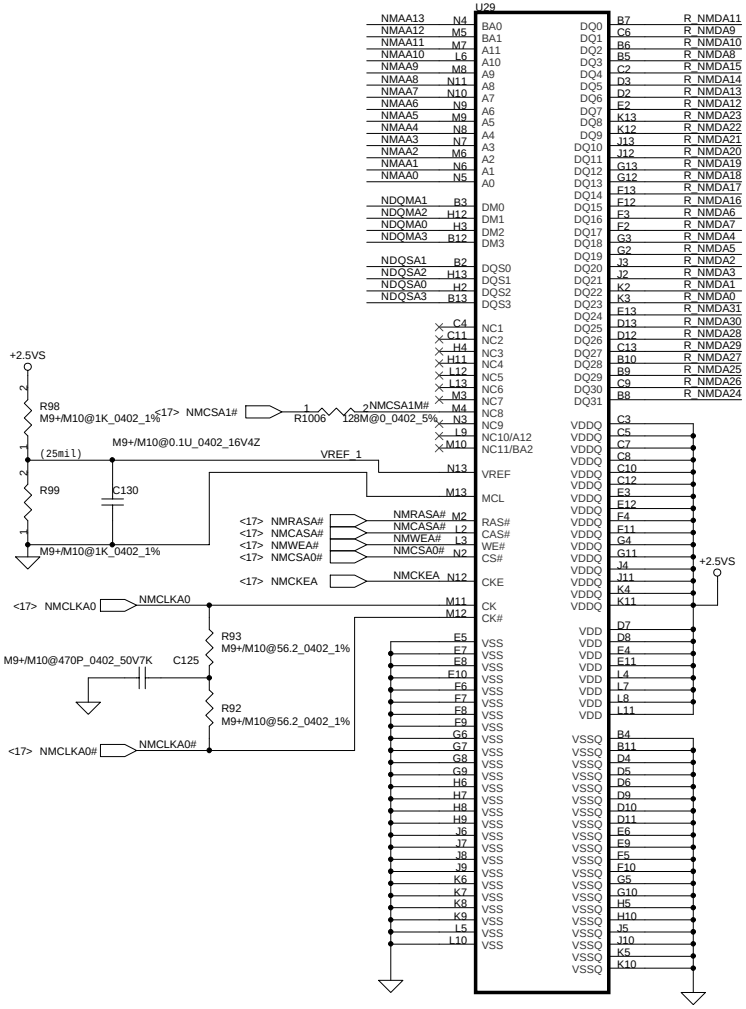


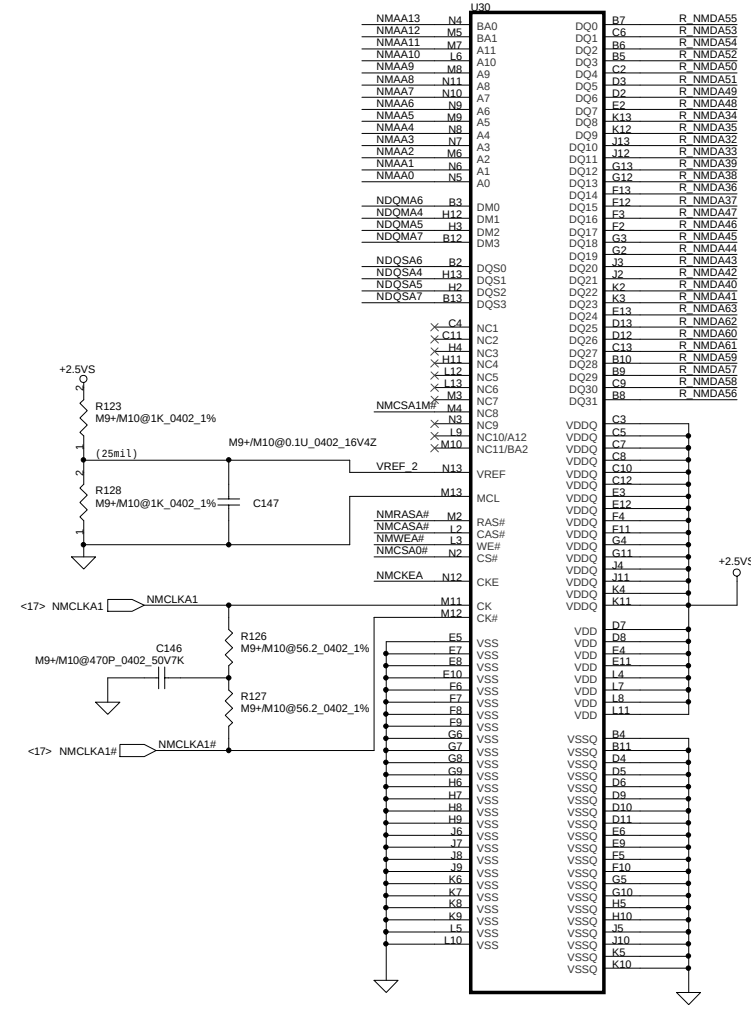


As close as ppossible to related pin

As close as ppossible to related pin

<17> NMAA[0..13] — NMAA[0..13]
<17> R_NMDA[0..63] — R_NMDA[0..63]
<17> NDQMA[0..7] — NDQMA[0..7]
<17> NDQSA[0..7] — NDQSA[0..7]





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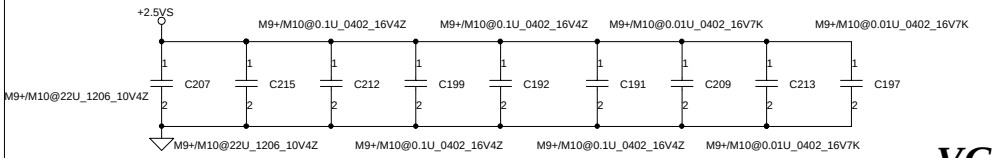
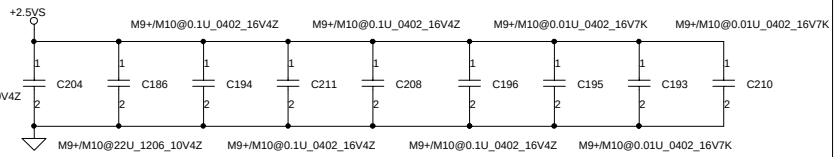
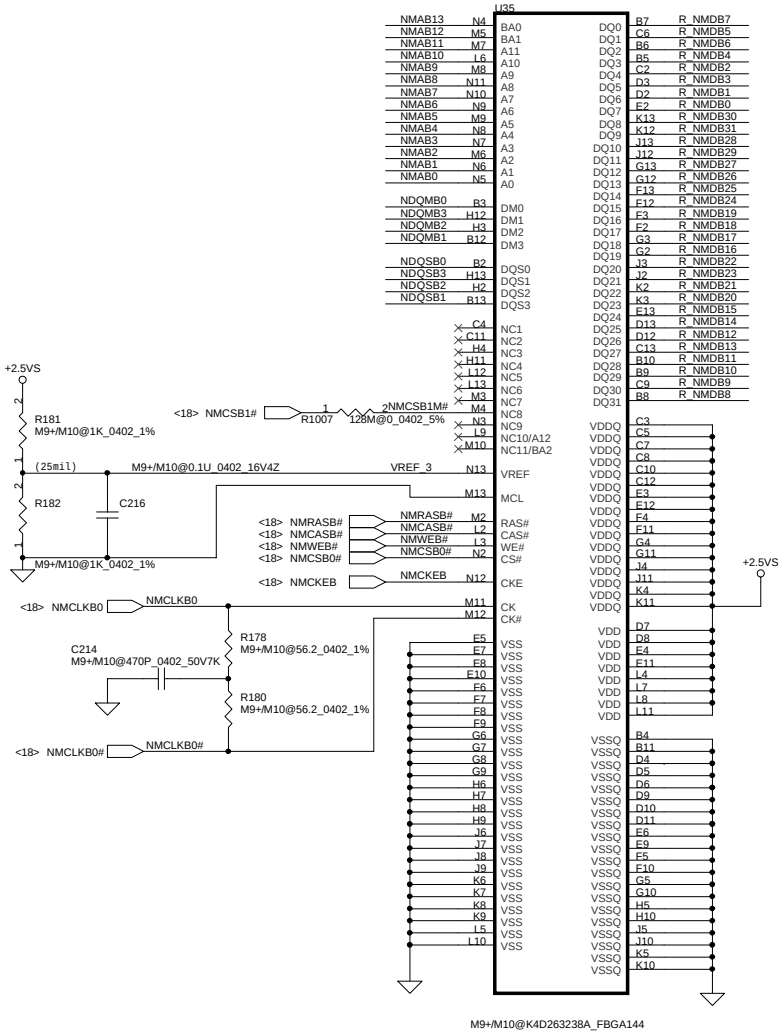
VGA DDR FOR CHANNEL B

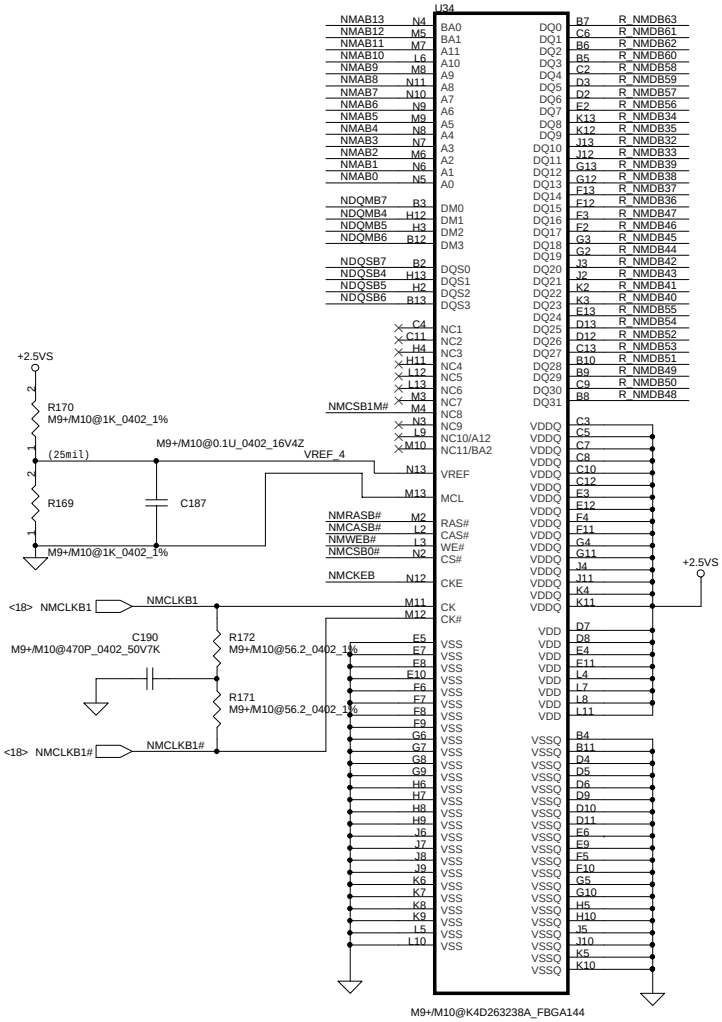


As close as ppossible to related pin



As close as ppossible to related pin





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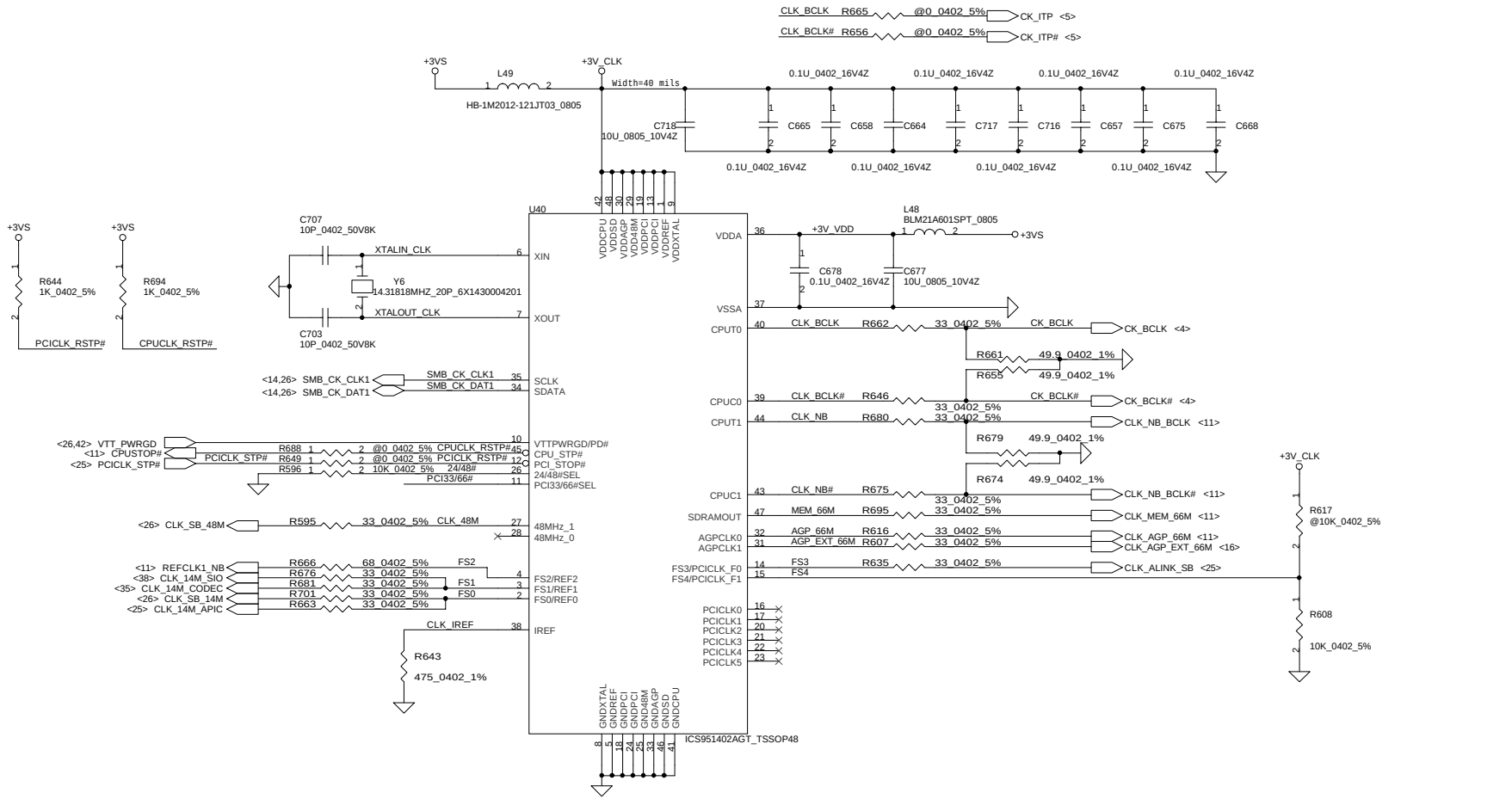

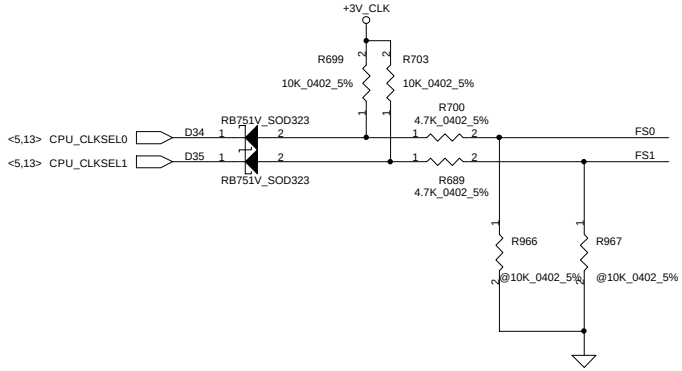

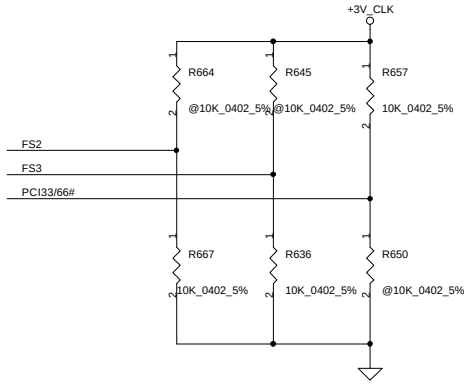

CLOCK FREQUENCY SELECT TABLE

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled…
0	0	0	1	0	200	200	
0	0	0	0	1	133	133	* Spreaf OFF OR Center spread +/-0.3%
0	0	0	0	0	100	100	

Note: 0 = PULL LOW
1 = PULL HIGH

A-LINK FREQ

PCI33/66# = HIGH	66MHZ
PCI33/66# = LOW	33MHZ

A_AD[31..30] : FSB CLK SPEED

DEFAULT: 01

00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11:166 MHZ

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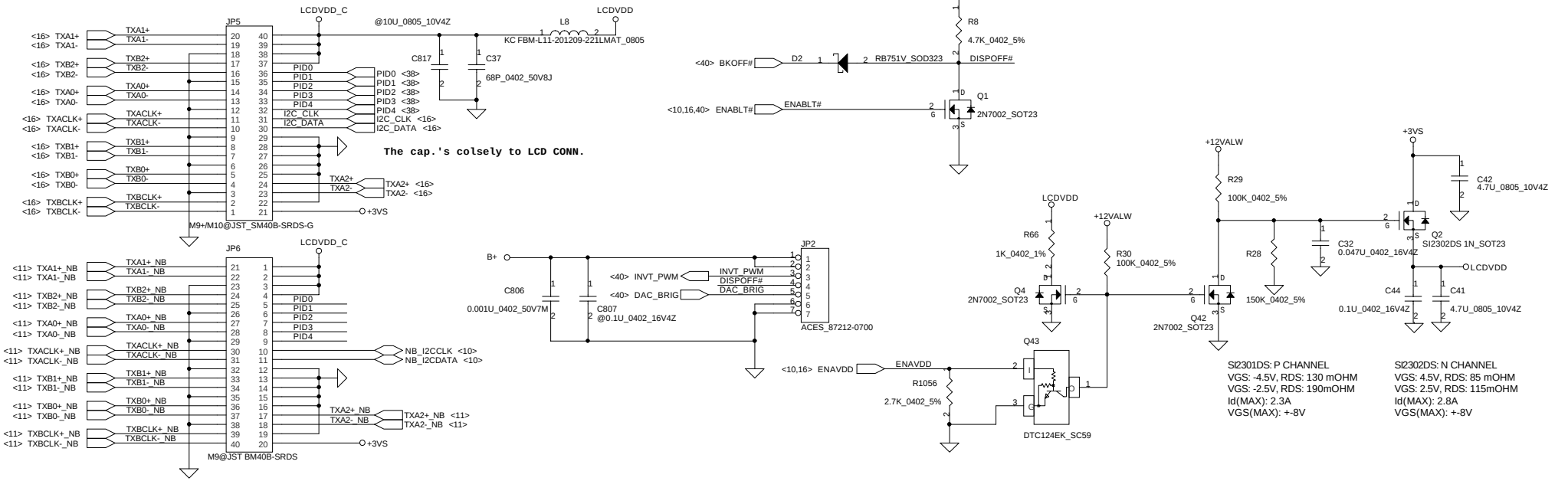
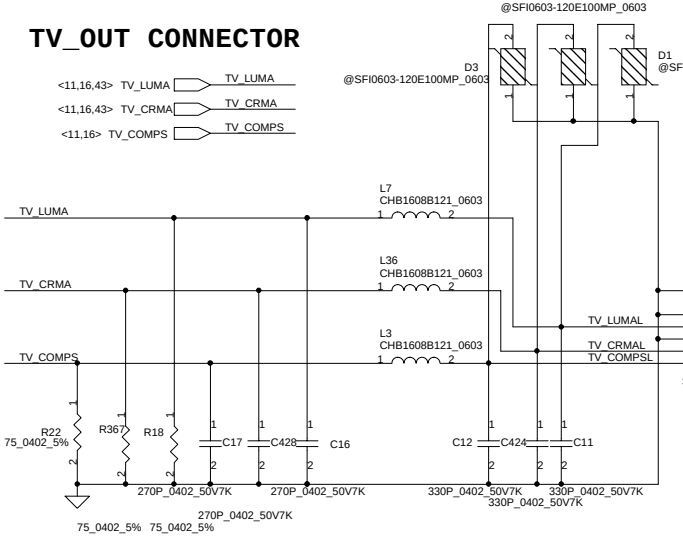
LCD CONN



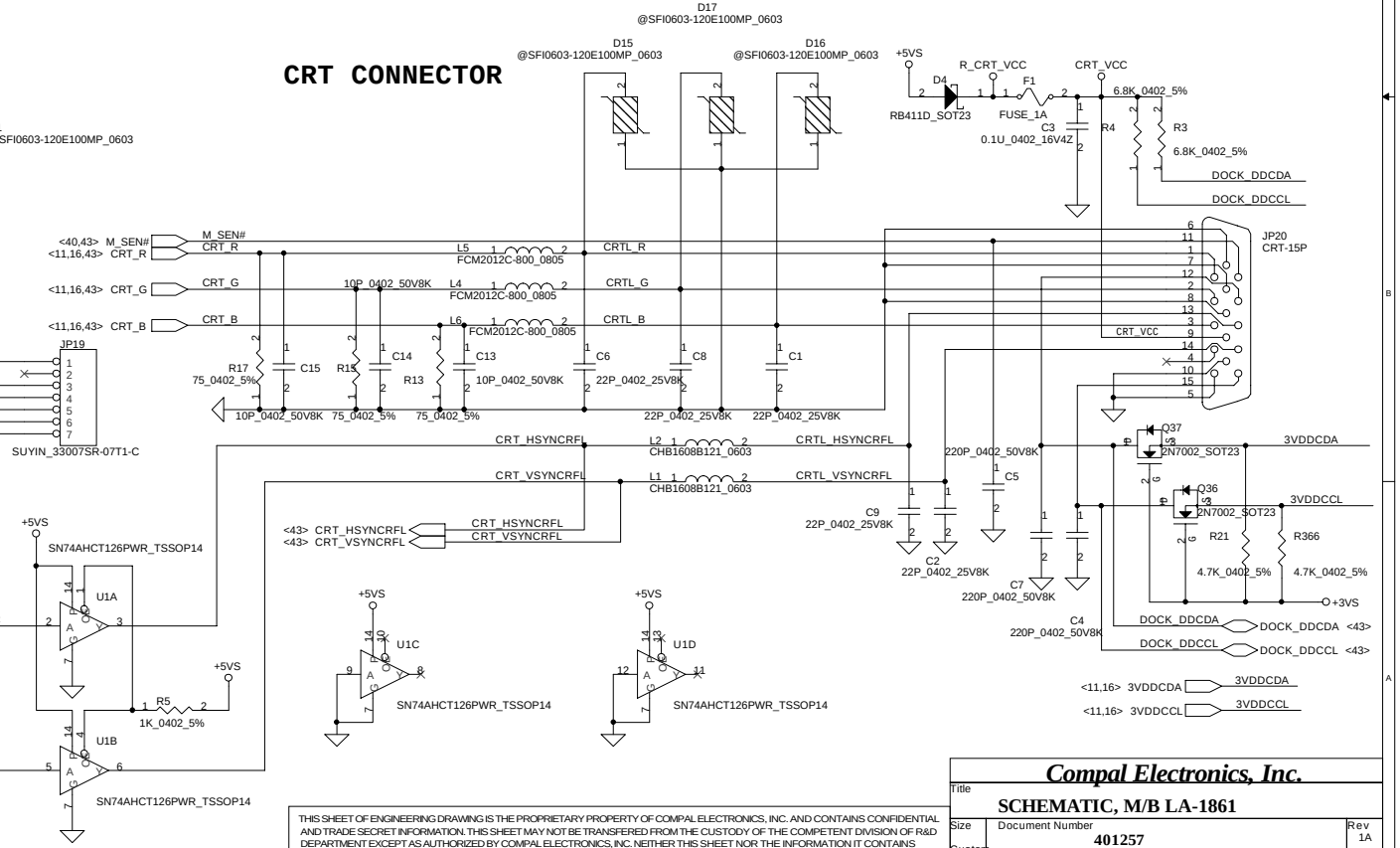
SI2301DS: P CHANNEL
VGS: -4.5V, RDS: 130 mOHM
VGS: -2.5V, RDS: 190mOHM
Id(MAX): 2.3A
VGS(MAX): +-8V

SI2302DS: N CHANNEL
VGS: 4.5V, RDS: 85 mOHM
VGS: 2.5V, RDS: 115mOHM
Id(MAX): 2.8A
VGS(MAX): +-8V

TV_OUT CONNECTOR



CRT CONNECTOR



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Layout note:
Trace length of PCI_CLK_R + PCI_CLK_FB should be less than 200 mils.

U15A

SB200 SB

Part 1 of 3

PULL DOWN FOR S3

Near SB

PLACE CLOSE TO CPU SOCKET

South bridge SB200

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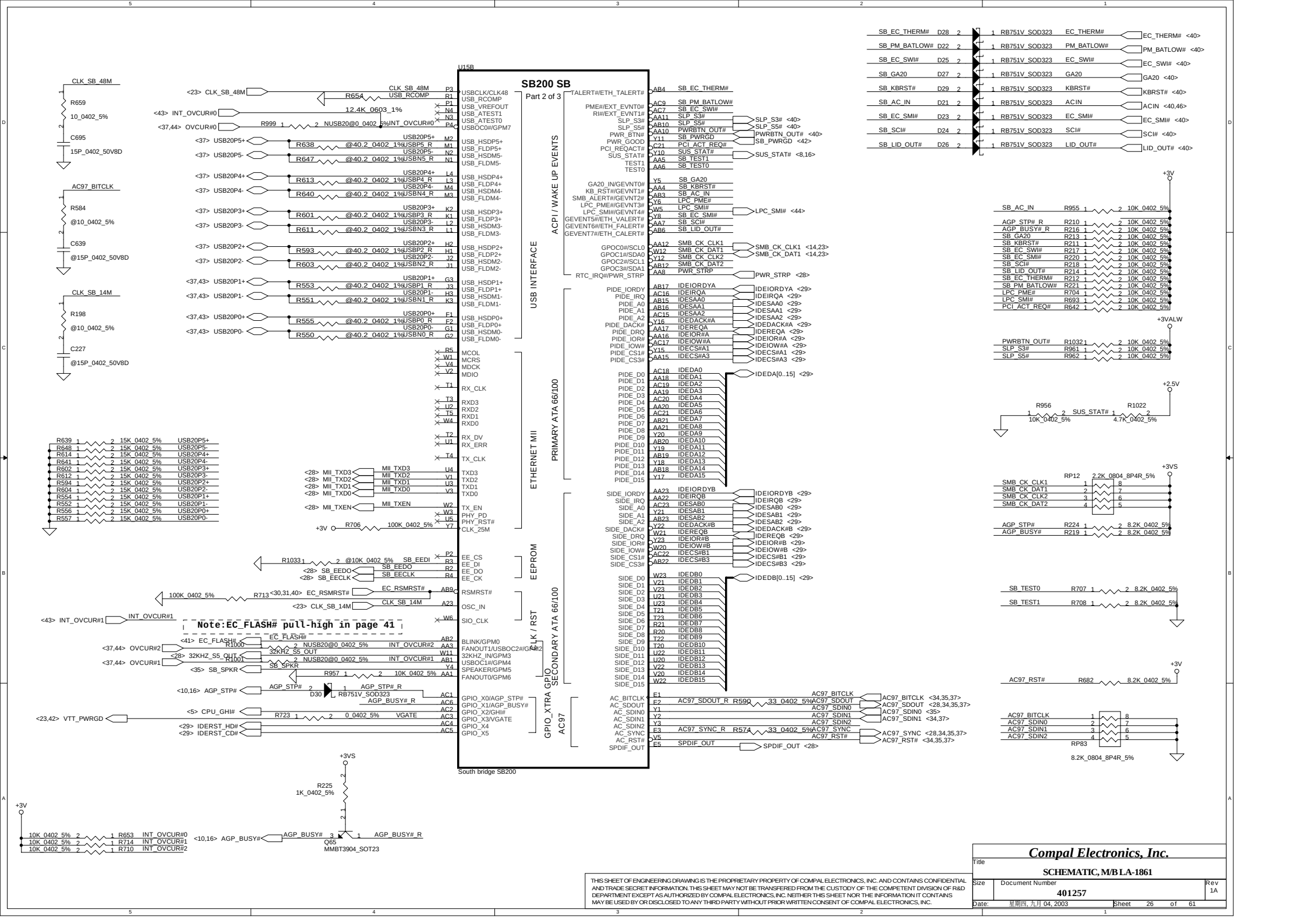
SB200 SB
Part 2 of 3
U15B
South bridge SB200
USB INTERFACE
ACPI / WAKE UP EVENTS
PRIMARY ATA 66/100
ETHERNET MII
EEPROM
CLK / RST
SECONDARY ATA 66/100
GPIO_XTRA GPIO
AC97
Note:EC_FLASH# pull-high in page 41
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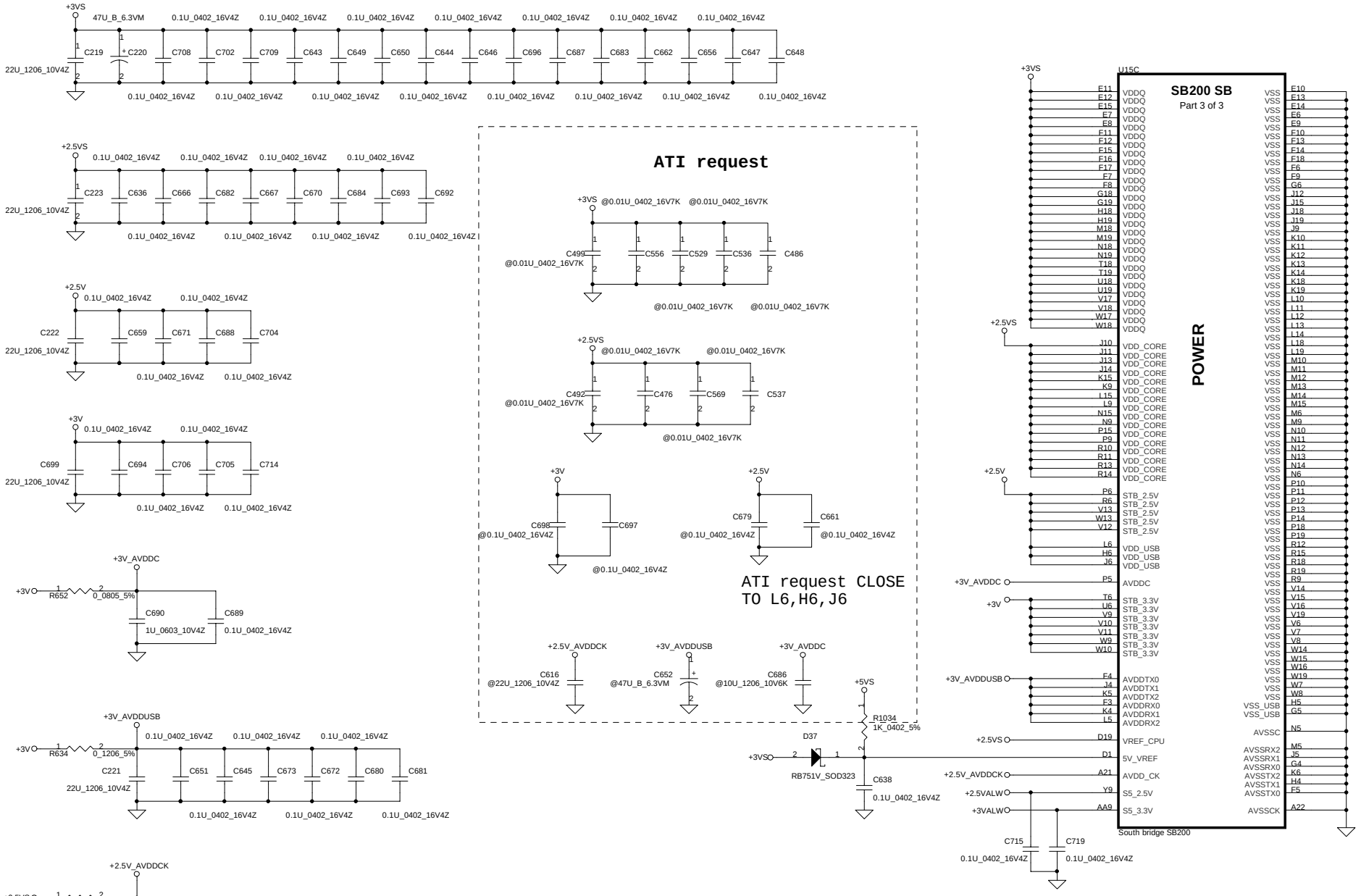

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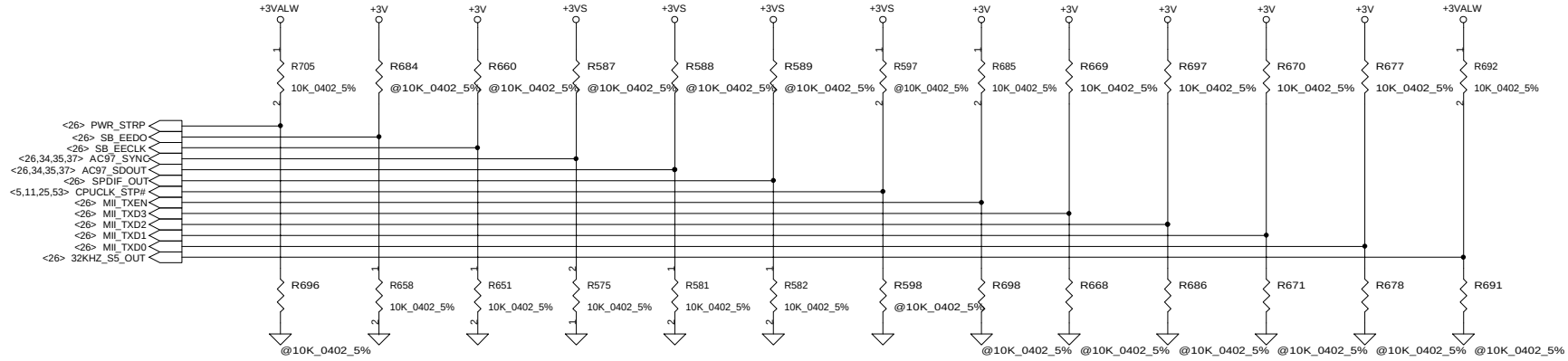
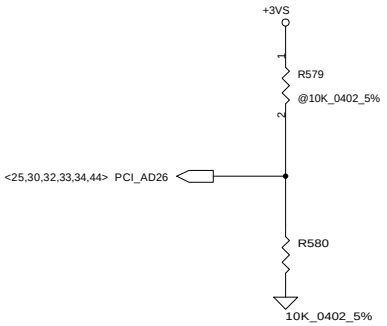


REQUIRED SYSTEM STRAPS

	PWR_STRP	IGN DEBUG EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	SPEEDSTEP CPU_STP#	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS DEFAULT	INIT ACTIVE HIGH	33MHz NB BUS DEFAULT	SIO 24MHz	ENABLE SPEED STEP	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)



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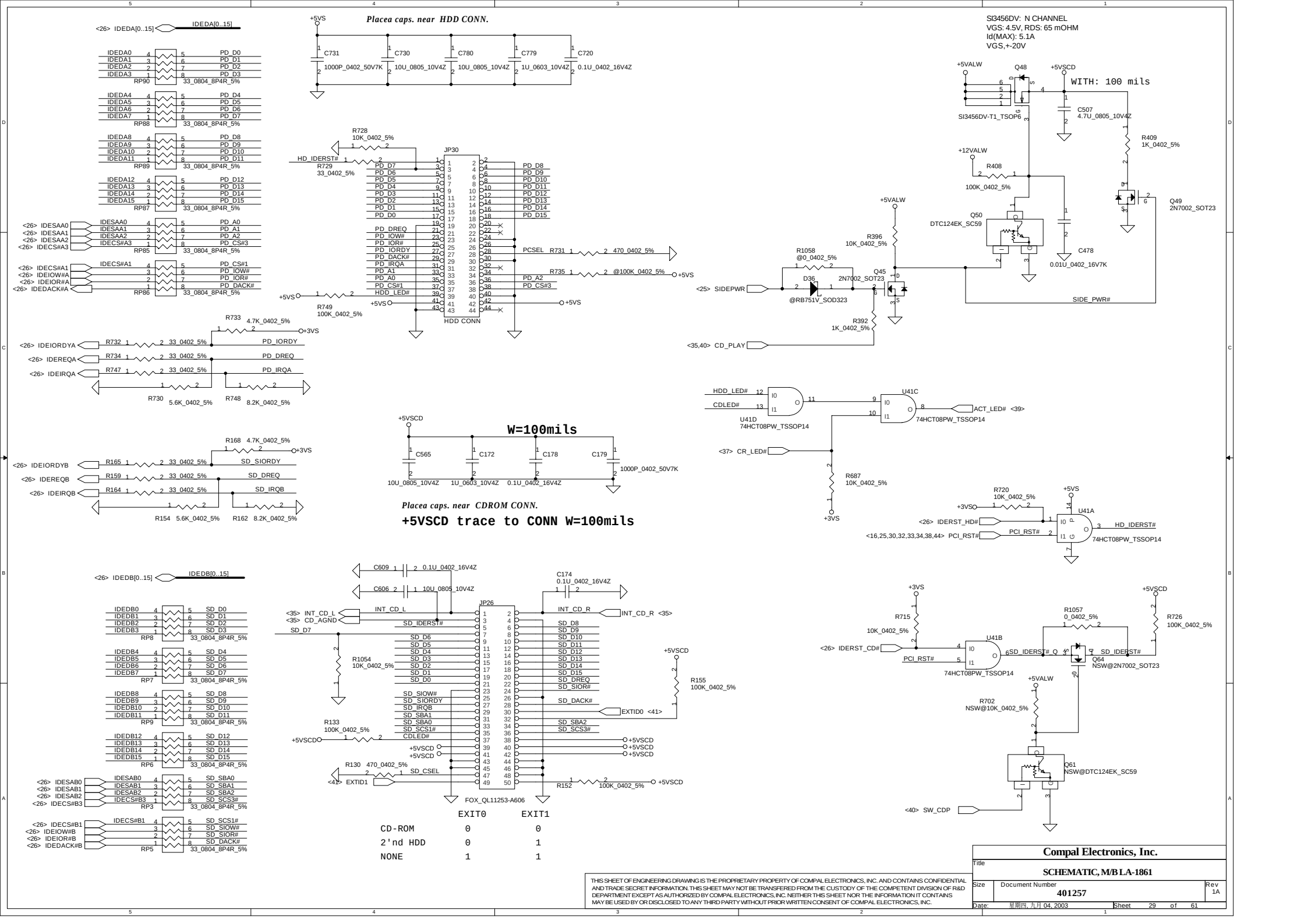
Placea caps. near HDD CONN.
SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+-20V
WITH: 100 mils
W=100mils
Placea caps. near CDROM CONN.
+5VSCD trace to CONN W=100mils
HDD CONN
FOX_QL11253-A606
EXIT0 EXIT1
CD-ROM 0 0
2'nd HDD 0 1
NONE 1 1
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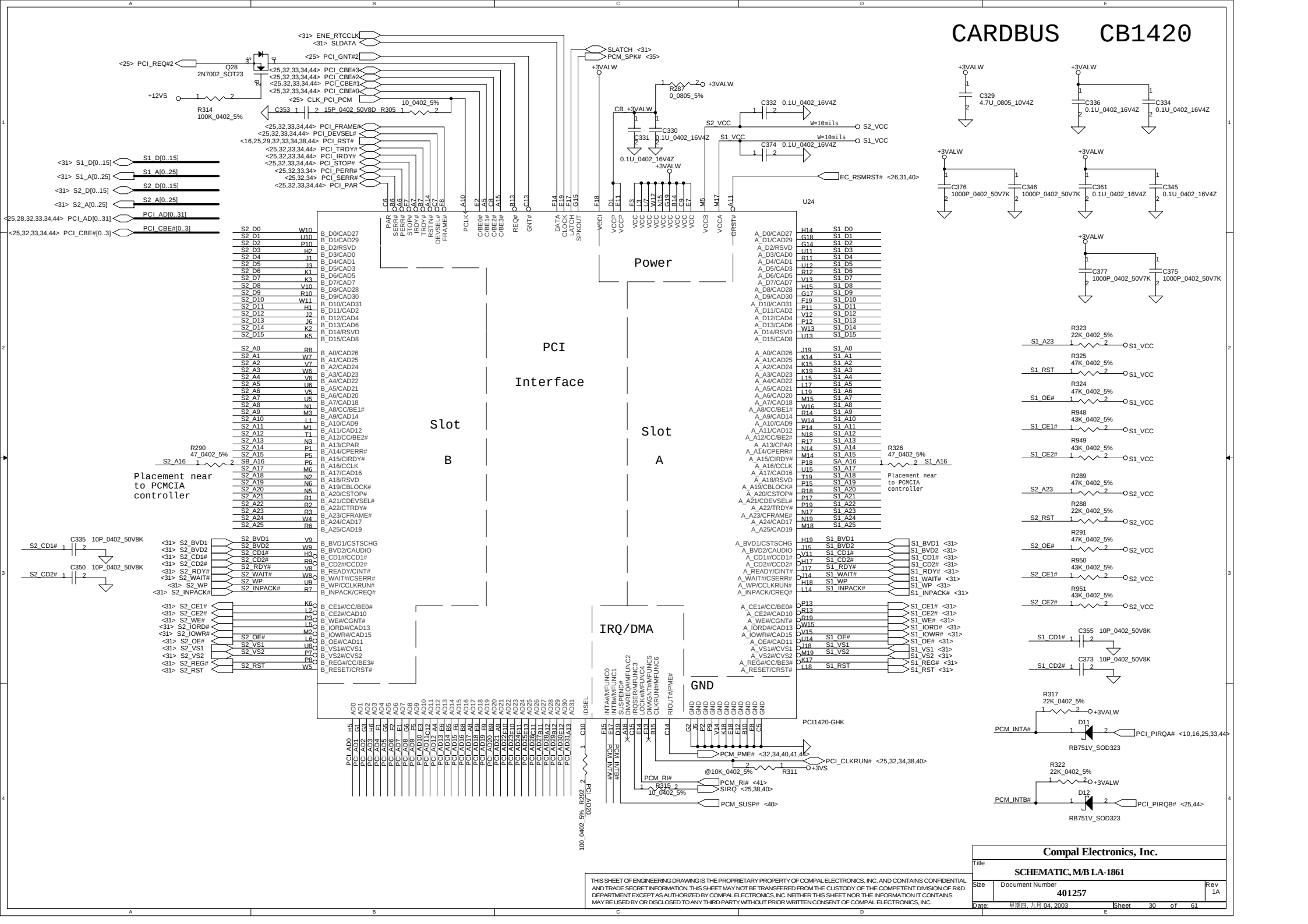
CARDBUS CB1420



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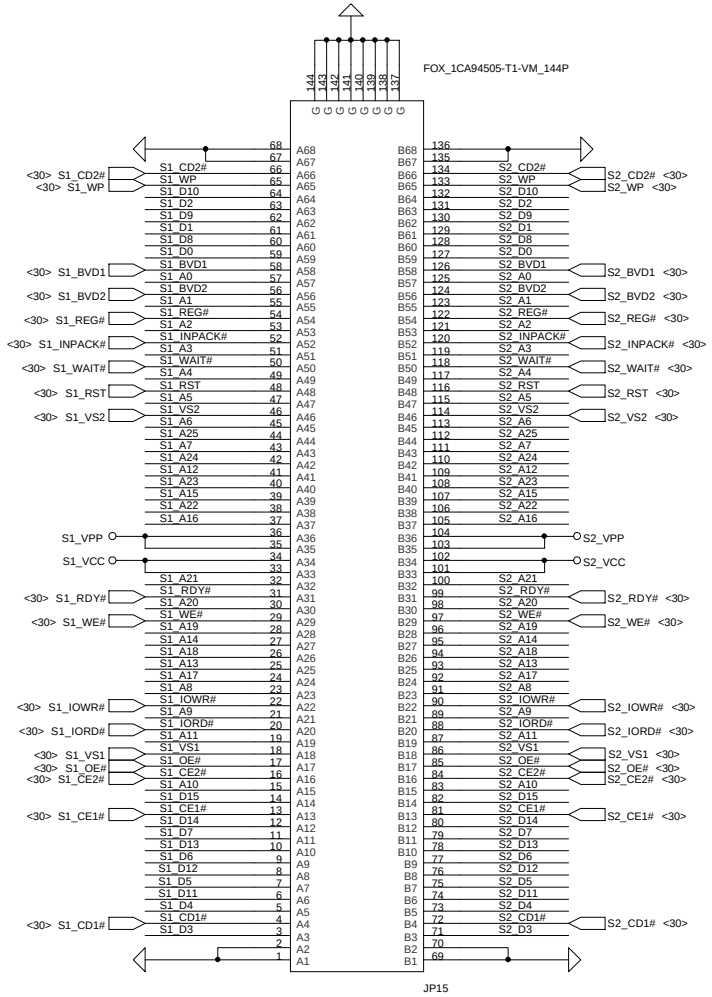
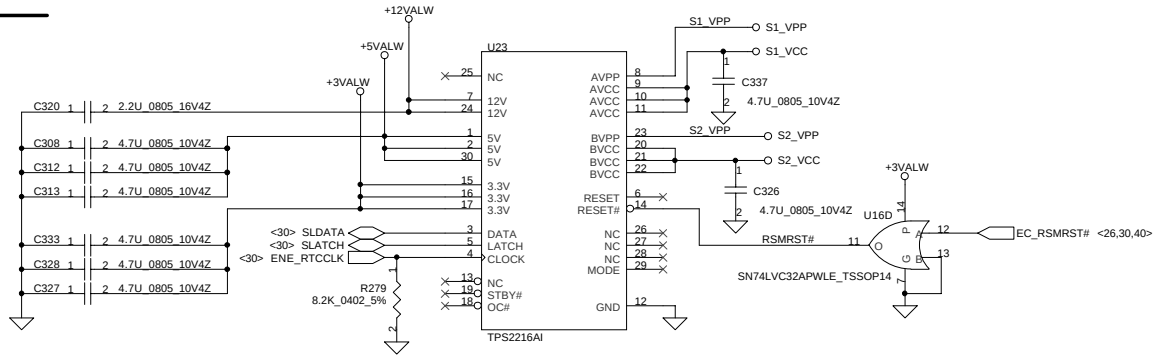
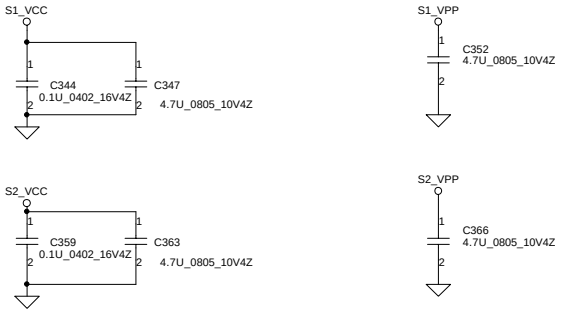
CARDBUS SOCKET

PCMCIA POWER CTRL.







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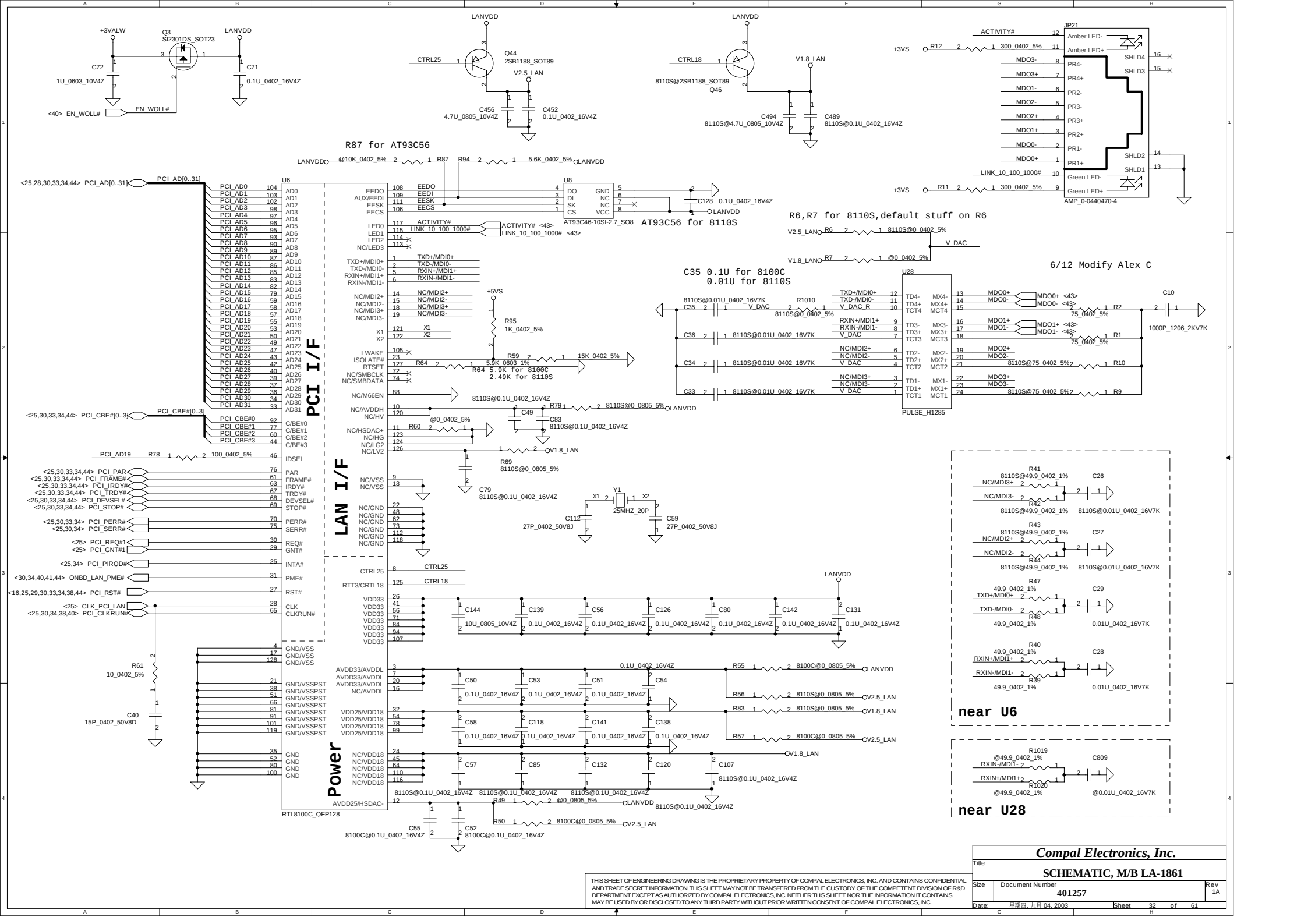

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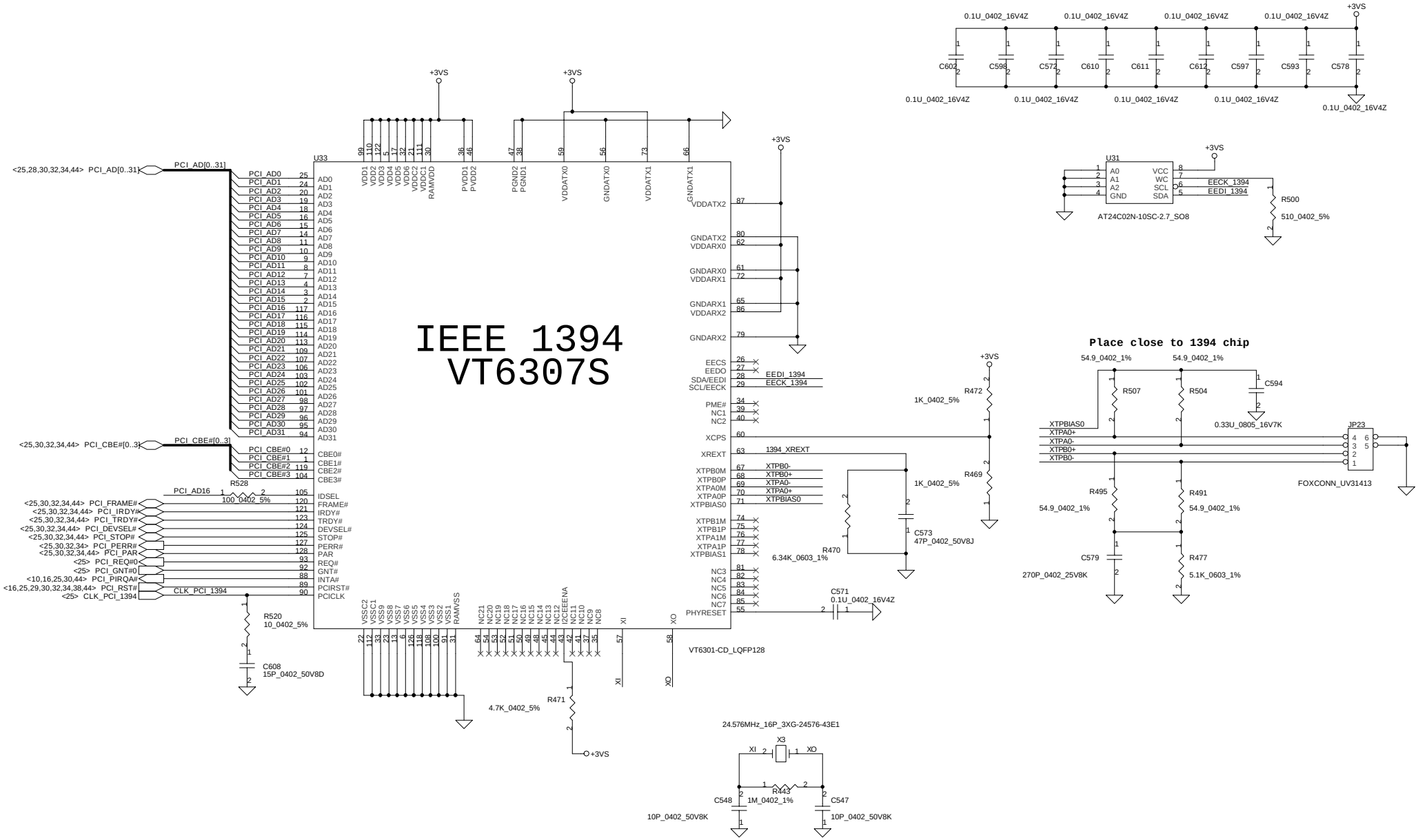
IEEE 1394
VT6307S



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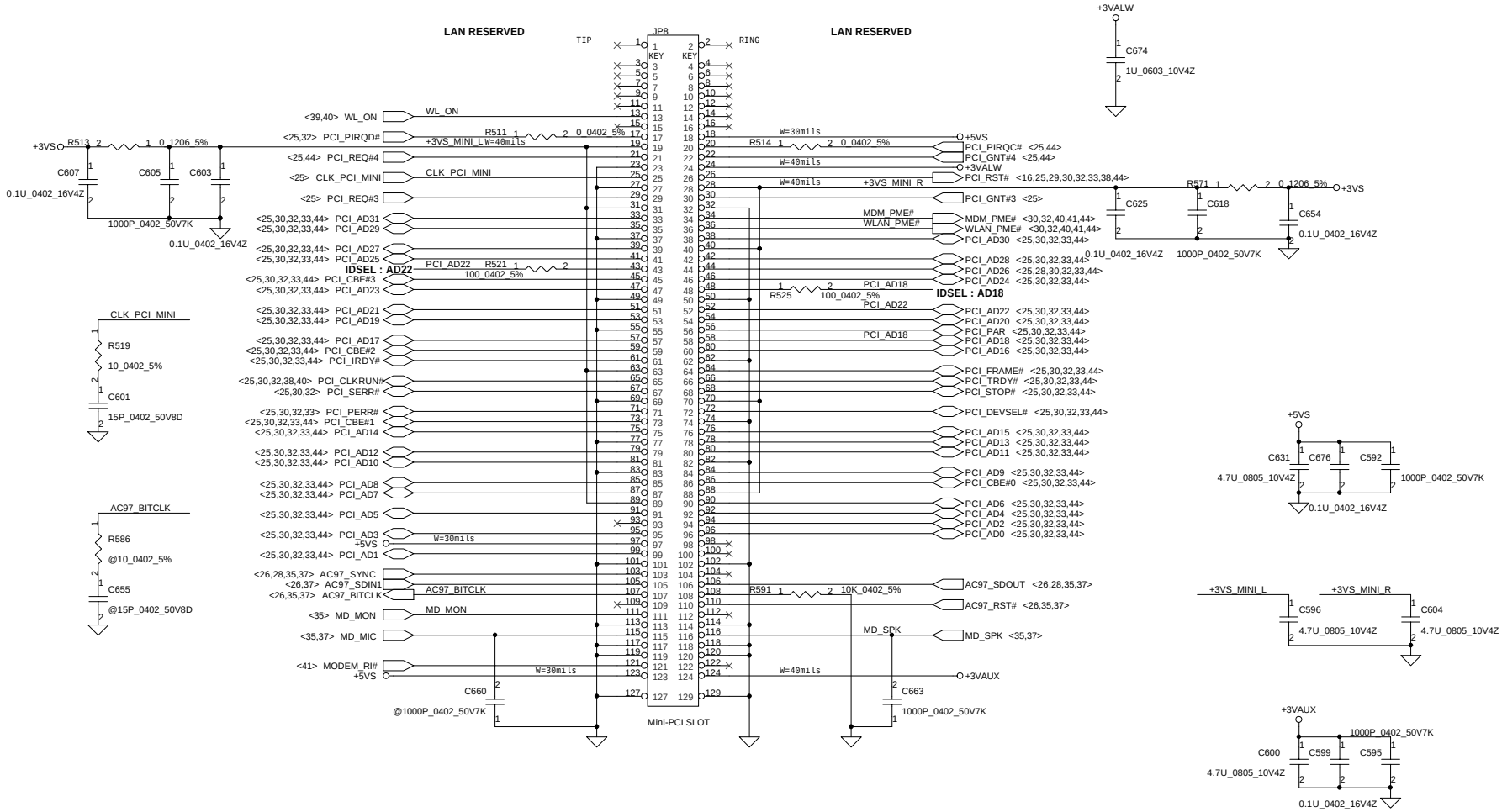

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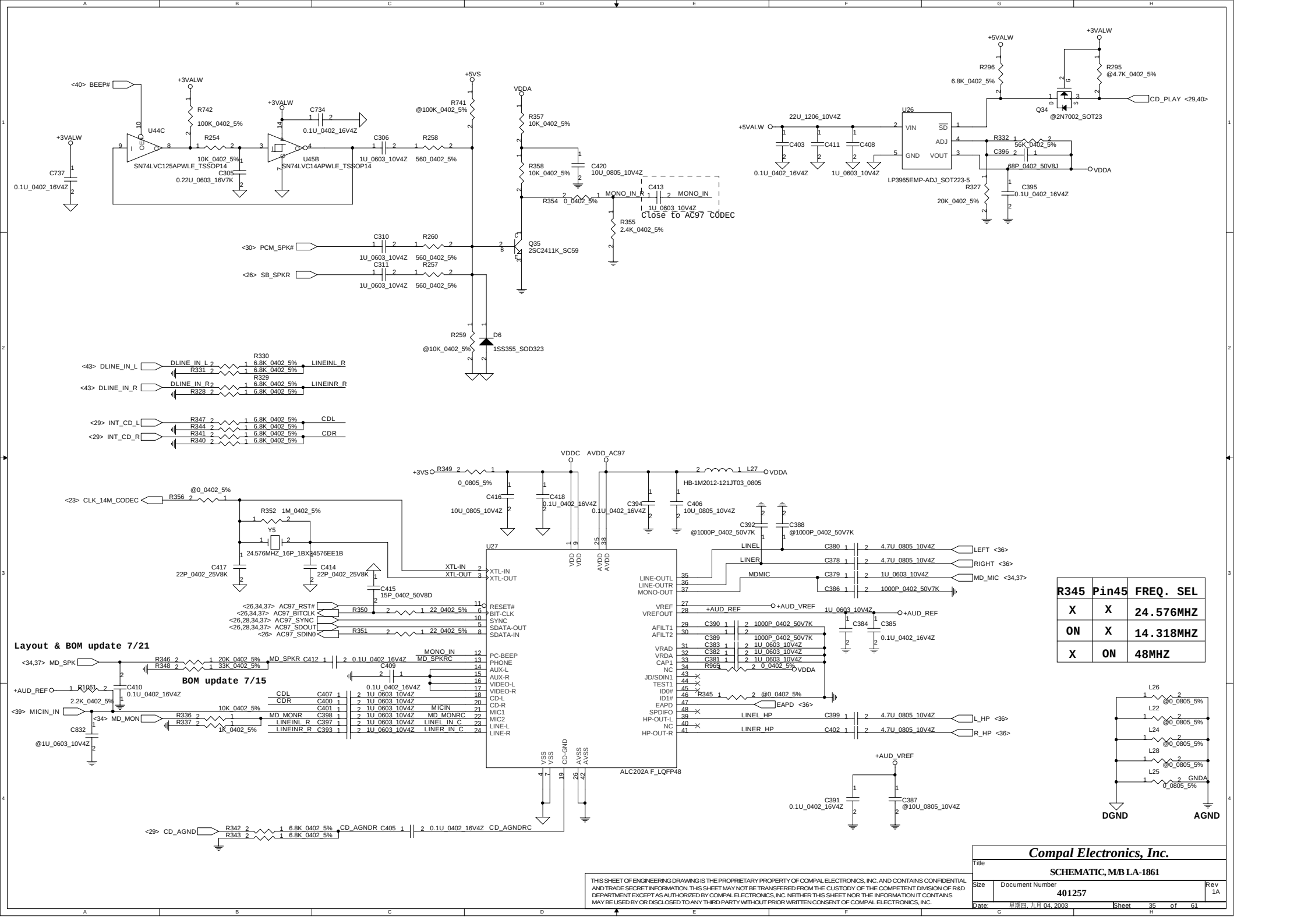

R345	Pin45	FREQ. SEL
X	X	24.576MHZ
ON	X	14.318MHZ
X	ON	48MHZ

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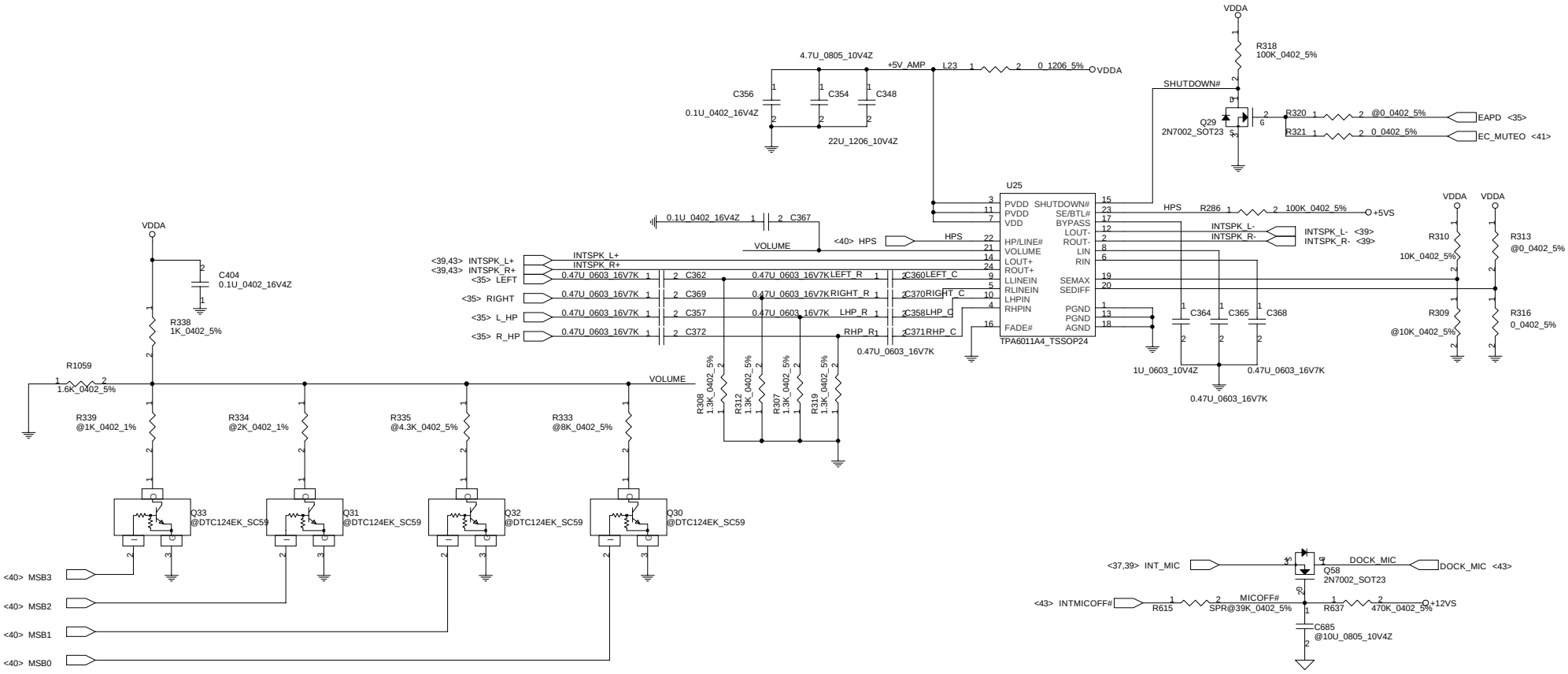

MSB3	MSB2	MSB1	MSB0	Vo	BTL (dB)	SE (dB)
0	0	0	0	0		
0	0	0	1	4.7225	20	14
0	0	1	0	4.47	20	14
0	0	1	1	4.34	20	14
0	1	0	0	4.0485	20	14
0	1	0	1	3.86	20	14
0	1	1	0	3.719	20	14
0	1	1	1	3.56		
1	0	0	0	3.4	14	8
1	0	0	1	3.272	12	6
1	0	1	0	3.1659	10	4
1	0	1	1	3.05	8	2
1	1	0	0	2.938	6	0
1	1	0	1	2.84		
1	1	1	0	2.76		
1	1	1	1	2.67		

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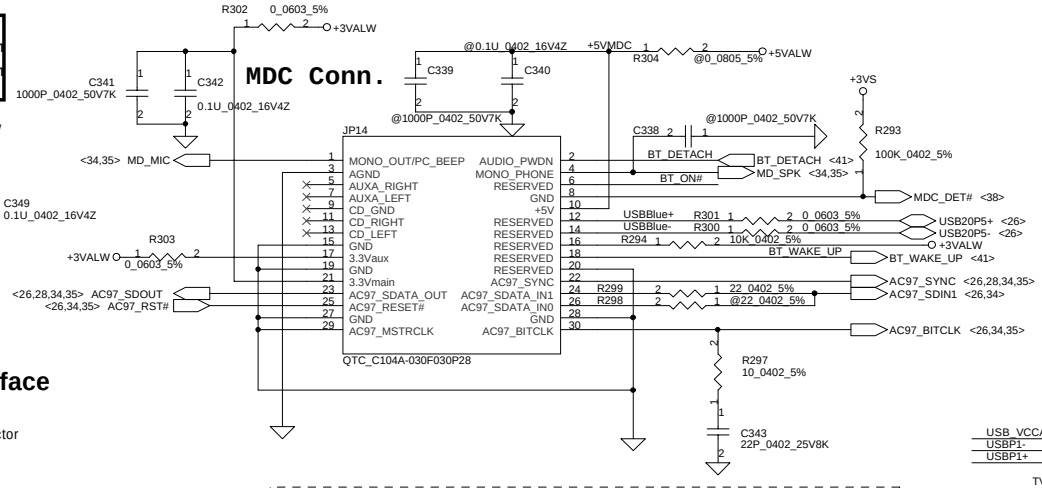
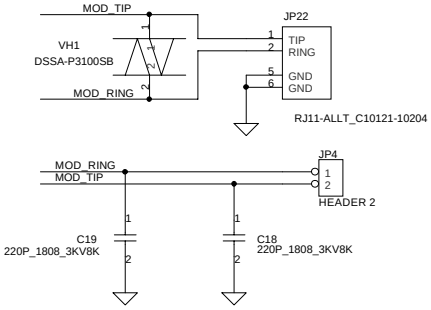
MDC Note
Pin 1 is NC for Pctel and connexant MDC modem
Pin 2 is NC for Pctel and connexant MDC modem

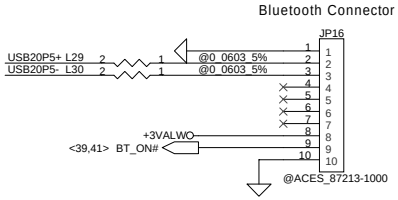
MDC Conn.

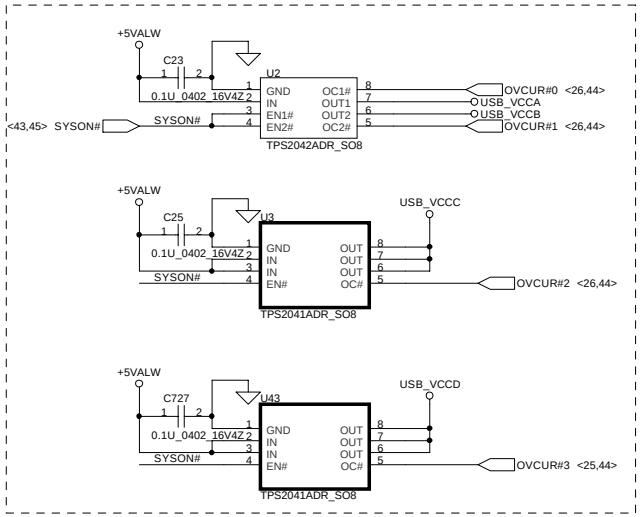


RJ11 CONN.

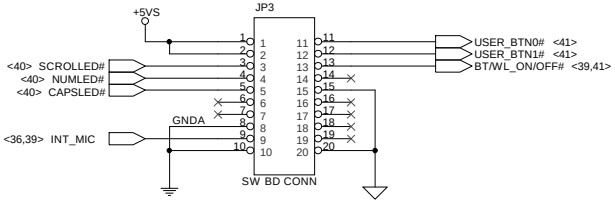


BlueTooth Interface

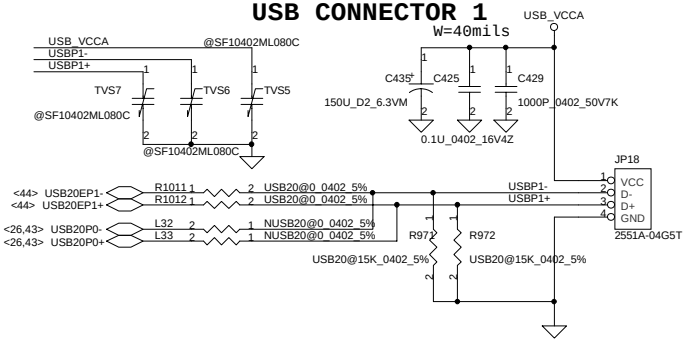




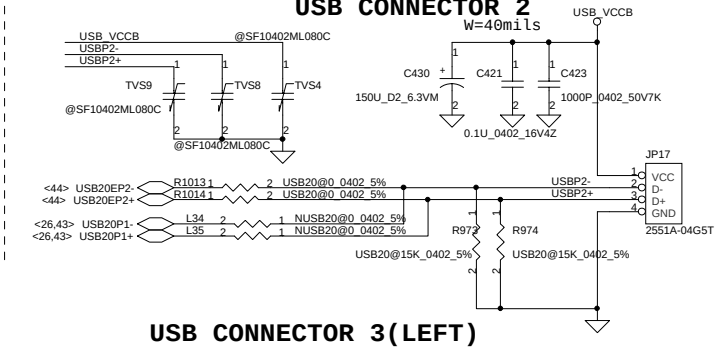
SWITCH BOARD CONN.



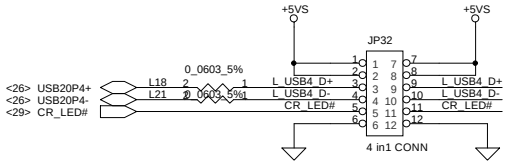
USB CONNECTOR 1



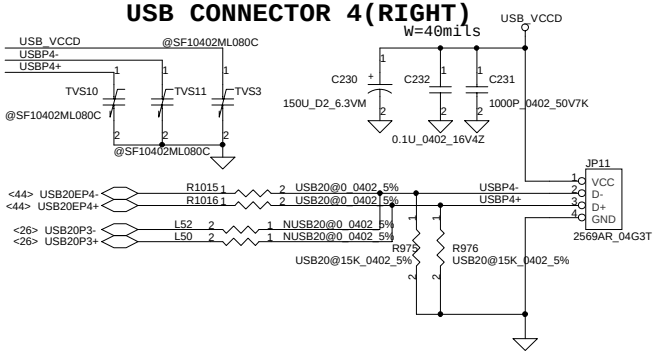
USB CONNECTOR 2



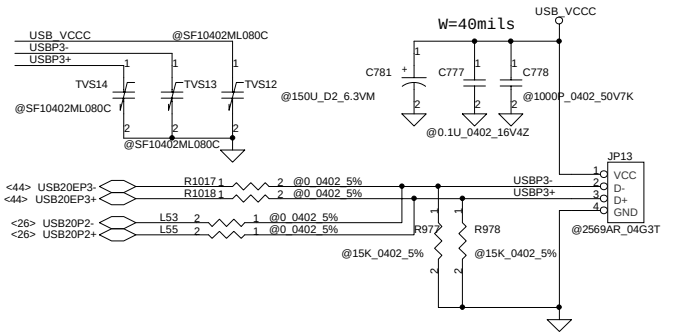
5 IN 1 CONN



USB CONNECTOR 4(RIGHT)



USB CONNECTOR 3(LEFT)



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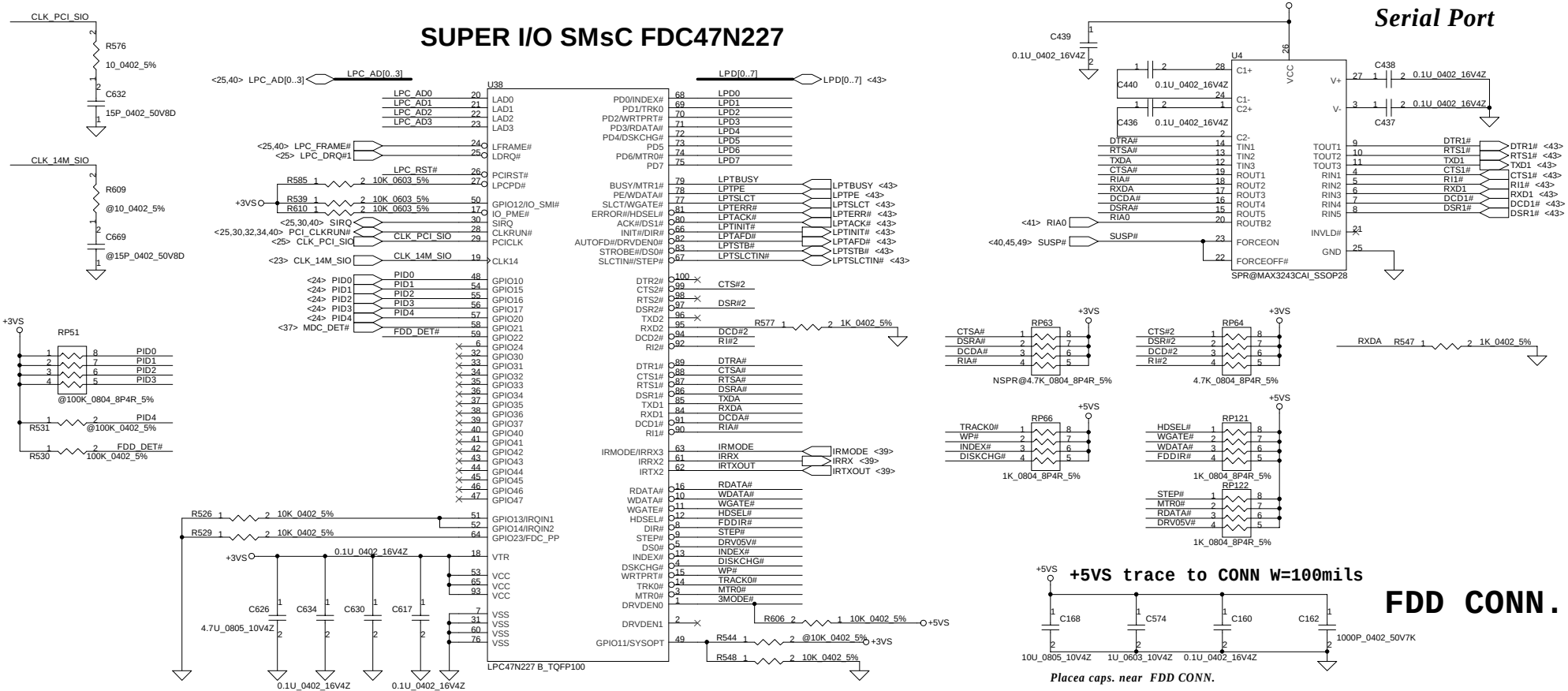
SUPER I/O SMsC FDC47N227



Base I/O Address

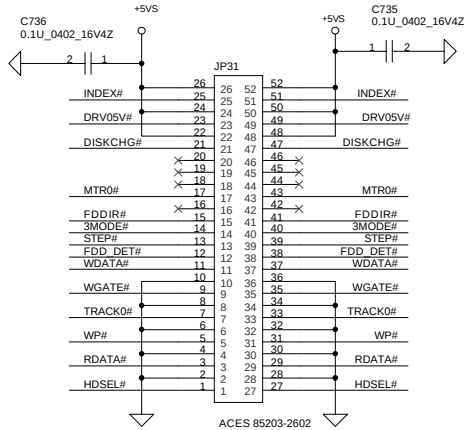
0 = 02Eh

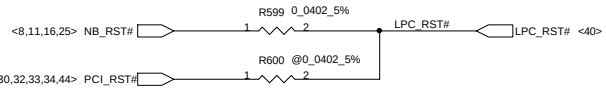
*** 1 = 04Eh**

Serial Port

FDD CONN.

Placea caps. near FDD CONN.





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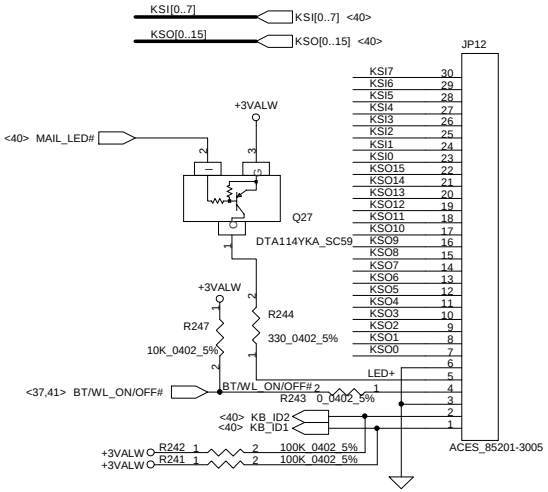
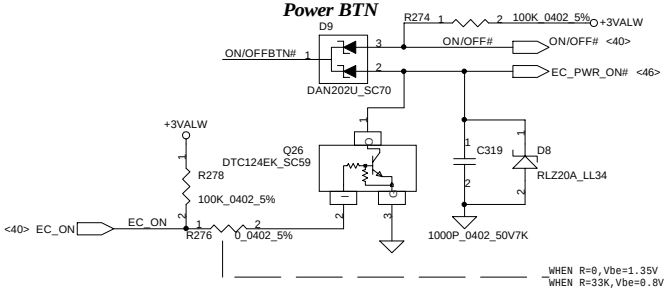
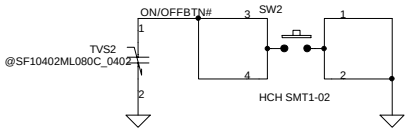
INT_KBD CONN.

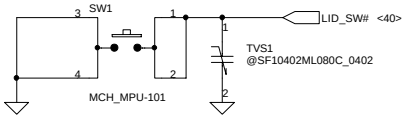


NEED CLOSEST JP18 ADD BY EMI REQUEST

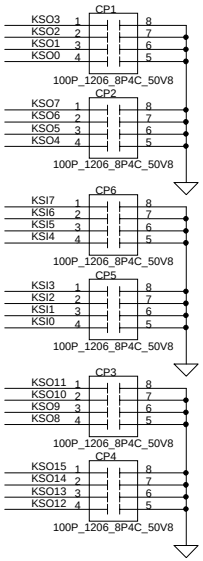
Power BTN

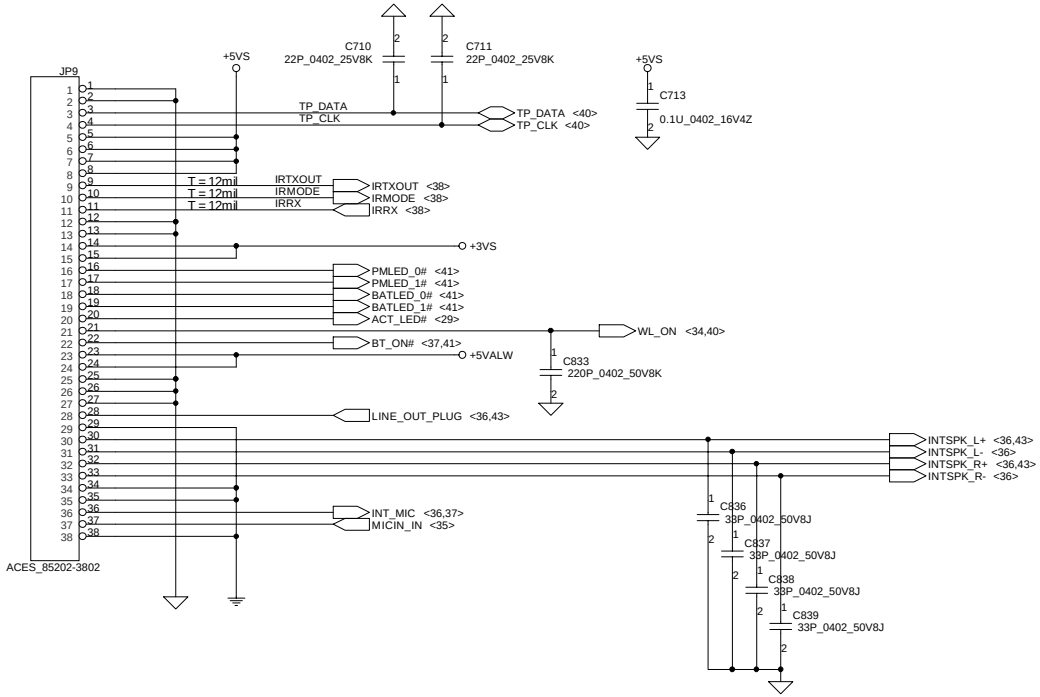






Touch Pad & Status LED Conn.





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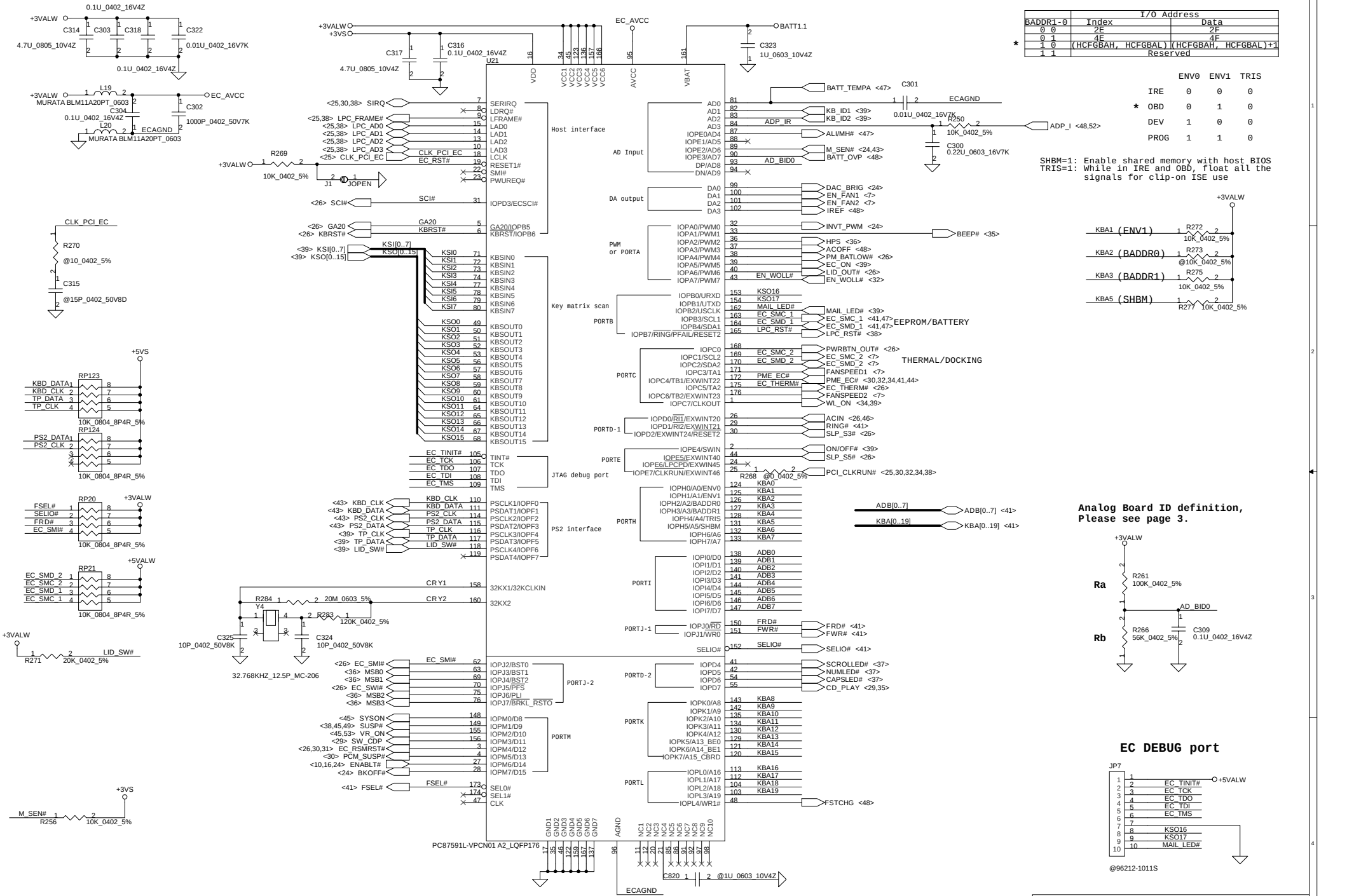

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
* 1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

	ENV0	ENV1	TRIS
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use

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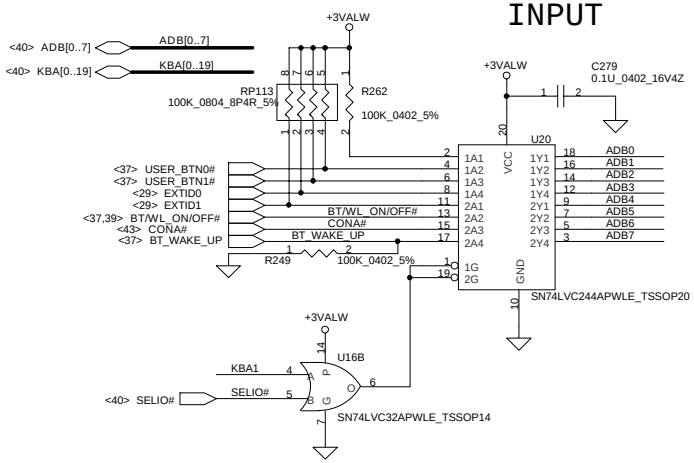
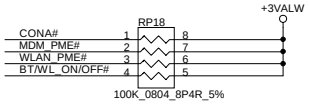
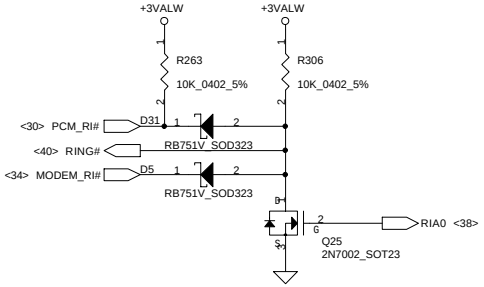
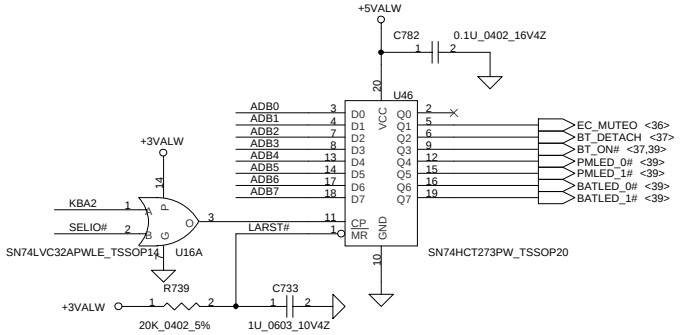
INPUT

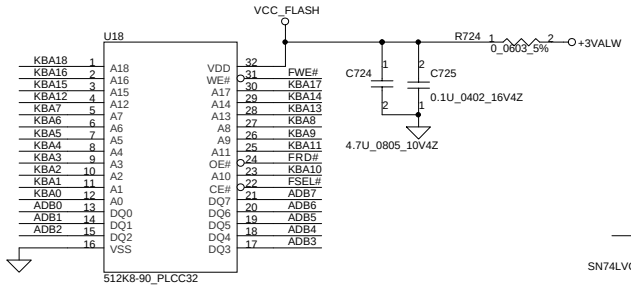


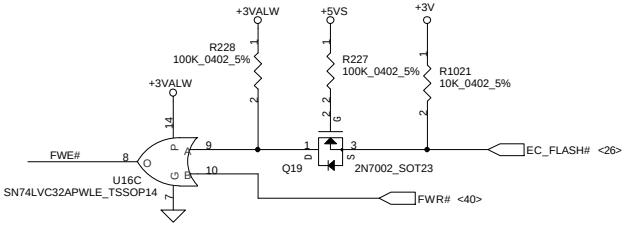


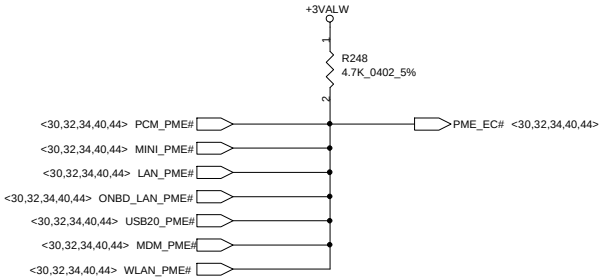


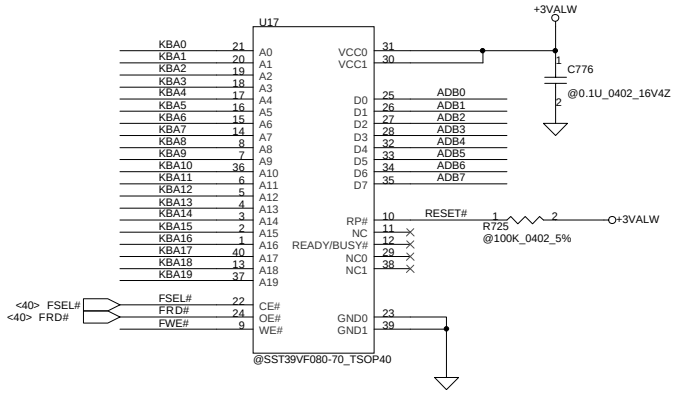
OUTPUT

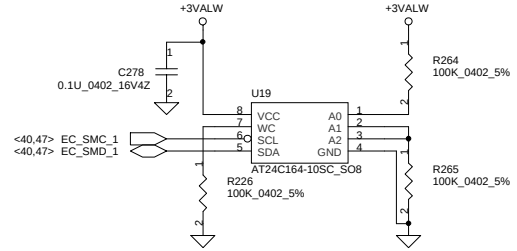












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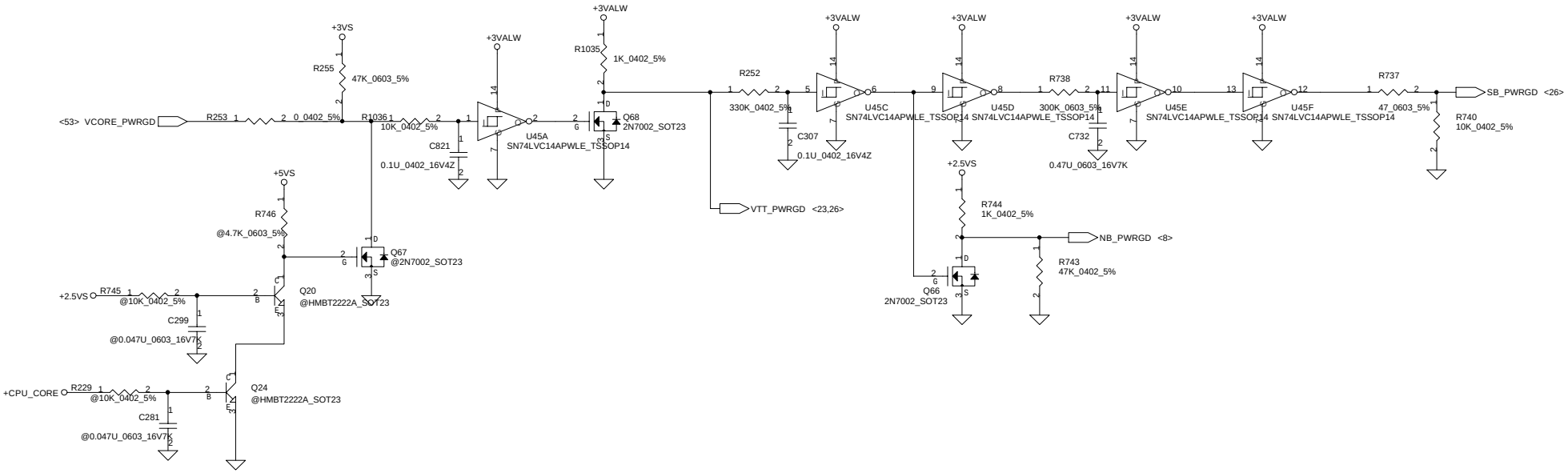

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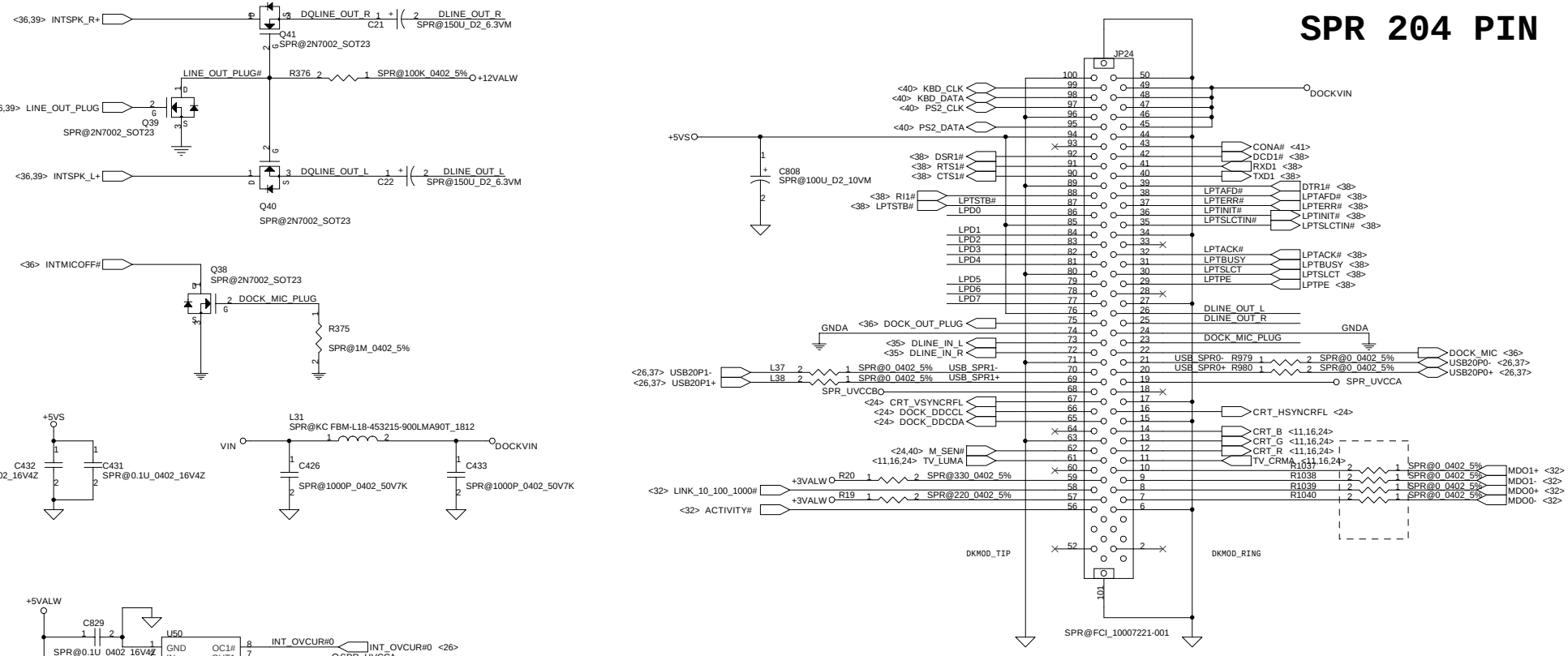
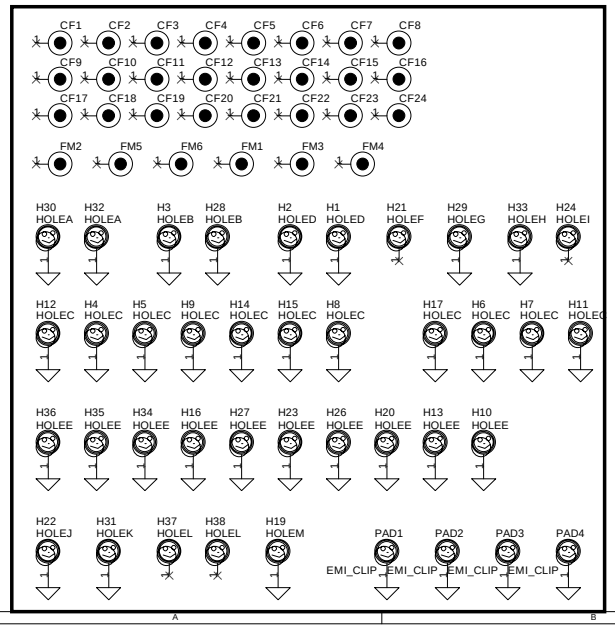
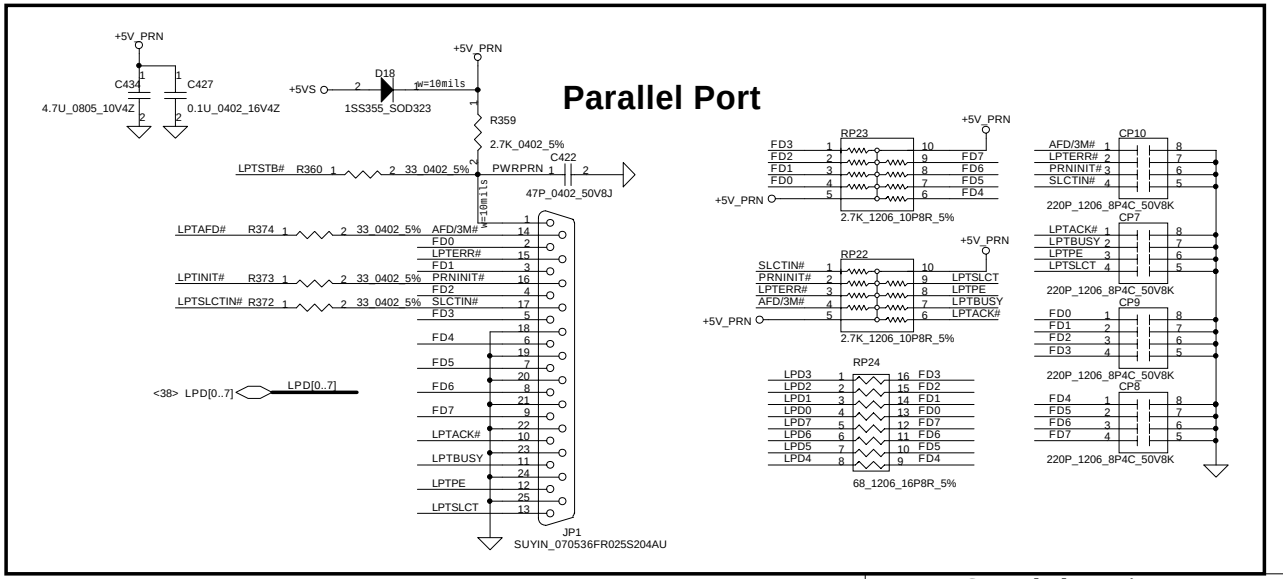
SPR 204 PIN







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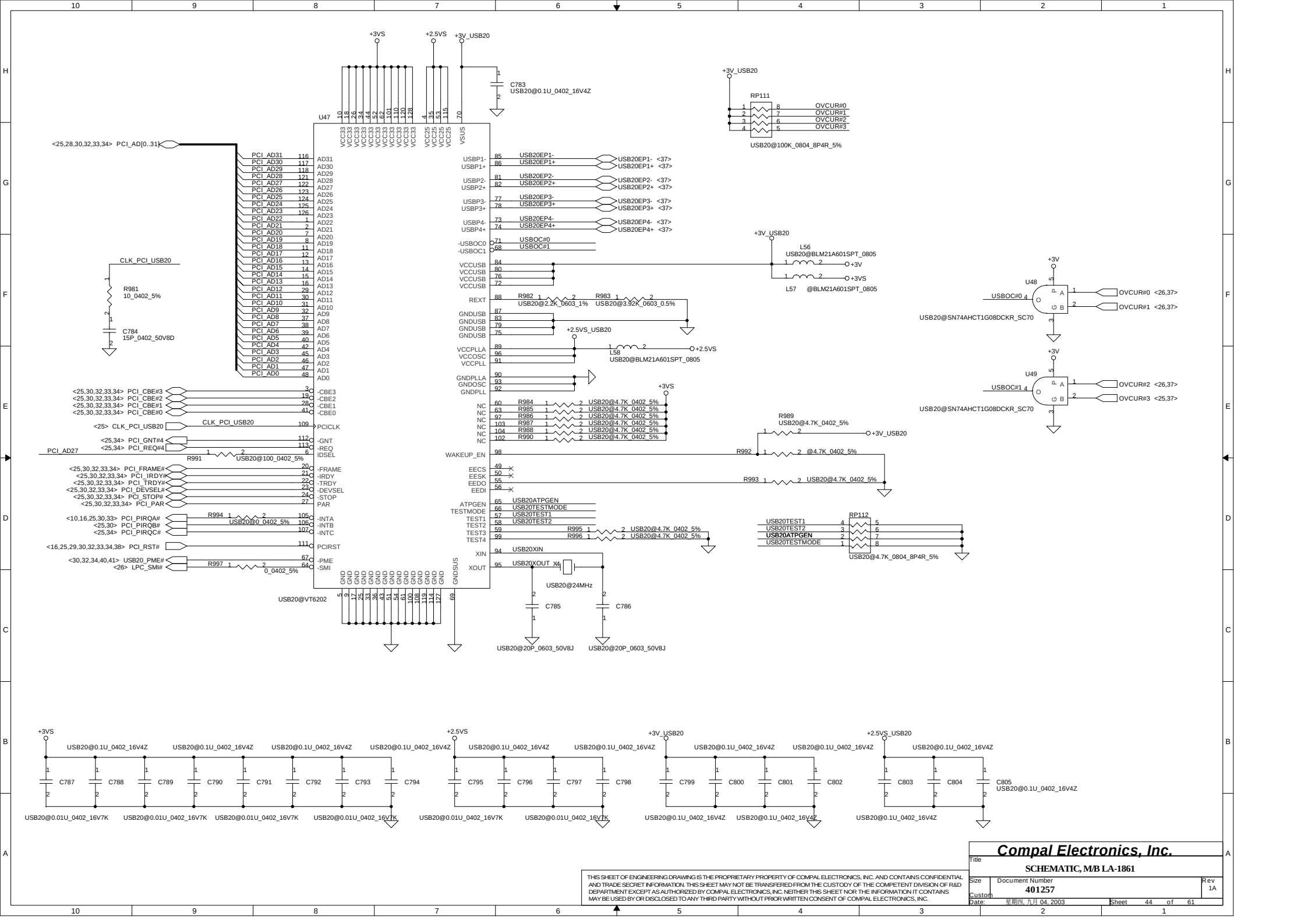

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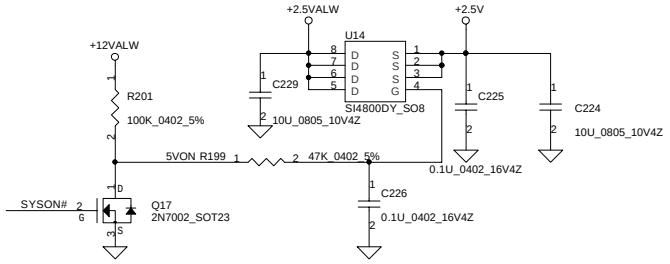
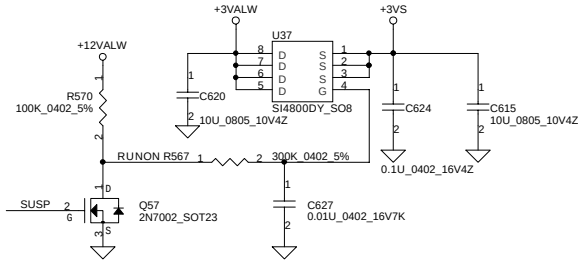
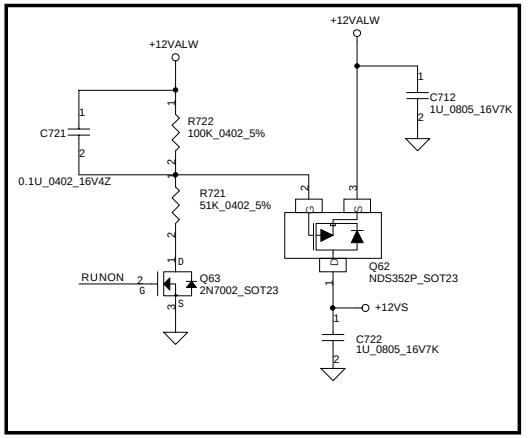
+2.5VALW to +2.5V Transfer



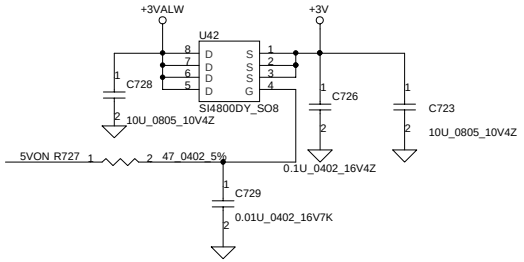
+3VALW to +3VS Transfer



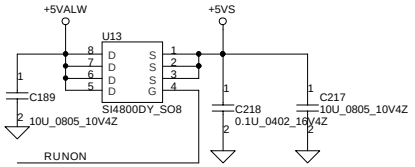
+12VALW TO +12VS Transfer



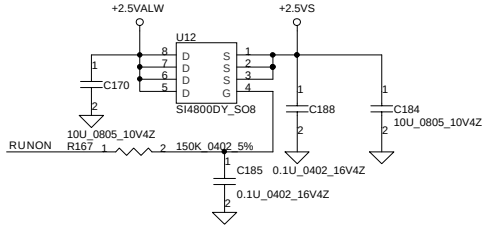
+3VALW to +3V Transfer

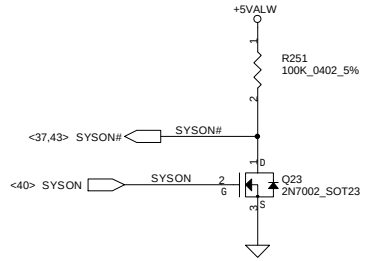


+5VALW to +5VS Transfer

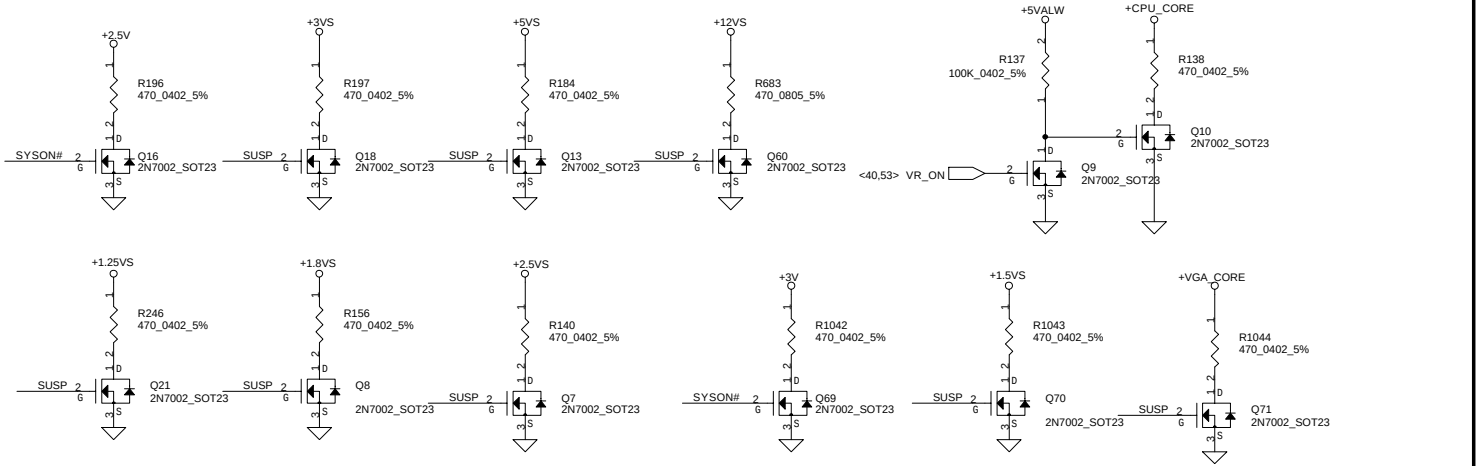


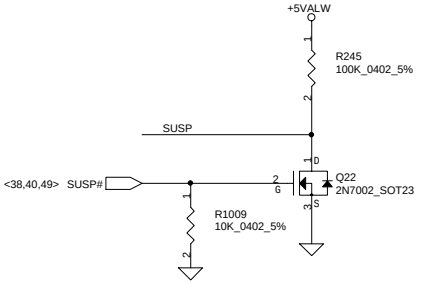
+2.5V to +2.5VS Transfer





Discharge circuit





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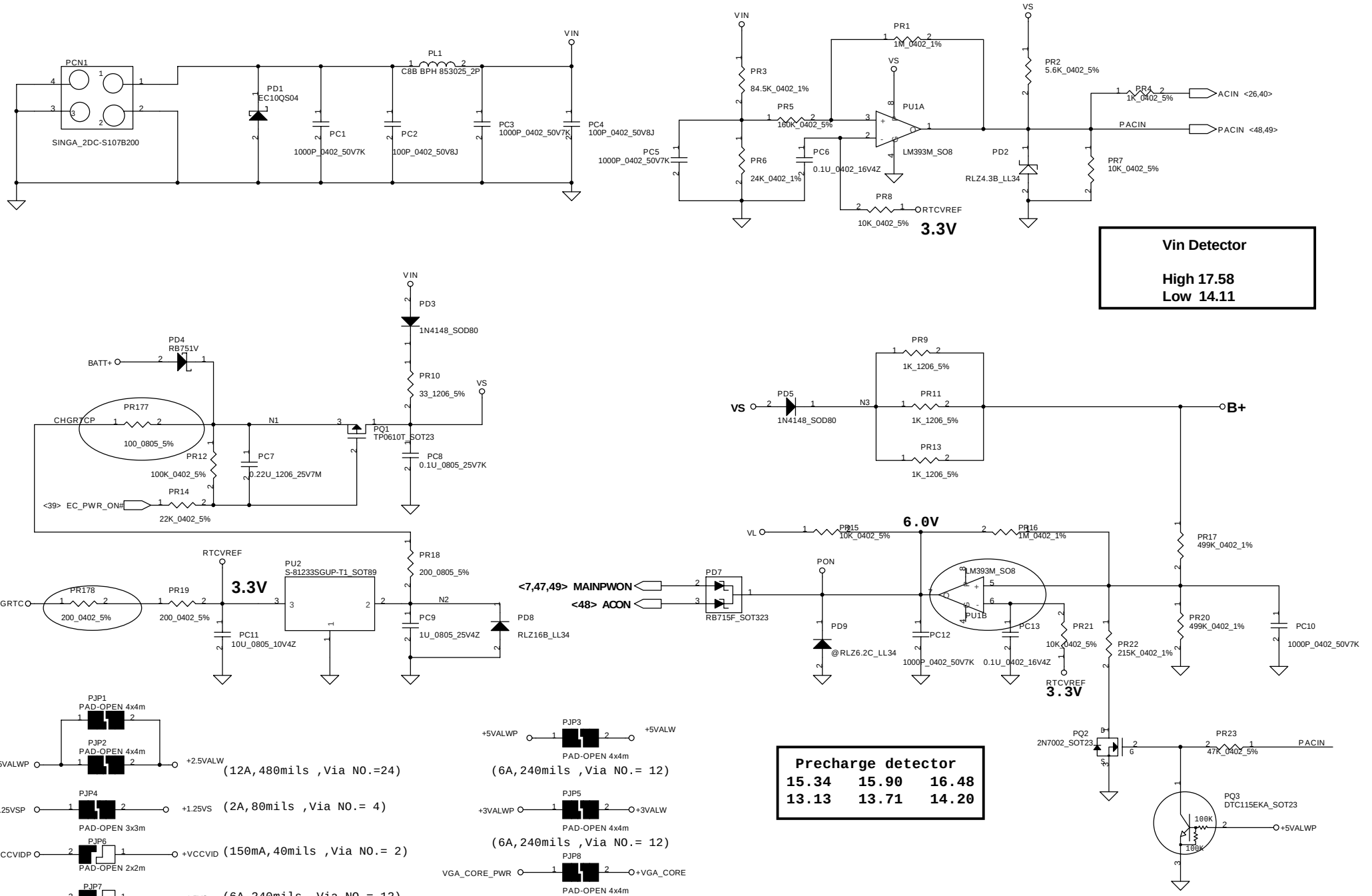

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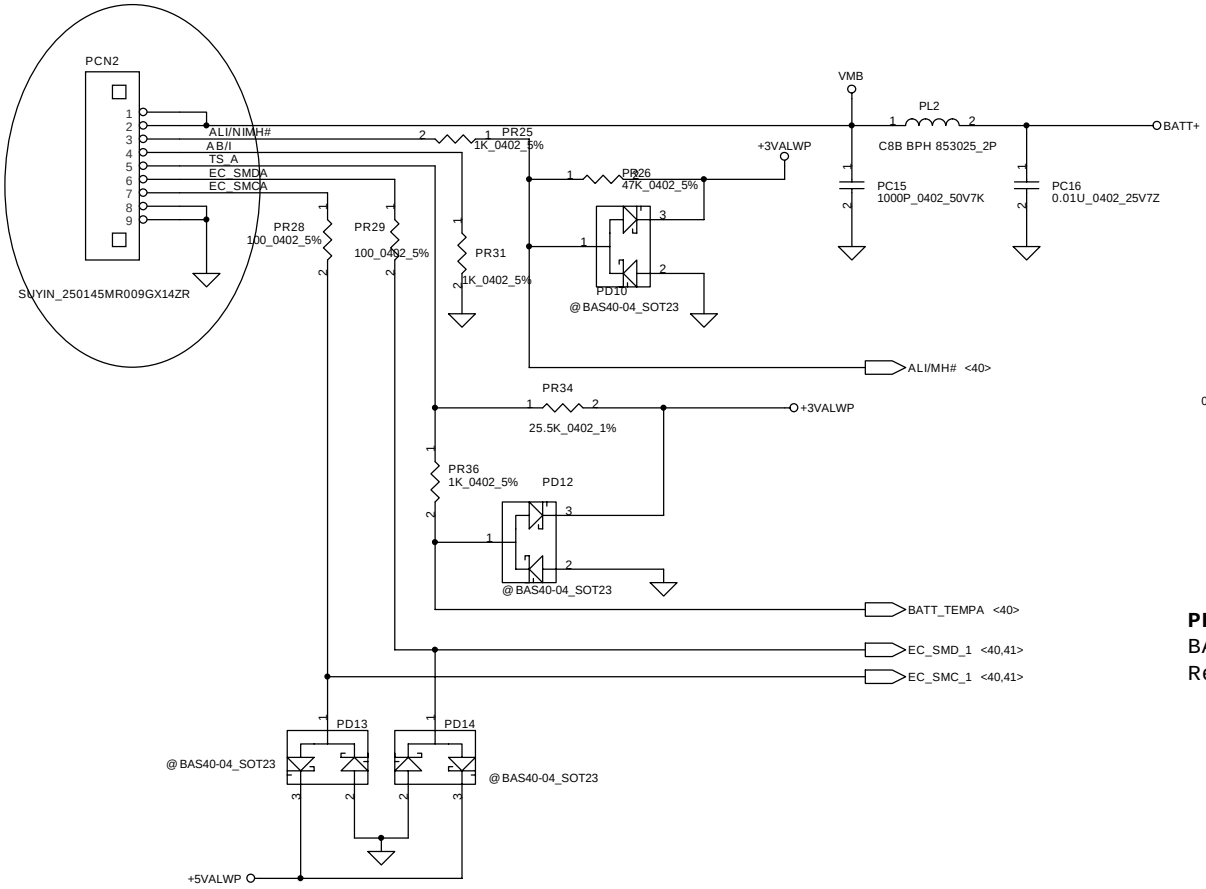
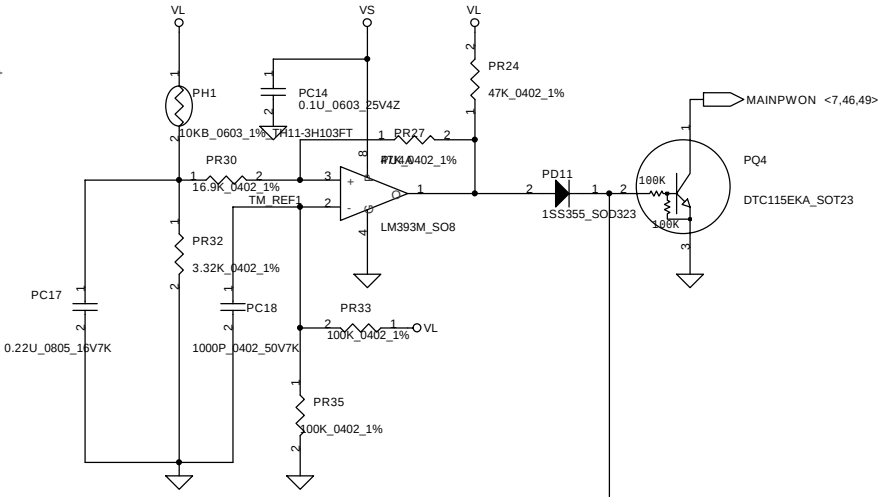
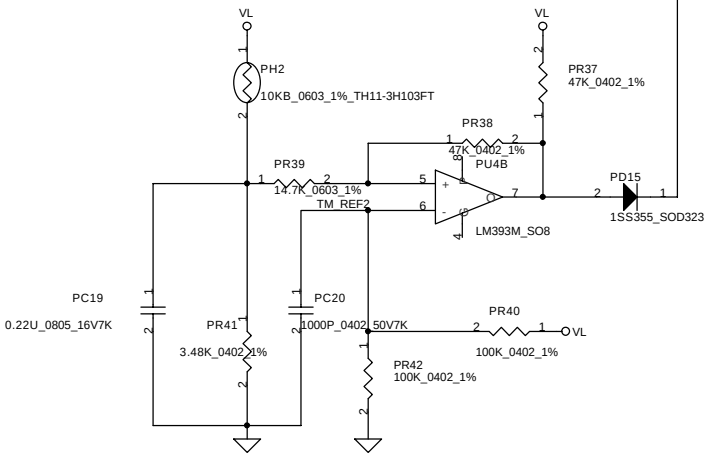
CHANGE CONNECTER



PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



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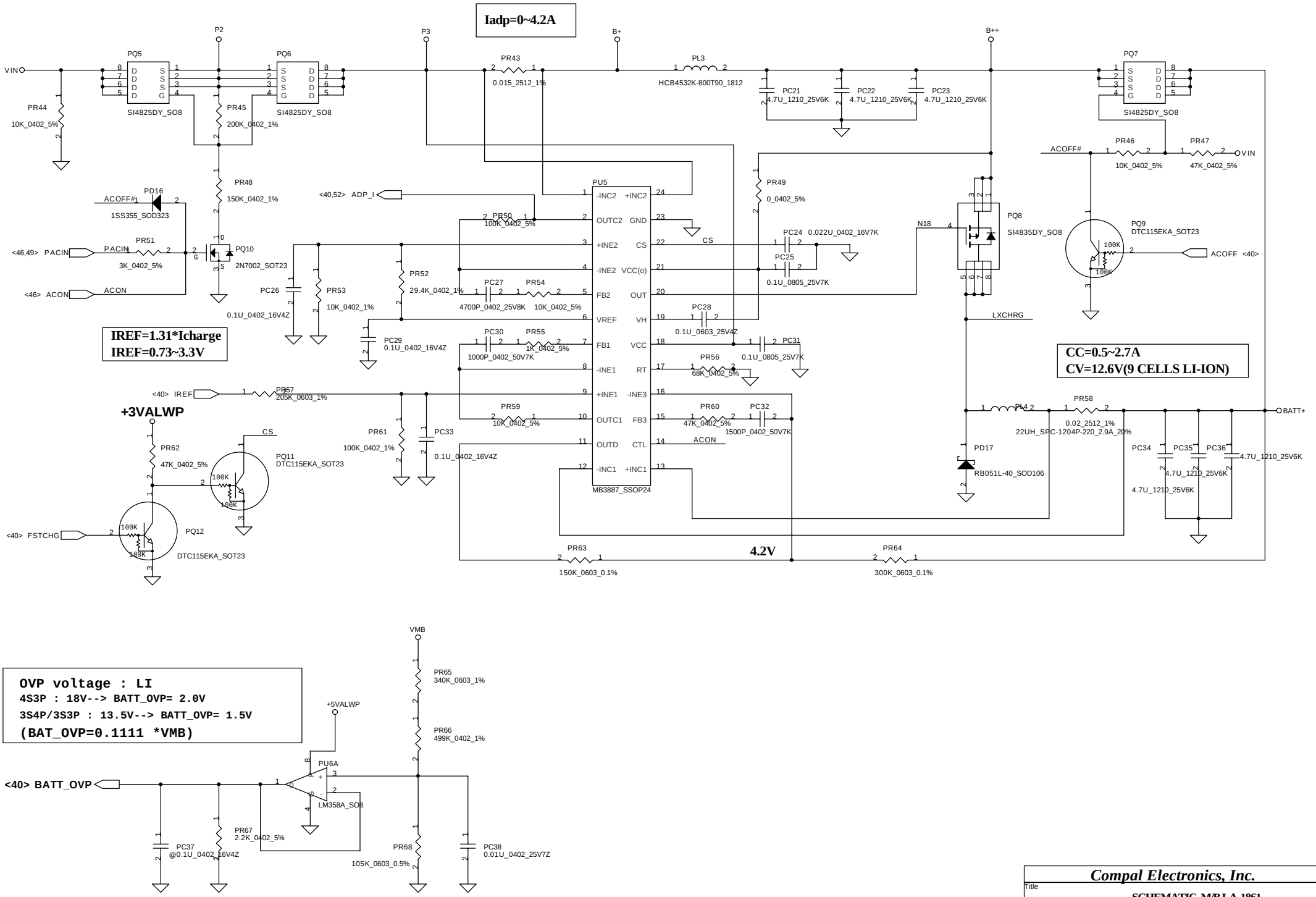

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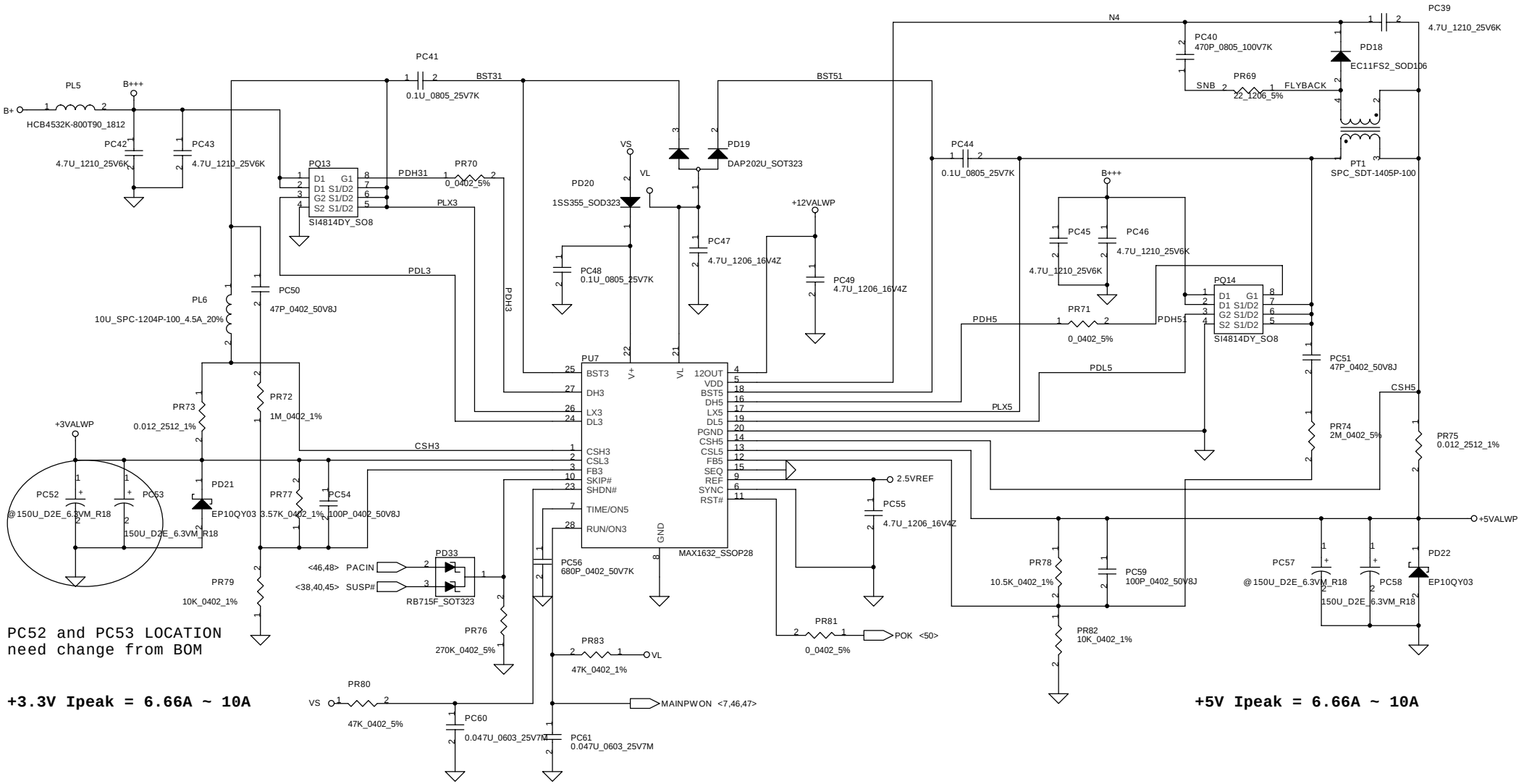

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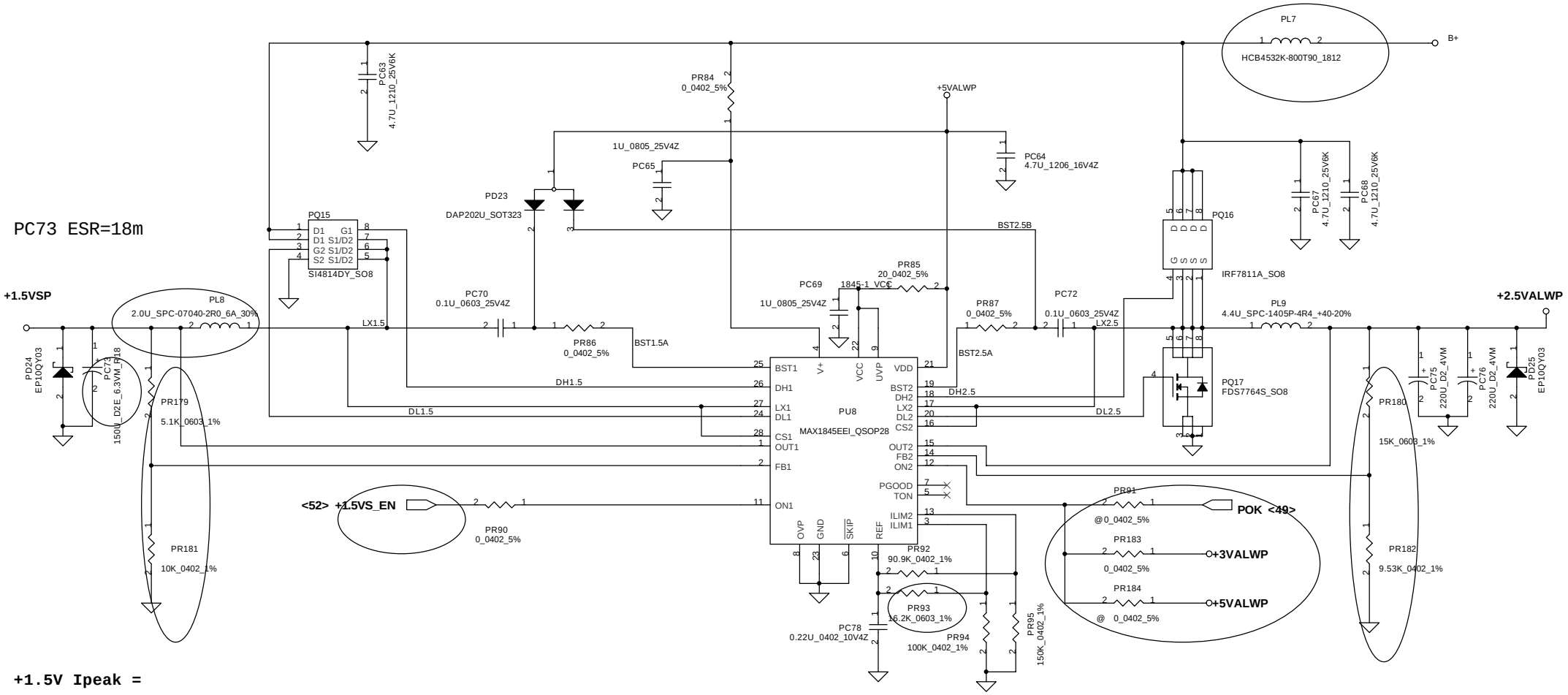

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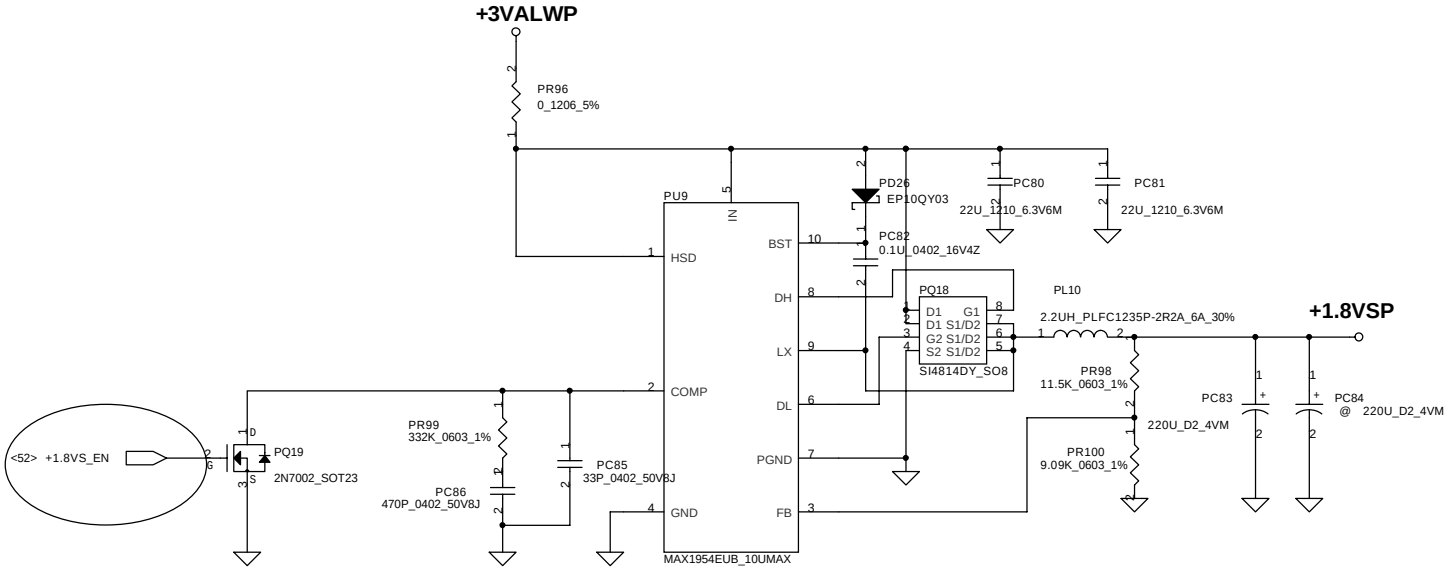

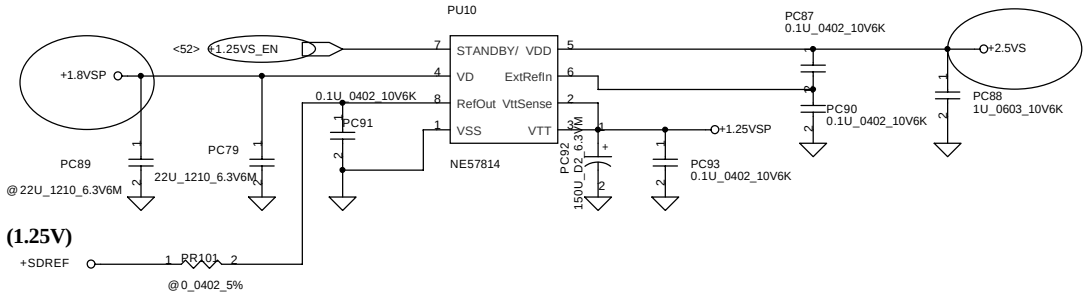

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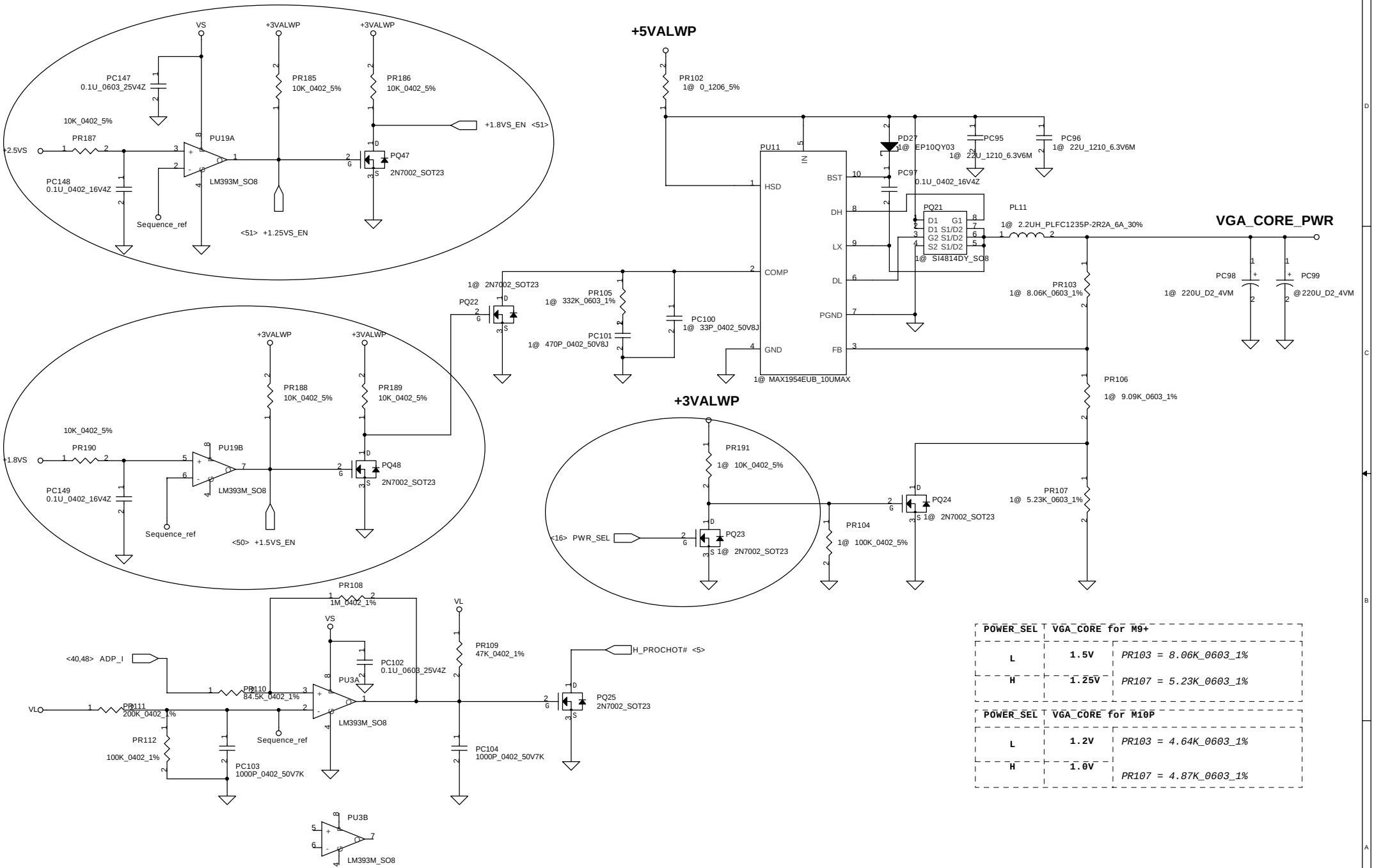

POWER_SEL	VGA_CORE for M9+	
L	1.5V	*PR103 = 8.06K_0603_1%*
H	1.25V	*PR107 = 5.23K_0603_1%*

POWER_SEL	VGA_CORE for M10P	
L	1.2V	*PR103 = 4.64K_0603_1%*
H	1.0V	*PR107 = 4.87K_0603_1%*

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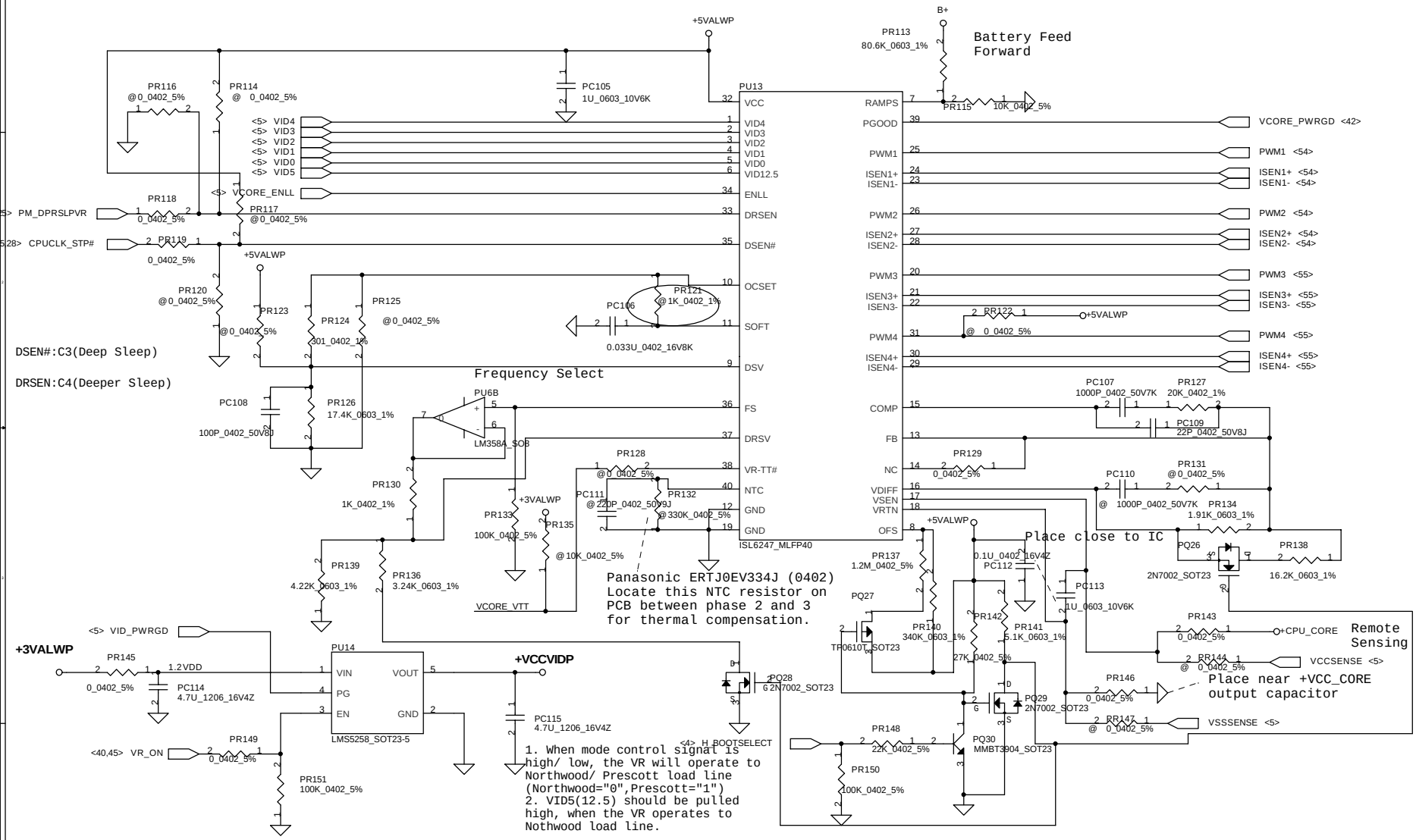

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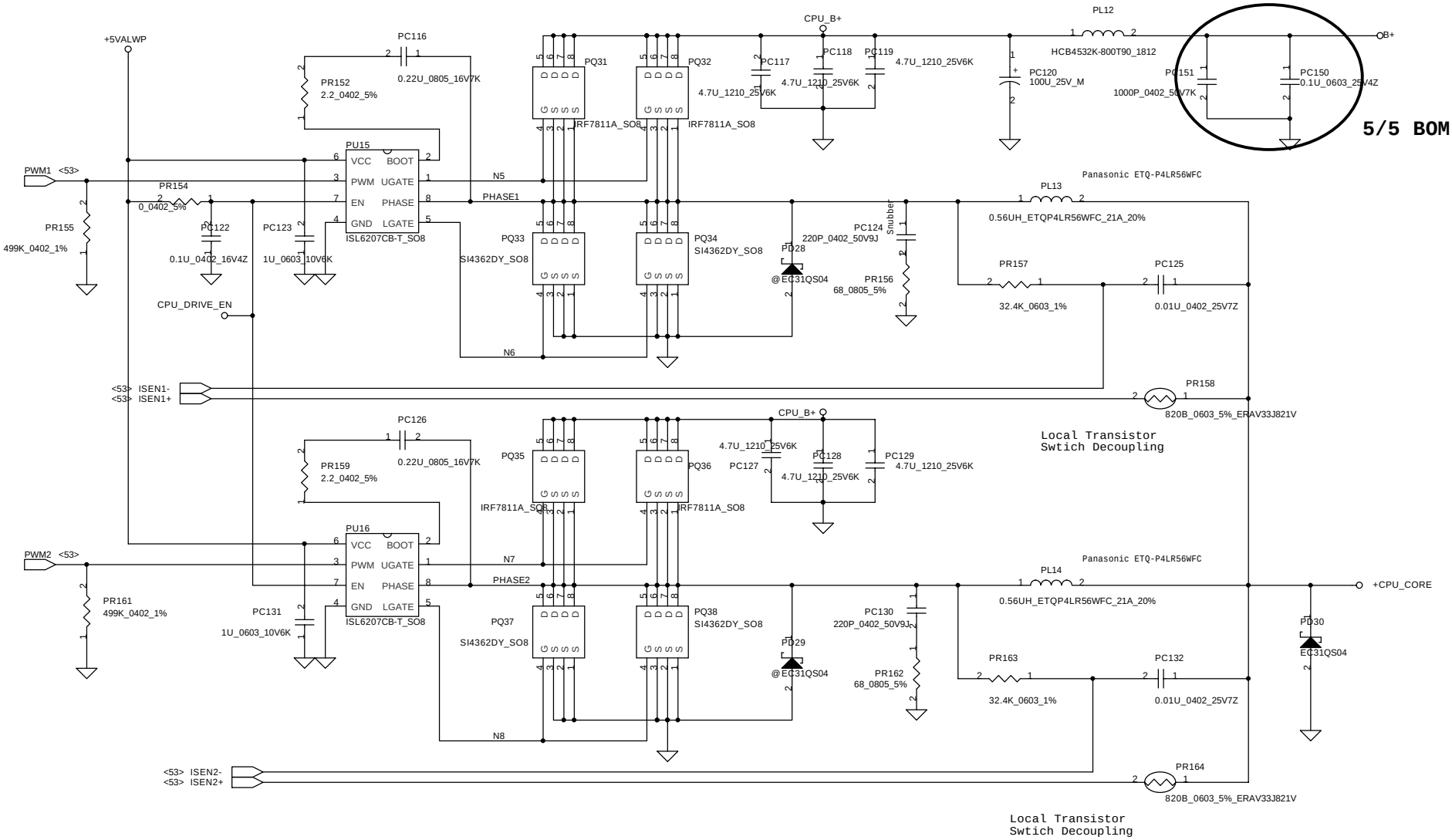

Local Transistor
Swtich Decoupling

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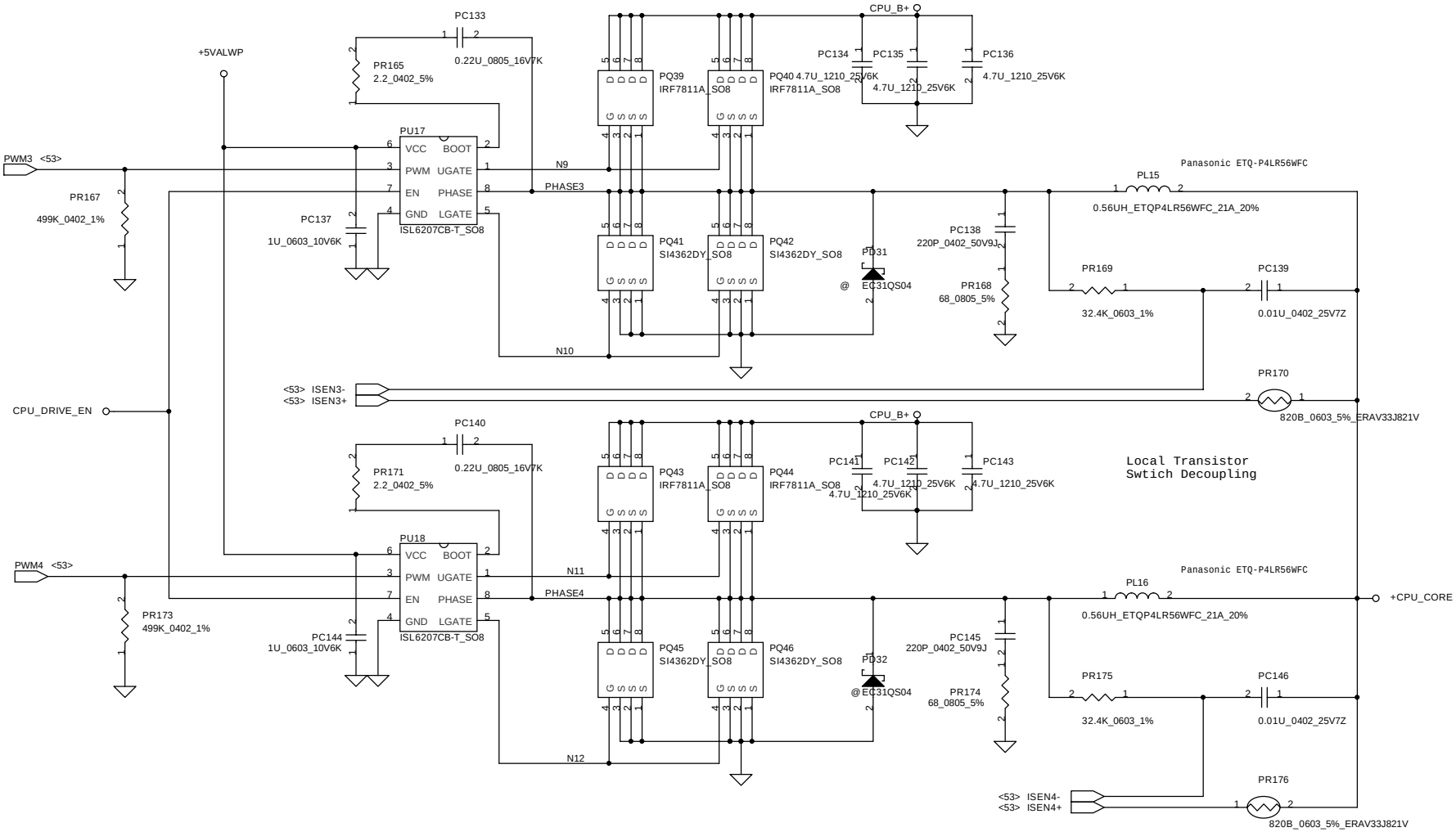

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MODIFY PIR LIST

1. Modify the Block Diagram for schematic page swap . (Page 2)
2. Modify ATI chip related schematic for recomend demo schematic and layout action . (Page 8~23)
2. Modify LAN chip related schematic for Model SPEC changed . (Page 33,34)

For B test

2003/4/10

1.Modify Q48 join to C507 (Page 29)

2003/4/15

1.SGA19471D00 470u 2.5V D4 change to SGA20471D00 470u 2.5V D2

2003/4/22

1.Page5 change R23/R139 footprint and form 51.1_0402 to 51.1_0603(BOM&layout update)
2.Page7 net name FANSPEED1 and FANSPEED2 swap(layout update)
3.Page8 change R132 from 49.9_0402 to 24.9_0402(BOM update)
4.Page8 change R134 from 24.9K_0402 to 49.9_0402(BOM update)
5.Page10 change R958.1 contact to AGP_SBA0(BOM&layout update)
6.Page10 change R959.1 contact to AGP_SBA1(BOM&layout update)
7.Page10 new add R963/R964 2.2K_0402(BOM&layout update)
8.Page10 new add R969 0_0402 for ATI INTA# issue(BOM&layout update)
9.Page10 new add R1005 4.7K_0402 pull-high +1.8VS for internal VGA Vref power(BOM&layout update)
10.Page11 change R84 to 0_0402 and R88 to 68_0603(BOM update)
11.Page12 R104 for external VGA,R102 for internal VGA(BOM control)
12.Page13 New add D32/D33 RB751V,Add R147(BOM update)
13.Page13 del R146/R493(layout update)
14.Page13 R476/R150 change to @(BOM update)
15.Page13 R475/R151 change to Pop(BOM update)
16.Page16 new add R1002/R1003 for VGA 128M DRAM(BOM&layout update)
17.Page17 U7.F20 new add trace NMCSA1#
18.Page18 U7.R6 new add trace NMCSB1#
19.Page23 change R666 from 33_0402 to 68_0402,change R699/R703 from 1K_0402 to 10K_0402,change R689/R700 from 10K_0402 to 4.7K_0402(BOM update)
20.Page23 new add D34/D35 RB751V(BOM&layout update)
21.Page24 chnage U1.14 from CRT_VCC to +5VS(layout update)
22.Page24 chnage R5.2 from GND to +5VS(layout update)
23.Page25 del R717 and RP84.1 contact to GPIO0(layout update)
24.Page25 chnage R718.1 contact to INT_OVCUR#3(layout update)
25.Page25 add R998 0_0402(BOM&layout update)
26.Page25 add R970 22_0402 for add external USB2.0 PCI clock (BOM&layout update)
27.Page26 add R1004 10K_0402 for VCORE _PWRGD pull-high +3V(BOM&layout update)
28.Page26 del RP11 and add R961/R962 10K_0402(BOM&layout update)
29.Page26 add R999/R1000/R1001 0_0402 for extrenal ovcur option(BOM&layout update)
30.Page29 Q48 pin1.2.5.6/R396.2/R702.1 contact to +5VALW for sw_cdplay power(layout update)
31.Page32 change R95.2 contact to R59.2(layout update)
32.Page35 del C415(BOM update)
33.Page35 U27 pin34 pull-high R965 0_0402 to VDDA for codec by pass mode(BOM&layout update)
34.Page37 del L39/L40/L54/L51 and add R971~R978 for external USB2.0 option(BOM&layout update)
35.Page36 add R968 for CY30/BY31 BOM option(BOM&layout update)
36.Page39 JP9 Footprint update for factory request(layout update)
37.Page40 U21 pin3,4 swap(layout update)
38.Page40 AD_BID0 for Board ID update(BOM update)
39.Page21 U29/U30 pin M4 add NMCSA1# and add R1006 0_0402 for external VGA 128M RAM option(BOM&layout update)
40.Page22 U34/U35 pin M4 add NMCSB1# and add R1007 0_0402 for external VGA 128M RAM option(BOM&layout update)
41.Page17/18 del R85,R81,R89,R97,R484,R483,R485,R486(BOM&layout update)
42.Page32 JP21 Footprint update for CIS(layout update)
43.Page25 remove R711 from page26 to page25
44.Page41 add RP113 100K_8P4R_0804 100K_0402(BOM&layout update)
45.Page44 all new add for external USB2.0(BOM&layout update)
46.Y3,Y4 footprint update(layout update)
47.D9 footprint update(layout update)
48.page32 R69.2 contact to V1.8_LAN for LAN vender updater(layout update)
49.page32 R94.1 contact to LANVDD(layout update)
50.page32 R60/R49/C55/C52 BOM option(BOM update)

2003/4/24

1.page5 Add R1008 for speedstep issue(BOM&layout update)
2.page25/40 Y3/Y4 pin define update(layout update)

2003/4/25

1.page31 add resume for carbus issue(layout update)
2.page26 del R215 for R216 only(BOM&layout update)

2003/4/30

1.page45 add R1009 for SUSP#(BOM&layout update)
2.page32 add R1010 for LAN transformer issue(BOM&layout update)

2003/5/02

1.page40 change HPS from U21 88pin to 36pin(layout update)
2.page43 change JP24 pin7/8/9/10 to MDI0-/MDI0+/MDI1-/MDI1+ (layout update)
3.page43 USB20P2+ and USB20P2- swap(layout update)
4.page38 del RP1/RP91(BOM&layout update)
5.page23 del R605(BOM&layout update)
6.page28 change R598 to @ and del @ for R597(BOM update)
7.page37 add R1011~R1018 for USB2.0 option(BOM&layout update)

2003/5/05

1.page11 del R74,C84(layout update)
2.page25/30/32/33/34/38/40/44 add AC termination R305,C353,R61,C40,R520,C608,R519,C601,R576,C632,R270, C315,R981,C784,R200,C228 for EMI request(BOM update)
3.page25 change damping resistor R561,R563,R562,R560,R566,R549,R970,R559 to 33 ohm(BOM update)
4.page11/16 add AC termination R395,C464,R101,C127,R389,C451 for EMI request(BOM update)
5.page11/16 add AC termination R395,C464,R101,C127,R389,C451 for EMI request(BOM update)
6.page35 add AC termination C415 for EMI request(BOM update)
7.page7 add FAN Cap C641,C640,C633,C623 for EMI request(BOM update)
8.page24 new add Cap C806,C807 for EMI request(BOM&layout update)
9.page43 new add Cap C808 for SPR PS2 issue(BOM&layout update)
10.page27 change cap R634 footprint to 0_1206(BOM&layout update)

2003/5/14

1.R702 from 100K change to 10K (BOM update)

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2003/5/22

1.Page13 R147.1 connect to R473.2,R489.1 connect to R502.2(layout update)

2003/6/09

1.Page7 C623/C633 update footprint 0402 type(layout update)
2.Page45 R199,R567,R167 update value for power sequence delay(BOM update)
3.Page25 del R569 for PCI_CLKRUN# pull_high(Layout & BOM update)
4.Page25 Add R578 for PCI_CLKRUN# pull_high(Layout & BOM update)
5.Page30 Del R311 for PCI_CLKRUN# pull_high(BOM update)
6.Page40 Del R268 for EC591 not need (BOM update)
7.Page29 add D36 for SIDEPWR leakage current(layout & BOM update)
8.Page10 Del R1005 it's not need(BOM update)
9.Page41 Add R1021 for EC_FLASH# pull_high(Layout & BOM update)
10.Page26 Add R1022 pull_high(Layout & BOM update)
11.Page26 R956 pin1 contact to GND(Layout update)
12.Page8 add R1023(BOM update)
13.Page8 Del R173,R479,Q12 for change to @(BOM update)

2003/6/11

1.Page5 R1008 change to 4.7K_0402 for follow HR60(BOM update)
2.Page5 Q5,Q6 change to MMBT3904 for follow HR60(BOM update)
3.Page5 del RP4 for ITP update (BOM update)
4.Page5 add R1024 47_0402,R1027 47_0402 ,R1025 150_0402 ,R1026 680_0402,R390 54.9_0603_1%,R404 54.9_0603_1% for ITP update(Layout & BOM update)
5.Page6 del C122,C46 for cost down (BOM update)
6.Page12 del C576,C588,C201,C198 for cost down (BOM update)
7.Page12 Change C150 to 47U_B(Layout & BOM update)
8.Page12 add C810,C811,C812 0.1U_0402 for +1.5VS(BOM update)
9.Page15 add C813,C814 22U_1206 for +1.25VS(Layout & BOM update)
10.Page15 del C280,C282 for cost dowN(BOM update)
11.Page16 add @ R1028 contact to PCI_RST# for RST# option(Layout update)
12.Page16 add R1029 0_0402 contact to NB_RST# for RST# option(Layout & BOM update)
13.Page16 add @ R1030 for M9+ SUS_STAT# option(Layout update)
14.Page16 add R1031 10K_0402 for M9+ SUS_STAT# pull-high +3VS(Layout & BOM update)
15.Page17,18 del R405,R407,R420,R421,R466,R467,R465,R464(BOM update)
16.Page19 Add C815,C816 for +VDDC15(Layout & BOM update)
17.Page20 Del C497 for cost down(BOM update)
18.Page21 Del RP25,RP26,RP27,RP28,RP29,RP30,RP31,RP32,RP33,RP34,RP35 for cost down(Layout & BOM update)
19.Page21,22 Del RP36,RP37,RP38,RP39,RP40 for cost down(Layout & BOM update)
20.Page21,22 Del RP41,RP42,RP43,RP44,RP45,RP46,RP47,RP48,RP49,RP50 for cost down(Layout & BOM update)
21.Page22 Del RP52,RP53,RP54,RP55,RP56,RP57 for cost down(Layout & BOM update)
22.Page21 Del R384,R394,R418,R385,R383,R398,R410,R386 for cost down(Layout & BOM update)
23.Page21 Del R505,R453,R474,R509,R506,R455,R461,R508 for cost down(Layout & BOM update)
24.Page22 Del R516,R534,R497,R524,R518,R535,R496,R522 for cost down(Layout & BOM update)
25.Page22 Del R523,R498,R533,R515,R527,R499,R532,R517 for cost down(Layout & BOM update)
26.Page23 Change U40 pin10 contact to VTT_PWRGD (Layout update)
27.Page24 Add C817 10U_0805 for LCDVDD_C power (Layout & BOM update)
28.Page25 Add C818,C819 180P_0603 (Layout & BOM update)
29.Page25 Add C621,C622 180P_0603 (BOM update)
30.Page26 Add R1032,R1033 10K_0402 for PWRBTN_OUT pull-high and SB_EEDI pull-down (Layout & BOM update)
31.Page26 Del R208,R209 8.2K_0402(Layout & BOM update)
32.Page26 Change R224,R219,R707,R708 to 8.2K_0402(BOM update)
33.Page26 Del R1004 10K_0402(Layout & BOM update)
34.Page44 Add R997 0_0402(BOM update)
35.Page44 R997 pin1 contact to LPC_SMI# for DOS mode USB support (Layout update)
36.Page27 Add D37 RB751V,R1034 1K_0402(Layout & BOM update)
37.Page27 Change C219,C223,C222,C699 to 22U_1206(Layout & BOM update)
38.Page28 Add R685,R669,R697,R670,R677 10K_0402(BOM update)
39.Page28 Del R698 10K_0402(BOM update)
40.Page40 Add C820 for EC97591 option(Layout update)
41.Page42 Add R253 0_0402(BOM update)
42.Page42 Del R229,R745,R746,Q67,C299,C281,Q20,Q24,(BOM update)
43.Page42 Change R252 to 330K_0402(BOM update)
44.Page42 Change C307 to 0.1U_0402(BOM update)
45.Page42 Add R1035 1K_0402,R1036 10K_0402,C821 0.1U_0603,Q68 2N7002(Layout & BOM update)
46.Page43 Add R1037,R1038,R1039,R1040 0_0402 for SPR LAN option(Layout & BOM update)

2003/6/12

1.Page43 Change R979,R980 contact to JP24 pin21,20 for USB trace option (Layout update)
2.Page43 Change R979,R980,L37,L38 to 0_0402 for SPR USB option(Layout & BOM update)
3.Page37 Change L32,L33,L34,L35,L53,L55,L50,L52 to 0_0402 for SPR USB option(Layout & BOM update)
4.Page26 Del R638,R647,R613,R640,R601,R611,R593,R603,R553,R551,R555,R550 for ATI DOC_PA_218IXP0T1 request(BOM update)
5.Page24 JP5,JP6 reverse for ME update(Layout update)

2003/6/12

1.Page32 Del U6 Pin114,113(schematic update)
2.Page32 Q44,Q46 from 2SB1197 change to 2SB1188(Layout & BOM update)
3.Page32 U28 from 24ST0023P change to H5007(H1285)
4.Page32 C10 1000P_0402_50V7K change to 1000P_1206_2KV7K (Layout & BOM update)

2003/6/16

1.page11 Add L59,L60,L61,L62,L63 0805 type NB power bed (Layout & BOM update)
2.page11 Change R399,R70 type to 0805 for NB power bed (Layout & BOM update)
3.page11 Del Q47 for change to @(BOM update)

2003/6/17

1.Page24 JP5,JP6 reverse again for ME update(Layout update)
2.page40 Change C820 to 0603 type(Layout update)

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2003/6/18
1.Page8 Add C822 D2 type for CPVDD power(Layout update)
2.Page16 Add R1041 8.2K_0402 AGP_FRAME# pull-high to +3VS(Layout & BOM update)
3.Page45 Add R1042,Q69 / R1043,Q70 / R1044,Q7 ,for +3V,+1.5VS,+VGA_CORE discharge circuit(Layout & BOM update)
4.Page8 add C823 0.1u_0402 for ATI recommand
5.Page19 add C824,C825,C826 0.1U for 1.5VS
C828,C827 0.1U for +VDDC15
2003/6/19
1.Page32 U28 +-pair reverse(Layout update)
2.Page14 add RP114,RP115,RP116,RP117,RP118,RP119,RP120,R1045,R1046,R1047,R1048,R1049,R1050,R1051,R1052,R1053 for ATI DDR recommand(Layout & BOM update)
3.Page23 R688 pin1 contact to U40 pinD5(Layout update)
4.Page42 C821 change to 0402 type(Layout & BOM update)
5.Page8 Update C822(Layout update)
6.Page43 Update L34,L38 to JP24 NET name.
2003/6/20
1.Page34 add C663 for audio noise(BOM update)
2003/6/22
1.Page25 R187 change to 4.7K for 4/22 ATI review update(BOM update)
2.Page25 GPIO0,OVCUR#4 pull-down for 4/22 ATI review update(Layout update)
3.Page26 del R1033 for 4/22 ATI review update(BOM update)
4.Page26 R706 pull-high to +3V for 4/22 ATI review update(BOM update)
5.Page28 R579 pull-high to +3VS for 4/22 ATI review update(Layout update)
6.Page28 del R597(CPU_STP# strap not need) for 4/22 ATI review update(BOM update)
7.Page29 Change R732,R734,R747,R165,R159,R164 to 33_0402 for 4/22 ATI review update(BOM update)
8.Page29 SD_D7 Add R1054 10k_0402 Pull-down for 6/22 ATI review update(Layout & BOM update)
2003/6/24
1.Page38 Del RP65 for cost down(Layout & BOM update)
2.Page38 Add RP0121,RP122 for cost down(Layout & BOM update)
3.Page40 Add RP0123,RP124 for cost down(Layout & BOM update)
4.Page40 Del RP19 for cost down(Layout & BOM update)
2003/6/25
1.Page43 change SPR USB power source(Layout update)
2003/6/26
1.Page43 add U50,C829 for SPR USB power switch(Layout & BOM update)
2.Page26 add R659,C659 for EMI request(BOM update)
2003/7/01
1.Page16 add R1030 0_0402 for S3 SUS_STAT# issue(BOM update)
2.Page16 del R1031 for S3 SUS_STAT# issue(BOM update)

For C test

2003/7/07
1.Page36 C364 from 1U_0402 change to 1U_0603 (Layout & BOM update)
2.Page31 C366,C352 from 4.7U_1206 change to 4.7U_0805 (Layout & BOM update)
3.Page29 C507 from TAN4.7U_0805 change to 4.7U_0805 (Layout & BOM update)
4.C170,C184,C189,C217,C224,C229,C277,C615,C620,C677,C718,C723,C728 from 10U_1206 change to 10U_0805 (Layout & BOM update)
5.C68,C92,C168,C406,C416,C420,C468,C565,C606,C730,C780,C637,C642 from 10U_1206 change to 10U_0805 (Layout & BOM update)
2003/7/10
1.Page5 change R194 from 62_0402 to 200_0402 for ATI recommend(BOM update)
2.Page8 change R80 from 412_0402 to 330_0805_1% for ATI recommend(BOM update)
3.Page11 del M9@ C75/X2/R73 ATI recommend(BOM update)
4.Page11 add R1055 4.7K_0402 for ATI recommend(Layout & BOM update)
5.Page16 add Q72 for SUSSTAT# level shift and ATI recommend(Layout & BOM update)
6.Page16 add R1031 10K_0402 for SUSSTAT# level shift and ATI recommend(BOM update)
7.Page16 change R1030 to 470_0402 for SUSSTAT# level shift and ATI recommend(BOM update)
8.Page24 add R1056 2.7K_0402 for ENAVDD pull-down and ATI recommend(Layout & BOM update)
9.Page25 change D13 to RB751V for ATI recommend(Layout & BOM update)
10.Page40 change +RTCVCC to BATT1.1 for ATI recommend(Layout update)
11.Page8 del C97 for CEL CPU can't BOOT issue(BOM update)
12.Page40 del R270/C315 for can't BOOT issue(BOM update)
13.Page32 update Q44/46 footprint(Layout update)
14.Page14 add C830/C831 for ATI recommend(Layout & BOM update)

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For C test

2003/7/11

1.Page29 add R1057 0_0402 for cost down(Layout & BOM update)
2.Page29 del Q64/R702/Q61 for cost down(BOM update)
3.Page29 del D36 for cost down(BOM update)
4.Page29 add R1058 for cost down(BOM update)
5.Page35 del R295/Q34 for cost down(BOM update)

2003/7/15

1.Page35 add C832_1U_0603 for MIC noise issue(Layout & BOM update)
2.Page35 Change C379 form 0805 to 0603(Layout & BOM update)
3.Page35 add C410 form audio noise(BOM update)
4.Page29 add C609/C174 form audio noise(BOM update)
5.Page36 add R1059 form audio AMP(Layout & BOM update)
6.Page36 del R339/R334/R335/R333/Q30/Q31/Q32/Q33 form audio AMP(BOM update)
7.Page36 R338 change to 1K_0402(BOM update)

2003/7/18

1.Page39 add C833/C836/C837/C838/C839 for EMI request(Layout & BOM update)
2.Page10 DEL R118/R112/U9/L16/R117/C148/R111/R108/R116/C137/C133 for EMI request(BOM update)
3.Page35 add R1061 2.2K_0402(Layout & BOM update)
4.Page35 change JP9 pin34/35 to (Layout update)
5.Page26 RP12 from 10k change to 2.2K (BOM update)

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B Ver.
1		modify for RTC battery	46	Del PD6(RLZ3.6B) and add PR177(100_0805_5%) Add PR178(200_0603_5%)	EVT
2		For ME change battery connecter	47	change P/N: from DC040012310 to DC040012330	EVT
3		Modify +1.5VSP ripple and OCP +2.5ALWP output voltage	50	change PL8 from 5U_SPC-06704-5R0_2.9A to 2U_SPC-SPC-07040-2R0_6A change PC73 from 150U/4V(ESR=45) to 150U/6.3V(ESR=18) change PR93 from 102K_0402_1% to 16.2K_0402_1% add PR179(5.1K_0402_1%) add PR181(10K_0402_1%) add PR180(15K_0402_1% add PR182(9.53K_0402_1%)	EVT
4		add power sequence circuit for HW requirement	52 50	add PU19 LM393M_SO8 add PC147 0.1U_0603_50V add PC148 0.1U_0603_50V add PC149 0.1U_0603_50V add PR187 10K_0603_5% add PR185 10K_0603_5% add PR186 10K_0603_5% add PR183 0_0402_5% add PR184 0_0402_5% add PR188 10K_0603_5% add PR189 10K_0603_5% add PR190 10K_0603_5% add PQ47 2N7002_SOT23 add PQ48 2N7002_SOT23	EVT
5		add VGA_CORE power select for HW requirement	52	add PQ23 2N7002_SOT23(for DBY31)	EVT
6		change CPU CORE boost resister value for EMI requirement	54 55	change PR152 , PR159 , PR165 , PR171 from 0_0603_5% to 2.2_0603_5%	EVT
7		Add by pass cap. for EMI requirement	54	Add PC150 0.1U_0603_50V Add PC151 1000P_0603_50V	EVT
8		For BOM error	51	Change PR98 vaule from 4.87K_0603_1% to 11.5K_0603_1%	EVT
9		Change Battery side OTP point to 79C for thermal requirement	47	Change PR39 from 16.9K_0603_1% to 14.7K_0603_1% Change PR41 from 3.32K_0603_1% to 3.48K_0603_1%	DVT
10		Delete CPU_CORE IC's OTP function	53	Delete PR132,PC111	DVT
11		Add snubber for EMI requirement	54,55	Add 68_0805_5% at PR156,PR162,PR168,PR174 Add 220P_0603_50V at PC124,PC130,PC138,PC145	DVT
12		Change Material	49,50	Change PC53,PC58,PC73 from SGA19151330(H2.8) to SGA20151320(H1.9)	DVT

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B Ver.
14		**To prevent surge current at CPU_CORE**	54,55	Add 499K_0603_5% at PR155,PR161,PR167,PR173	**PVT**