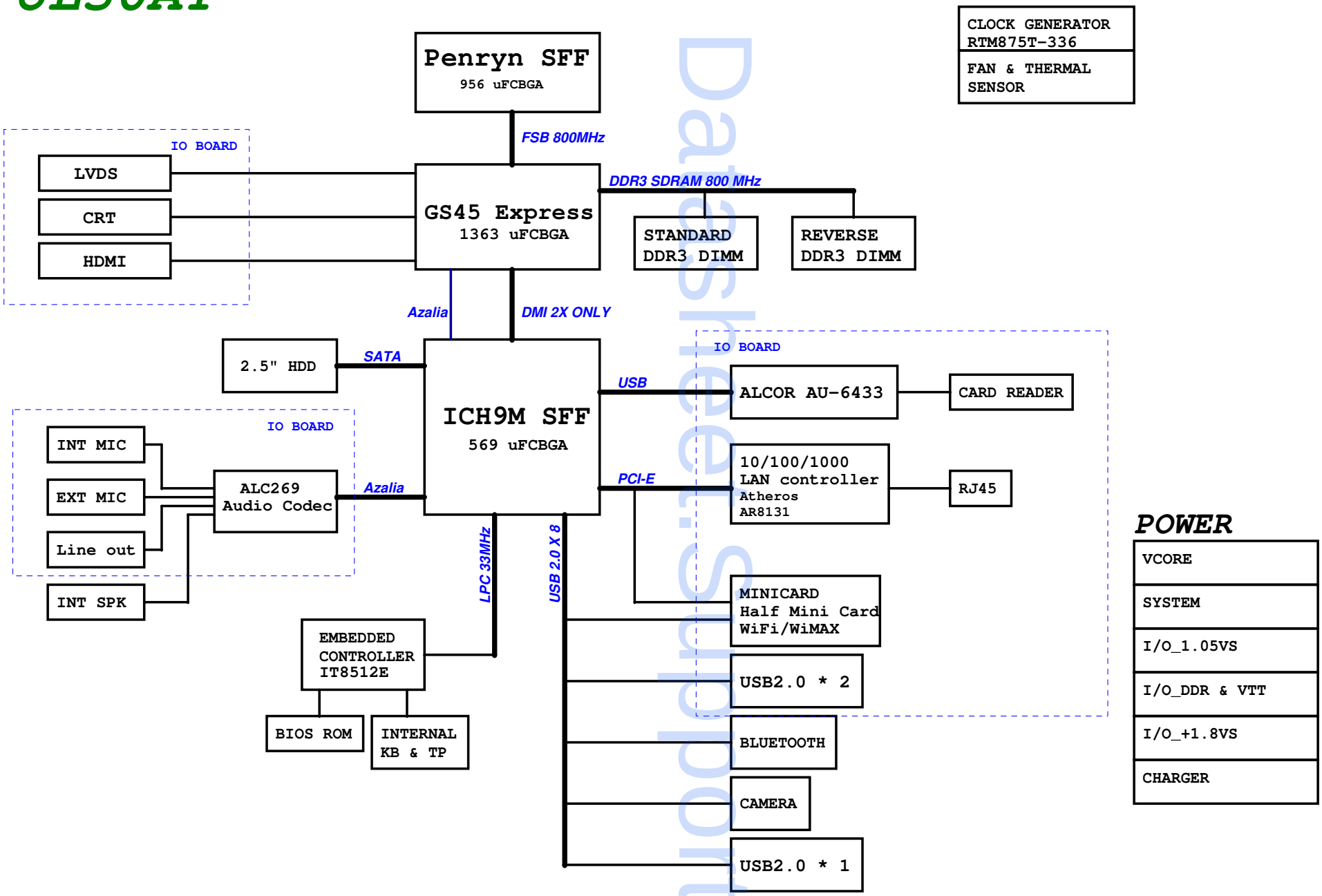
UL50AT



<Variant Name>

ASUSTeK COMPUTER INC.

Title : Block Diagram

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 1 of 97

UL50A SCHEMATIC Revision 2.1

PAGE	Content

SYSTEM PAGE REF.

PAGE	Content

POWER PAGE REF.

<Variant Name>

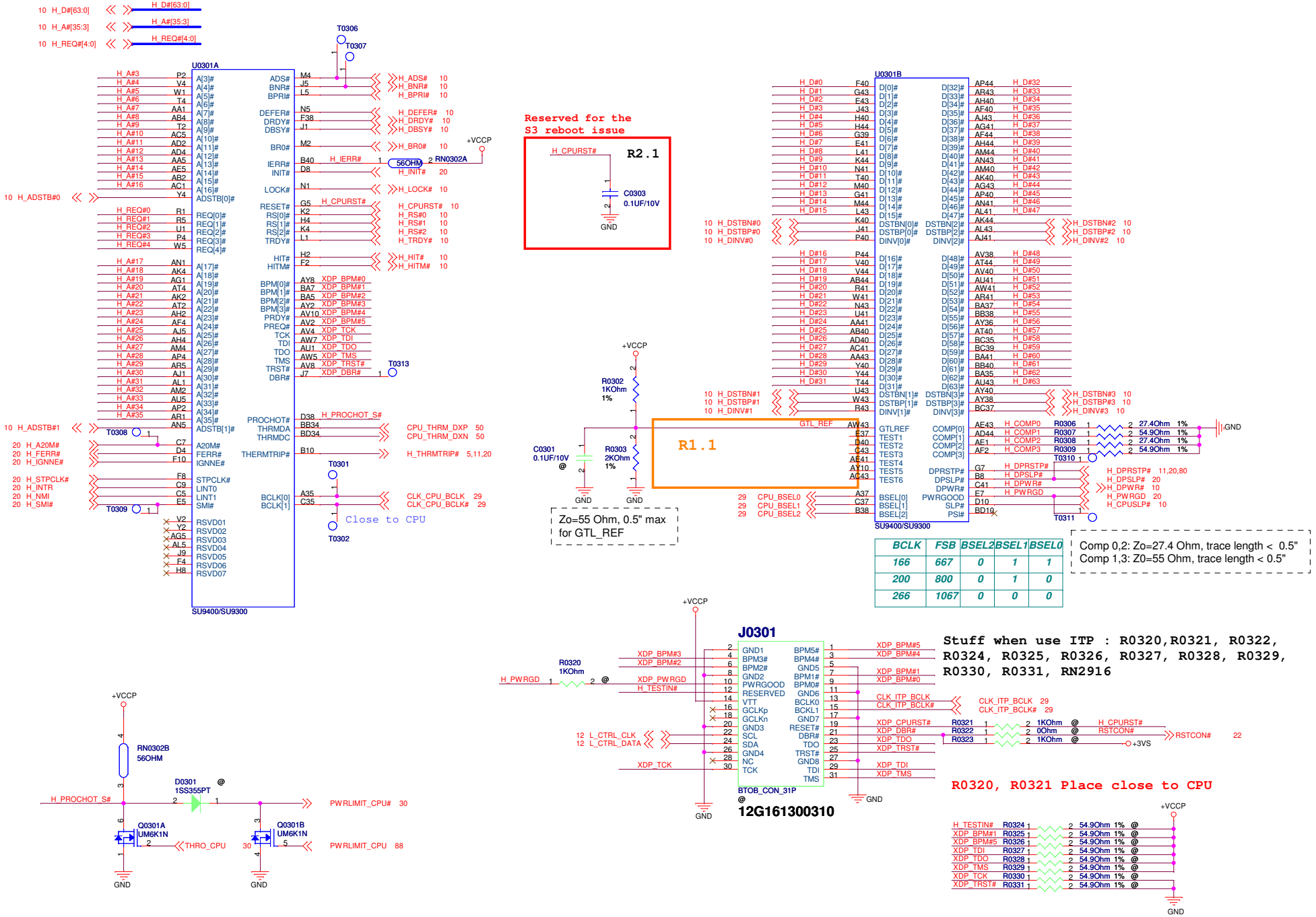
ASUSTeK COMPUTER INC.

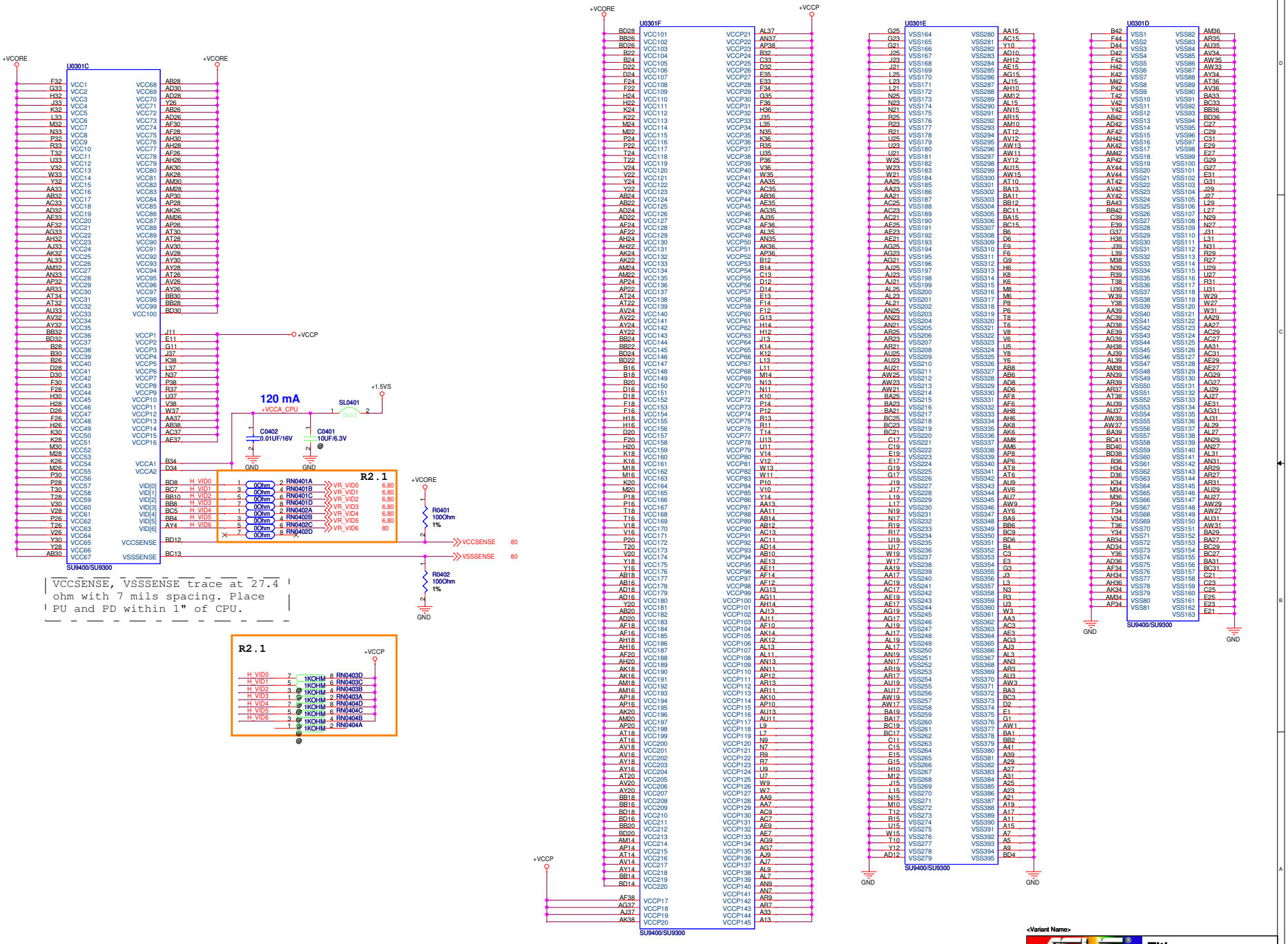
Title : Page Reference

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 2 of 97


U0301A
SU9400/SU9300
U0301B
SU9400/SU9300
Reserved for the S3 reboot issue
R2.1
C0303 0.1UF/10V
R1.1
Zo=55 Ohm, 0.5" max for GTL_REF
Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"
BCLK FSB BSEL2 BSEL1 BSEL0
166 667 0 1 1
200 800 0 1 0
266 1067 0 0 0
J0301
BTOB_CON_31P
12G161300310
Stuff when use ITP : R0320,R0321, R0322, R0324, R0325, R0326, R0327, R0328, R0329, R0330, R0331, RN2916
R0320, R0321 Place close to CPU
Close to CPU
RN0302B 56OHM
D0301 1SS355PT
Q0301A UM6K1N
Q0301B UM6K1N
RN0302A 56OHM
Title : PENRYN ULV FSB
ASUSTeK COMPUTER INC.
Engineer: Jack Hsu
Project Name UL50AT
Rev 2.0
Date: Friday, October 16, 2009
Sheet 3 of 97



<Variant Name>

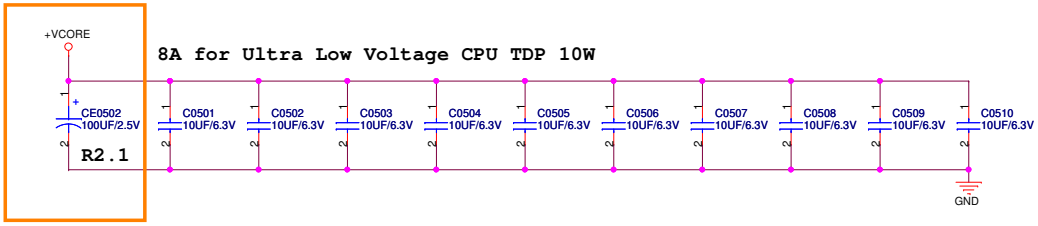
Title : PENRYN ULV POWER

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

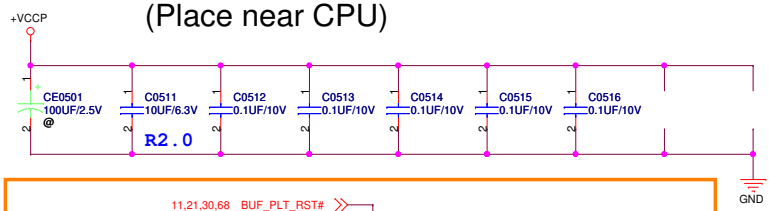
Date: Friday, October 16, 2009 Sheet 4 of 97

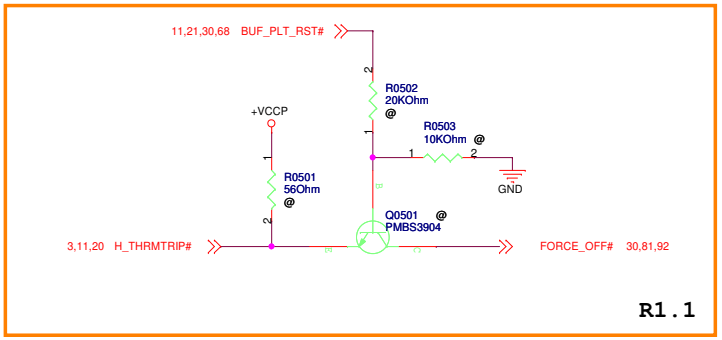


Decoupling guide from Intel

VCORE	10uF mount	*4pcs
	0.1uF mount	*5pcs
VCCP	1uF	* 12pcs
	270uF	* 1pcs
VCCA	0.01uF	* 1 pcs
	10uF	* 1 pcs

+VCCP Decoupling Capacitor (Place near CPU)

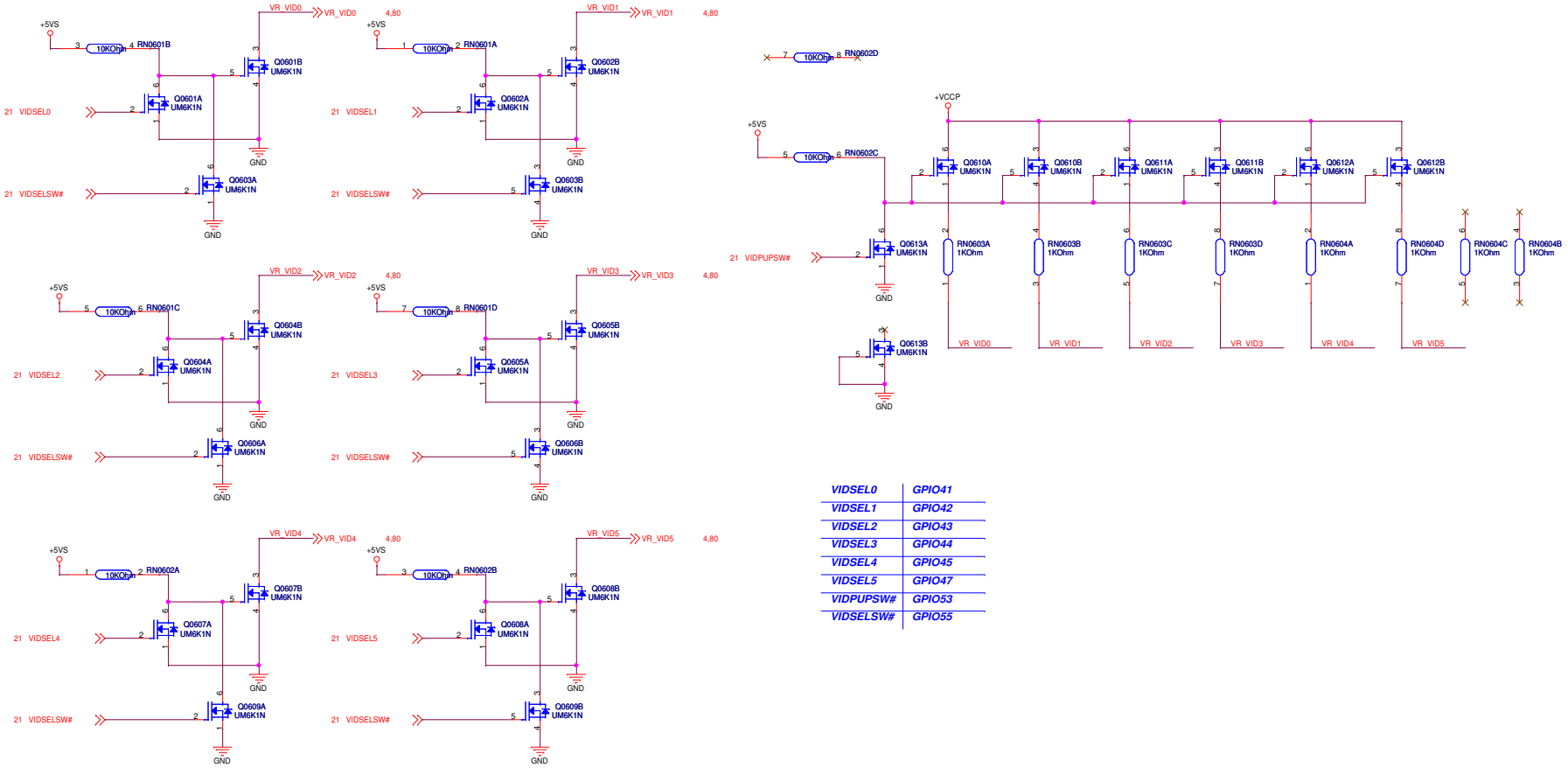




<Variant Name>

ASUSTeK COMPUTER INC.	Title : CPU CAPACITORS	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 5 of 97	

R2.1



VIDSEL0	GPIO41
VIDSEL1	GPIO42
VIDSEL2	GPIO43
VIDSEL3	GPIO44
VIDSEL4	GPIO45
VIDSEL5	GPIO47
VIDPUPSW#	GPIO53
VIDSELSW#	GPIO55

<Variant Name>

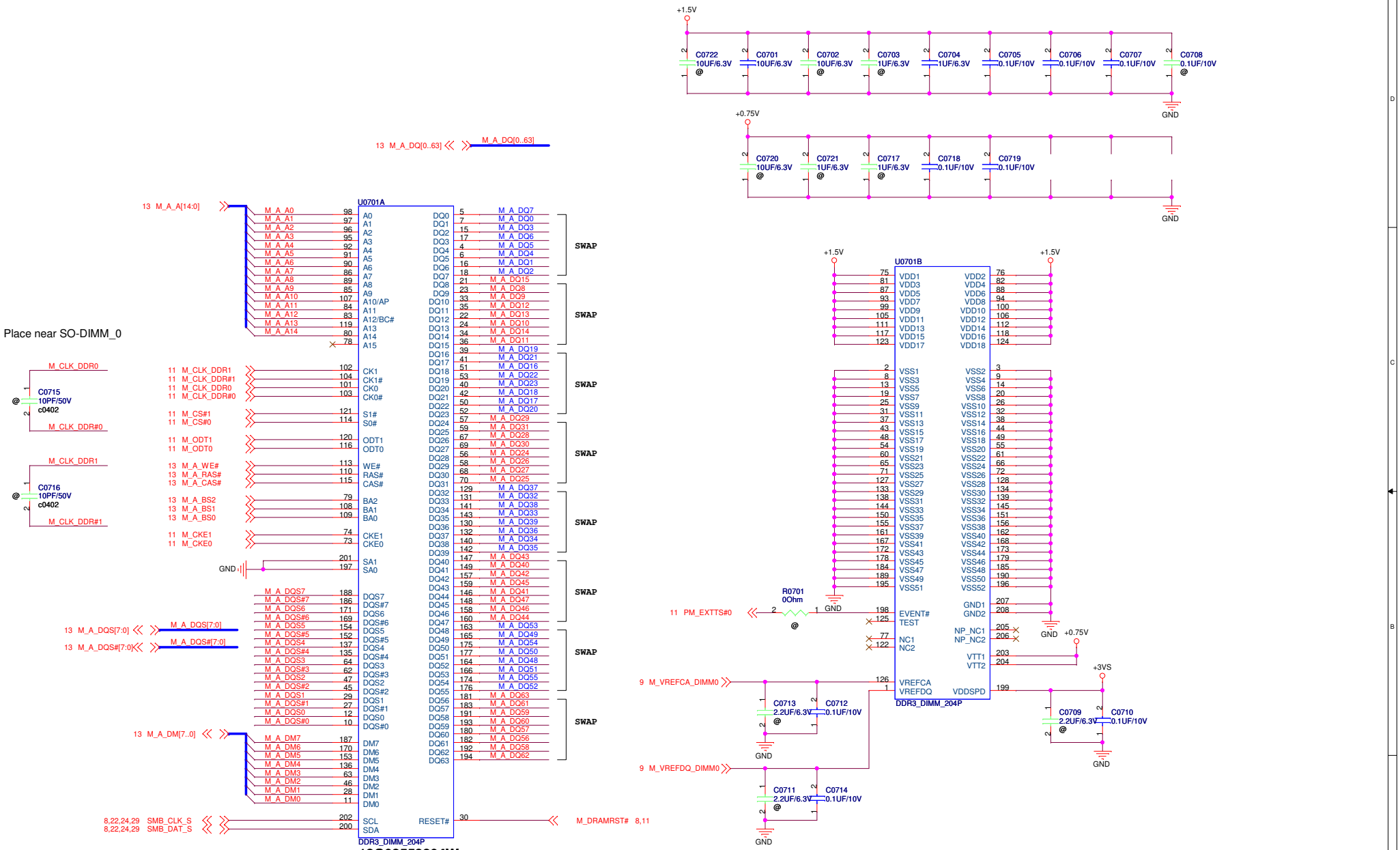
ASUSTeK COMPUTER INC.

Title :

Engineer: Jack Hsu

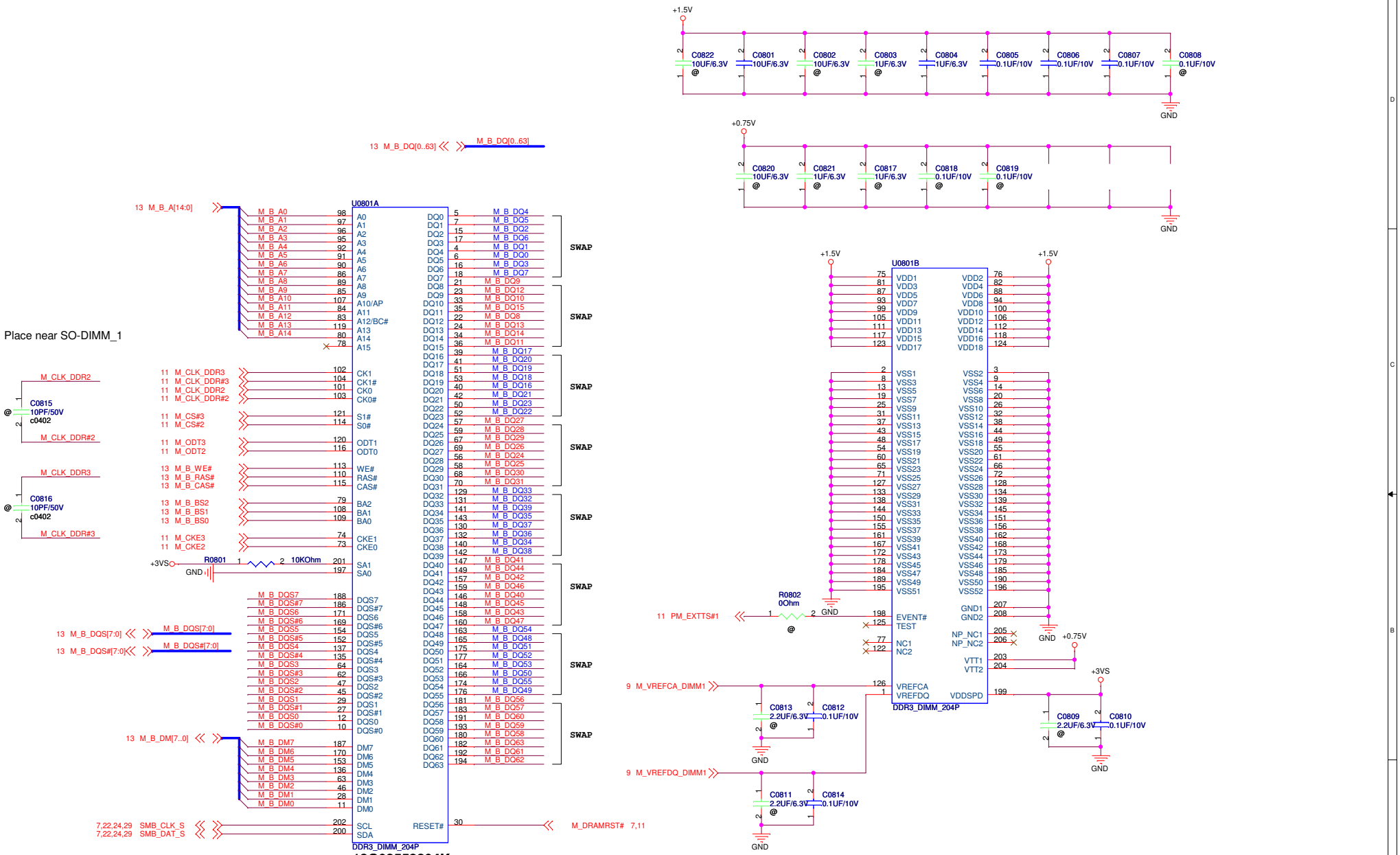
Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 6 of 97



<Variant Name>

ASUSTeK COMPUTER INC.	Title : DDR3 SO-DIMM A	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 7 of 97	



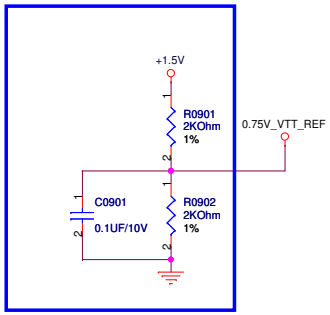
12G02553204K

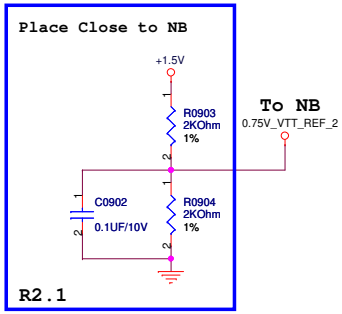
DDR3 DIMM 204P,1.5V,5.2H,STD

<Variant Name>

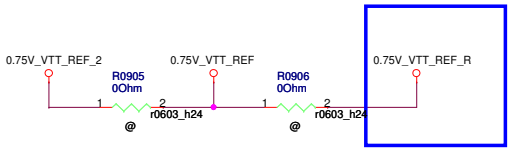
ASUSTeK COMPUTER INC.	Title : DDR3 SO-DIMM B		
	Engineer: Jack Hsu		
Size: Custom	Project Name: UL50AT		Rev: 2.0
Date: Friday, October 16, 2009	Sheet 8 of 97		

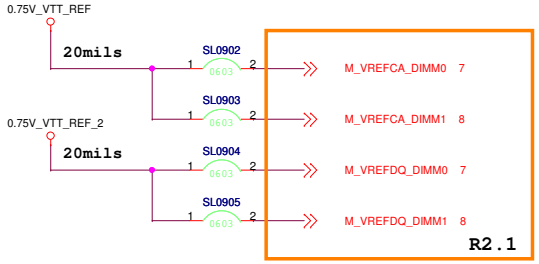
R2.1





From DDR/VTT Power Circuit





<Variant Name>

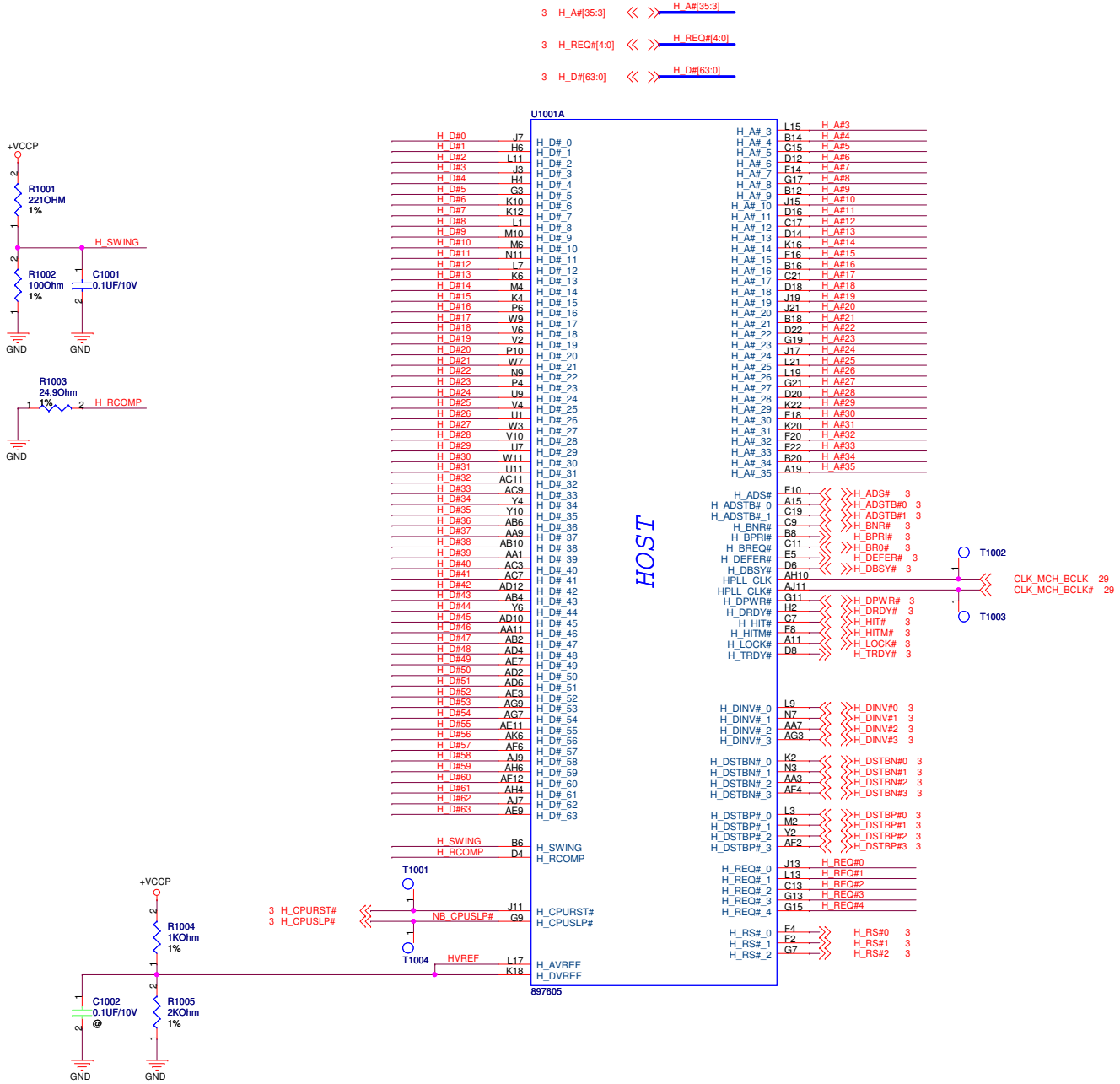
ASUSTeK COMPUTER INC.

Title : DDR3 VREF

Engineer: Jack Hsu

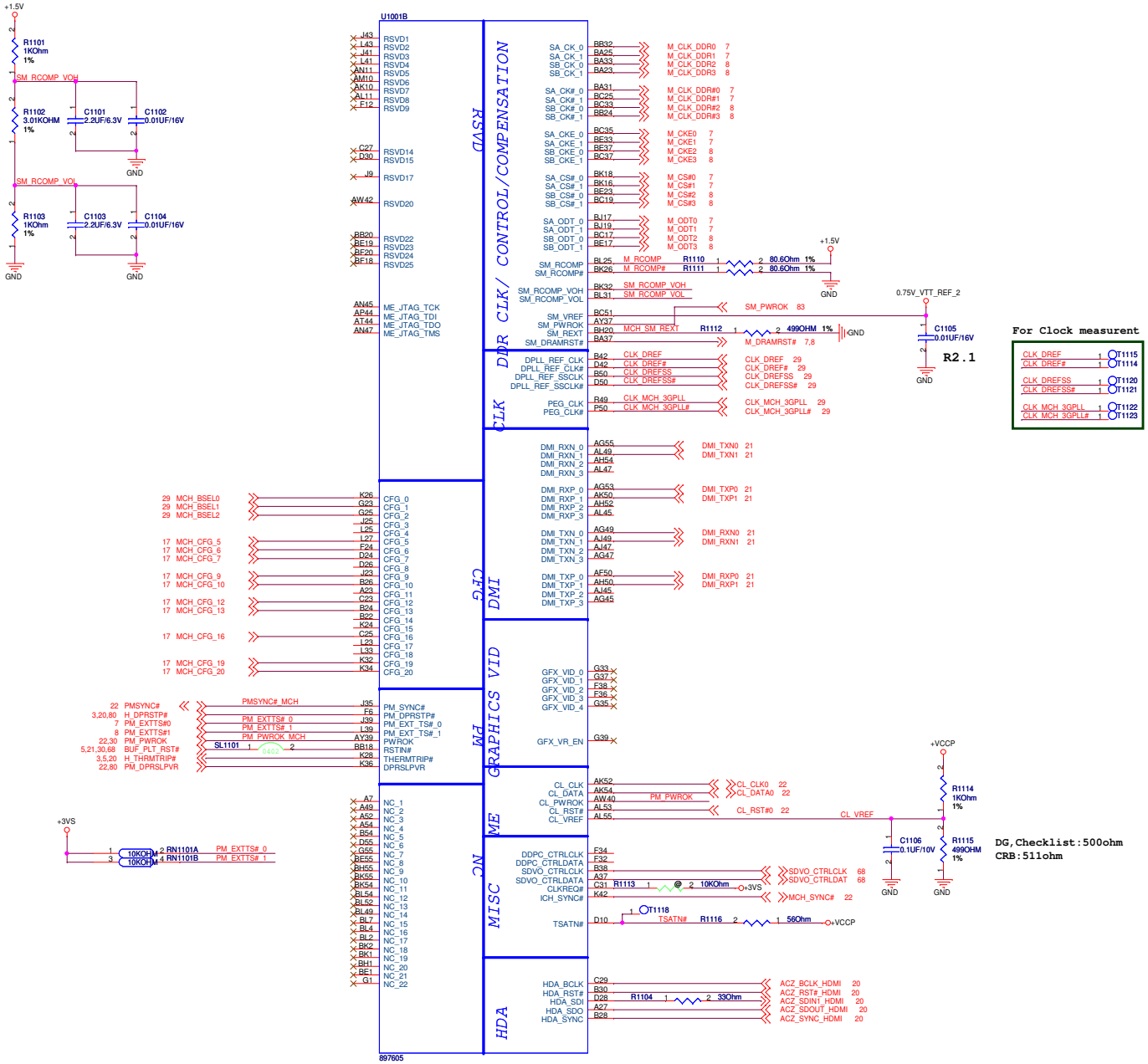
Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 9 of 97



<Variant Name>

ASUSTeK COMPUTER INC.	Title : NB GS45 HOST	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 10 of 97	



<Variant Name>

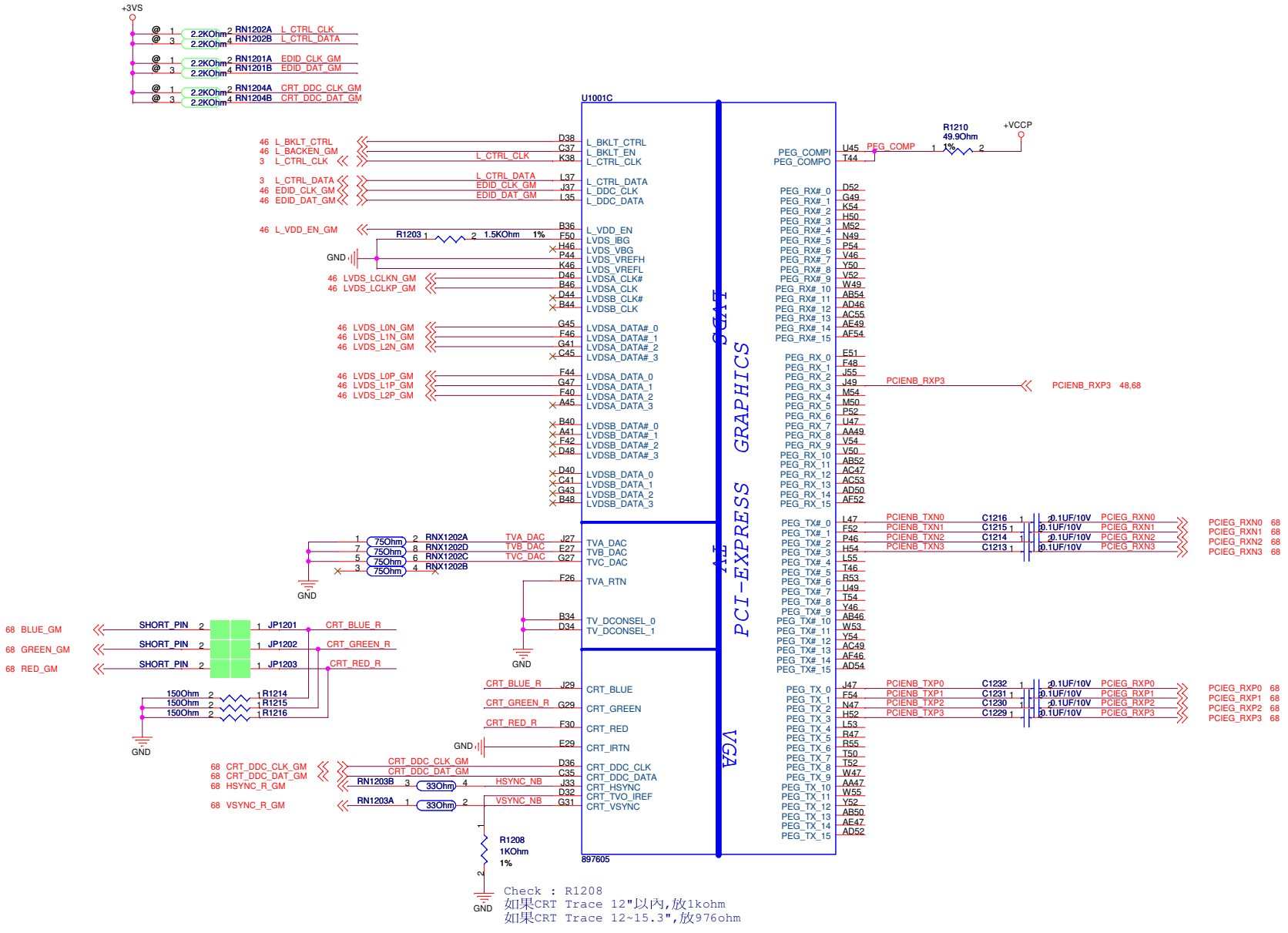
ASUSTeK COMPUTER INC.

Title : NB GS45 DMI

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 11 of 97



<Variant Name>

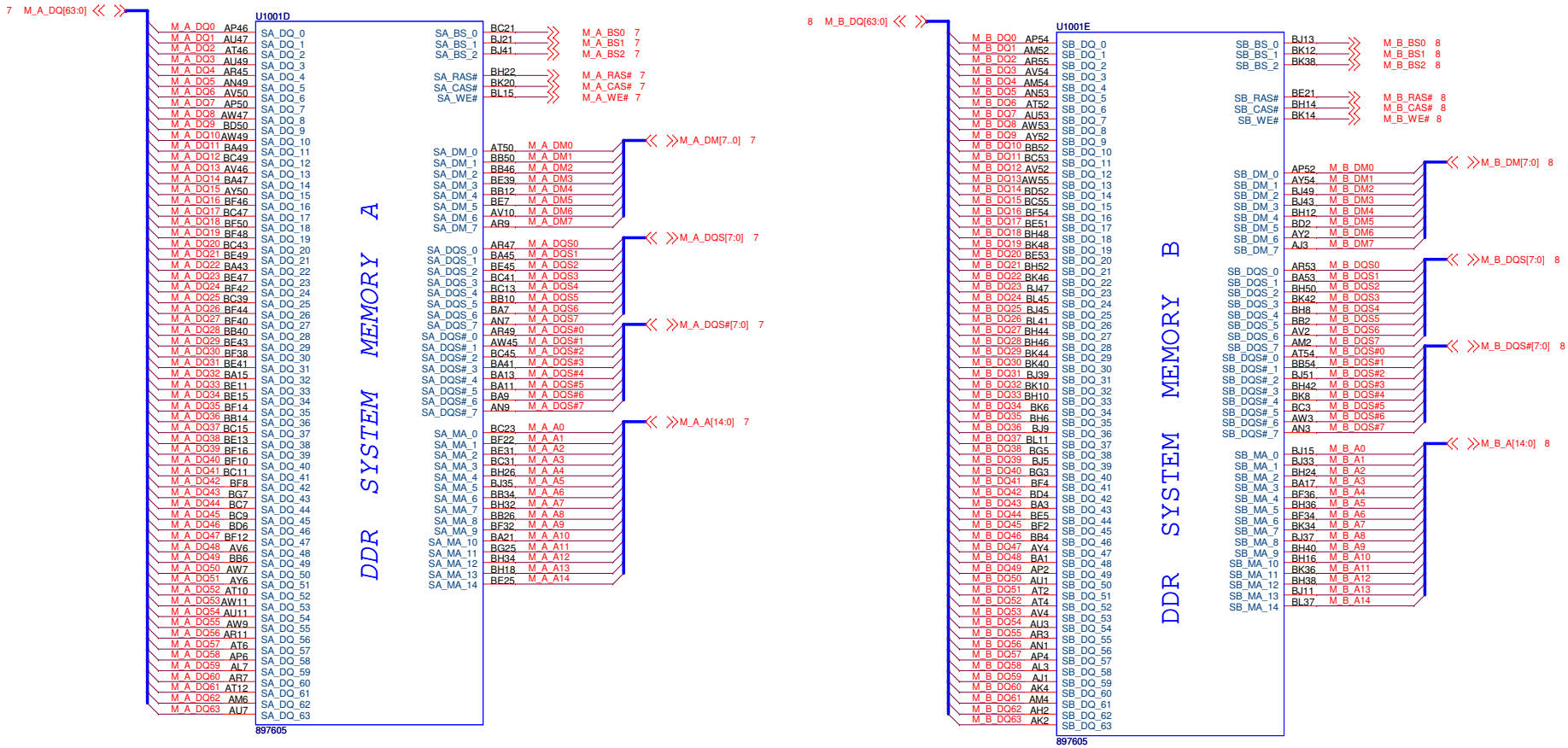
ASUSTeK COMPUTER INC.

Title : NB GS45 DISPLAY

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 12 of 97



<Variant Name>

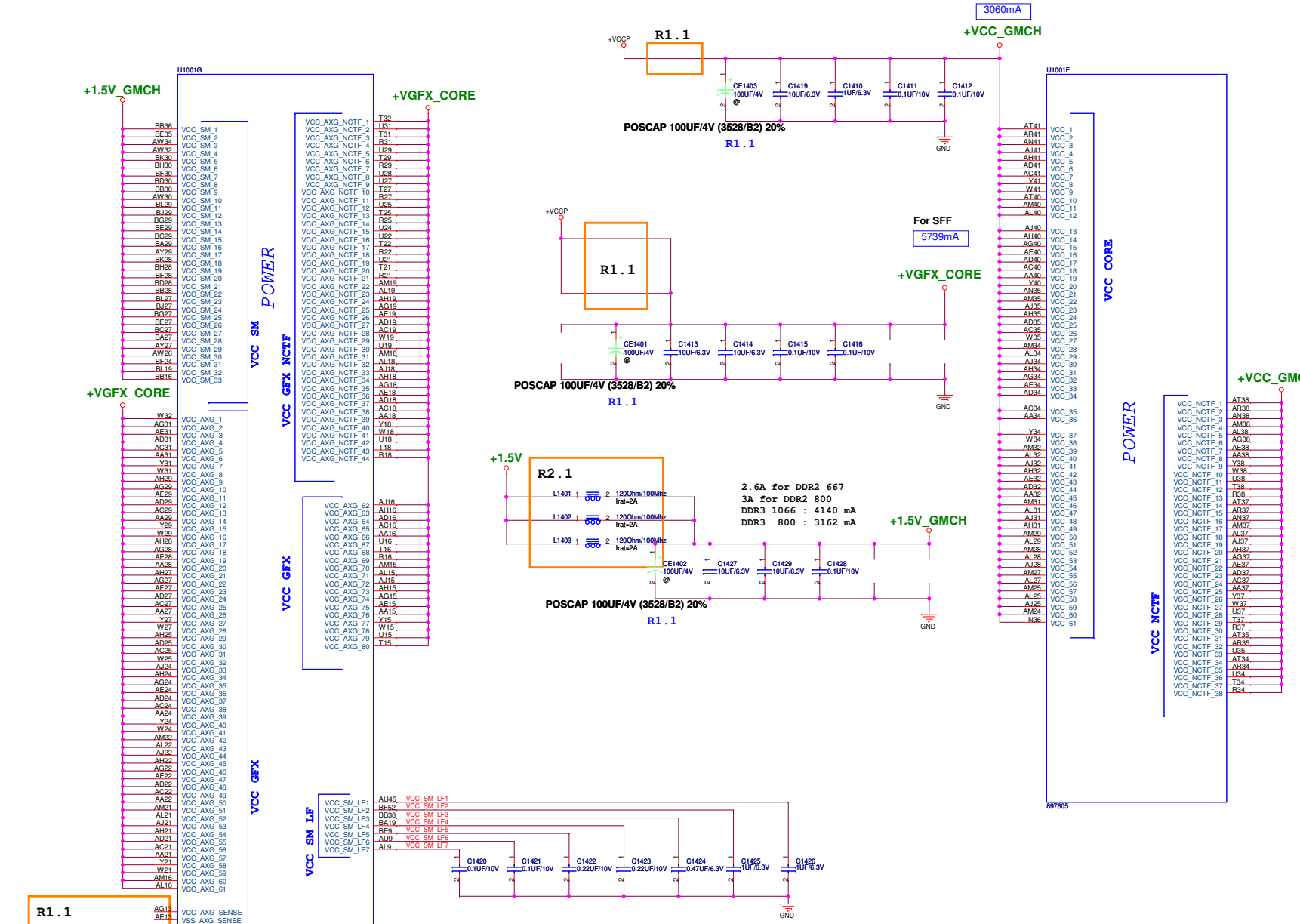
ASUSTeK COMPUTER INC.

Title : NB GS45 DDR3 BUS

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 13 of 97



<Variant Name>

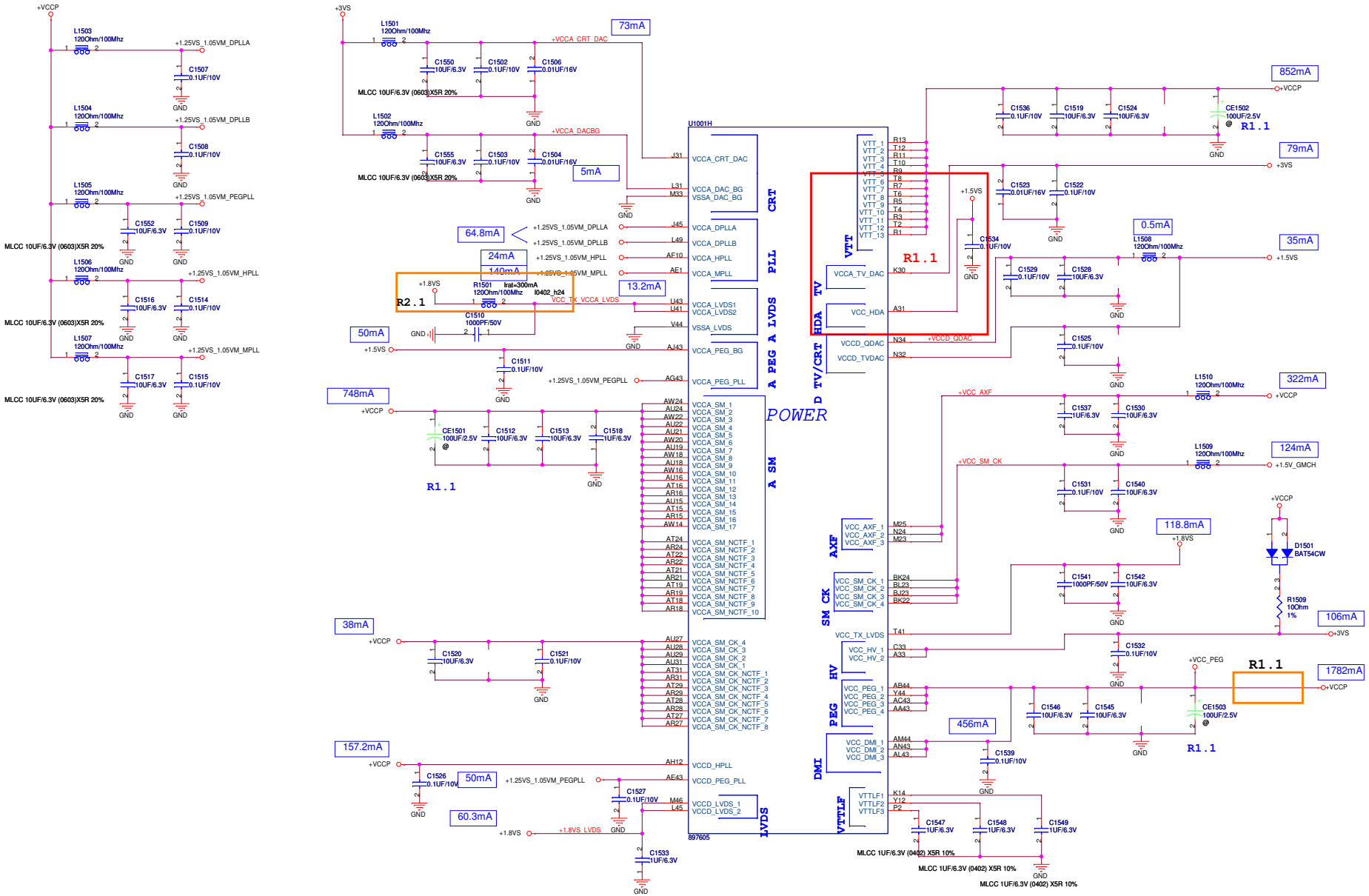
ASUSTeK COMPUTER INC.

Title : NB GS45 POWER

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 14 of 97



<Variant Name>

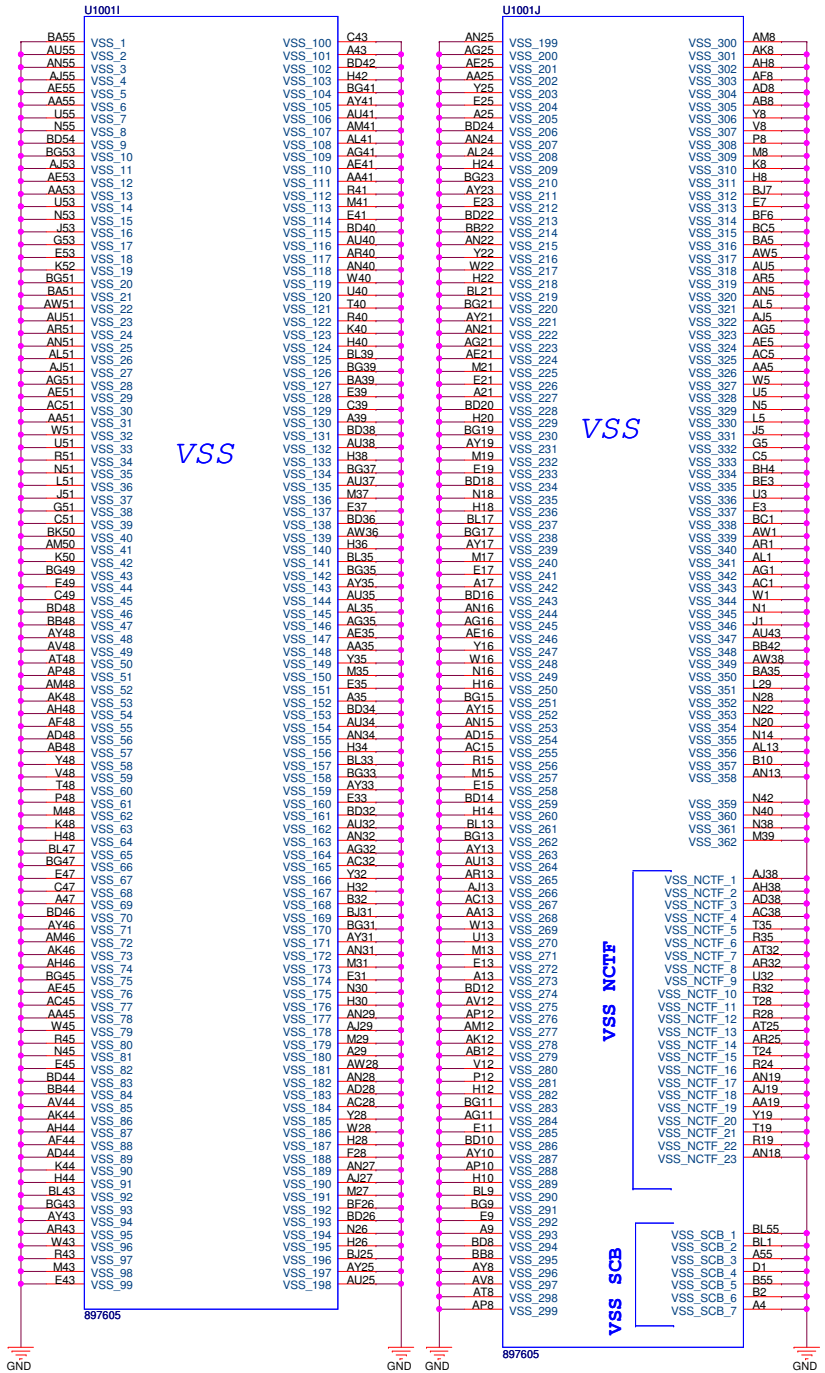
ASUSTeK COMPUTER INC.

Title : NB GS45 POWER

Engineer: Jack Hsu

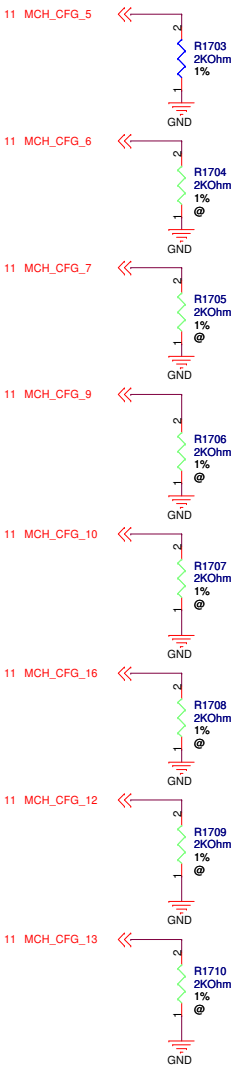
Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 15 of 97



<Variant Name>

ASUSTeK COMPUTER INC.	Title : NB GS45 GND	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 16 of 97	



CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2

CFG6 : ITPM Host Interface (Relate to SPI_MOSI)
H = ITPM Disable (Default)
L = ITPM enable(Can disable by SW)

CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality

CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse

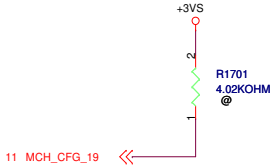
CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable

CFG16 : FSB Dynamic ODT
H =Enable (Default)
L = Disable

CFG12 : ALL-Z Mode
H =Disable (Default)
L = Enable

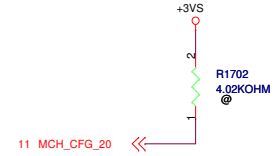
CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)



CFG19 : DMI Lane Reversal

H =DMI Lane Reversal
L = Normal (Default)



CFG20 : SDVO/PCIE CONCURRENT MODE

L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>

ASUSTeK COMPUTER INC.	Title : NB GS45 STRAPPING	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 17 of 97	

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 18 of 97

<Variant Name>

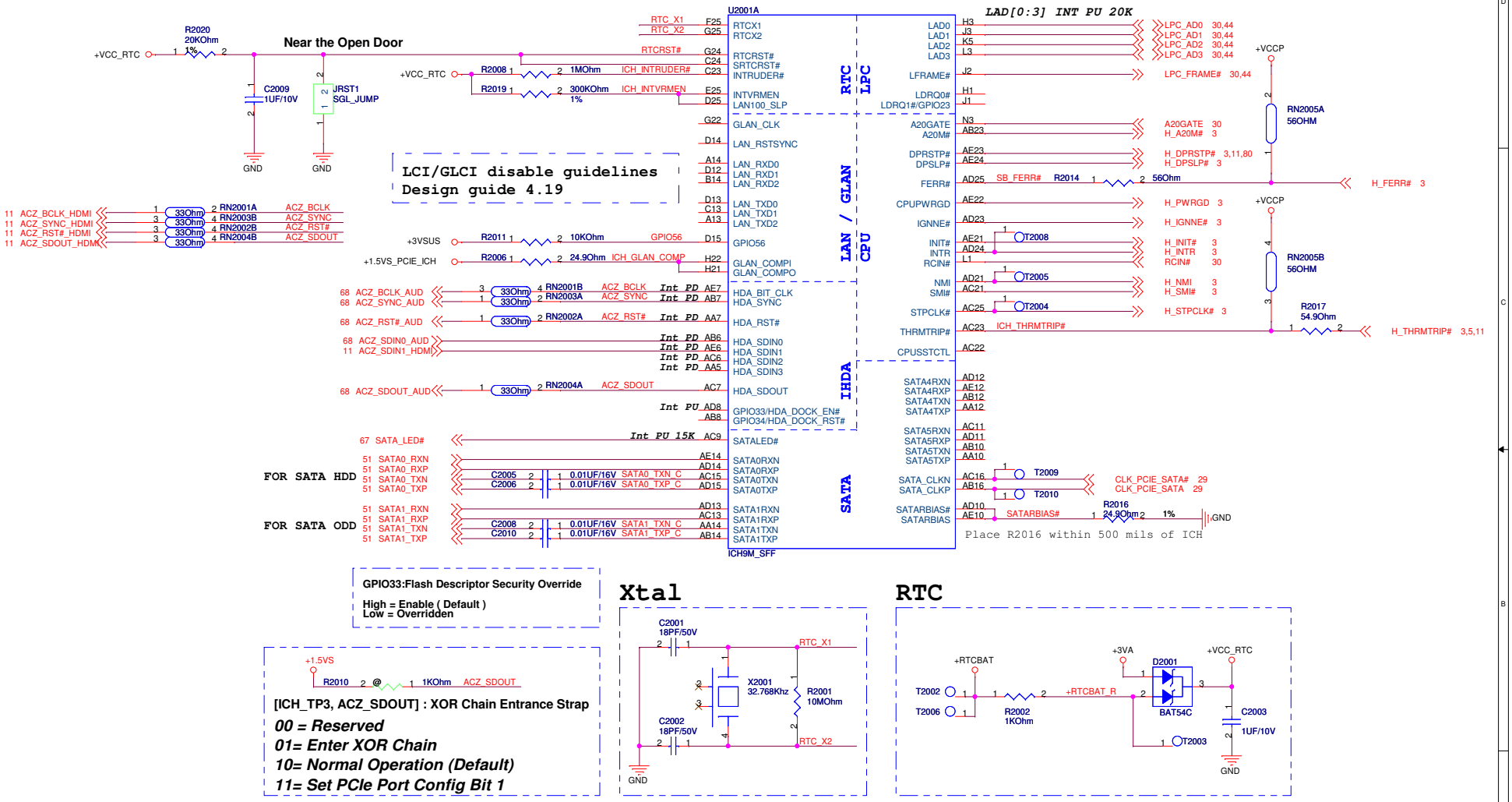
Title :

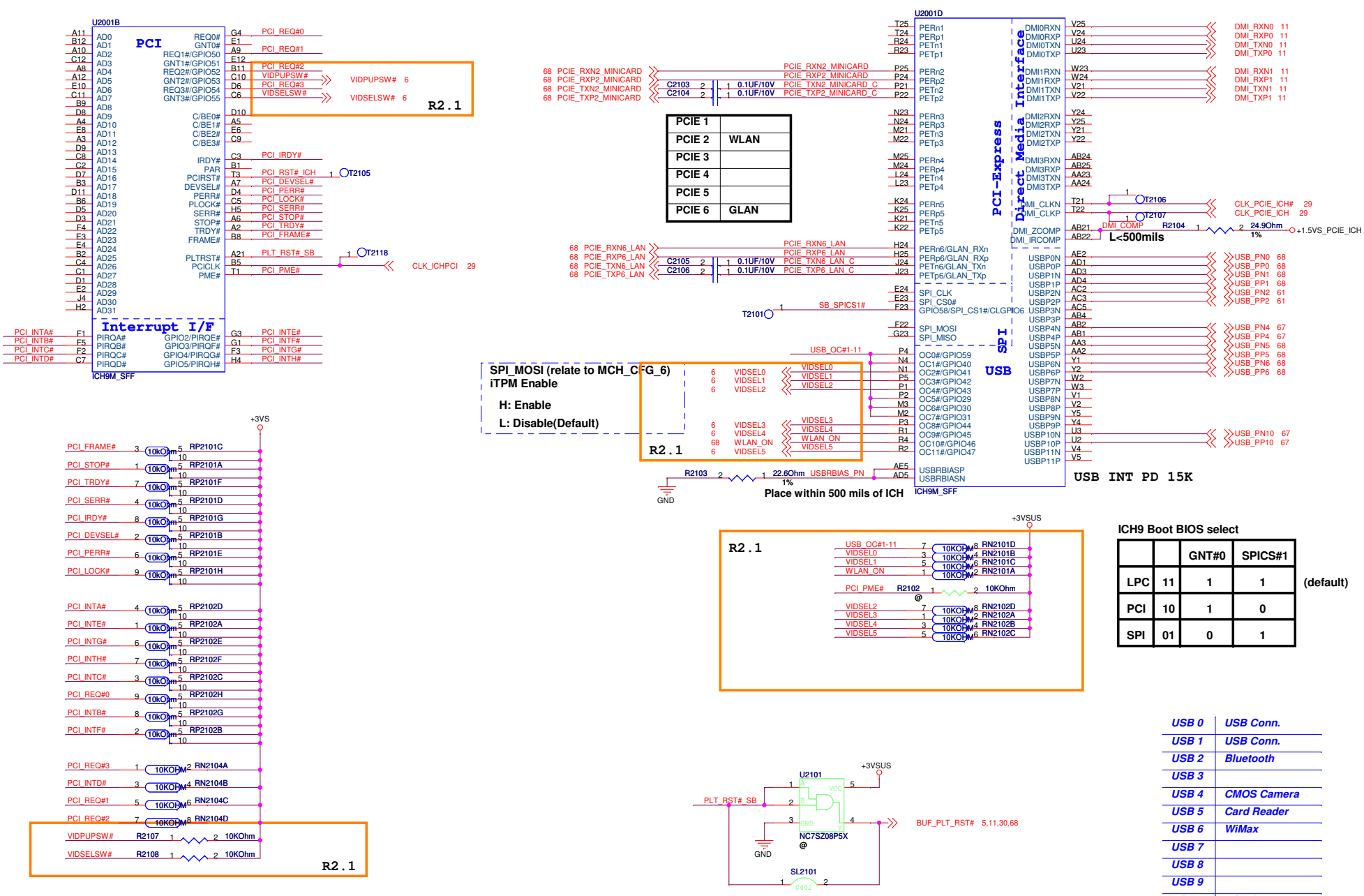
ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 19 of 97


Near the Open Door
LCI/GLCI disable guidelines
Design guide 4.19
LAD[0:3] INT PU 20K
U2001A
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
ICH9M_SFF
Place R2016 within 500 mils of ICH
FOR SATA HDD
FOR SATA ODD
GPIO33:Flash Descriptor Security Override
High = Enable (Default)
Low = Overridden
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
Xtal
RTC
Title : SB ICH9M (1)
ASUSTeK COMPUTER INC.
Engineer: Jack Hsu
Project Name
UL50AT
Rev
2.0
Date: Friday, October 16, 2009
Sheet 20 of 97



ICH9 Boot BIOS select

		GNT#0	SPICS#1	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Bluetooth
USB 3	
USB 4	CMOS Camera
USB 5	Card Reader
USB 6	WiMax
USB 7	
USB 8	
USB 9	
USB 10	USB Conn.
USB 11	

<Variant Name>

Title : SB ICH9M (2)

ASUSTeK COMPUTER INC. Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 21 of 97

SATA[X]GP unused need PU 10K to +3VS
(DG 4.2.6)

U2001C

SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STPPCI#/GPIO15
STPCPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP11
GPIO1/TACH1
GPIO6
GPIO7
GPIO8
GPIO12/LAN_PHY_PWR_CTRL
GPIO13
GPIO17
GPIO18
GPIO20
GPIO22/SCLOCK
GPIO27
GPIO28
SATACLKREQ#/GPIO35
GPIO38/SLOAD
GPIO39/SDATAOUT0
GPIO48/SDATAOUT1
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
TP8
TP9
TP10
ICH9M_SFF

SMB
sata GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC

GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA4GP
GPIO37/SATA5GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
GPIO26/S4_STATE#
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CL_PWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_ST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN

T2204 SM_LINK0
T2218 SM_LINK1
T2224 PM_SUS_STAT#
3 RSTCON#
11 PMSYNC#
30 EXT_SCI#
29 STP_PCI#
29,80 STP_CPU#
30 PM_CLKRUN#
68 PCIE_WAKE#
30 INT_SERIRQ
T2225 PM_THERM#_ICH
VR_PWRGD_CLKEN
T2226 HDMI_HP_ICH
30 EXT_SMI#
HDTV_DET#
67 WLAN_LED_ON
61 BT_ON/OFF#
67 BTLED_ON
29 CLK_REQ_SATA#
PCB_ID1
PCB_ID2
GPIO57
68 SB_SPKR
11 MCH_SYNC#

RSTCON#
SUS_PWRGD
RSTCON#
EXT_SCI#
STP_PCI#
STP_CPU#
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
PM_THERM#_ICH
EXT_SMI#
HDTV_DET#
WLAN_LED_ON
BT_DET#
PCB_ID1
PCB_ID2
SB_SPKR
MCH_SYNC#

R1.1

SPKR
No Reboot Strap
Low = Default
High = No Reboot

AE19 GPIO21 → T2228
AA18 EDID_HDMI_SELECT# → T2234
AE20 dGPU_PRSNT# → T2235
AA20 dGPU_RUNPWROK → T2236
K1 → T2203 → CLK_ICH14 29
AB5 → T2205 → CLK_USB48 29
R3 SUSCLK → T2223
D18 SLP_S3# → PM_SUSB# 30,46
B20 SLP_S4# → PM_SUSC# 30
D16 SLP_S5#
E14 SUS
D23 RTC PM_PWROK_R
M1 INT PD SB_DPRSLPVR → PM_DPRSLPVR 11,80
C16 BAT_LL#
U4 INT PU 20K → PM_PWRBTN# 30
D22 GND
D19 RTC PM_RSMRST#_R 1 10KOHM 2 RN2208A → PM_RSMRST# 30
U1 SUS → CLK_PWRGD 29
T4 PM_PWROK_R
B23 1 T2213
C22 INT PU → CL_CLK0 11
A18 INT PU
F22 INT PU → CL_DATA0 11
B18 INT PU
F21 CL_VREF0
A17
C17 INT PU → CL_RST#0 11
B17 INT PU
A22 SUS
E16 SUS
A15 SUS AC_PRESENT
D21 SUS R2205 1 @ 2 100KOhm R2206 1 2 100KOhm +3VSUS
GND

R1.1
CL1 not required if IAMT disable
DG 4.8

Follow DesignIP
Follow M51Va

+3VS
PM_CLKRUN# 1 10KOHM 2 RN2206A
HDMI_HP_ICH 7 10KOHM 8 RN2206D
PM_THERM#_ICH 3 10KOHM 4 RN2206B
GPIO21 5 10KOHM 6 RN2206C
EDID_HDMI_SELECT# 1 10KOHM 2 RN2207A
INT_SERIRQ 3 10KOHM 4 RN2207B
SB_SPKR R2216 1 2 1KOhm @
STP_PCI# 1 10KOHM 2 RN2201A @
STP_CPU# 3 10KOHM 4 RN2201B @
dGPU_PRSNT# 1 10KOHM 2 RN2210A @
dGPU_RUNPWROK 3 10KOHM 4 RN2210B @

R1.1

+3VSUS
LINKALERT# 1 10KOHM 2 RN2203A
SM_LINK1 7 10KOHM 8 RN2204D
SM_LINK0 5 10KOHM 6 RN2203C
PM_RI# 3 10KOHM 4 RN2203B
EXT_SCI# 5 10KOHM 6 RN2204C
EXT_SMI# 7 10KOHM 8 RN2203D
PCIE_WAKE# 1 10KOHM 2 RN2204A
BAT_LL# 3 10KOHM 4 RN2204B
AC_PRESENT 5 10KOHM 6 RN2207C
WLAN_LED_ON 7 10KOHM 8 RN2207D
GND

+3VSUS
RSTCON# R2201 1 2 10KOhm
HDTV_DET# @ R2203 1 2 10KOhm
+3VS
BT_DET# @ R2214 1 2 10KOhm

R2.0

+3VS +3VS
R2222 10KOhm @ R2223 10KOhm @
PCB_ID1
PCB_ID2
R2225 10KOhm R2226 10KOhm
GND

PCB ID	GPIO38	GPIO39
UL50A	0	0
UL50V	0	1

+3VSUS
R2231 10KOhm
R2241 10KOhm @
VR_PWRGD_CLKEN
VRM_PWRGD 30,80,92
Q2201 2N7002
CLK_EN# 80
GND

+3VSUS
R2204 @ 10KOhm
R2217 100KOhm
GPIO57
GND

+3VS
R2227 2.37KOHM 1%
CL_VREF0
C2201 0.1UF/10V
R2228 330Ohm
GND

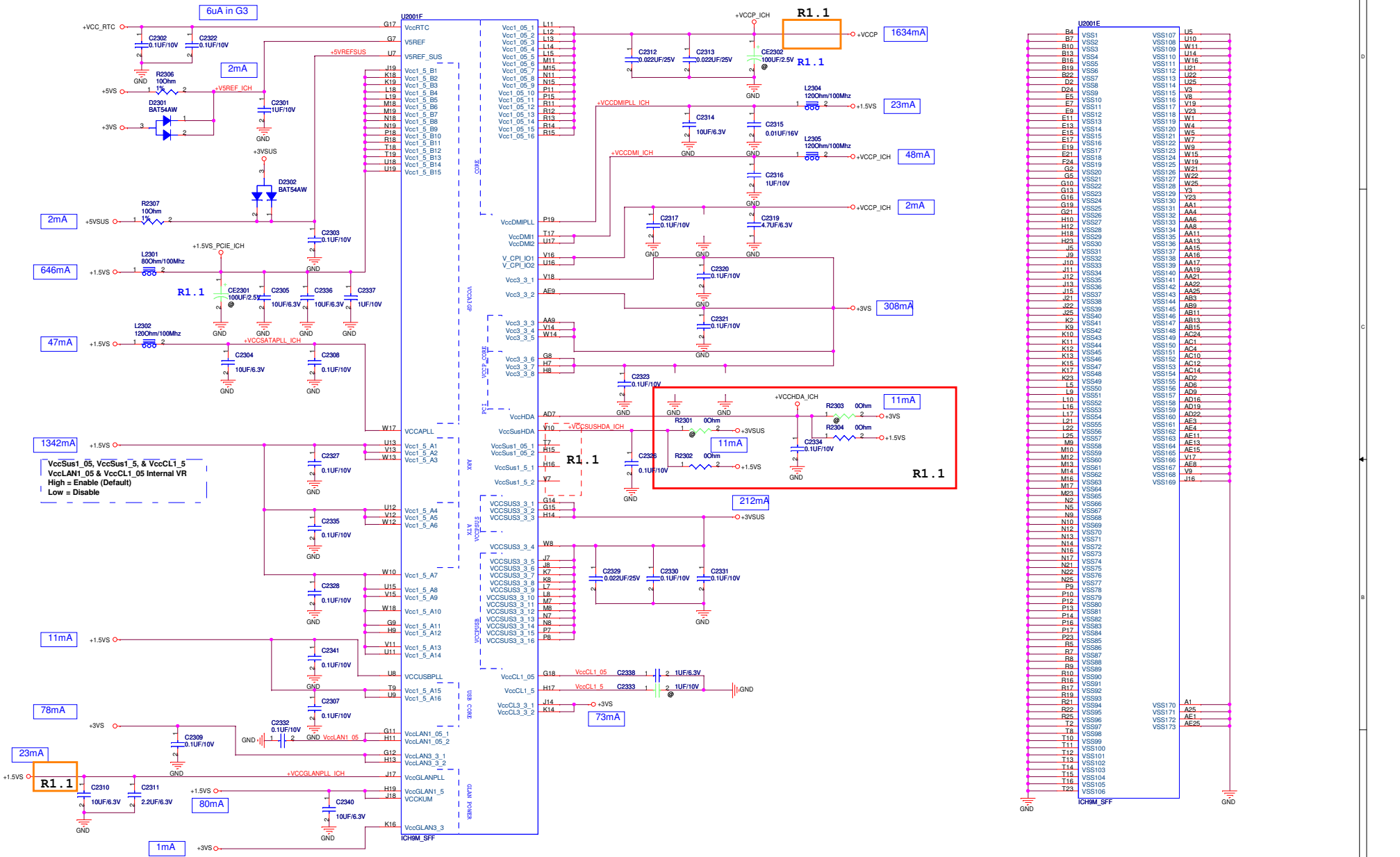
CL_VREF0 routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out = 5 mils on 5 mils for 300 mils max

+3VSUS
RN2209A 4.7KOhm
RN2209C 4.7KOhm
+12VS
+3VS
RN2209D 4.7KOhm
RN2209B 4.7KOhm
SCL_3A
Q2202A UM6K1N
SMB_CLK_S 7,8,24,29
SDA_3A
Q2202B UM6K1N
SMB_DAT_S 7,8,24,29

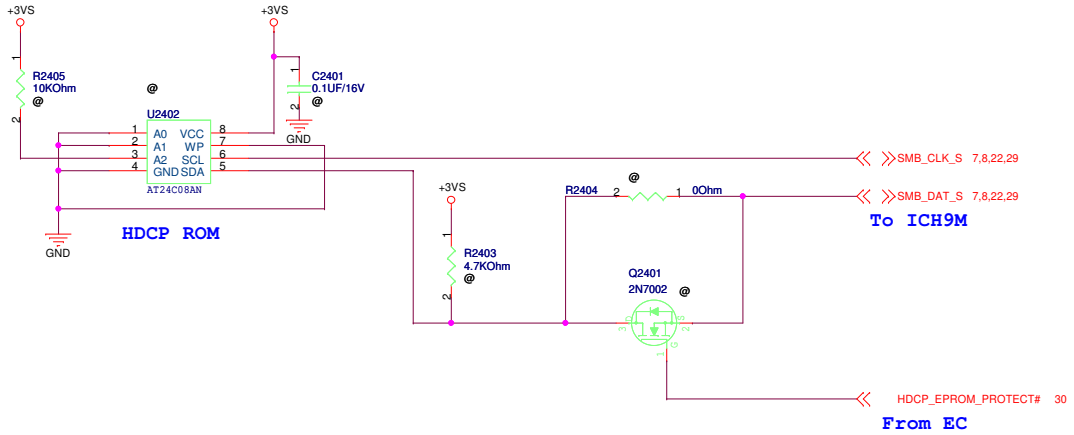
11,30 PM_PWROK
RN2208B 10KOHM
PM_RSMRST#_R
PM_PWROK_R
D2201 BAT54CW
SUS_PWRGD 30,81,92
R2230 10KOhm @
GND

<Variant Name>

ASUSTeK COMPUTER INC.
Title: SB ICH9M (3)
Engineer: Jack Hsu
Size: Custom
Project Name: UL50AT
Rev: 2.0
Date: Friday, October 16, 2009
Sheet 22 of 97



<Variant Name>
ASUSTeK COMPUTER INC.
Title : SB ICH9M (4)
Engineer: Jack Hsu
Size: C
Project Name: UL50AT
Rev: 2.0
Date: Friday, October 16, 2009
Sheet 23 of 97



<Variant Name>

ASUSTeK COMPUTER INC.	Title : SB ICH9M (5)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 24 of 97	

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 25 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 26 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 27 of 97

<Variant Name>

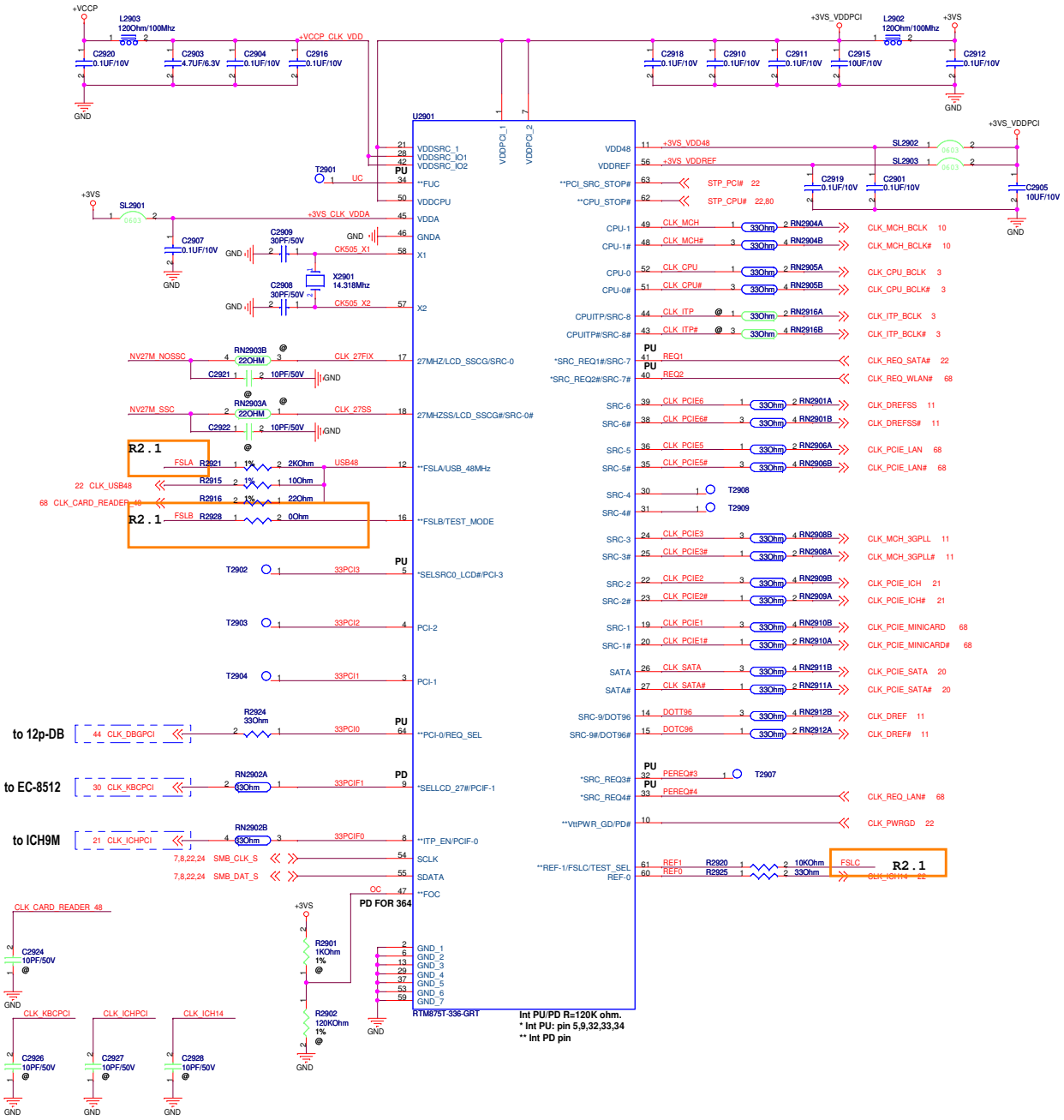
Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

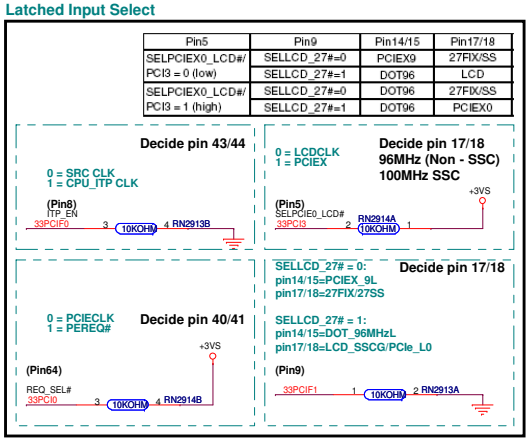
Size	Project Name	Rev
C	UL50AT	2.0

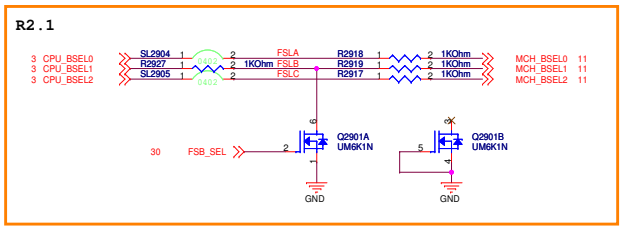
Date: Friday, October 16, 2009 Sheet 28 of 97



Latched Input Select

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIEX0_LCD#/ PCI3 = 0 (low)	SELLCD_27#=0	PCIEX9	27FIX/SS
	SELLCD_27#=1	DOT96	LCD
SELPCIEX0_LCD#/ PCI3 = 1 (high)	SELLCD_27#=0	DOT96	27FIX/SS
	SELLCD_27#=1	DOT96	PCIEX0





BCLK	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

<Variant Name>

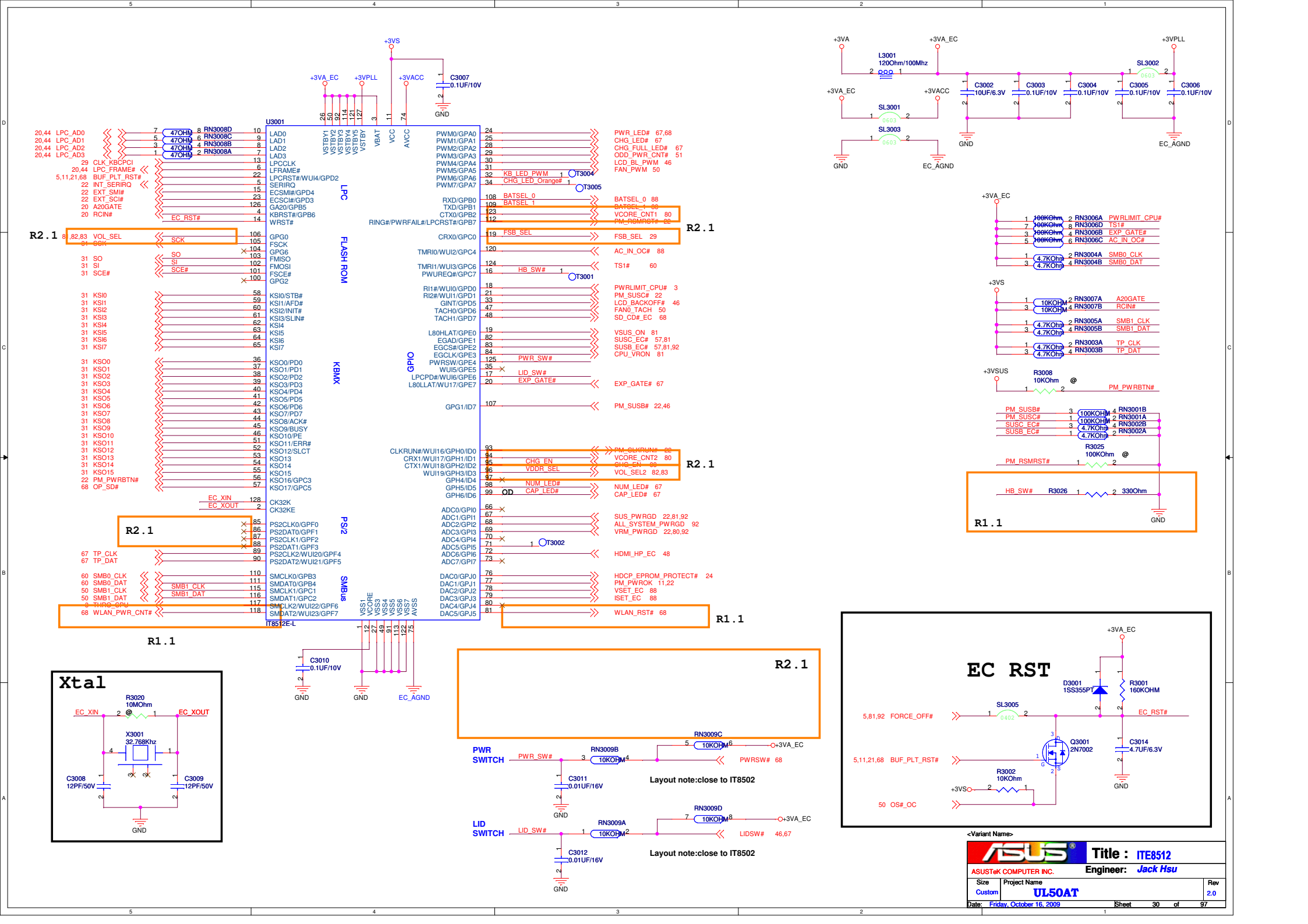
ASUSTeK COMPUTER INC.

Title : RTM875T-336-GRT

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 29 of 97


U3001
IT8512E-L
LPC
FLASH ROM
KBMX
GPIO
PS/2
SMBus
R2.1
R1.1
Xtal
X3001
32.768Khz
R3020
10MOhm
C3008
12PF/50V
C3009
12PF/50V
EC RST
D3001
1SS355PT
R3001
160KOHM
Q3001
2N7002
C3014
4.7UF/6.3V
R3002
10KOhm
PWR SWITCH
LID SWITCH
Layout note:close to IT8502
Title : ITE8512
ASUSTeK COMPUTER INC.
Engineer: Jack Hsu
Project Name
UL50AT
Rev
2.0
Date: Friday, October 16, 2009
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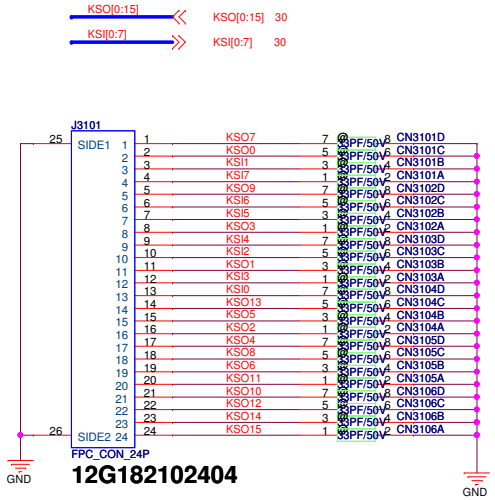
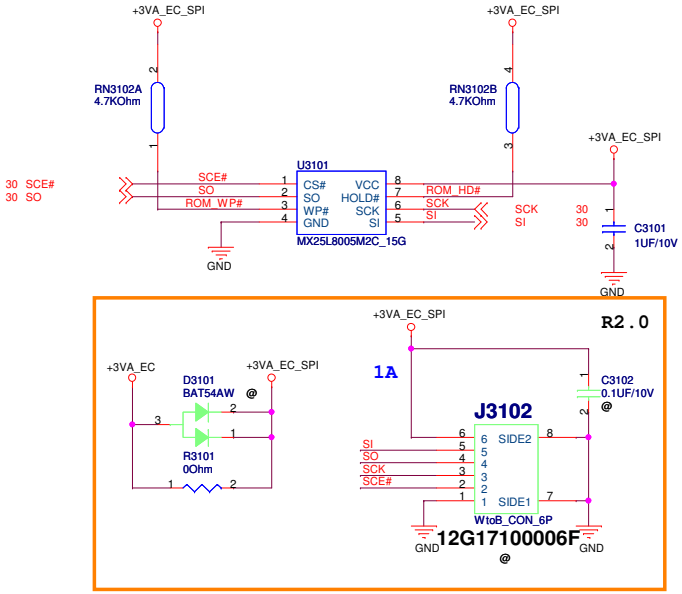
Internal Keyboard



SPI Flash ROM (8Mb)



<Variant Name>

ASUSTeK COMPUTER INC.	Title : KB & SPI ROM	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 31 of 97	

<Variant Name>

Title: <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 32 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 33 of 97

<Variant Name>

Title :<Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 34 of 97

<Variant Name>

Title :<Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 35 of 97

<Variant Name>

Title :<Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 36 of 97

<Variant Name>

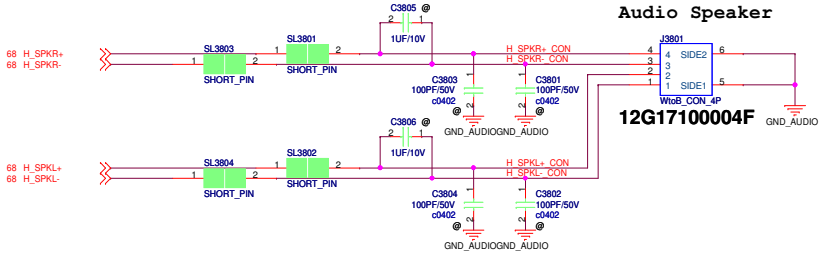
Title :<Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 37 of 97



<Variant Name>

ASUSTeK COMPUTER INC.

Title : Internal Speaker

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 38 of 97

<Variant Name>

Title :<Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 39 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 40 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 41 of 97

<Variant Name>

Title :<Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 42 of 97

<Variant Name>

Title :<Title>

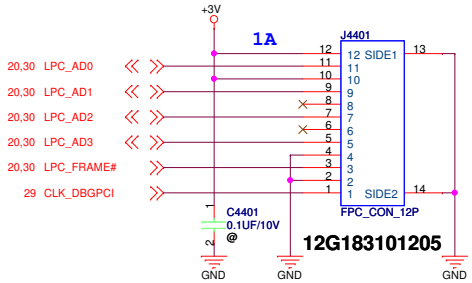
ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 43 of 97

LPC DEBUG PORT



<Variant Name>

ASUSTeK COMPUTER INC.	Title : DEBUG PORT	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 44 of 97	

<Variant Name>

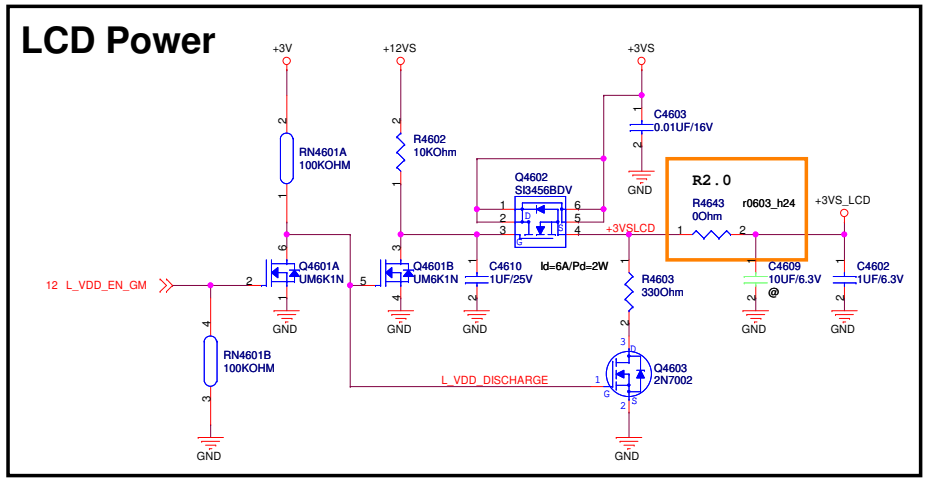
Title :<Title>

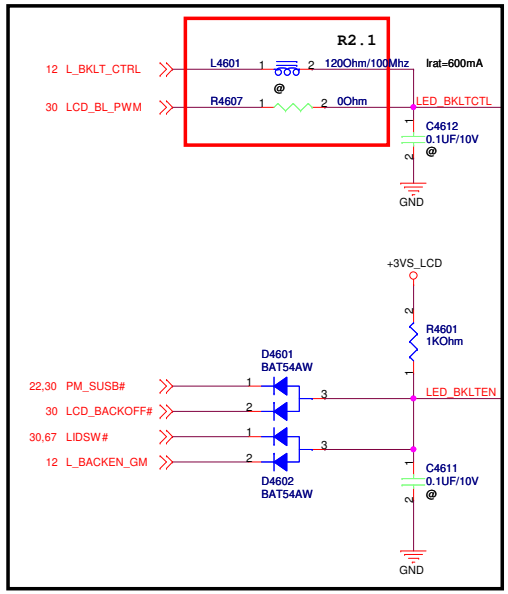
ASUSTeK COMPUTER INC.

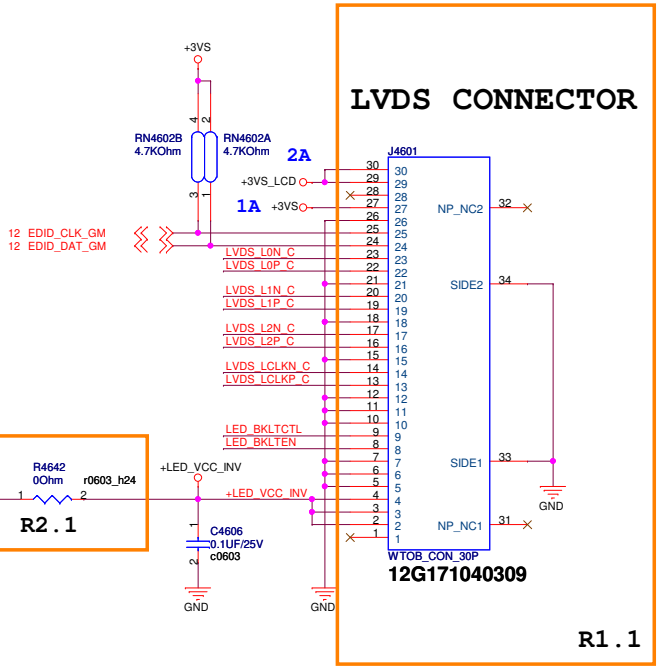
Engineer: Jack Hsu

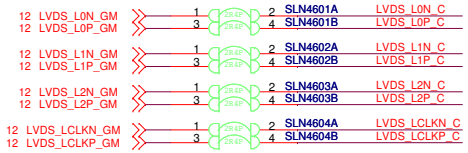
Size	Project Name	Rev
C	UL50AT	2.0

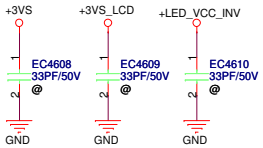
Date: Friday, October 16, 2009 Sheet 45 of 97











<Variant Name>

ASUSTeK COMPUTER INC.	Title : LVDS CONNECTOR	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 46 of 97	

<Variant Name>

Title :<Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 47 of 97

<Variant Name>

ASUSTeK COMPUTER INC.

Title : Hybrid Switch

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 48 of 97

<Variant Name>

Title : HDMI LEVEL SHIFT

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 49 of 97

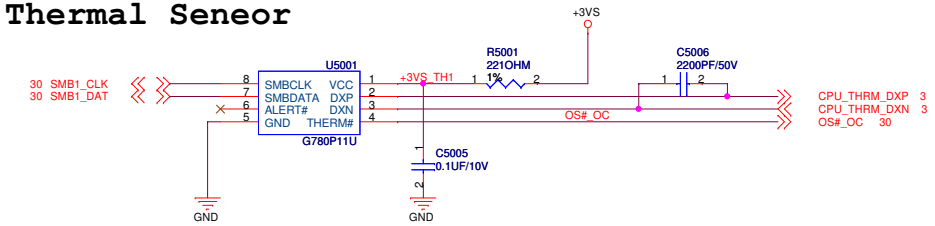
1nd: 06G023096010 G780P11U SOP-8
2nd: 06G023026012 MAX6657YMS+ SOP-8

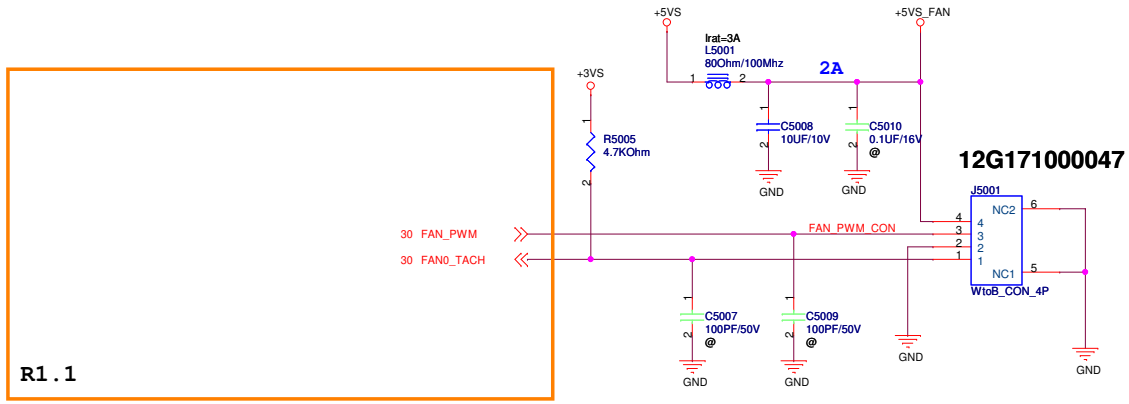
Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
10 mils
----------OTHER SIGNALS

Avoid FSB,Power

Thermal Seneor





<Variant Name>

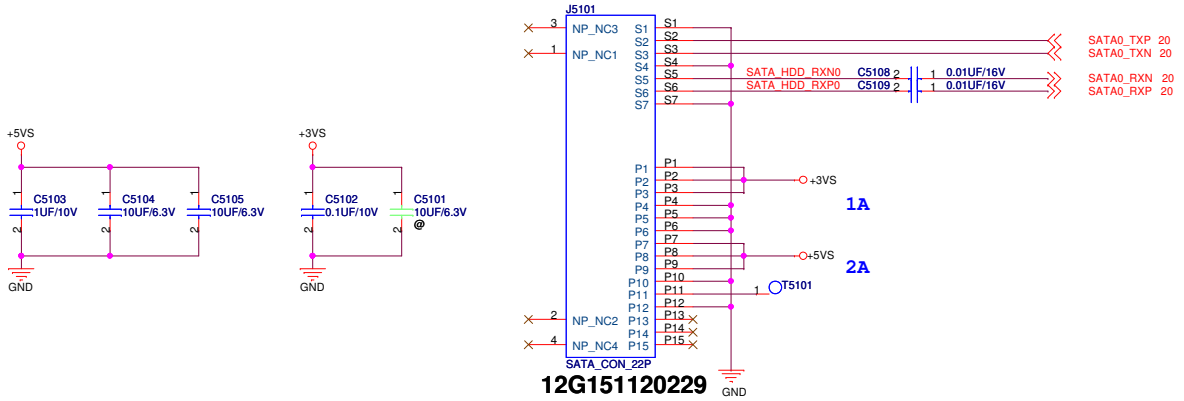
Title : THERMAL & FAN

ASUSTeK COMPUTER INC. Engineer: Jack Hsu

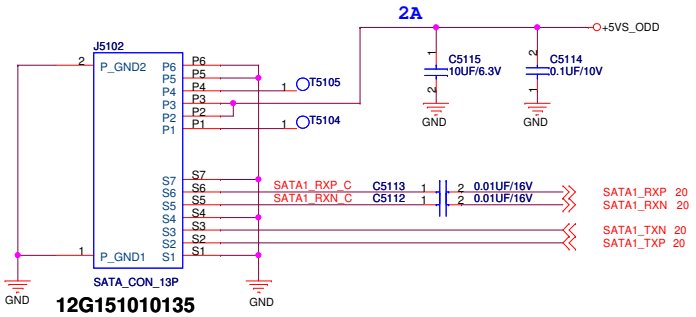
Size	Project Name	Rev
Custom	UL50AT	2.0

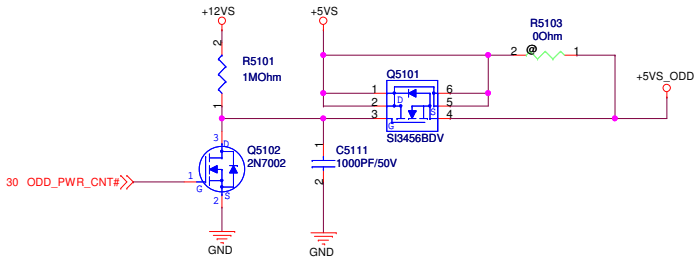
Date: Friday, October 16, 2009 Sheet 50 of 97

SATA HDD



SATA ODD





<Variant Name>

ASUSTeK COMPUTER INC.	Title : SATA HDD & ODD	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 51 of 97	

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 52 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 53 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 54 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 55 of 97

<Variant Name>

Title : LID

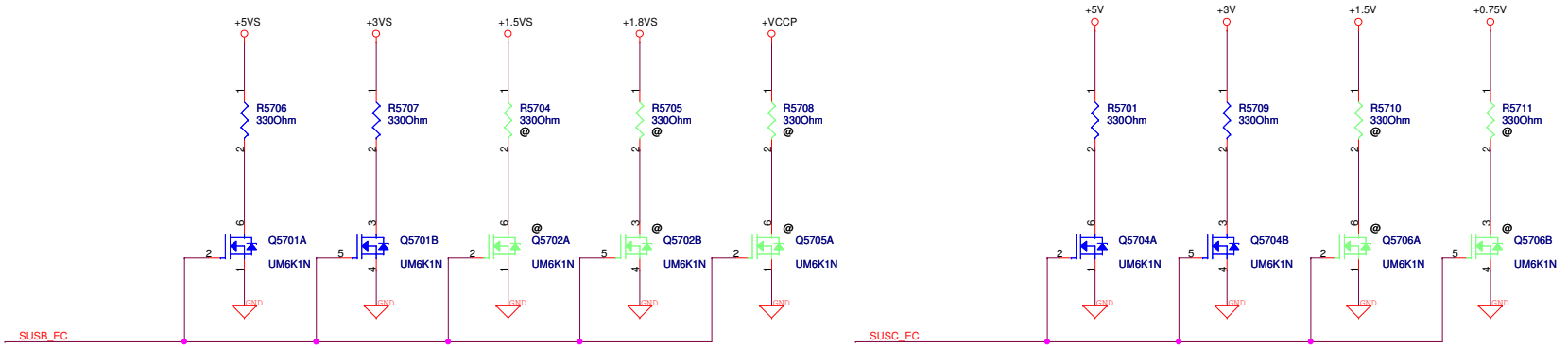
ASUSTeK COMPUTER INC.

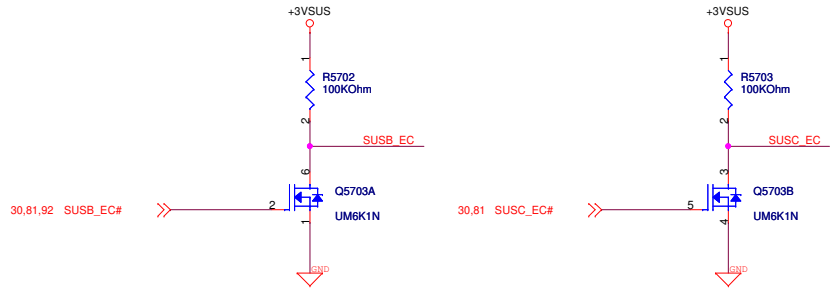
Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 56 of 97

Discharge Circuit





<Variant Name>

ASUSTeK COMPUTER INC.	Title DISCHARGE CIRCUIT	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 57 of 97	

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 58 of 97

<Variant Name>

Title :

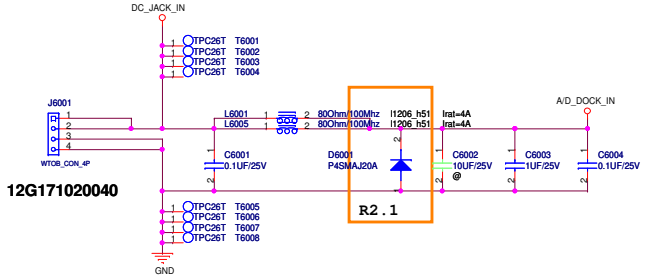
ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

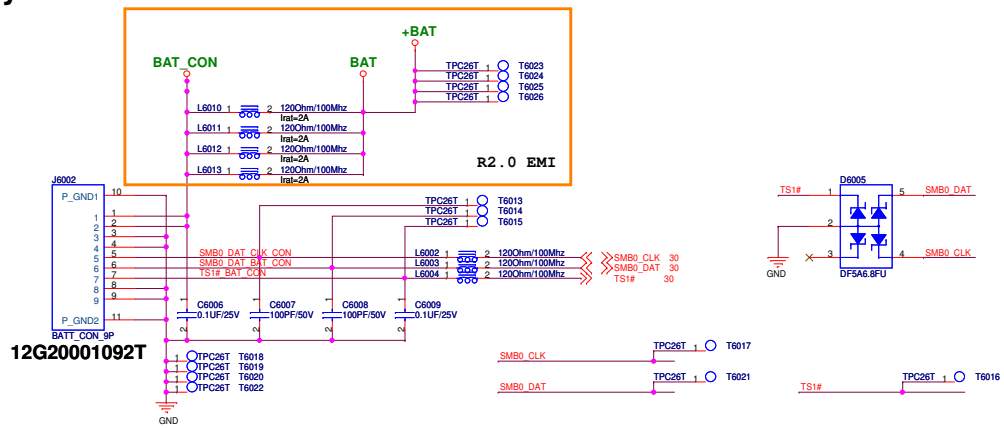
Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 59 of 97

DC-IN

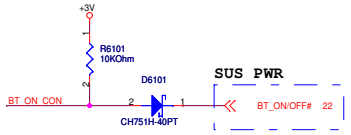


Battery Connector



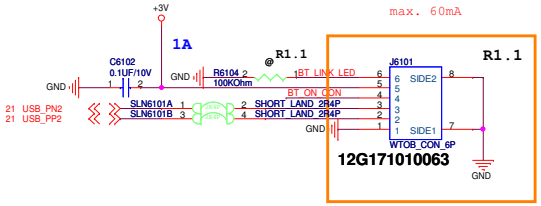
<Variant Name>

ASUSTeK COMPUTER INC.	Title : DC IN & BAT IN	
	Engineer: Jack Hsu	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 60 of 97	



Bluetooth Connector

max. 60mA



<Variant Name>

ASUSTeK COMPUTER INC.

Title : BlueTooth

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 61 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 62 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 63 of 97

<Variant Name>

Title : <Title>

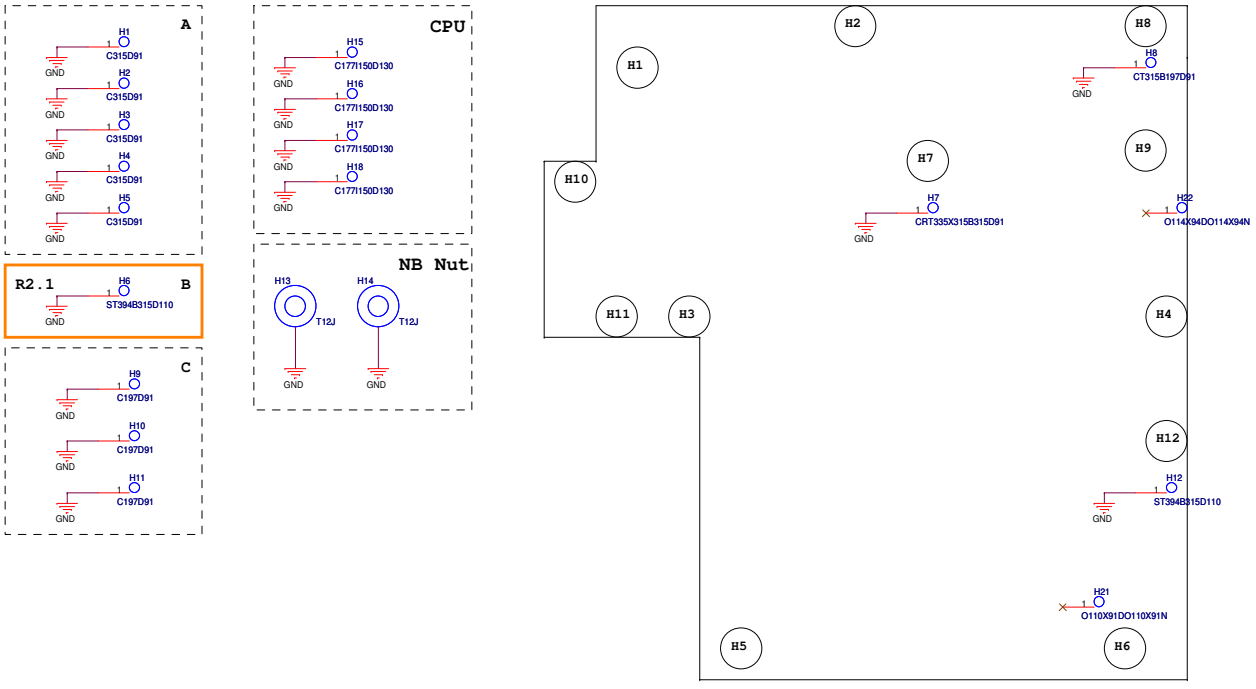
ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 64 of 97

Screw Hole & SMT Nut



<Variant Name>

ASUSTeK COMPUTER INC.

Title : SCREW HOLE & NUT

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 65 of 97

<Variant Name>

Title :

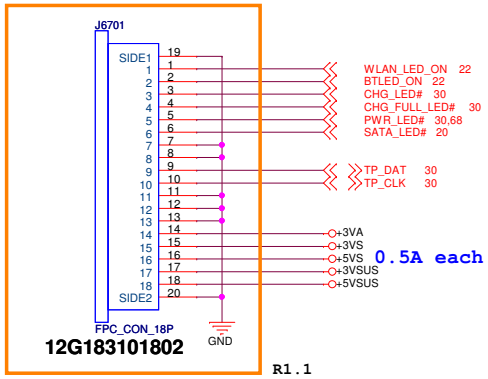
ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

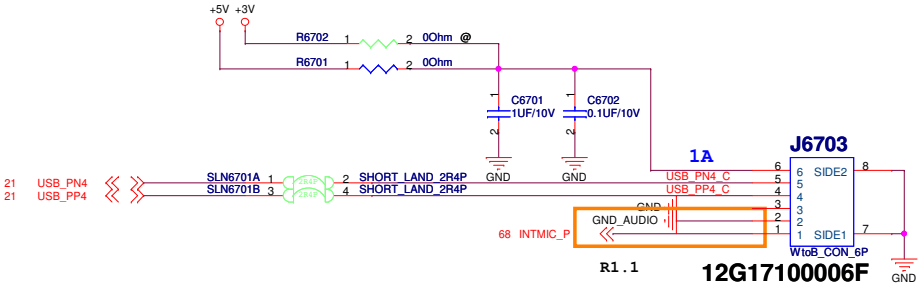
Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 66 of 97

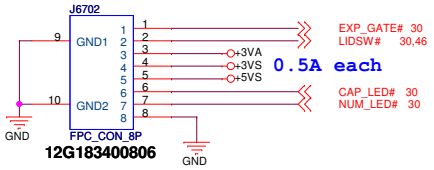
Touch Pad / LED Board

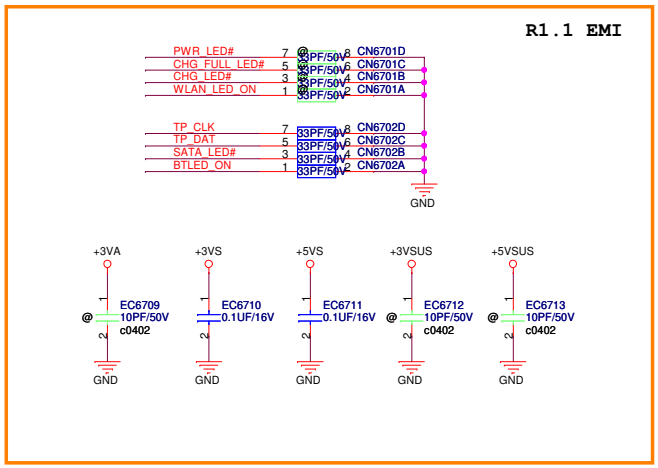


Camera Module

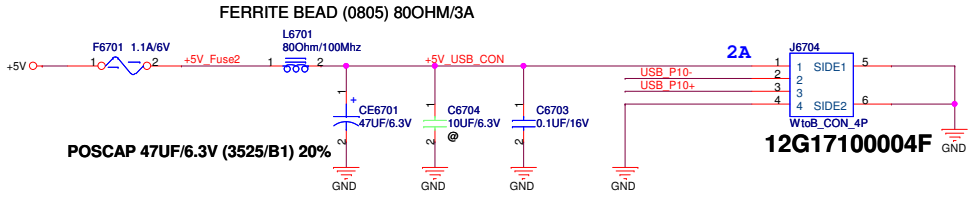


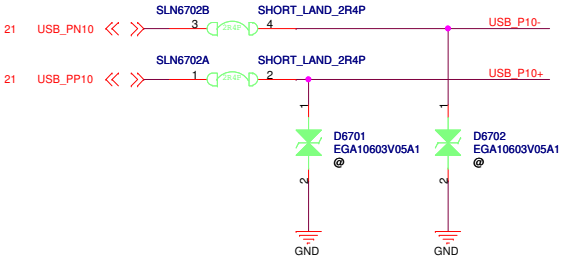
Function Board

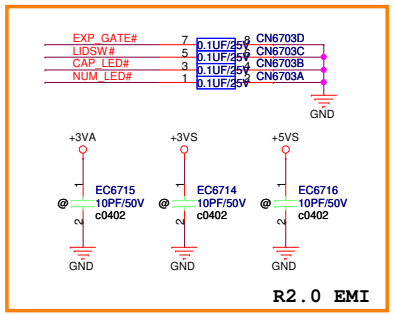


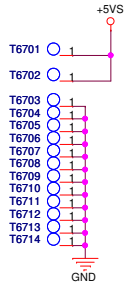


FLY USB Cable







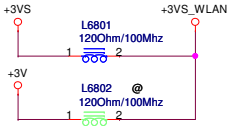


<Variant Name>

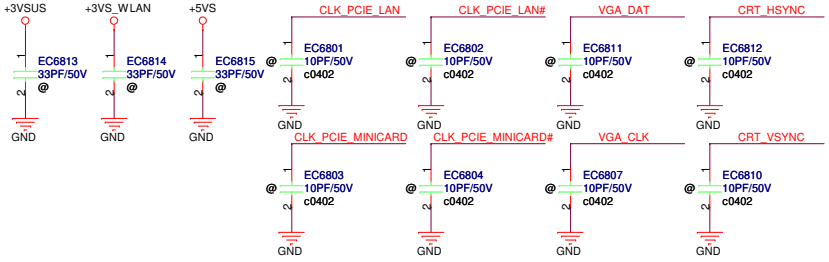
ASUSTeK COMPUTER INC.	Title : SUB BOARD	
	Engineer: Jack Hsu	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 67 of 97	

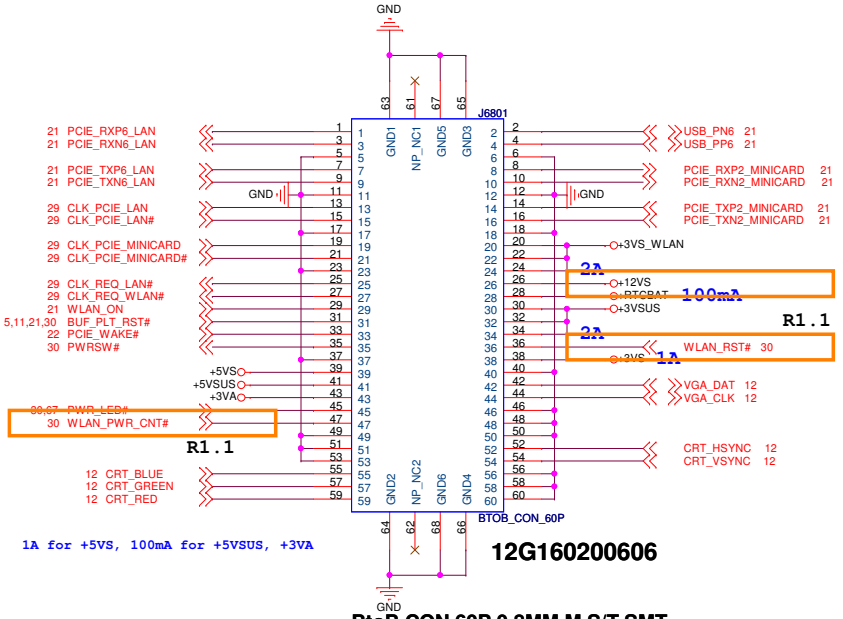
IO BOARD – 02

LAN IC
RJ45
CRT
RTC Conn.
MiniCard



WLAN Power Source Selection





1A for +5VS, 100mA for +5VSUS, +3VA

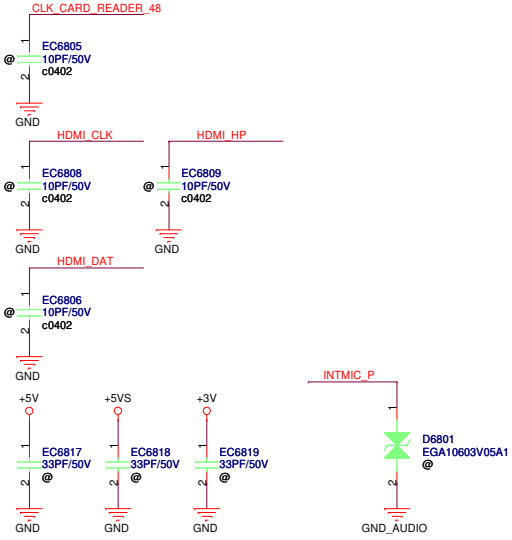
12G160200606

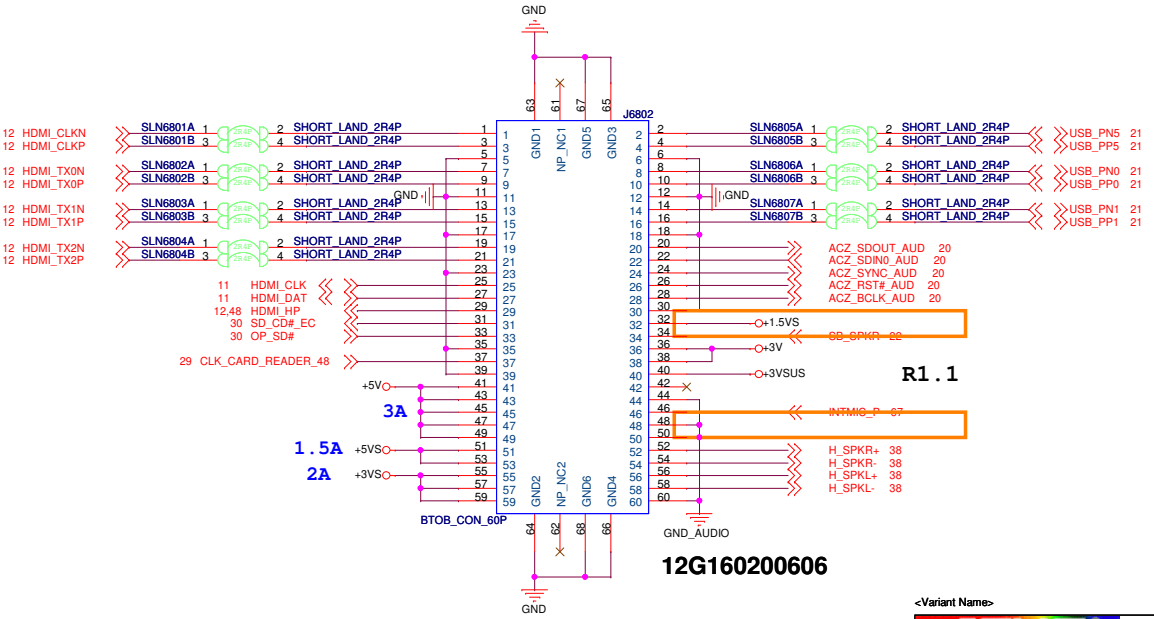
BtoB CON 60P,0.8MM,M,S/T,SMT

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Bluetooth
USB 3	
USB 4	CMOS Camera
USB 5	Card Reader
USB 6	WiMax
USB 7	
USB 8	
USB 9	
USB 10	USB Conn.
USB 11	

IO BOARD – 01

HDMI Conn.
USB Conn.x2
MIC-IN Conn.
Head Phone Conn.
Audio IC
Card Reader IC
Card Reader Conn.





12G160200606

BtoB CON 60P,0.8MM,M,S/T,SMT

<Variant Name>

ASUSTeK COMPUTER INC.

Title : B TO B CONNECTOR

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 68 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
C	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 69 of 97

ASUSTeK COMPUTER INC.		Title : M10M-GE1 (1)	
		Engineer: Alan Chen	
Size: C	Project Name: <Variant Name> UL50AT		Rev: 2.0
Date: Friday, October 16, 2009		Sheet 70 of 97	

ASUSTeK COMPUTER INC.		Title : M10M-GE1 (2)	
		Engineer: Alan Chen	
Size: C	Project Name: UL50AT		Rev: 2.0
Date: Friday, October 16, 2009		Sheet 71 of 97	

ASUSTeK Computer Inc.	Title : M10M-GE1 (3)		
	Engineer: Alan Chen		
Size: C	Project Name: UL50AT		Rev: 2.0
Date: Friday, October 16, 2009	Sheet 72 of 97		

ASUSTeK COMPUTER INC.	Title : M10M-GE1 (4)		
	Engineer: Alan Chen		
Size: C	Project Name: UL50AT		Rev: 2.0
Date: Friday, October 16, 2009	Sheet 73 of 97		

ASUSTeK COMPUTER INC.		Title : M10M-GE1 (5)	
		Engineer: Alan Chen	
Size: C	Project Name: UL50AT		Rev: 2.0
Date: Friday, October 16, 2009		Sheet 74 of 97	

Variant Name:

Title : N10M-GE1 (6)

ASUSTeK COMPUTER INC.

Engineer: Alan Chen

Size	Project Name	Rev
C	UL50AT	2.0

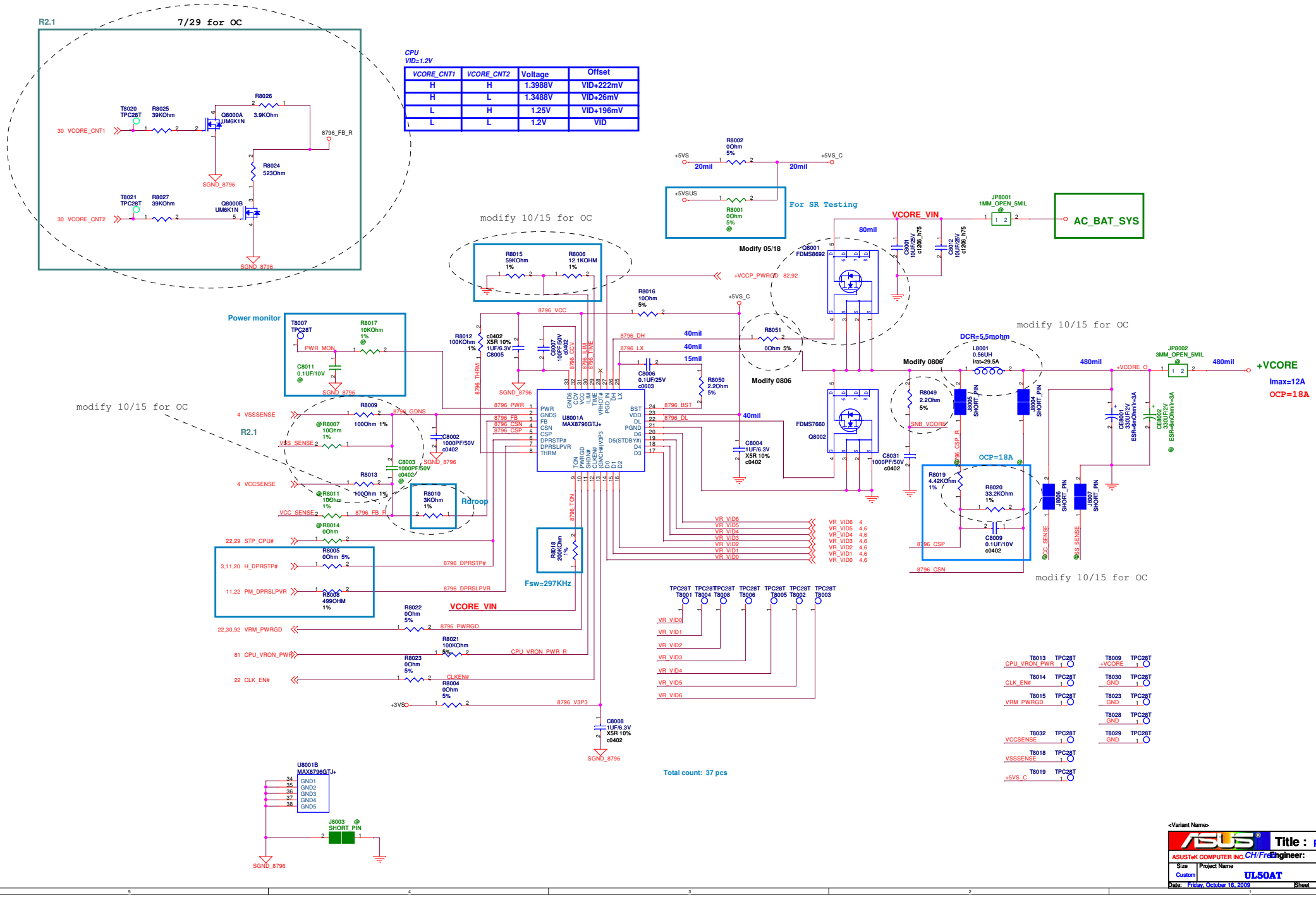
Date: Friday, October 16, 2009 Sheet 75 of 97

Title	VGA Power Sequence
ASUSTeK COMPUTER INC.	Engineer: Alan Chen
Size: C	Project Name: UL50AT
Rev: 2.0	
Date: Friday, October 16, 2009	Sheet 76 of 97

ASUSTeK COMPUTER INC.	Title: <Title>	
	Engineer: Alan Chen	
Size: C	Project Name: UL50AT <Variant Name>	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 77 of 97	

ASUSTeK COMPUTER INC.	Title: <Title>	
	Engineer: Alan Chen	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 78 of 97	

ASUSTeK COMPUTER INC.	Title: <Title>	
	Engineer: Alan Chen	
Size: C	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 79 of 97	



<Variant Name>

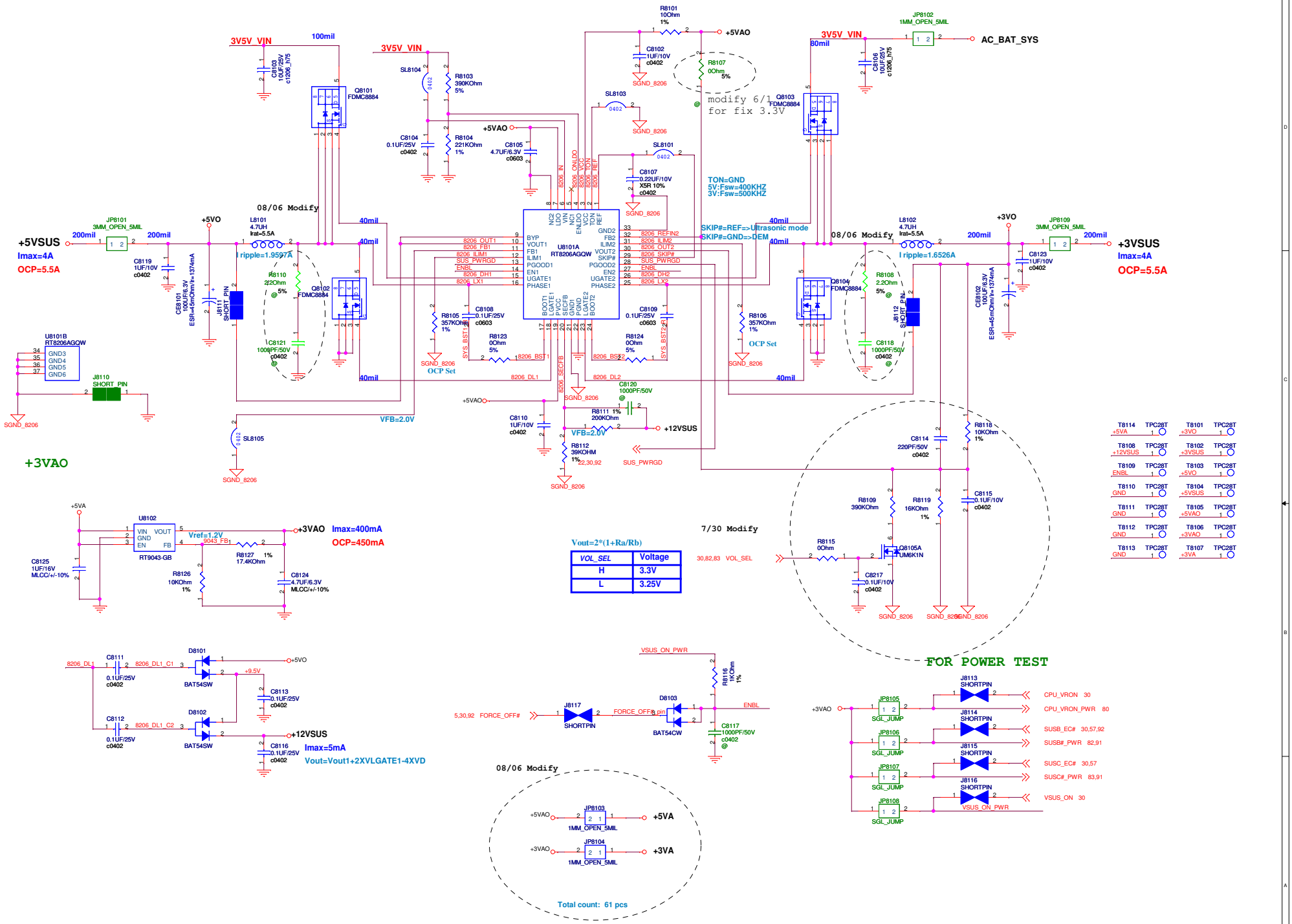
ASUSTeK COMPUTER INC.

Title : POWER_VCORE

Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 80 of 97



<Variant Name>

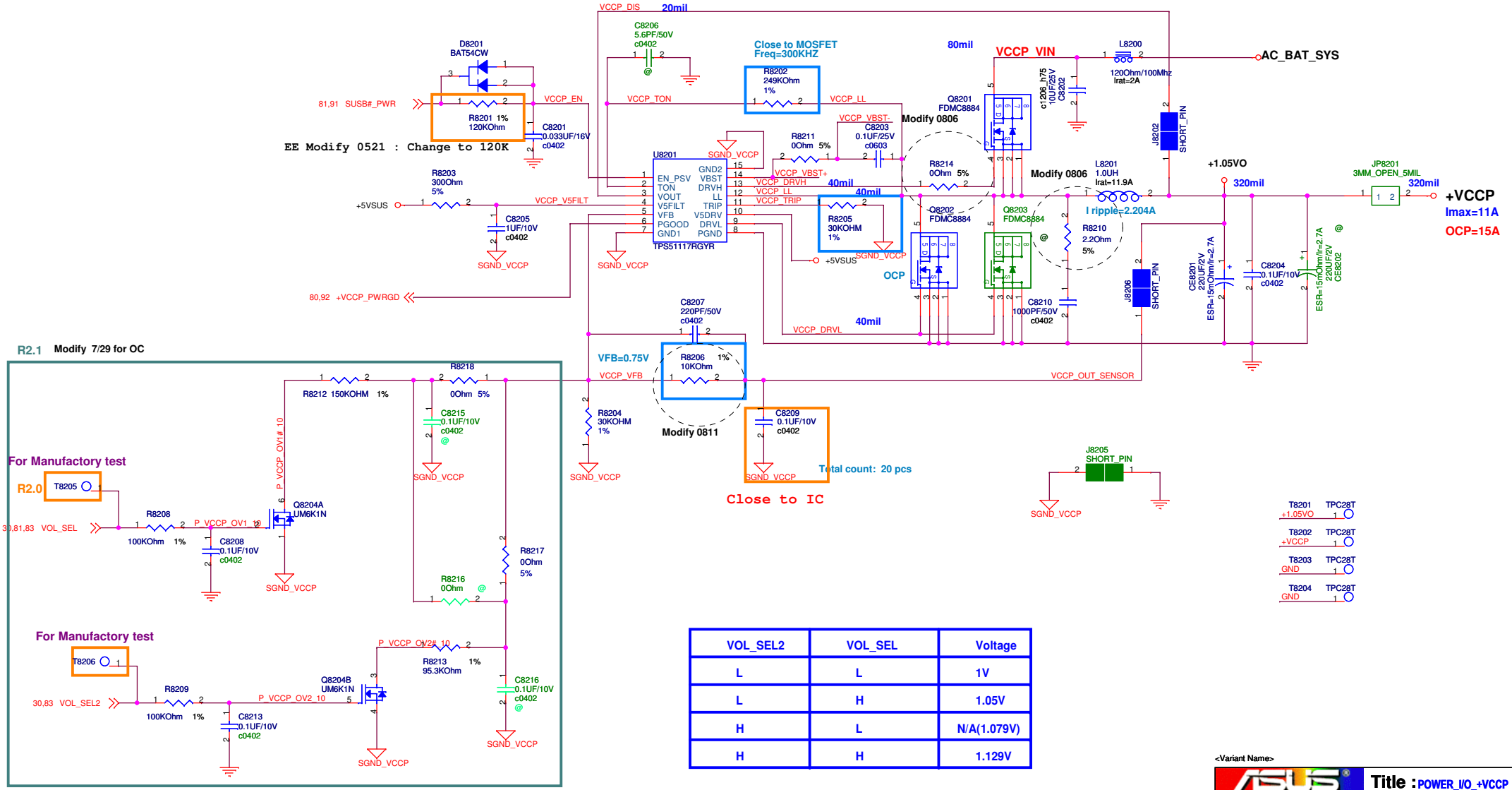
ASUSTeK COMPUTER INC.

Title : POWER_SYSTEM

Engineer: CHFred

Size	Project Name	Rev
Custom	UL5OAT	2.0

Date: Friday, October 16, 2009 Sheet 81 of 97



VOL_SEL2	VOL_SEL	Voltage
L	L	1V
L	H	1.05V
H	L	N/A(1.079V)
H	H	1.129V

<Variant Name>

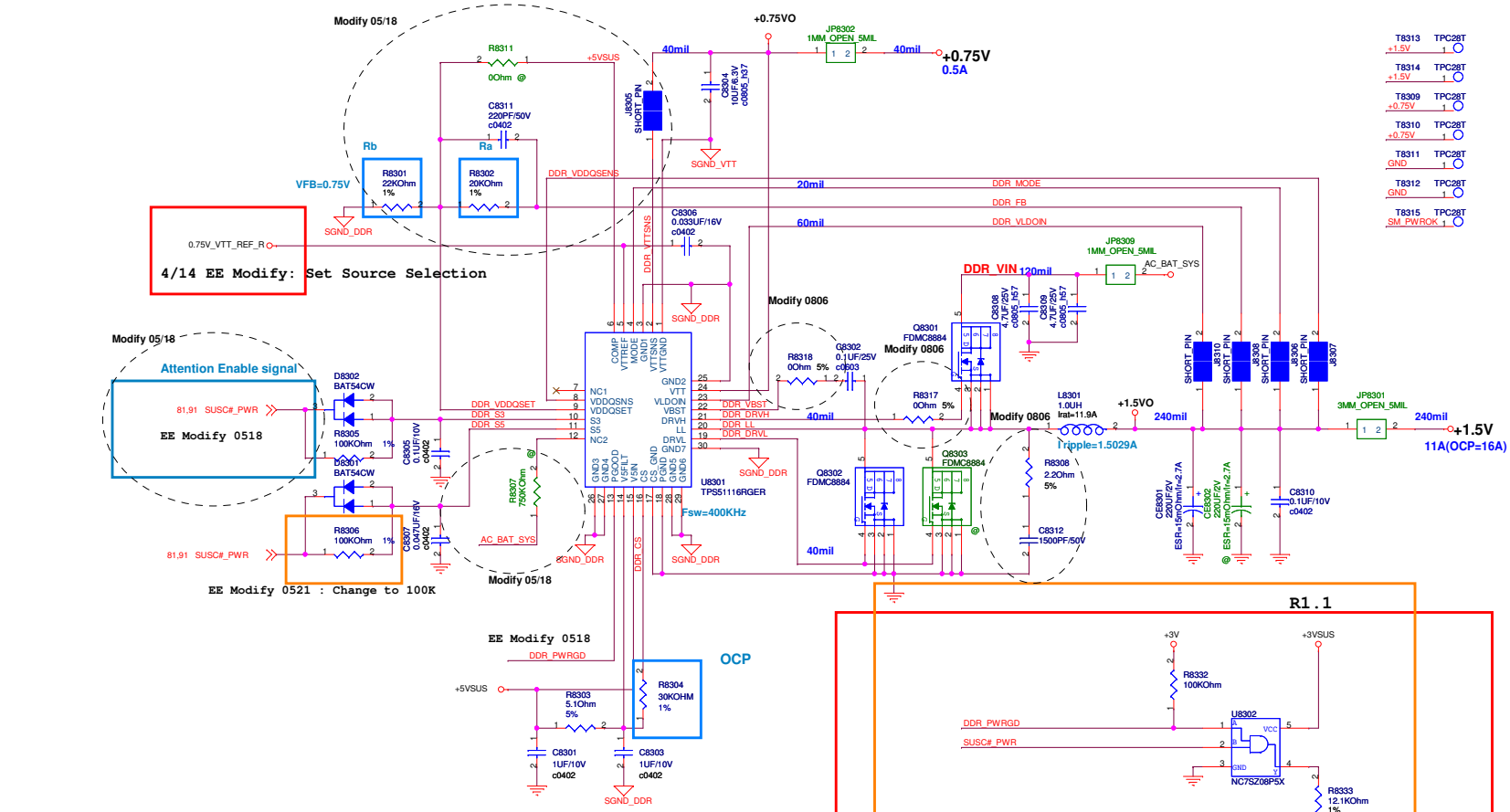
ASUSTeK COMPUTER INC.

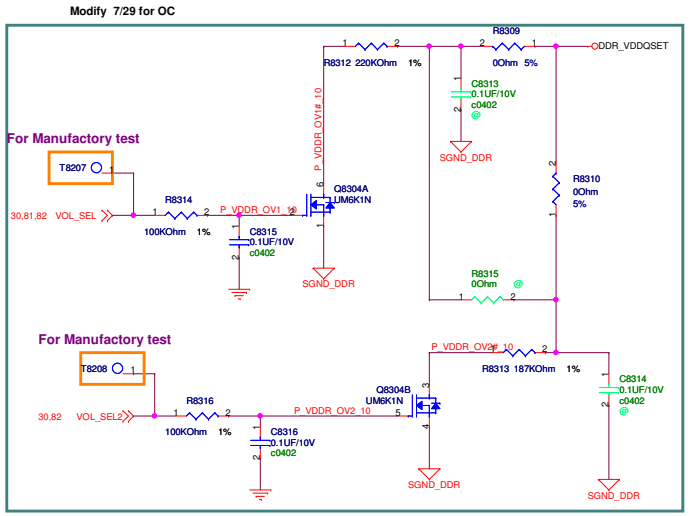
Title : POWER_I/O_+VCCP

Engineer: CH/Fred

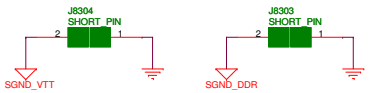
Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 82 of 97





VOL_SEL2	VOL_SEL	Voltage
L	L	1.43V
L	H	1.5V
H	L	N/A(1.512V)
H	H	1.58V



<Variant Name>

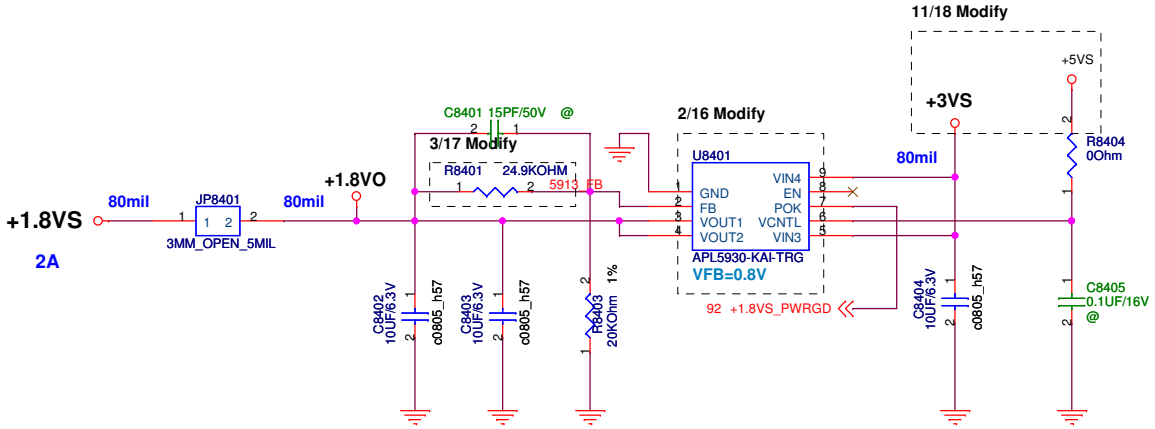
Title : POWER_I/O_DDR & VTT

ASUSTeK COMPUTER INC. Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 83 of 97

+1.8VS



T8401 TPC28T +1.8VO 1

T8402 TPC28T +1.8VS 1

T8403 TPC28T GND 1

T8404 TPC28T GND 1

<Variant Name>

ASUSTeK COMPUTER INC.	Title : POWER_I/O_ +1.8VS	
	Engineer: CH/Fred	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 84 of 97	

<Variant Name>

Title : POWER_I/O_VGA

ASUSTeK COMPUTER INC.

Engineer: CH/Fred

Size	Project Name	Rev
B	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 85 of 97

<Variant Name>

Title : <Title>

ASUSTeK COMPUTER INC.

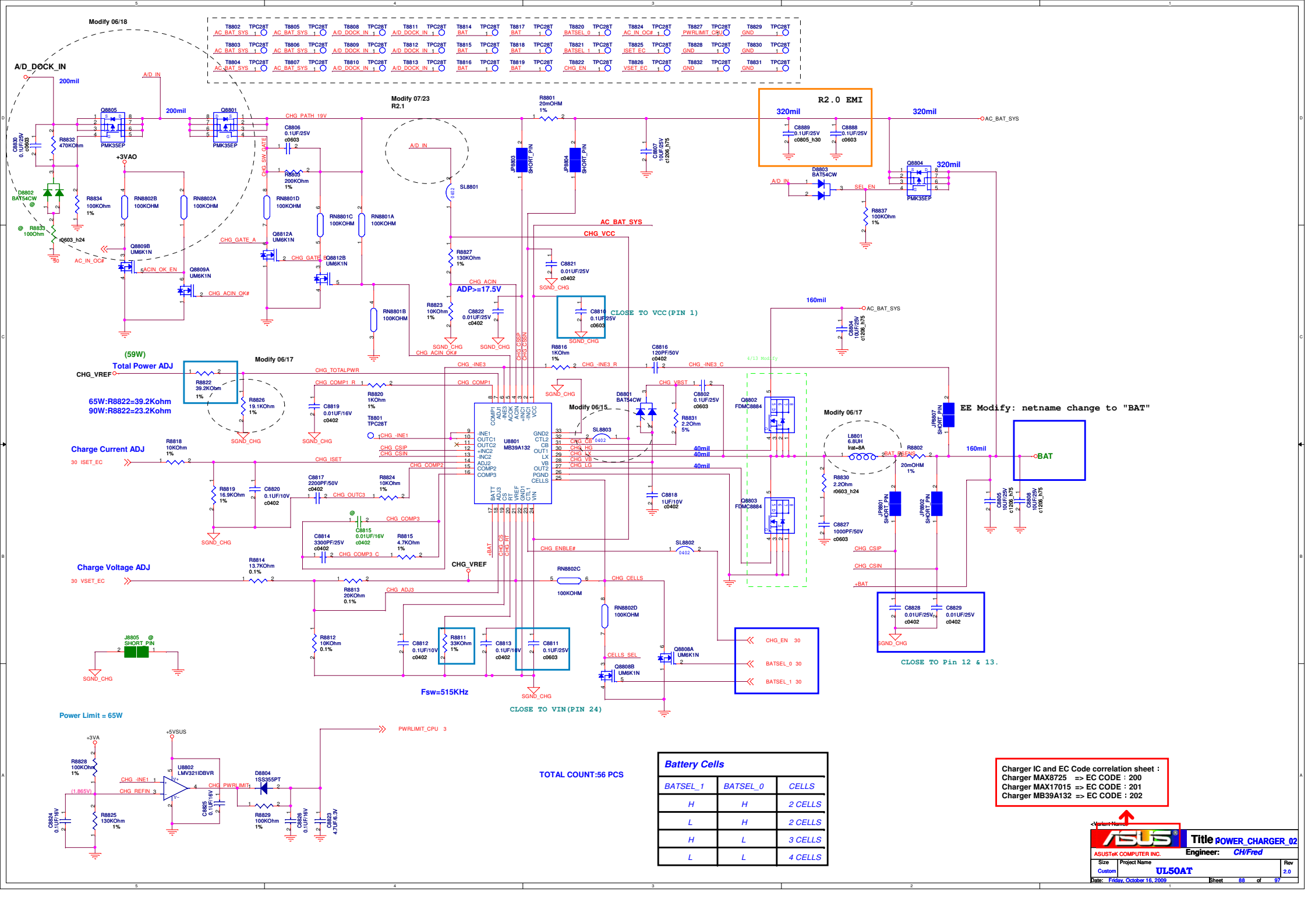
Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 86 of 97

<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: CH/Fred	
Size: A	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 87 of 97	


Modify 06/18
A/D_DOCK_IN
200mil
A/D_IN
Q8805
Q8801
PMK35EP
R8832 470KOhm
+3VAO
D8802 BAT54CW
R8834 100KOhm 1%
R8833 100Ohm
r0603_h24
RN8802B 100KOHM
RN8802A 100KOHM
Q8809B UM6K1N
Q8809A UM6K1N
ACIN_OK_EN
CHG_ACIN_OK#
AC_IN_OC#
CHG_PATH_19V
C8806 0.1UF/25V c0603
CHG_SW_GATE
R8803 200KOhm 1%
RN8801D 100KOHM
RN8801C 100KOHM
RN8801A 100KOHM
RN8801B 100KOHM
CHG_GATE_A
Q8812A UM6K1N
CHG_GATE_B
Q8812B UM6K1N
Modify 07/23
R2.1
SL8801
R8801 20mOHM 1%
JP8803 SHORT_PIN
JP8804 SHORT_PIN
C8807 10UF/25V c1206_h75
R2.0 EMI
320mil
C8889 0.1UF/25V c0805_h30
C8888 0.1UF/25V c0603
AC_BAT_SYS
Q8804
D8803 BAT54CW
SEL_EN
R8837 100KOhm 1%
AC_BAT_SYS
CHG_VCC
C8821 0.01UF/25V c0402
SGND_CHG
C8810 0.1UF/25V c0603
CLOSE TO VCC(PIN 1)
CHG_ACIN
ADP>=17.5V
R8827 130KOhm 1%
R8823 10KOhm 1%
C8822 0.01UF/25V c0402
CHG_ACIN_OK#
CHG_CSSP
CHG_CSSN
160mil
C8804 10UF/25V c1206_h75
(59W)
Total Power ADJ
CHG_VREF
R8822 39.2KOhm 1%
65W:R8822=39.2Kohm
90W:R8822=23.2Kohm
Modify 06/17
R8826 19.1KOhm 1%
CHG_TOTALPWR
CHG_COMP1_R
R8820 1KOhm 1%
C8819 0.01UF/16V c0402
T8801 TPC28T
CHG_-INE1
CHG_-INE3
R8816 1KOhm 1%
CHG_-INE3_R
C8816 120PF/50V c0402
CHG_-INE3_C
4/13 Modify
CHG_VBST
C8802 0.1UF/25V c0603
D8801 BAT54CW
R8831 2.2Ohm 5%
Modify 06/15
U8801 MB39A132
SL8803
CHG_CB
CHG_HG
CHG_LX
CHG_VB
CHG_LG
Q8802 FDMC8884
Q8803 FDMC8884
40mil
L8801 6.8UH Irat=8A
R8802 20mOHM 1%
BAT_VSENS
EE Modify: netname change to "BAT"
JP8807 SHORT_PIN
JP8801 SHORT_PIN
JP8802 SHORT_PIN
BAT
C8805 10UF/25V c1206_h75
C8808 10UF/25V c1206_h75
R8830 2.2Ohm r0603_h24
C8827 1000PF/50V c0603
CHG_CSIP
CHG_CSIN
+BAT
C8828 0.01UF/25V c0402
C8829 0.01UF/25V c0402
CLOSE TO Pin 12 & 13.
Charge Current ADJ
30 ISET_EC
R8818 10KOhm 1%
CHG_ISET
R8819 16.9KOhm 1%
C8820 0.1UF/10V c0402
C8817 2200PF/50V c0402
CHG_OUTC3
R8824 10KOhm 1%
CHG_COMP2
CHG_COMP3
C8815 0.01UF/16V c0402
C8814 3300PF/25V c0402
CHG_COMP3_C
R8815 4.7KOhm 1%
C8818 1UF/10V c0402
CHG_ENBLE#
SL8802
Charge Voltage ADJ
30 VSET_EC
R8814 13.7KOhm 0.1%
R8813 20KOhm 0.1%
CHG_ADJ3
RN8802C 100KOHM
RN8802D 100KOHM
CHG_CELLS
R8812 10KOhm 0.1%
C8812 0.1UF/10V c0402
R8811 33KOhm 1%
C8813 0.1UF/10V c0402
C8811 0.1UF/25V c0603
CELLS_SEL
Q8808A UM6K1N
Q8808B UM6K1N
CHG_EN 30
BATSEL_0 30
BATSEL_1 30
J8805 @ SHORT_PIN
Fsw=515KHz
CLOSE TO VIN(PIN 24)
Power Limit = 65W
+3VA
+5VSUS
R8828 100KOhm 1%
(1.865V)
R8825 130KOhm 1%
U8802 LMV321IDBVR
CHG_-INE1
CHG_REFIN
CHG_PWRLIMIT
D8804 1SS355PT
R8829 100KOhm 1%
C8824 0.1UF/16V
C8825 0.1UF/16V
C8826 0.1UF/16V
C8823 4.7UF/6.3V
PWRLIMIT_CPU 3
TOTAL COUNT:56 PCS
Battery Cells
BATSEL_1 | BATSEL_0 | CELLS
H | H | 2 CELLS
L | H | 2 CELLS
H | L | 3 CELLS
L | L | 4 CELLS
Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202
ASUSTeK COMPUTER INC.
Title POWER_CHARGER_02
Engineer: CH/Fred
Size Custom
Project Name UL50AT
Rev 2.0
Date: Friday, October 16, 2009
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: CH/Fred	
Size: A	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 89 of 97	

<Variant Name>

Title : POWER_DETECT

ASUSTeK COMPUTER INC.

Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

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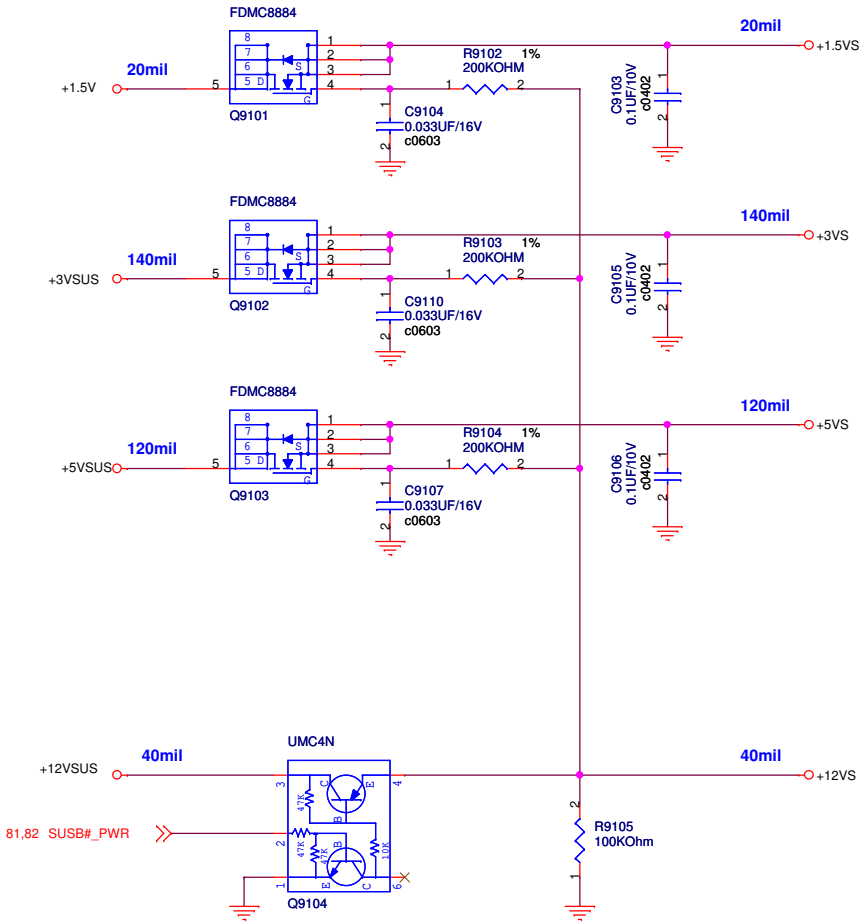
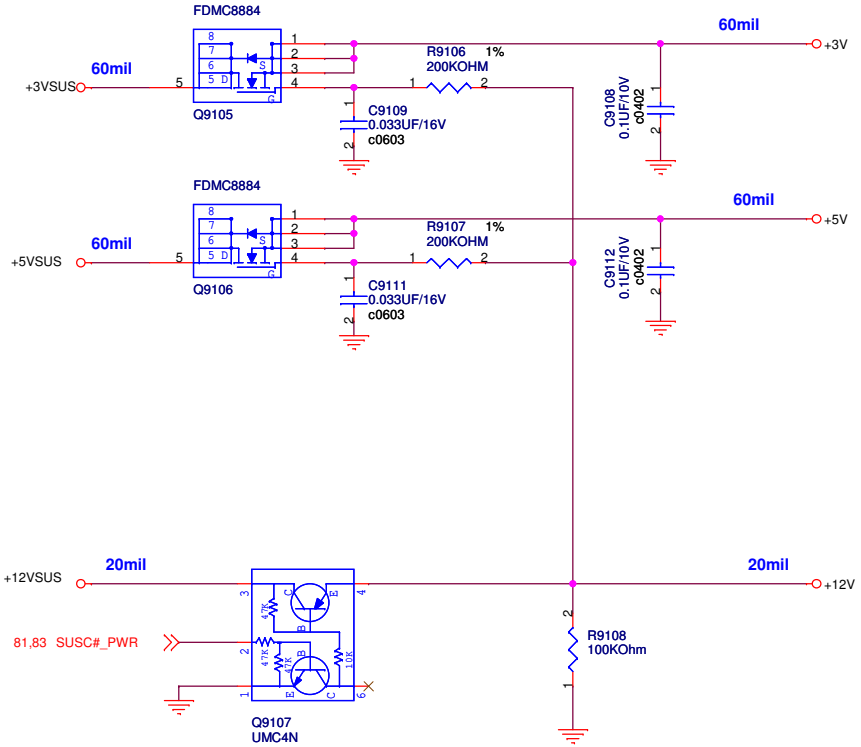
SUSB#_PWR POWER



Total count: 19 pcs

SUSC#_PWR POWER

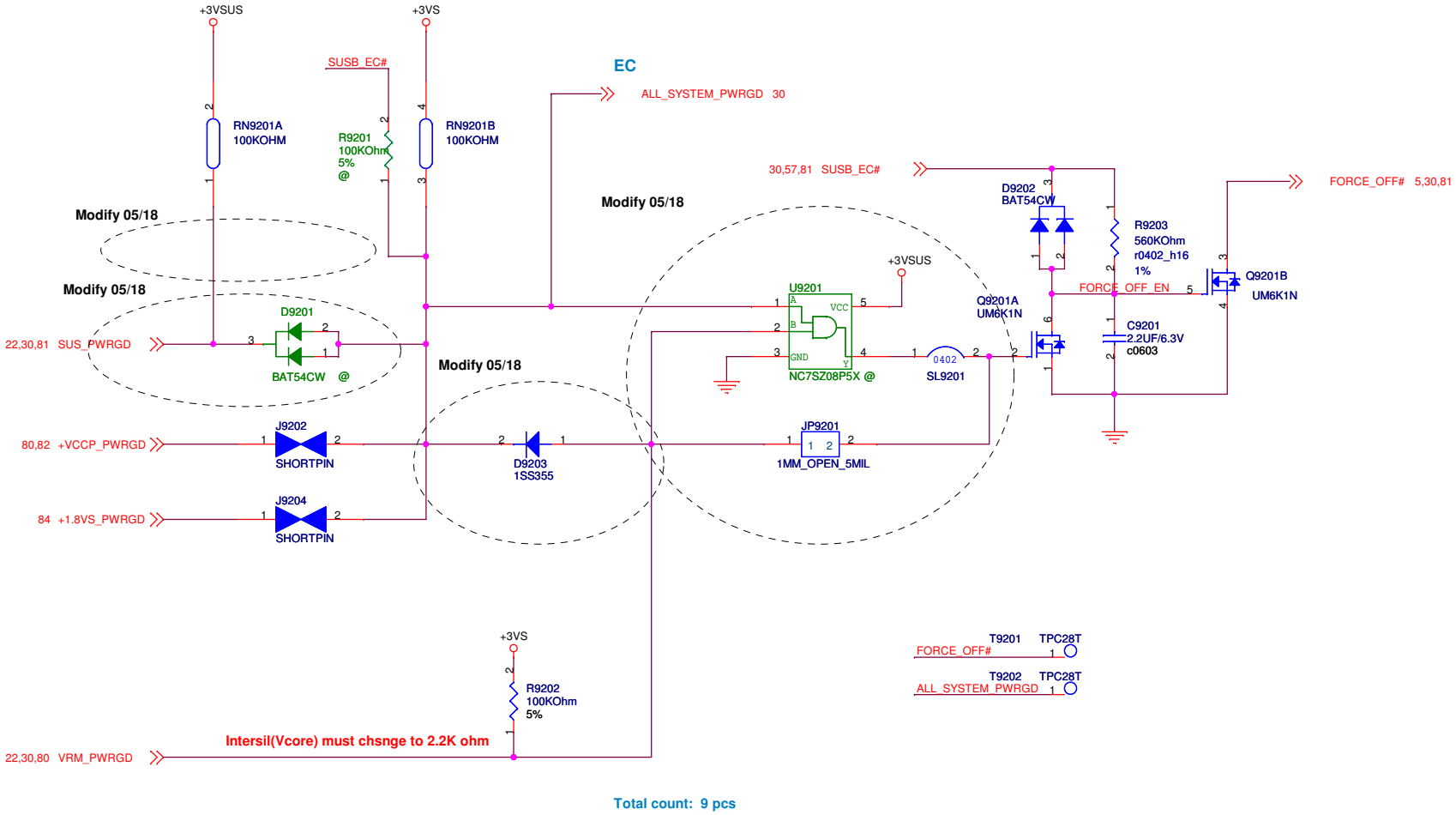


T9101 TPC28T +12VSUS 1		T9111 TPC28T +3VSUS 1	
T9102 TPC28T +12VS 1		T9113 TPC28T +3VS 1	
T9103 TPC28T +12V 1		T9115 TPC28T +3V 1	
T9104 TPC28T +5VSUS 1		T9120 TPC28T +1.5V 1	
T9106 TPC28T +5VS 1		T9121 TPC28T +1.5VS 1	
T9110 TPC28T +5V 1		T9123 TPC28T SUSB#_PWR 1	
		T9114 TPC28T SUSC#_PWR 1	

<Variant Name>

ASUSTeK COMPUTER INC.	Title : POWER_LOAD SWITCH	
	Engineer: CH/Fred	
Size: B	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 91 of 97	

POWER GOOD DETECTER



Total count: 9 pcs

<Variant Name>

ASUSTeK COMPUTER INC.	Title : POWER_PROTECT	
	Engineer: CH/Fred	
Size: B	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 92 of 97	

<Variant Name>

Title : POWER_SIGNAL

ASUSTeK COMPUTER INC.

Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

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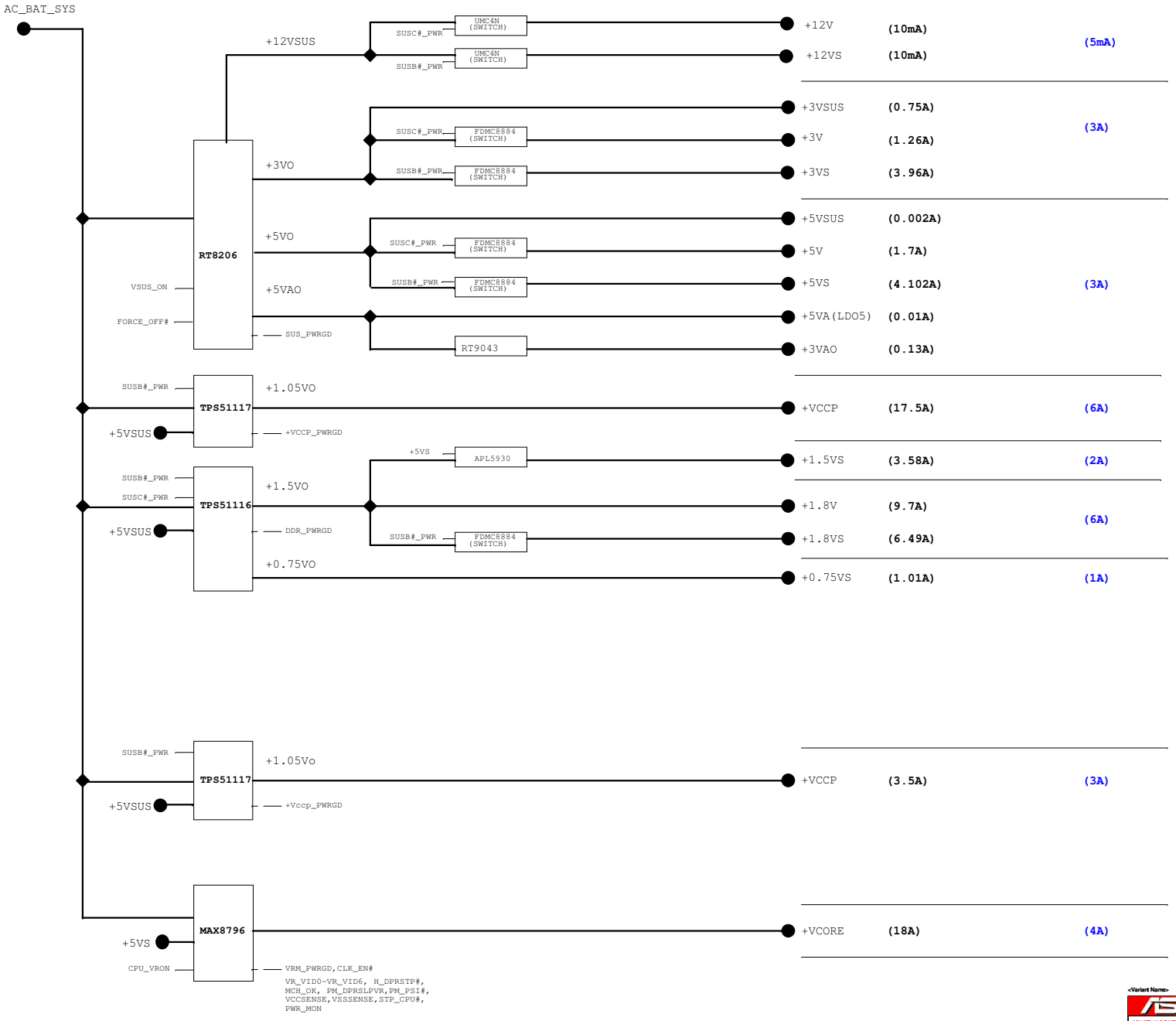

<Variant Name>

Title : POWER_FLOWCHART

ASUSTeK COMPUTER INC.

Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 84 of 97

<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: CH/Fred	
Size: A	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 95 of 97	

Rev	Date	Description
1.00		First Release!
1.10		
2.00		

<Variant Name>

ASUSTeK COMPUTER INC.

Title : HISTORY

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

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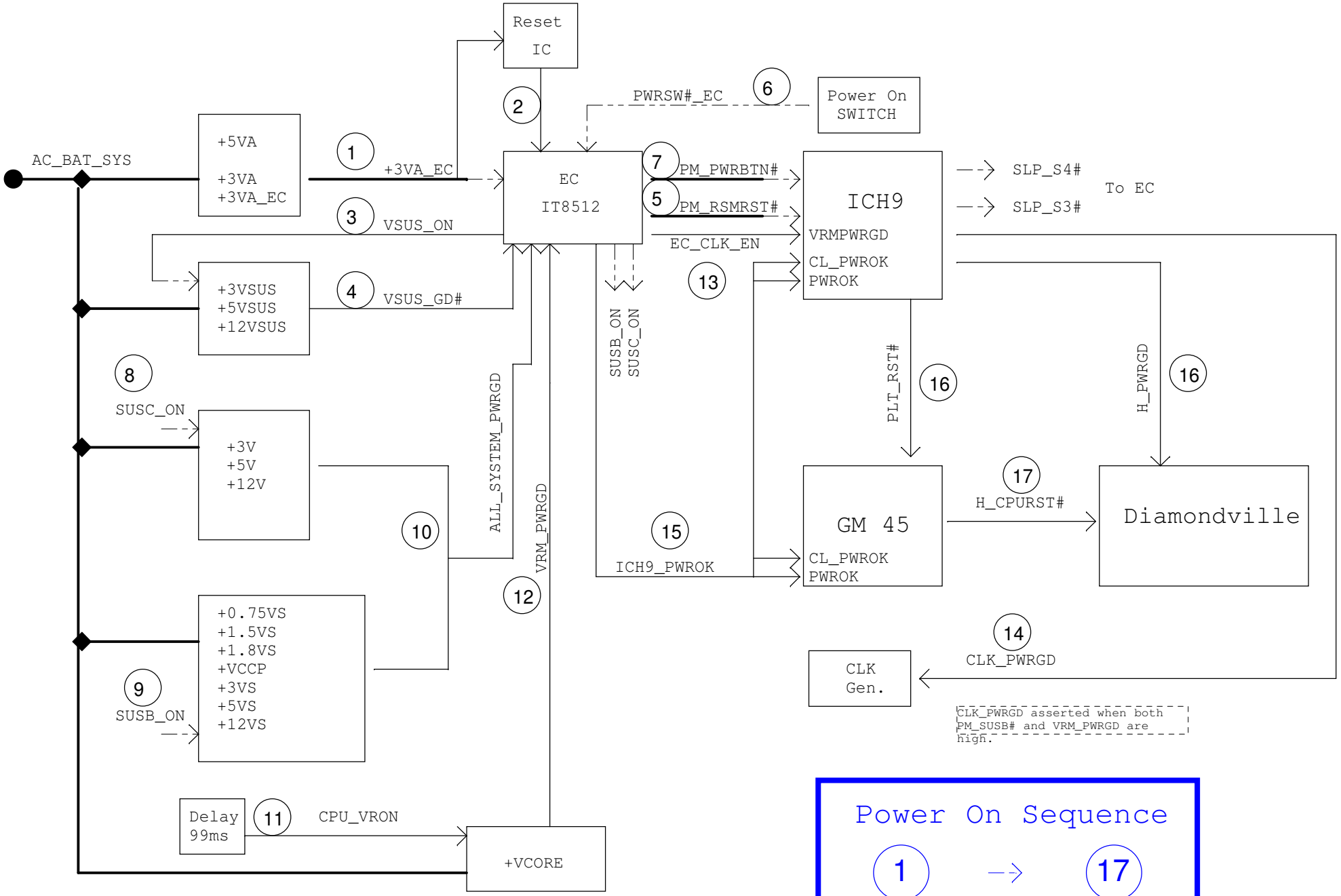

<Variant Name>

ASUSTeK COMPUTER INC.	Title : POWER SEQUENCE	
	Engineer: Eric_Ho	
Size: Custom	Project Name: UL50AT	Rev: 2.0
Date: Friday, October 16, 2009	Sheet 97 of 97	