28LV64A

64K (8K x 8) Low Voltage CMOS EEPROM

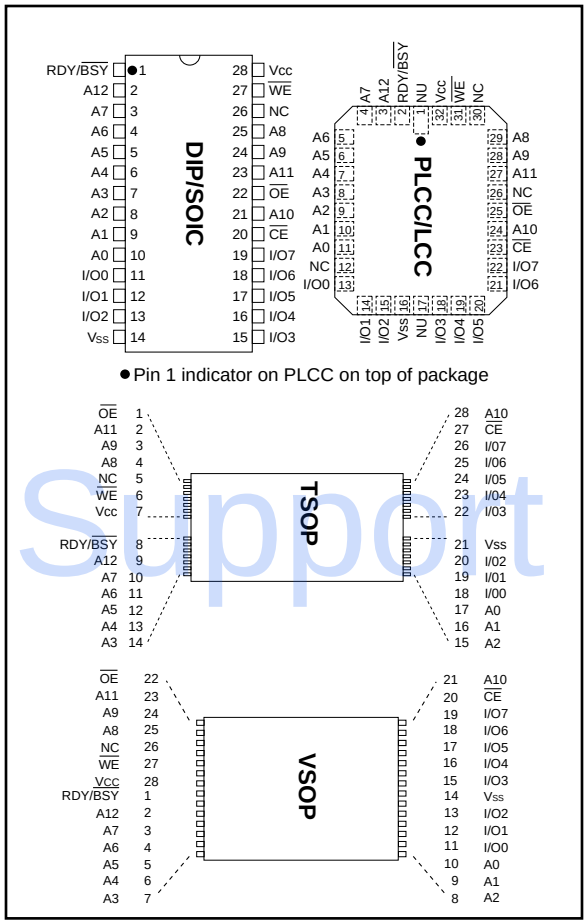
FEATURES

- 2.7V to 3.6V Supply
- Read Access Time—300 ns
- CMOS Technology for Low Power Dissipation
  - 8 mA Active
  - 50 µA CMOS Standby Current
- Byte Write Time—3 ms
- Data Retention >200 years
- High Endurance - Minimum 100,000 Erase/Write Cycles
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- Data Polling
- Ready/Busy
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- Electronic Signature for Device Identification
- Organized 8Kx8 JEDEC Standard Pinout
  - 28-pin Dual-In-Line Package
  - 32-pin Chip Carrier (Leadless or Plastic)
  - 28-pin Thin Small Outline Package (TSOP) 8x20mm
  - 28-pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - Commercial: 0˚C to +70˚C
  - Industrial: -40˚C to +85˚C

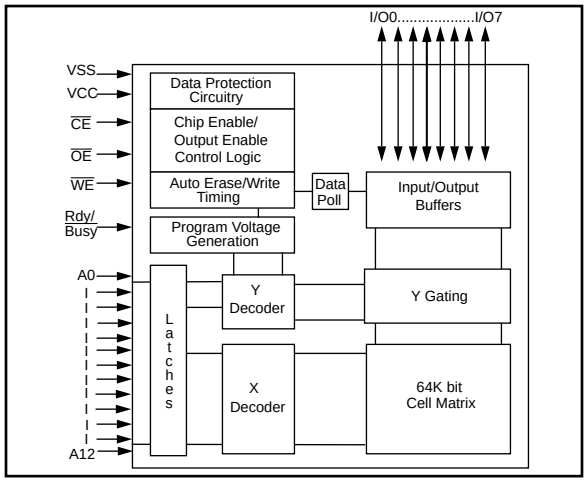
DESCRIPTION

The Microchip Technology Inc. 28LV64A is a CMOS 64K non-volatile electrically Erasable PROM organized as 8K words by 8 bits. The 28LV64A is accessed like a static RAM for the read or write cycles without the need of external components. During a “byte write”, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using Data polling. The Ready/Busy pin is an open drain output, which allows easy configuration in ‘wired-or’ systems. Alternatively, Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

PACKAGE TYPES



BLOCK DIAGRAM



Datasheet.Support

1.0 ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

VCC and input voltages w.r.t. V_{SS} ..... -0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. V_{SS}..... -0.6V to +13.5V

Voltage on A9 w.r.t. V_{SS}..... -0.6V to +13.5V

Output Voltage w.r.t. V_{SS} ..... -0.6V to VCC+0.6V

Storage temperature ..... -65˚C to +150˚C

Ambient temp. with power applied .....-55°C to +125°C

*Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUCTION TABLE

Name	Function
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
V_{CC}	+ Power Supply
V_{SS}	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

	V_{CC} = 2.7 to 3.6V Commercial (C): Tamb = 0°C to 70°C Industrial (I): Tamb = -40°C to 85°C					
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic “1” Logic “2”	V_{IH} V_{IL}	2.0	 0.6	V V	
Input Leakage	—	I_{LI}	—	5	µA	V_{IN} = 0V to V_{CC}+1
Input Capacitance	—	C_{IN}	—	6	pF	Vin = 0V; Tamb = 25°C; f = 1 MHz (Note 1)
Output Voltages	Logic “1” Logic “0”	V_{OH} V_{OL}	2.0	 0.3	V V	I_{OH} = -100µA I_{OL} = 1.0 mA $I0_L$ = 2.0 mA for RDY/$\overline{Busy}$
Output Leakage	—	I_{LO}	—	5	µA	V_{OUT} = 0V to V_{CC}+0.1V
Output Capacitance	—	C_{OUT}	—	12	pF	V_{OUT} = 0V; Tamb = 25°C; f = 1 MHz (Note 1)
Power Supply Current, Activity	TTL input	I_{CC}	—	8	mA	f = 5 MHz (Note 2) I_O = OmA V_{CC} = 3.3 $\overline{CE}$ = V_{IL}
Power Supply Current, Standby	TTL input TTL input CMOS input	$I_{CC(S)TTL}$ $I_{CC(S)TTL}$ $I_{CC(S)CMOS}$	—	2 3 100	mA mA µA	$\overline{CE}$ = V_{IH} (0°C to 70°C°) $\overline{CE}$ = V_{IH} (-40°C to 85°C°) $\overline{CE}$ = V_{CC} -3.0 to V_{CC}+1

Note 1: Not 100% tested.
2: AC power supply current above 5 MHz: 2 mA/Mhz.

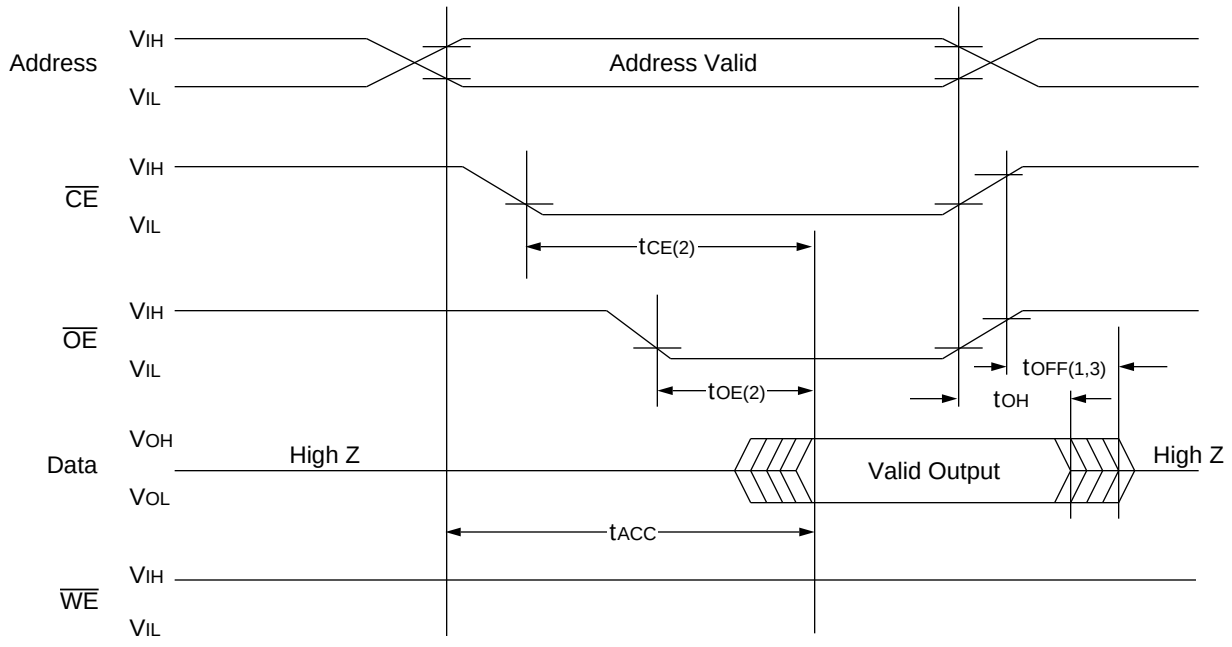
 © 1996 Microchip Technology Inc.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.0V; V_{IL} = 0.6V; V_{OH} = V_{OL} = V_{CC}/2			
	Output Load:	1 TTL Load + 100 pF			
	Input Rise and Fall Times:	20 ns			
	Ambient Temperature:	Commercial (C): Tamb = 0°C to +70°C Industrial (I) : Tamb = -40°C to +85°C			
Parameter	**Sym**	**28LV64-30**		**Units**	**Conditions**
		Min	**Max**		
Address to Output Delay	t_{ACC}	—	300	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	150	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	60	ns	(Note 1)
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0	—	ns	(Note 1)
Endurance	—	10M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 2)

Note 1: Not 100% tested.
2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

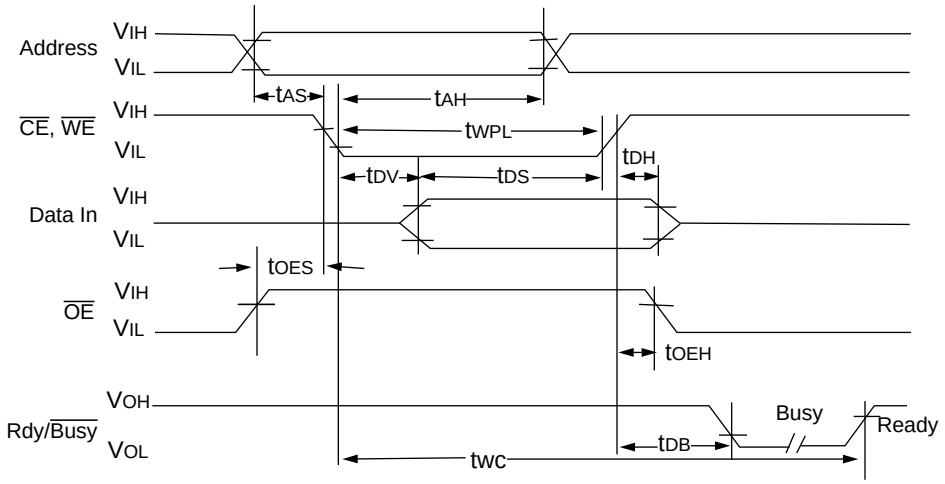
TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.0V; V_{IL} = 0.6V; V_{OH} = V_{OL} = V_{CC}/2			
	Output Load:	1 TTL Load + 100 pF			
	Input Rise/Fall Times:	20 ns			
	Ambient Temperature:	Commercial (C): Tamb = 0°C to +70°C Industrial (I) : Tamb = -40°C to +85°C			
Parameter	**Sym**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	100		ns	
Data Set-Up Time	t_{DS}	120		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	150		ns	(Note 1)
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	(Note 2)
Time to Device Busy	t_{DB}		50	ns	
Write Cycle Time (28LV64A)	t_{WC}		3	ms	1.5 ms typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS



 © 1996 Microchip Technology Inc.

FIGURE 1-3: $\overline{\text{DATA}}$ POLLING WAVEFORMS

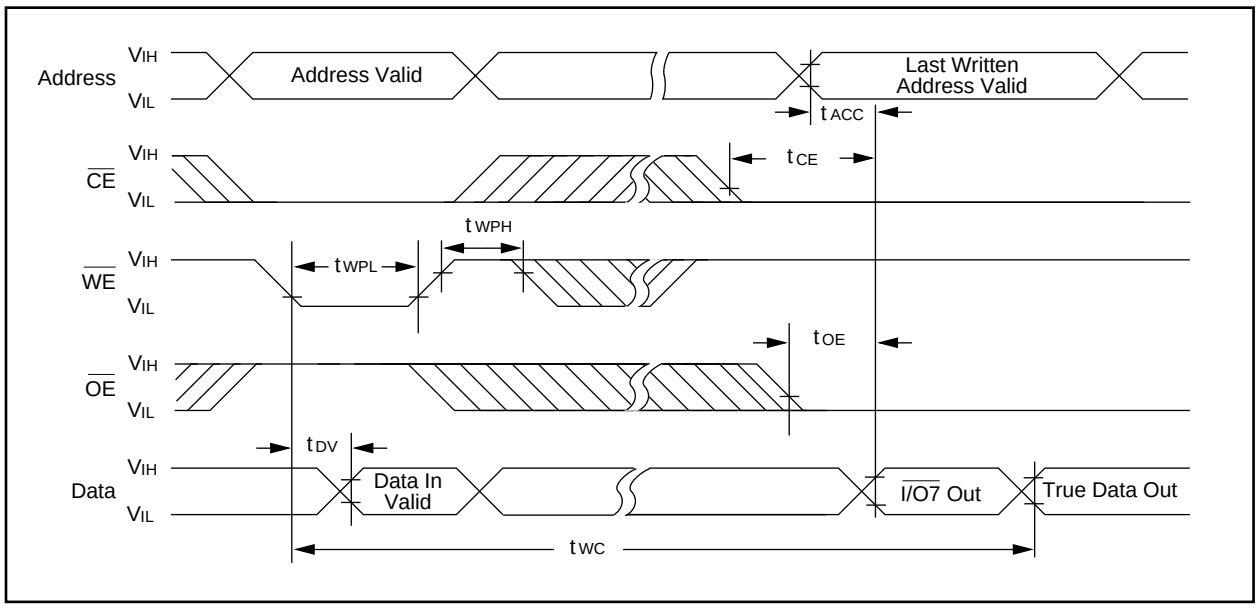


FIGURE 1-4: CHIP CLEAR WAVEFORMS

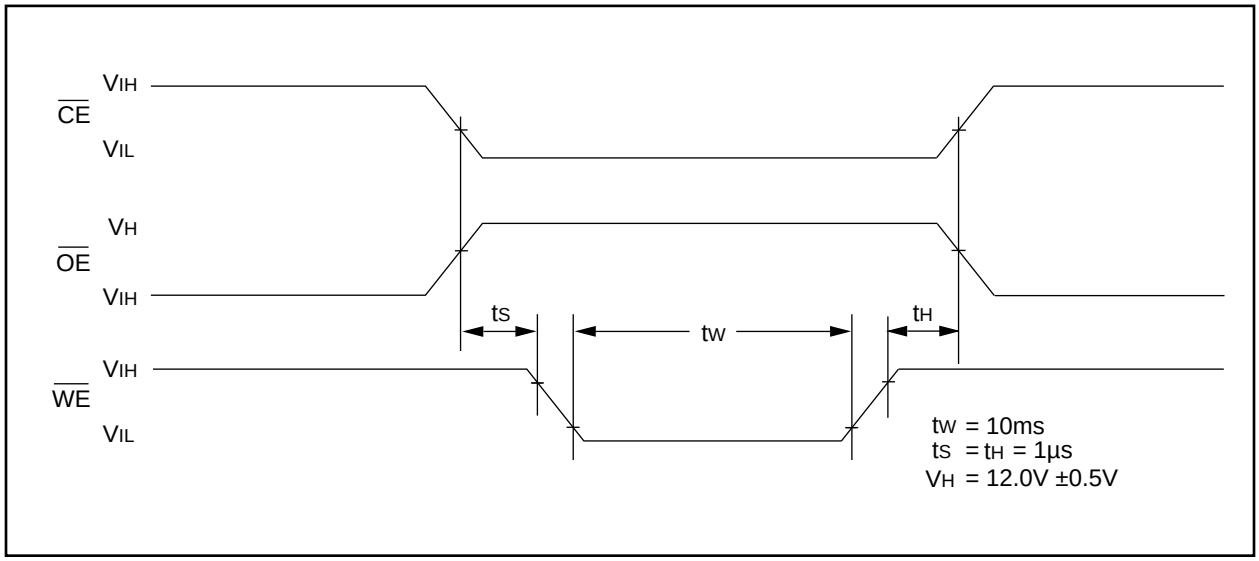


TABLE 1-5: SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A_I	V_{CC}	I/O_I
Chip Clear	V_{IL}	V_H		X	V_{CC}	
Extra Row Read	V_{IL}	V_{IL}	V_{IH}	A9 = V_H	V_{CC}	Data Out
Extra Row Write		V_{IH}		A9 = V_H	V_{CC}	Data In
Note: V_H = 12.0V ± 0.5V						

2.0 DEVICE OPERATION

The Microchip Technology Inc. 28LV64A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$ (1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note: (1) Open drain output.

2.1 Read Mode

The 28LV64A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the output t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

2.2 Standby Mode

The 28LV64A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (2.0 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

2.4 Write Mode

The 28LV64A has a write cycle similar to that of a static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28LV64A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28LV64A has completed writing and is ready to accept another cycle.

2.5 $\overline{Data}$ Polling

The 28LV64A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 can not be determined). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 1FEO to 1FFF, the additional bytes can be written to or read from in the same manner as the regular memory array.

2.7 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and CE low. This procedure clears all data, except for the extra row.

 © 1996 Microchip Technology Inc.

28LV64A Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.

28LV64A – F T – 20 I /P

Package:	L =	Plastic Leaded Chip Carrier (PLCC)
	P =	Plastic DIP
	SO =	Plastic Small Outline IC
	TS =	Thin Small Outline Package (TSOP) 8 x 20 mm
	VS =	Very Small Outline Package (VSOP) 8 x 13.4 mm
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
Access Time:	20 =	200 ns
	30 -	300 ns
Shipping:	Blank =	Tube
	T =	Tape and Reel “L” and “SO”
Option:	Blank =	twc = 1ms
	F =	twc = 200µs
Device:	24LV64A	8K x 8 CMOS EEPROM

WORLDWIDE SALES & SERVICE

AMERICAS

Corporate Office
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602 786-7200 Fax: 602 786-7277
Technical Support: 602 786-7627
Web: http://www.microchip.com

Atlanta
Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770 640-0034 Fax: 770 640-0307

Boston
Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508 480-9990 Fax: 508 480-8575

Chicago
Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 708 285-0071 Fax: 708 285-0075

Dallas
Microchip Technology Inc.
14651 Dallas Parkway, Suite 816
Dallas, TX 75240-8809
Tel: 972 991-7177 Fax: 972 991-8588

Dayton
Microchip Technology Inc.
Suite 150
Two Prestige Place
Miamisburg, OH 45342
Tel: 513 291-1654 Fax: 513 291-9175

Los Angeles
Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 714 263-1888 Fax: 714 263-1338

New York
Microchip Technmgy Inc.
150 Motor Parkway, Suite 416
Hauppauge, NY 11788
Tel: 516 273-5305 Fax: 516 273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408 436-7950 Fax: 408 436-7955

Toronto
Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905 405-6279 Fax: 905 405-6253

ASIA/PACIFIC

China
Microchip Technology
Unit 406 of Shanghai Golden Bridge Bldg.
2077 Yan'an Road West, Hongiao District
Shanghai, Peoples Republic of China
Tel: 86 21 6275 5700
Fax: 011 86 21 6275 5060

Hong Kong
Microchip Technology
RM 3801B, Tower Two
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T. Hong Kong
Tel: 852 2 401 1200 Fax: 852 2 401 3431

India
Microchip Technology
No. 6, Legacy, Convent Road
Bangalore 560 025 India
Tel: 91 80 526 3148 Fax: 91 80 559 9840

Korea
Microchip Technology
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku,
Seoul, Korea
Tel: 82 2 554 7200 Fax: 82 2 558 5934

Singapore
Microchip Technology
200 Middle Road
#10-03 Prime Centre
Singapore 188980
Tel: 65 334 8870 Fax: 65 334 8850

Taiwan, R.O.C
Microchip Technology
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886 2 717 7175 Fax: 886 2 545 0139

EUROPE

United Kingdom
Arizona Microchip Technology Ltd.
Unit 6, The Courtyard
Meadow Bank, Furlong Road
Bourne End, Buckinghamshire SL8 5AJ
Tel: 44 1628 850303 Fax: 44 1628 850178

France
Arizona Microchip Technology SARL
Zone Industrielle de la Bonde
2 Rue du Buisson aux Fraises
91300 Massy - France
Tel: 33 1 69 53 63 20 Fax: 33 1 69 30 90 79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Muenchen, Germany
Tel: 49 89 627 144 0 Fax: 49 89 627 144 44

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleone Pas Taurus 1
Viale Colleoni 1
20041 Agrate Brianza
Milan Italy
Tel: 39 39 6899939 Fax: 39 39 689 9883

JAPAN

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shin Yokohama
Kohoku-Ku, Yokohama
Kanagawa 222 Japan
Tel: 81 45 471 6166 Fax: 81 45 471 6122

9/3/96

MICROCHIP

All rights reserved. © 1996, Microchip Technology Incorporated, USA. 9/96

Printed on recycled paper.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights. The Microchip logo and name are registered trademarks of Microchip Technology Inc. All rights reserved. All other trademarks mentioned herein are the property of their respective companies.