

Power Logic Level MOSFETs

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

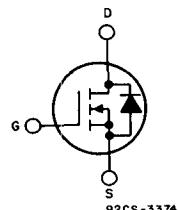
10 A, 120 V — 150 V

 $r_{DS(on)} = 0.3 \Omega$

Features:

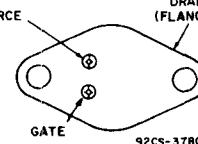
- Design optimized for 5 volt gate drive
- Can be driven directly from Q-MOS, N-MOS, TTL Circuits
- Compatible with automotive drive requirements
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

TERMINAL DIAGRAM

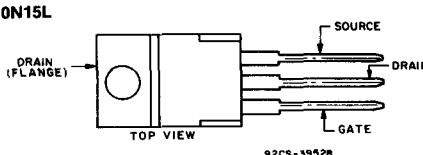


N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS RFM10N12L RFM10N15L



JEDEC TO-204AA



JEDEC TO-220AB

The RFM10N12L and RFM10N15L and the RFP10N12L and RFP10N15L* are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Because of space limitations branding (marking) on type RFM10N12L is F10N12L and on type RFP10N15L is F10N15L.

*The RFM and RFP series were formerly RCA developmental numbers TA9530 and TA9531, respectively.

MAXIMUM RATINGS, Absolute-Maximum Values ($T_c = 25^\circ C$):

	RFM10N12L	RFM10N15L	RFP10N12L	RFP10N15L	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	120	150
DRAIN-GATE VOLTAGE ($R_{DS(on)} = 1 \text{ M}\Omega$)	$V_{DG(on)}$	120	150	120	150
GATE-SOURCE VOLTAGE	V_{GS}		± 10		V
DRAIN CURRENT, RMS Continuous	I_D		10		V
Pulsed	I_{DM}		25		A
POWER DISSIPATION @ $T_c = 25^\circ C$	P_T	75	75	60	60
Derate above $T_c = 25^\circ C$		0.6	0.6	0.48	0.48
OPERATING AND STORAGE TEMPERATURE	$T_{J}, T_{S(tg)}$		-55 to +150		$^\circ C$

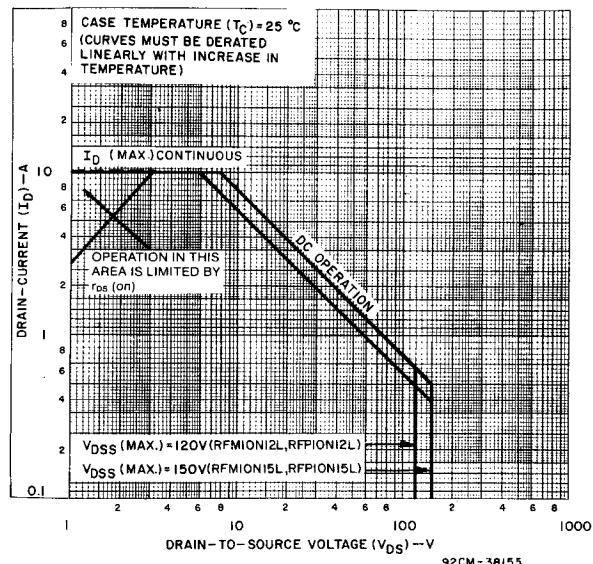
RFM10N12L, RFM10N15L, RFP10N12L, RFP10N15L

Fig. 1 - Maximum safe operating areas for all types.

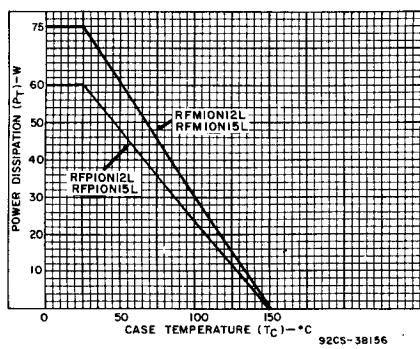


Fig. 2 - Power vs. temperature derating curve for all types.

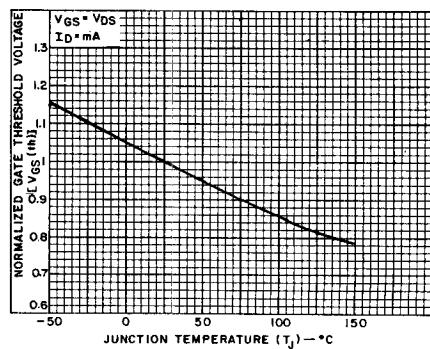


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

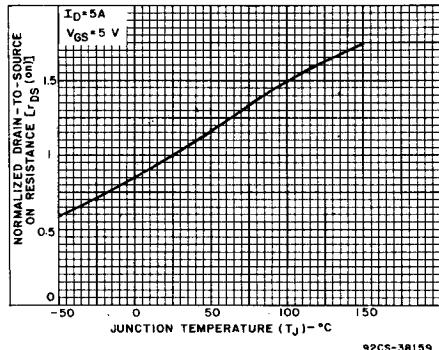


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

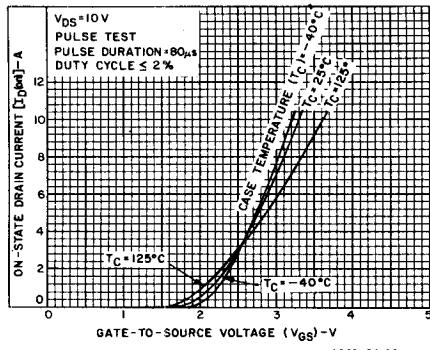
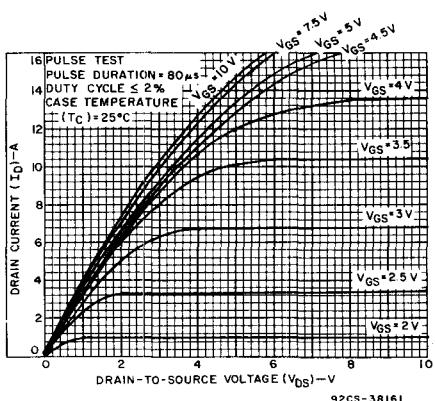
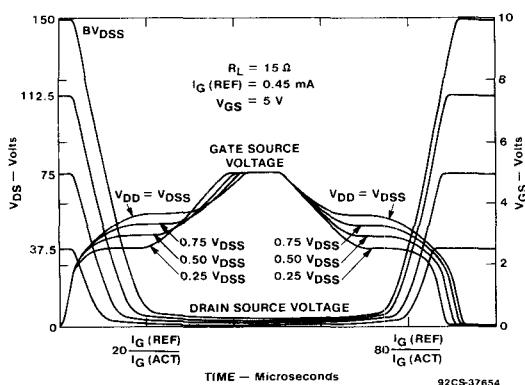


Fig. 5 - Typical transfer characteristics for all types.

RFM10N12L, RFM10N15L, RFP10N12L, RFP10N15L



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