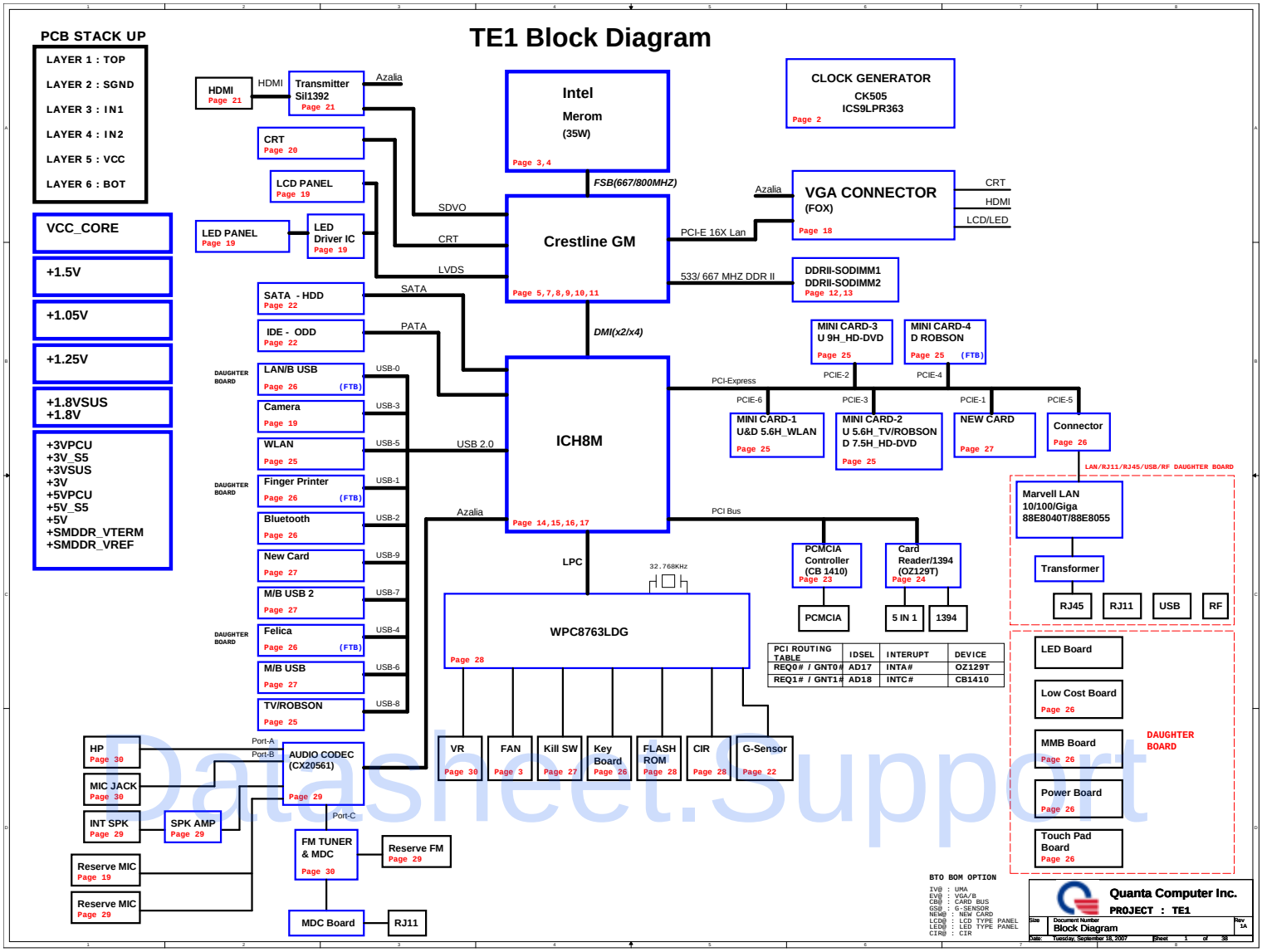
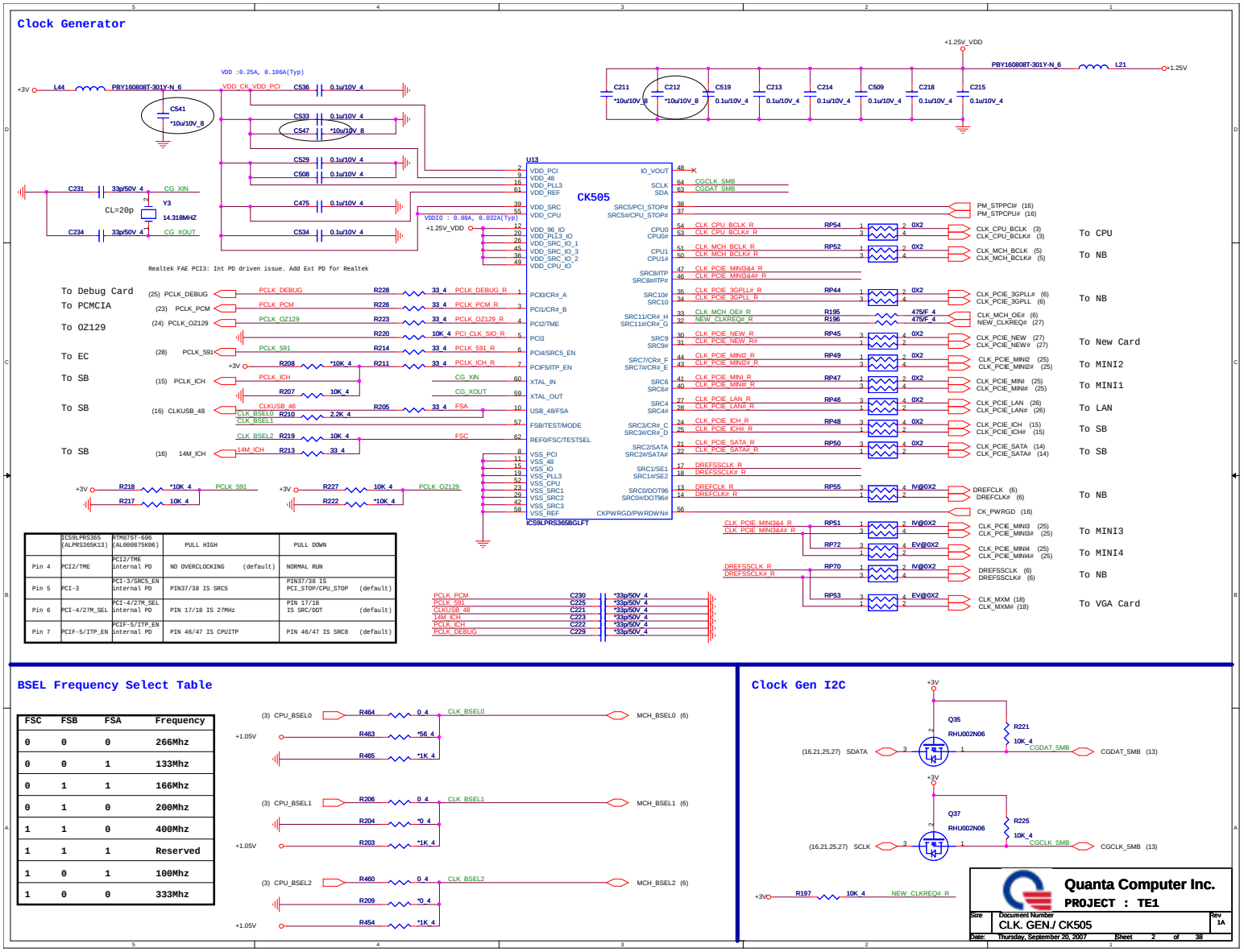
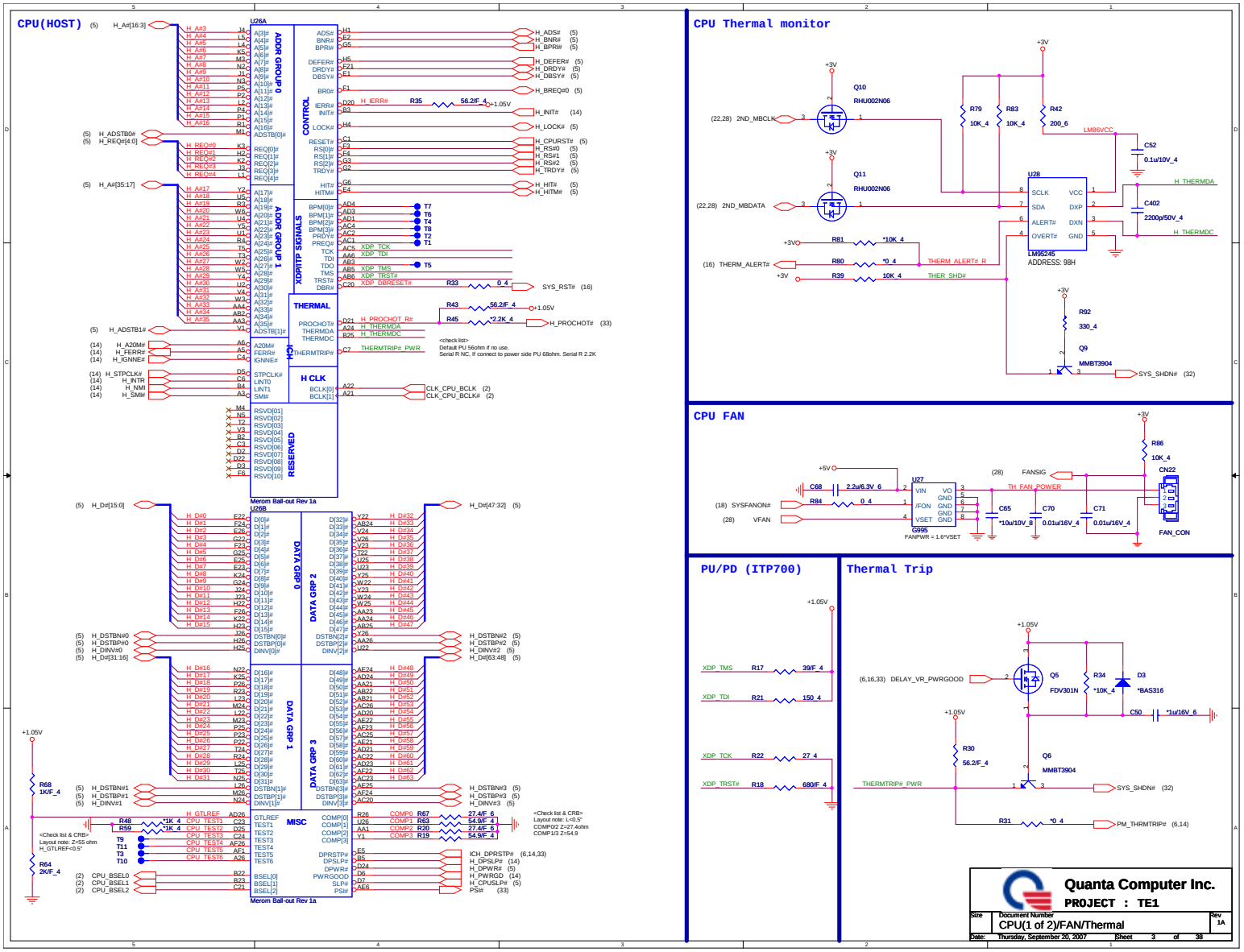
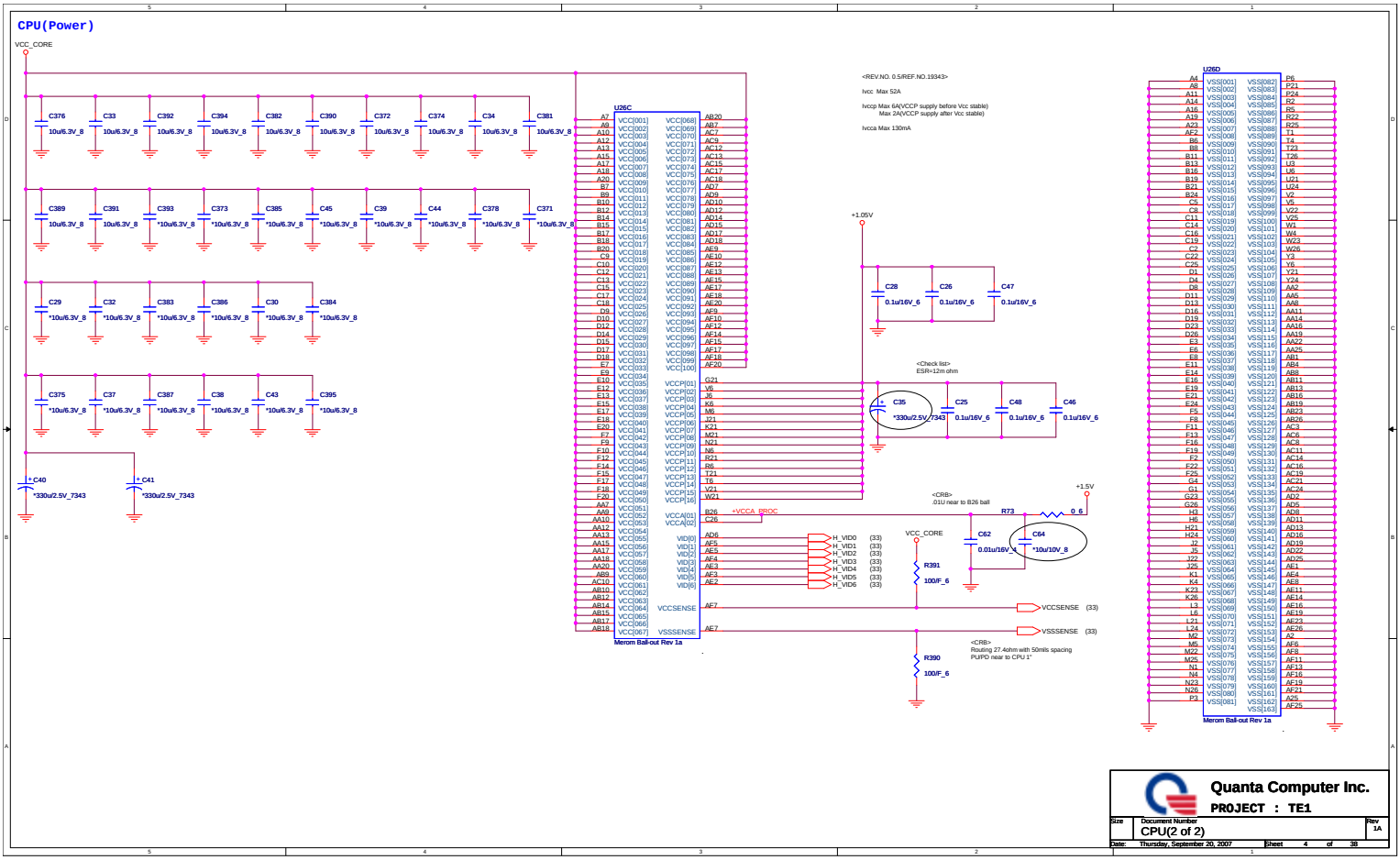
TE1 Block Diagram

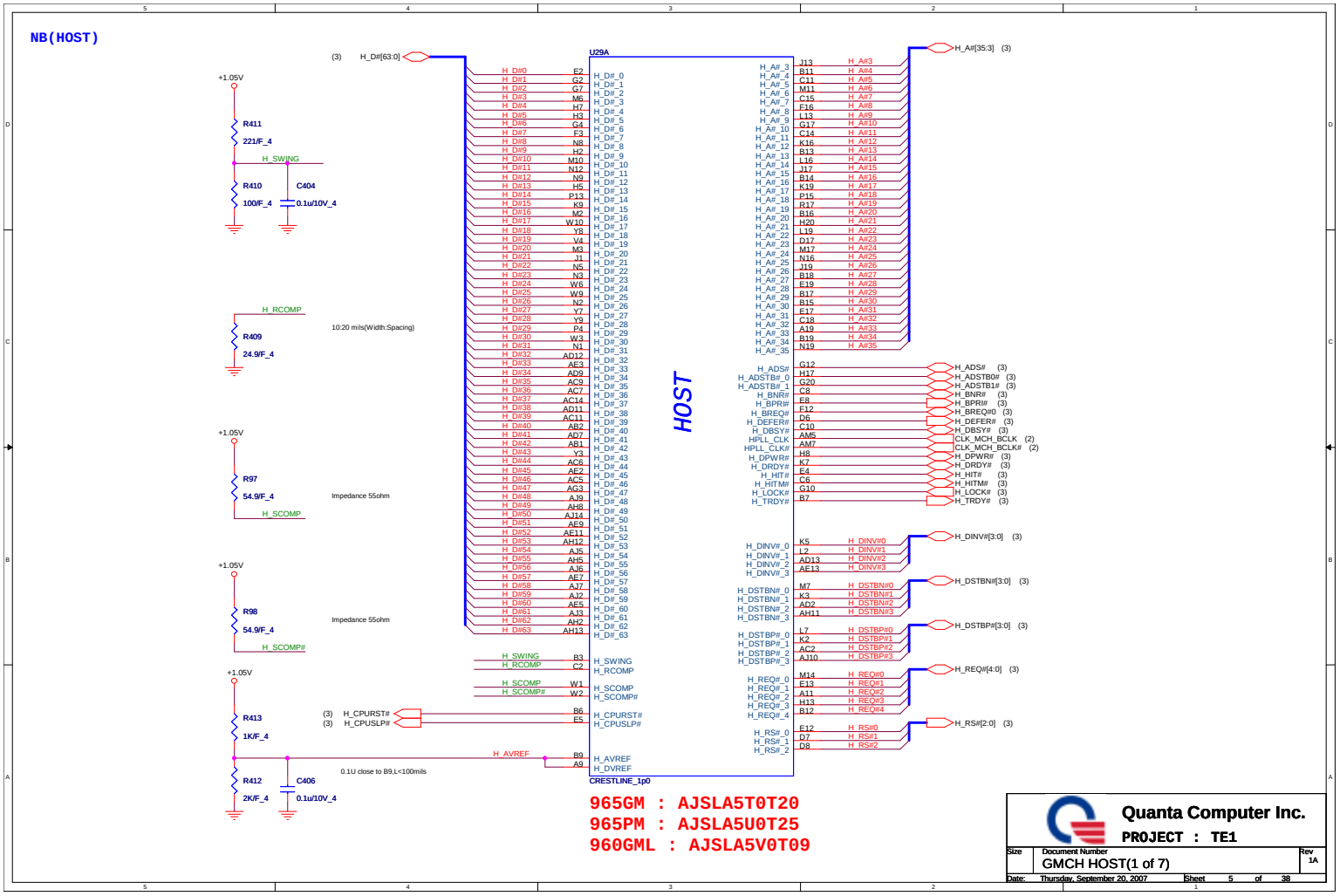


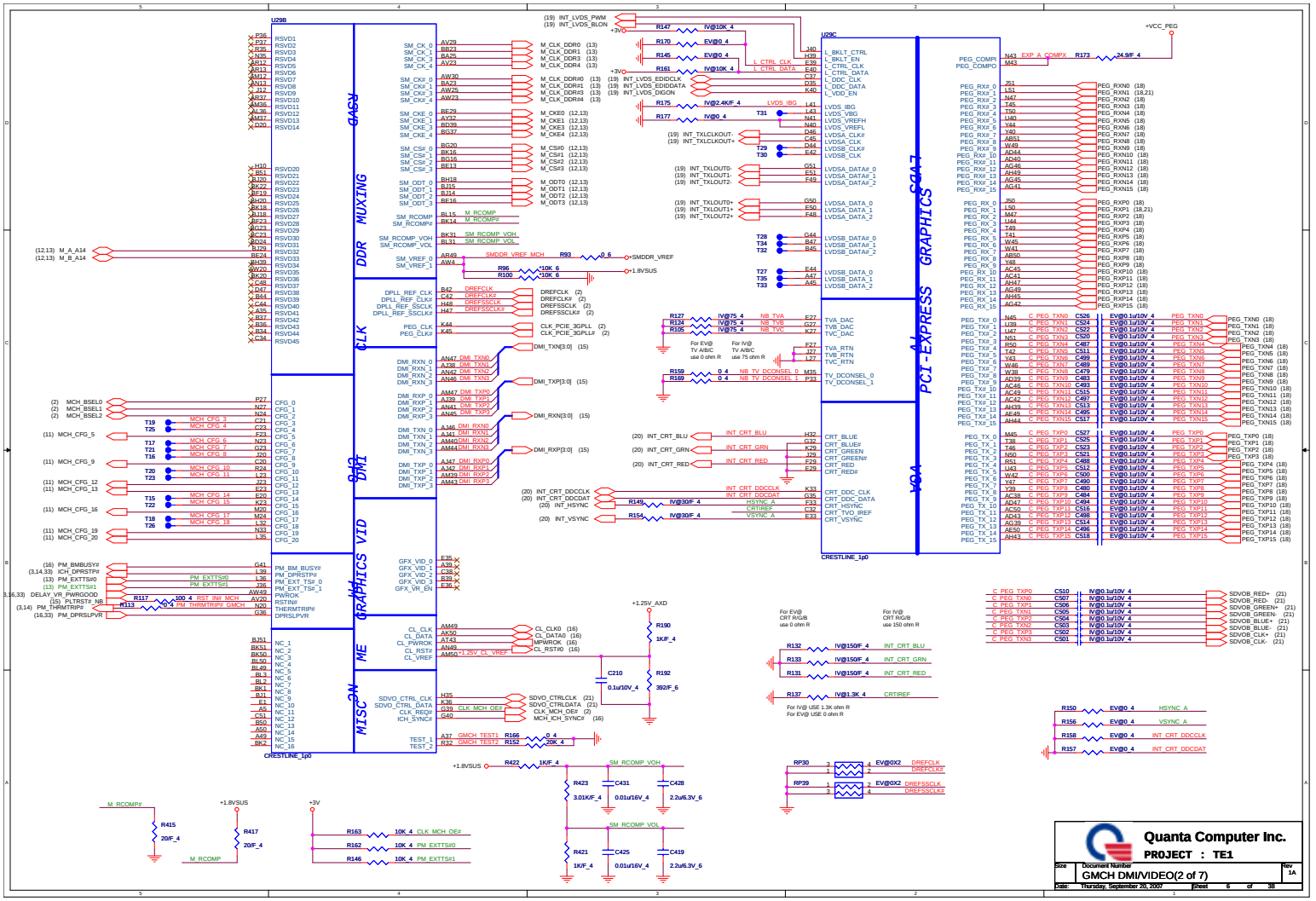


	ICS9LPRS365 (ALPRS365K13)	RTM875T-606 (AL000875K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

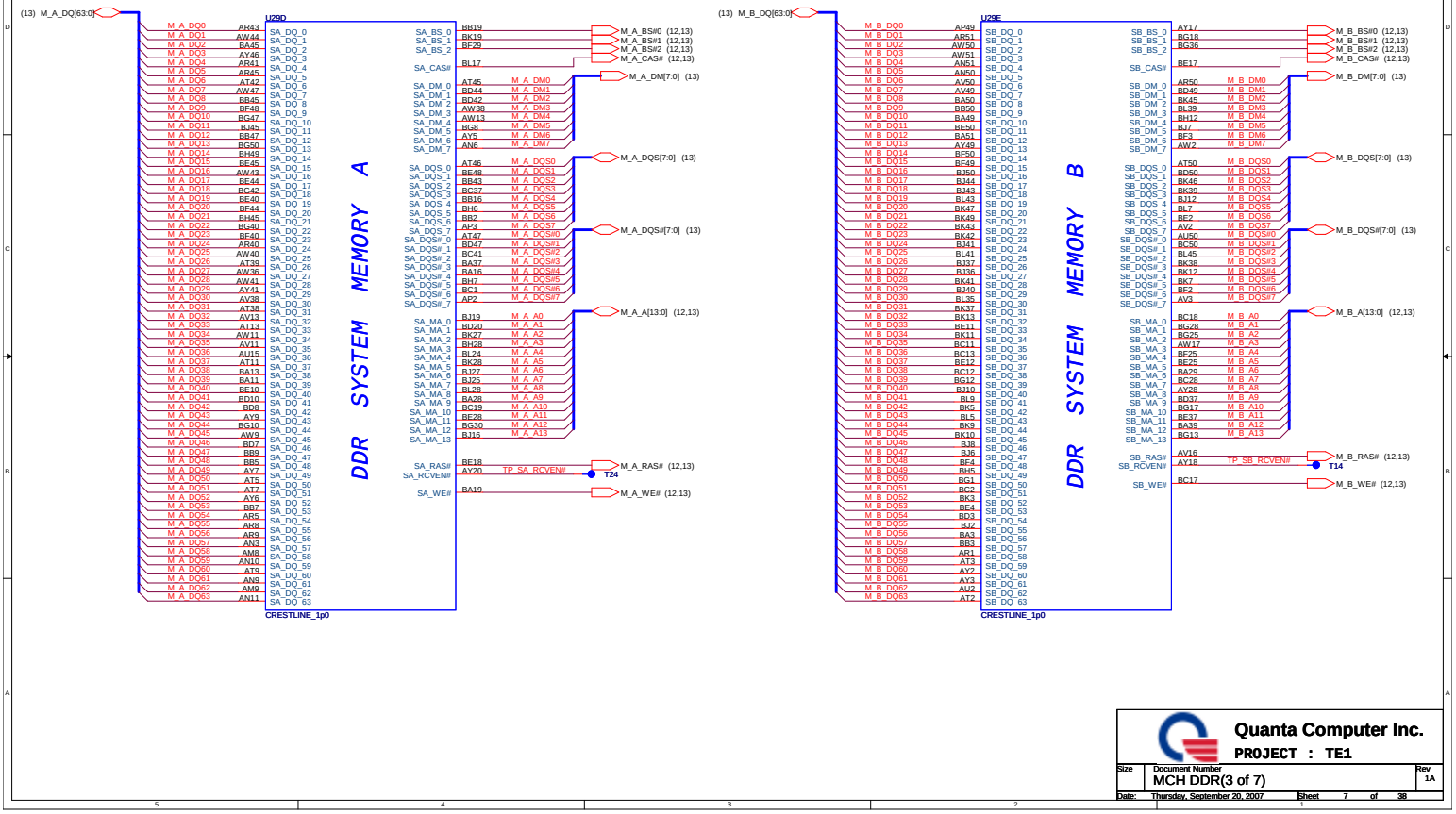








NB(Memory controller)



Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	MCH DDR(3 of 7)	1A
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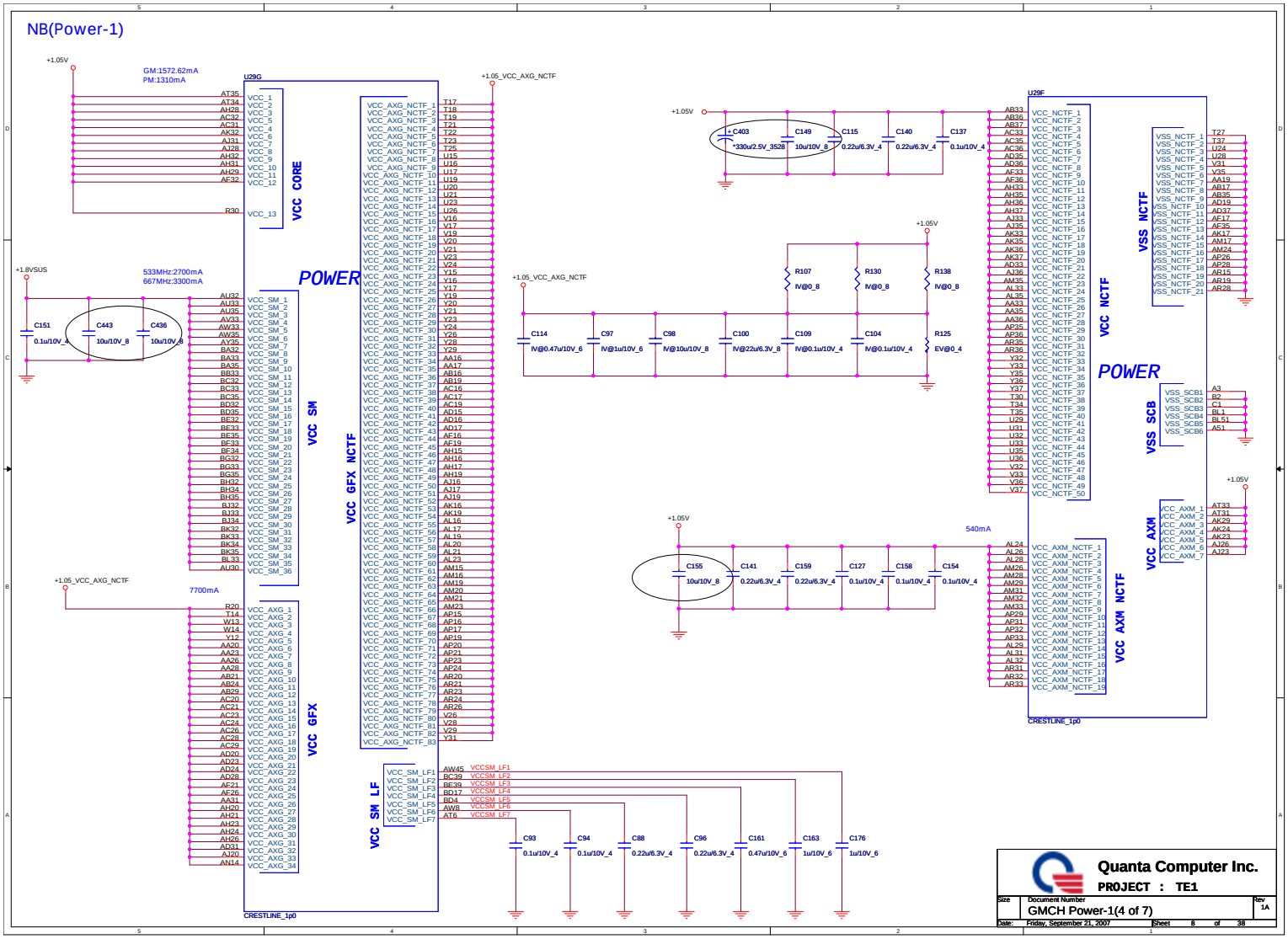
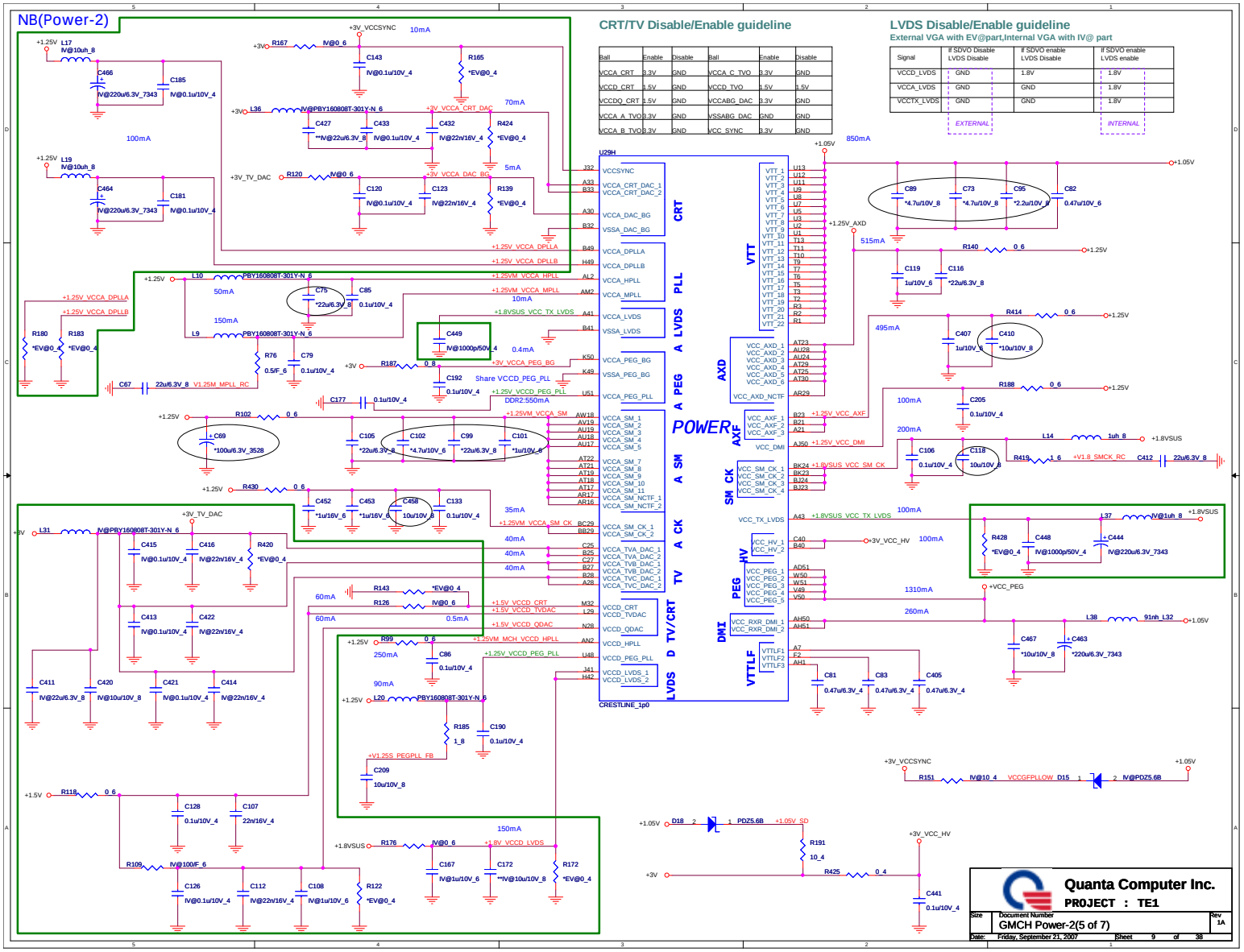
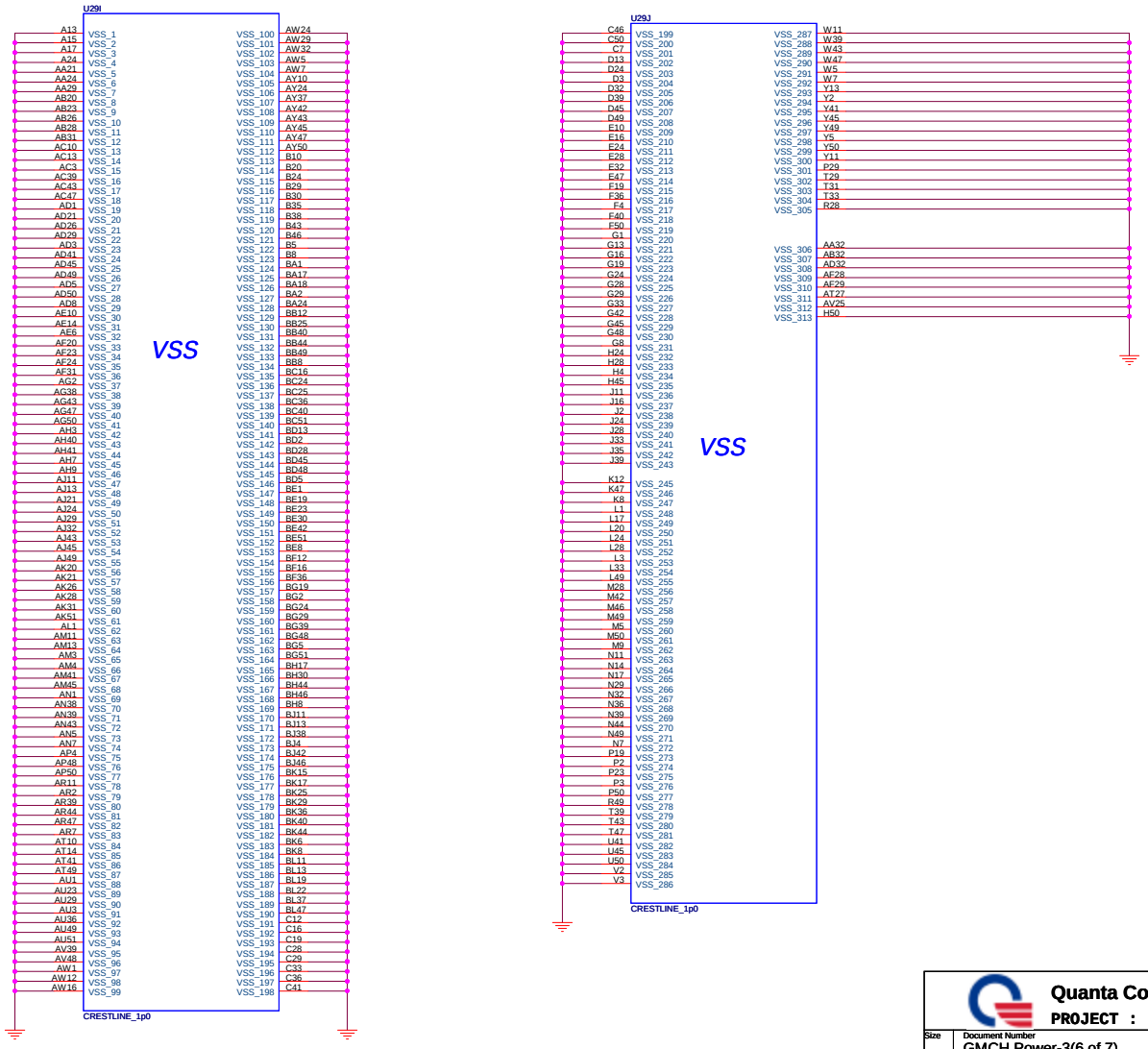
PROJECT : ZU1
Quanta Computer I





NB(Power-3)



Quanta Computer Inc.

PROJECT : TE1

Size	Document Number	Rev
	GMCH Power-3(6 of 7)	1A

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Strap table(base on checklist Ver1.6)

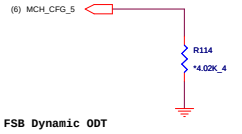
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	Intel? Management Engine Crypto strap	0 = Intel? Management Engine Crypto Transport Layer.Security (TLS) cipher suite with no confidentiality 1= Intel Management Engine Crypto TLS Cipher Suite with confidentiality (default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE is operation(Default) 1 = SDVO and PCIE are operating simultaneously via the PEG port

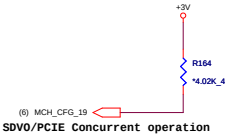
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

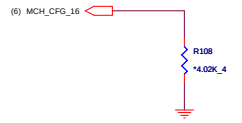
MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

SDVO Present

Strap define at External HDMI control page

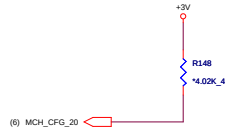
FSB Dynamic ODT

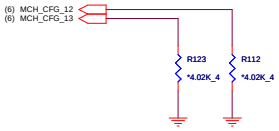
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE is operational(Default) High = SDVO andPCIE are operating simultaneously via the PEG port





Quanta Computer Inc.
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	GMCH Strap(7 of 7)	1A

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DDR2 Dual channel A/B PU

M_A_A[13..0] → M_A_A[13..0] (7,13)

M_B_A[13..0] → M_B_A[13..0] (7,13)

DDRII A CHANNEL

+SMDDR_VTERM

C148 C165 C121 C132 C183 C174 C162 C147 C142 C194 C193 C195 C134

0.1u/10V_4

DDRII B CHANNEL

+SMDDR_VTERM

C202 C171 C124 C139 C125 C196 C203 C169 C160 C144 C178 C199 C152

0.1u/10V_4

Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

M_A_A3 M_A_A1 — RP28 — 56X2 — +SMDDR_VTERM

M_A_A9 M_A_A5 — RP34 — 56X2

M_A_A2 M_A_A4 — RP32 — 56X2

(6,13) M_CKE1 — M_A_A11 — RP40 — 56X2

(6,13) M_CKE0 — M_A_A8 — RP38 — 56X2

(7,13) M_A_BS#2 — M_A_A12 — RP41 — 56X2

(7,13) M_A_BS#1 — M_A_A0 — RP25 — 56X2

M_B_A10 RP26 56X2 +SMDDR_VTERM

(7,13) M_B_WE#

M_B_A3 M_B_A1 — RP29 — 56X2

(7,13) M_B_BS#1 — M_B_A0 — RP27 — 56X2

M_B_A7 M_B_A11 — RP35 — 56X2

M_B_A8 M_B_A5 — RP33 — 56X2

M_B_A2 M_B_A4 — RP31 — 56X2

M_B_A9 M_B_A12 — RP36 — 56X2

(6,13) M_A_A14 (6,13) M_B_A14 — R181 56_4 R178 56_4 — +SMDDR_VTERM

M_A_A7 M_A_A6 — RP37 — 56X2 — +SMDDR_VTERM

(6,13) M_CKE3 (7,13) M_B_BS#2 — RP43 — 56X2

(6,13) M_ODT1 (6,13) M_CS#1 — RP18 — 56X2

(6,13) M_ODT3 (7,13) M_B_BS#0 — RP19 — 56X2

M_A_A10 — RP24 — 56X2

(7,13) M_A_BS#0

(7,13) M_A_CAS# (7,13) M_A_WE# — RP21 — 56X2

(6,13) M_CS#0 (7,13) M_A_RAS# — RP23 — 56X2

(7,13) M_B_CAS# (6,13) M_CS#3 — RP22 — 56X2

M_B_A6 — RP42 — 56X2

(6,13) M_CKE4

(6,13) M_ODT2 (7,13) M_B_RAS# — RP20 — 56X2

(6,13) M_ODT0 — M_A_A13 — RP16 — 56X2

M_B_A13 — RP17 — 56X2

(6,13) M_CS#2

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	DDR RES. ARRAY	1A

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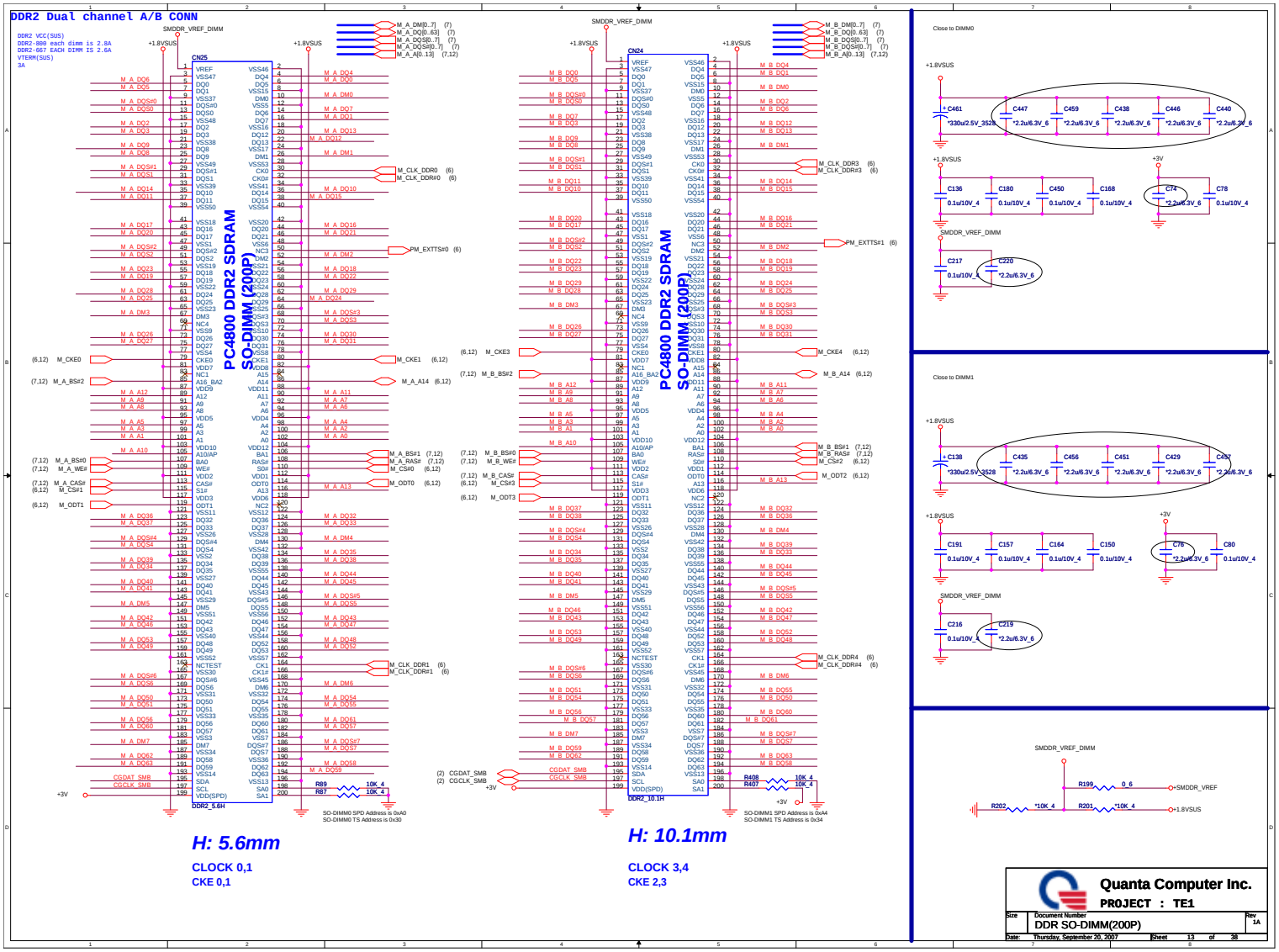
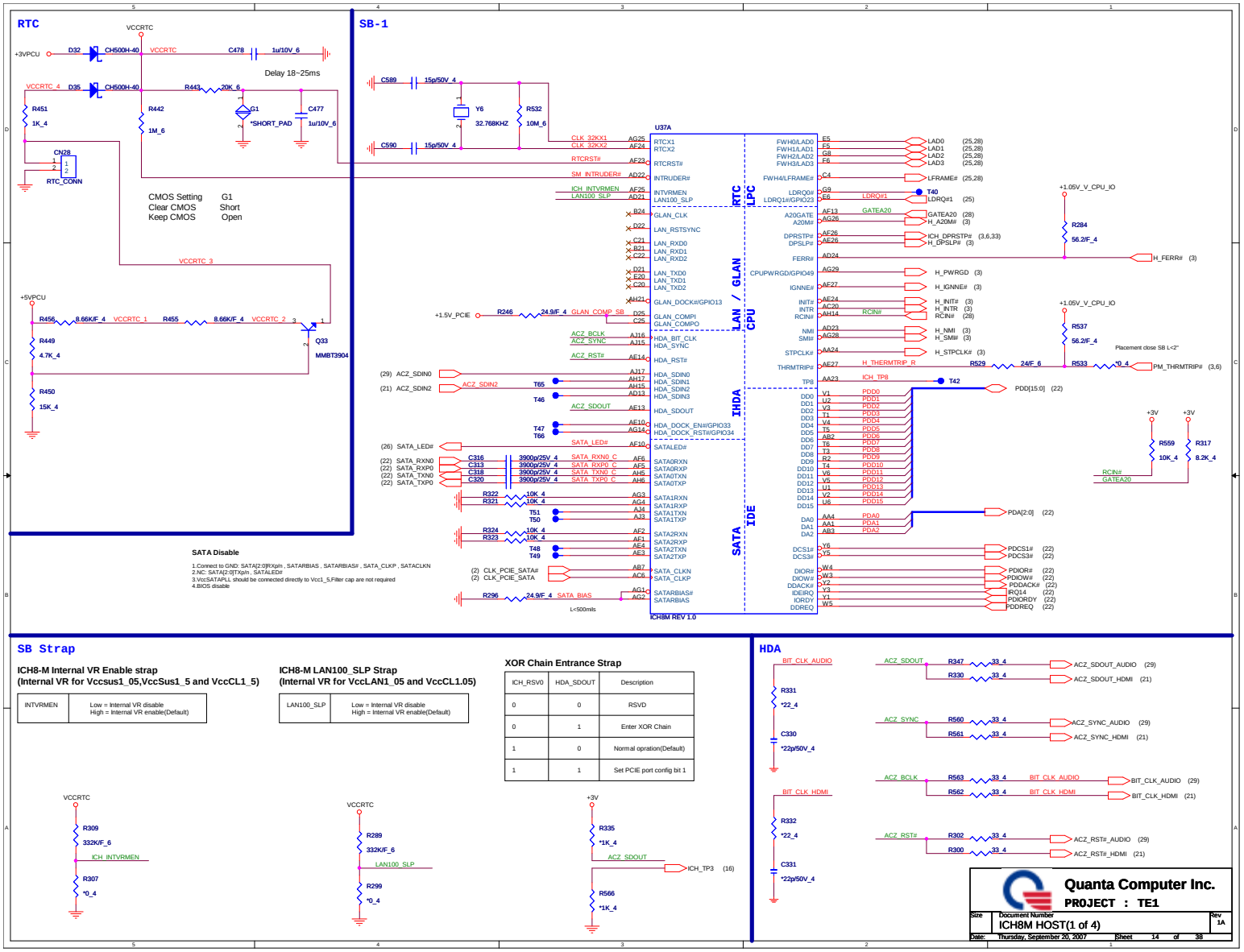
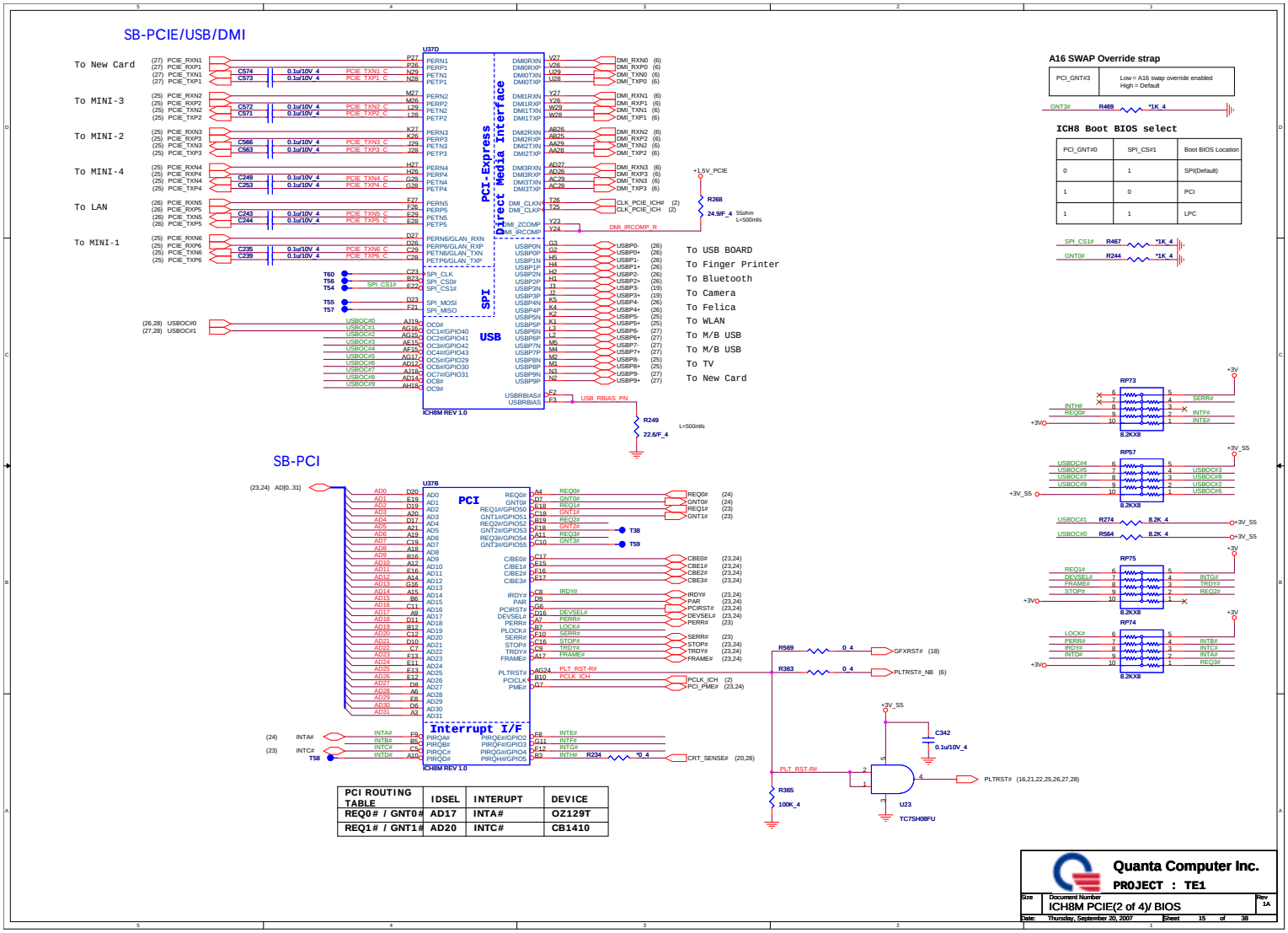
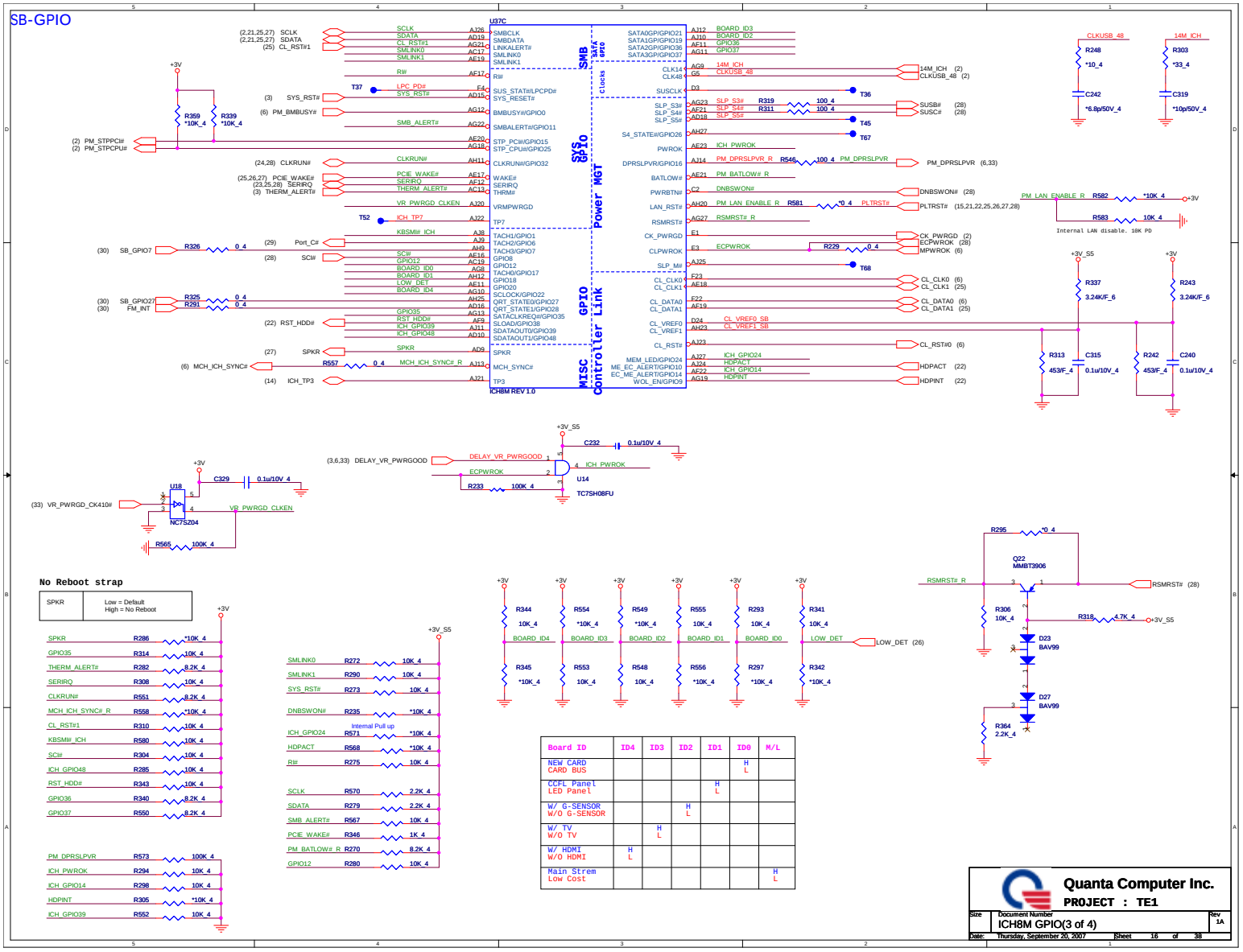
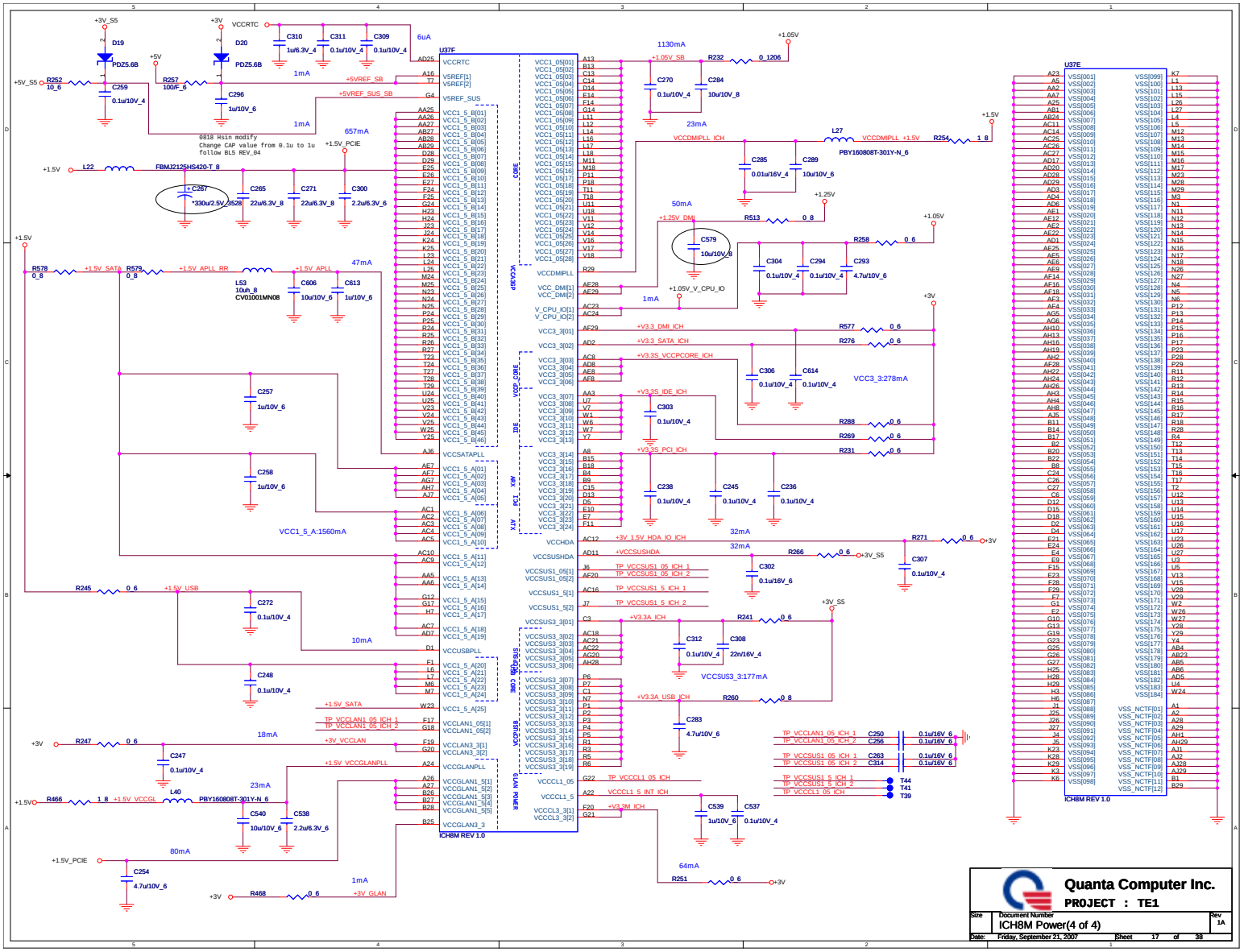
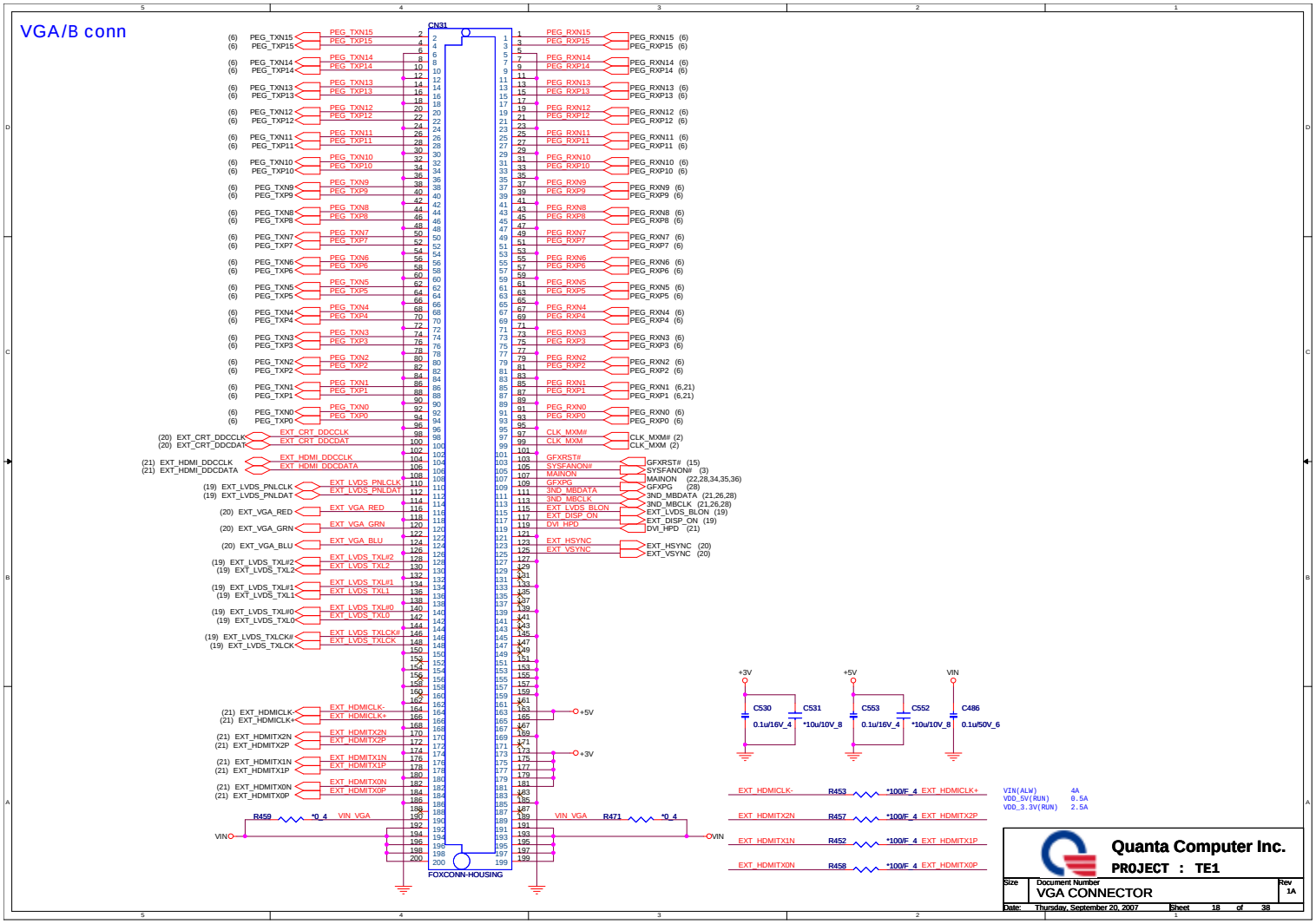


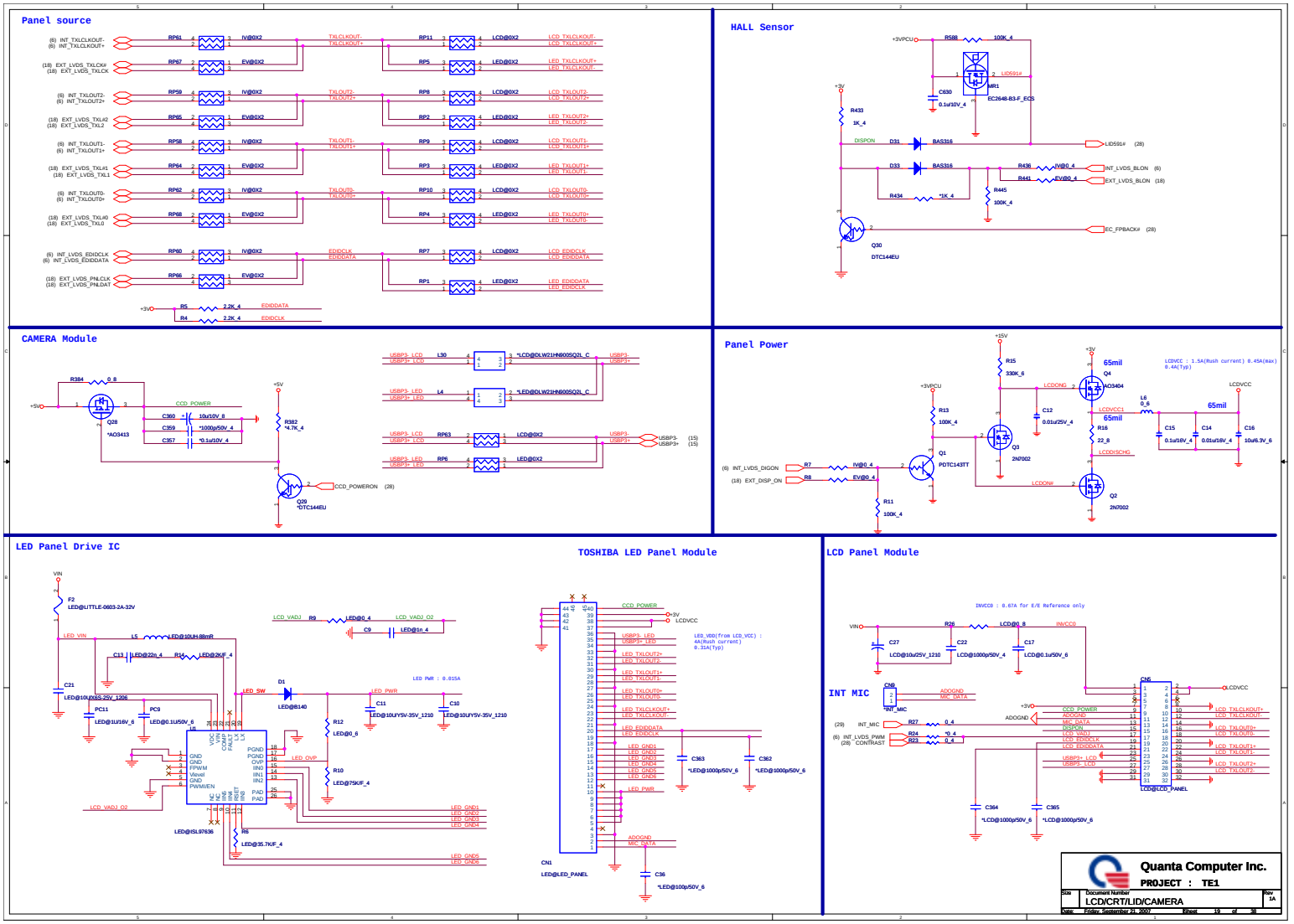


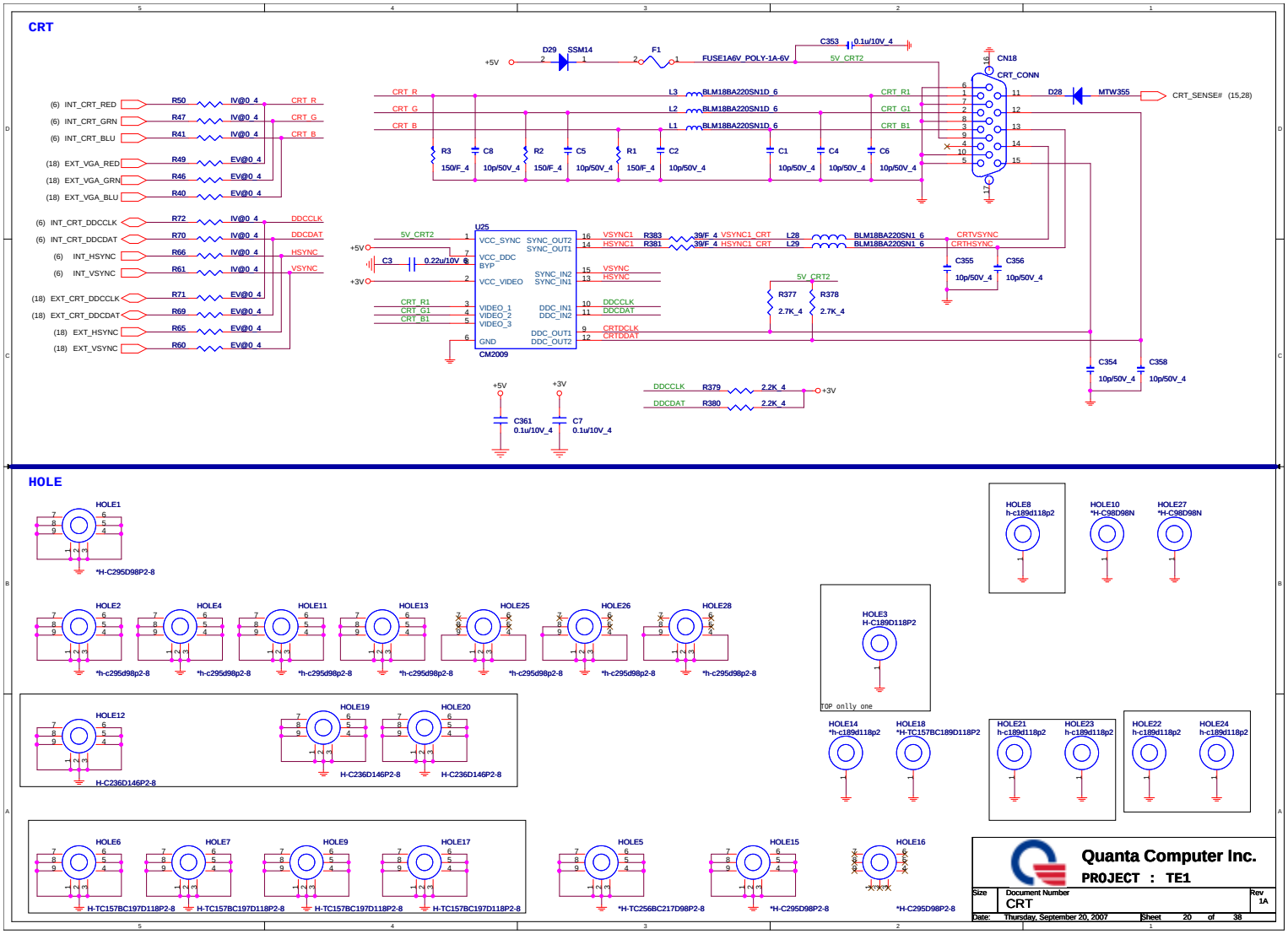


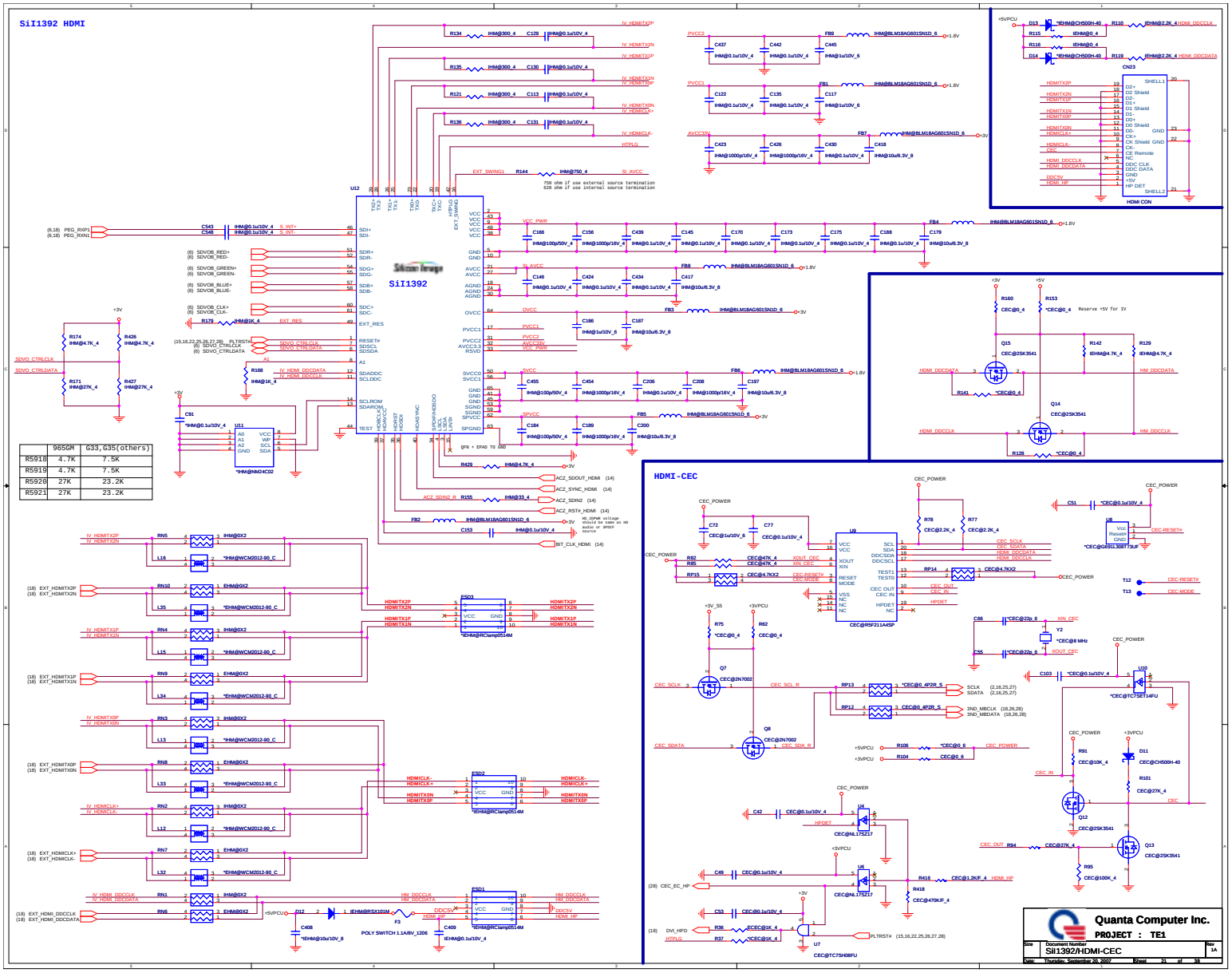




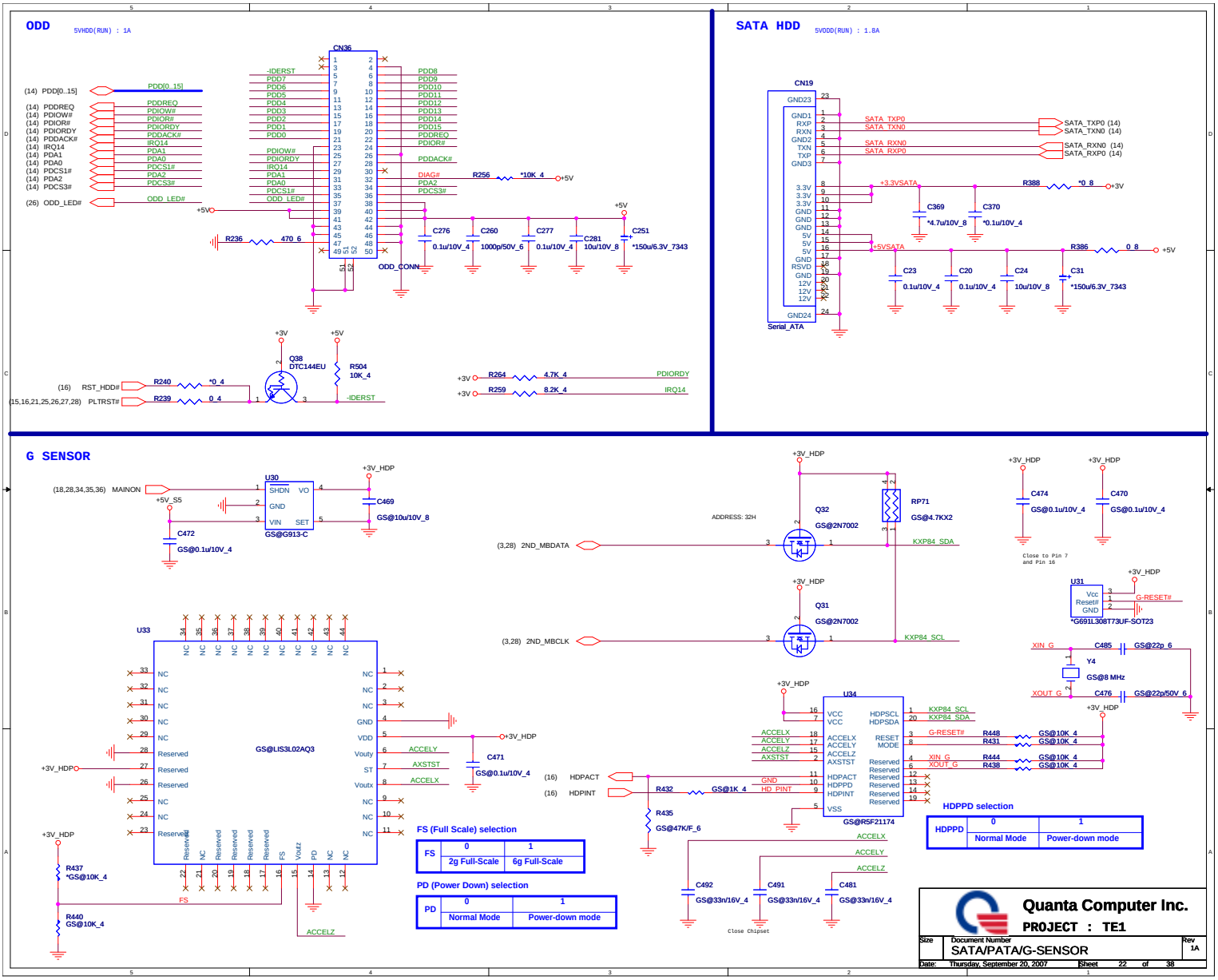


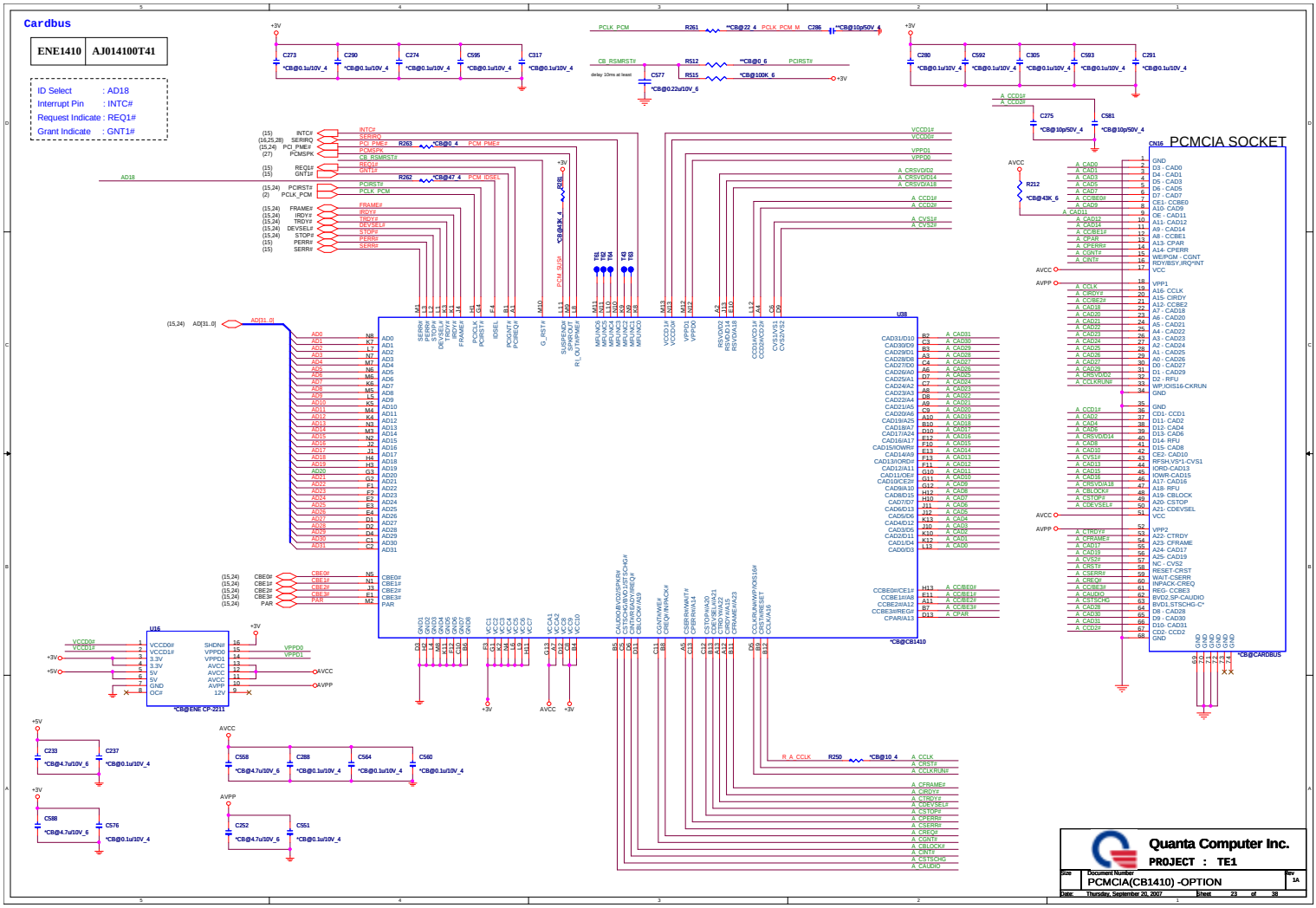


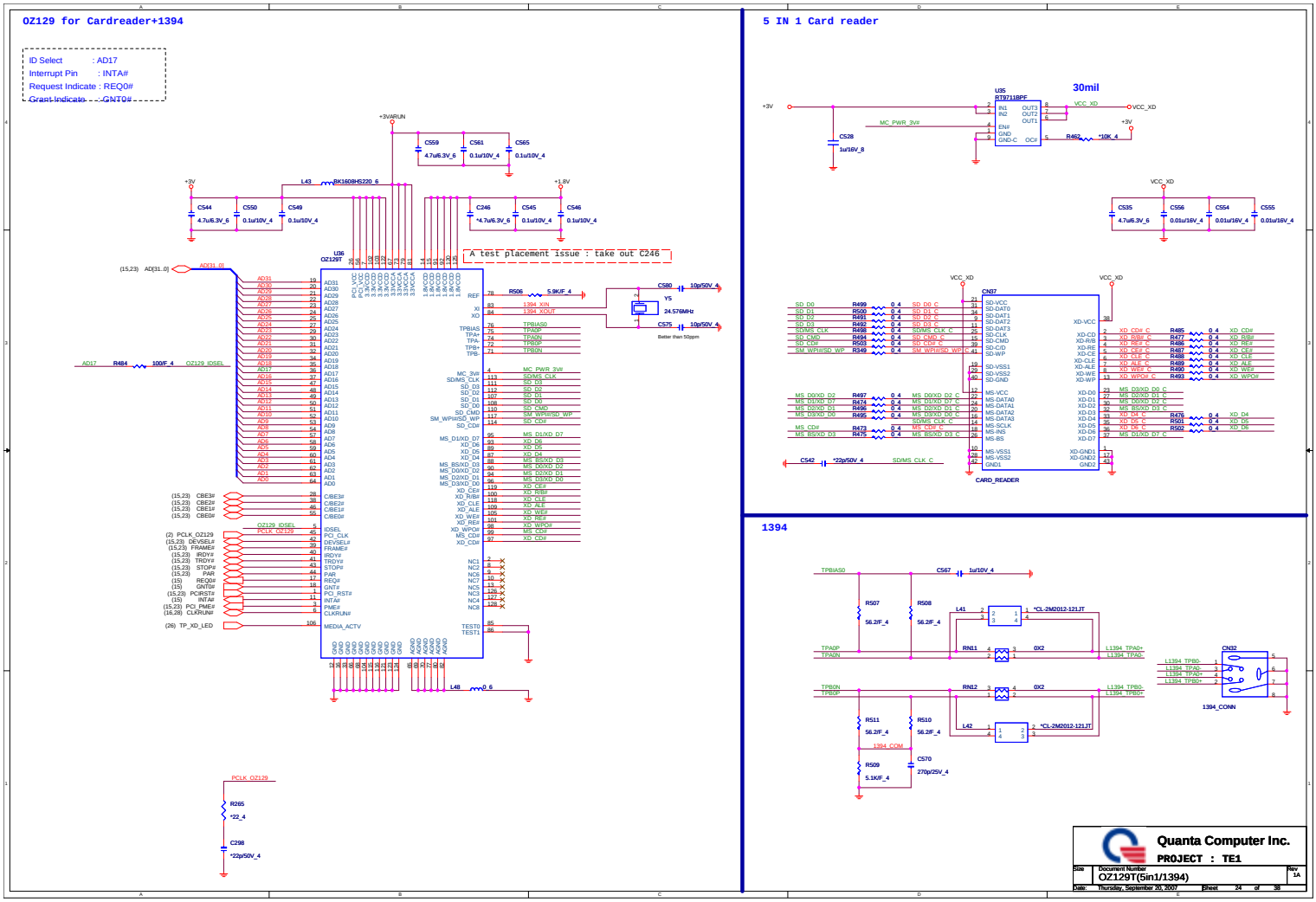


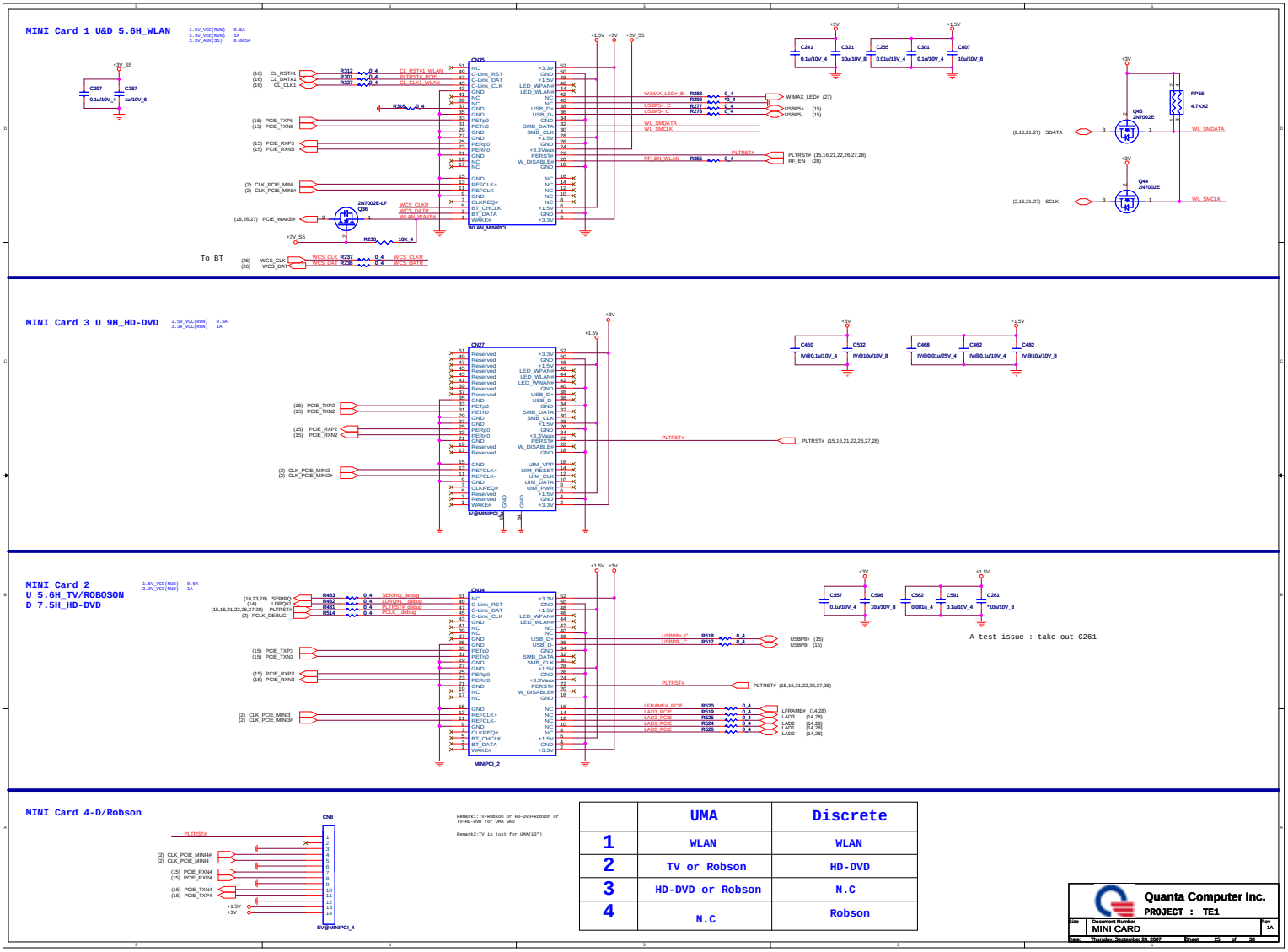


	965GM	G33,G35(others)
R5918	4.7K	7.5K
R5919	4.7K	7.5K
R5920	27K	23.2K
R5921	27K	23.2K









	UMA	Discrete
1	WLAN	WLAN
2	TV or Robson	HD-DVD
3	HD-DVD or Robson	N.C
4	N.C	Robson

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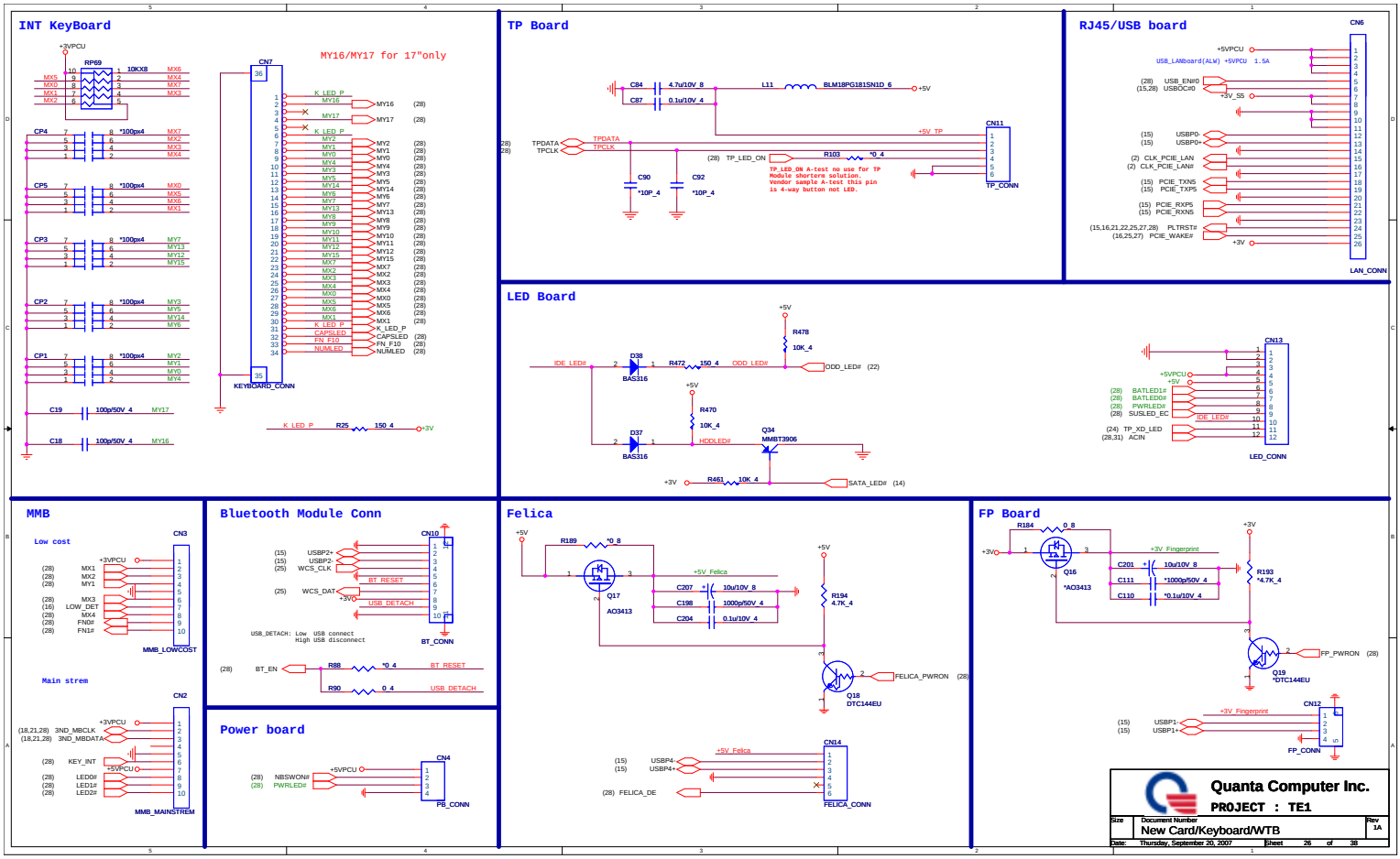

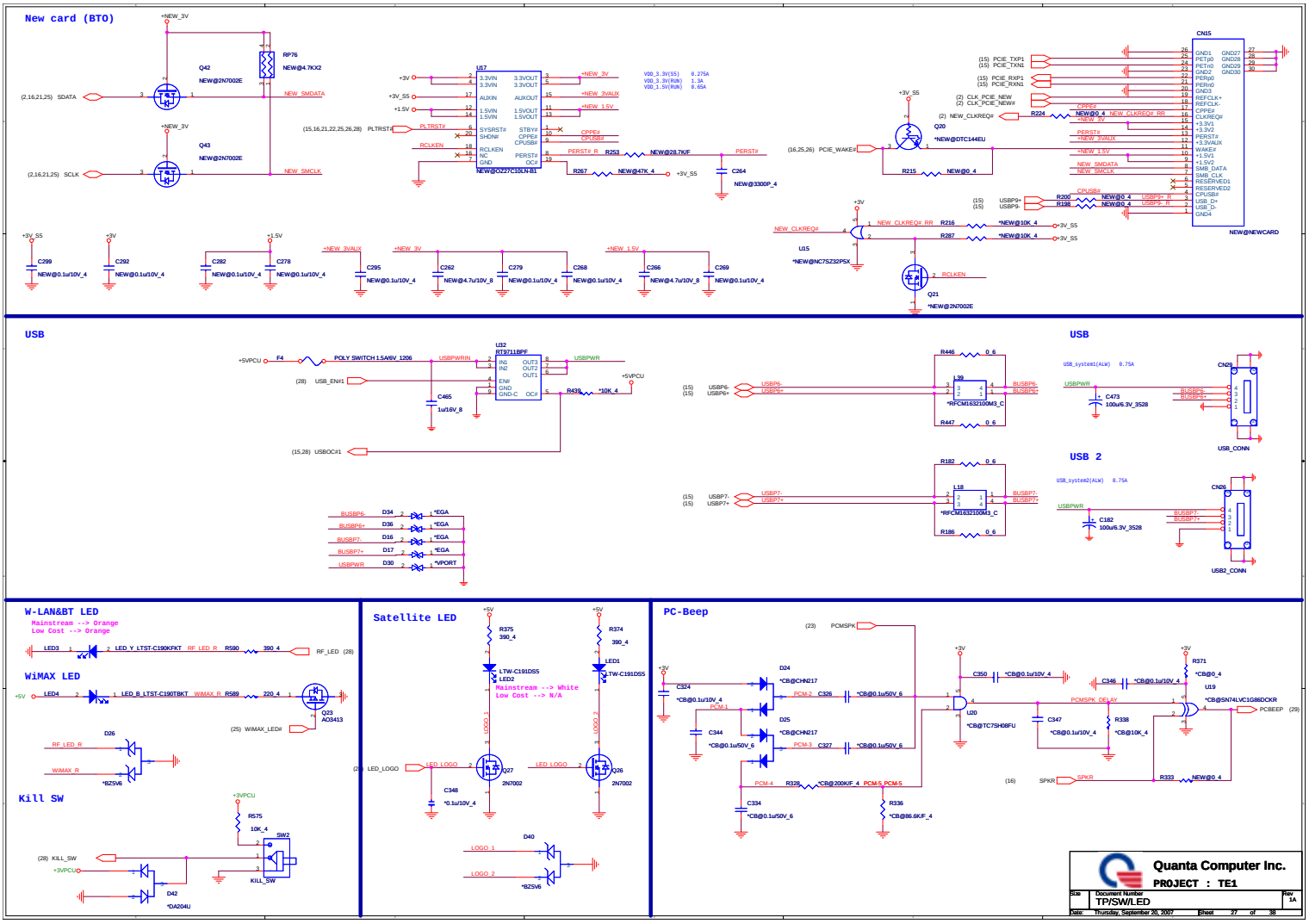

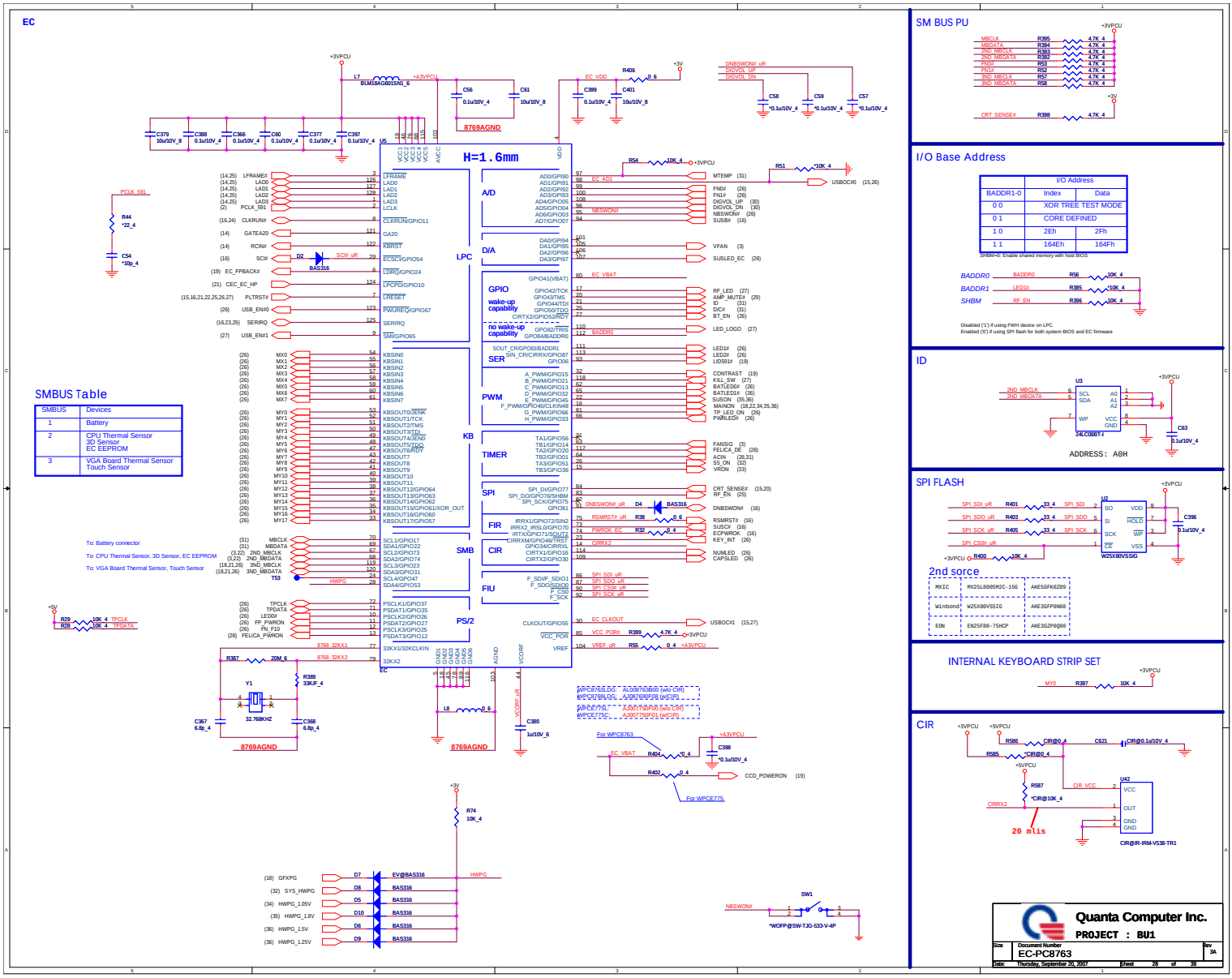

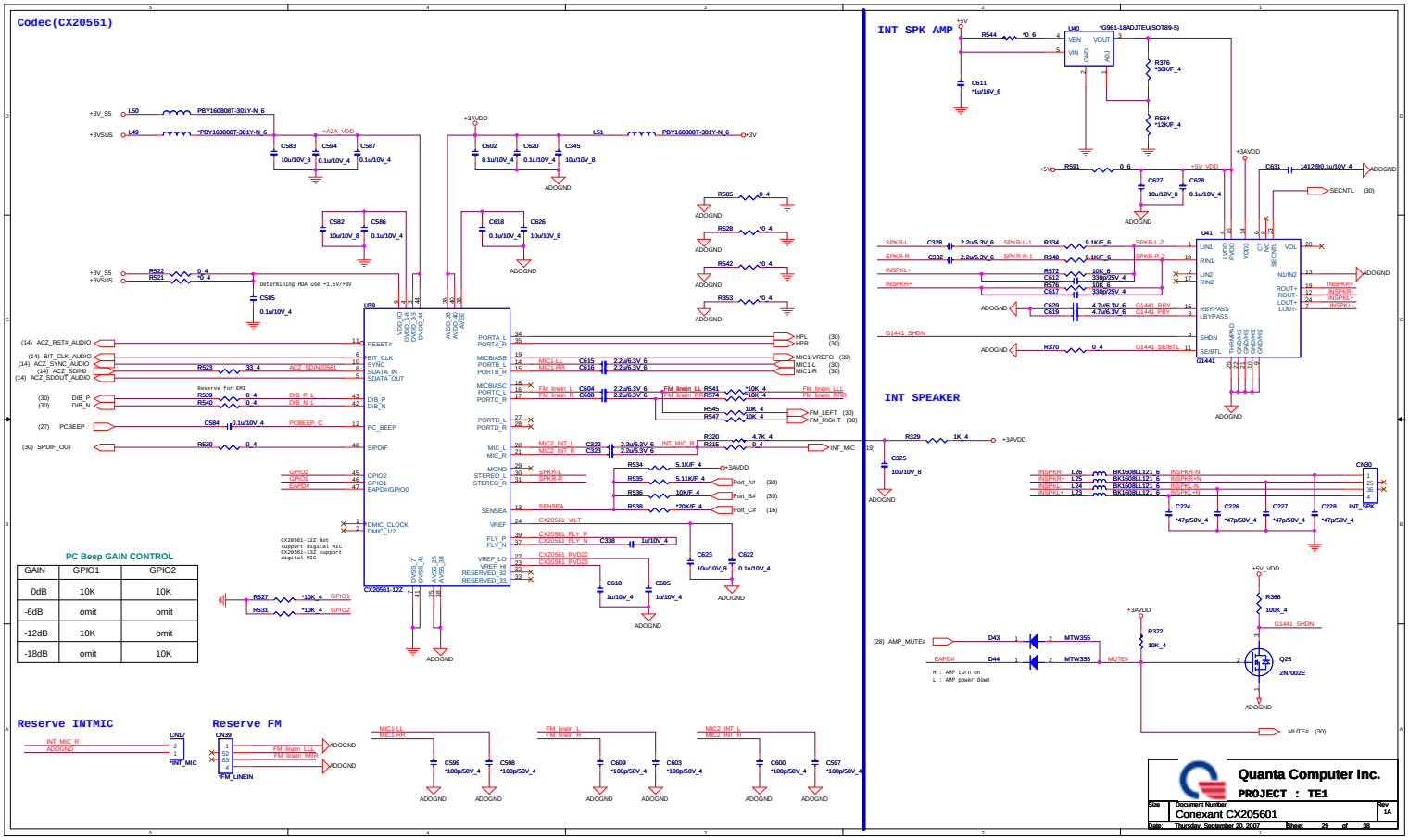

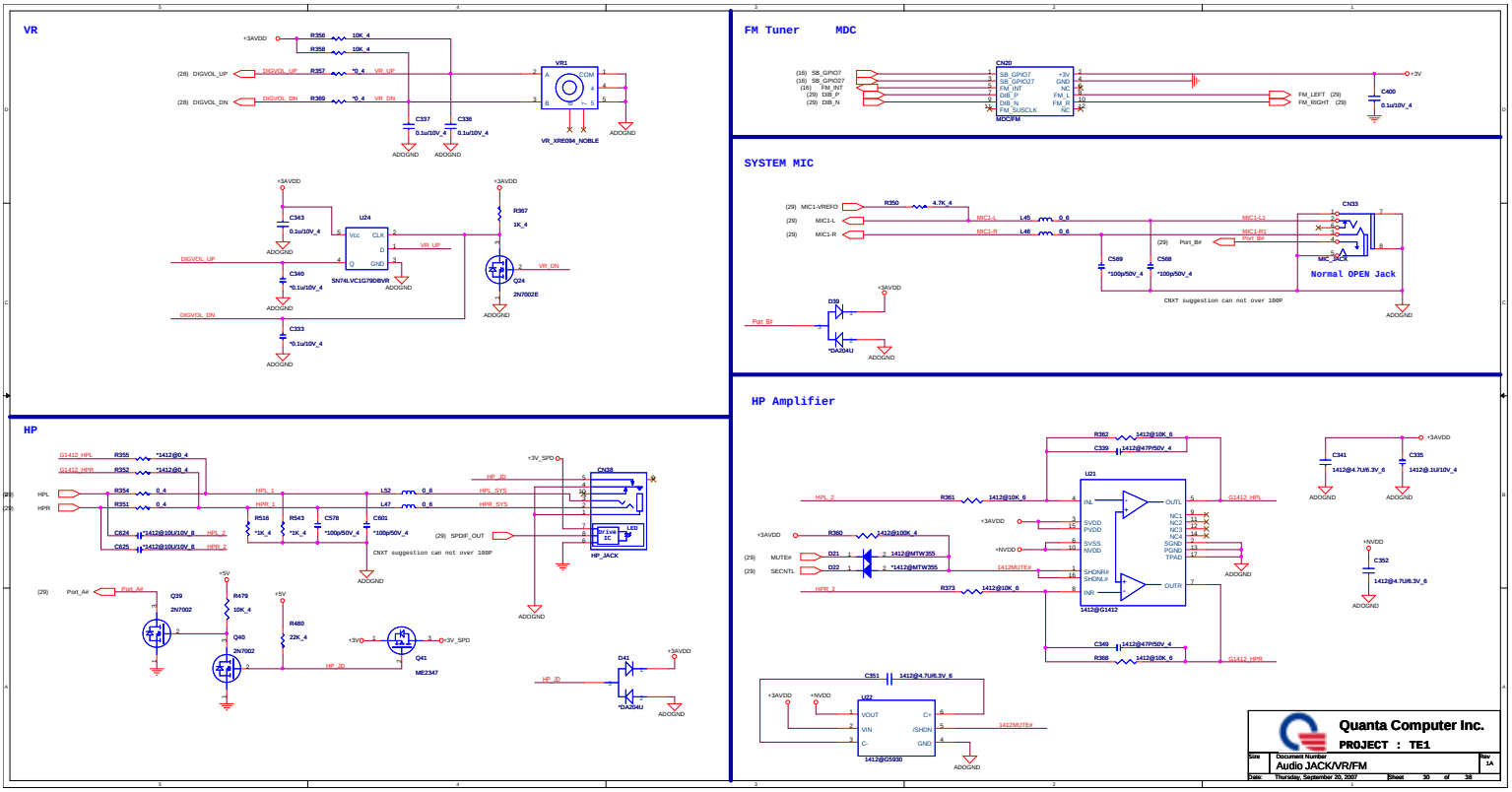

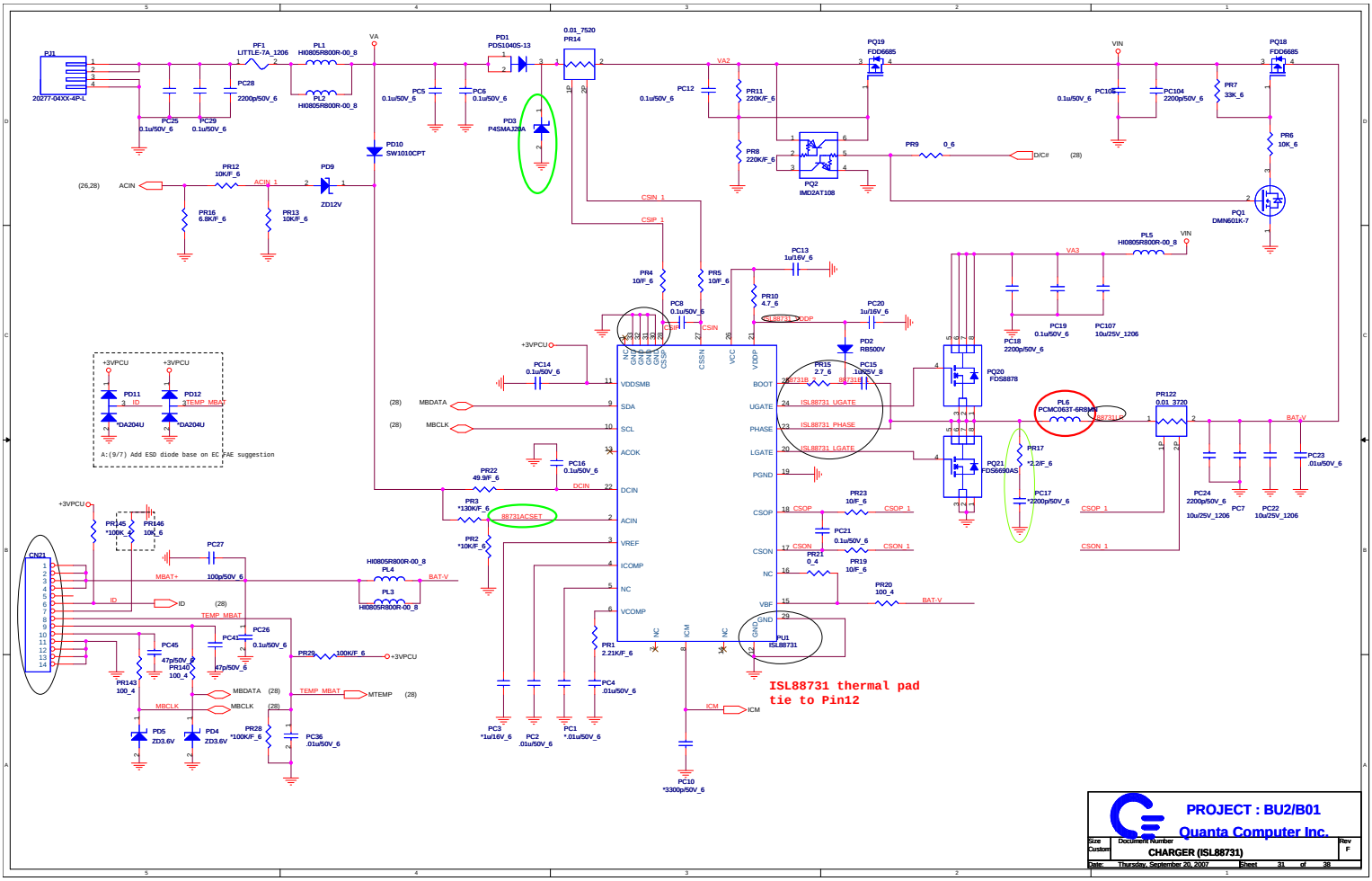

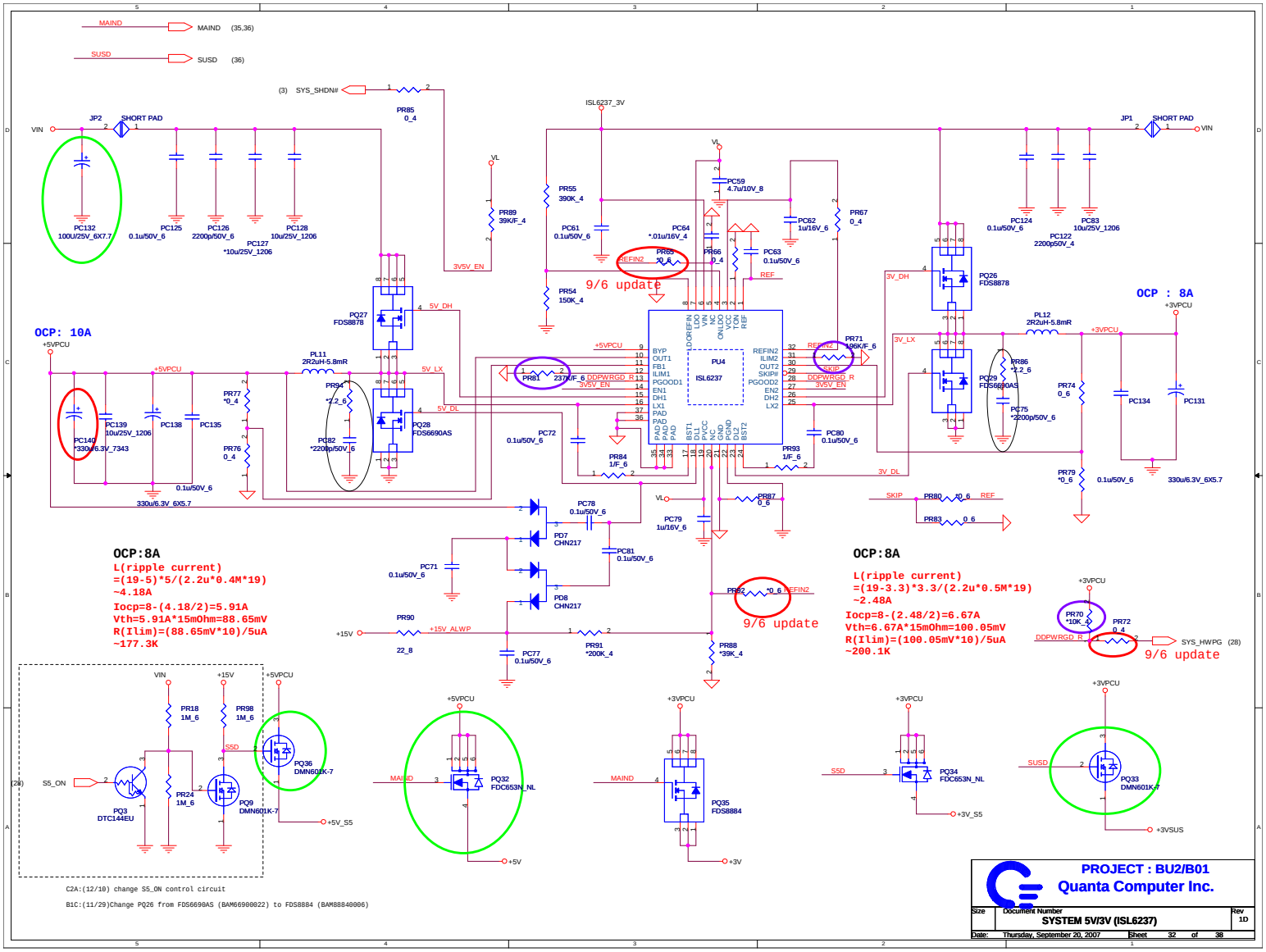

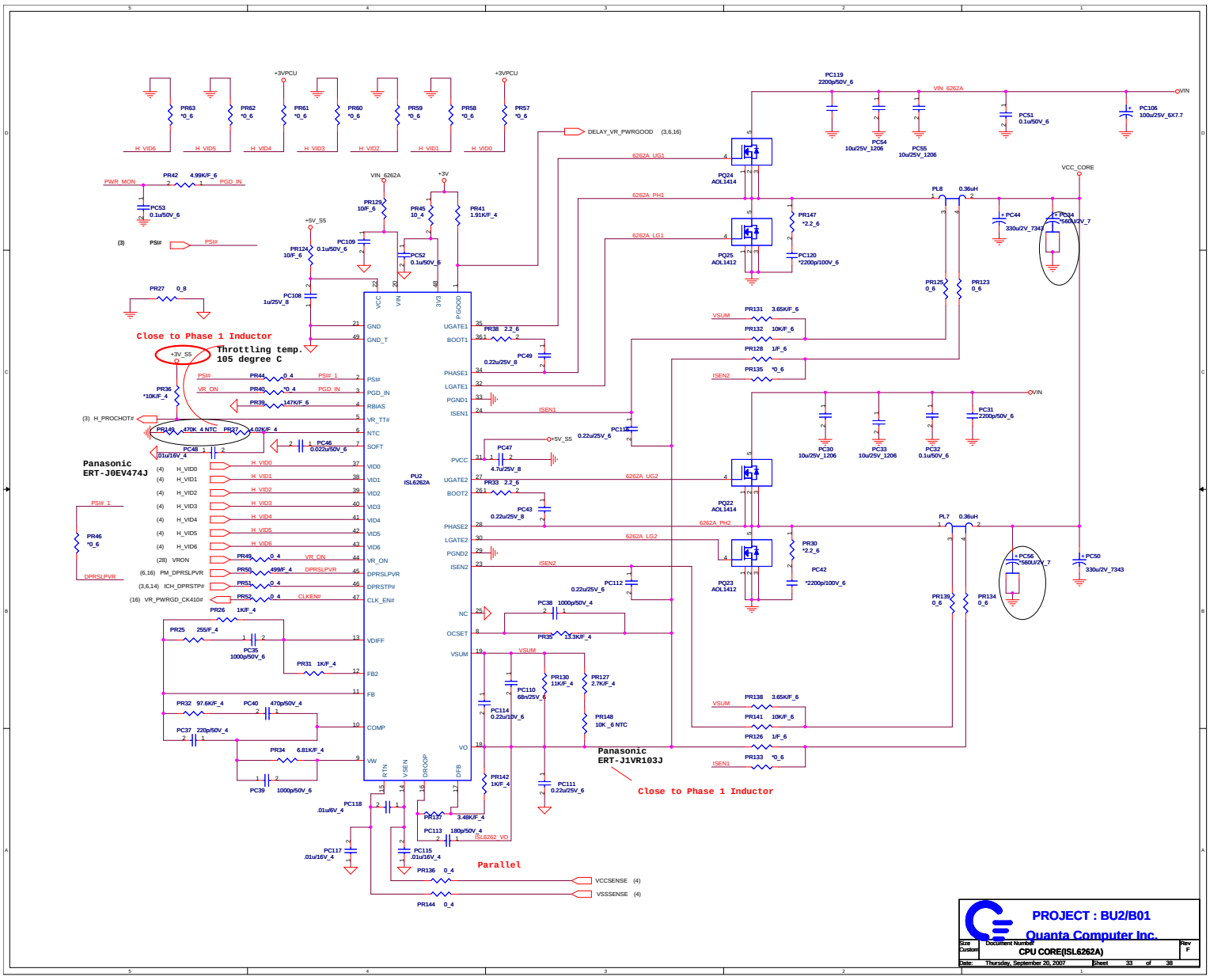

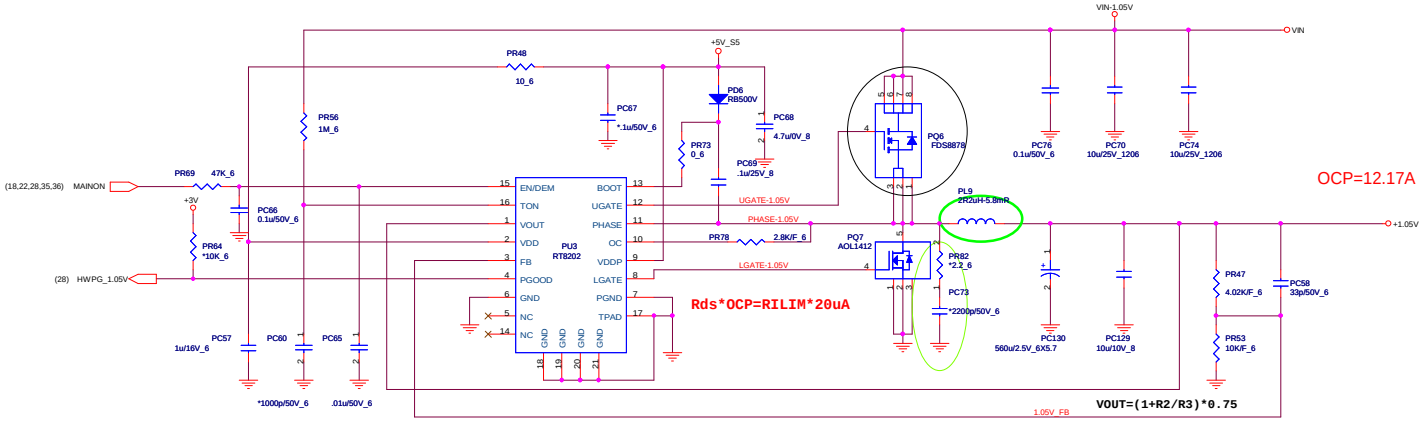

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

AO1412 Rds=4.6mOhm

12.17A OCP --- OC=2.8K(CS22803F914)

PROJECT : BU2/B01 Quanta Computer Inc.		
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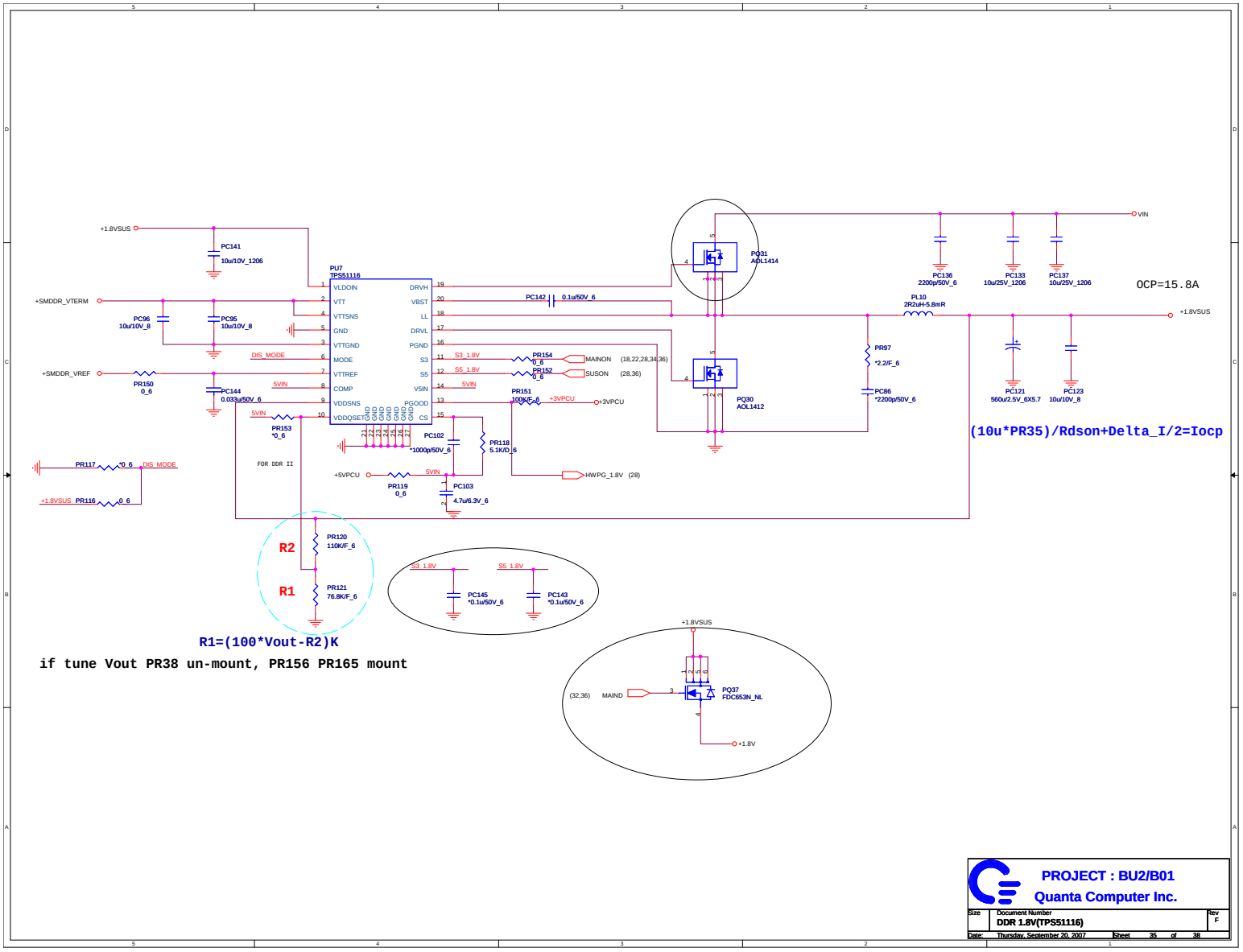

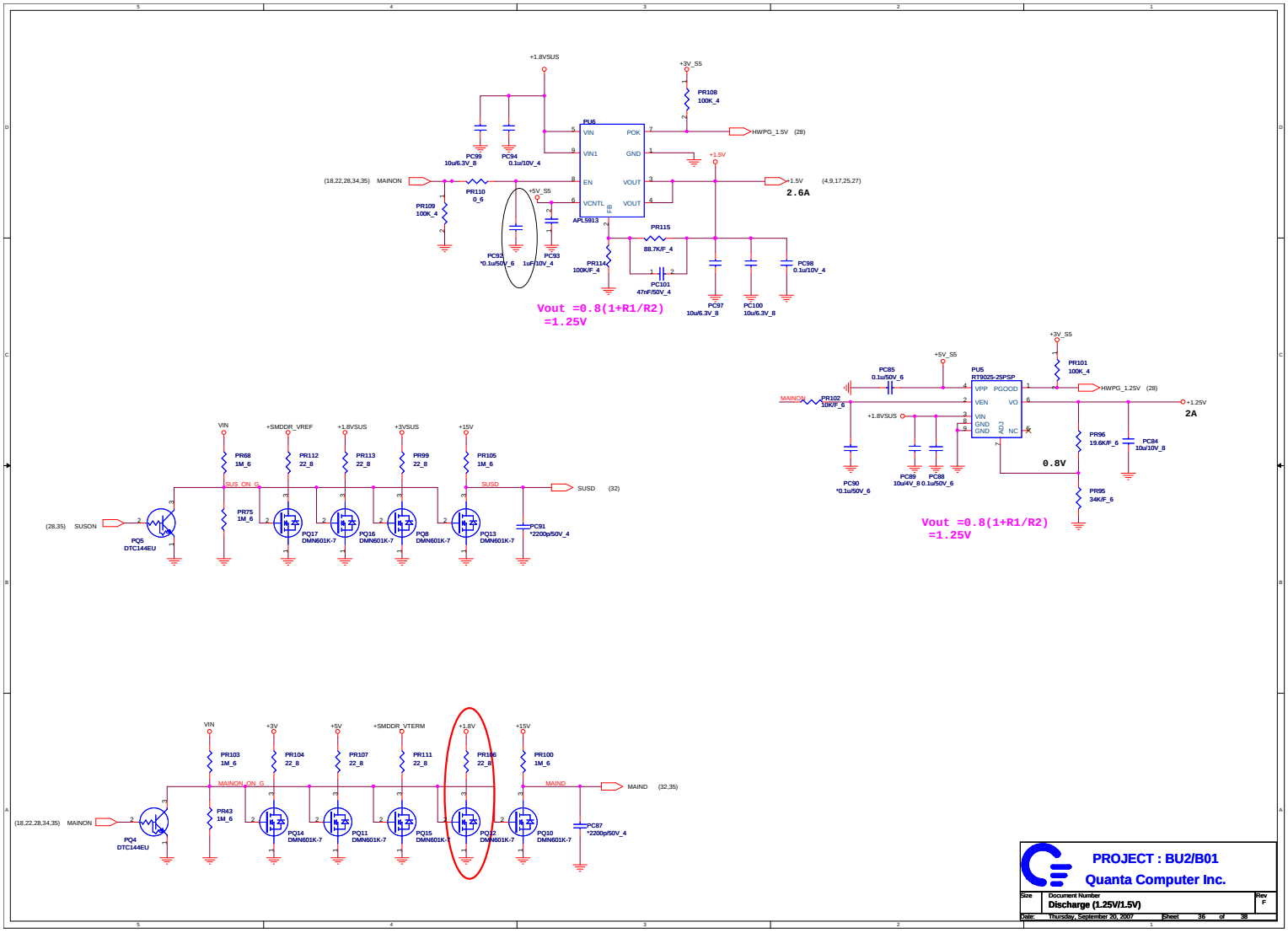

Model	REV	DATE	CHANGE LIST	NOTE
	01	20070824	FIRST RELEASED : 20070824	
TE1	02			

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	Change list	1A

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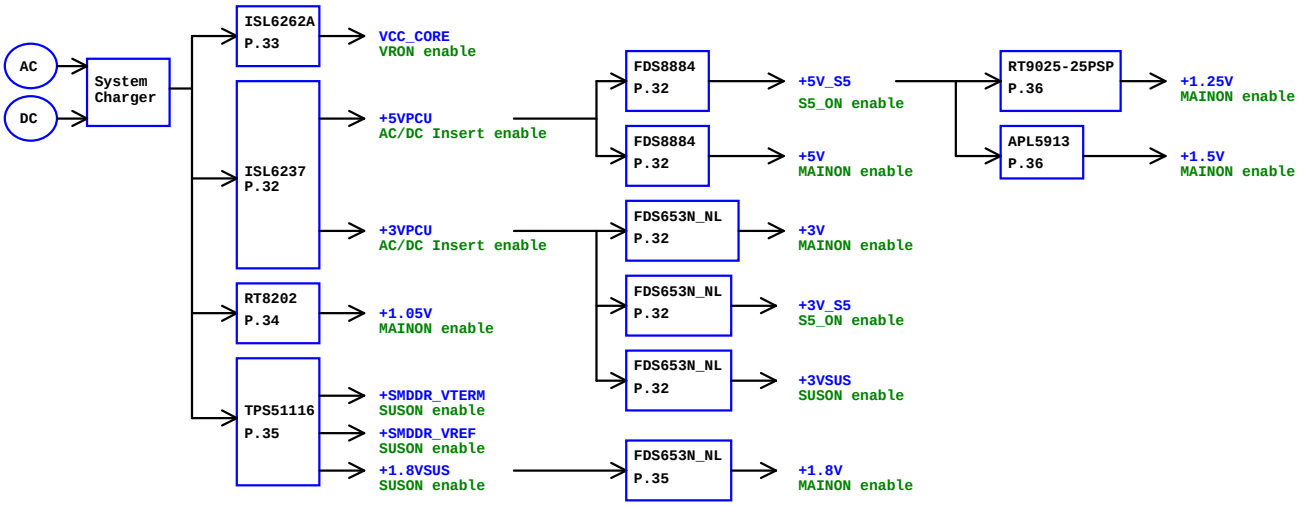
Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M

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