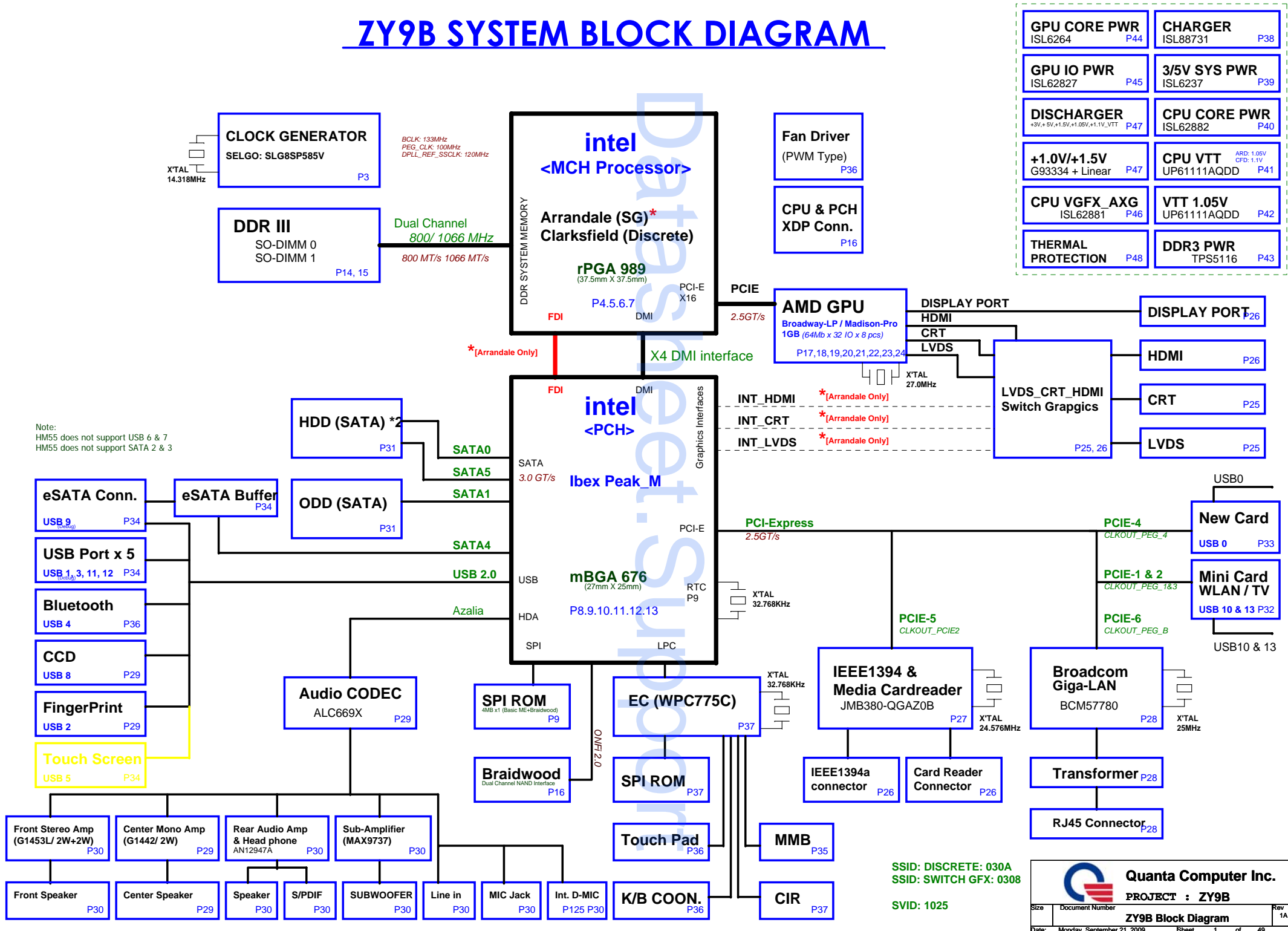


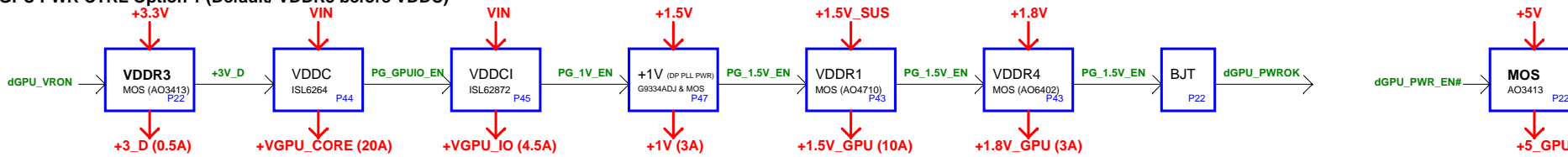
ZY9B SYSTEM BLOCK DIAGRAM



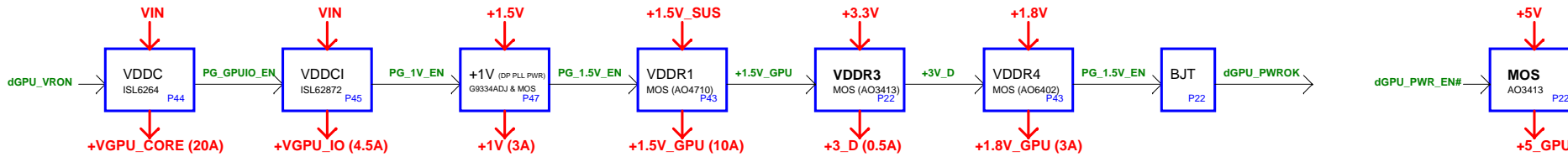
Note:
HMS5 does not support USB 6 & 7
HMS5 does not support SATA 2 & 3

SSID: DISCRETE: 030A
SSID: SWITCH GFX: 0308
SVID: 1025

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDR4)



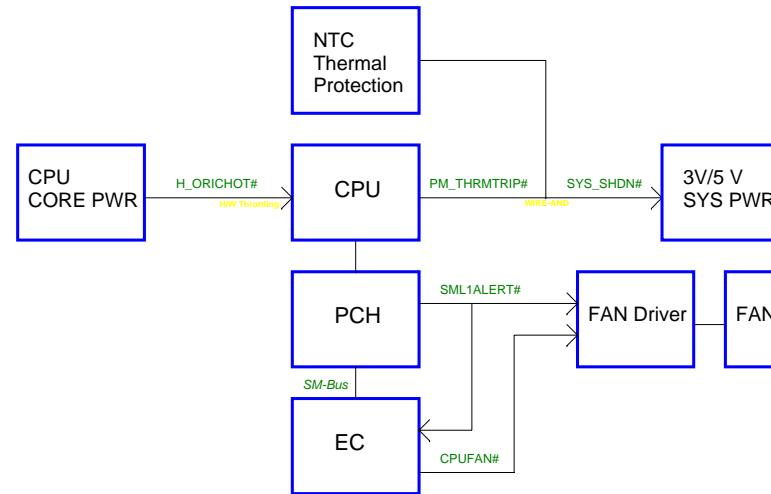
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

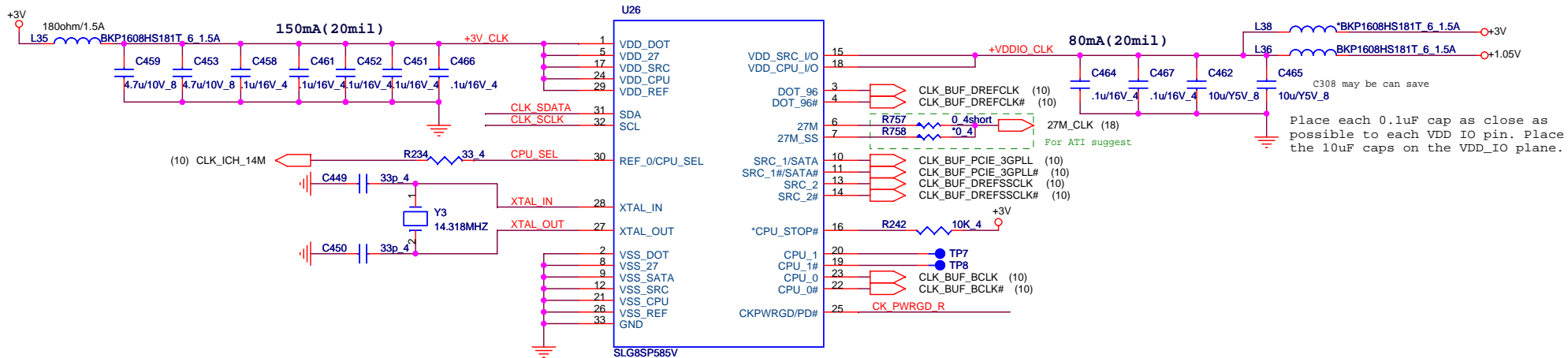


Power States

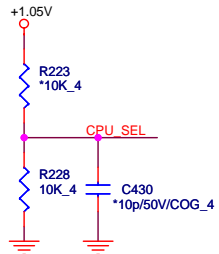
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



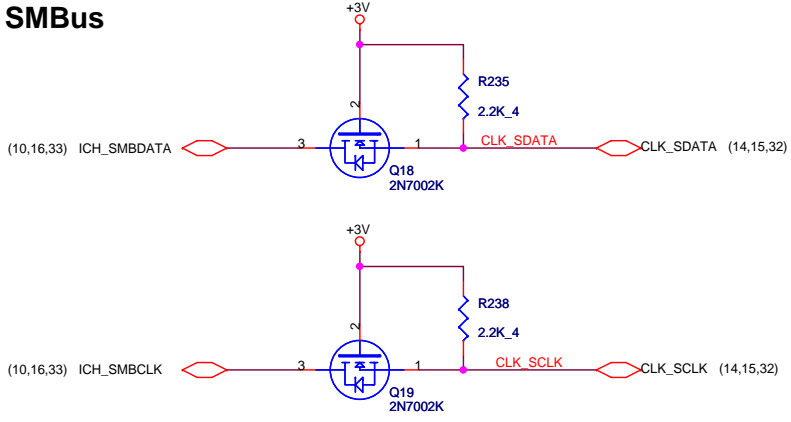


CPU_CLK select

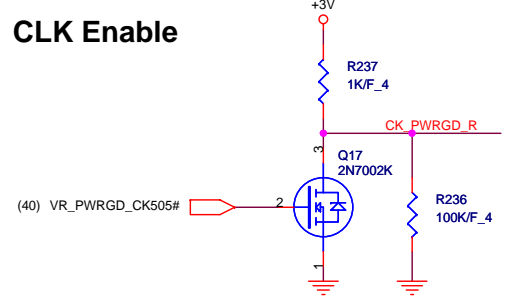



	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



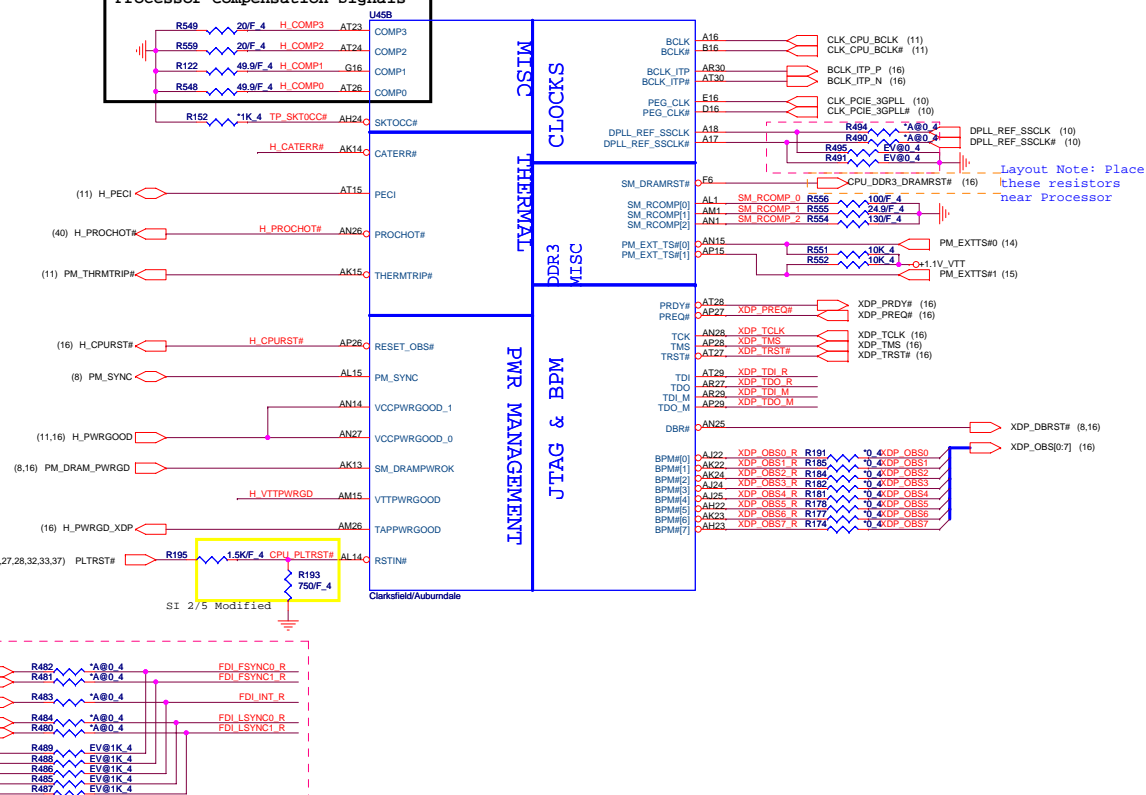
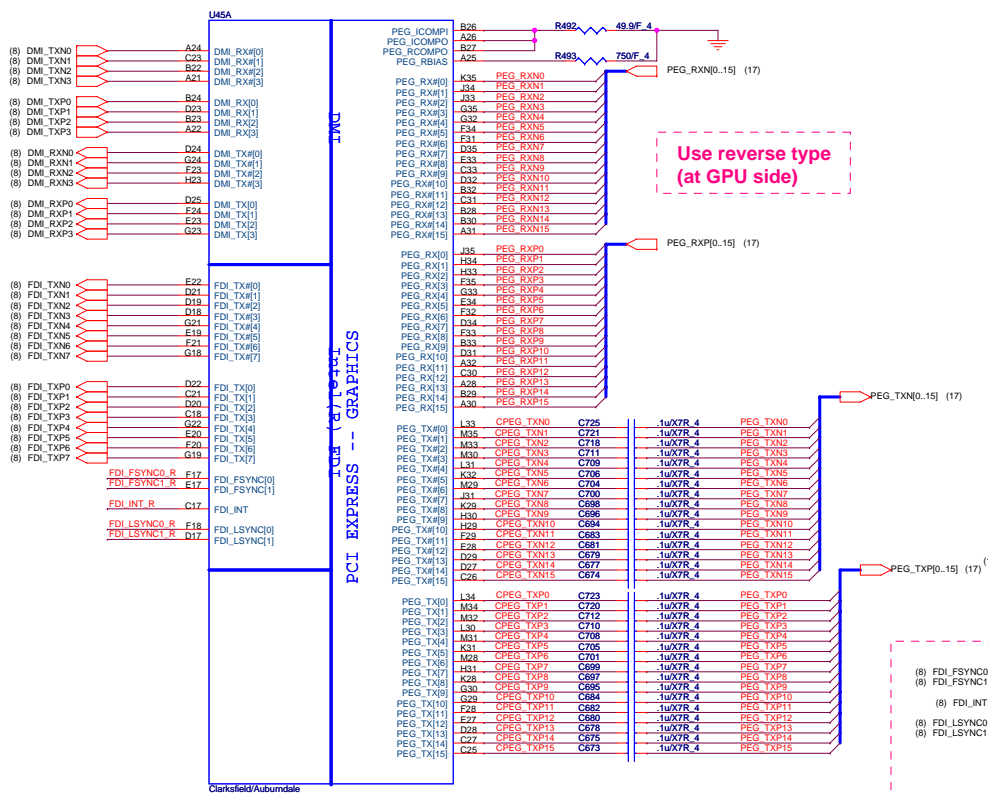
CLK Enable



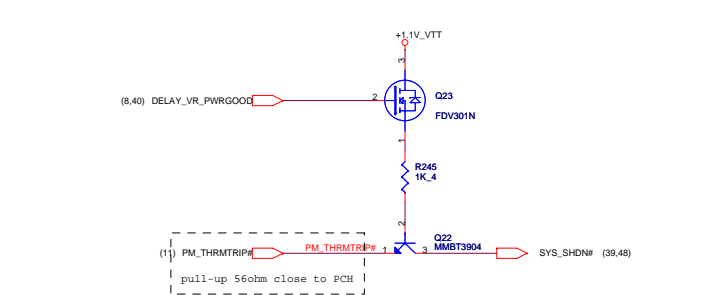


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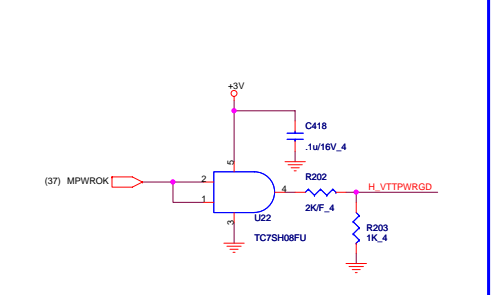
Size	Document Number	Rev
	Clock Generator	1A
Date:	Monday, November 02, 2009	Sheet 3 of 49



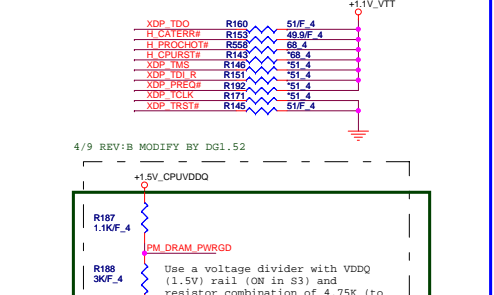
Thermaltrip protect



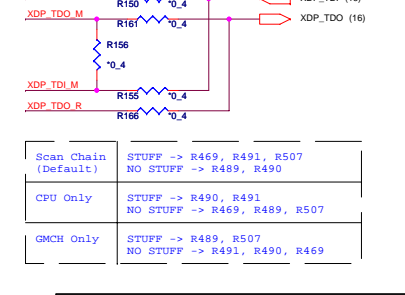
VTT PWR_Good



Processor pull-up



JTAG MAPPING

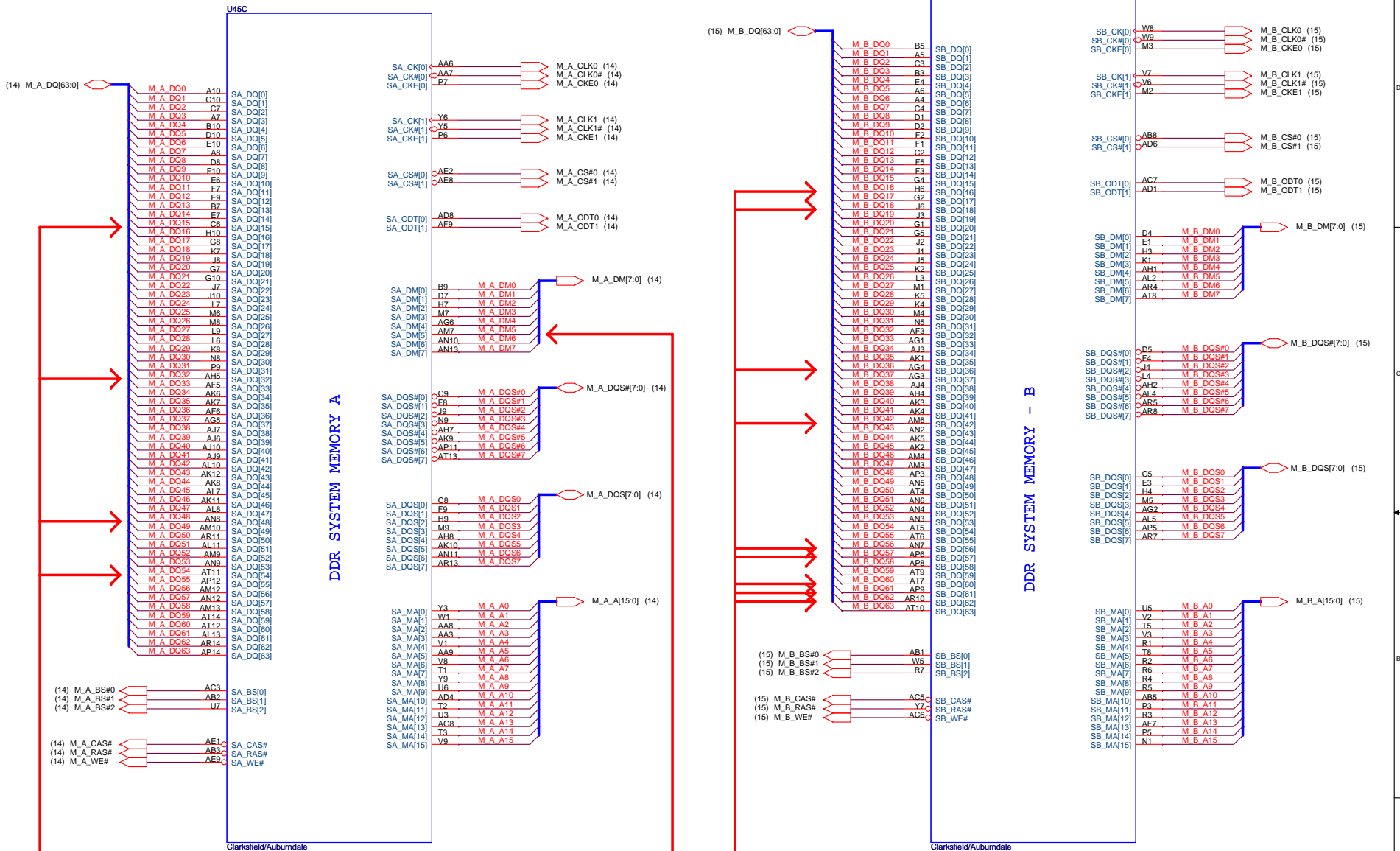


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Size Document Number
AUBURND 1/4 Rev 1A

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AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

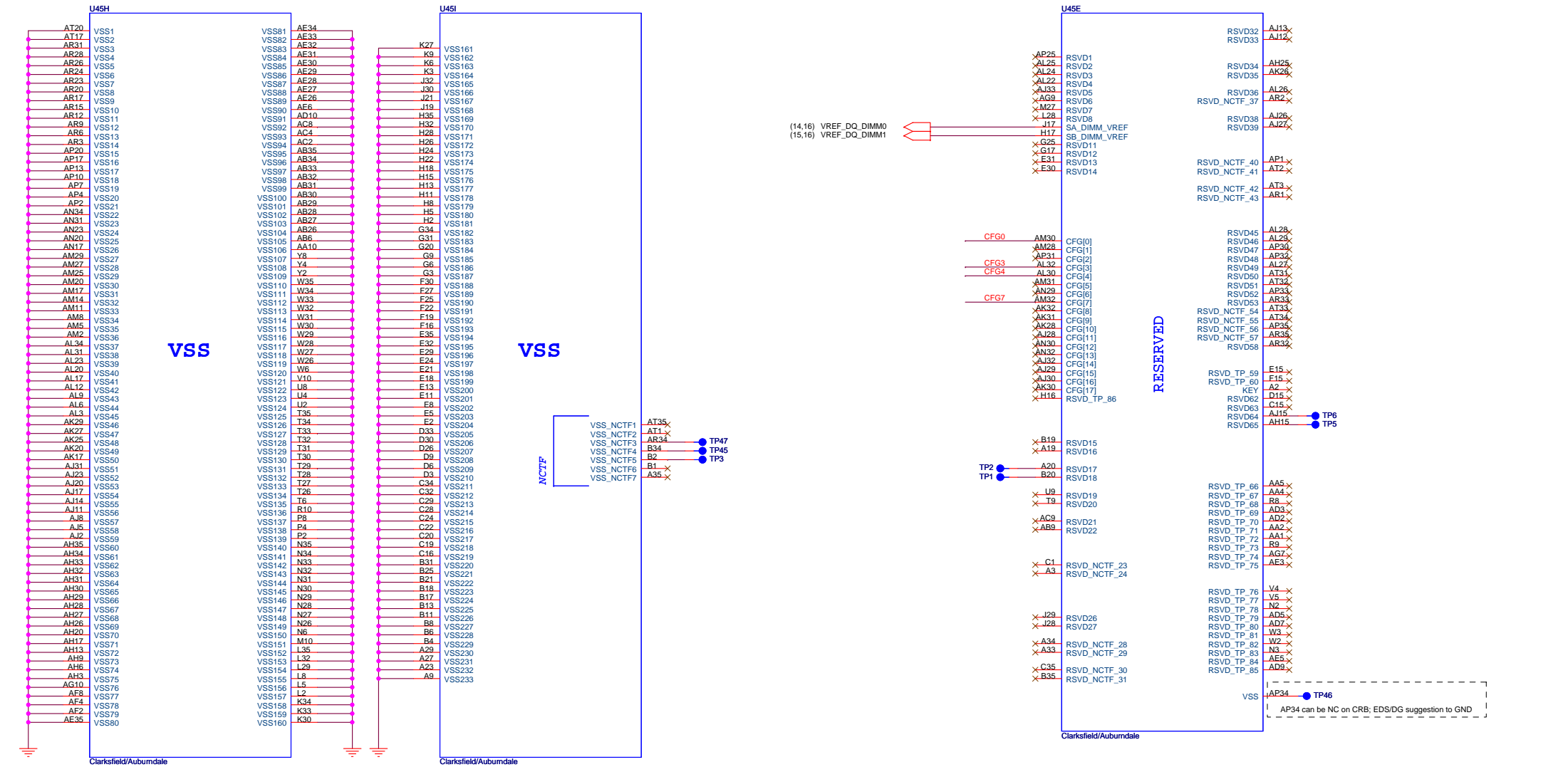


Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

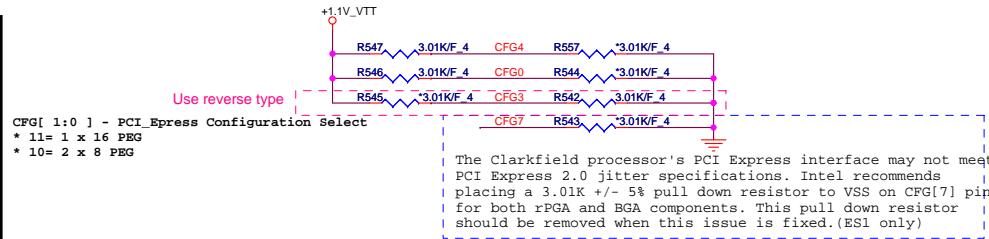
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



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Size Document Number
AUBURND 4/4

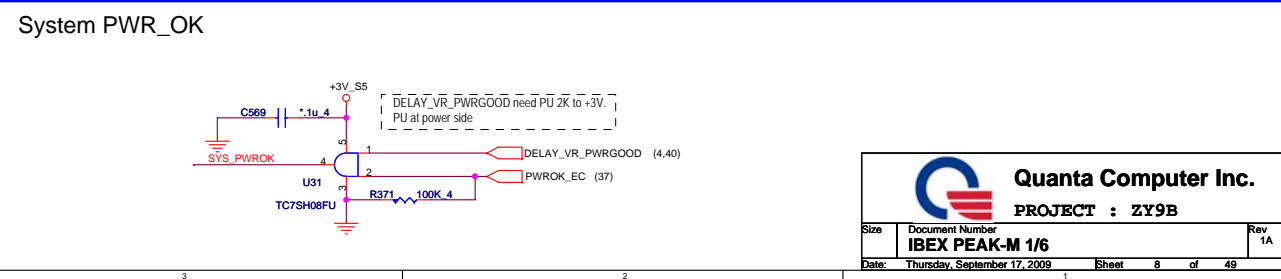
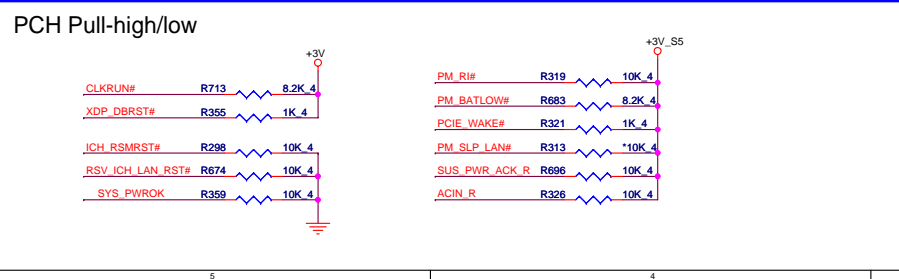
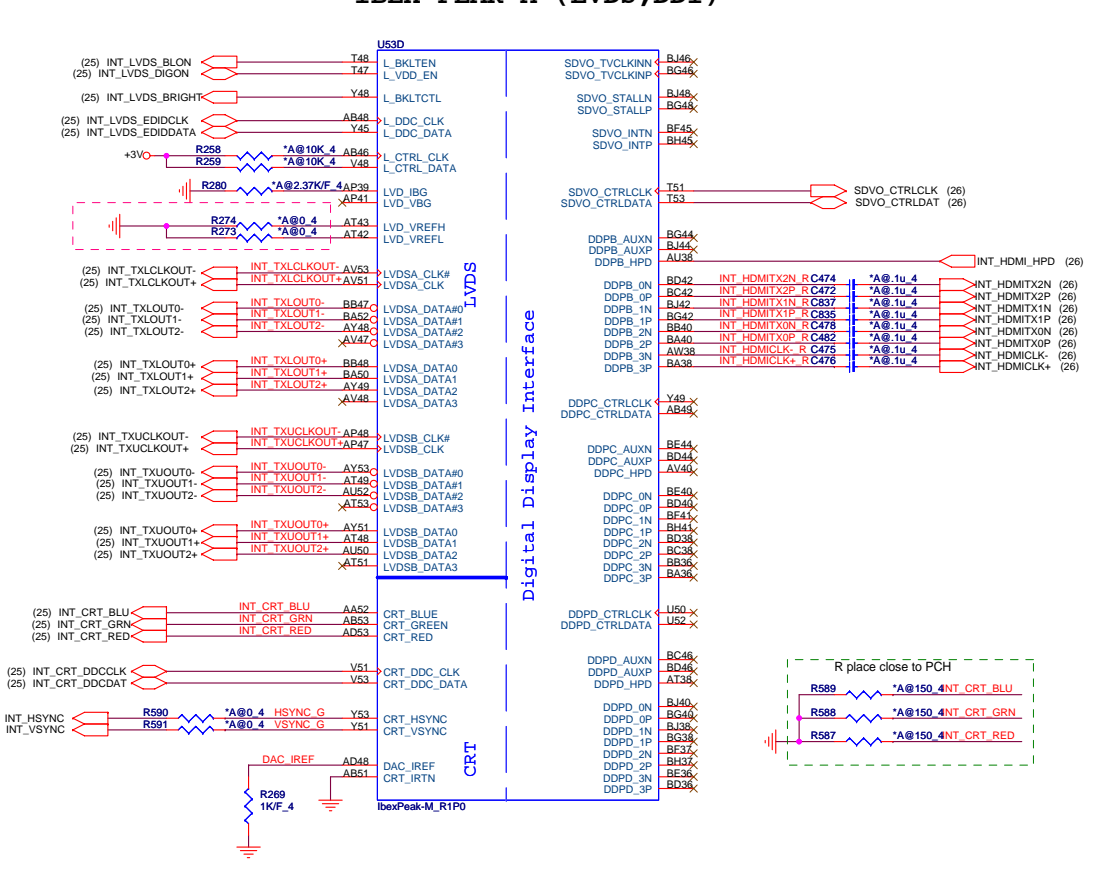
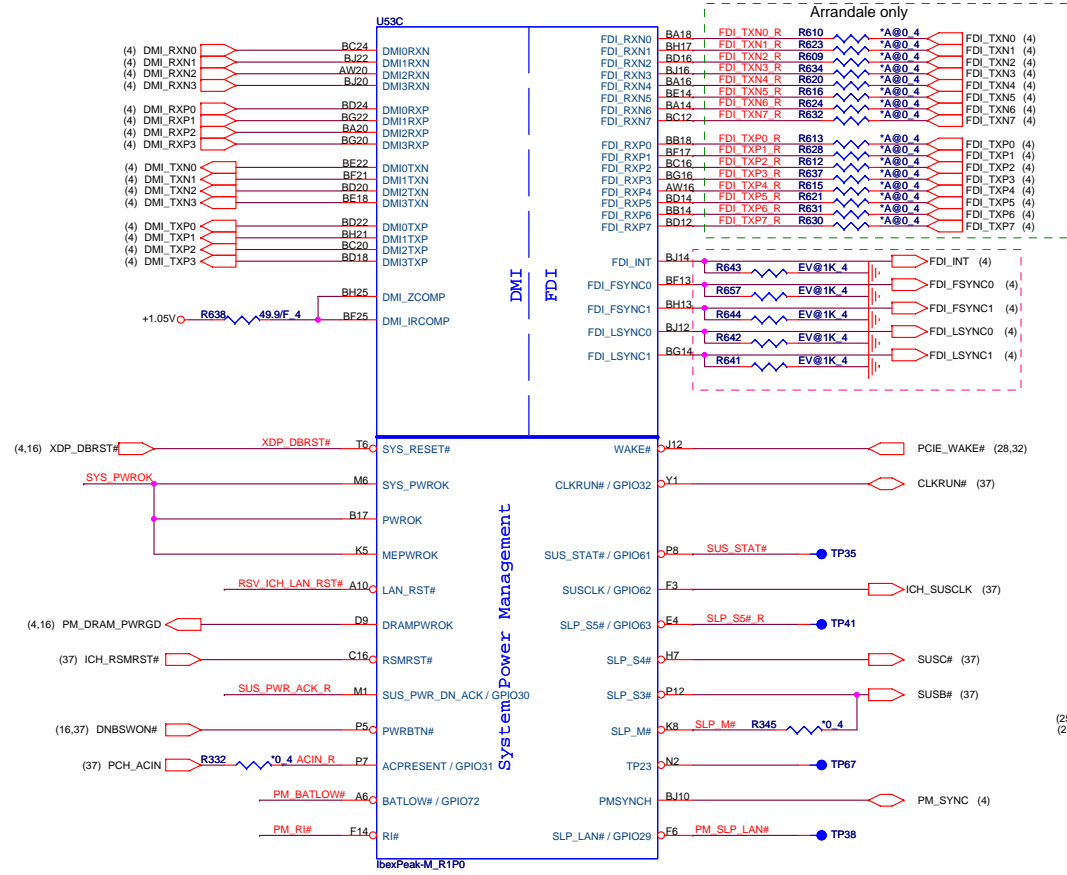
Date: Thursday, September 17, 2009 Sheet 7 of 49


Rev 1A

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed. (ES1 only)

IBEX PEAK-M (DMI, FDI, GPIO)

IBEX PEAK-M (LVDS, DDI)

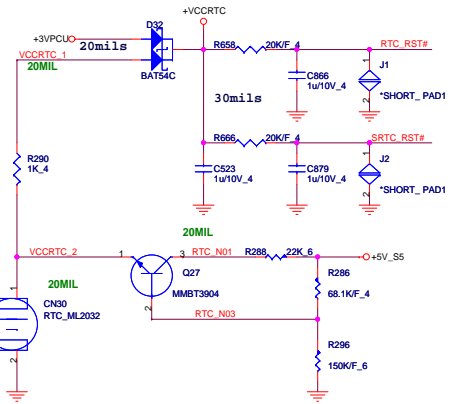




Quanta Computer Inc.
PROJECT : ZY9B

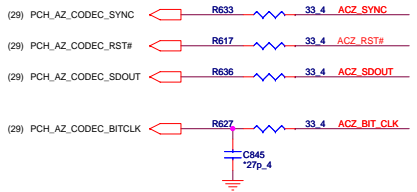
Size	Document Number	Rev	1A
	IBEX PEAK-M 1/6		
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RTC Circuitry



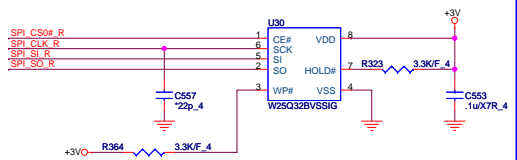
HDA_SYNC (PCH strap pin)
 Internal weak pull-down
 VCCVRM=>1.8V (default)
 external pull-up
 VCCVRM=>1.5V

HDA Bus

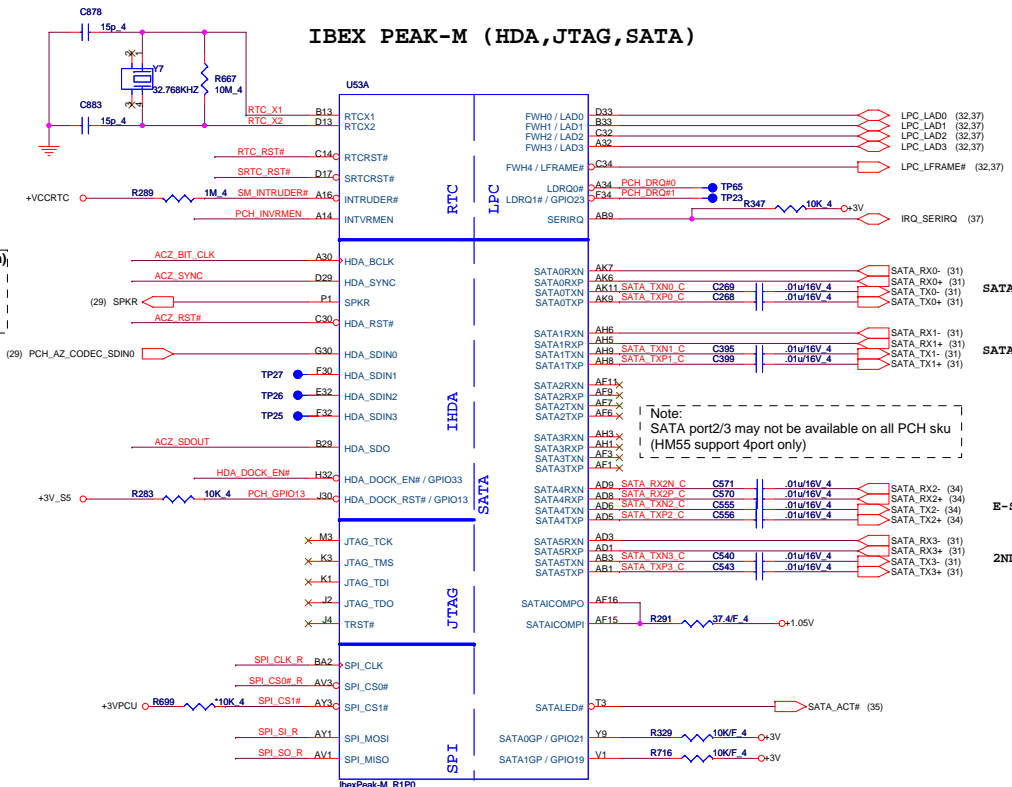


Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI



IBEX PEAK-M (HDA, JTAG, SATA)

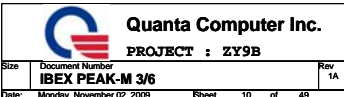
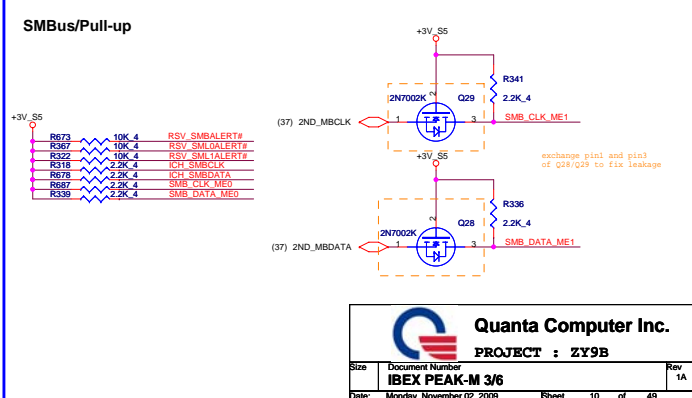
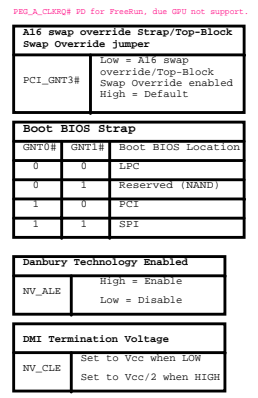
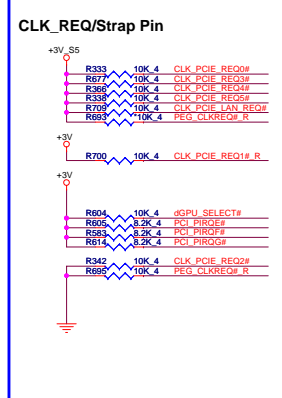
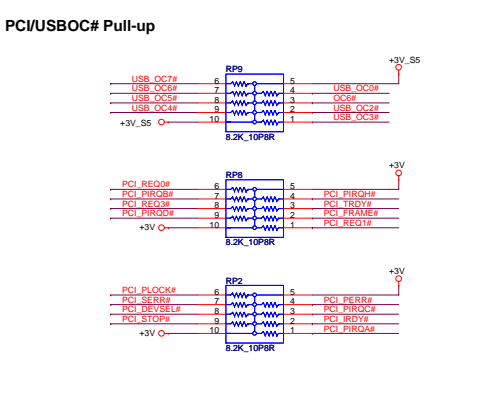
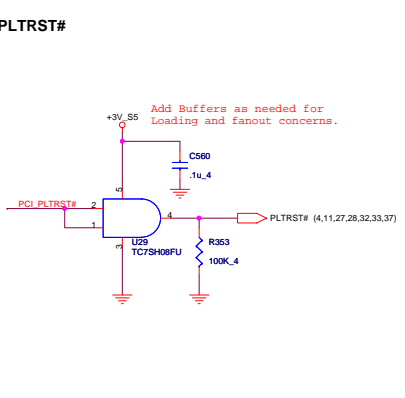
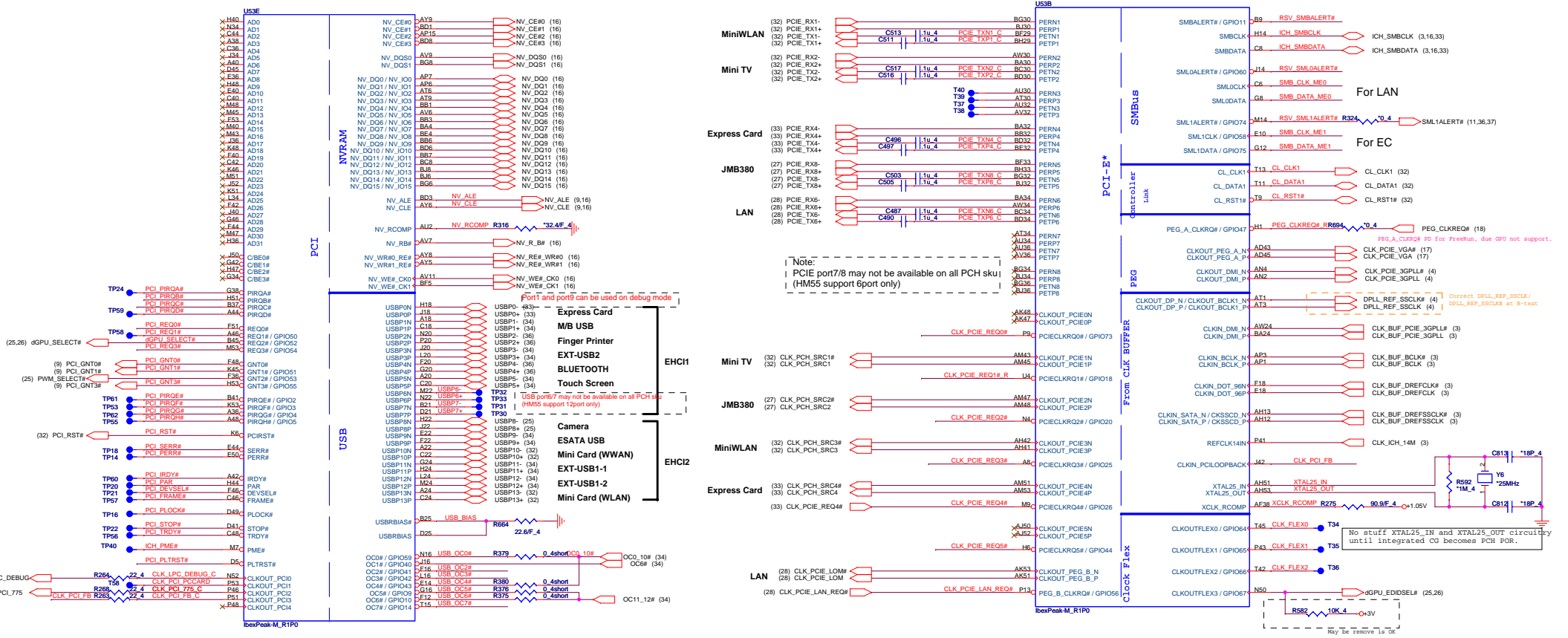


PCH Strap Table

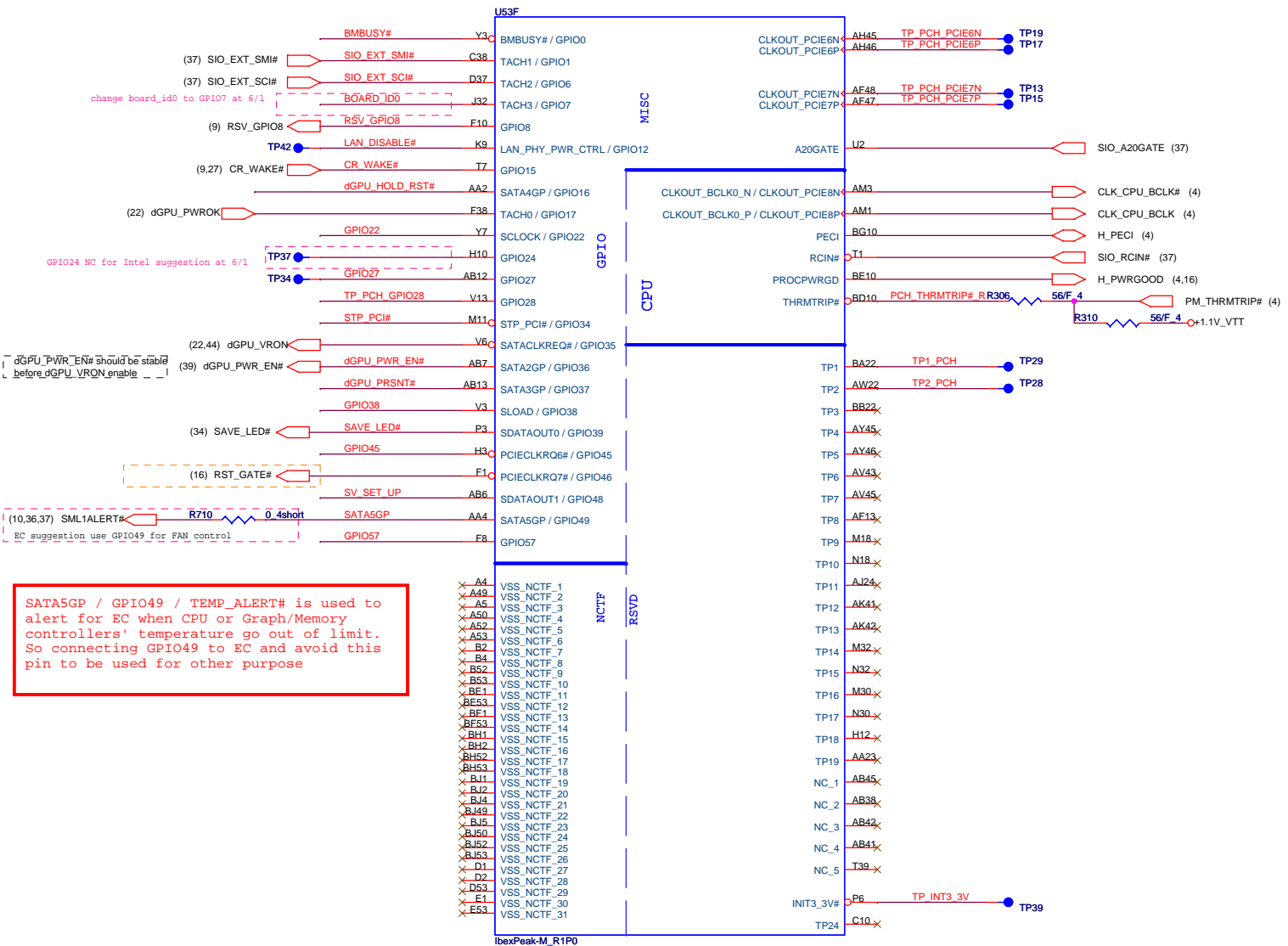
Pin Name	Strap description	Sampled	Configuration	ZY9B note												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V - R702 - 10K - SPKR												
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down													
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R584 - 10K - PCL_GNT3# (10)												
INTRVMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC - R662 - 330K - PCH_INTRVMEN												
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>1</td> <td>SPI</td> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI	1	0	PCI	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] +3V - R270 - 1K - R256 - 1K - PCL_GNT0# (10) +3V - R272 - 1K - R271 - 1K - PCL_GNT1# (10)
GNT1#	GNT0#	Boot Location														
1	1	SPI														
1	0	PCI														
0	0	LPC														
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK														
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN												
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V - R698 - 1K - NV_ALE - NV_ALE (10,16)												
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V - R697 - 1K - NV_CLE - NV_CLE (10,16)												
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V - R279 - 1K - R276 - 10K - HDA_DOCK_EN#												
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V - R352 - 1K - SPI_SI_R												
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)													
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 - R340 - 10K - RV_S_GPIO8 (11)												
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)													
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use default (0 = 1.8V supply)												
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 - R330 - 1K - CR_WAKE# (11,27)												

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

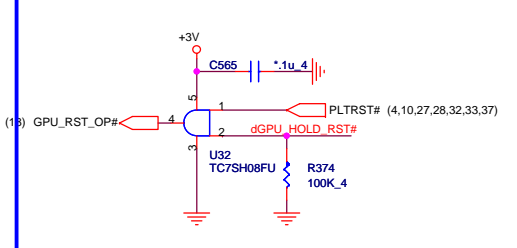


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

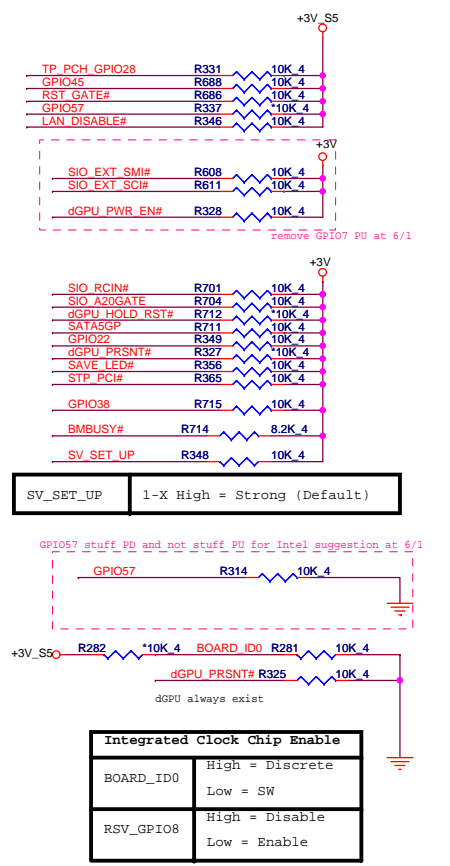


SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU_RST#



GPIO Pull-up/Pull-down



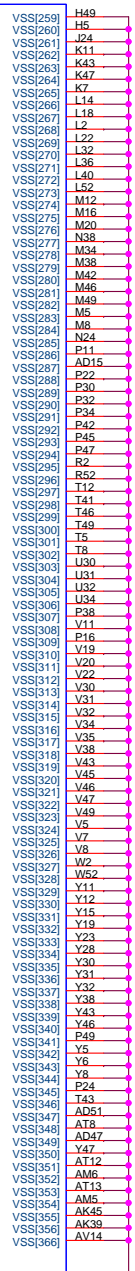
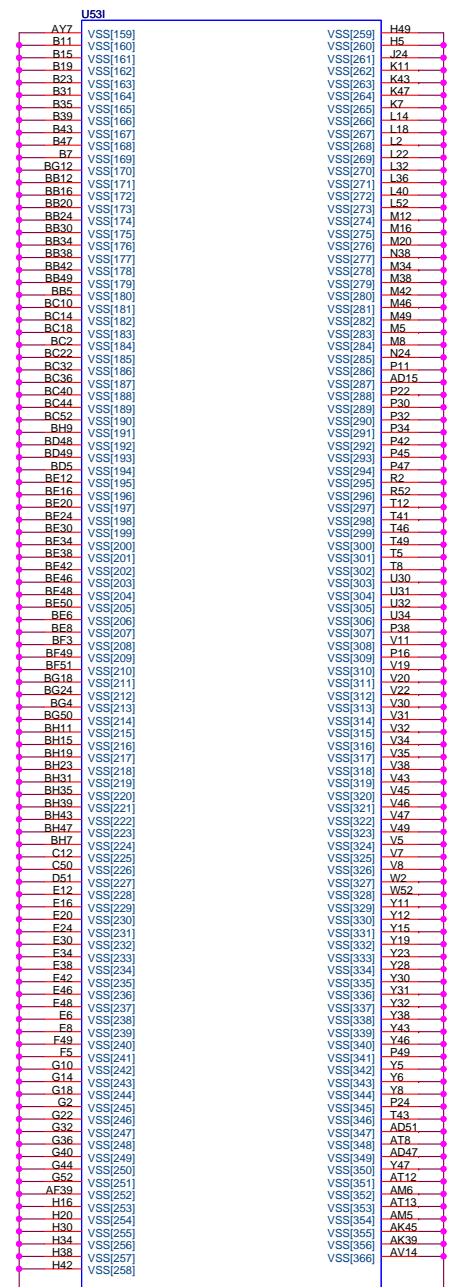
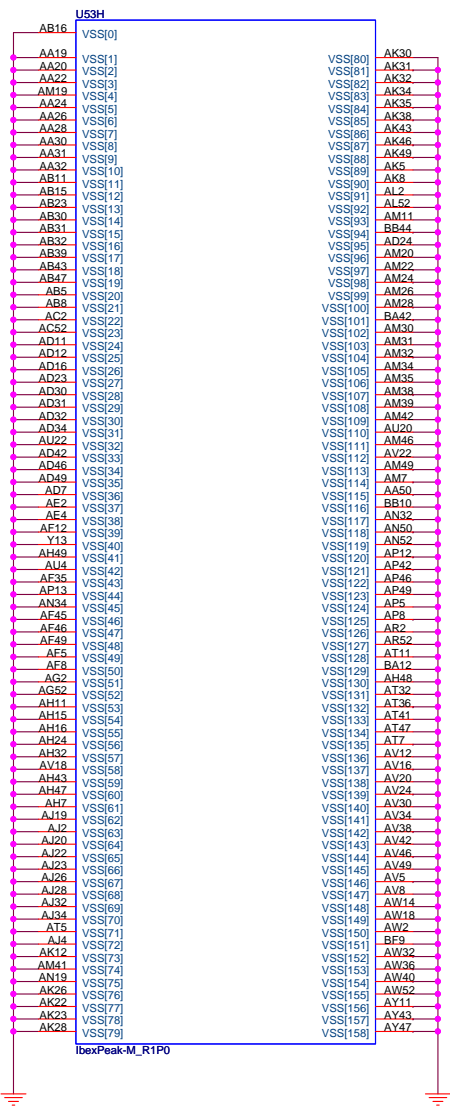
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PROJECT : ZY9B


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Rev 1A

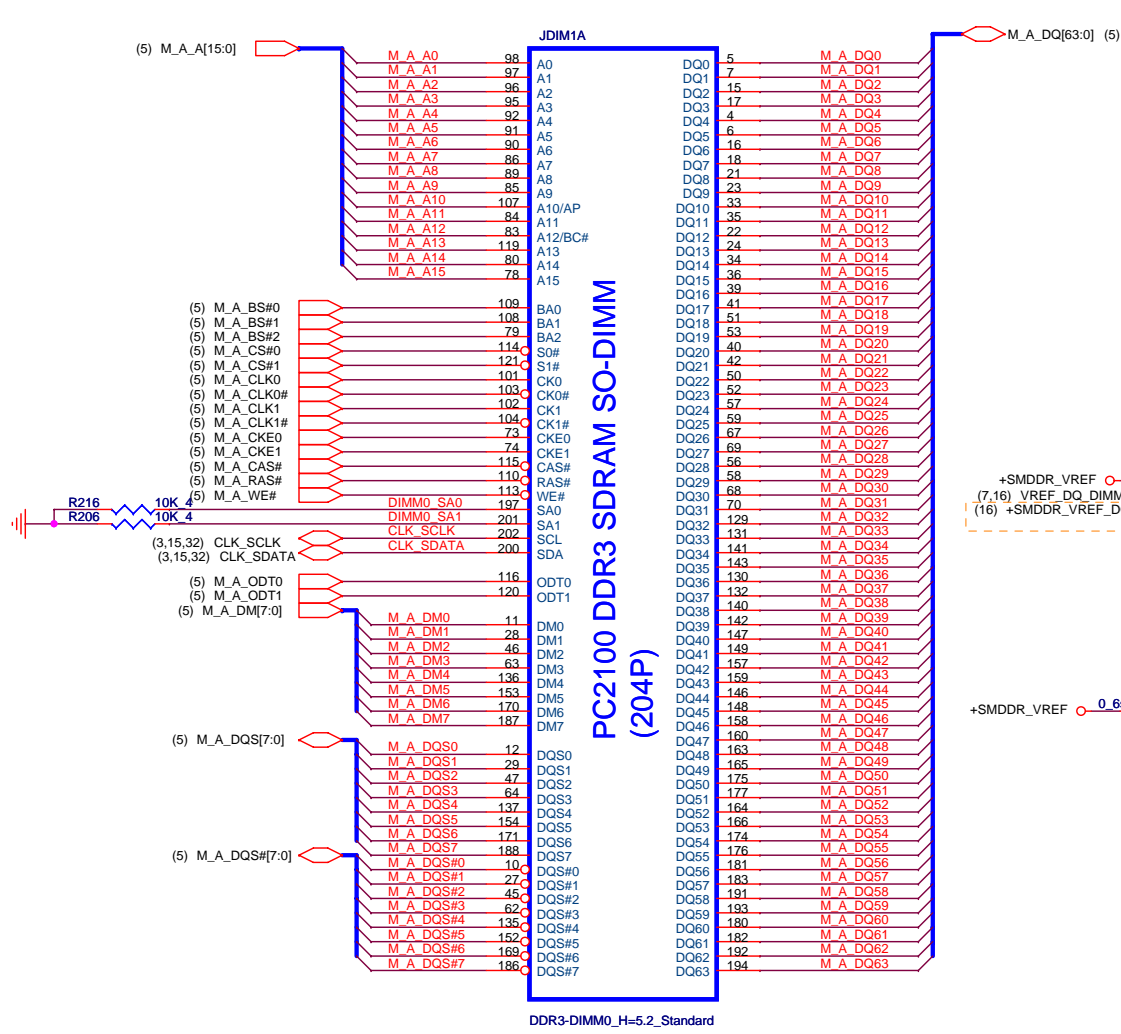
IBEX PEAK-M (GND)



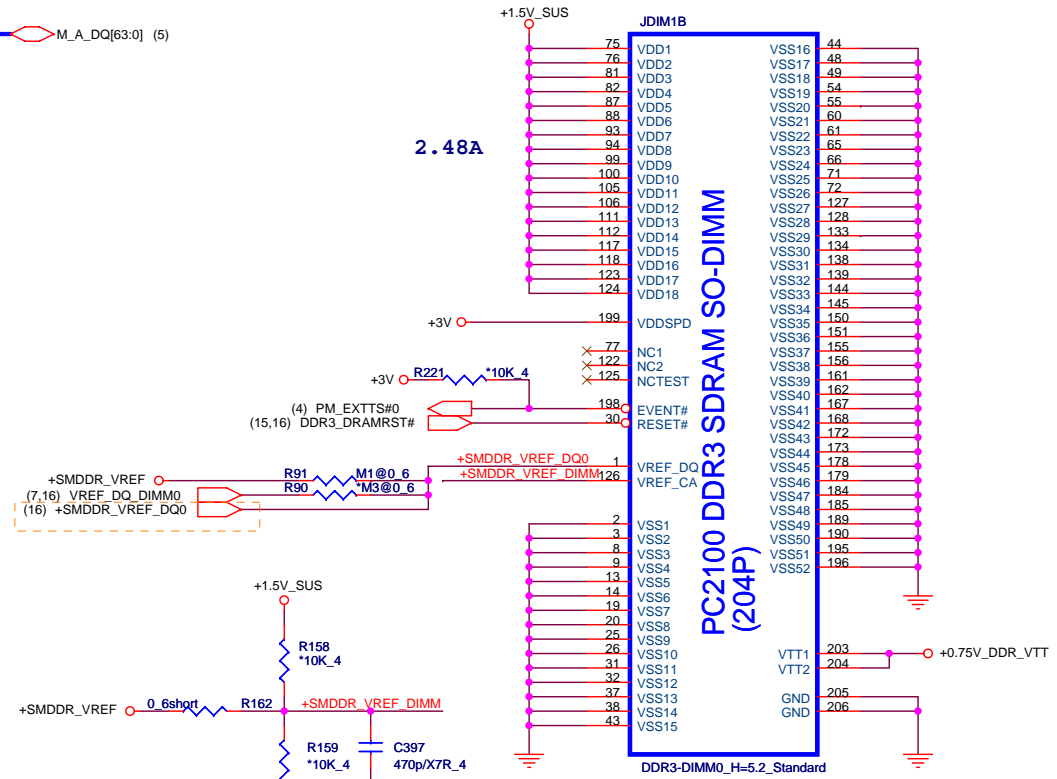


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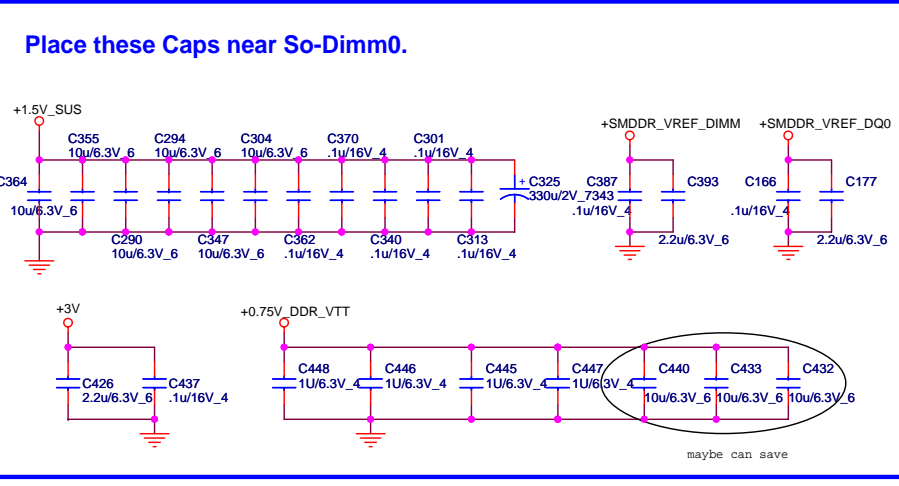
Size	Document Number	Rev
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DDR3-DIMM0_H=5.2_Standard



2.48A



maybe can save

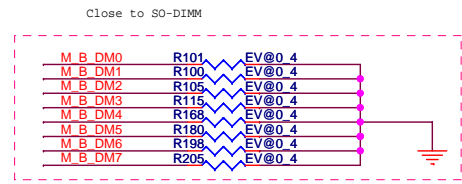
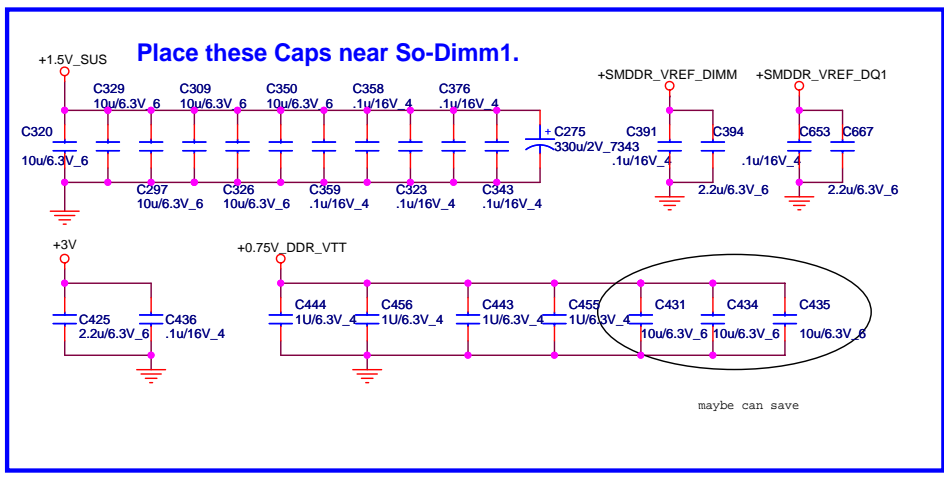
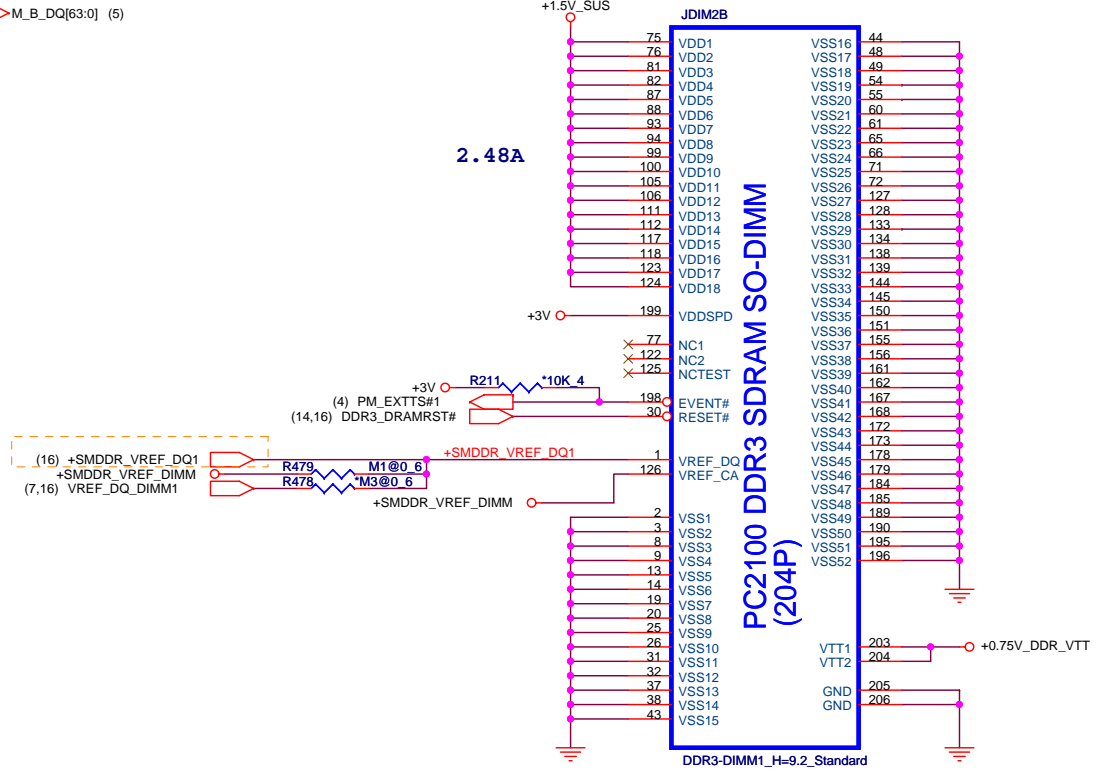
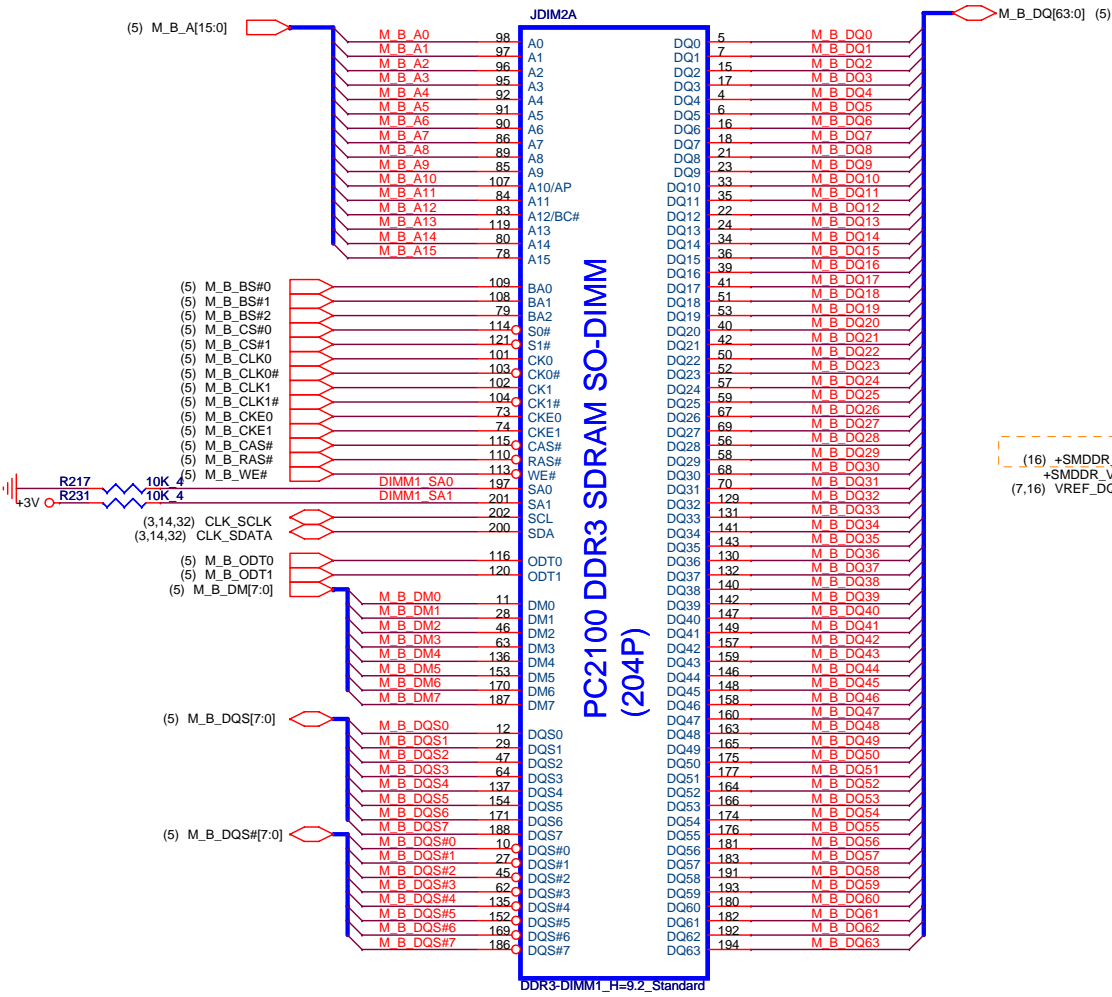


Close to SO-DIMM

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PROJECT : ZY9B

Size: Document Number: **DDR3 SO-DIMM-0** Rev: 1A

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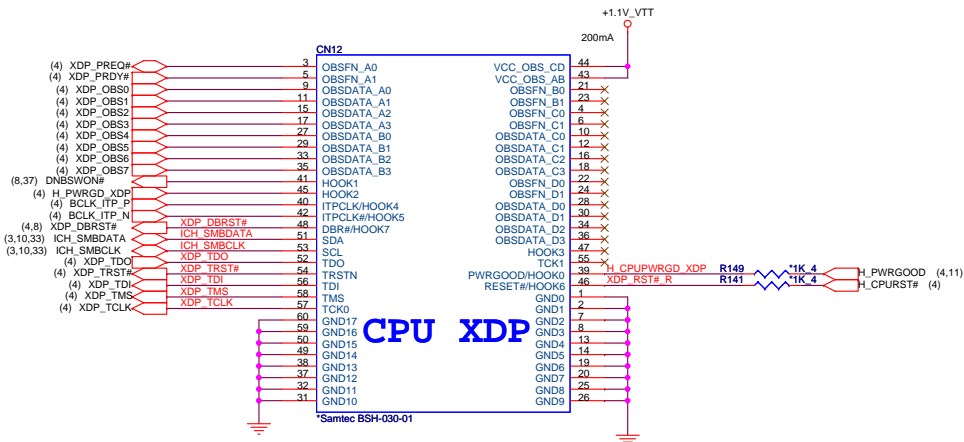


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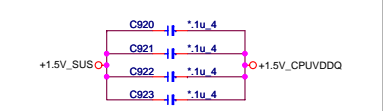
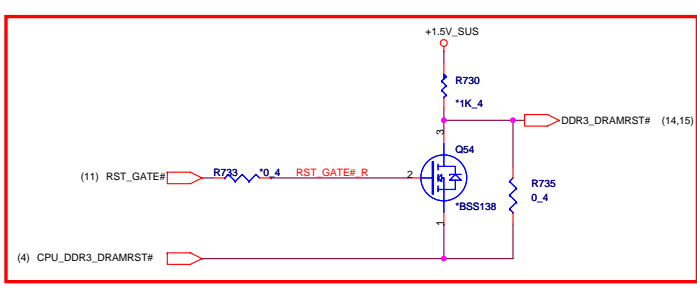
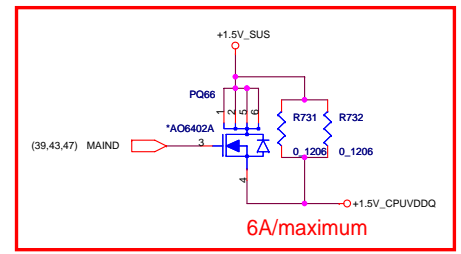
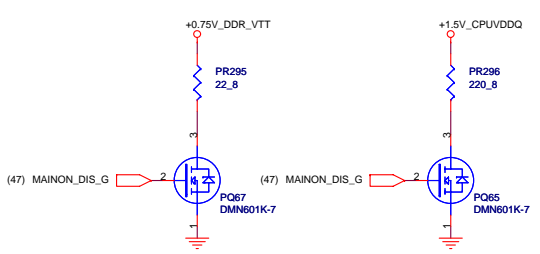
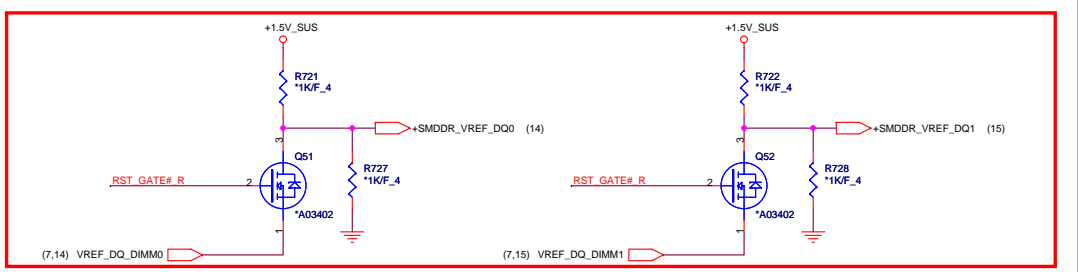
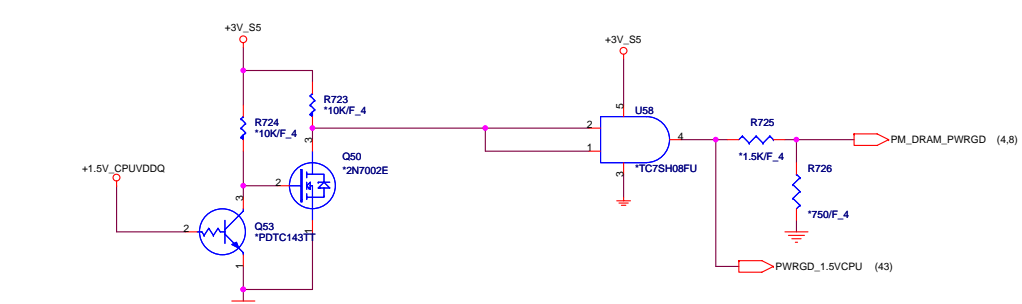
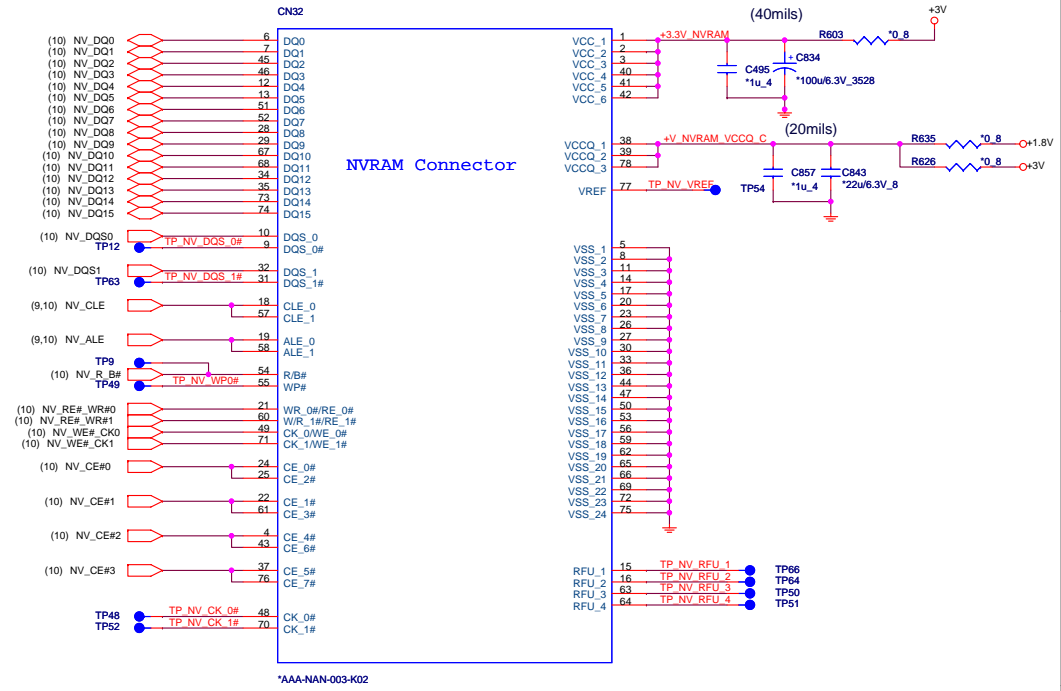
PROJECT : ZY9B

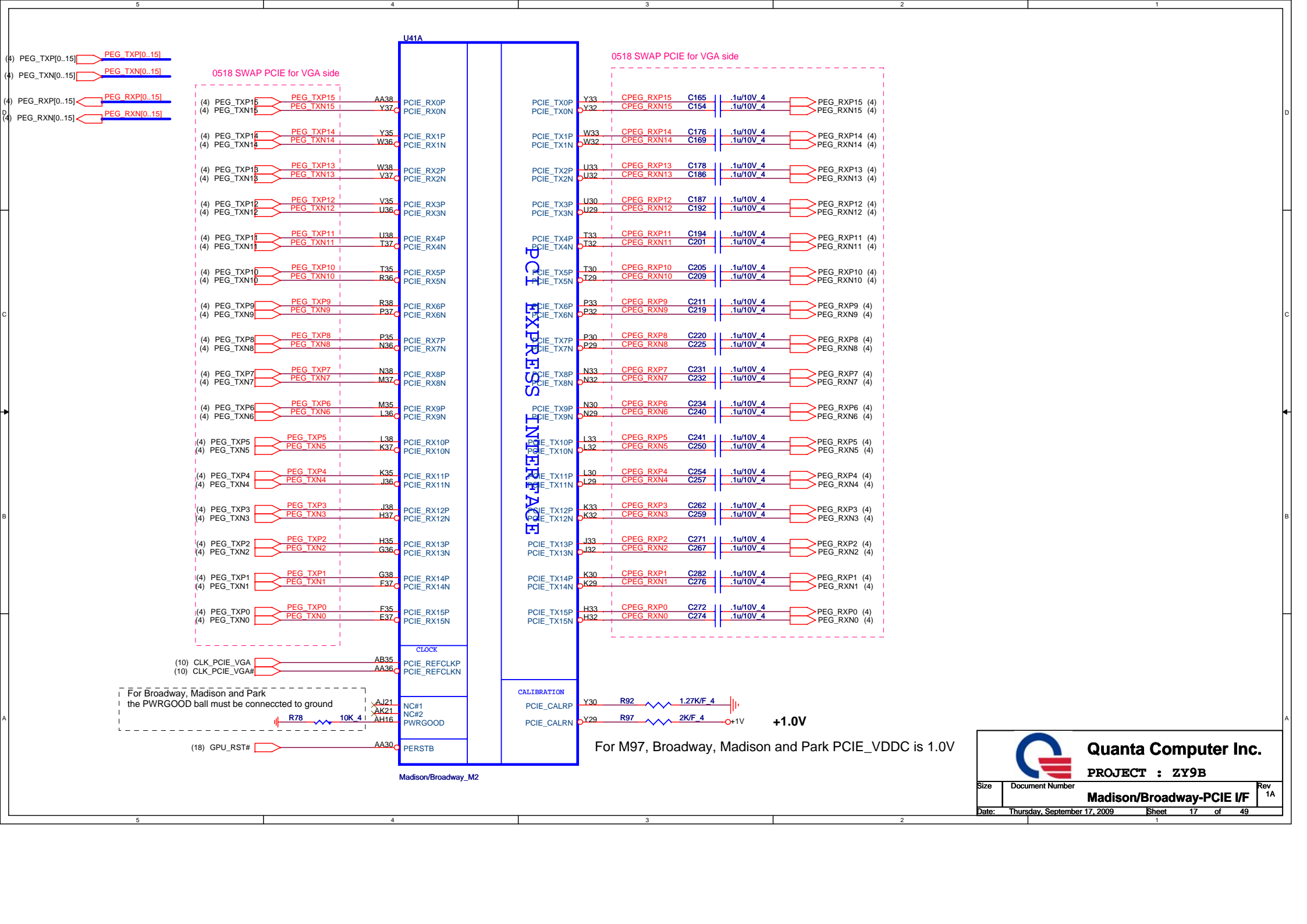
Size	Document Number	Rev
	DDR3 SO-DIMM-1	1A
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CPU XDP Connector



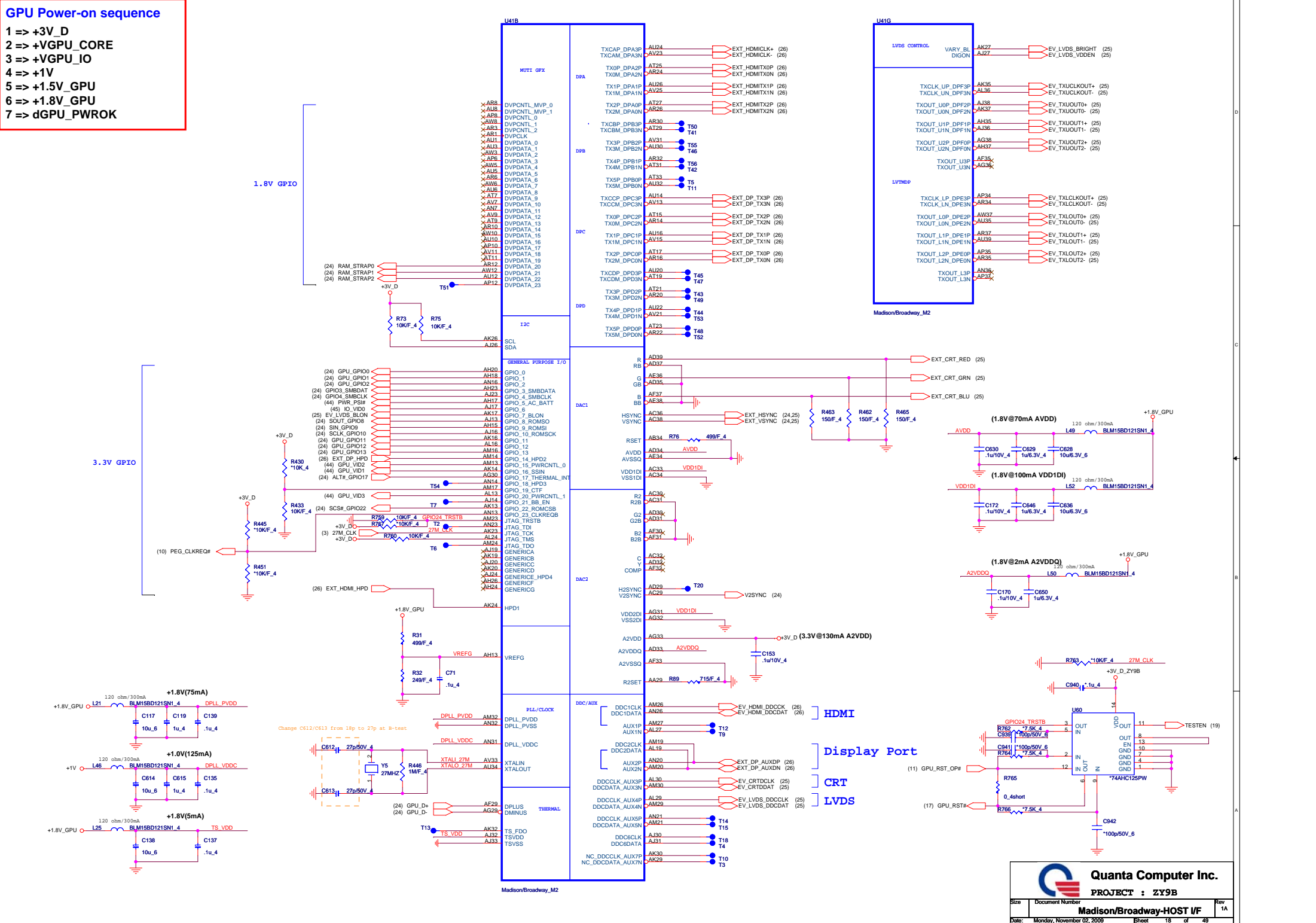
Braidwood





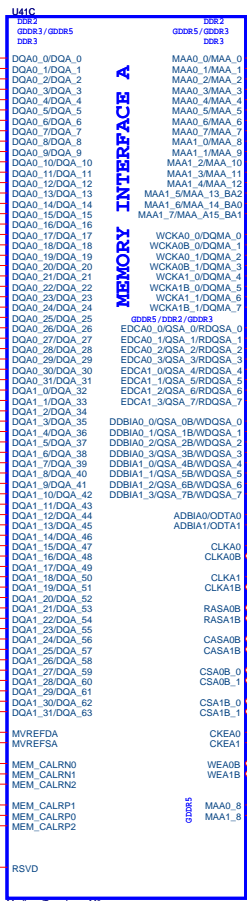
GPU Power-on sequence

- 1 => +3V_D
- 2 => +VGPU_CORE
- 3 => +VGPU_IO
- 4 => +1V
- 5 => +1.5V_GPU
- 6 => +1.8V_GPU
- 7 => dGPU_PWROK



- (20) VMA_DQ[63..0] \leftarrow VMA_DQ[63..0]
- (20) VMA_DM[7..0] \leftarrow VMA_DM[7..0]
- (20) VMA_RDQS[7..0] \leftarrow VMA_RDQS[7..0]
- (20) VMA_WDQS[7..0] \leftarrow VMA_WDQS[7..0]
- (20) VMA_MA[13..0] \leftarrow VMA_MA[13..0]
- (20) VMA_BA0 \leftarrow VMA_BA0
- (20) VMA_BA1 \leftarrow VMA_BA1
- (20) VMA_BA2 \leftarrow VMA_BA2

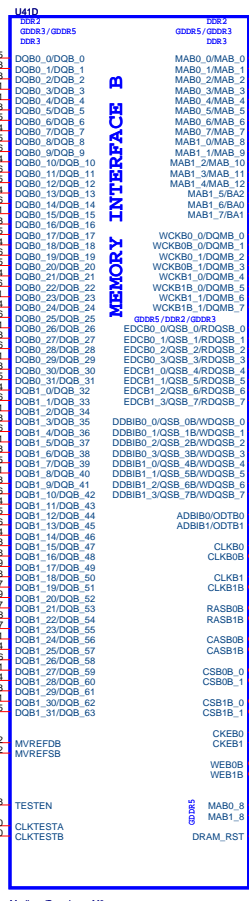
- (21) VMB_DQ[63..0] \leftarrow VMB_DQ[63..0]
- (21) VMB_DM[7..0] \leftarrow VMB_DM[7..0]
- (21) VMB_RDQS[7..0] \leftarrow VMB_RDQS[7..0]
- (21) VMB_WDQS[7..0] \leftarrow VMB_WDQS[7..0]
- (21) VMB_MA[13..0] \leftarrow VMB_MA[13..0]
- (21) VMB_BA0 \leftarrow VMB_BA0
- (21) VMB_BA1 \leftarrow VMB_BA1
- (21) VMB_BA2 \leftarrow VMB_BA2



MEMORY INTERFACE A

QSA[7..0]

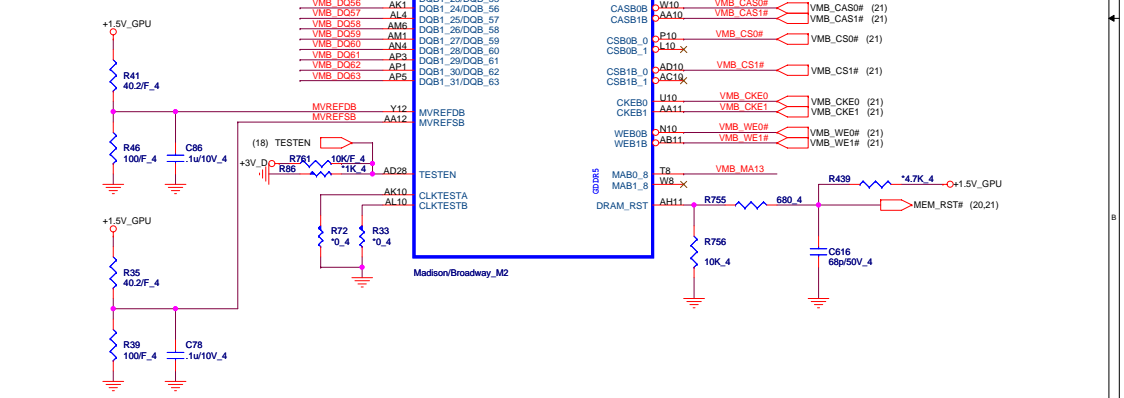
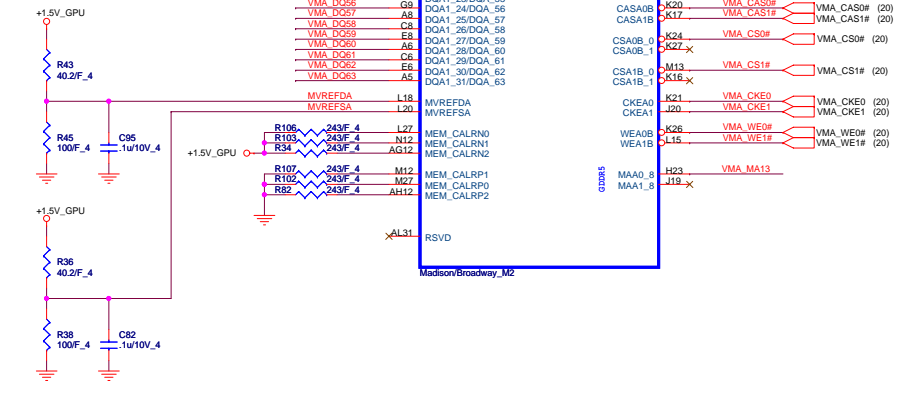
QSA# [7..0]



MEMORY INTERFACE B

QSB[7..0]

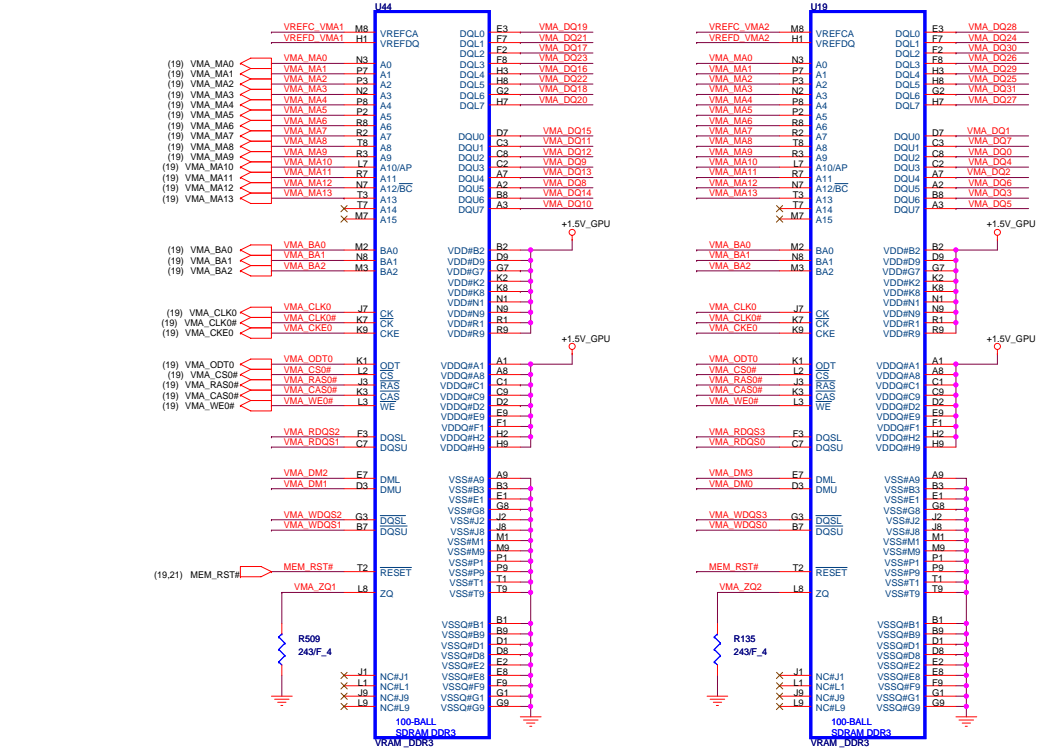
QSB# [7..0]



CHANNEL A: 512MB DDR3 (64M*16*4pcs)

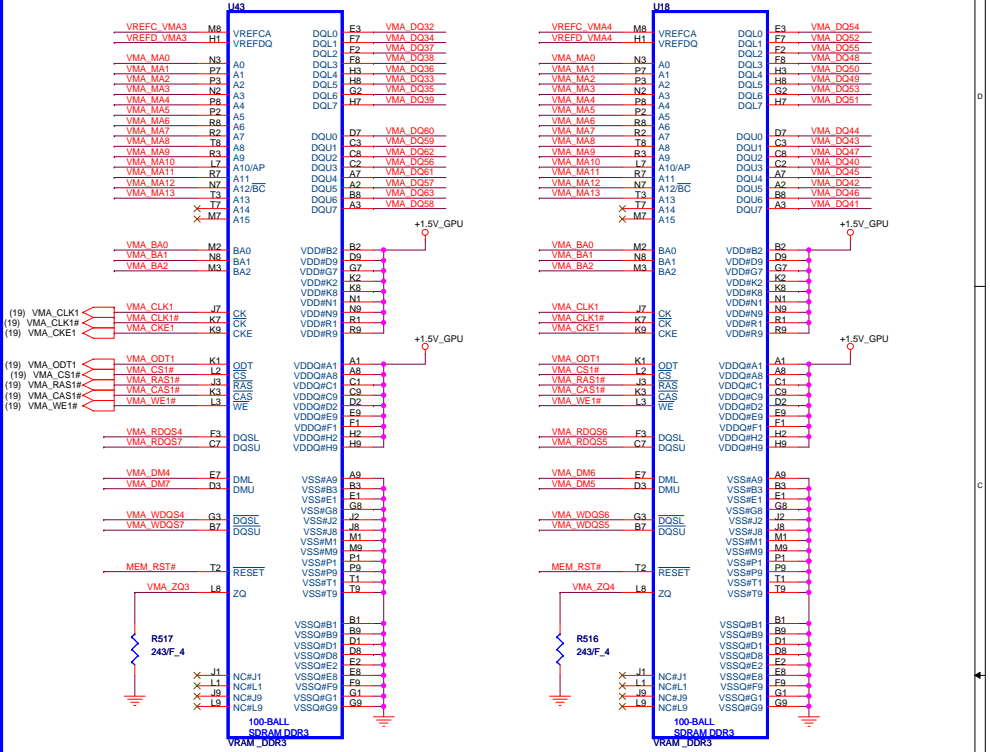
- (19) VMA_DQ[63..0] VMA_DQ[63..0]
- (19) VMA_DM[7..0] VMA_DM[7..0]
- (19) VMA_RDQS[7..0] VMA_RDQS[7..0]
- (19) VMA_WDQS[7..0] VMA_WDQS[7..0]

QSA[7..0]
QSA#[7..0]



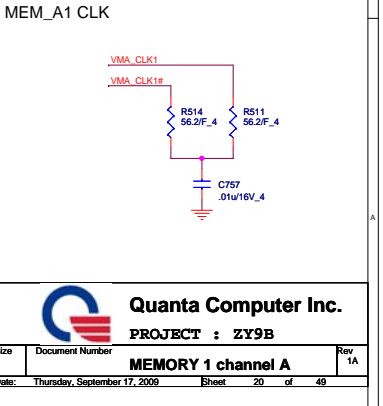
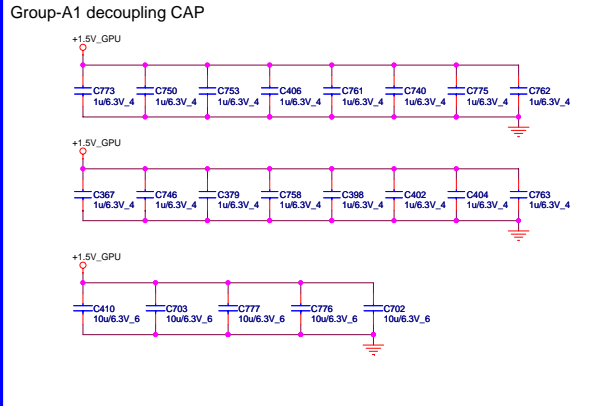
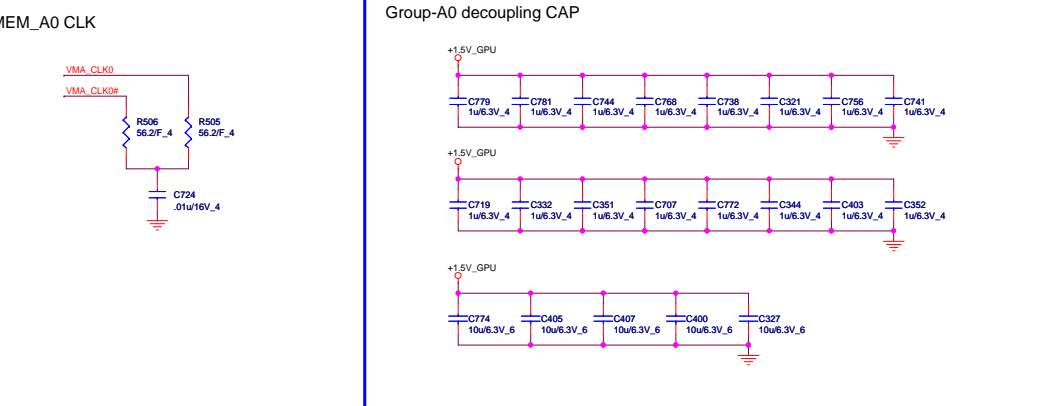
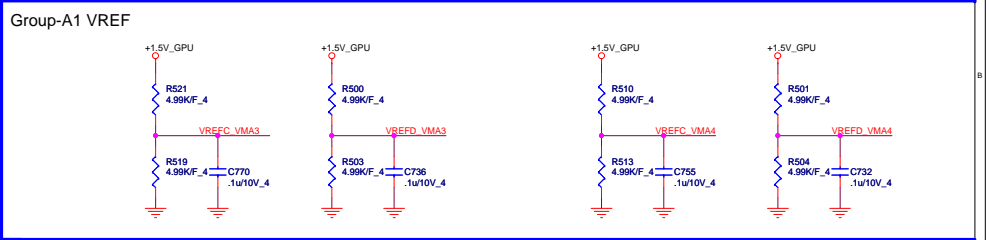
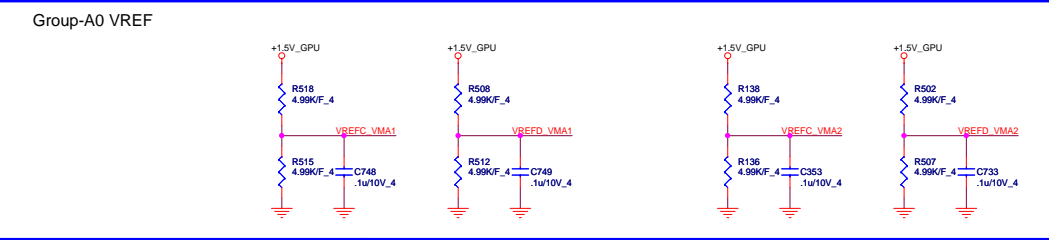
TOP Left

BOT Left



BOT Right

TOP Right

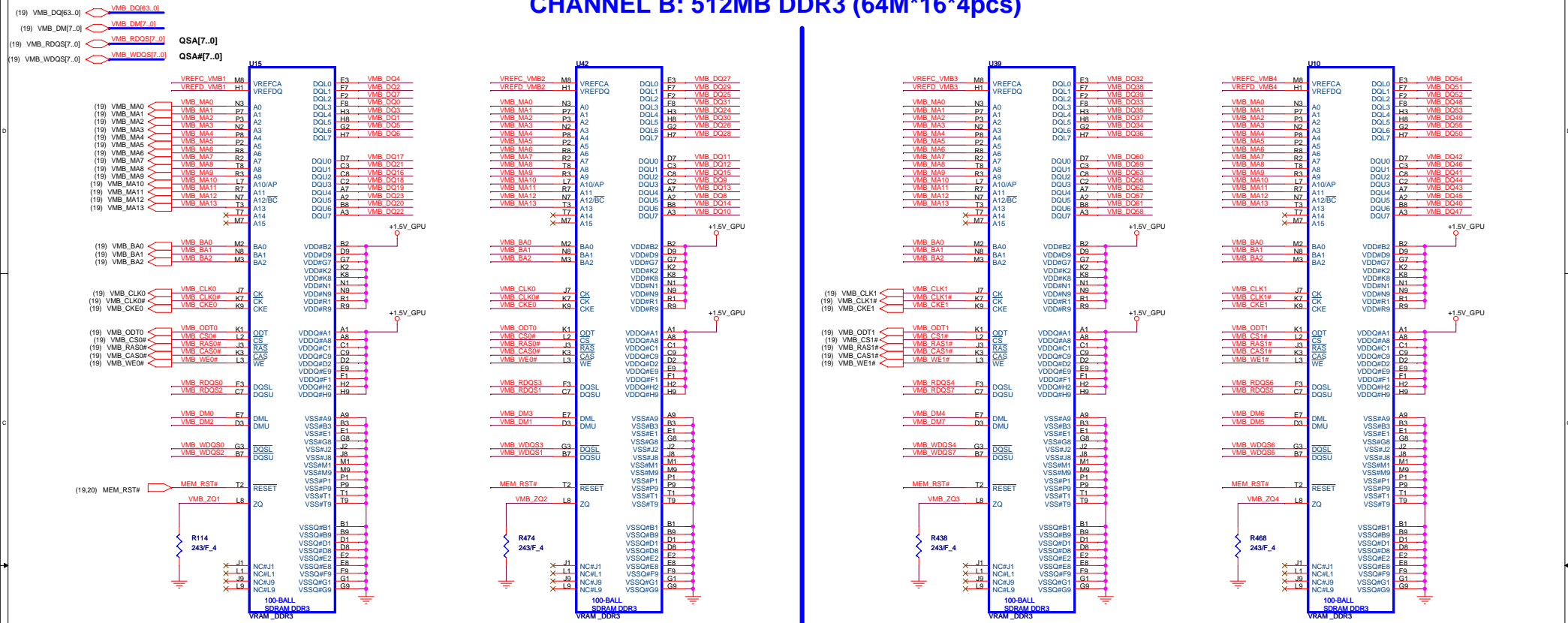


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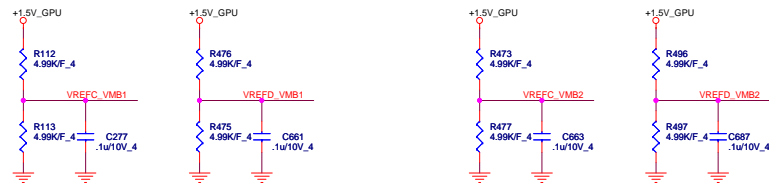
PROJECT : ZY9B

Size	Document Number	MEMORY 1 channel A	Rev 1A
Date: Thursday, September 17, 2009		Sheet 20 of 49	

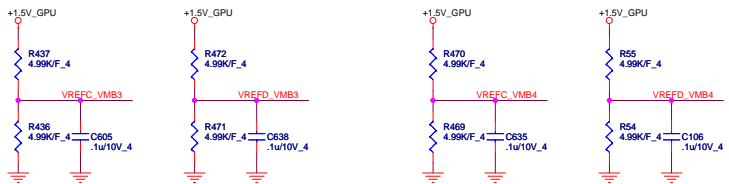
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



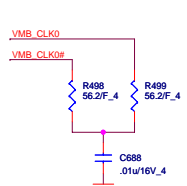
Group-B0 VREF



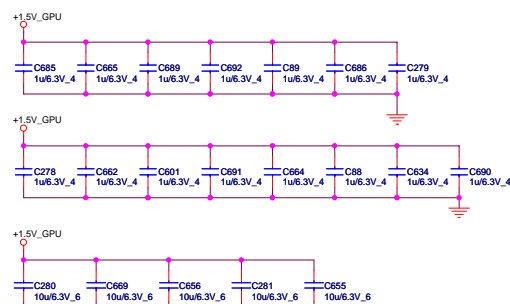
Group-B1 VREF



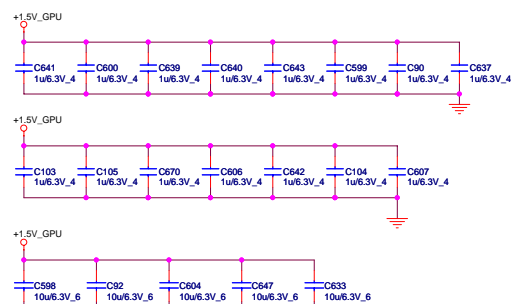
MEM_B0 CLK



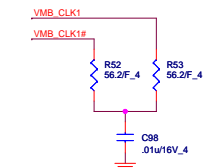
Group-B0 decoupling CAP



Group-B1 decoupling CAP

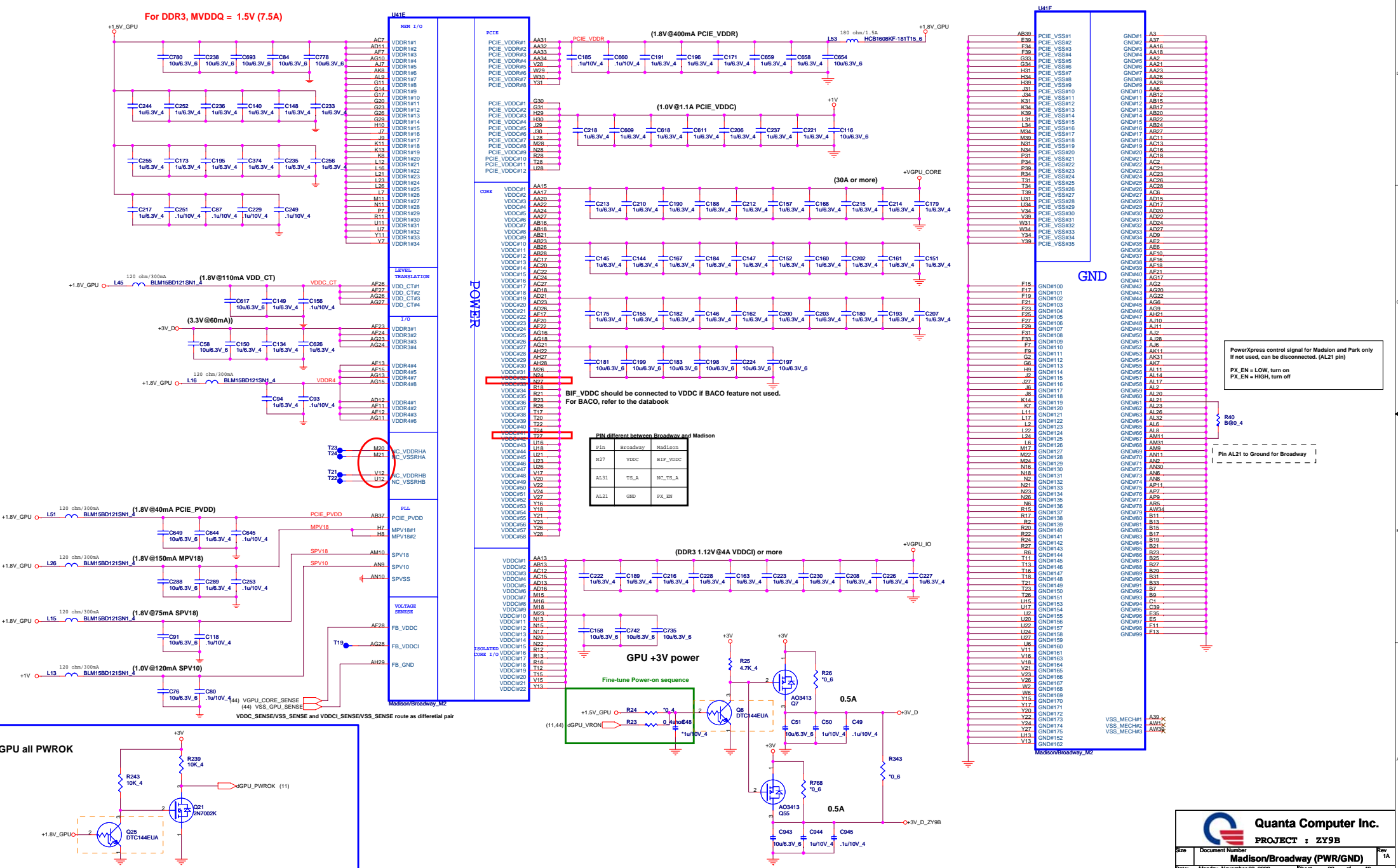


MEM_B1 CLK



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PROJECT : ZY9B
MEMORY 2 channel B
 Date: Thursday, September 17, 2009 Sheet 21 of 49

For DDR3, MVDDQ = 1.5V (7.5A)



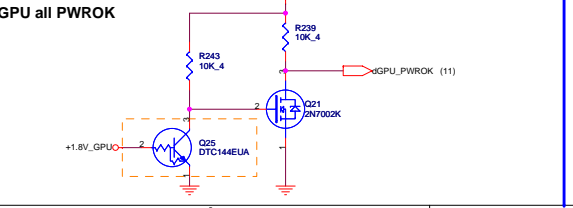
BIF_VDDC should be connected to VDDC if BACO feature not used. For BACO, refer to the databook

Pin different between Broadway and Madison

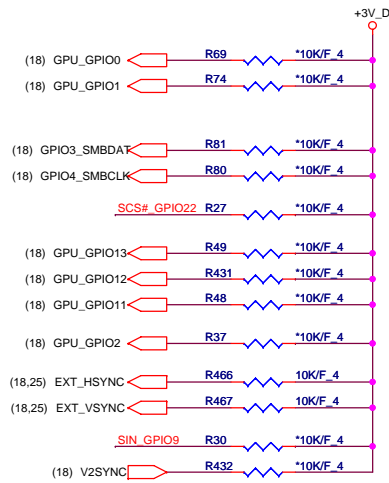
Pin	Broadway	Madison
N27	VDDC	BIF_VDDC
AL31	TS_A	NC_TS_A
AL21	GND	PX_EN

PowerPlex control signal for Madison and Park only. If not used, can be disconnected. (AL21 pin) PX_EN = LOW, turn on PX_EN = HIGH, turn off

Pin AL21 to Ground for Broadway



PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

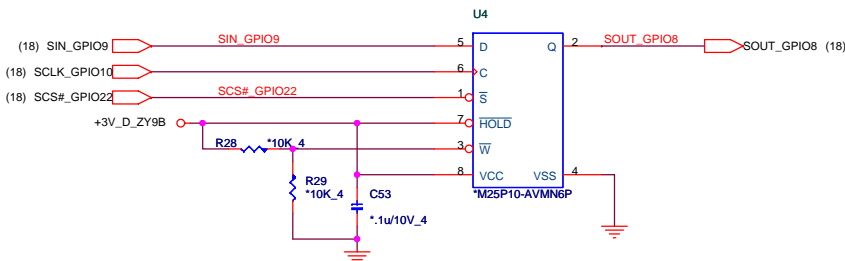
Audio Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM

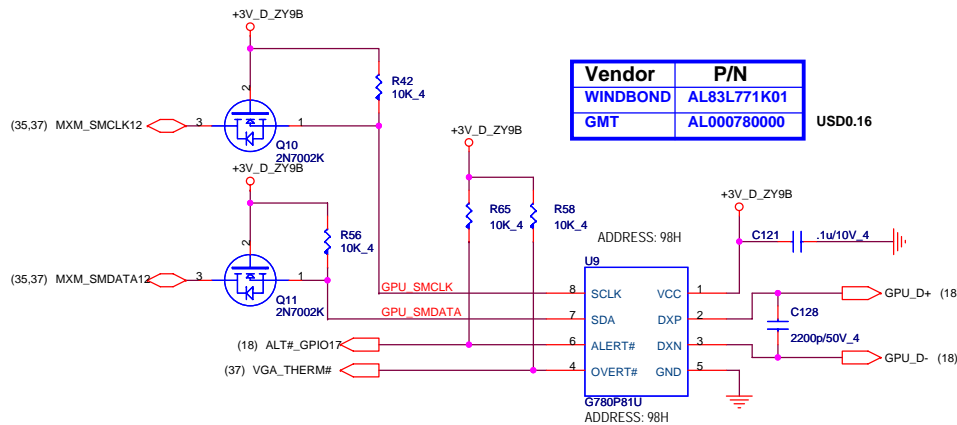


DDR3 VRAM SIZE Strap

DDR3 VRAM size

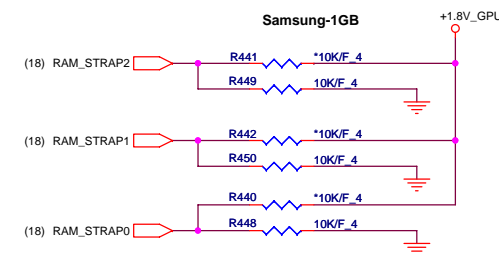
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB			
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	512MB	0	1	0
			1GB	0	0	0
			2GB	0	0	1

Thermal Sensor



Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16



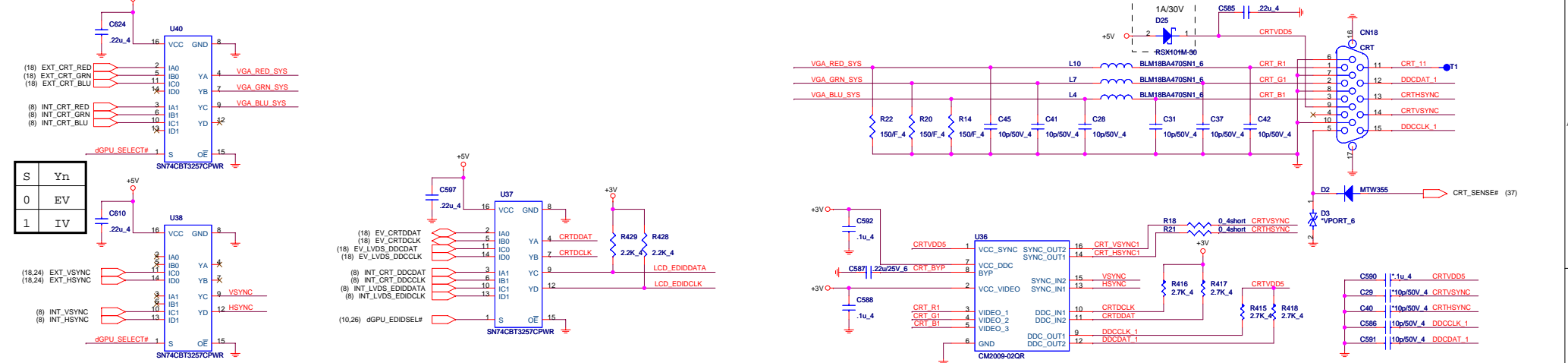
RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

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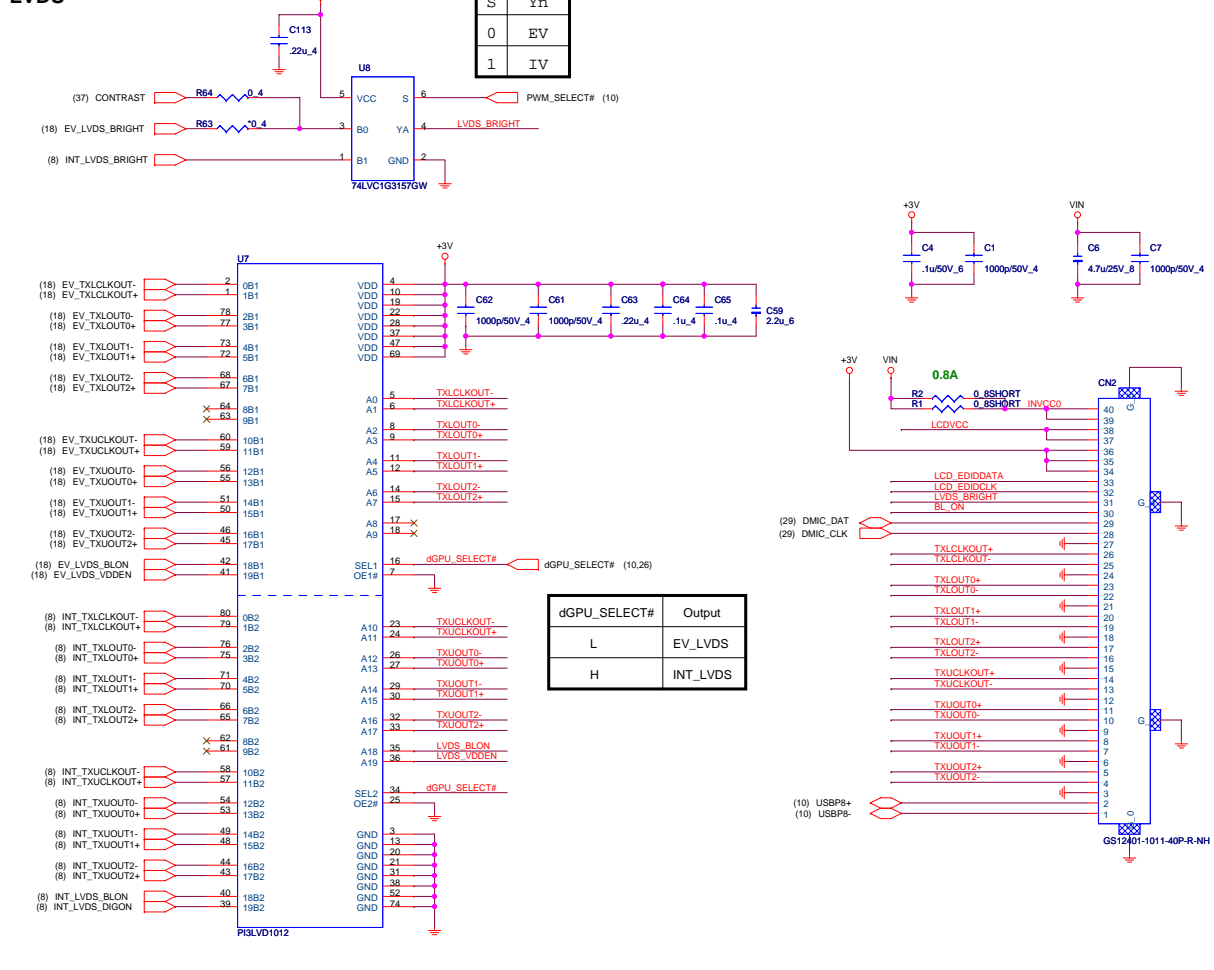
Size	Document Number	Rev
	Strip/Thermal	1A

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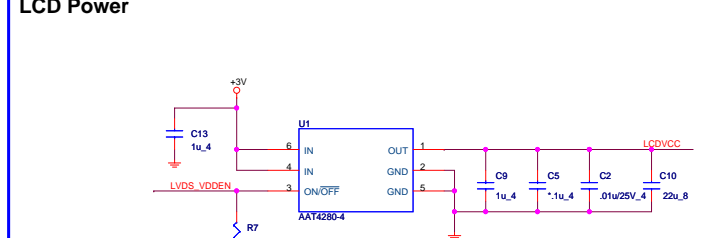
CRT



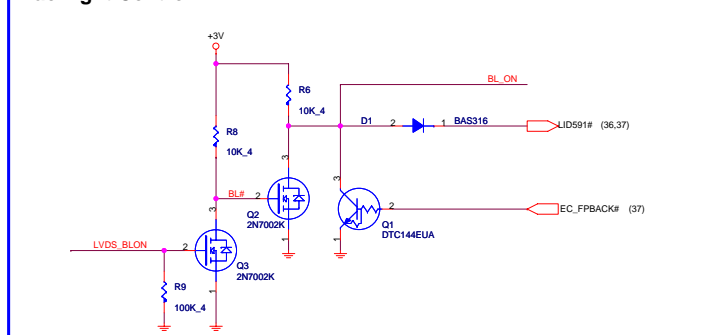
LVDS



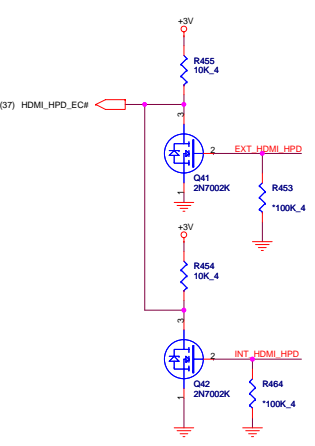
LCD Power



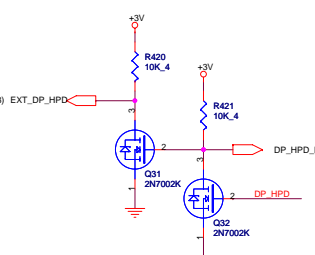
Backlight Control



HDMI Hot-PLUG to EC and GPU



DP Hot-PLUG to EC and GPU



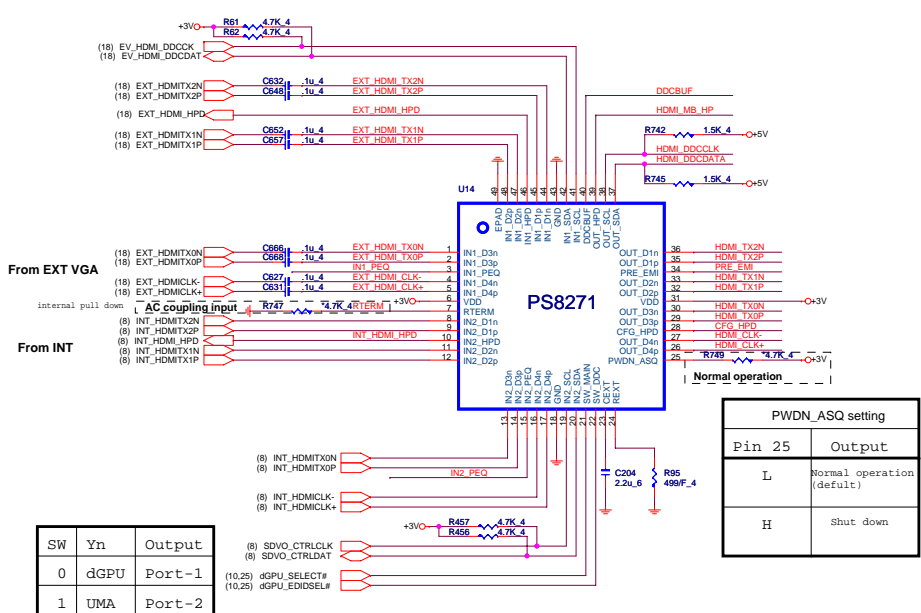
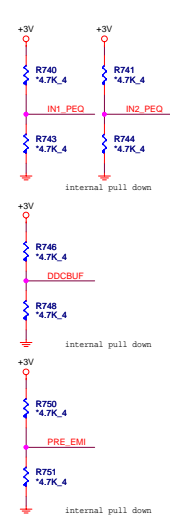
HDMI

Input EQ setting	
INn_PEQ	Output
L	Middle EQ
H	High EQ
M	Low EQ

DDC Buffer setting	
DDC_BUF	Output
L	Passive DDC
H	Active Set-1
M	Active Set-2

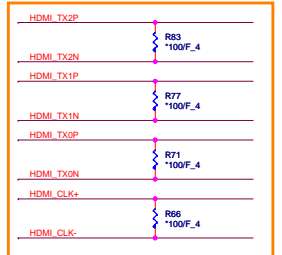
Pre-emphasis and EMI setting	
PRE_EMI	Output
L	No_PRE&EMI
H	PRE enable
M	EMI control

Hot-plug detect	
CFG_HPD	Output
L	Follow SW_MAIN
H	Follow SW_DDC
M	SW or DDC



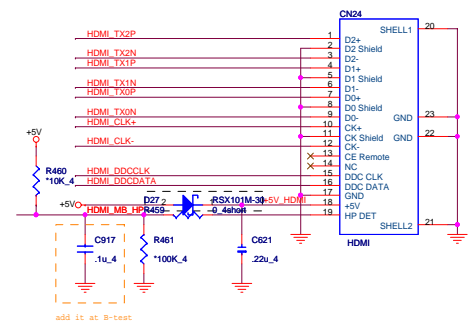
PWDN_ASQ setting	
Pin 25	Output
L	Normal operation (default)
H	Shut down

EMI reserve for HDMI

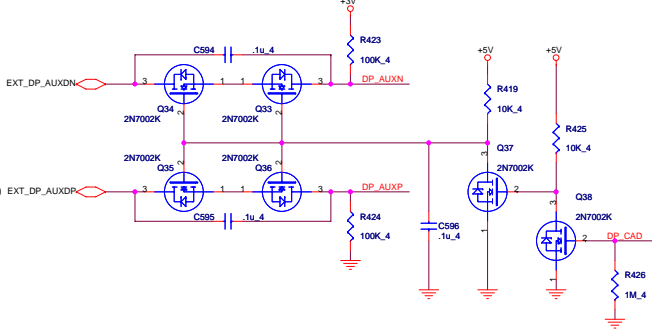


close CN24

HDMI connector

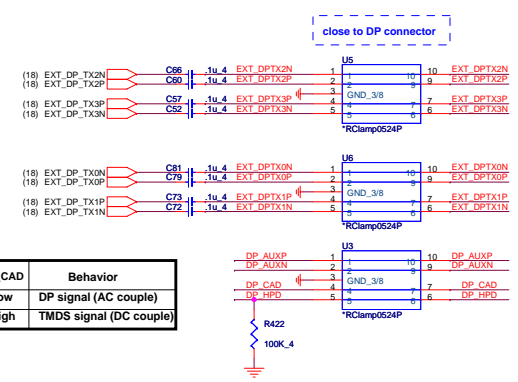


DisplayPort

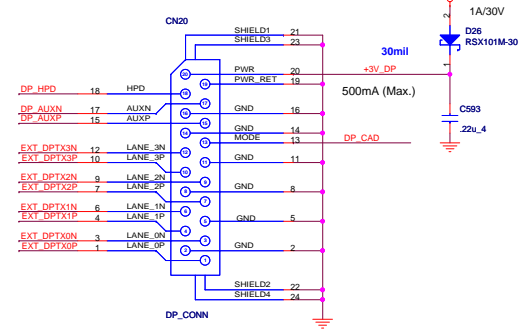


DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

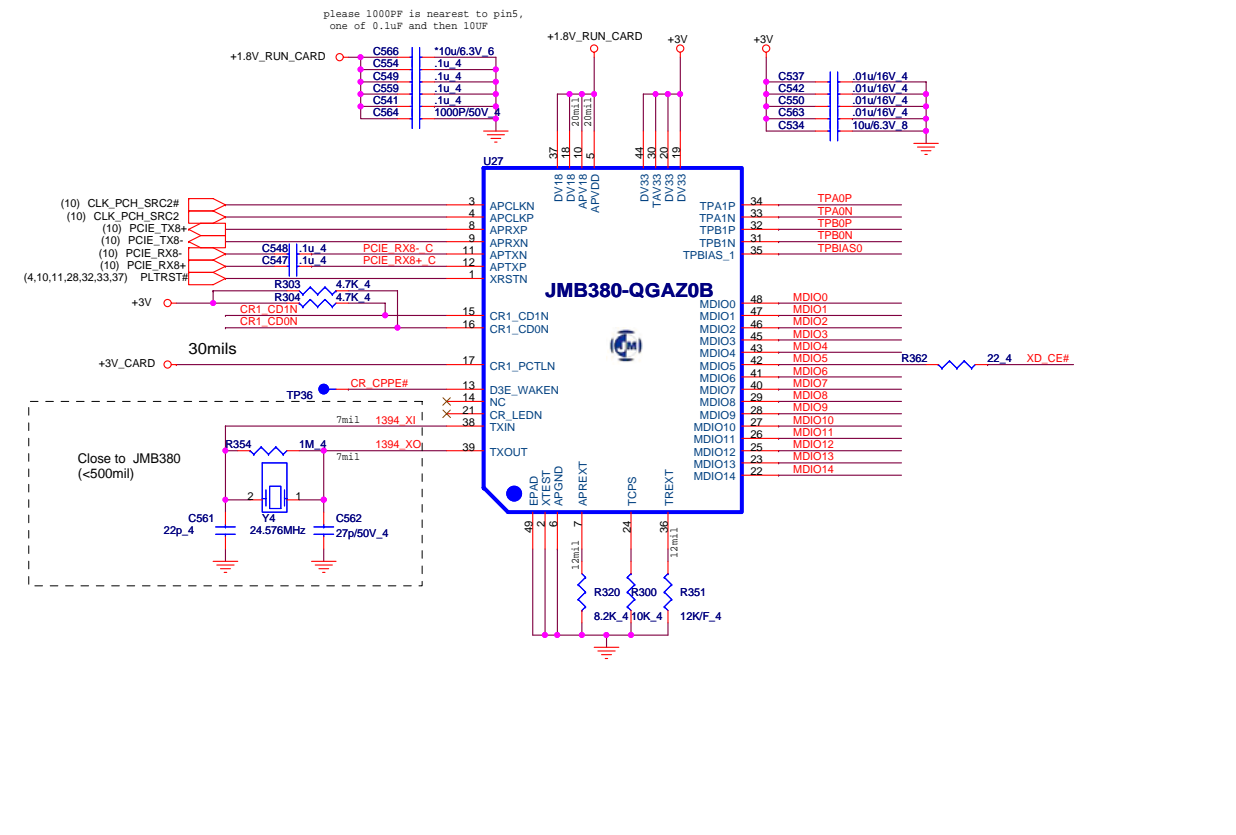
ESD Protect



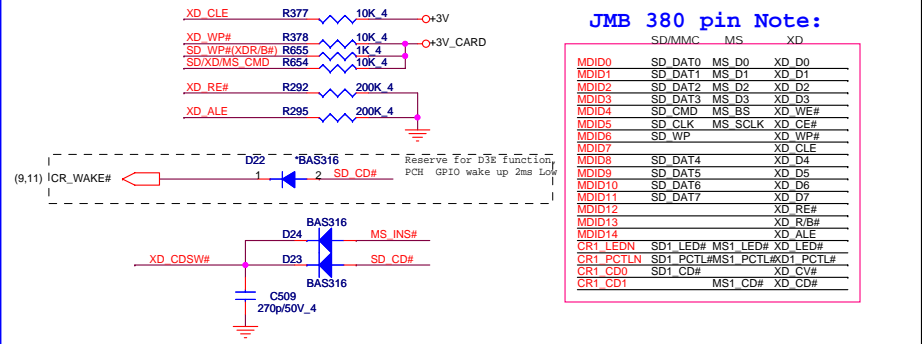
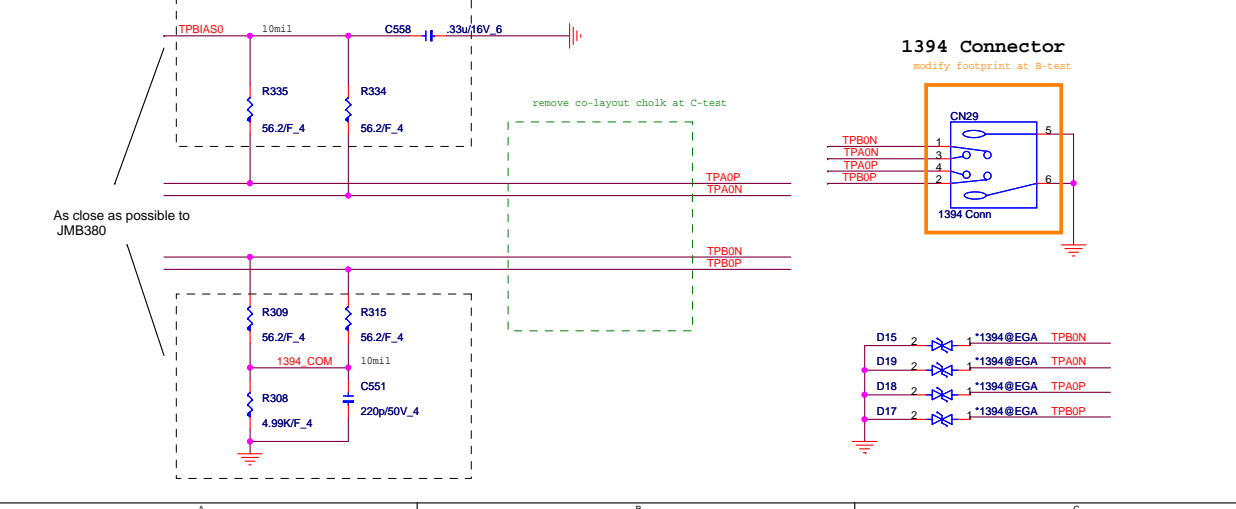
DP connector



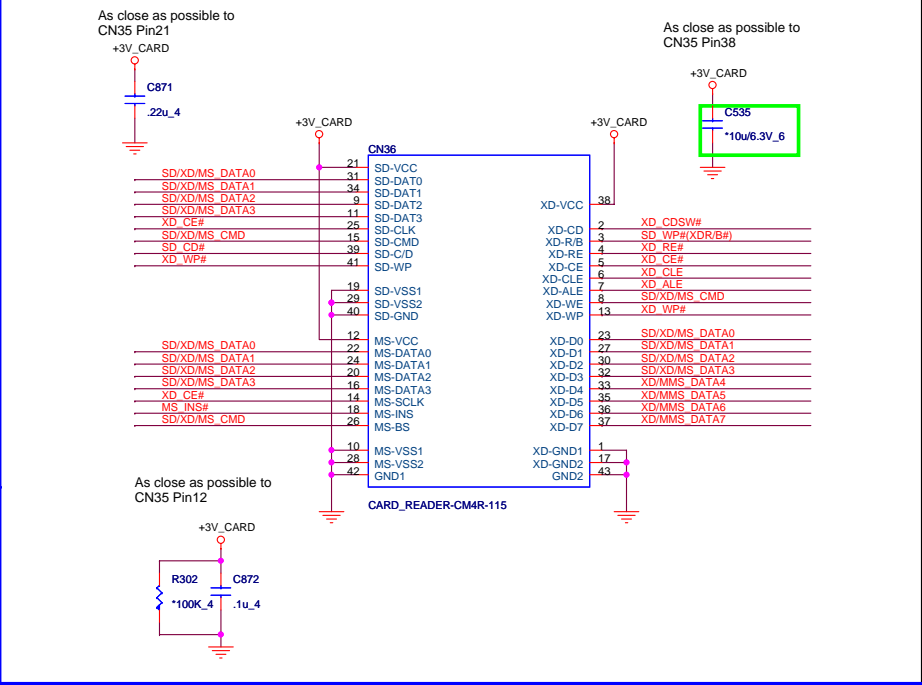
Cardreader/1394



IEEE-1394



5 IN 1 CARD READER



EMI reserve

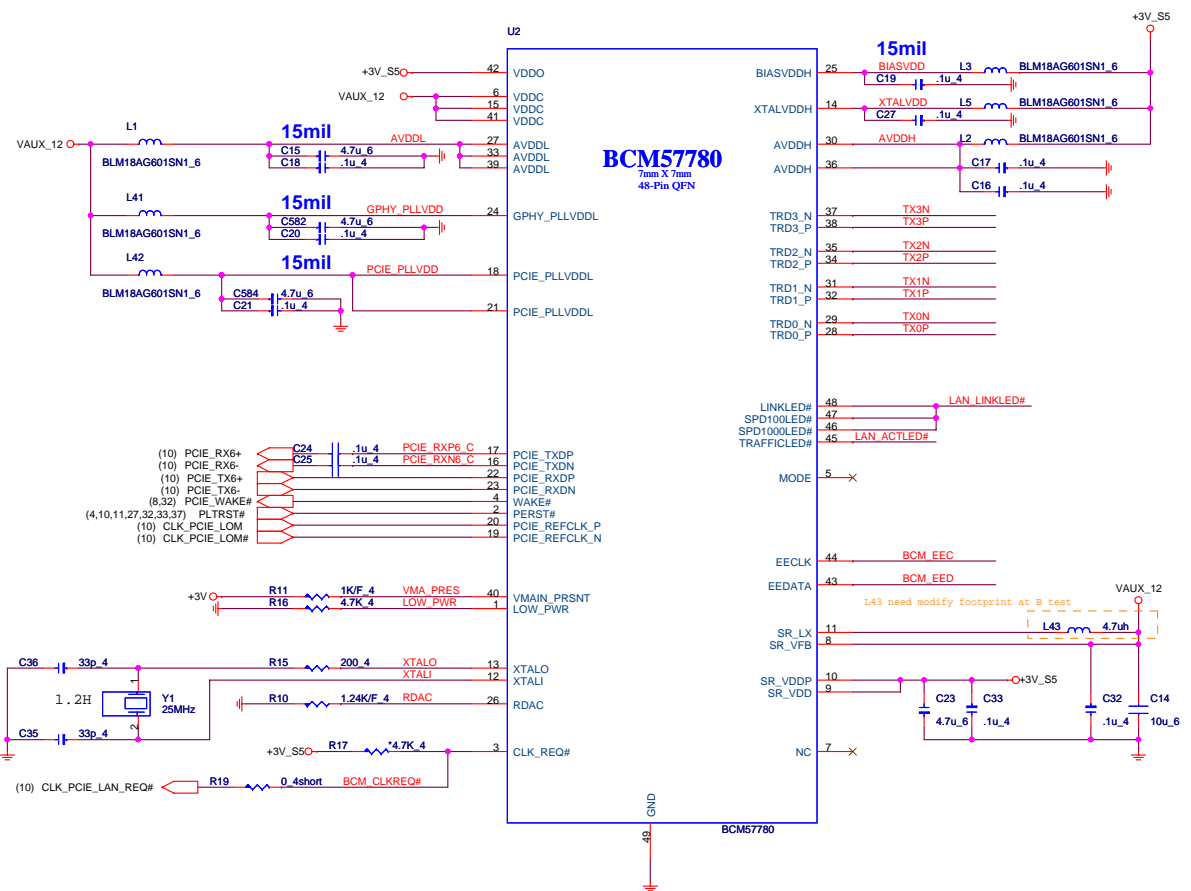
MDIO0	R651	0 4shortD	XD/MS DATA0
MDIO1	R648	0 4shortD	XD/MS DATA1
MDIO2	R652	0 4shortD	XD/MS DATA2
MDIO3	R650	0 4shortD	XD/MS DATA3
MDIO4	R653	0 4shortD	XD/MS CMD
MDIO6	R361	0 4shortD	WP#
MDIO7	R360	0 4shortD	CLE
MDIO8	R649	0 4shortD	MMS DATA4
MDIO9	R647	0 4shortD	MMS DATA5
MDIO10	R646	0 4shortD	MMS DATA6
MDIO11	R645	0 4shortD	MMS DATA7
MDIO12	R299	0 4shortD	RE#
MDIO13	R656	0 4shortD	WP#(XDR/B#)
MDIO14	R301	0 4shortD	ALE
CR1_CD1N	R294	0 4shortD	MS_INS#
CR1_CD0N	R293	0 4shortD	CD#

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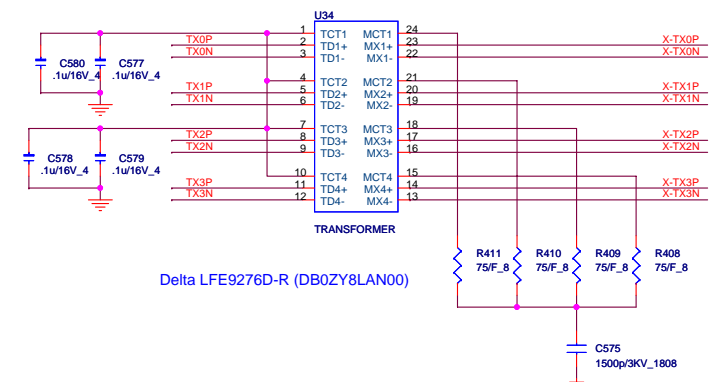
Size: Document Number
JMB380 Card Reader & 1394
Rev 1A

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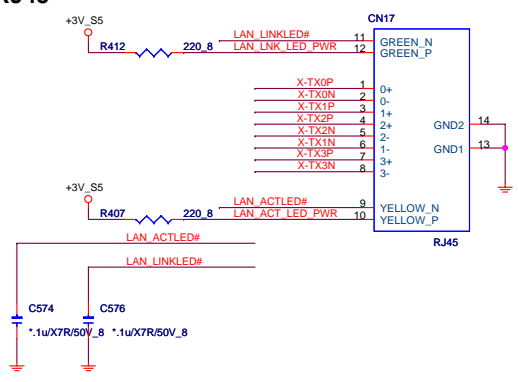
Giga-LAN BCM57780



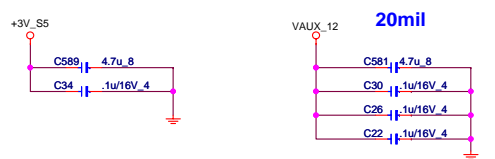
TRANSFORMER



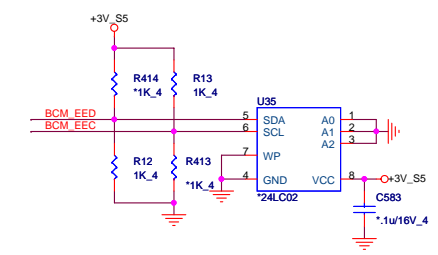
RJ45



LAN POWER



EEPROM



EEPROM Strapping

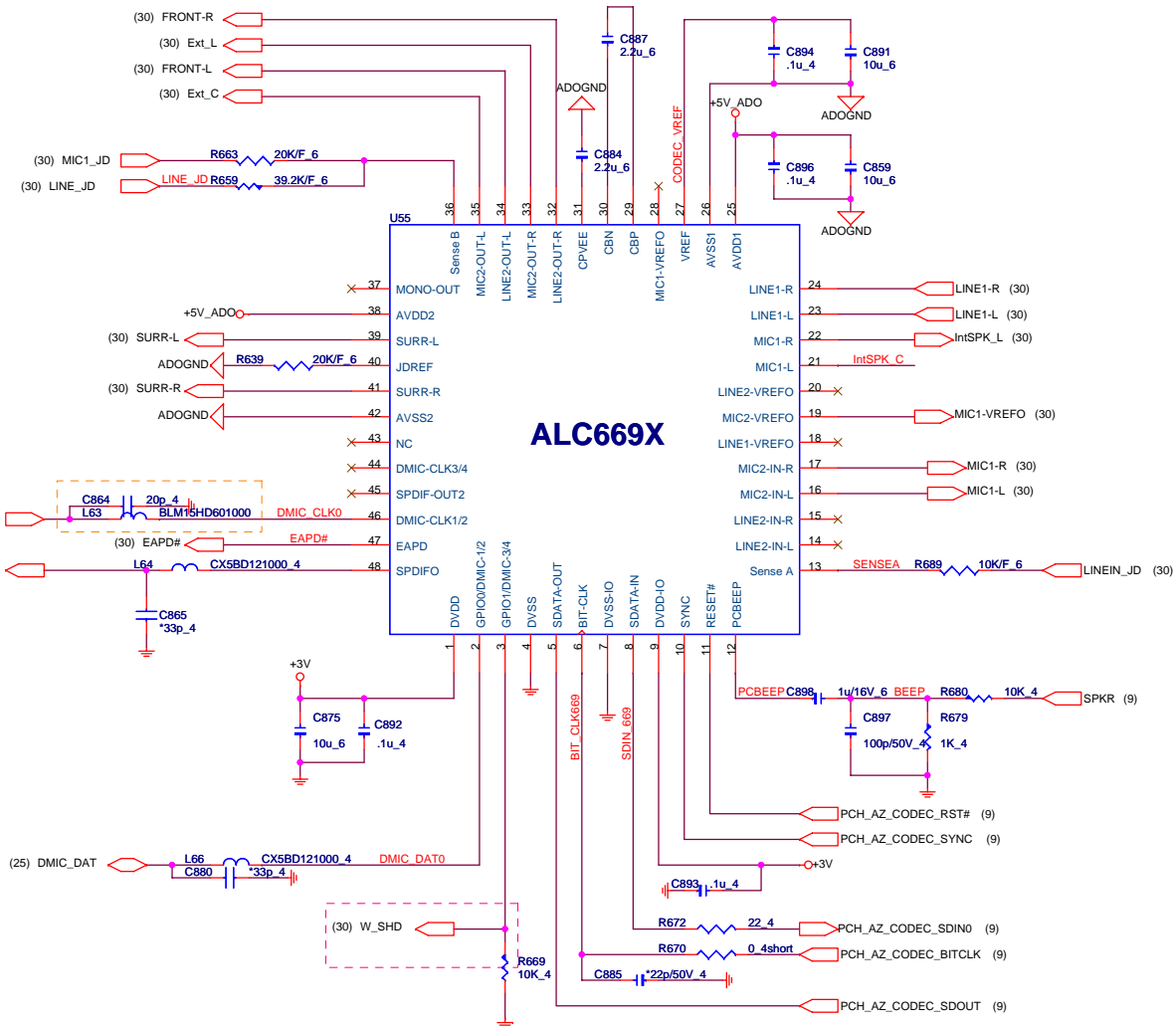
EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

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Size	Document Number	Rev	1A
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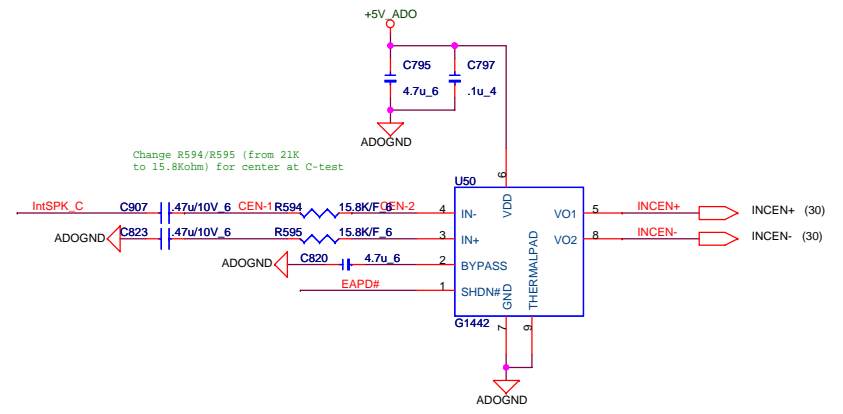
LAN (BCM57780)

CODEC(ALC669X)

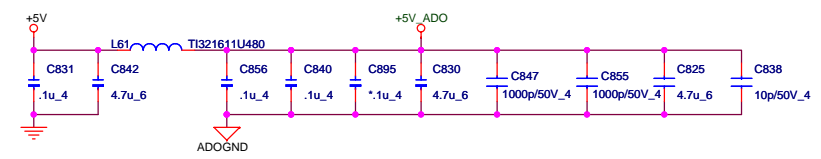


ALC669X

CENTER MONO

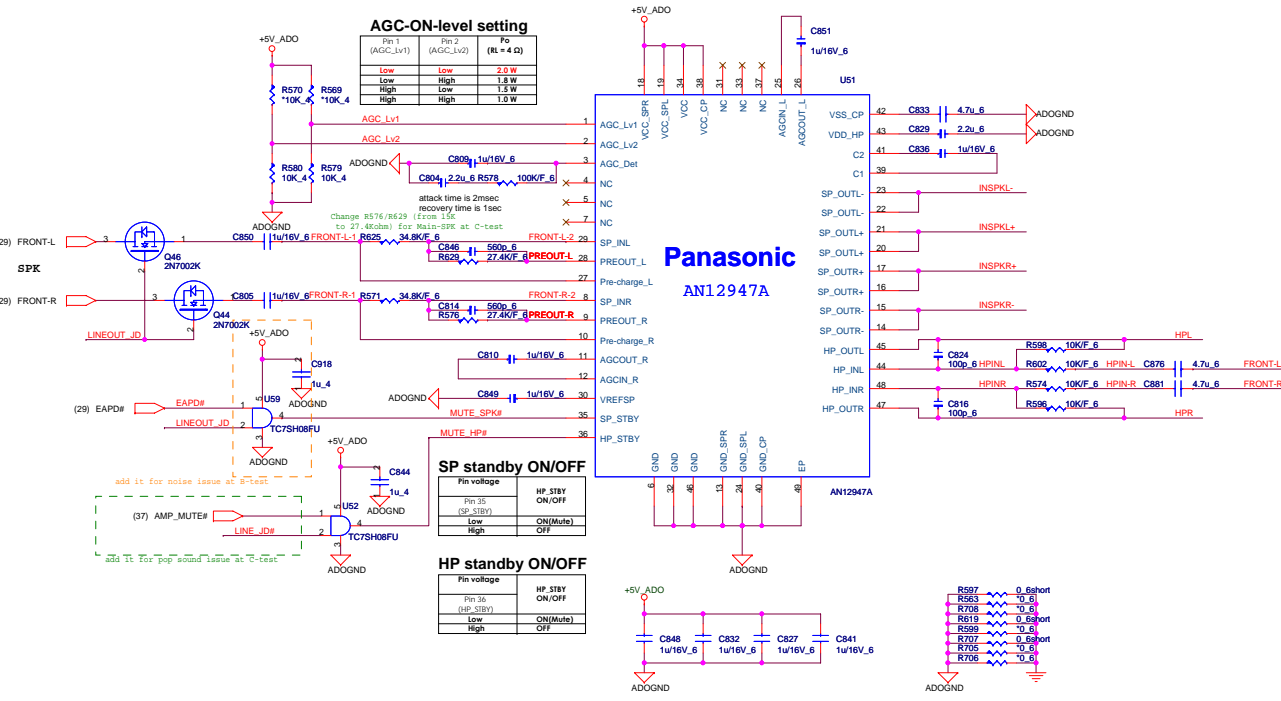


CODEC/AMP Power

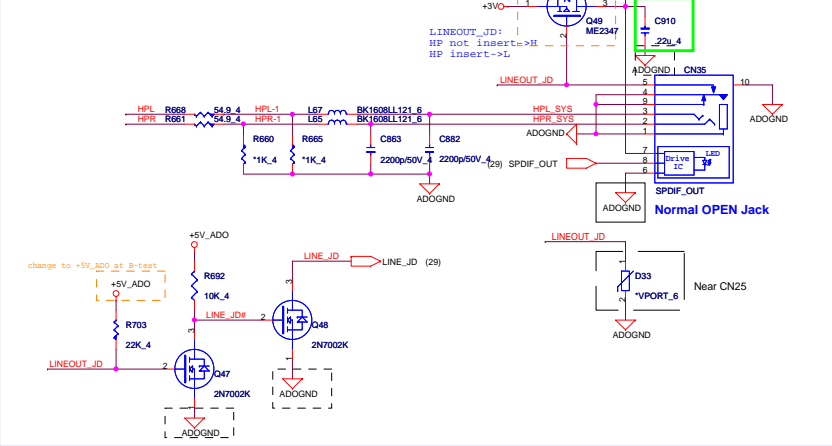


Size	Document Number	Rev
	REALTEK ALC889X/MONO-AMP	1A
Date:	Monday, November 02, 2009	Sheet 29 of 49

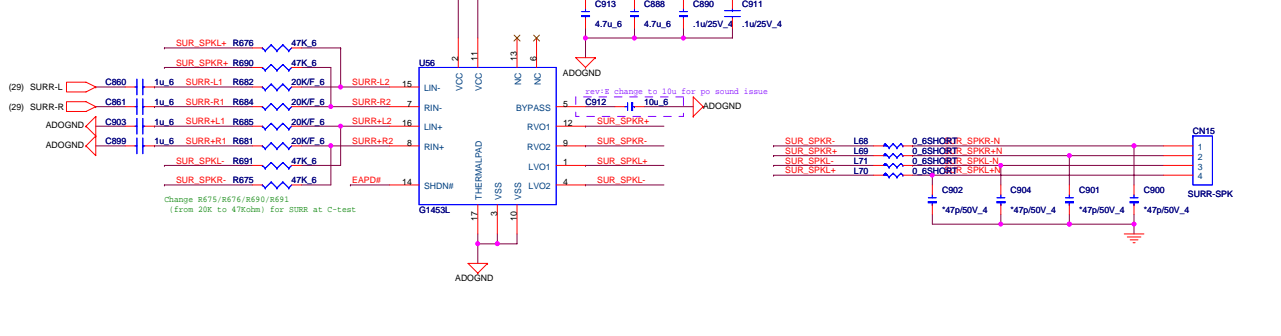
SPEAKER/HP AMP.



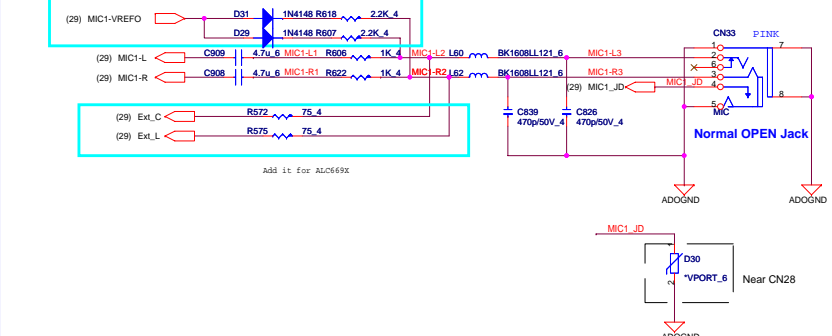
LINE-OUT/SPDIFO



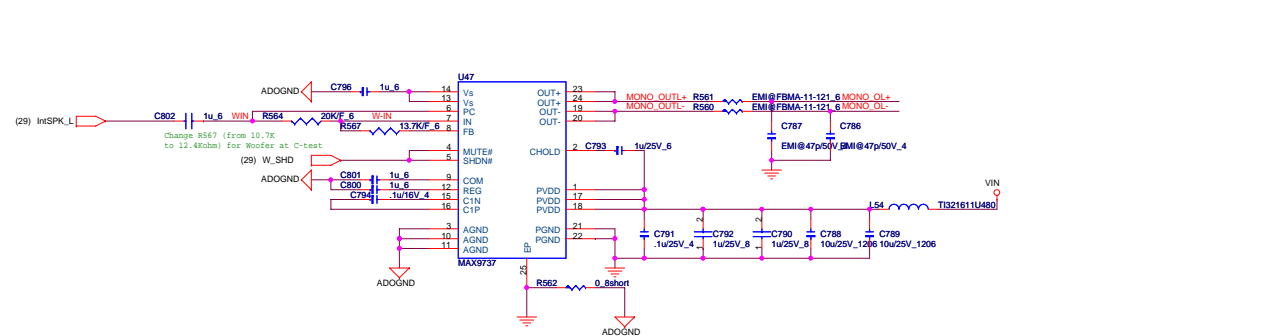
SURR-SPK



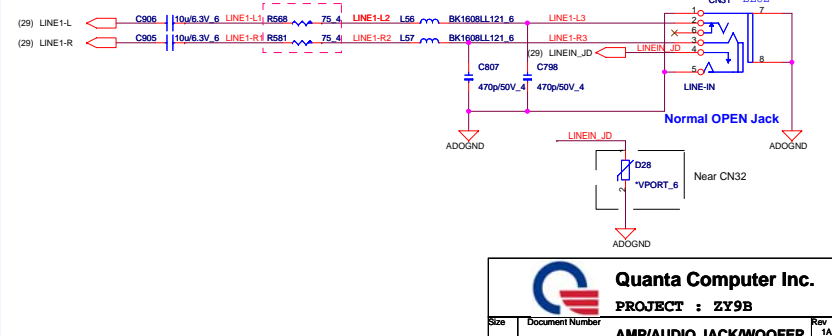
MIC



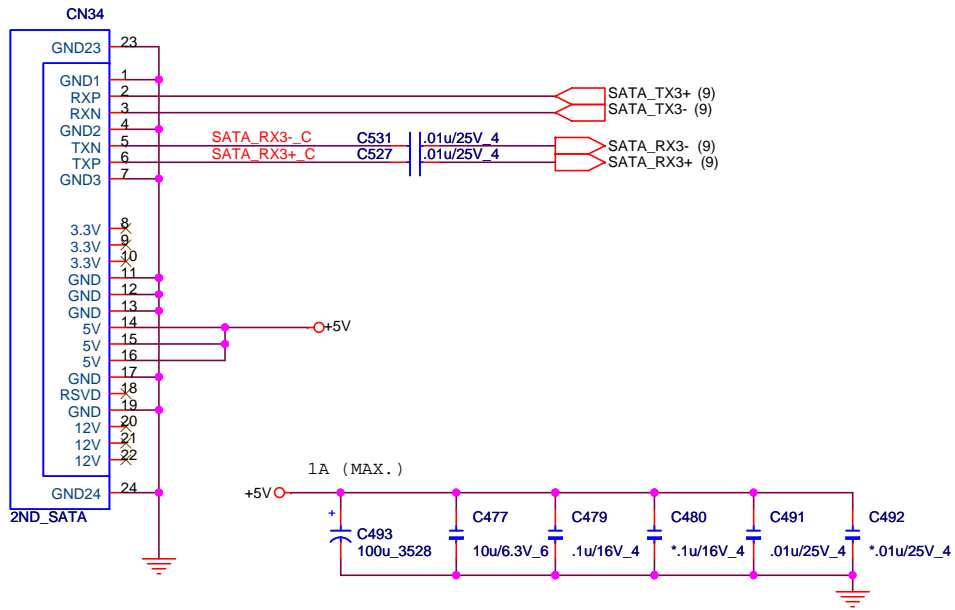
SUBWOOFER



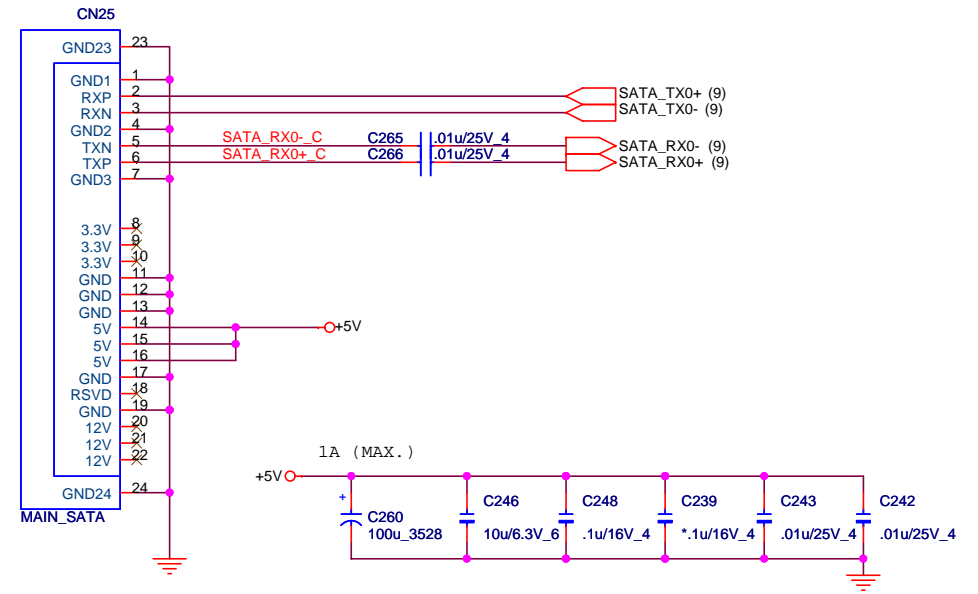
LINE IN



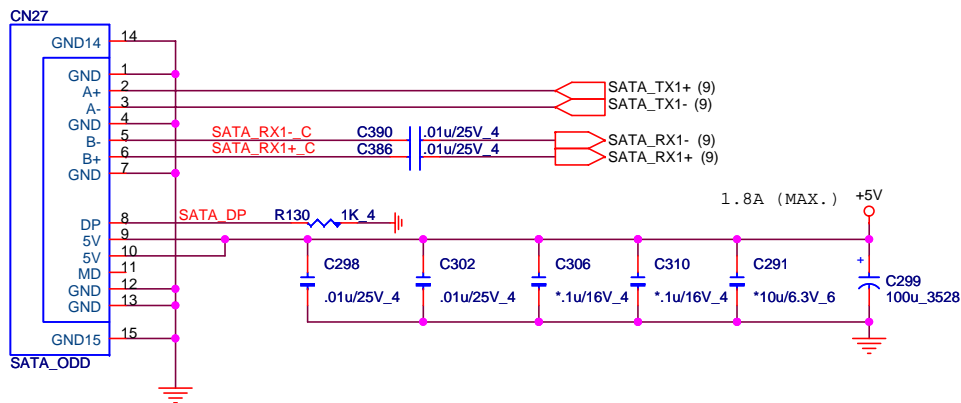
2nd SATA HDD (edge of board)



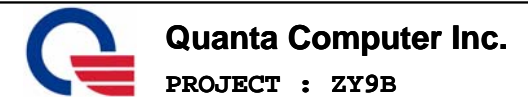
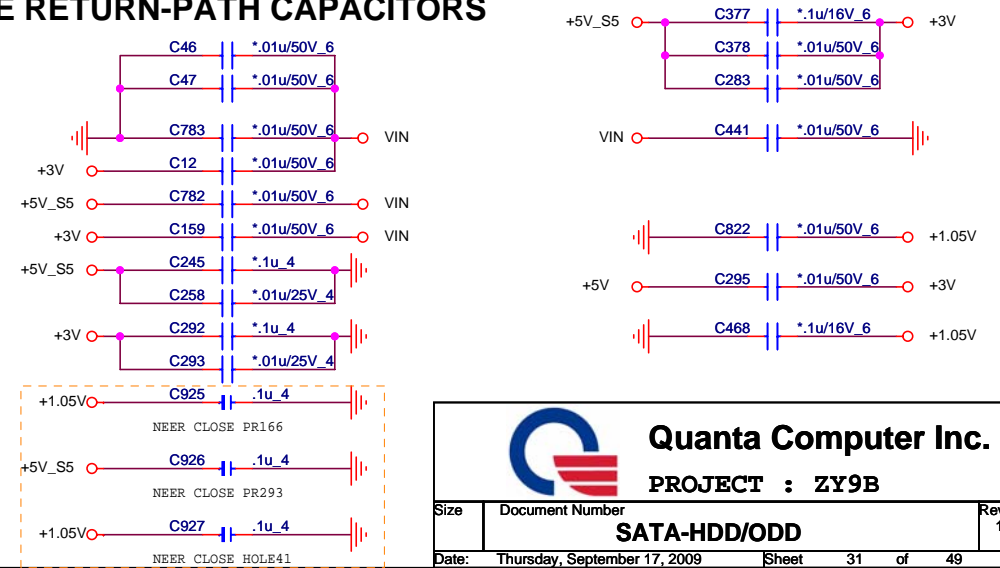
MAIN SATA HDD



ODD (SATA)



EE RETURN-PATH CAPACITORS

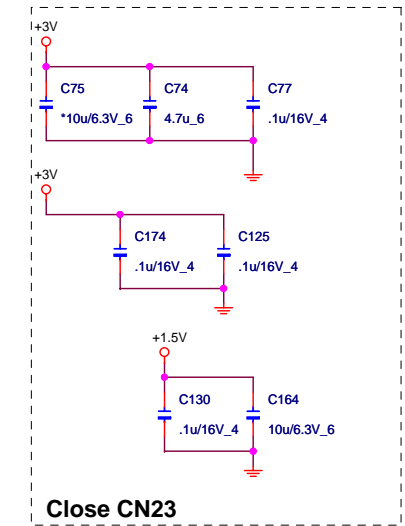
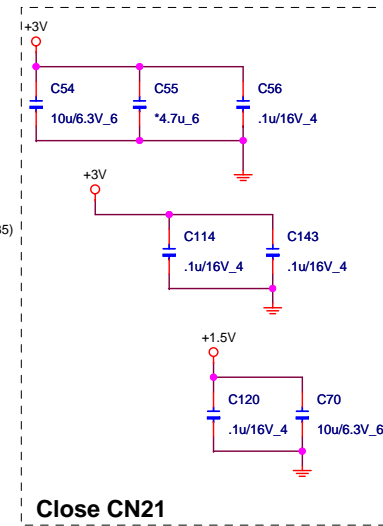
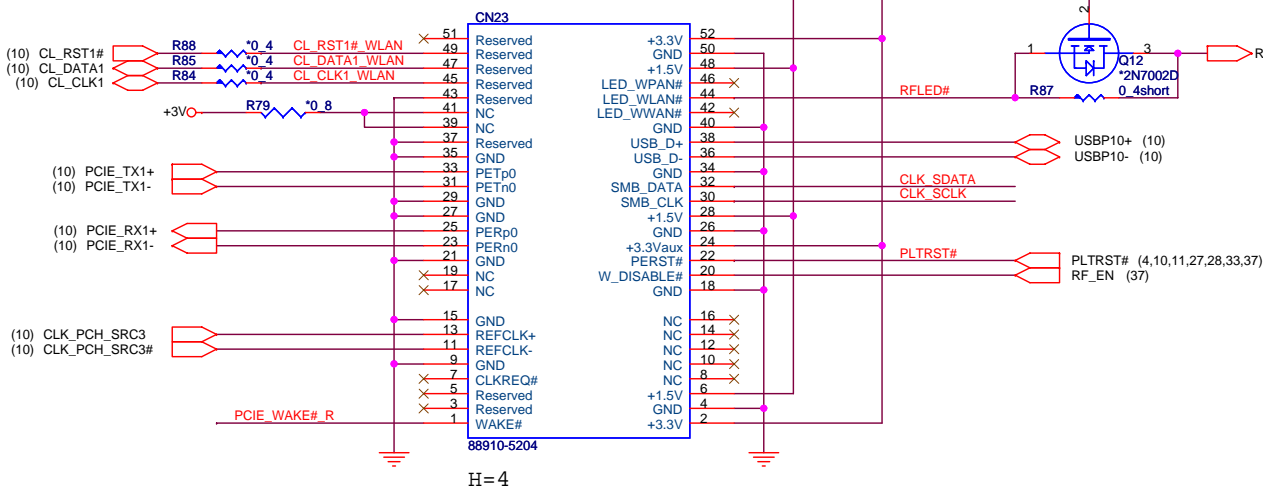


Size	Document Number	Rev
	SATA-HDD/ODD	1A
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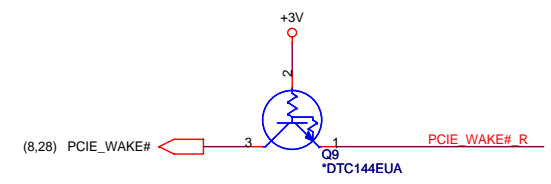
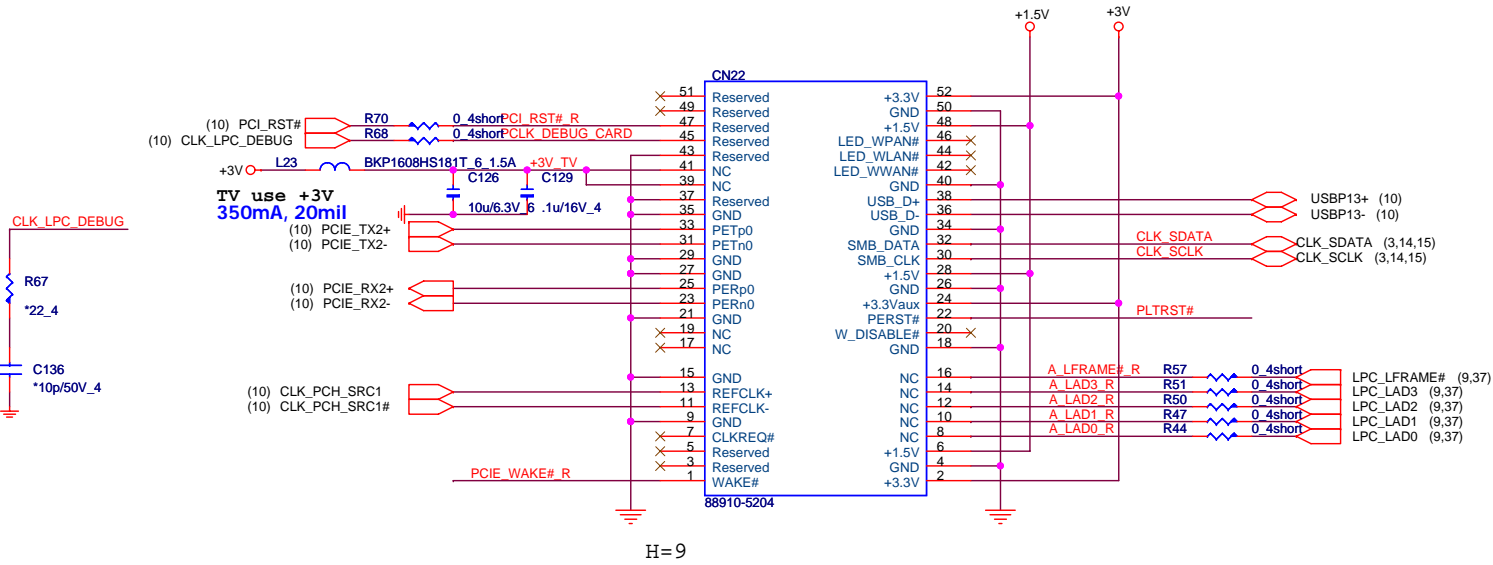
Wireless

+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA

Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4

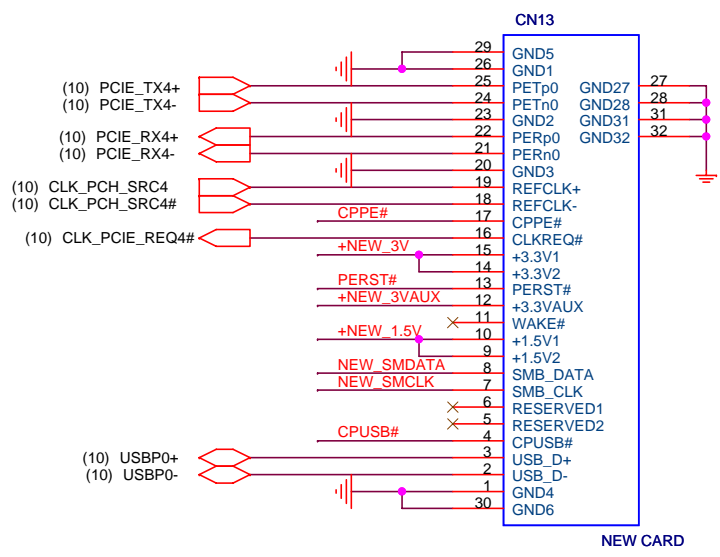


TV and Debug



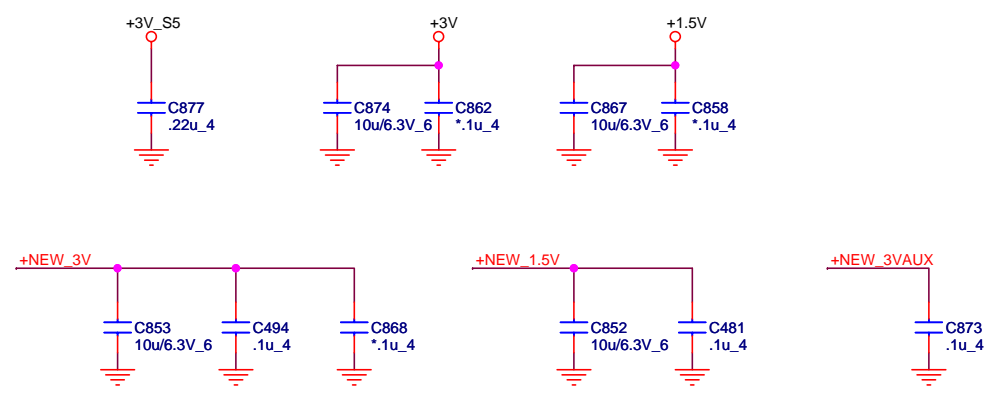
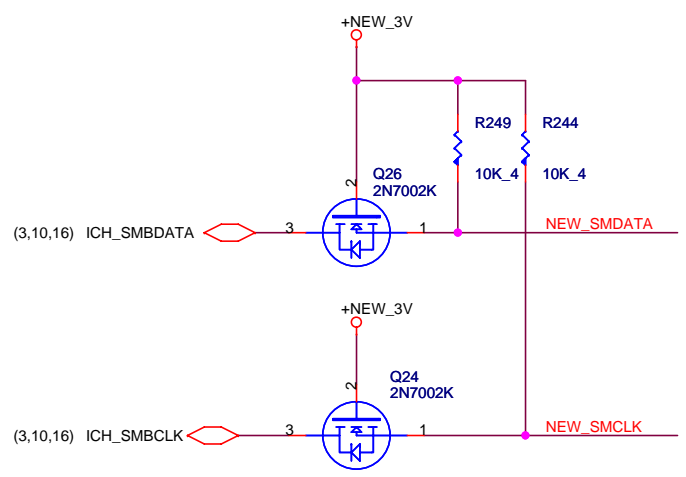
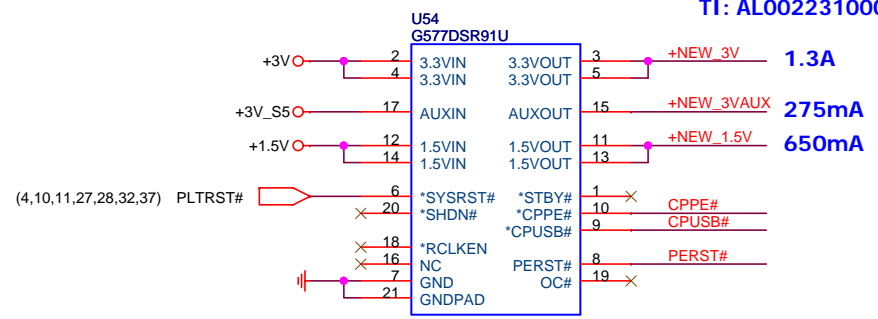
		Quanta Computer Inc.	
		PROJECT : ZY9B	
Size	Document Number	MINI PCI-E card/TV	
Date:	Monday, November 02, 2009	Sheet	32 of 49
			Rev 1A

NEW CARD



NEW CARD'S POWER SWITCH

GMT: AL000577002
TI: AL002231000

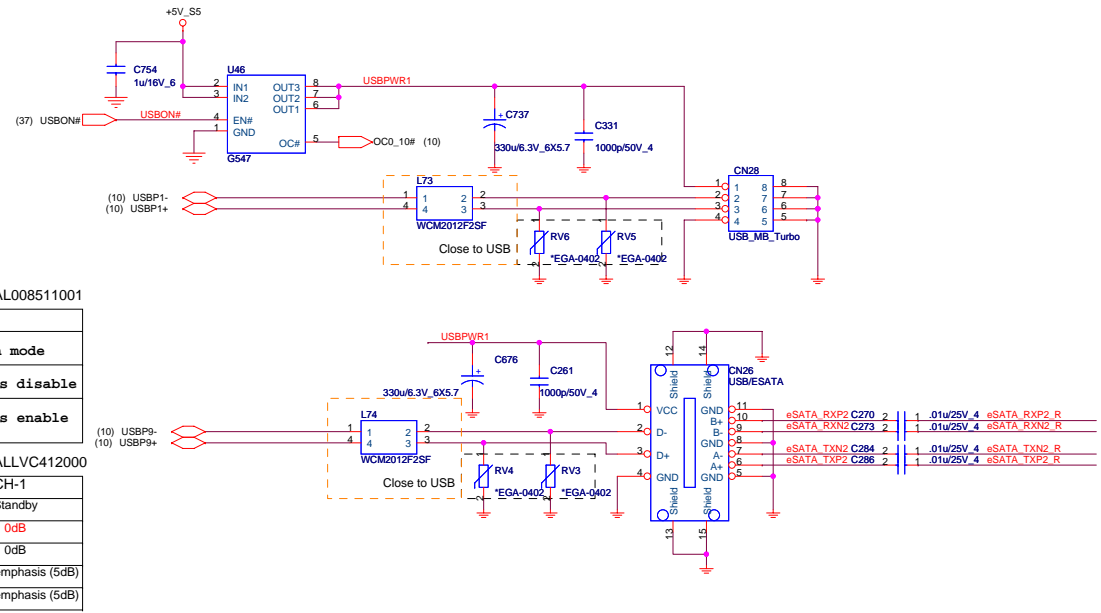
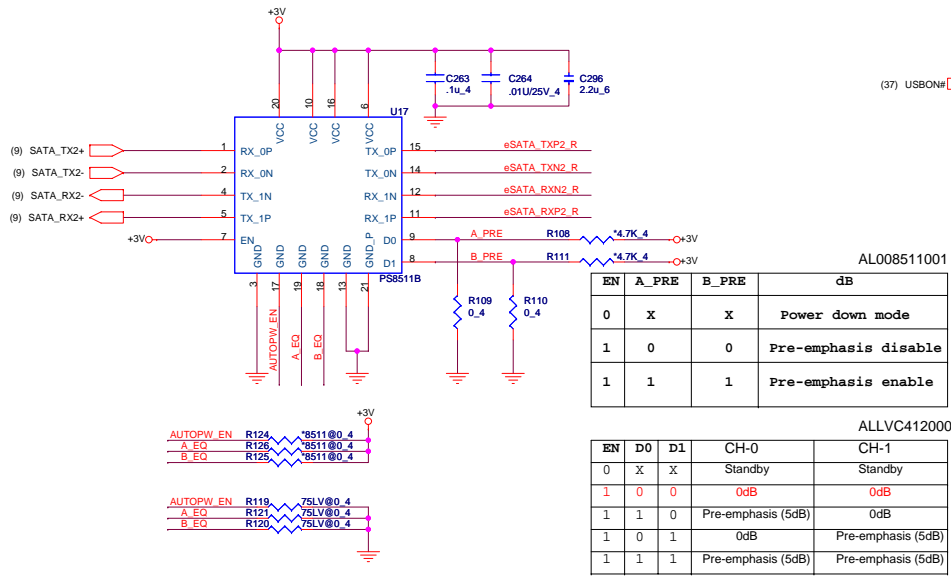


Quanta Computer Inc.
PROJECT : ZY9B

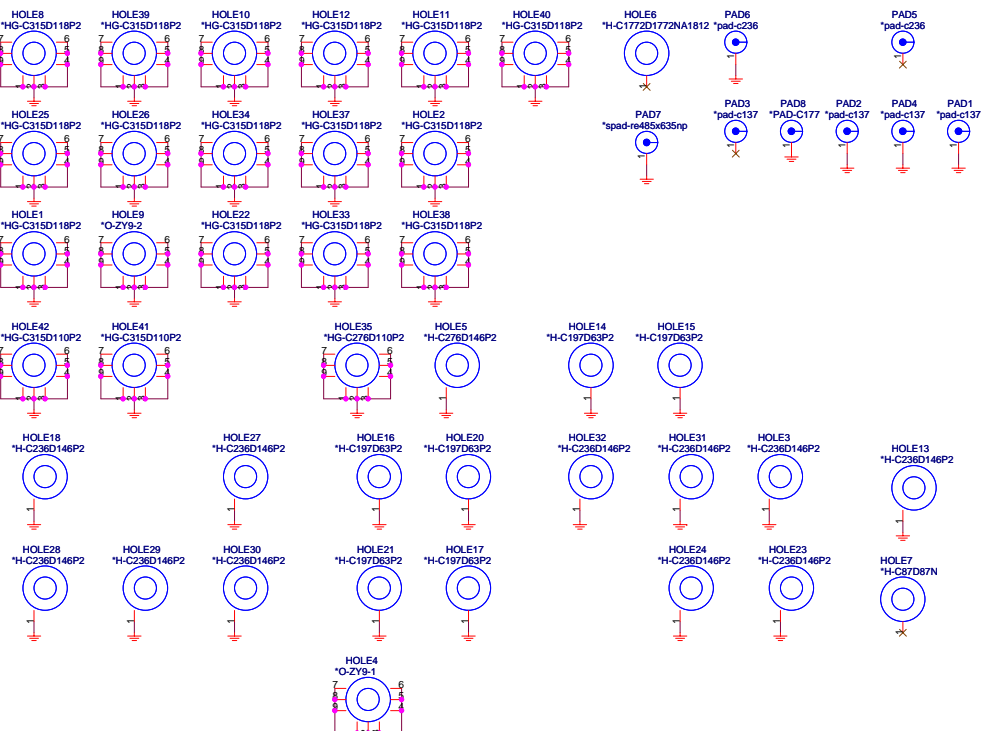
Size	Document Number	Rev 1A
Date: Thursday, September 17, 2009		Sheet 33 of 49

NEW CARD

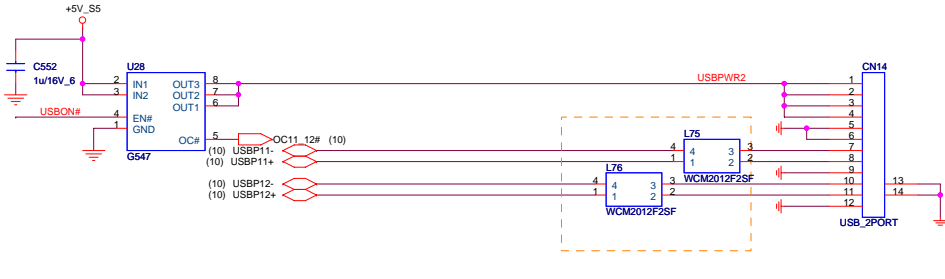
USB & ESATA



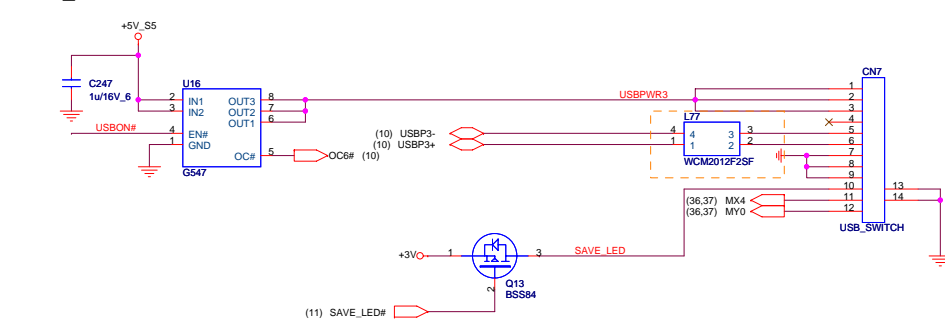
HOLES



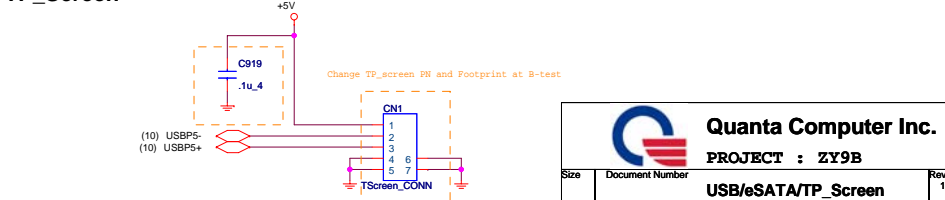
USB_2PORT/B



USB_SWITCH/B

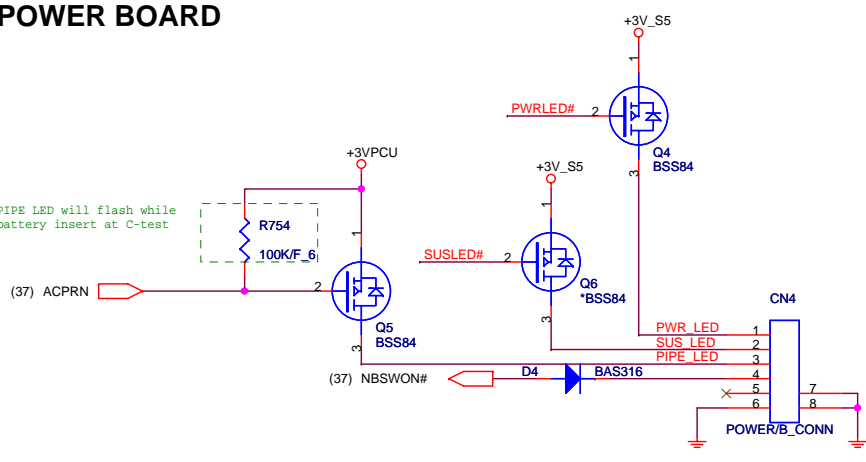


TP_Screen

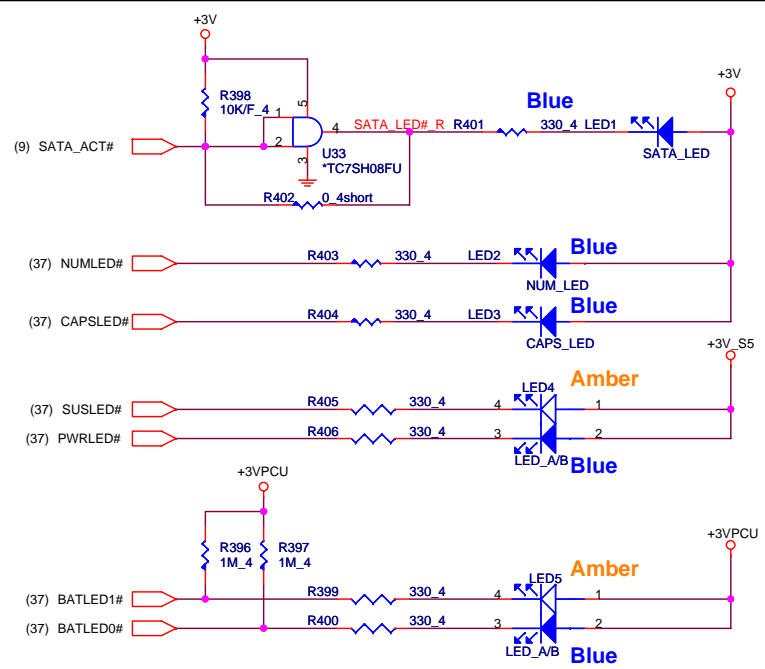


POWER BOARD

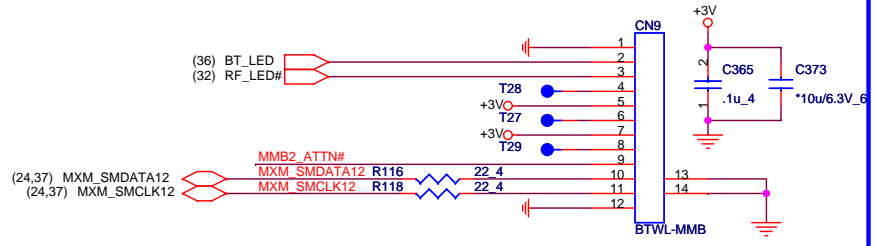
PIPE LED will flash while battery insert at C-test



M/B LED

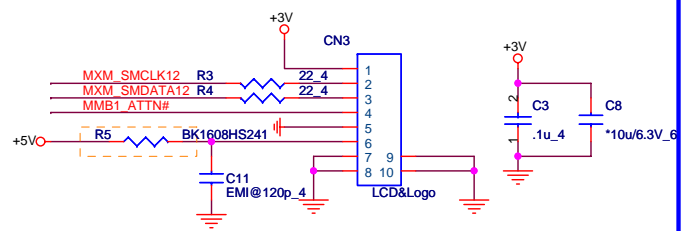


Left side MMB

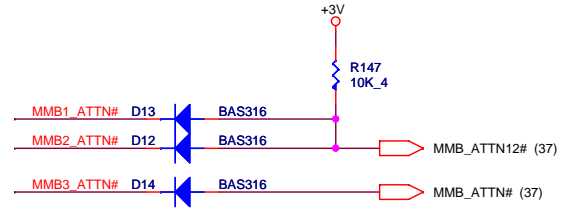


MXMCLK=MXM_SMCLK; MXMDATA=MXM_SMDATA12
MMB1 and MMB2 need add ISOLATE circuit where are on MXM page.

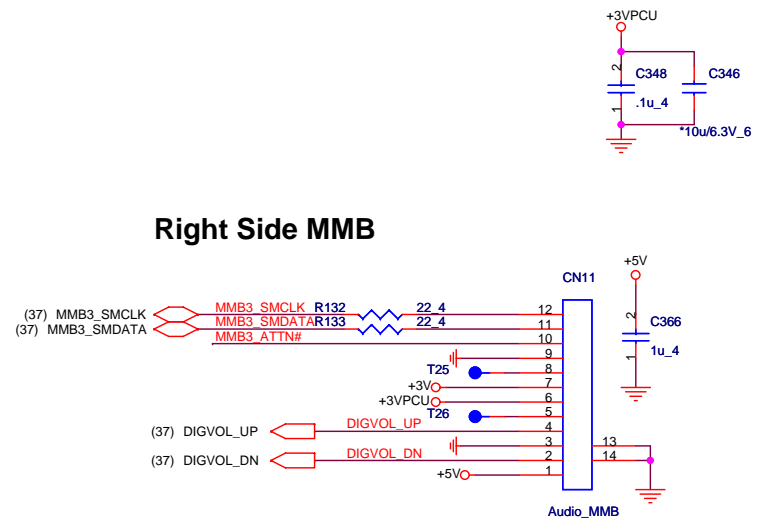
LCD BL_ON/OFF MMB & Backlight Logo LED



MMB Status

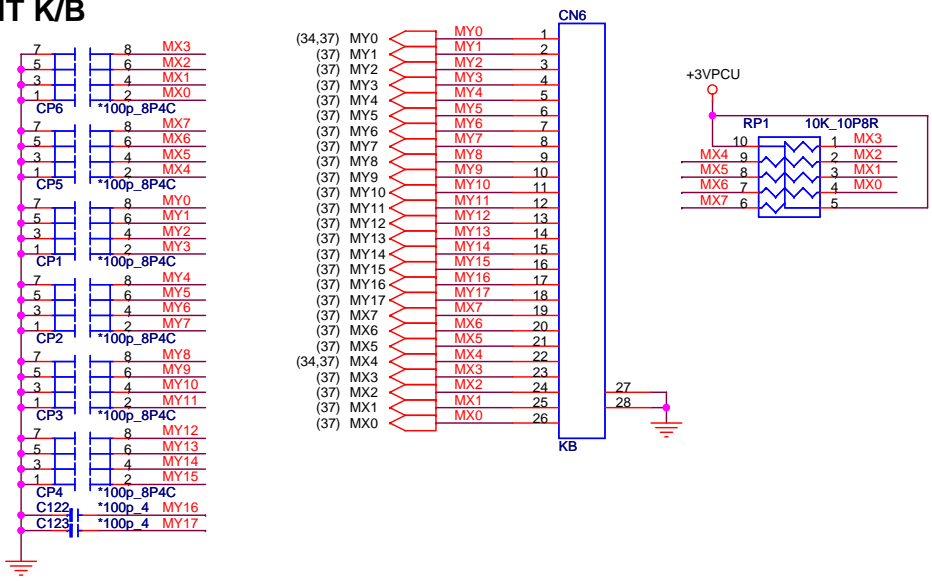


Right Side MMB

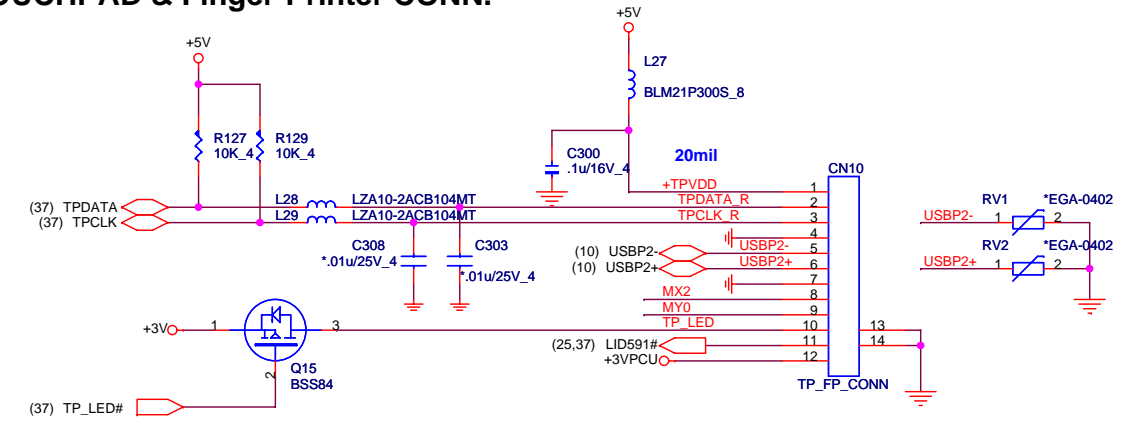


Quanta Computer Inc. PROJECT : ZY9B		Rev	1A
		POWER/MMB/LAUNCH/LED	
Date:	Monday, November 02, 2009	Sheet	35 of 49

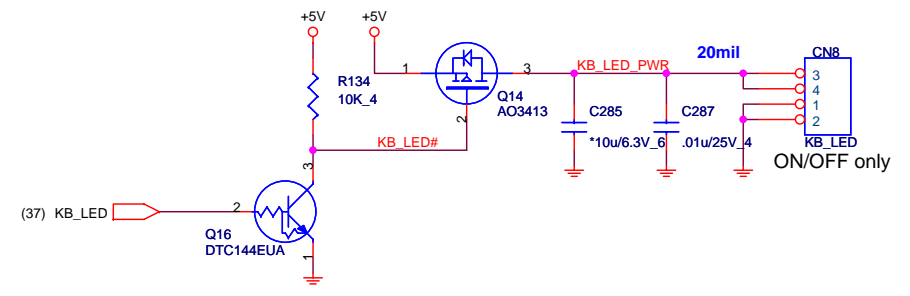
INT K/B



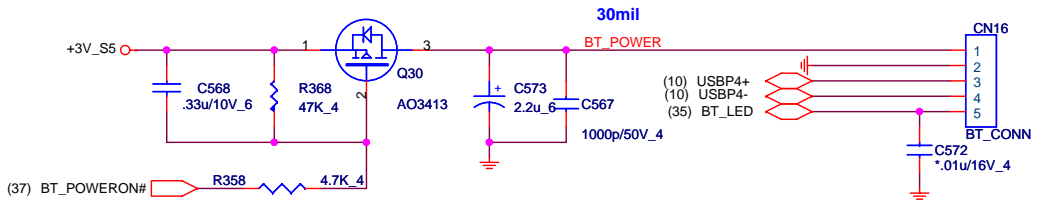
TOUCHPAD & Finger-Printer CONN.



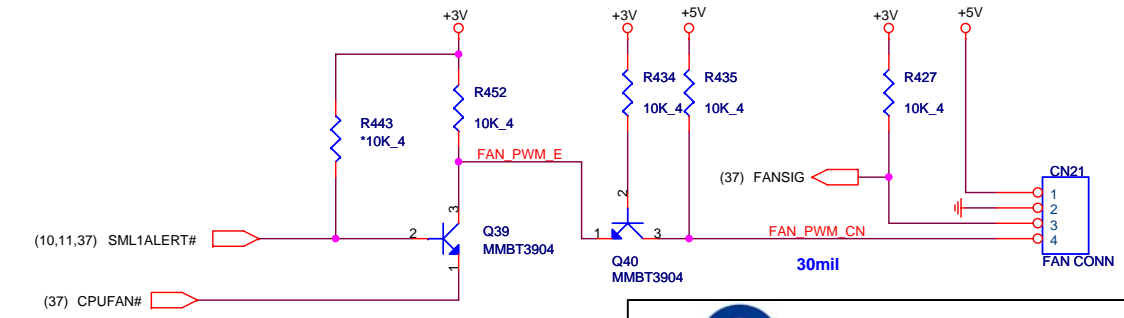
Keyboard LED control




BLUETOOTH CONNECTOR



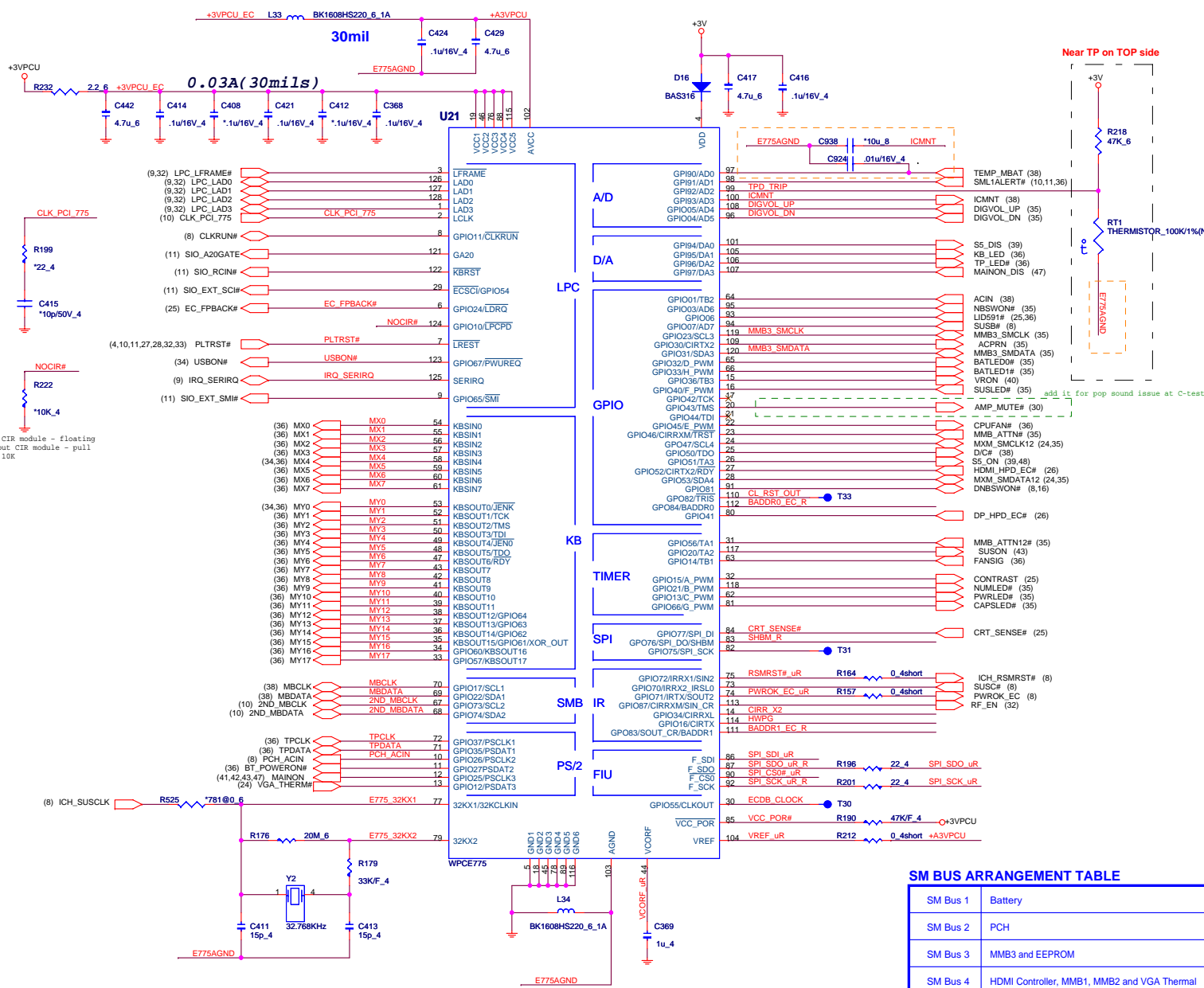
CPU FAN





Quanta Computer Inc.
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Size	Document Number	Rev
	KB/FAN/TP+FP/BT	1A
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I/O ADDRESS SETTING

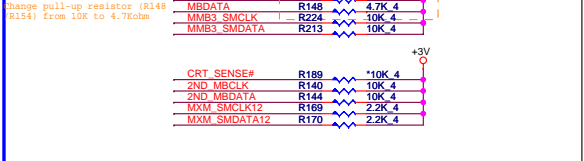
I/O Address	
BADDR1-0	Index Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

SHBM=0: Enable shared memory with host BIOS

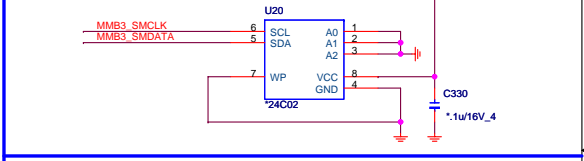
BADDR0 = BADDR0_EC_R R227 10K_4
 BADDR1 = BADDR1_EC_R R220 10K_4
 SHBM = SHBM_R R183 10K_4

1/13 Conform by vendor mail :
 Disabled (*) if using FWH device on LPC.
 Enabled (0) if using SPI flash for both system BIOS and EC firmware

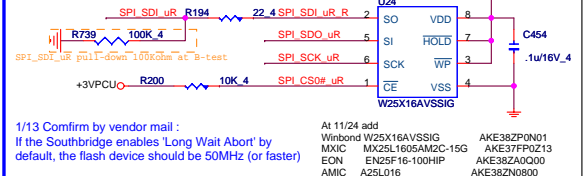
SM BUS PU



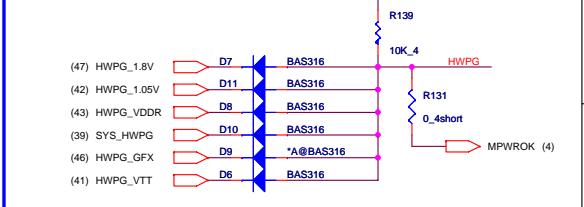
ACER ID



SPI FLASH



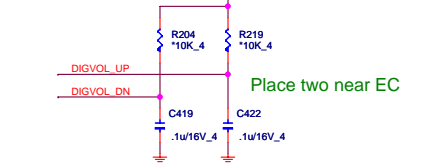
HWPG



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Thermal

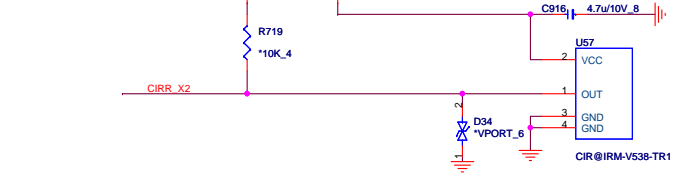
VR Cap.



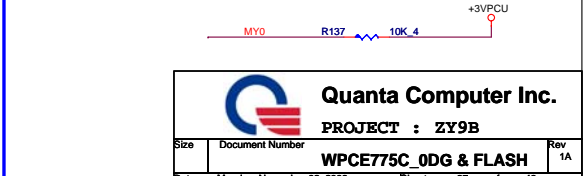
POWER-ON Switch

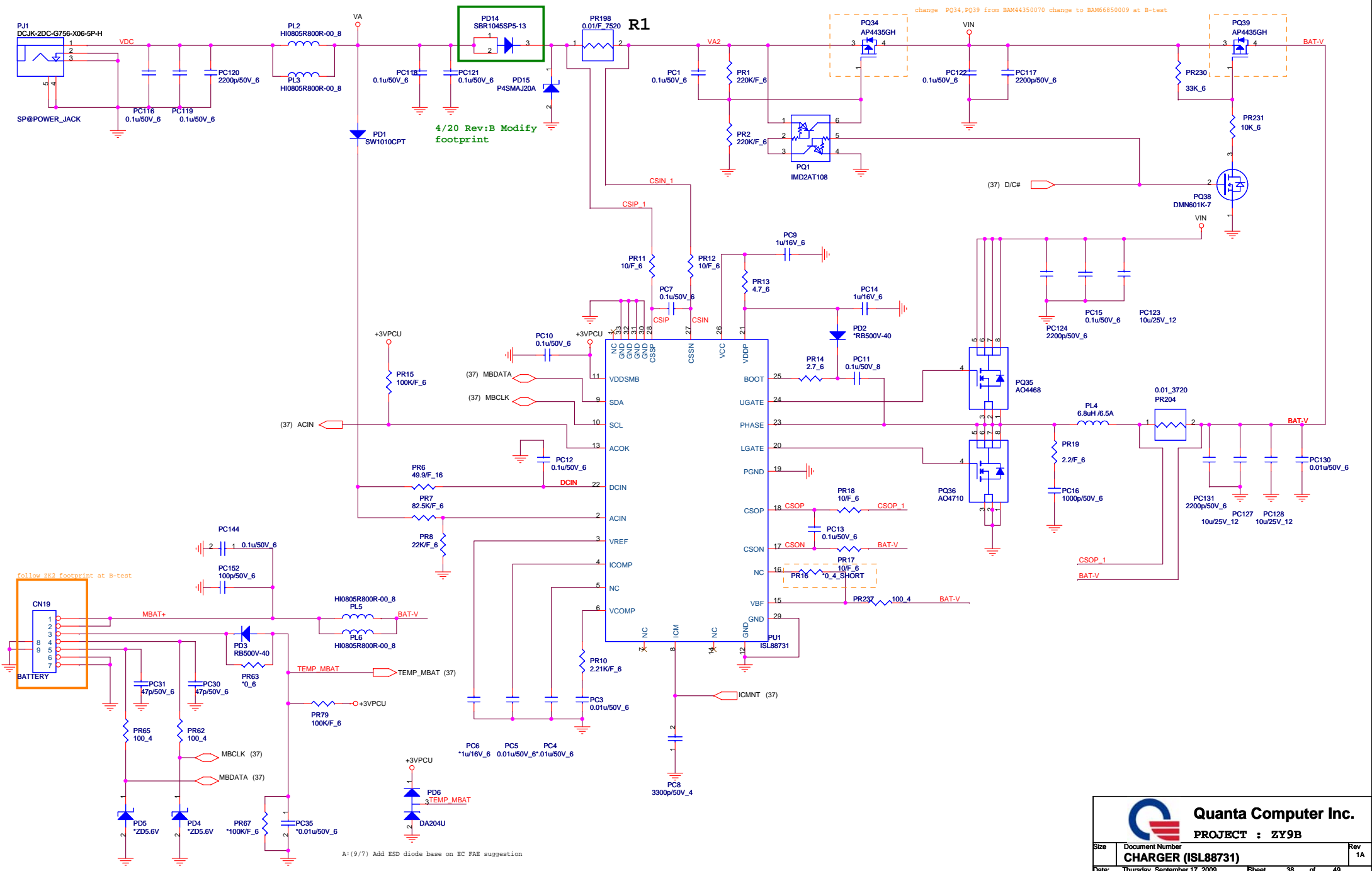


CIR



INTERNAL KEYBOARD STRIP SET






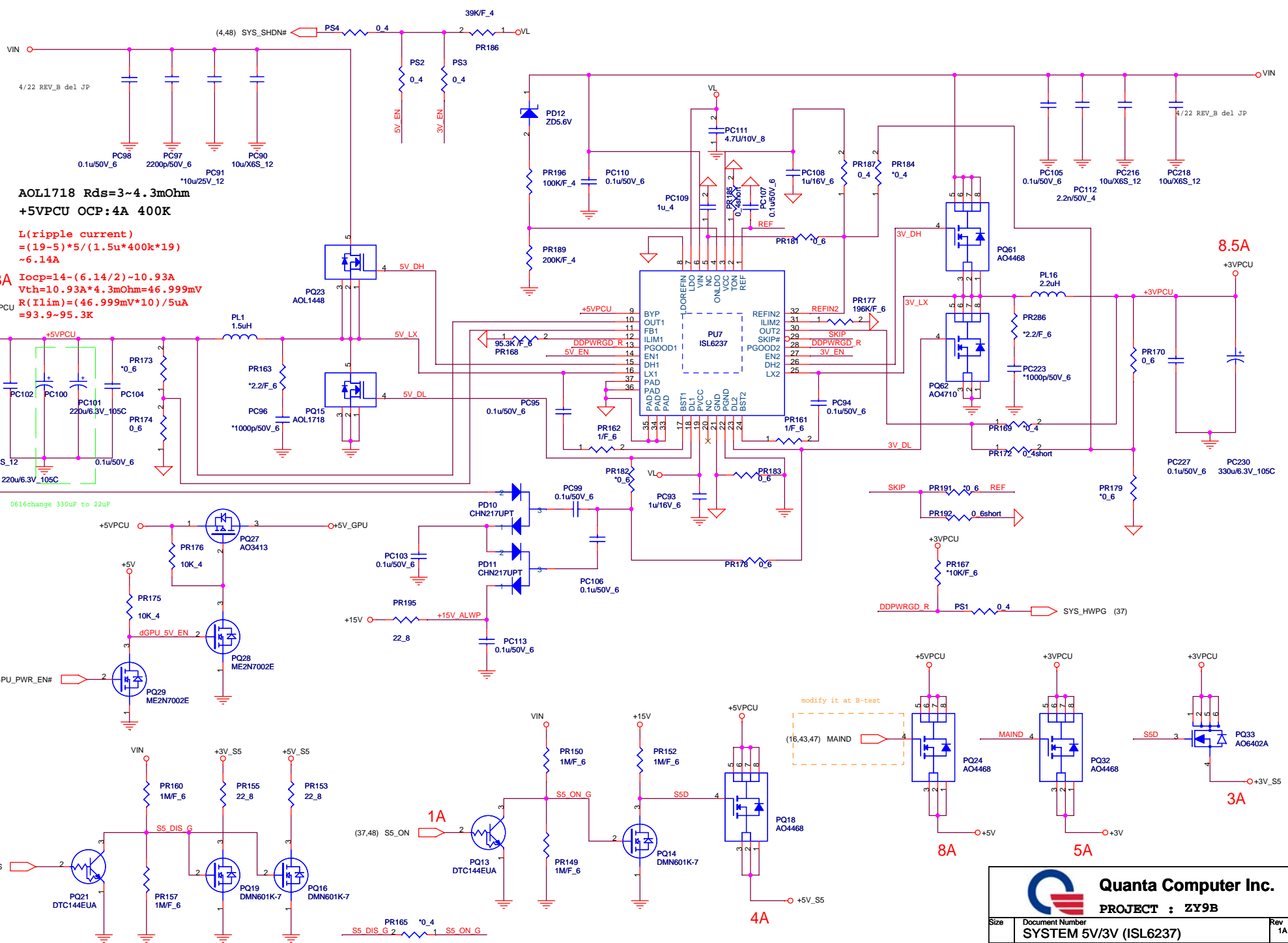
change PQ34,PQ39 from B4M44350070 change to B4M66850009 at B-test

4/20 Rev:B Modify footprint

follow ZK2 footprint at B-test

A:(9/7) Add ESD diode base on EC FAB suggestion

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Size	Document Number	Rev
	CHARGER (ISL88731)	1A
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AOL1718 $R_{ds} = 3 \sim 4.3 \text{m}\Omega$
+5VPCU OCP: 4A 400K

$I(\text{ripple current}) = (19-5) * 5 / (1.5 \mu * 400k * 19) \sim 6.14 \text{A}$

13A $I_{ocp} = 14 - (6.14 / 2) \sim 10.93 \text{A}$
 $V_{th} = 10.93 \text{mV} * 4.3 \text{m}\Omega = 46.999 \text{mV}$
 $R(I_{lim}) = (46.999 \text{mV} * 10) / 5 \mu \text{A} = 93.9 \sim 95.3 \text{k}\Omega$

8.5A

8A

5A

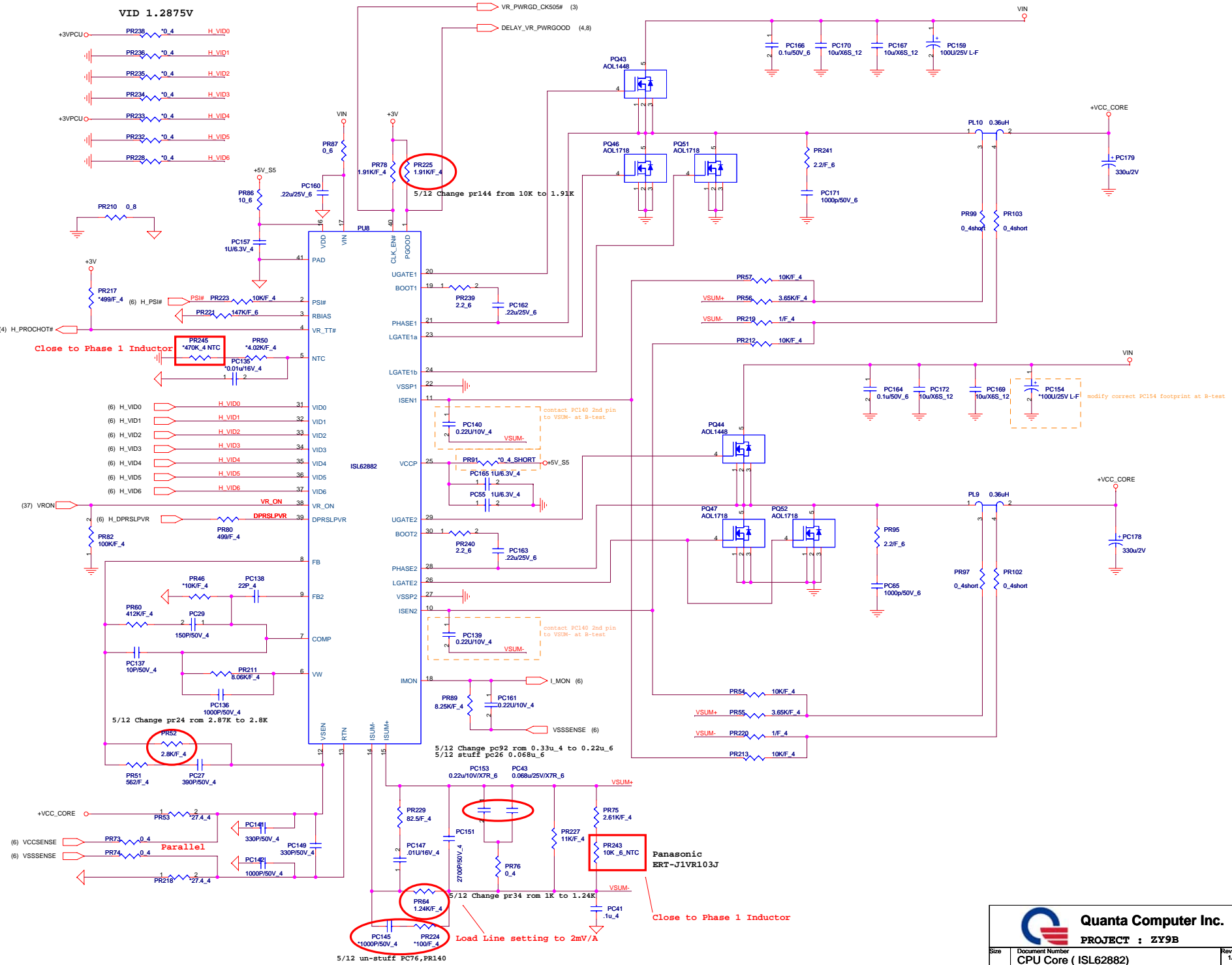
3A

4A

Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	SYSTEM 5V/3V (ISL6237)	1A
Date:	Monday, November 02, 2009	Sheet 39 of 49

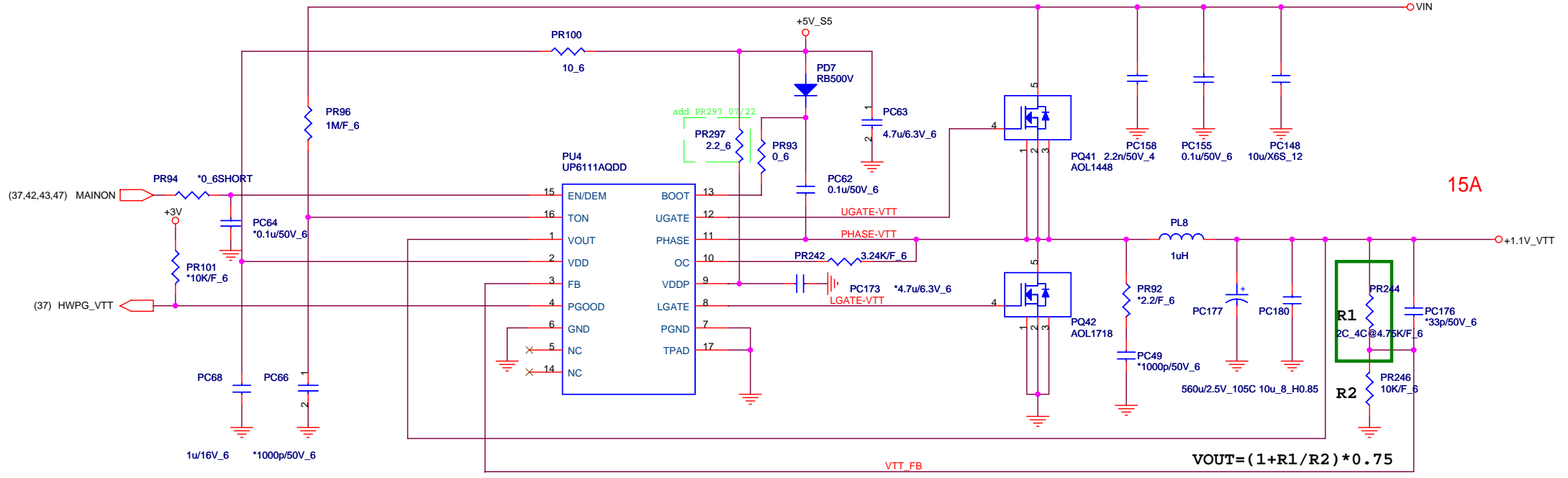
VID 1.2875V



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Size	Document Number	Rev
	CPU Core (ISL62882)	1A
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[PWM]



15A

$$VOUT = (1 + R1/R2) * 0.75$$

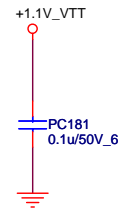
AO1718 $R_{dson} = 3 \sim 4.3m\Omega$

$L(\text{ripple current})$
 $= (19 - 1.05) * 1.05 / (1\mu * 272k * 19)$
 $\sim 3.64A$
 $4.3m * 15 = RILIM * 20\mu A$
 $RILIM = 3.24K (3.22K)$

BOM change notice

Arrandale (1.05V) R1 = 4.02K (CS24023F928)
 Clarksfield (1.1V) R1 = 4.75K (CS24753F919)

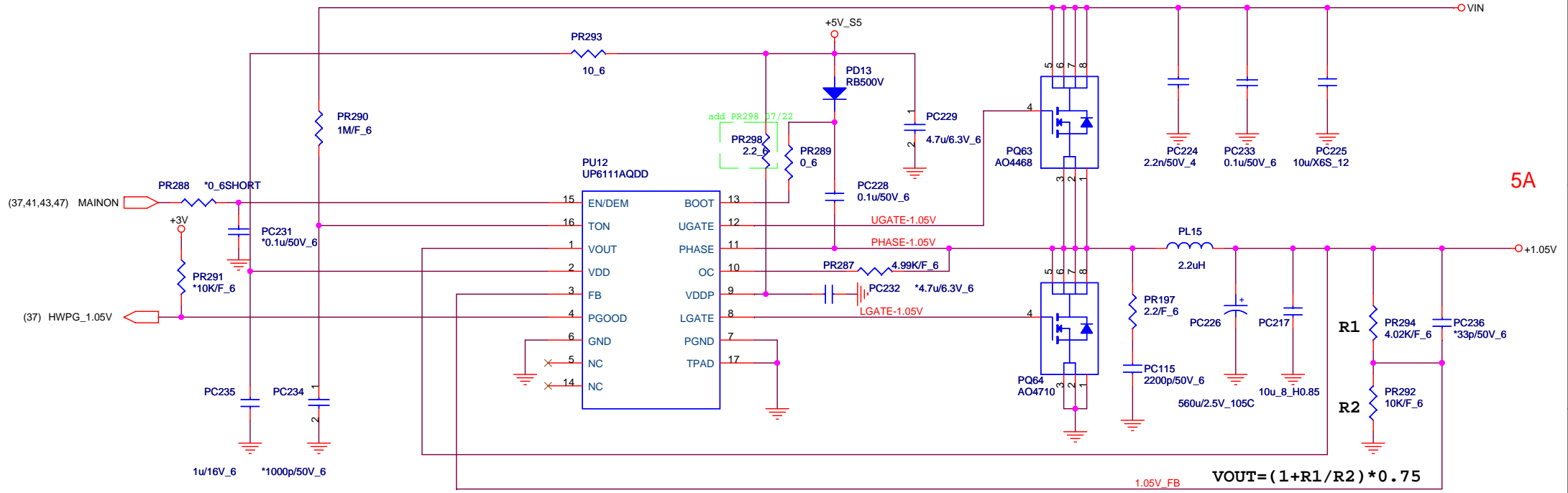
5/4
PR157 change to 4.75K



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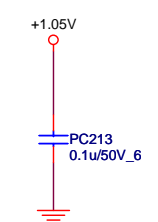
Size	Document Number	Rev
	+VTT (UP6111A)	1A
Date:	Thursday, September 17, 2009	Sheet 41 of 49


[PWM]

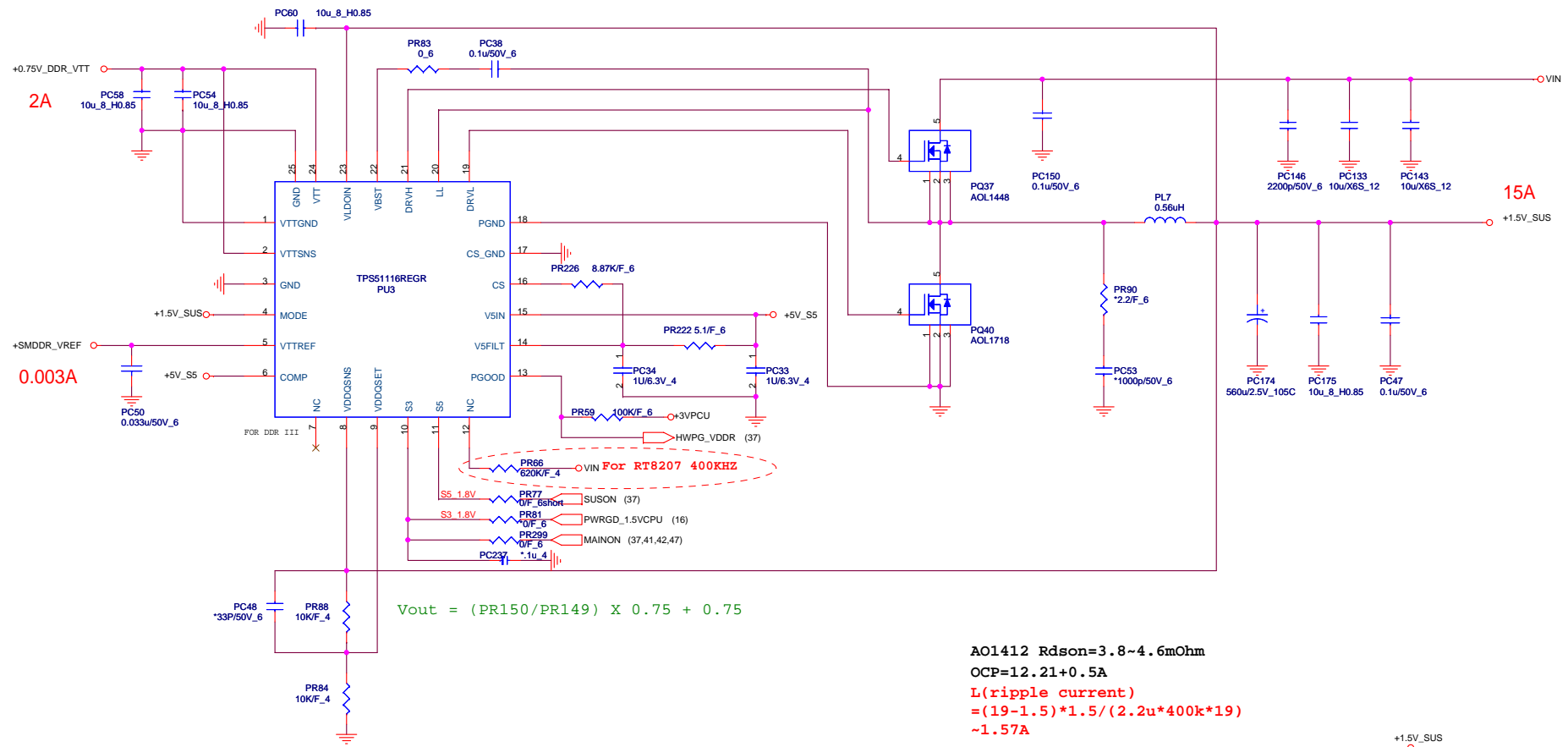


AO4710 $R_{dson}=11.8\sim 14.2m\Omega$
 OCP=7.2-0.8A
 L(ripple current)
 $= (19-1.05) * 1.05 / (2.2u * 272k * 19)$
 $\sim 1.6577A$
 $14.2m * 7 = RILIM * 20uA$
 $RILIM = 4.99K (4.97K)$

$V_{OUT} = (1 + R1/R2) * 0.75$

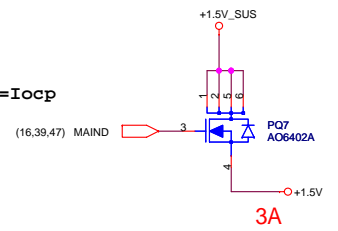
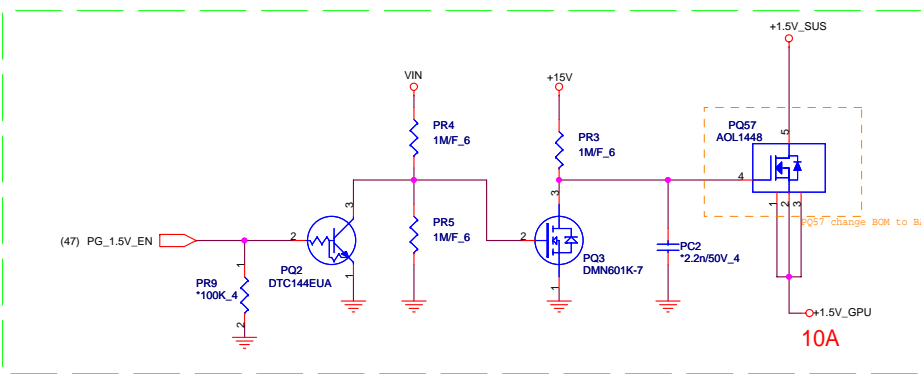


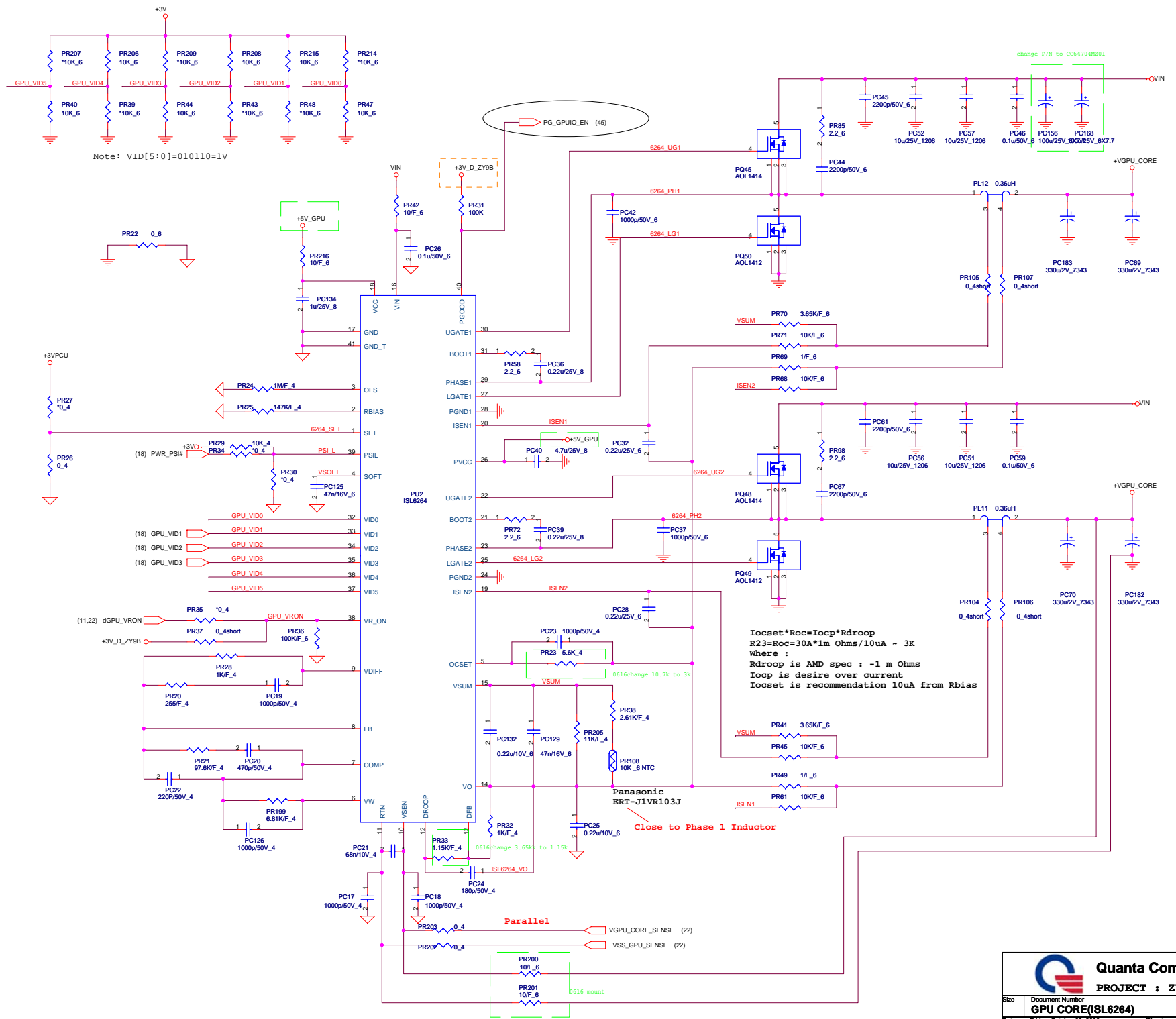
 Quanta Computer Inc. PROJECT : ZY9B		Size	Document Number	Rev
			+1.05V(UP6111AQDD)	1A
Date:	Monday, September 21, 2009	Sheet	42	of 49

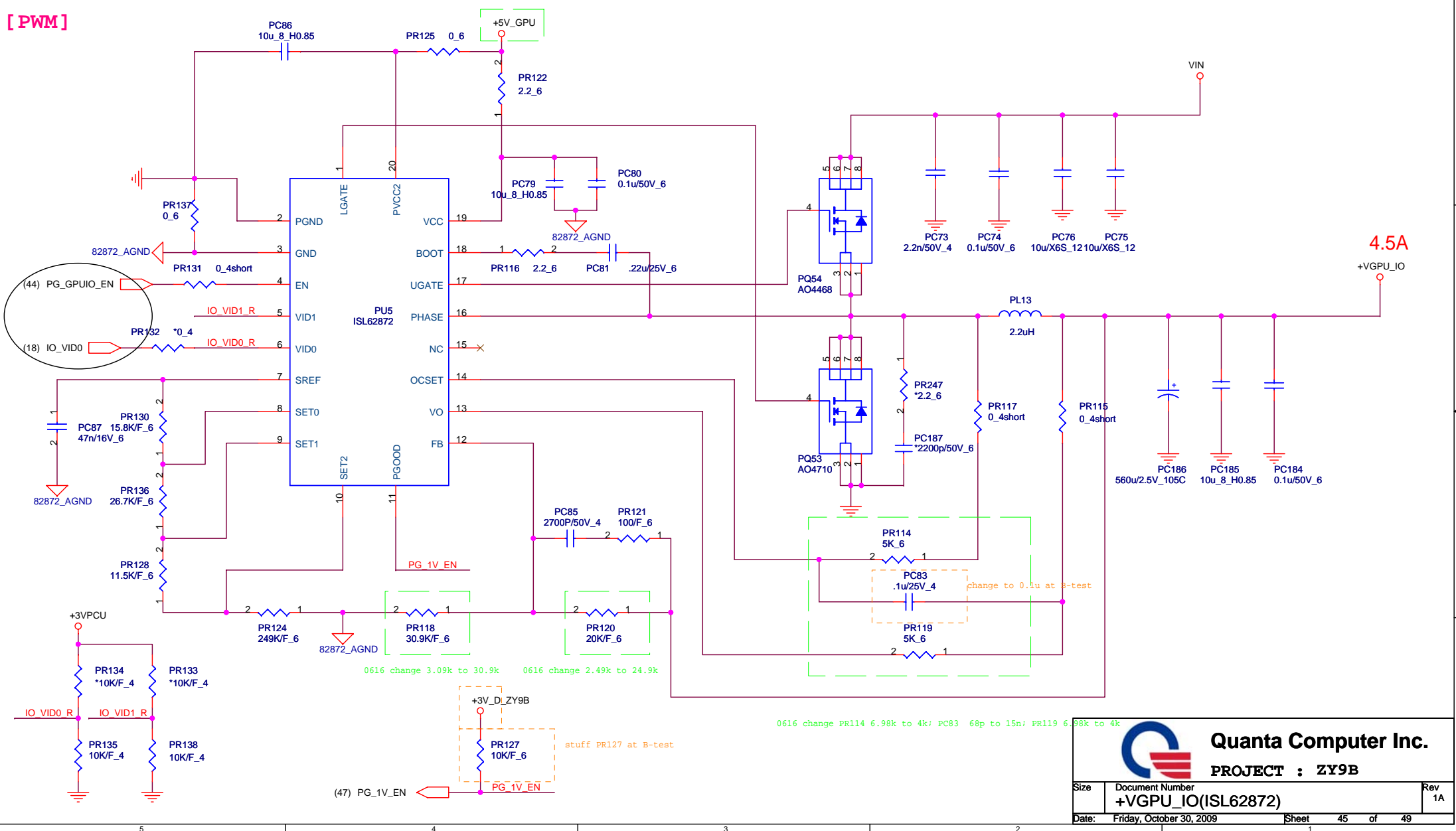


$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

AO1412 $R_{dson}=3.8\sim 4.6m\Omega$
 $OCP=12.21+0.5A$
L(ripple current)
 $= (19-1.5) \times 1.5 / (2.2\mu \times 400k \times 19)$
 $\sim 1.57A$
 $4.6m \times 19 = RILIM \times 10\mu A$
RILIM=8.74K --- 8.87K
 $(10\mu \times PR35) / R_{dson} + \Delta I / 2 = I_{ocp}$







0616 change 3.09k to 30.9k 0616 change 2.49k to 24.9k

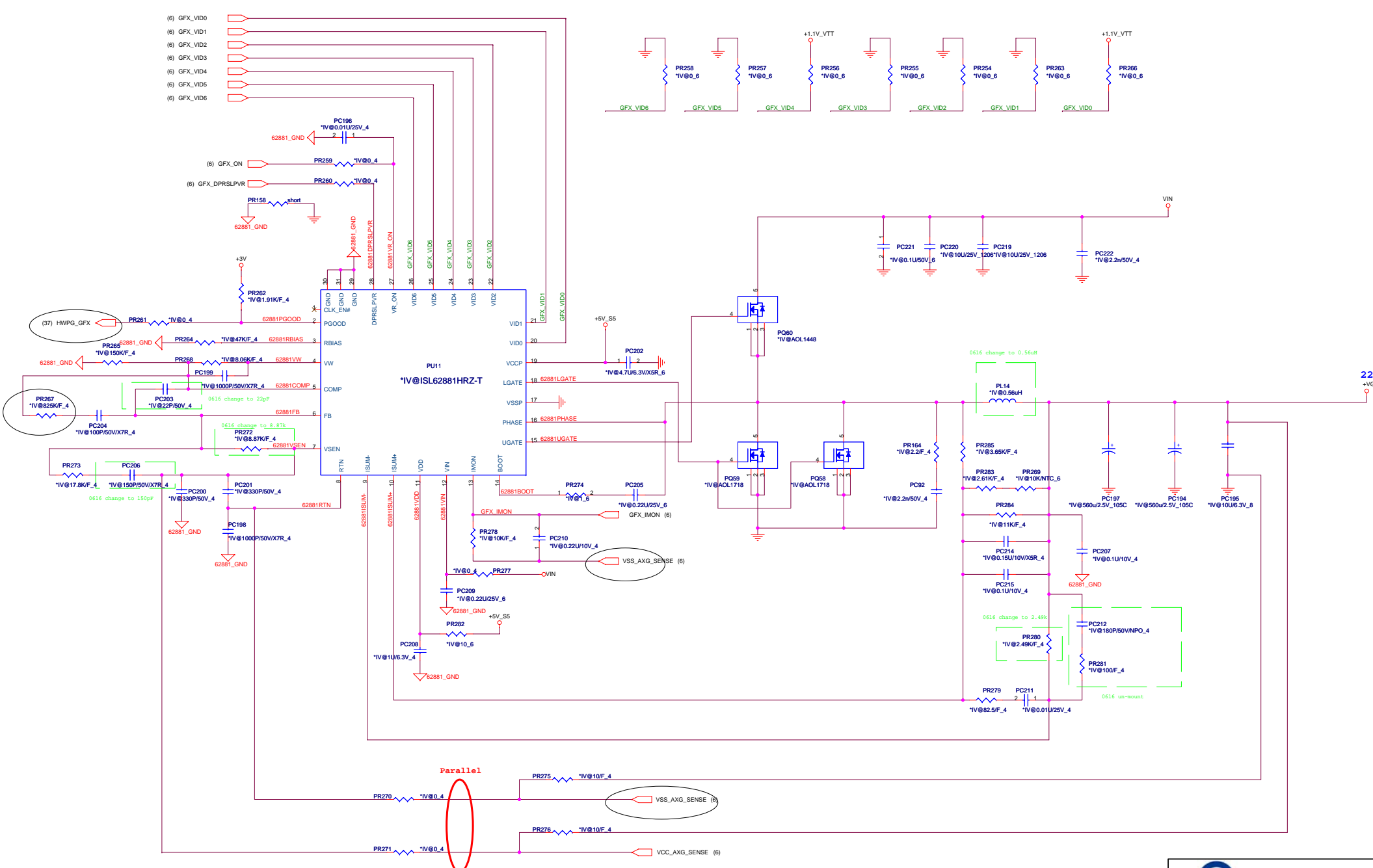
0616 change PR114 6.98k to 4k; PC83 68p to 15n; PR119 6.98k to 4k

stuff PR127 at B-test

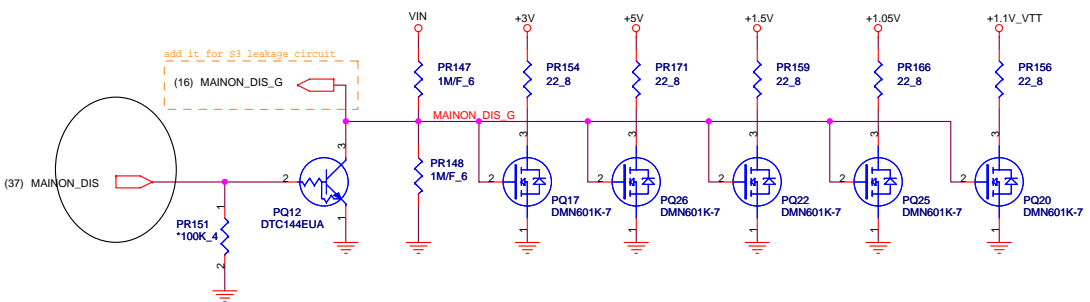
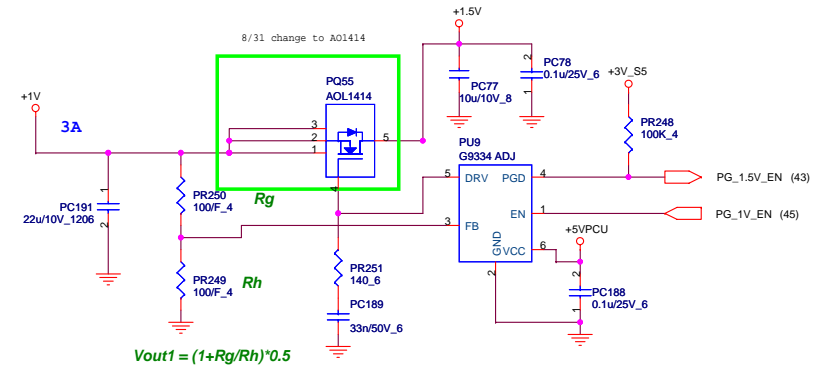
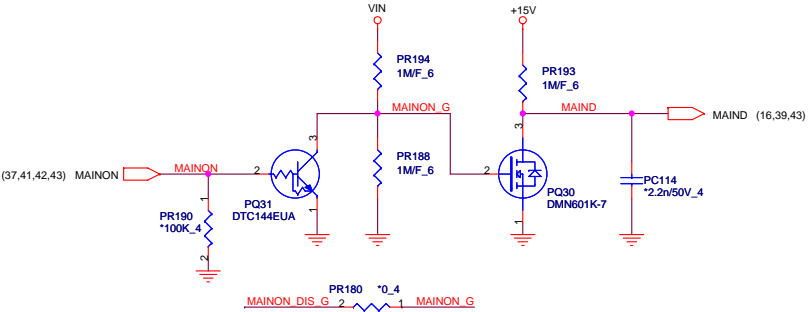
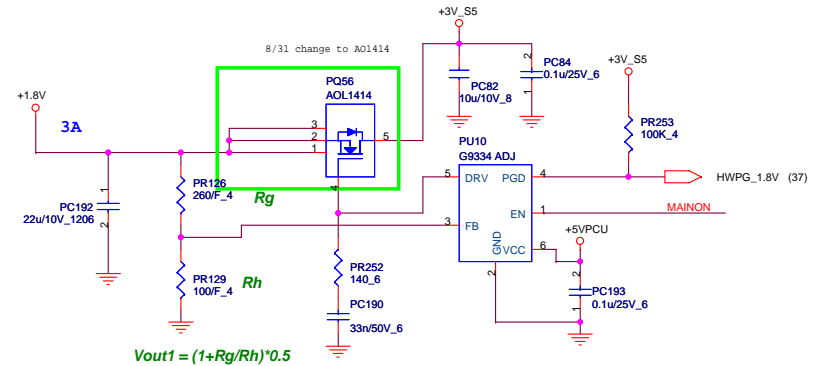
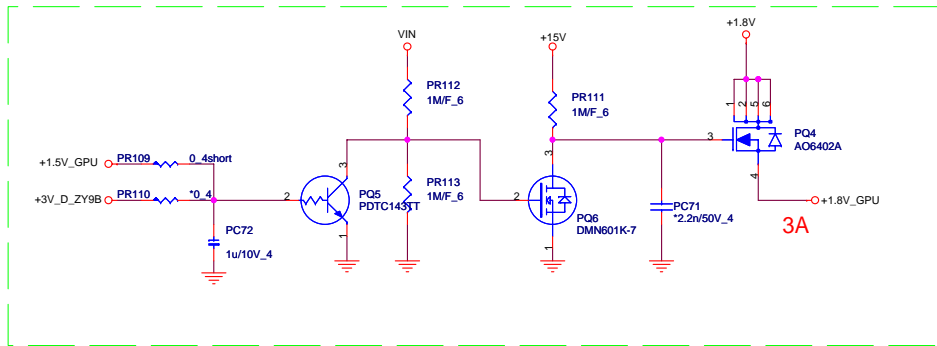
change to 0.1u at B-test

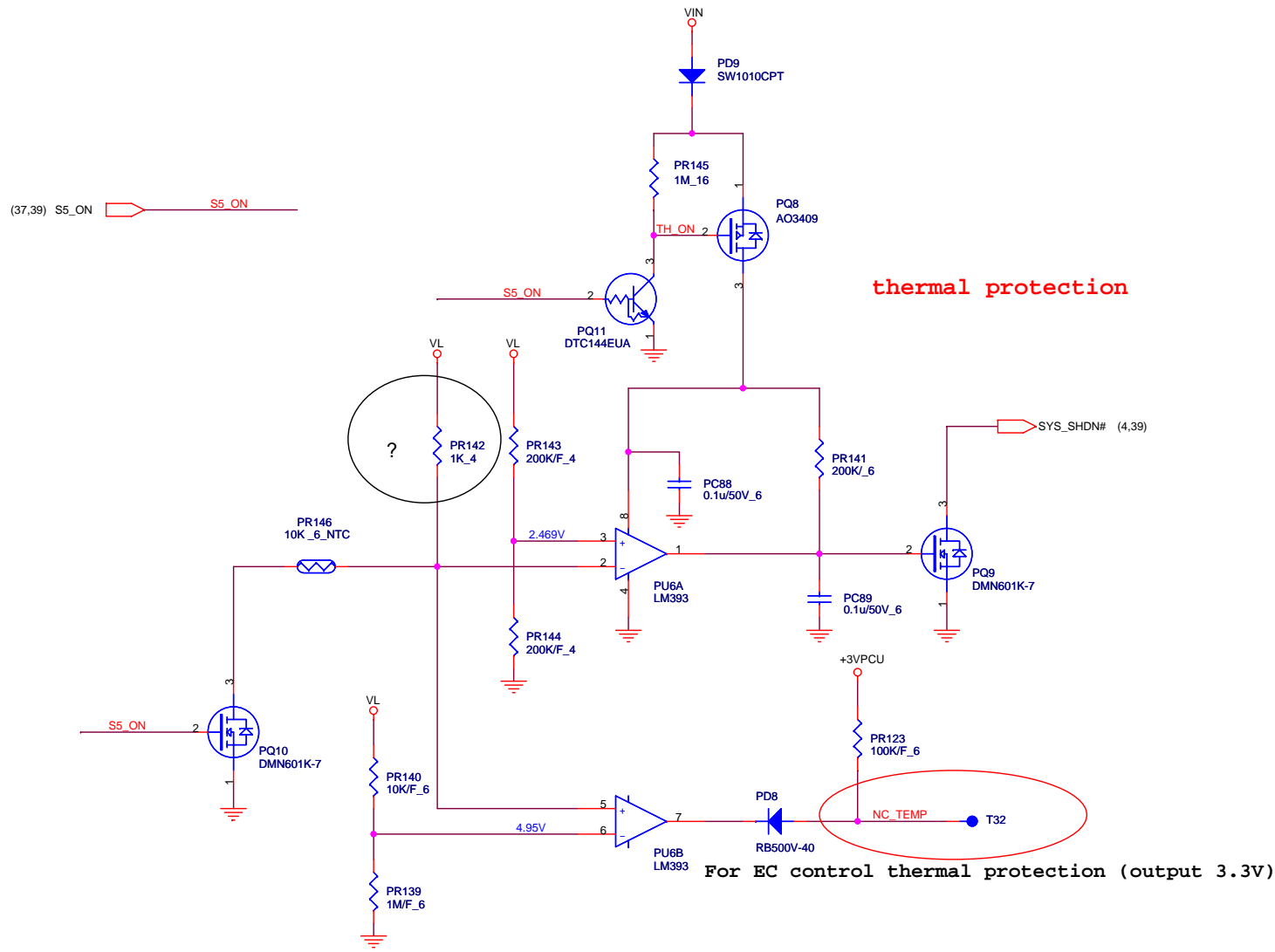
Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	+VGPU_IO(ISL62872)	1A




Quanta Computer Inc.
PROJECT : ZY9B
 Size Document Number
+V_GFX_AXG (ISL62881)
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thermal protection

For EC control thermal protection (output 3.3V)

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		1A
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Thermal Protection		
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