LM301A, LM201A, LM201AV

Non Compensated Single Operational Amplifiers

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to 10 V/μs can be obtained.

Features

- Low Input Offset Current: 20 nA Maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short Circuit Protection
- Guaranteed Drift Characteristics
- Pb−Free Packages are Available

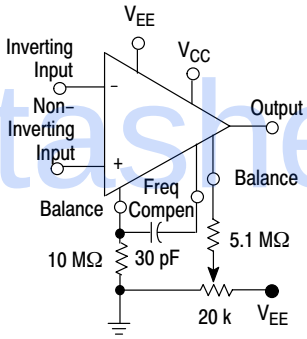
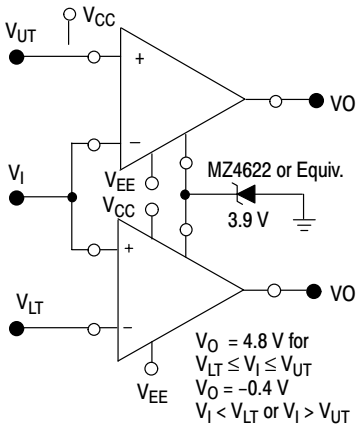


Figure 1. Standard Compensation and Offset Balancing Circuit



(Pins Not Shown Are Not Connected)

Figure 2. Double−Ended Limit Detector

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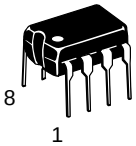
http://onsemi.com

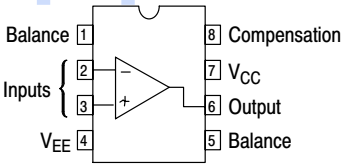


PDIP−8
N SUFFIX
CASE 626

SOIC−8
D SUFFIX
CASE 751

Datasheet.Support

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 3 of this data sheet.

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May, 2004 − Rev. 9

Publication Order Number:
LM301A/D

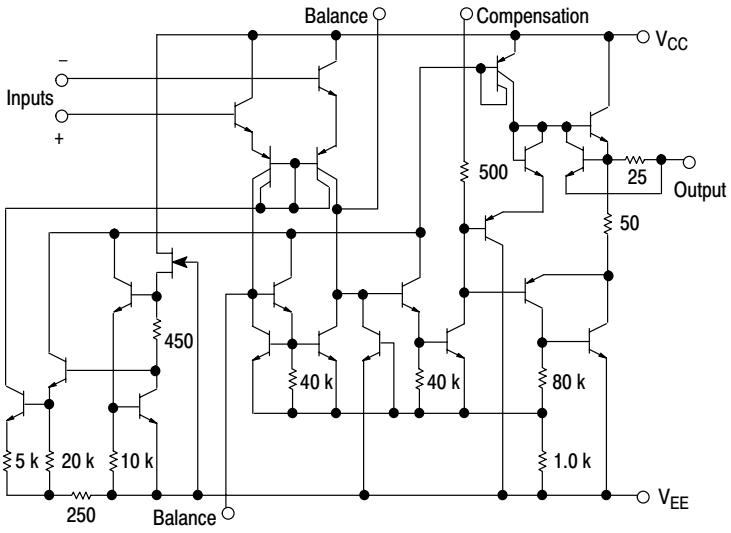


Figure 3. Representative Circuit Schematic

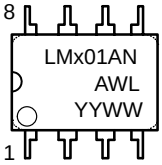
ORDERING INFORMATION

Device	Package	Shipping†
LM301AD	SOIC−8	98 Units/Rail
LM301ADG	SOIC−8 (Pb−Free)	
LM301ADR2	SOIC−8	2500 Tape & Reel
LM301ADR2G	SOIC−8 (Pb−Free)	
LM301AN	PDIP−8	50 Units/Rail
LM201AD	SOIC−8	98 Units/Rail
LM201ADR2	SOIC−8	2500 Tape & Reel
LM201AN	PDIP−8	50 Units/Rail
LM201AVDR2	SOIC−8	2500 Tape & Reel

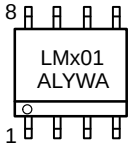
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

PDIP−8
N SUFFIX
CASE 626



SOIC−8
D SUFFIX
CASE 751



x	= 2 or 3
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

MAXIMUM RATINGS

Rating	Symbol	Value			Unit
		LM201A	LM201AV	LM301A	
Power Supply Voltage	V_{CC}, V_{EE}	±22	±22	±18	Vdc
Input Differential Voltage	V_{ID}	±30			V
Input Common Mode Range (Note 1)	V_{ICR}	±15			V
Output Short Circuit Duration	t_{SC}	Continuous			
Power Dissipation (Package Limitation)	P_D				
Plastic Dual−In−Line Package		625	625	625	mW
Derate above T_A = +25°C		5.0	5.0	5.0	mW/°C
Operating Ambient Temperature Range	T_A	−25 to +85	−40 to +105	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150			°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the LM201A and LM201AV, and from ±5.0 V to ±15 V for the LM301A.

Characteristic	Symbol	LM201A / LM201AV			LM301A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 50$ kΩ)	V_{IO}	−	0.7	2.0	−	2.0	7.5	mV
Input Offset Current	I_{IO}	−	1.5	10	−	3.0	50	nA
Input Bias Current	I_{IB}	−	30	75	−	70	250	nA
Input Resistance	r_i	1.5	4.0	−	0.5	2.0	−	MΩ
Supply Current V_{CC}/V_{EE} = ±20 V V_{CC}/V_{EE} = ±15 V	I_{CC}, I_{EE}	 − −	 1.8 −	 3.0 −	 − −	 − 1.8	 − 3.0	mA
Large Signal Voltage Gain (V_{CC}/V_{EE} = ±15 V, V_O = ±10 V, R_L > 2.0 kΩ)	A_V	50	160	−	25	160	−	V/mV
The following specifications apply over the operating temperature range.								
Input Offset Voltage ($R_S \le 50$ kΩ)	V_{IO}	−	−	3.0	−	−	10	mV
Input Offset Current	I_{IO}	−	−	20	−	−	70	nA
Avg Temperature Coefficient of Input Offset Voltage (Note 2) $T_A(min) \le T_A \le T_A$ (max)	$\Delta V_{IO}/\Delta T$	−	3.0	15	−	6.0	30	μV/°C
Avg Temperature Coefficient of Input Offset Current (Note 2) +25°C ≤ $T_A \le T_A$ (max) $T_A(min) \le T_A \le$ 25°C	$\Delta I_{IO}/\Delta T$	 − −	 0.01 0.02	 0.1 0.2	 − −	 0.01 0.02	 0.3 0.6	nA/°C
Input Bias Current	I_{IB}	−	−	100	−	−	300	nA
Large Signal Voltage Gain (V_{CC}/V_{EE} = ±15 V, V_O = ±10V, R_L > 2.0 kΩ)	A_{VOL}	25	−	−	15	−	−	V/mV
Input Voltage Range V_{CC}/V_{EE} = ±20 V V_{CC}/V_{EE} = ±15 V	V_{ICR}	 −15 −	 − −	 +15 −	 − −12	 − −	 − +12	V
Common Mode Rejection ($R_S \le 50$ kΩ)	CMR	80	96	−	70	90	−	dB
Supply Voltage Rejection ($R_S \le 50$ kΩ)	PSR	80	96	−	70	96	−	dB
Output Voltage Swing (V_{CC}/V_{EE} = ±15 V, R_L = ±10 kΩ, R_L > 2.0 kΩ)	V_O	±12 ±10	±14 ±13	− −	±12 ±10	±14 ±13	− −	V
Supply Currents ($T_A = T_A$(max), V_{CC}/V_{EE} = ±20 V)	I_{CC}, I_{EE}	−	1.2	2.5	−	−	−	mA

1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Guaranteed by design.

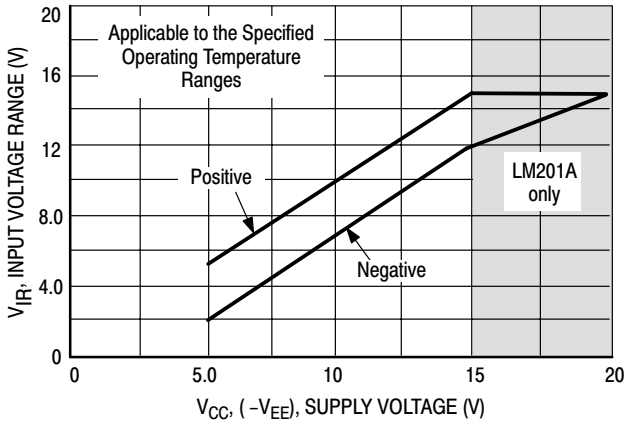


Figure 4. Minimum Input Voltage Range

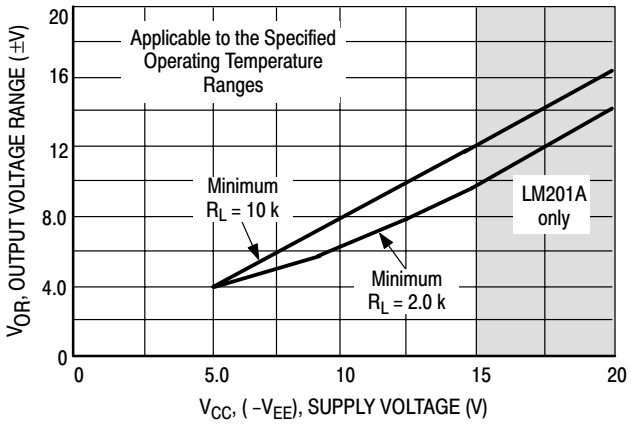


Figure 5. Minimum Output Voltage Swing

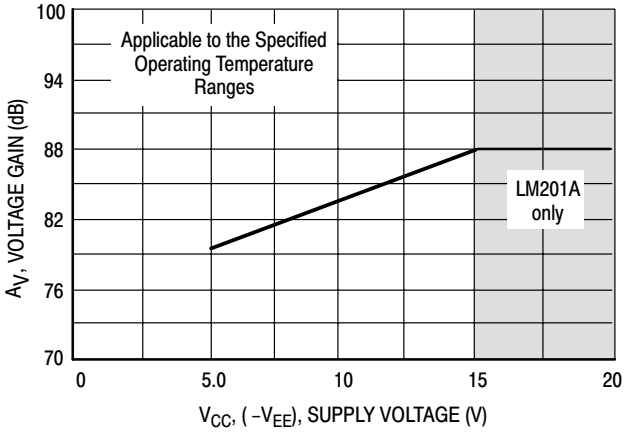


Figure 6. Minimum Voltage Gain

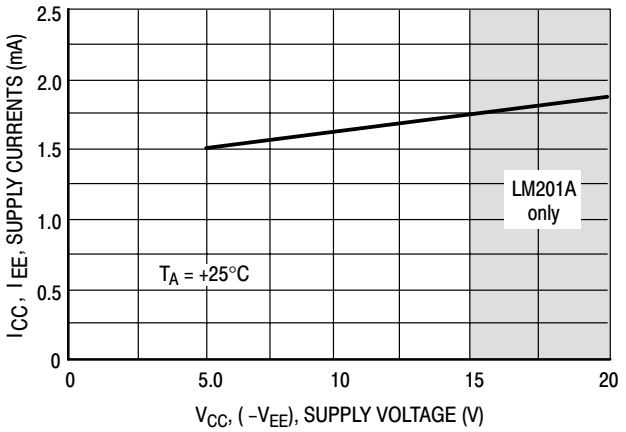


Figure 7. Typical Supply Currents

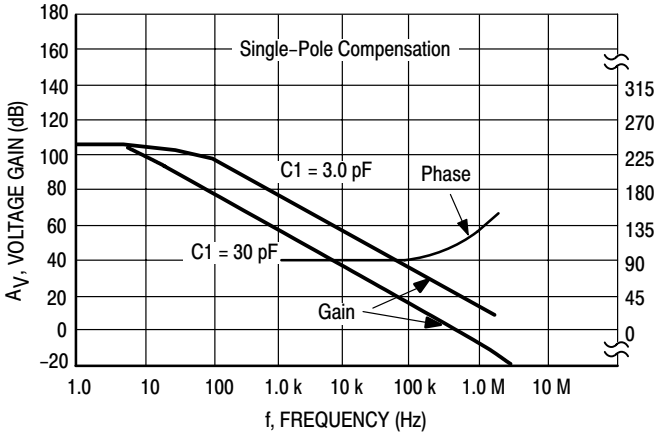


Figure 8. Open Loop Frequency Response

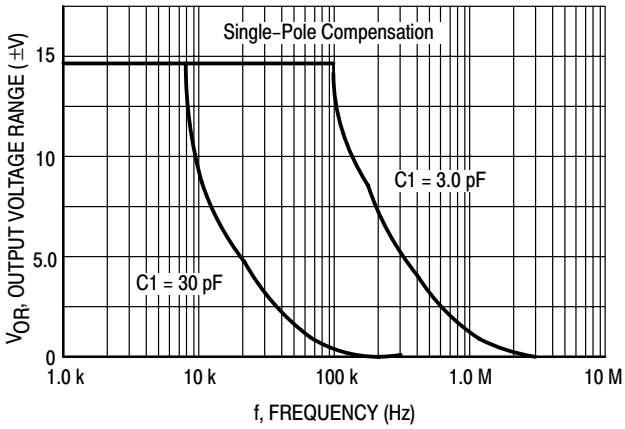


Figure 9. Large Signal Frequency Response

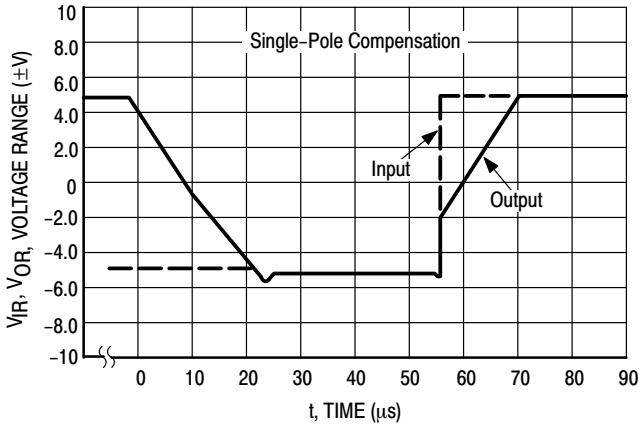


Figure 10. Voltage Follower Pulse Response

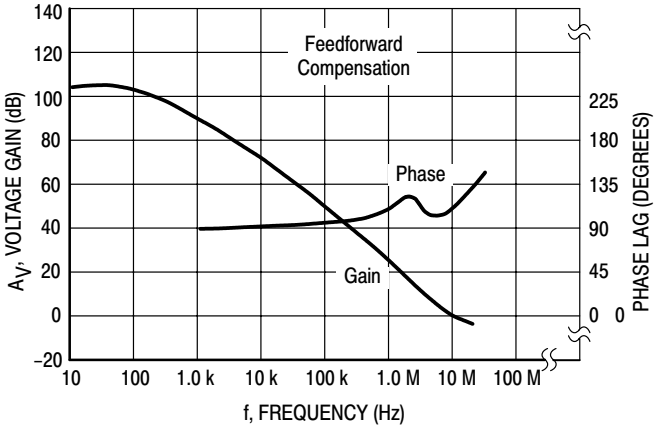


Figure 11. Open Loop Frequency Response

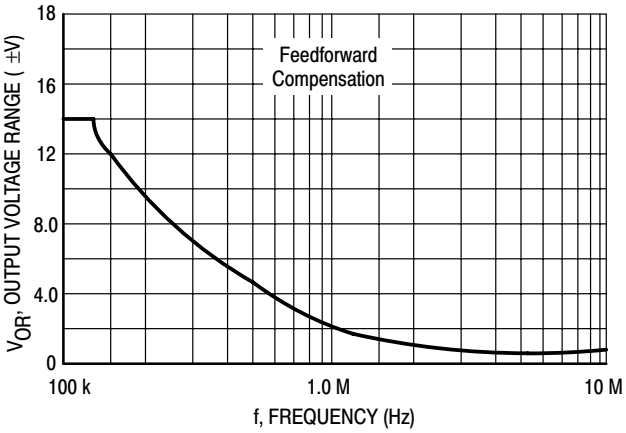


Figure 12. Large Signal Frequency Response

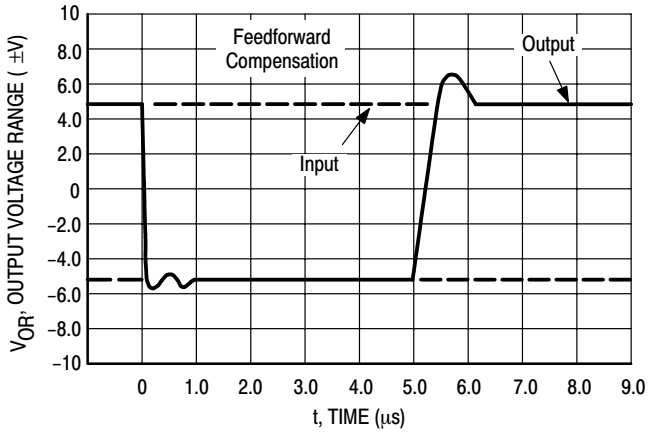


Figure 13. Inverter Pulse Response

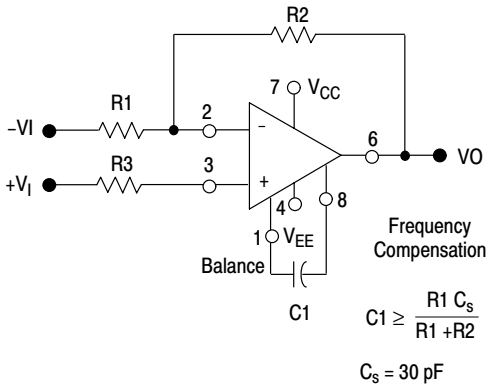


Figure 14. Single−Pole Compensation

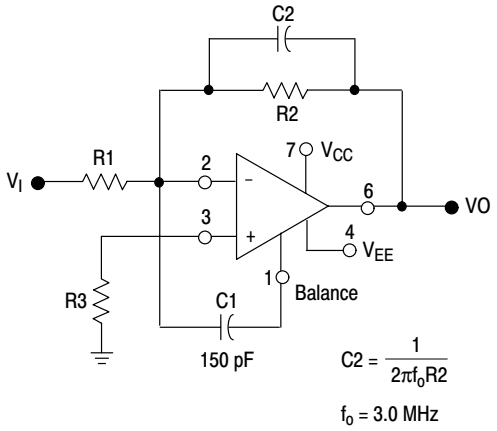
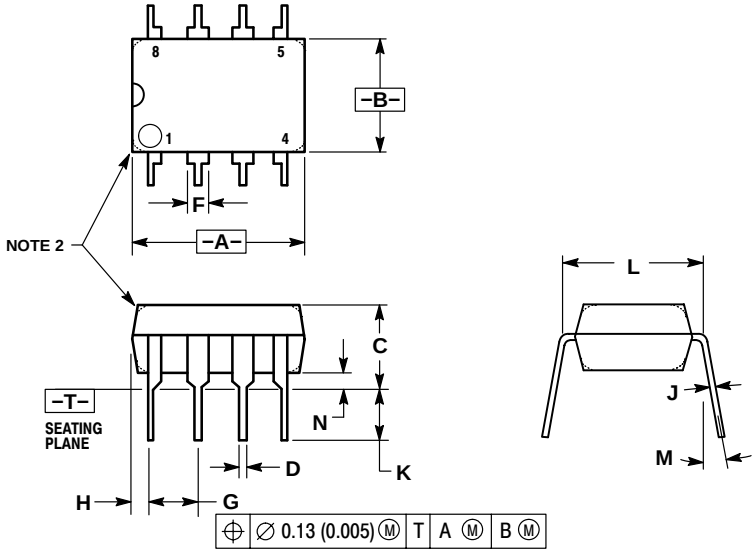


Figure 15. Feedforward Compensation

PACKAGE DIMENSIONS

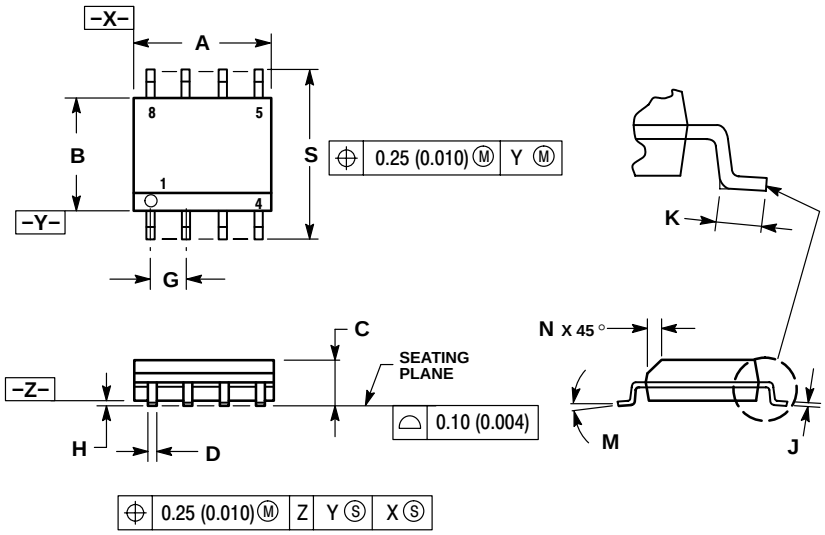
PDIP−8
N SUFFIX
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	−−−	10°	−−−	10°
N	0.76	1.01	0.030	0.040

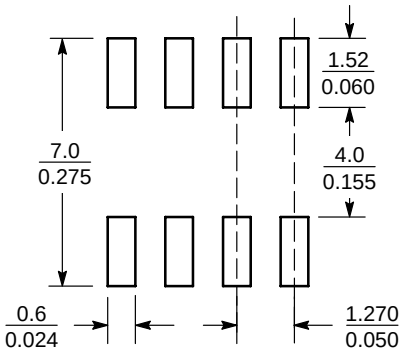
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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