

## PowerMOS transistor

## BUK455-200A/B

## GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.  
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

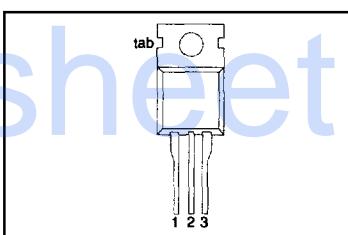
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	BUK455	MAX.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-200A	-200B		V
$I_D$	Drain current (DC)	200	200		A
$P_{tot}$	Total power dissipation	14	13		W
$T_j$	Junction temperature	125	125		°C
$R_{DS(ON)}$	Drain-source on-state resistance	175	175		
		0.23	0.28		Ω

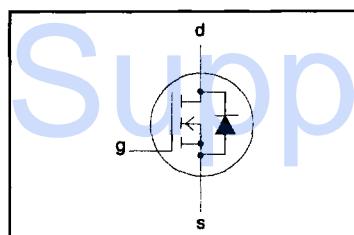
## PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

## PIN CONFIGURATION



## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
$V_{DS}$	Drain-source voltage	-		200		V
	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	200		V
	$\pm V_{GS}$	-	-	30		V
$I_D$	Drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	-200A	-200B	A
	Drain current (DC)	$T_{mb} = 100 \text{ }^\circ\text{C}$	-	14	13	A
	Drain current (pulse peak value)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	10	9	A
$I_{DM}$	Drain current (DC)	$T_{mb} = 56 \text{ }^\circ\text{C}$	-	56	52	A
	Total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-		125	W
	Storage temperature	-	-55		175	°C
$P_{tot}$	Junction Temperature	-	-		175	°C
	$T_{stg}$	-	-			
$T_j$		-	-			

## THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th(j-mb)}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th(j-a)}$	Thermal resistance junction to ambient		-	60	-	K/W

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**STATIC CHARACTERISTICS** $T_{mb} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.25 \text{ mA}$	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1 \text{ mA}$	2.1	3.0	4.0	V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 200 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25^\circ\text{C}$	-	1	10	$\mu\text{A}$
$I_{DS}$	Zero gate voltage drain current	$V_{DS} = 200 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125^\circ\text{C}$	-	0.1	1.0	mA
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 30 \text{ V}; V_{DS} = 0 \text{ V}$	-	10	100	nA
$R_{DS(on)}$	Drain-source on-state resistance	$V_{GS} = 10 \text{ V}; BUK455-200A$ $I_D = 7 \text{ A} \quad BUK455-200B$	-	0.2	0.23	$\Omega$
			-	0.22	0.28	$\Omega$

**DYNAMIC CHARACTERISTICS** $T_{mb} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$g_{fs}$	Forward transconductance	$V_{DS} = 25 \text{ V}; I_D = 7 \text{ A}$	6	8.4	-	S
$C_{iss}$	Input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}$	-	1400	1750	pF
$C_{oss}$	Output capacitance		-	190	250	pF
$C_{rss}$	Feedback capacitance		-	55	80	pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}$	-	18	30	ns
$t_r$	Turn-on rise time	$V_{GS} = 10 \text{ V}; R_{GS} = 50 \Omega$	-	35	60	ns
$t_{d(off)}$	Turn-off delay time		-	85	120	ns
$t_f$	Turn-off fall time	$R_{gen} = 50 \Omega$	-	35	50	ns
$L_d$	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
$L_d$	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
$L_s$	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS** $T_{mb} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current	-	-	-	14	A
$I_{DRM}$	Pulsed reverse drain current	-	-	-	56	A
$V_{SD}$	Diode forward voltage	$I_F = 14 \text{ A}; V_{GS} = 0 \text{ V}$	-	1.0	1.5	V
$t_{rr}$	Reverse recovery time	$I_F = 14 \text{ A}; -dI_F/dt = 100 \text{ A}/\mu\text{s}$	-	180	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{GS} = 0 \text{ V}; V_R = 30 \text{ V}$	-	1.8	-	$\mu\text{C}$

**AVALANCHE LIMITING VALUE** $T_{mb} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 14 \text{ A}; V_{DD} \leq 100 \text{ V}; V_{GS} = 10 \text{ V}; R_{GS} = 50 \Omega$	-	-	100	mJ

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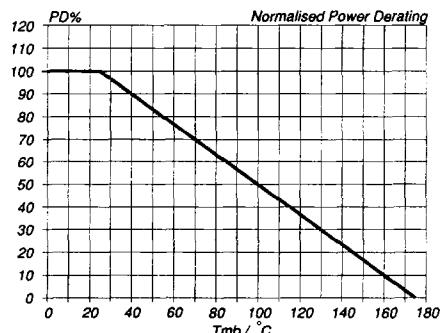


Fig.1. Normalised power dissipation.  
 $PD\% = 100 \cdot P_D / P_{D25\text{ °C}} = f(T_{mb})$

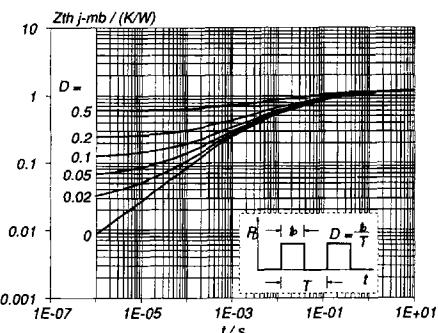


Fig.4. Transient thermal impedance.  
 $Z_{th,j-mb} = f(t); \text{parameter } D = t_p/T$

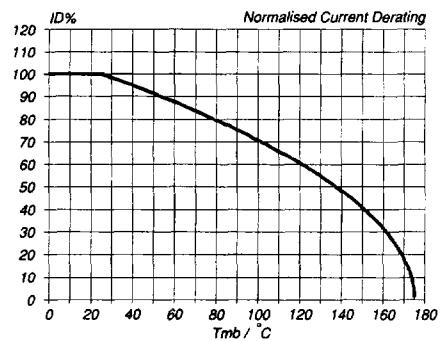


Fig.2. Normalised continuous drain current.  
 $ID\% = 100 \cdot I_D / I_{D25\text{ °C}} = f(T_{mb}); \text{conditions: } V_{GS} \geq 10 \text{ V}$

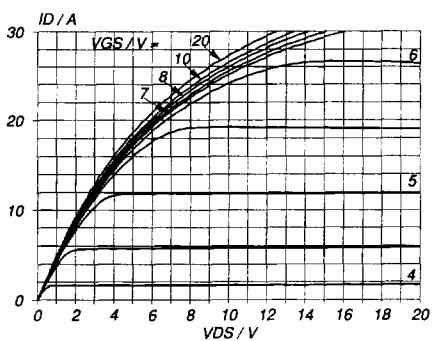


Fig.5. Typical output characteristics,  $T_j = 25 \text{ °C}$ .  
 $I_D = f(V_{DS}); \text{parameter } V_{GS}$

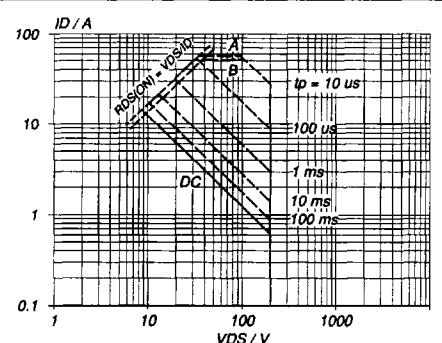


Fig.3. Safe operating area.  $T_{mb} = 25 \text{ °C}$   
 $I_D \text{ & } I_{DM} = f(V_{DS}); I_{DM} \text{ single pulse; parameter } t_p$

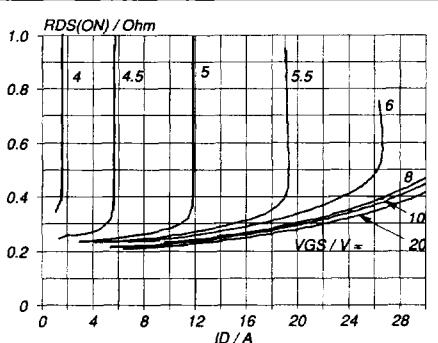


Fig.6. Typical on-state resistance,  $T_j = 25 \text{ °C}$ .  
 $R_{DS(ON)} = f(I_D); \text{parameter } V_{GS}$

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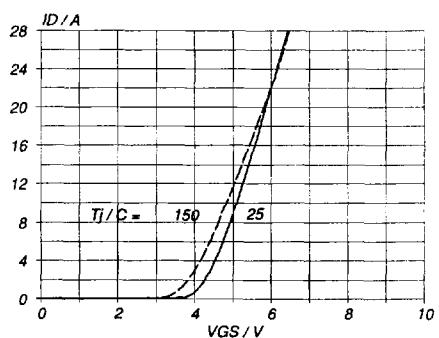


Fig.7. Typical transfer characteristics.  
 $I_D = f(V_{GS})$ ; conditions:  $V_{DS} = 25$  V; parameter  $T_j$

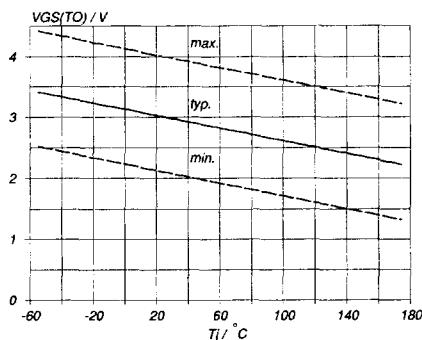


Fig.10. Gate threshold voltage.  
 $V_{GS(TO)} = f(T_j)$ ; conditions:  $I_D = 1$  mA;  $V_{DS} = V_{GS}$

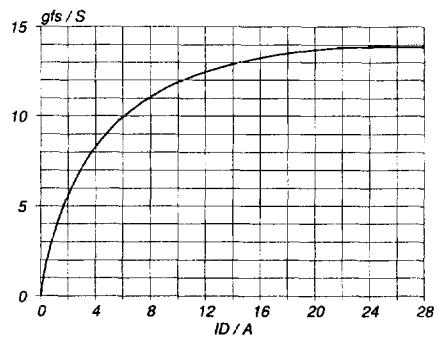


Fig.8. Typical transconductance,  $T_j = 25$  °C.  
 $g_{ts} = f(I_D)$ ; conditions:  $V_{DS} = 25$  V

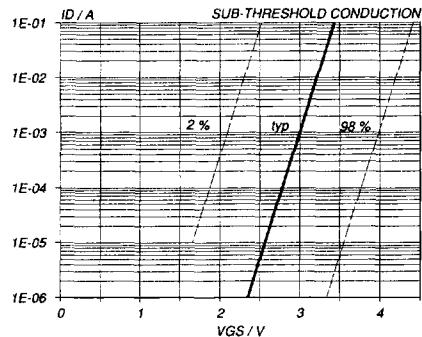


Fig.11. Sub-threshold drain current.  
 $I_D = f(V_{GS})$ ; conditions:  $T_j = 25$  °C;  $V_{DS} = V_{GS}$

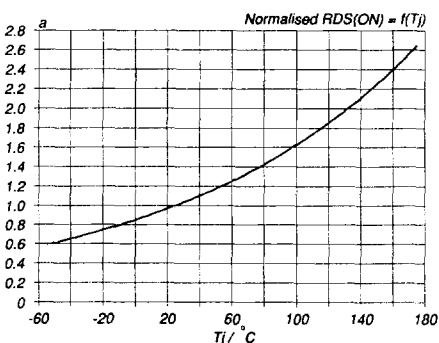


Fig.9. Normalised drain-source on-state resistance.  
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ C} = f(T_j)$ ;  $I_D = 7$  A;  $V_{GS} = 10$  V

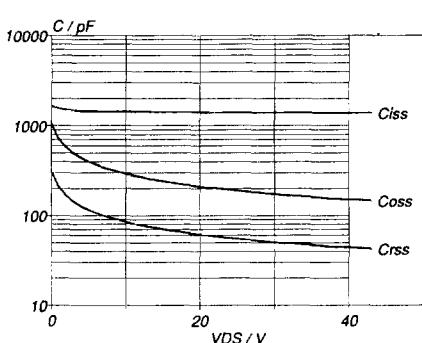


Fig.12. Typical capacitances,  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$ .  
 $C = f(V_{DS})$ ; conditions:  $V_{GS} = 0$  V;  $f = 1$  MHz

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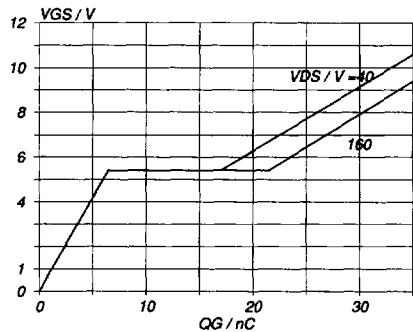


Fig.13. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$ ; conditions:  $I_D = 14 \text{ A}$ ; parameter  $V_{DS}$

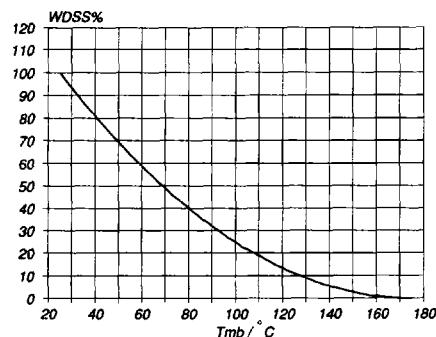


Fig.15. Normalised avalanche energy rating.  
 $W_{DSS\%} = f(T_{mb})$ ; conditions:  $I_D = 14 \text{ A}$

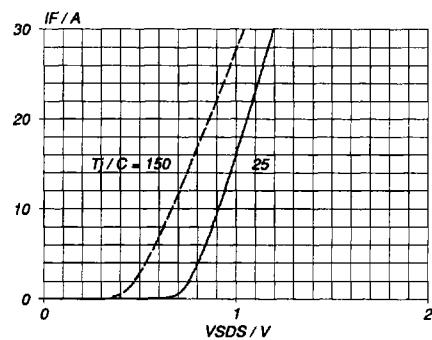


Fig.14. Typical reverse diode current.  
 $I_F = f(V_{DS})$ ; conditions:  $V_{GS} = 0 \text{ V}$ ; parameter  $T_j$

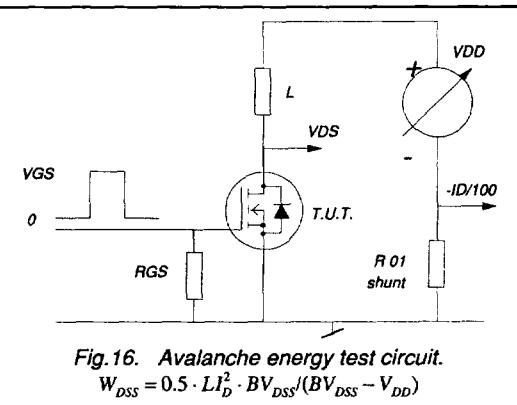


Fig.16. Avalanche energy test circuit.  
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$