HARRIS

IRF9530, IRF9531 IRF9532, IRF9533

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -10A and -12A, -80V and -100V
- $r_{DS(ON)}$ = 0.3Ω and 0.4Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

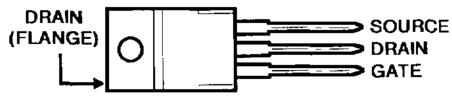
Description

The IRF9530, IRF9531, IRF9532 and IRF9533 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

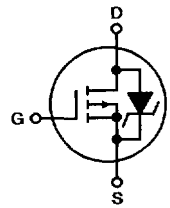
Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9530	IRF9531	IRF9532	IRF9533	UNITS
Drain-Source Voltage (1) .... V_{DS}	-100	-80	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) .... V_{DGR}	-100	-80	-100	-80	V
Continuous Drain Current					
T_C = 25°C .... I_D	-12	-12	-10	-10	A
T_C = 100°C .... I_D	-7.5	-7.5	-6.5	-6.5	A
Pulsed Drain Current (3) .... I_{DM}	-48	-48	-40	-40	A
Gate-Source Voltage .... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation .... P_D (See Figure 14)	75	75	75	75	W
Linear Derating Factor .... (See Figure 14)	0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4) .... E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range .... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering .... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

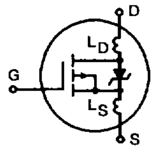
NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 5.2mHμ, R_G = 25Ω, Peak I_L = 12A (See Figures 15 and 16)

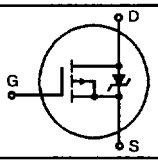
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2221.1**

Electrical Characteristics T_C = +25^oC, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage IRF9530, IRF9532	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9531, IRF9533			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125^oC	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9530, IRF9531	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-12	-	-	A
IRF9532, IRF9533			-10	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9530, IRF9531	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -6.5A	-	0.25	0.3	Ω
IRF9532, IRF9533			-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 6.5A	2.0	3.8	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	500	-	pF
Output Capacitance	C_{OSS}		-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -12A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	60	ns
Rise Time	t_r		-	70	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	140	ns
Fall Time	t_f		-	70	140	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -12A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	25	45	nC
Gate-Source Charge	Q_{gs}		-	13	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. / Modified MOSFET symbol showing the internal device inductances. 	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	$^oC/W$
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	$^oC/W$
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	$^oC/W$

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-12	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-48	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25^oC, I_S = -12A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150^oC, I_F = -12A, dI_F/dt = 100A/μs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150^oC, I_F = -12A, dI_F/dt = 100A/μs	-	1.8	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25^oC to +150^oC
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25^oC, L = 5.2mH, R_G = 25Ω, Peak I_L = 12A (See Figures 15 and 16)

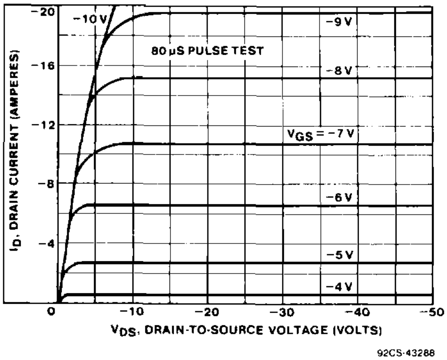


Fig. 1 - Typical Output Characteristics

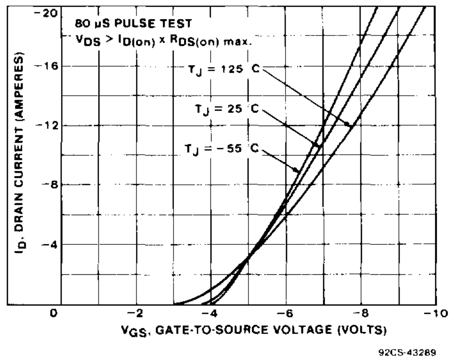


Fig. 2 - Typical Transfer Characteristics

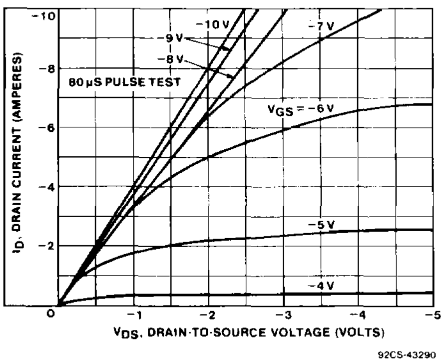


Fig. 3 - Typical saturation characteristic.

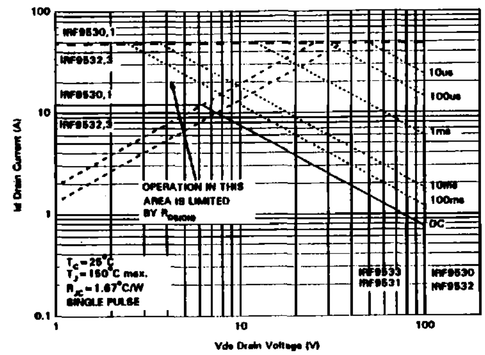


Fig. 4 - Maximum safe operating area.

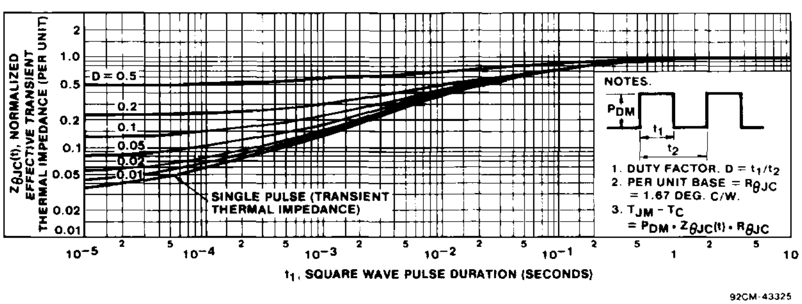


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

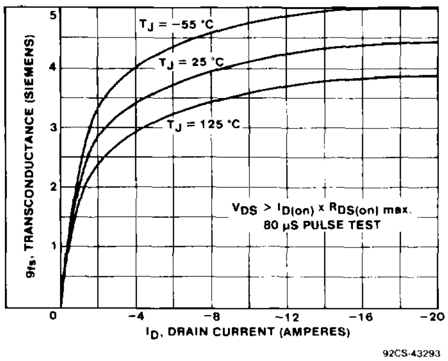


Fig. 6 - Typical transconductance vs. drain current.

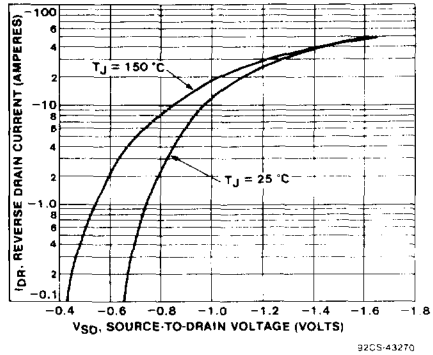


Fig. 7 - Typical source-drain diode forward voltage.

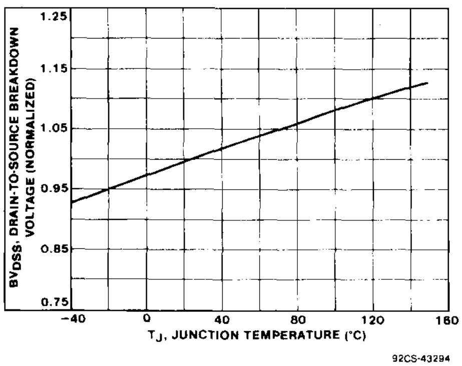


Fig. 8 - Breakdown voltage vs. temperature.

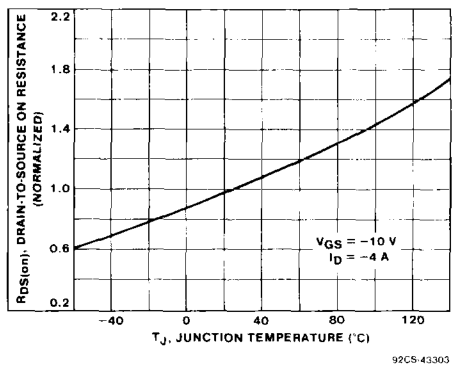


Fig. 9 - Normalized on-resistance vs. temperature.

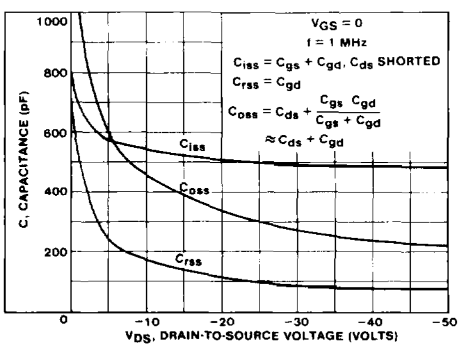


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

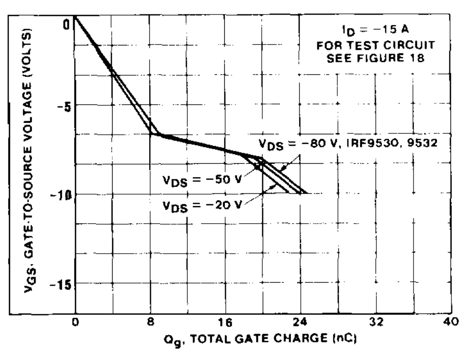


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

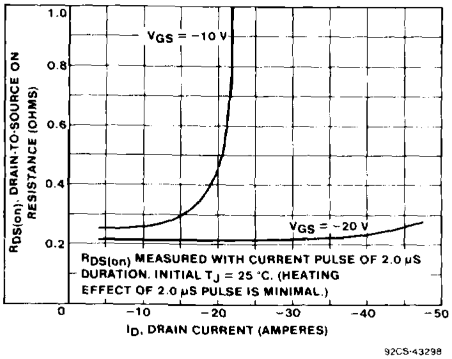


Fig. 12 - Typical on-resistance vs. drain current.

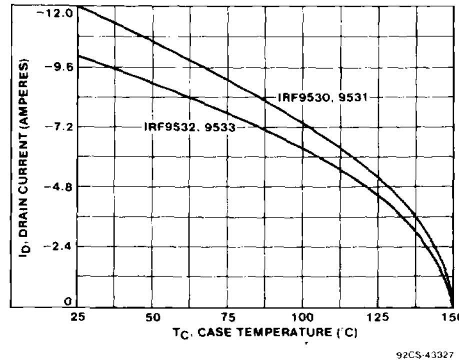


Fig. 13 - Maximum drain current vs. case temperature.

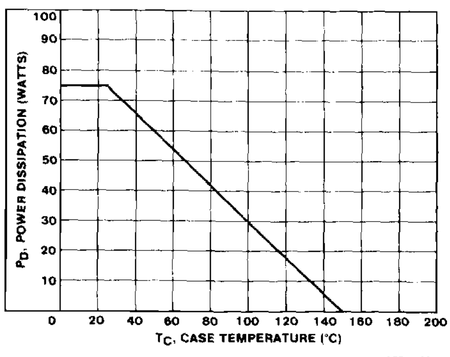


Fig. 14 - Power vs. temperature derating curve.

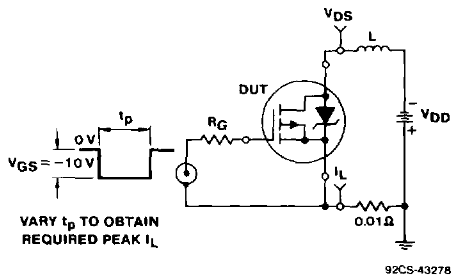


Fig. 15 - Unclamped inductive test circuit.

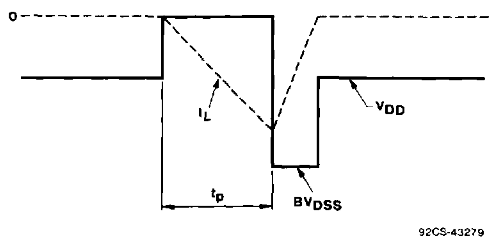


Fig. 16 - Unclamped inductive waveforms.

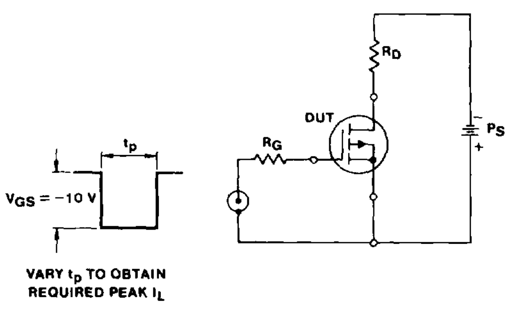


Fig. 17 - Switching time test circuit.

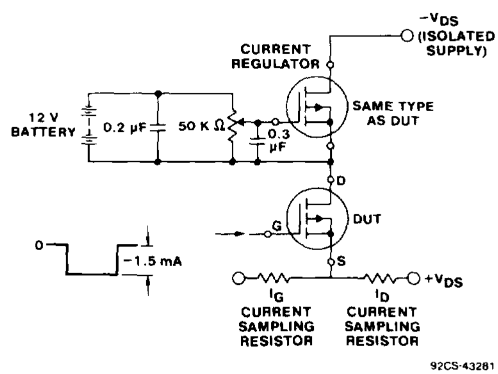


Fig. 18 - Gate charge test circuit.