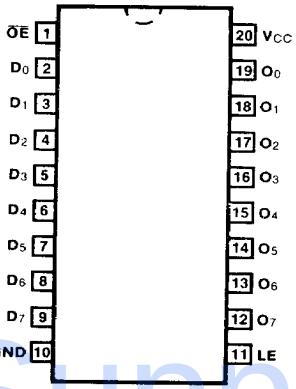
# 54LS/74LS573

## OCTAL D-TYPE LATCH

(With 3-State Outputs)

**CONNECTION DIAGRAM**
PINOUT A

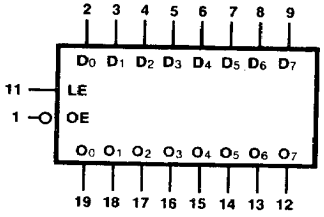



**DESCRIPTION** — The '573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally identical to the 'LS373, but has different pinouts. For truth tables, discussion of operations and ac and dc specifications, please refer to the 'LS373 data sheet.

- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 'LS373**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

**LOGIC SYMBOL**




VCC = Pin 20
Gnd = Pin 10

**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE<br>VCC = +5.0 V ±5%,<br>TA = 0°C to +70°C | MILITARY GRADE<br>VCC = +5.0 V ±10%,<br>TA = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 74LS573PC | | 9Z |
| Ceramic DIP (D) | A | 74LS573DC | 54LS573DM | 4E |
| Flatpak (F) | A | 74LS573FC | 54LS573FM | 4F |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 54/74LS (U.L.)<br>HIGH/LOW |
|---|---|---|
| D0 — D7 | Data Inputs | 0.5/0.25 |
| LE | Latch Enable Input (Active HIGH) | 0.5/0.25 |
| $\overline{OE}$ | 3-State Output Enable Input (Active LOW) | 0.5/0.25 |
| O0 — O7 | 3-State Latch Outputs | 65/15<br>(25)/(7.5) |