

# 2N7002



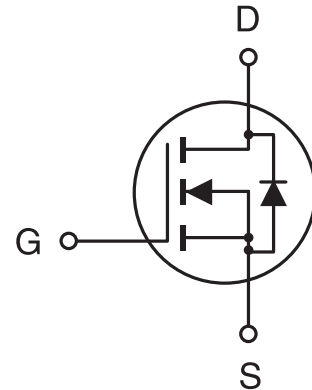
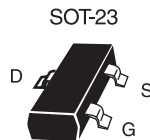
March 1998

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 60V , 0.115A ,  $R_{DS(ON)}=7.5\Omega$  @  $V_{GS}=10V$ .  
 $R_{DS(ON)}=7.5\Omega$  @  $V_{GS}=5V$ .
- High dense cell design for low  $R_{DS(ON)}$ .
- Rugged and reliable.
- SOT-23 package.

7



### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous <sup>a</sup> @ $T_J=125^\circ\text{C}$ -Pulsed <sup>b</sup>	$I_D$	115	mA
	$I_{DM}$	800	mA
Drain-Source Diode Forward Current <sup>a</sup>	$I_S$	115	mA
Maximum Power Dissipation <sup>a</sup>	$P_D$	200	mW
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	625	$^\circ\text{C/W}$
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# 2N7002

## ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =10μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
ON CHARACTERISTICS <sup>b</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1		2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =500mA			7.5	Ω
		V <sub>GS</sub> =5V, I <sub>D</sub> =50mA			7.5	Ω
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> =7V, V <sub>GS</sub> =10V	500			mA
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =7V, I <sub>D</sub> =200mA	80			mS
DYNAMIC CHARACTERISTICS <sup>c</sup>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		19	50	pF
Output Capacitance	C <sub>OSS</sub>			10	25	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			3	5	pF
SWITCHING CHARACTERISTICS <sup>c</sup>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =200mA, V <sub>GS</sub> =10V, R <sub>GEN</sub> =25Ω		23	30	ns
Rise Time	t <sub>r</sub>			15	20	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			75	100	ns
Fall Time	t <sub>f</sub>			15	20	ns

# 2N7002

## ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_S = 115mA$		0.76	1.5	V

### Notes

7

- a. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .
- b. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- c. Guaranteed by design, not subject to production testing.

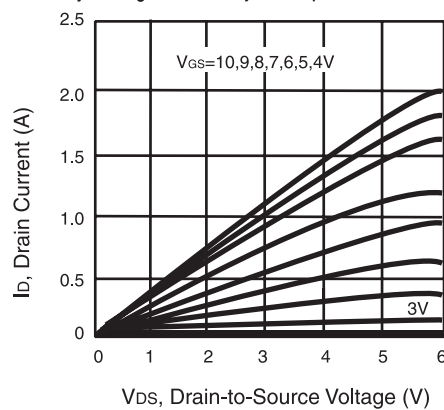


Figure 1. Output Characteristics

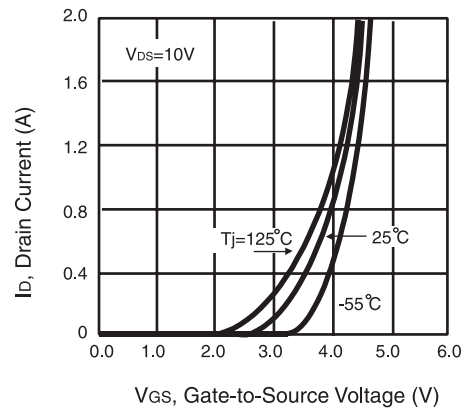


Figure 2. Transfer Characteristics

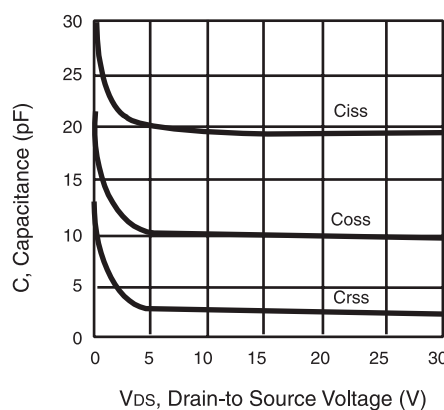


Figure 3. Capacitance

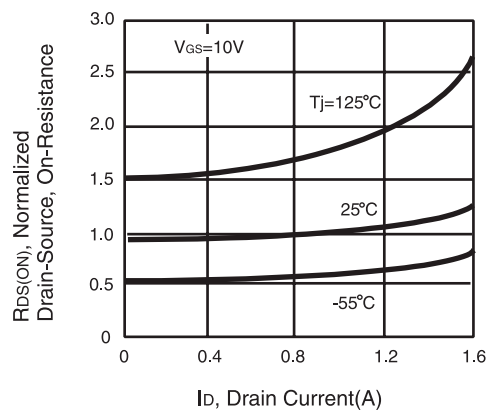
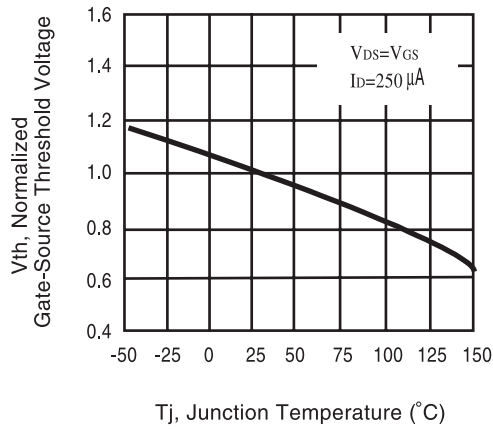
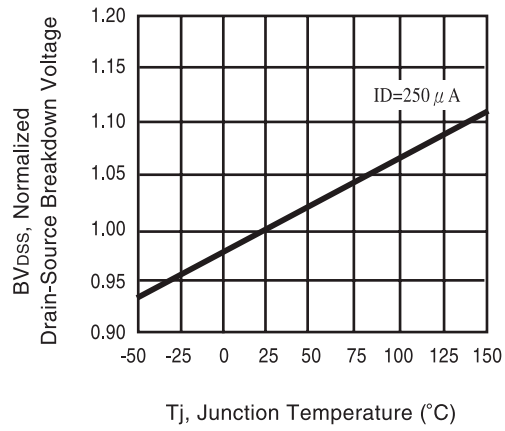


Figure 4. On-Resistance Variation with Drain Current and Temperature

# 2N7002

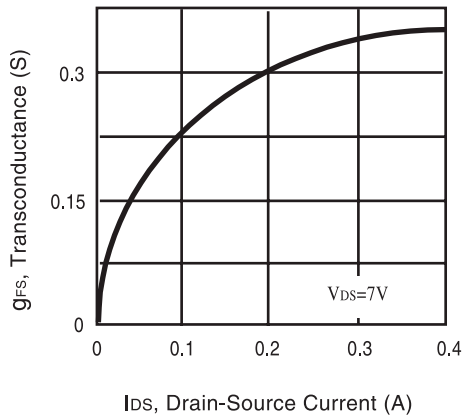


**Figure 5. Gate Threshold Variation with Temperature**

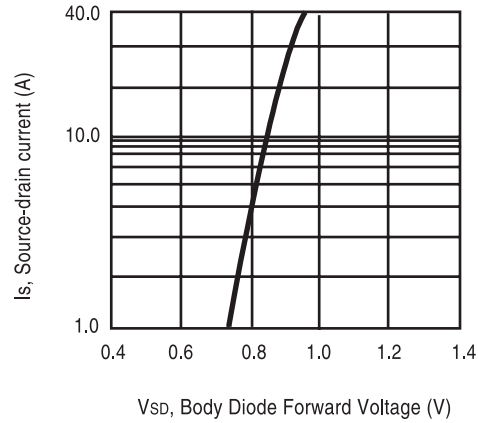


**Figure 6. Breakdown Voltage Variation with Temperature**

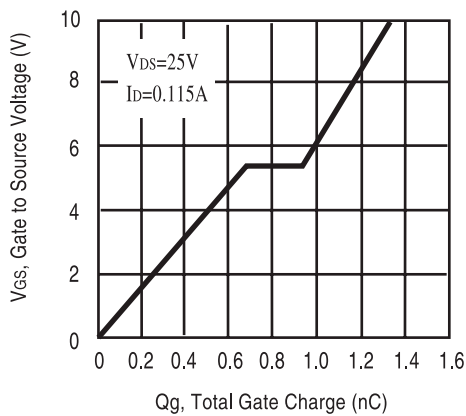
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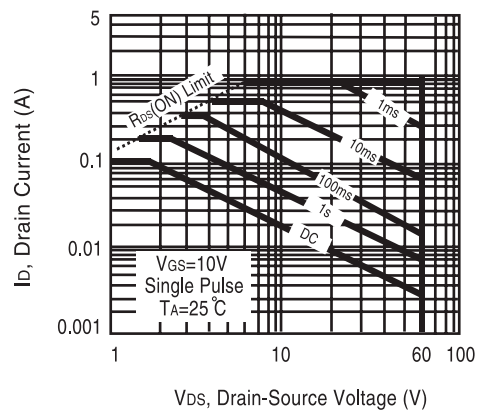
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

# 2N7002

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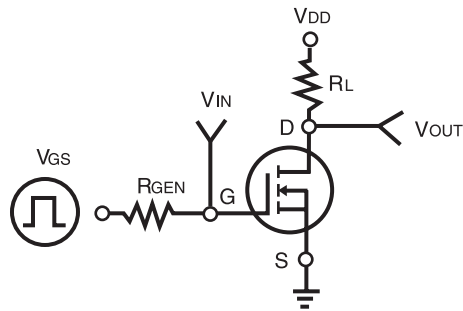


Figure 11. Switching Test Circuit

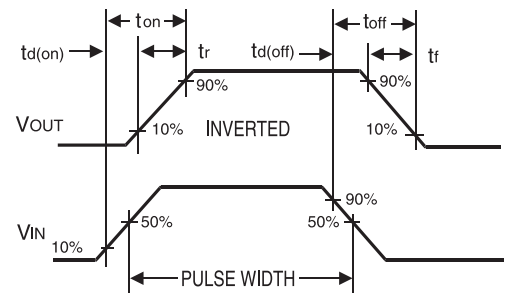


Figure 12. Switching Waveforms

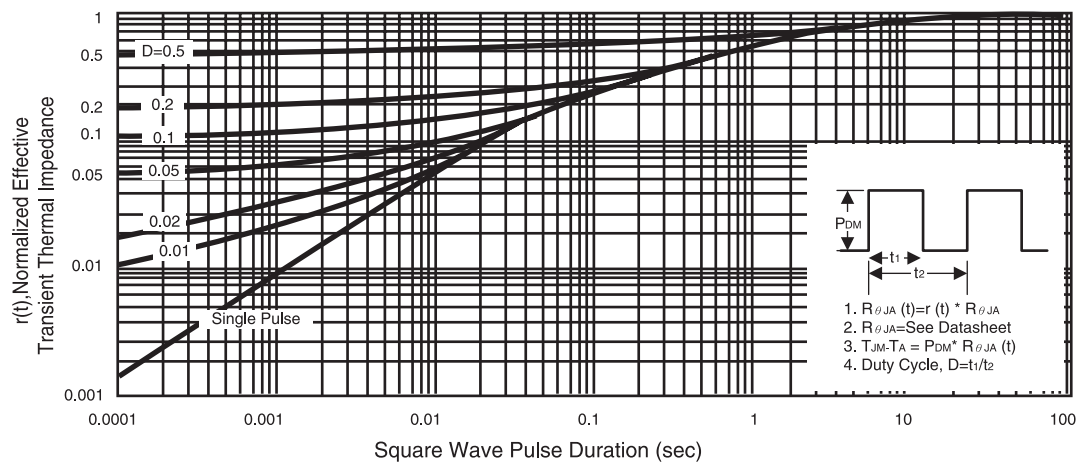


Figure 13. Normalized Thermal Transient Impedance Curve