

SRAM

32K x 8 SRAM

FEATURES

- High speed: 10, 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +5V \pm 10% power supply
- Easy memory expansion with \overline{CE} and \overline{OE} options
- All inputs and outputs are TTL-compatible

OPTIONS

- Timing

| | |
|-------------|-----|
| 10ns access | -10 |
| 12ns access | -12 |
| 15ns access | -15 |
| 20ns access | -20 |
| 25ns access | -25 |
- Packages

| | |
|-----------------------|------|
| Plastic DIP (300 mil) | None |
| Plastic SOJ (300 mil) | DJ |
- 2V data retention (optional) L
- Low power (optional) P
- Temperature

| | |
|------------------------------|------|
| Commercial (0°C to +70°C) | None |
| Industrial (-40°C to +85°C) | IT |
| Automotive (-40°C to +125°C) | AT |
| Extended (-55°C to +125°C) | XT |
- Part Number Example: MT5C2568DJ-20 L

MARKING

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

GENERAL DESCRIPTION

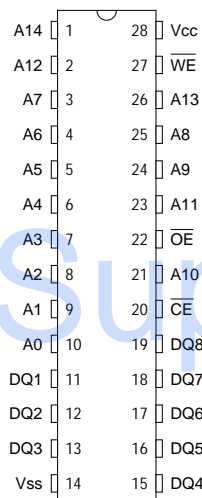
The MT5C2568 is organized as a 32,768 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable (\overline{CE}) and output enable (\overline{OE}) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

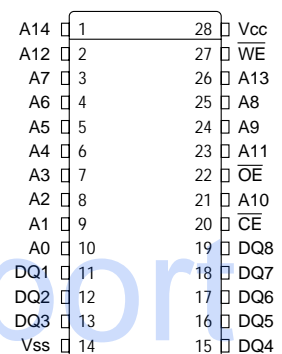
Writing to these devices is accomplished when write enable (\overline{WE}) and \overline{CE} inputs are both LOW. Reading is accomplished when \overline{WE} remains HIGH and \overline{CE} and \overline{OE} go LOW. The device offers a reduced power standby mode

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



28-Pin SOJ (SD-2)

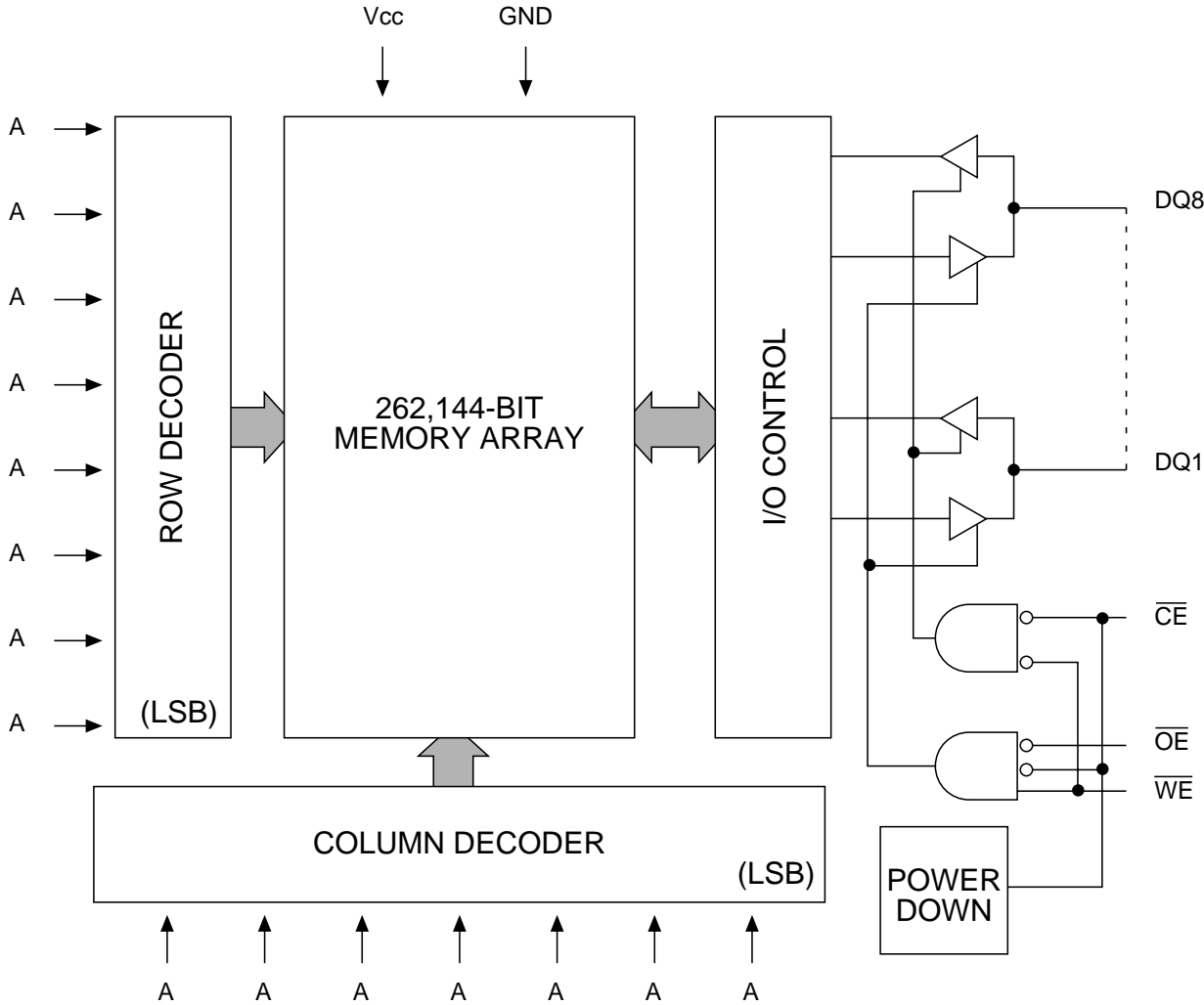


when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the \overline{WE} , \overline{OE} and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

| MODE | \overline{OE} | \overline{CE} | \overline{WE} | DQ | POWER |
|--------------|-----------------|-----------------|-----------------|--------|---------|
| STANDBY | X | H | X | HIGH-Z | STANDBY |
| READ | L | L | H | Q | ACTIVE |
| NOT SELECTED | H | L | H | HIGH-Z | ACTIVE |
| WRITE | X | L | L | D | ACTIVE |

ABSOLUTE MAXIMUM RATINGS*

| | |
|---|----------------------------|
| Voltage on V _{CC} Supply Relative to V _{SS} | -1V to +7V |
| Storage Temperature (plastic) | -55°C to +150°C |
| Short Circuit Output Current | 50mA |
| Voltage on Any Pin Relative to V _{SS} | -1V to V _{CC} +1V |
| Junction Temperature** | +150°C |

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|------------------------------|---|-----------------|------|--------------------|-------|-------|
| Input High (Logic 1) Voltage | | V _{IH} | 2.2 | V _{CC} +1 | V | 1 |
| Input Low (Logic 0) Voltage | | V _{IL} | -0.5 | 0.8 | V | 1, 2 |
| Input Leakage Current | 0V ≤ V _{IN} ≤ V _{CC} | I _{LI} | -5 | 5 | μA | |
| Output Leakage Current | Output(s) disabled 0V ≤ V _{OUT} ≤ V _{CC} | I _{LO} | -5 | 5 | μA | |
| Output High Voltage | I _{OH} = -4.0mA | V _{OH} | 2.4 | | V | 1 |
| Output Low Voltage | I _{OL} = 8.0mA | V _{OL} | | 0.4 | V | 1 |
| Supply Voltage | | V _{CC} | 4.5 | 5.5 | V | 1 |

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | MAX | | | | | UNITS | NOTES |
|---------------------------------|---|------------------|-----|------|------|------|-----|-----|-------|-------|
| | | | | -10† | -12† | -15† | -20 | -25 | | |
| Power Supply Current: Operating | $\overline{CE} \leq V_{IL}; V_{CC} = \text{MAX}$ f = MAX = 1/†RC outputs open | I _{CC} | 130 | 200 | 180 | 165 | 150 | 140 | mA | 3, 13 |
| | P version | I _{CC} | 100 | - | - | 140 | 125 | 120 | mA | 3, 13 |
| Power Supply Current: Standby | $\overline{CE} \geq V_{IH}; V_{CC} = \text{MAX}$ f = MAX = 1/†RC outputs open | I _{SB1} | 24 | 55 | 50 | 45 | 40 | 35 | mA | 13 |
| | P version | I _{SB1} | 1.4 | - | - | 4 | 4 | 4 | mA | 13 |
| | $\overline{CE} \geq V_{CC} - 0.2V; V_{CC} = \text{MAX}$ V _{IN} ≤ V _{SS} +0.2V or V _{IN} ≥ V _{CC} -0.2V; f = 0 | I _{SB2} | 0.6 | 5 | 5 | 5 | 5 | 5 | mA | 13 |
| | P version | I _{SB2} | 0.4 | - | - | 3 | 3 | 3 | mA | 13 |

†P version not available with this speed.



CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | MAX | UNITS | NOTES |
|--------------------|---|--------|-----|-------|-------|
| Input Capacitance | $T_A = 25^\circ\text{C}; f = 1 \text{ MHz}$ $V_{CC} = 5\text{V}$ | C_i | 6 | pF | 4 |
| Output Capacitance | | C_o | 6 | pF | 4 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}; V_{CC} = 5\text{V} \pm 10\%$)

| DESCRIPTION | SYM | -10 | | -12 | | -15 | | -20 | | -25 | | UNITS | NOTES |
|--|------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------|-------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| READ Cycle | | | | | | | | | | | | | |
| READ cycle time | t_{RC} | 10 | | 12 | | 15 | | 20 | | 25 | | ns | |
| Address access time | t_{AA} | | 10 | | 12 | | 15 | | 20 | | 25 | ns | |
| Chip Enable access time | t_{ACE} | | 10 | | 12 | | 15 | | 20 | | 25 | ns | |
| Output hold from address change | t_{OH} | 3 | | 3 | | 3 | | 3 | | 3 | | ns | |
| Chip Enable to output in Low-Z | t_{LZCE} | 3 | | 3 | | 3 | | 3 | | 3 | | ns | 7 |
| Chip disable to output in High-Z | t_{HZCE} | | 5 | | 6 | | 8 | | 9 | | 9 | ns | 6, 7 |
| Chip Enable to power-up time | t_{PU} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | 4 |
| Chip disable to power-down time | t_{PD} | | 10 | | 12 | | 15 | | 20 | | 25 | ns | 4 |
| Output Enable access time | t_{AOE} | | 5 | | 6 | | 8 | | 8 | | 8 | ns | |
| Output Enable to output in Low-Z | t_{LZOE} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Output disable to output in High-Z | t_{HZOE} | | 5 | | 6 | | 6 | | 7 | | 7 | ns | 6 |
| WRITE Cycle | | | | | | | | | | | | | |
| WRITE cycle time | t_{WC} | 10 | | 12 | | 15 | | 20 | | 25 | | ns | |
| Chip Enable to end of write | t_{CW} | 7 | | 8 | | 10 | | 12 | | 15 | | ns | |
| Chip Enable to end of write (P and LP version) | t_{CW} | - | | - | | 12 | | 12 | | 15 | | ns | |
| Address valid to end of write | t_{AW} | 7 | | 8 | | 10 | | 12 | | 15 | | ns | |
| Address valid to end of write (P and LP version) | t_{AW} | - | | - | | 12 | | 12 | | 15 | | ns | |
| Address setup time | t_{AS} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Address hold from end of write | t_{AH} | 1 | | 1 | | 1 | | 1 | | 1 | | ns | |
| WRITE pulse width | t_{WP1} | 7 | | 8 | | 10 | | 12 | | 15 | | ns | |
| WRITE pulse width | t_{WP2} | 10 | | 12 | | 12 | | 15 | | 15 | | ns | |
| Data setup time | t_{DS} | 6 | | 7 | | 7 | | 10 | | 10 | | ns | |
| Data hold time | t_{DH} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Write disable to output in Low-Z | t_{LZWE} | 2 | | 2 | | 2 | | 2 | | 2 | | ns | 7 |
| Write Enable to output in High-Z | t_{HZWE} | | 5 | | 6 | | 7 | | 8 | | 10 | ns | 6, 7 |



INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C2568 SRAMs.
 ($-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$)

| DESCRIPTION | CONDITIONS | SYMBOL | MAX | | | | | UNITS | NOTES |
|---------------------------------|---|------------------|-----|-----|-----|-----|-----|-------|-------|
| | | | -10 | -12 | -15 | -20 | -25 | | |
| Power Supply Current: Operating | $\overline{\text{CE}} \leq V_{\text{IL}}; V_{\text{CC}} = \text{MAX}$ $f = \text{MAX} = 1/\tau_{\text{RC}}$ outputs open | I _{CC} | 210 | 190 | 170 | 160 | 150 | mA | 3 |
| Power Supply Current: Standby | $\overline{\text{CE}} \geq V_{\text{IH}}; V_{\text{CC}} = \text{MAX}$ $f = \text{MAX} = 1/\tau_{\text{RC}}$ outputs open | I _{SB1} | 65 | 60 | 50 | 45 | 40 | mA | |
| | $\overline{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}; V_{\text{CC}} = \text{MAX}$ $V_{\text{IN}} \leq V_{\text{SS}} + 0.2\text{V}$ or $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}; f = 0$ | I _{SB2} | 6 | 6 | 6 | 6 | 6 | mA | |

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

| DESCRIPTION | CONDITIONS | SYMBOL | MAX | UNITS | NOTES |
|------------------------|--|-----------------------------|-------------------|-------|---------------|
| Data Retention Current | $\overline{\text{CE}} \geq (V_{\text{CC}} - 0.2\text{V})$ $V_{\text{IN}} \geq (V_{\text{CC}} - 0.2\text{V})$ or $\leq 0.2\text{V}$ | $V_{\text{CC}} = 2\text{V}$ | I _{CCDR} | 400 | μA |
| | | $V_{\text{CC}} = 3\text{V}$ | I _{CCDR} | 600 | μA |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
 (Notes 5, 13) ($-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$)

| DESCRIPTION | SYM | -12 | | -15 | | -20 | | -25 | | UNITS | NOTES |
|---------------------------------|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-------|-------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| READ Cycle | | | | | | | | | | | |
| Output hold from address change | t _{OH} | 2 | | 2 | | 2 | | 2 | | ns | |
| Chip Enable to output in Low-Z | t _{LZCE} | 2 | | 2 | | 2 | | 2 | | ns | 7 |
| WRITE Cycle | | | | | | | | | | | |
| Address hold from end of write | t _{AH} | 2 | | 2 | | 2 | | 2 | | ns | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|------------------------------|------------|-----------------|-----|--------------------|-------|-------|
| Input High (Logic 1) Voltage | | V _{IH} | 2.3 | V _{CC} +1 | V | 1 |



AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2568 SRAMs. ($-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ - AT) ($-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ - XT)

| DESCRIPTION | CONDITIONS | SYMBOL | MAX | | | | UNITS | NOTES |
|---------------------------------|---|------------------|-----|-----|-----|-----|-------|-------|
| | | | -12 | -15 | -20 | -25 | | |
| Power Supply Current: Operating | $\overline{\text{CE}} \leq V_{IL}$; $V_{CC} = \text{MAX}$ $f = \text{MAX} = 1/{}^t\text{RC}$ outputs open | I _{CC} | 195 | 175 | 165 | 155 | mA | 3 |
| Power Supply Current: Standby | $\overline{\text{CE}} \geq V_{IH}$; $V_{CC} = \text{MAX}$ $f = \text{MAX} = 1/{}^t\text{RC}$ outputs open | I _{SB1} | 60 | 50 | 45 | 40 | mA | |
| | $\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}$; $V_{CC} = \text{MAX}$ $V_{IN} \leq V_{SS} + 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}$; $f = 0$ | I _{SB2} | 7 | 7 | 7 | 7 | mA | |

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

| DESCRIPTION | CONDITIONS | SYMBOL | MAX | UNITS | NOTES |
|------------------------|---|----------------------|-------------------|-------|---------------|
| Data Retention Current | $\overline{\text{CE}} \geq (V_{CC} - 0.2\text{V})$ $V_{IN} \geq (V_{CC} - 0.2\text{V})$ or $\leq 0.2\text{V}$ | $V_{CC} = 2\text{V}$ | I _{CCDR} | 500 | μA |
| | | $V_{CC} = 3\text{V}$ | I _{CCDR} | 800 | μA |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) ($-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ - AT; $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ - XT; $V_{CC} = 5\text{V} \pm 10\%$)

| DESCRIPTION | SYM | -12 | | -15 | | -20 | | -25 | | UNITS | NOTES |
|---------------------------------|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-------|-------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| READ Cycle | | | | | | | | | | | |
| Output hold from address change | ${}^t\text{OH}$ | 2 | | 2 | | 2 | | 2 | | ns | |
| Chip Enable to output in Low-Z | ${}^t\text{LZCE}$ | 2 | | 2 | | 2 | | 2 | | ns | 7 |
| WRITE Cycle | | | | | | | | | | | |
| Address hold from end of write | ${}^t\text{AH}$ | 2 | | 2 | | 2 | | 2 | | ns | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ - AT) ($-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ - XT)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|------------------------------|------------|----------|-----|--------------|-------|-------|
| Input High (Logic 1) Voltage | | V_{IH} | 2.3 | $V_{CC} + 1$ | V | 1 |



AC TEST CONDITIONS

| | |
|-------------------------------------|-------------------------|
| Input pulse levels | V _{SS} to 3.0V |
| Input rise and fall times | 3ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output load | See Figures 1 and 2 |

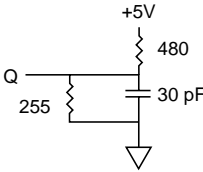


Fig. 1 OUTPUT LOAD EQUIVALENT

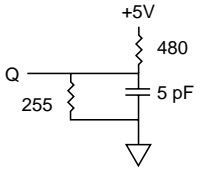


Fig. 2 OUTPUT LOAD EQUIVALENT

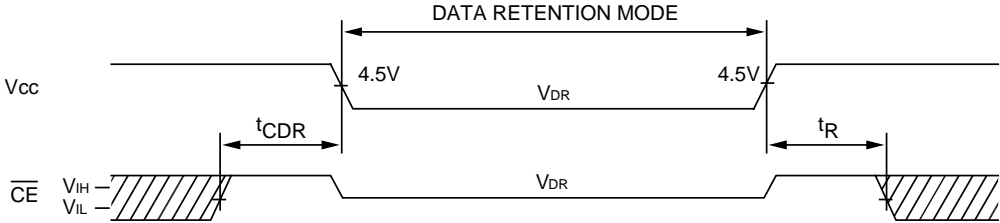
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < t_{RC}/2.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. t^HZCE, t^HZOE and t^HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, t^HZCE is less than t^LZCE, and t^HZWE is less than t^LZWE.
8. \overline{WE} is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

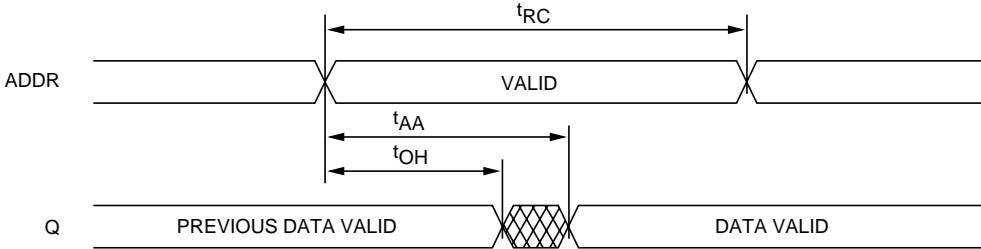
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

| DESCRIPTION | CONDITIONS | | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------------------|---|----------------------|-------------------|-----------------|-----|-----|-------|-------|
| V _{CC} for Retention Data | | | V _{DR} | 2 | | | V | |
| Data Retention Current L version | $\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$ | V _{CC} = 2V | I _{CCDR} | | 125 | 300 | μA | 14 |
| | | V _{CC} = 3V | I _{CCDR} | | 175 | 500 | μA | 14 |
| Data Retention Current LP version | $\overline{CE} \geq (V_{CC} - 0.2V)$ | V _{CC} = 2V | I _{CCDR} | | 100 | 300 | μA | 14 |
| | | V _{CC} = 3V | I _{CCDR} | | 150 | 500 | μA | 14 |
| Chip Deselect to Data Retention Time | | | t _{CDR} | 0 | | | ns | 4 |
| Operation Recovery Time | | | t _R | t _{RC} | | | ns | 4, 11 |

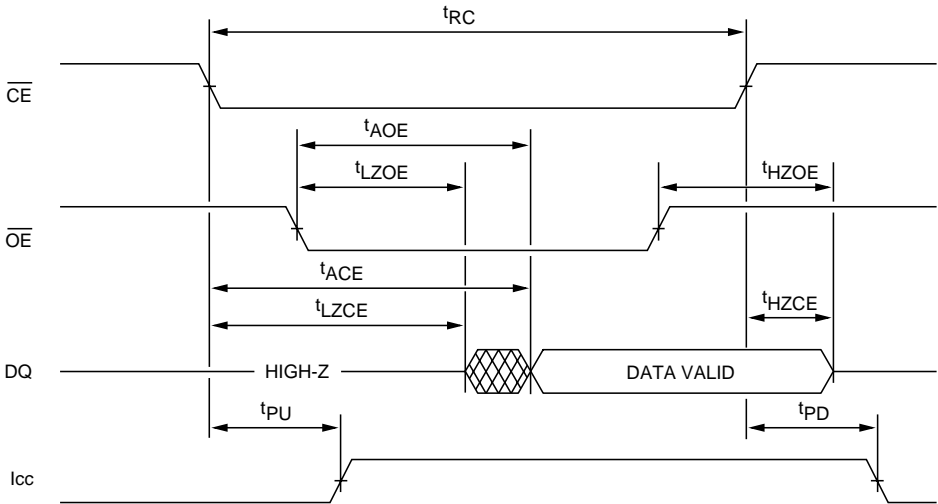
LOW V_{CC} DATA RETENTION WAVEFORM





READ CYCLE NO. 1 ^{8, 9}

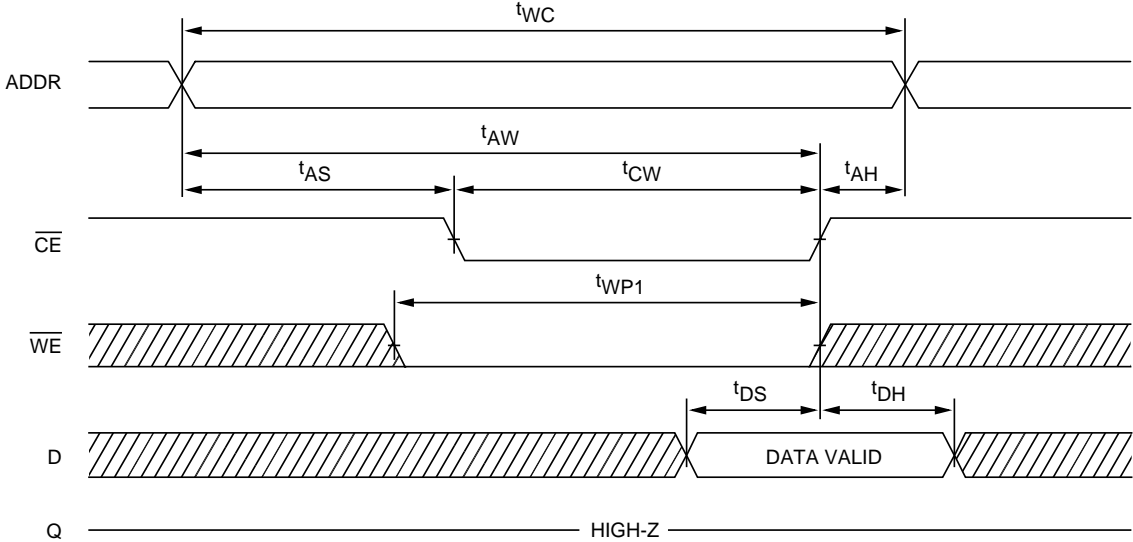


READ CYCLE NO. 2 ^{7, 8, 10}

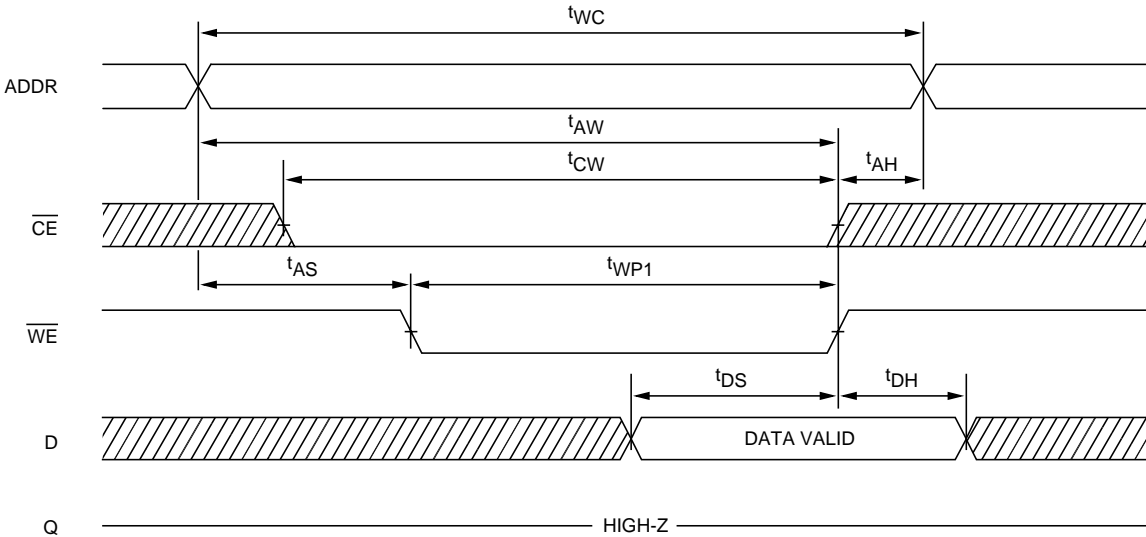




 DON'T CARE
 UNDEFINED

WRITE CYCLE NO. 1¹²
(Chip Enable Controlled)



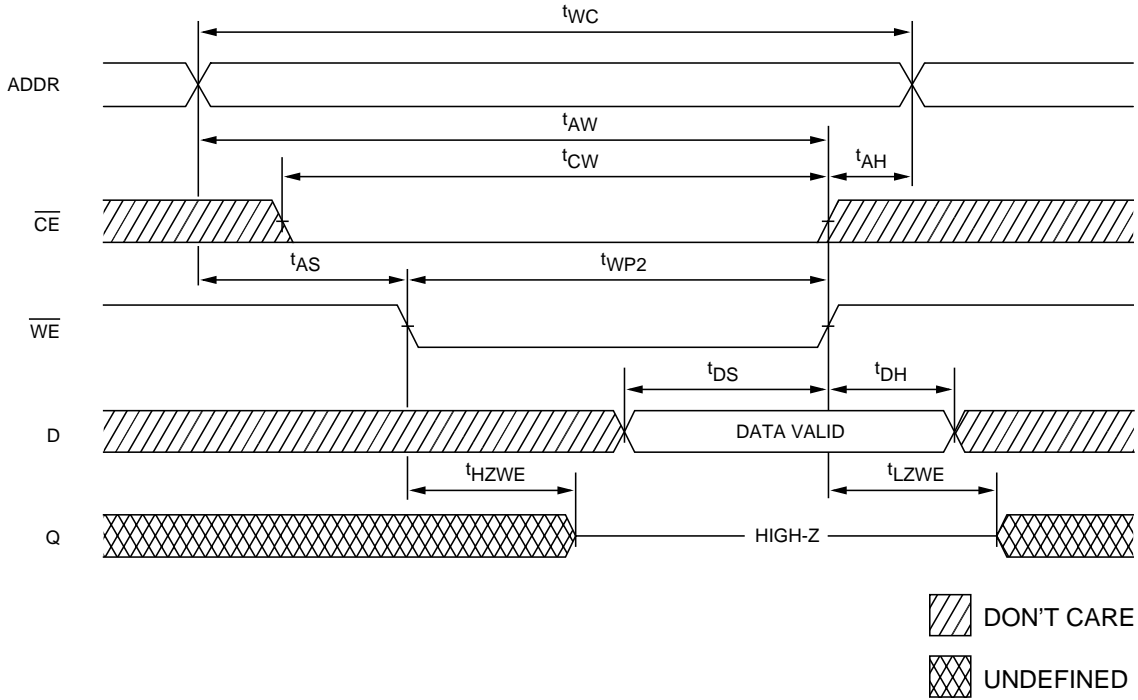
WRITE CYCLE NO. 2¹²
(Write Enable Controlled)



 DON'T CARE
 UNDEFINED

NOTE: Output enable (\overline{OE}) is inactive (HIGH).

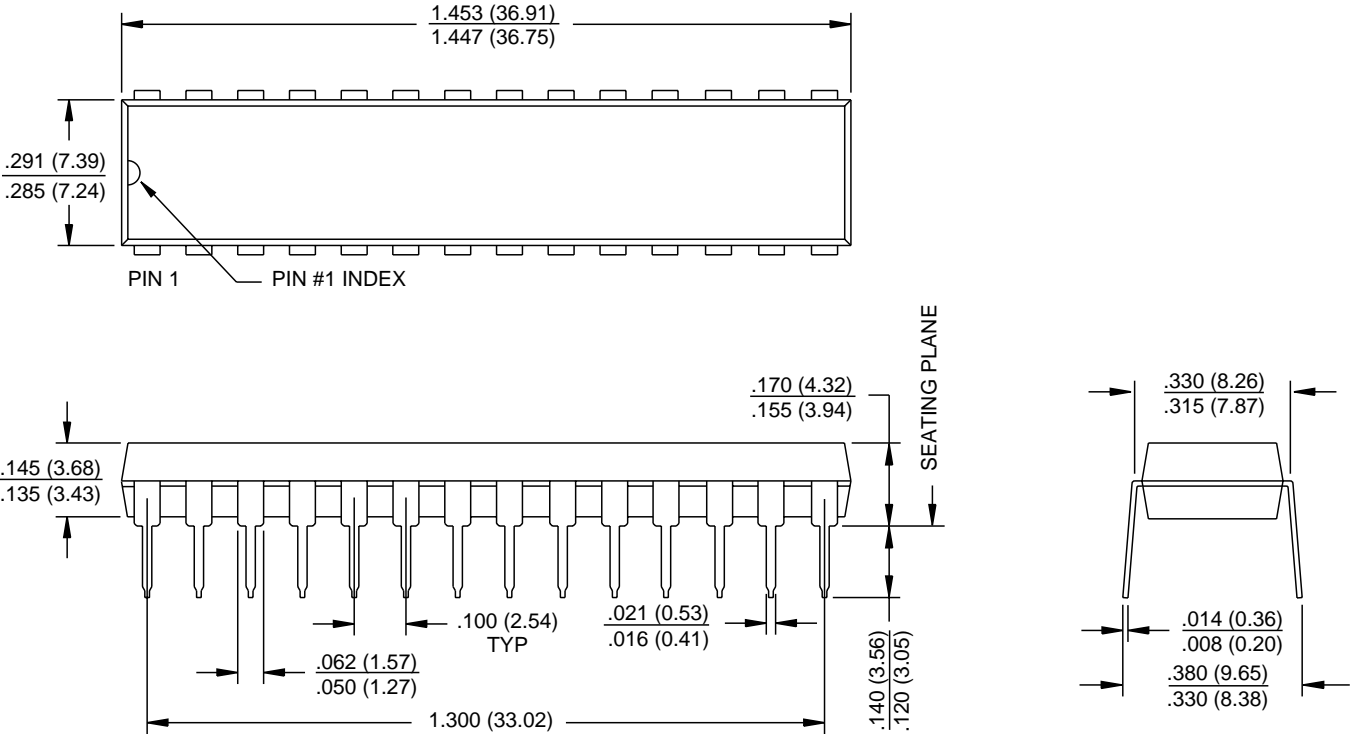
WRITE CYCLE NO. 3 ^{7, 12, 16}
(Write Enable Controlled)



NOTE: Output enable (\overline{OE}) is active (LOW).



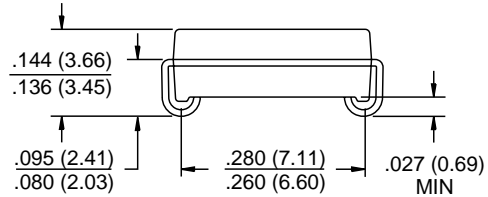
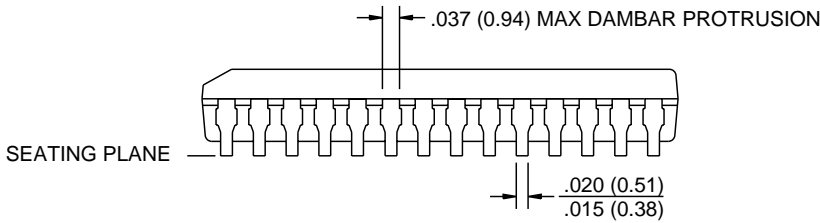
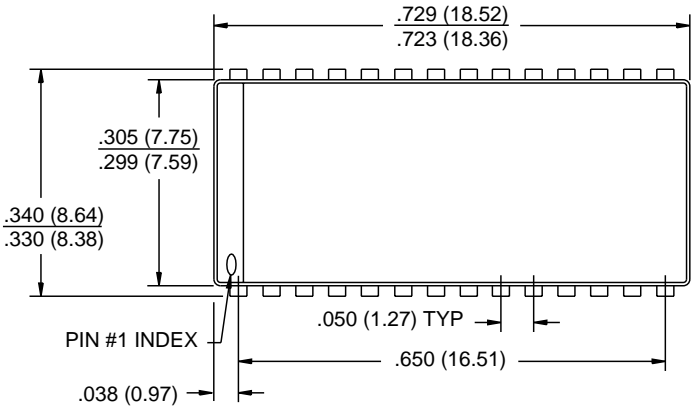
28-PIN PLASTIC DIP



- NOTE:**
1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.



28-PIN PLASTIC SOJ



- NOTE:**
1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.



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