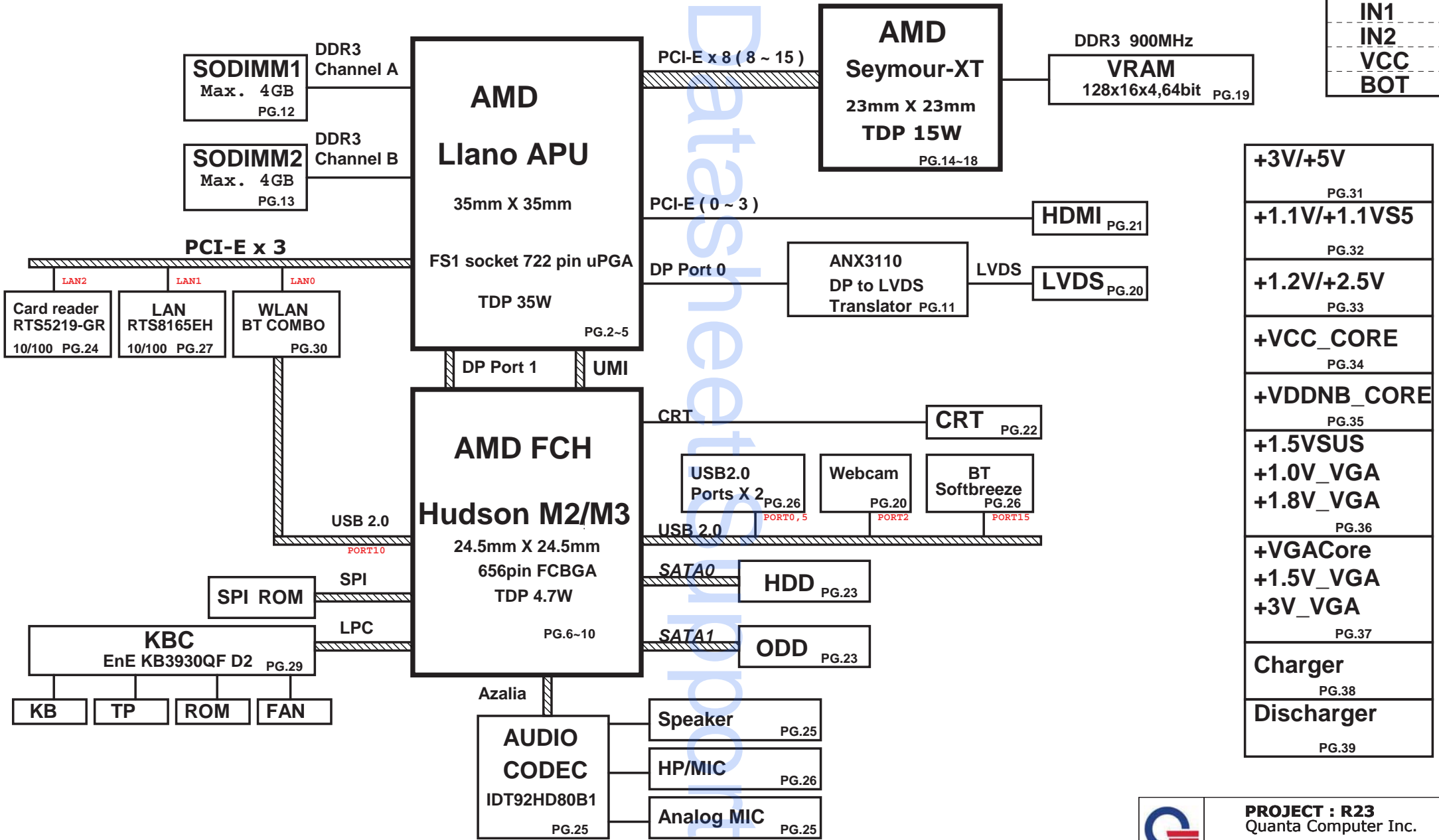
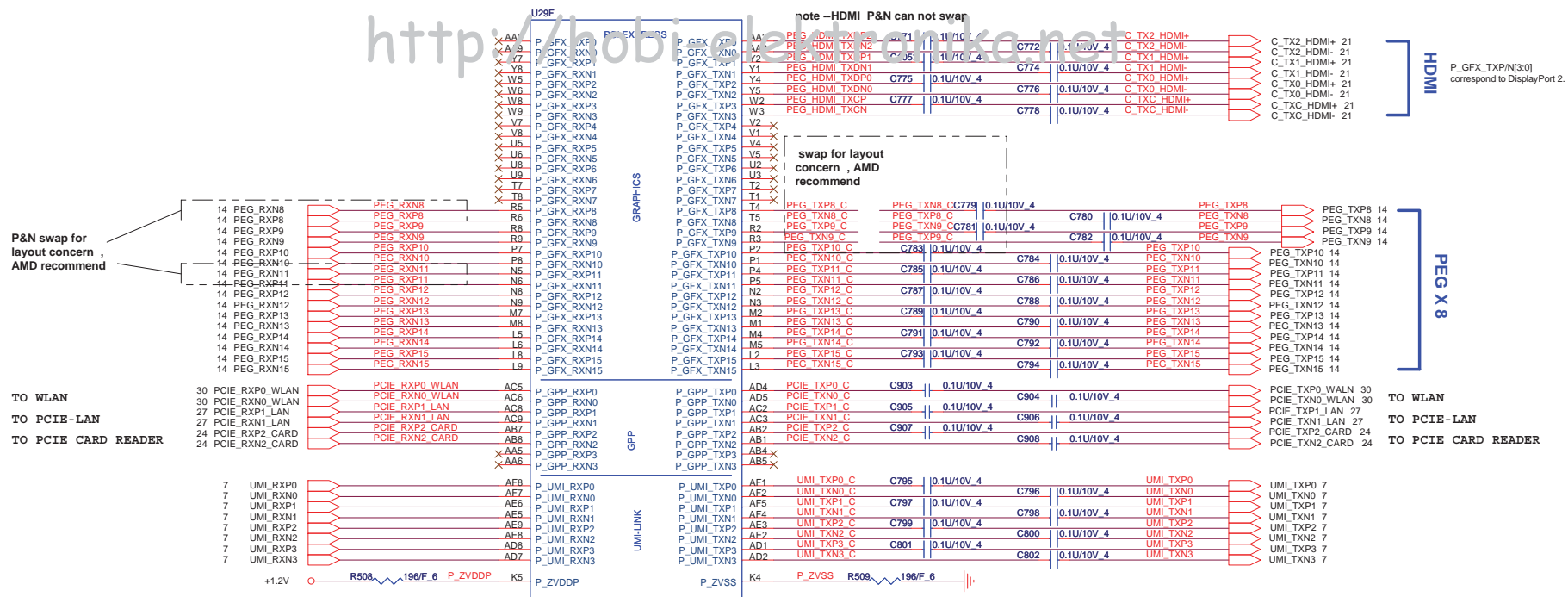


# R23 AMD Sabin UMA/Muxless SYSTEM DIAGRAM

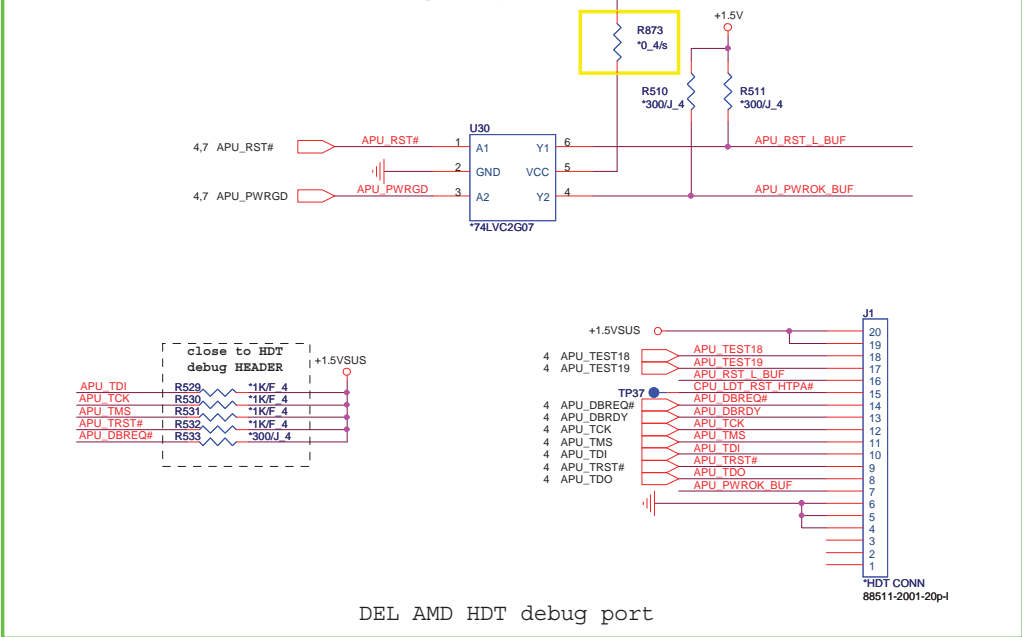
Stackup

TOP  
GND  
IN1  
IN2  
VCC  
BOT

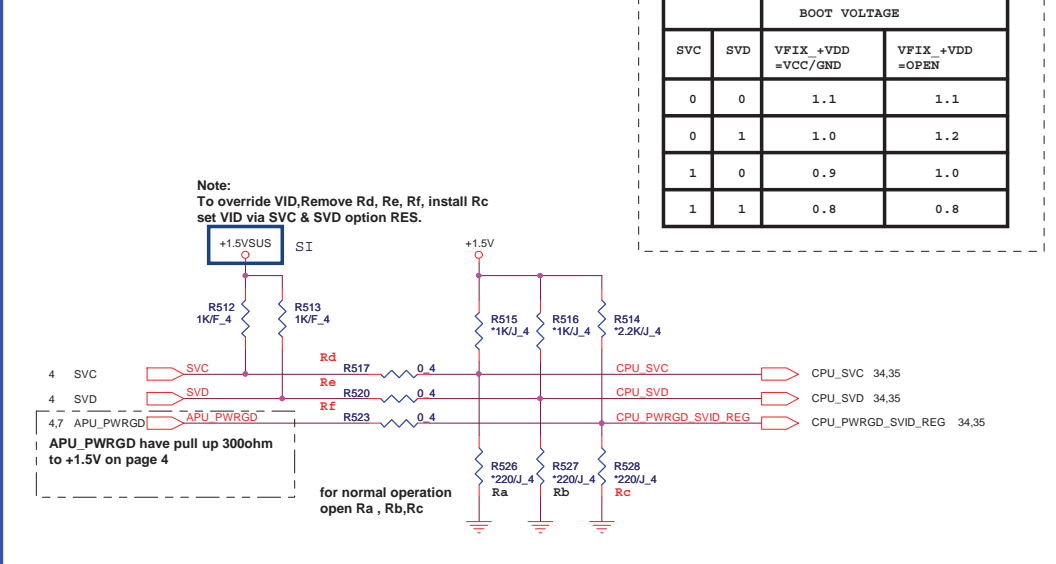




**HDT+ Connector for Debug only**



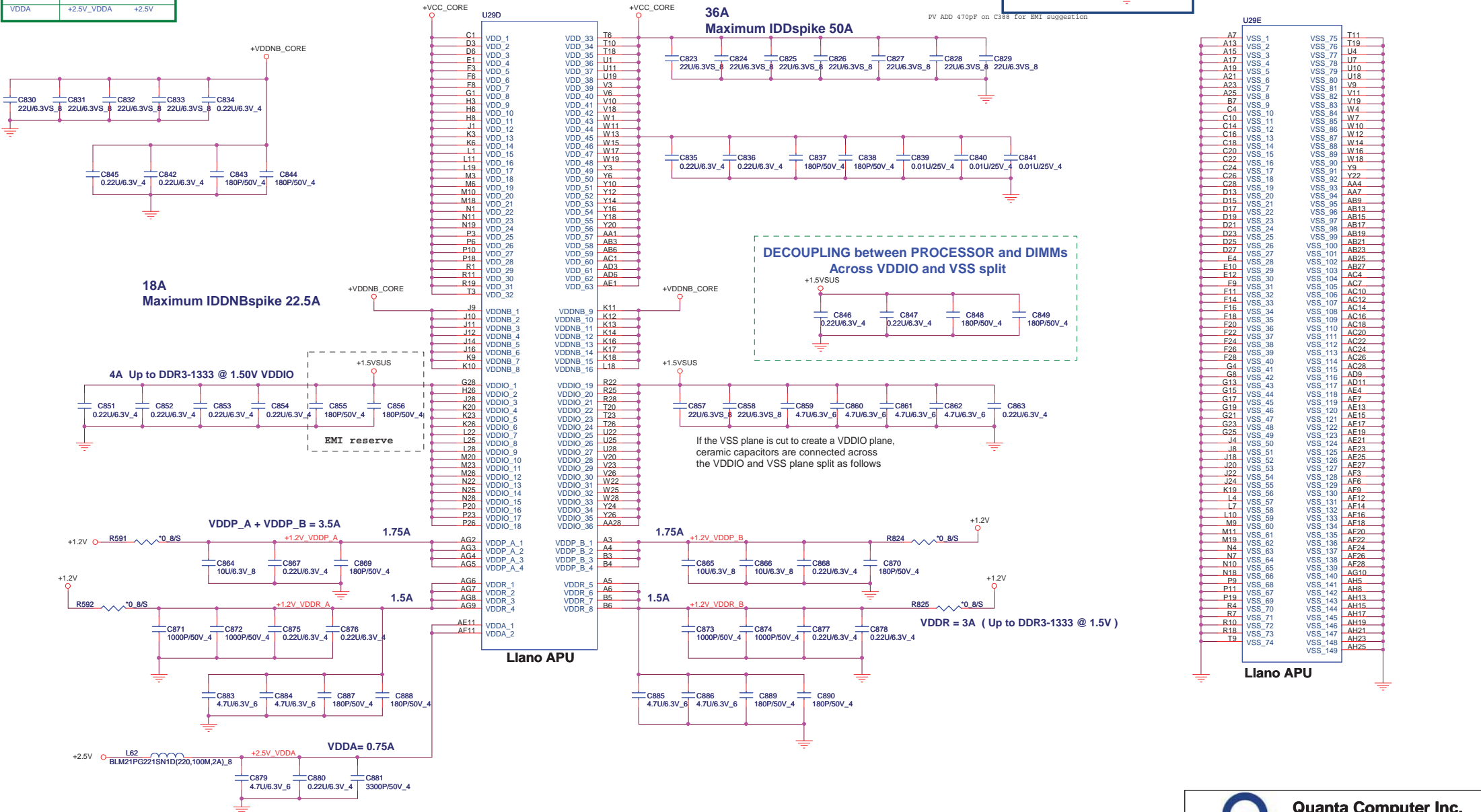
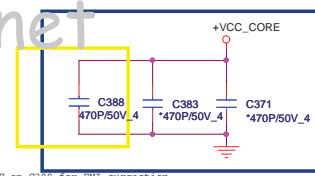
**VID Override Circuit**







PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

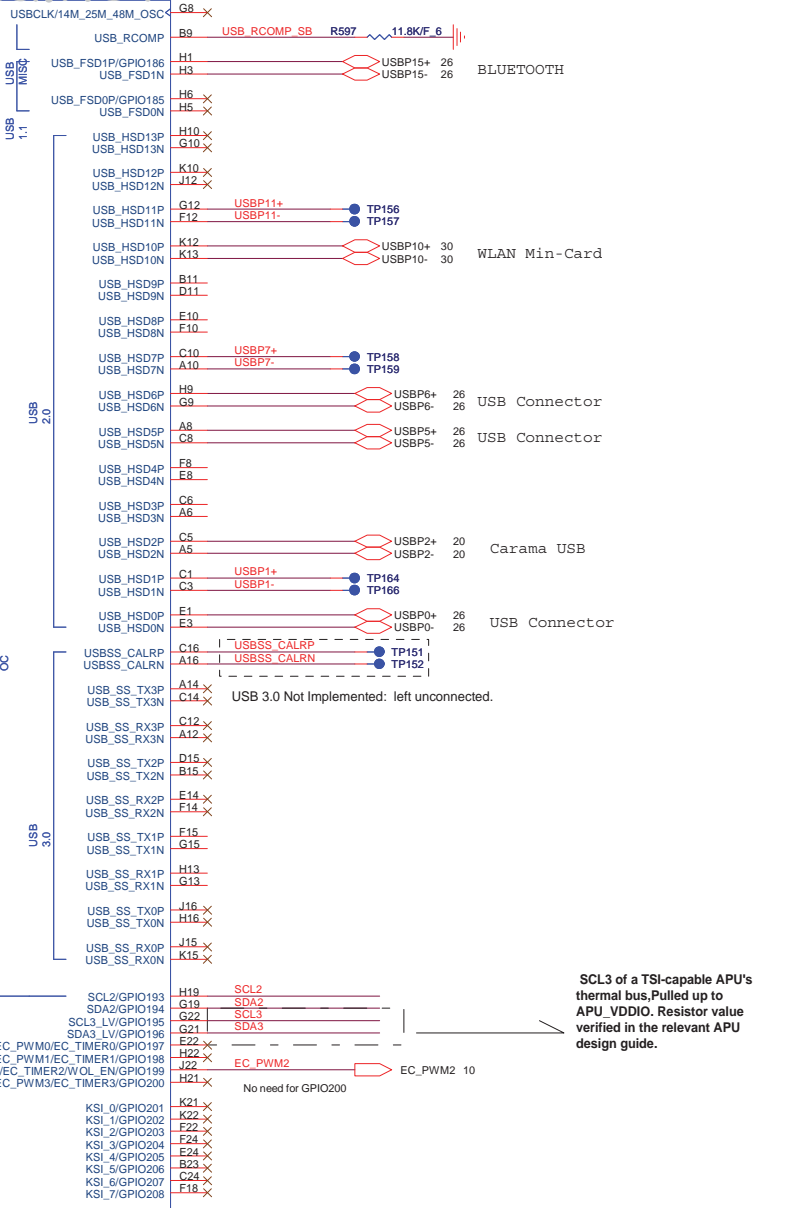
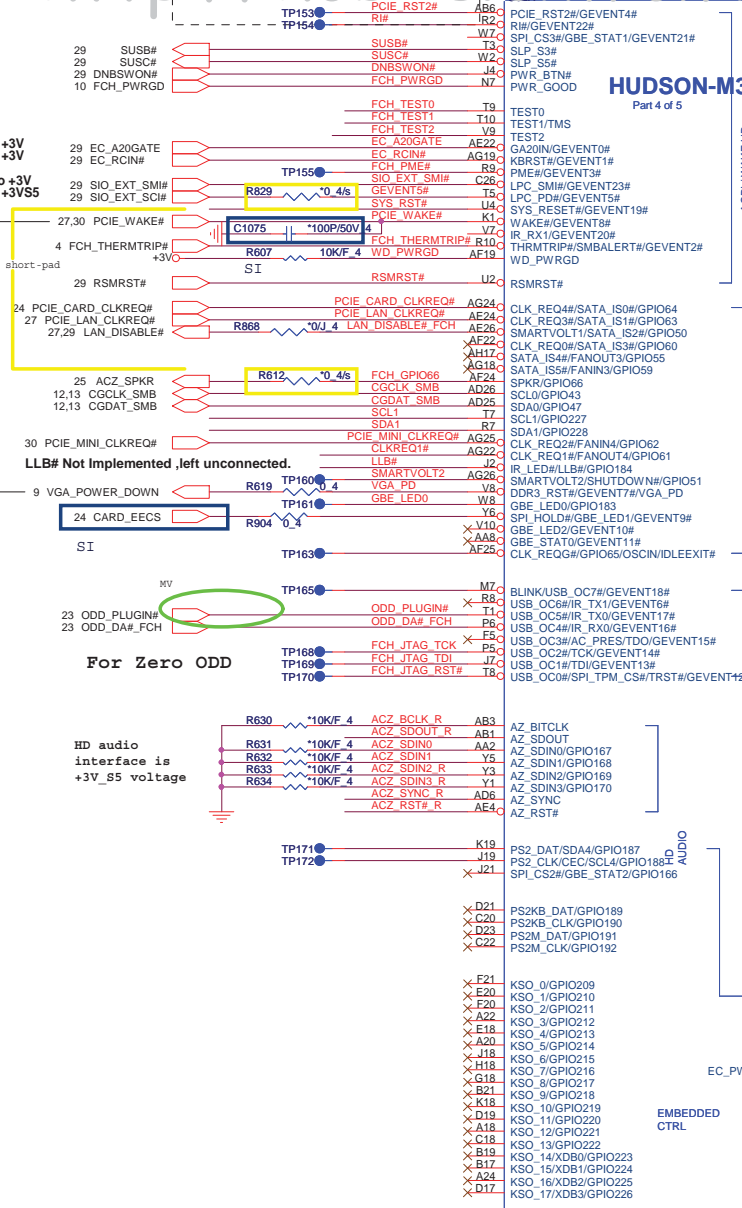
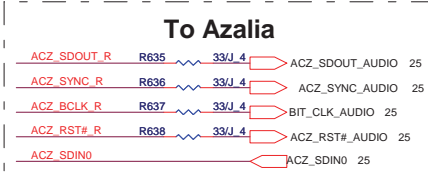
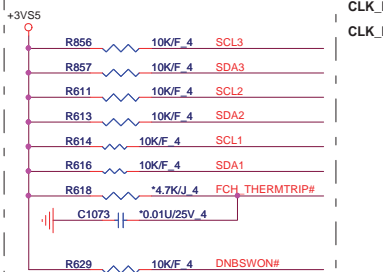
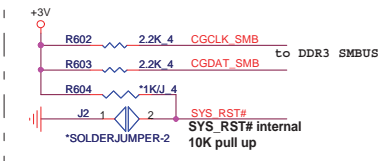
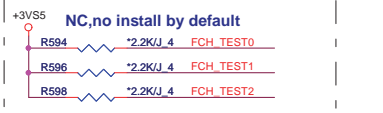


**DECOUPLING between PROCESSOR and DIMMs Across VDDIO and VSS split**

If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

U29E	VSS	T11
A7	VSS_1	VSS_75
A13	VSS_2	VSS_76
A15	VSS_3	VSS_77
A17	VSS_4	VSS_78
A19	VSS_5	VSS_79
A21	VSS_6	VSS_80
A23	VSS_7	VSS_81
A25	VSS_8	VSS_82
B7	VSS_9	VSS_83
C4	VSS_10	VSS_84
C10	VSS_11	VSS_85
C14	VSS_12	VSS_86
C16	VSS_13	VSS_87
C18	VSS_14	VSS_88
C22	VSS_15	VSS_89
C24	VSS_16	VSS_90
C26	VSS_17	VSS_91
C28	VSS_18	VSS_92
D15	VSS_19	VSS_93
D17	VSS_20	VSS_94
D19	VSS_21	VSS_95
D21	VSS_22	VSS_96
D23	VSS_23	VSS_97
D25	VSS_24	VSS_98
D27	VSS_25	VSS_99
E4	VSS_26	VSS_100
E12	VSS_27	VSS_101
F9	VSS_28	VSS_102
F11	VSS_29	VSS_103
F14	VSS_30	VSS_104
F16	VSS_31	VSS_105
F18	VSS_32	VSS_106
F20	VSS_33	VSS_107
F22	VSS_34	VSS_108
F24	VSS_35	VSS_109
F26	VSS_36	VSS_110
F28	VSS_37	VSS_111
G4	VSS_38	VSS_112
G8	VSS_39	VSS_113
G13	VSS_40	VSS_114
G15	VSS_41	VSS_115
G17	VSS_42	VSS_116
G19	VSS_43	VSS_117
G21	VSS_44	VSS_118
G23	VSS_45	VSS_119
G25	VSS_46	VSS_120
J4	VSS_47	VSS_121
J8	VSS_48	VSS_122
J18	VSS_49	VSS_123
J20	VSS_50	VSS_124
J22	VSS_51	VSS_125
K19	VSS_52	VSS_126
L4	VSS_53	VSS_127
L7	VSS_54	VSS_128
L10	VSS_55	VSS_129
M3	VSS_56	VSS_130
M11	VSS_57	VSS_131
M19	VSS_58	VSS_132
N4	VSS_59	VSS_133
N7	VSS_60	VSS_134
N10	VSS_61	VSS_135
N18	VSS_62	VSS_136
P9	VSS_63	VSS_137
P11	VSS_64	VSS_138
R4	VSS_65	VSS_139
R7	VSS_66	VSS_140
R10	VSS_67	VSS_141
R18	VSS_68	VSS_142
T9	VSS_69	VSS_143
	VSS_70	VSS_144
	VSS_71	VSS_145
	VSS_72	VSS_146
	VSS_73	VSS_147
	VSS_74	VSS_148
		VSS_149
		VSS_150



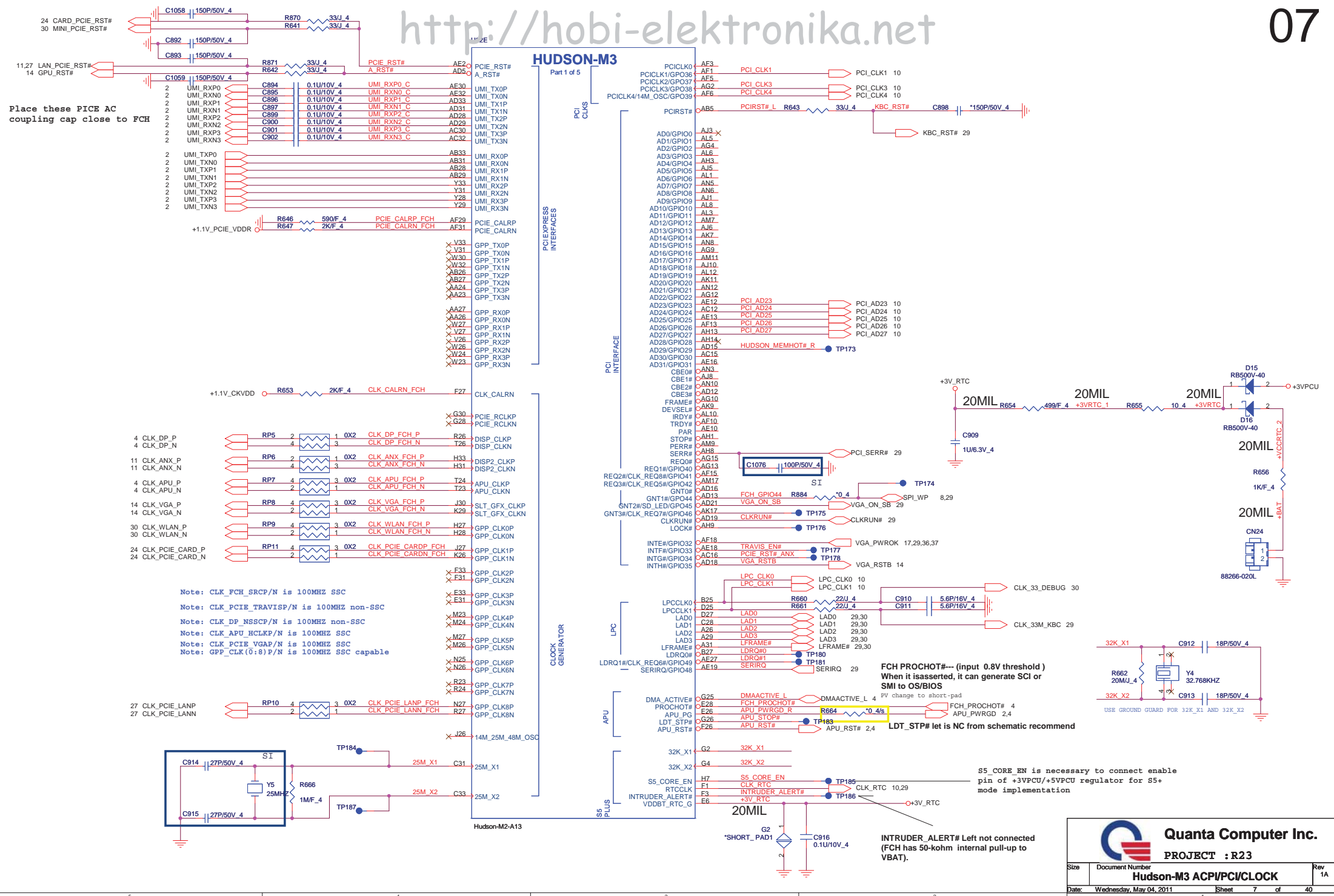


Hudson-M2-A13

SCL3 of a TSI-capable APU's thermal bus, Pulled up to APU\_VDDIO. Resistor value verified in the relevant APU design guide.

**Quanta Computer Inc.**  
PROJECT : R23

Size	Document Number	<b>Hudson-M3 GPIO/USB/AZ/RGMII</b>	Rev	1A
Date:	Wednesday, May 04, 2011	Sheet	6	of 40



**Quanta Computer Inc.**  
PROJECT : R23

Size	Document Number	Rev
	<b>Hudson-M3 ACP/PCI/CLOCK</b>	1A
Date:	Wednesday, May 04, 2011	Sheet 7 of 40

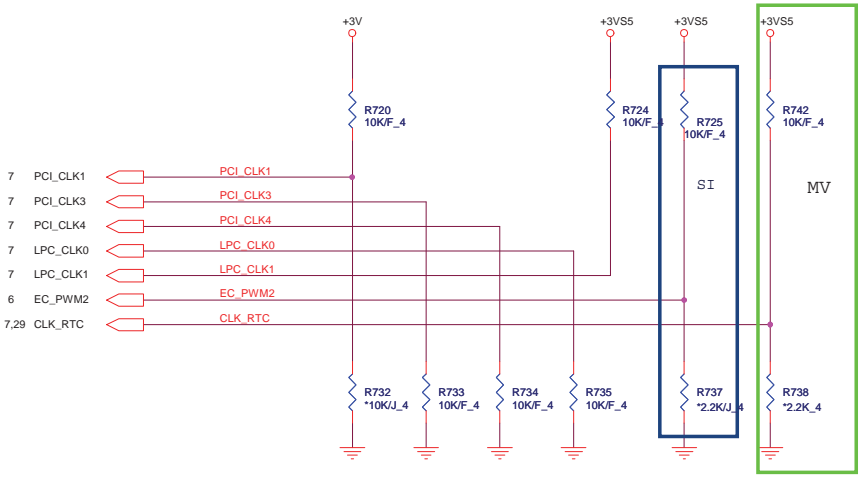






STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
<b>PULL HIGH</b>	-----	ALLOW PCIE Gen2 <b>DEFAULT</b>	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED <b>DEFAULT</b>	LPC ROM <b>DEFAULT</b>	S5 PLUS MODE DISABLED <b>DEFAULT</b>
<b>PULL LOW</b>	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP <b>DEFAULT</b>	FUSION CLOCK MODE <b>DEFAULT</b>	EC DISABLED <b>DEFAULT</b>	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

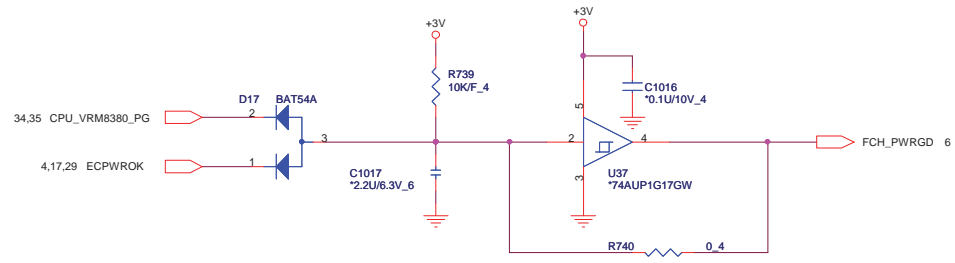
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI\_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL <b>DEFAULT</b>	DISABLE ILA AUTORUN <b>DEFAULT</b>	USE FC PLL <b>DEFAULT</b>	USE DEFAULT PCIE STRAPS <b>DEFAULT</b>	DISABLE PCI MEM BOOT <b>DEFAULT</b>
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

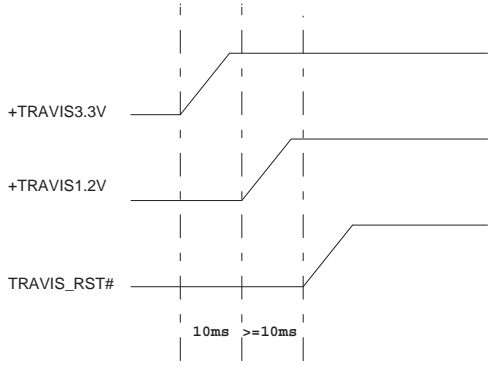
FCH\_PWRGD



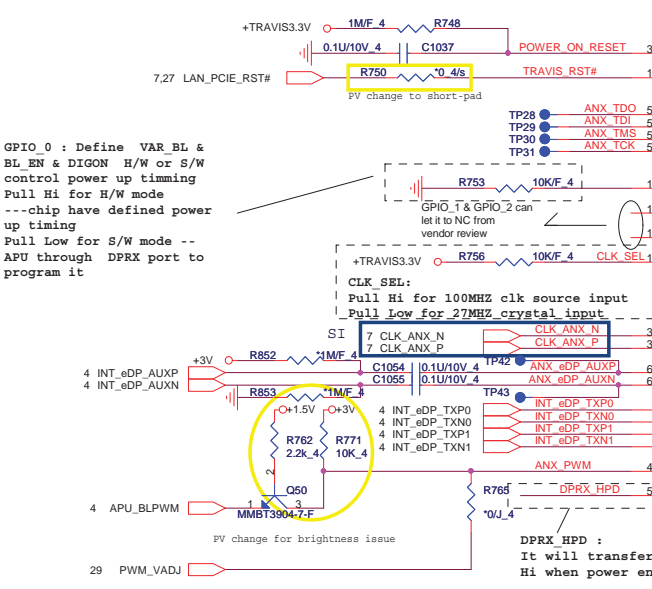
**Quanta Computer Inc.**  
PROJECT : R23

Size	Document Number	Rev
	<b>Hudson-M3 STRAP/PWRGD</b>	1A
Date:	Wednesday, May 04, 2011	Sheet 10 of 40

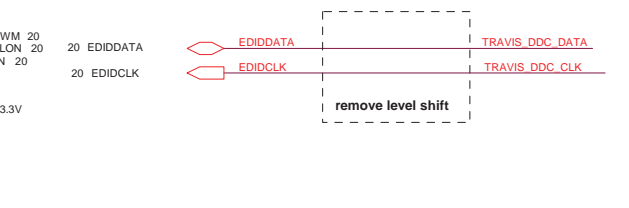
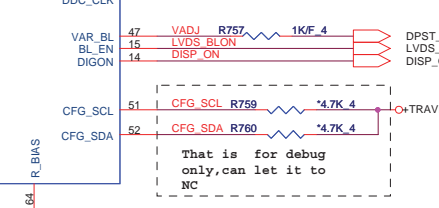
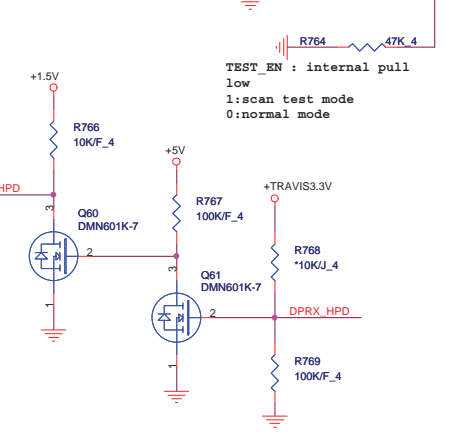
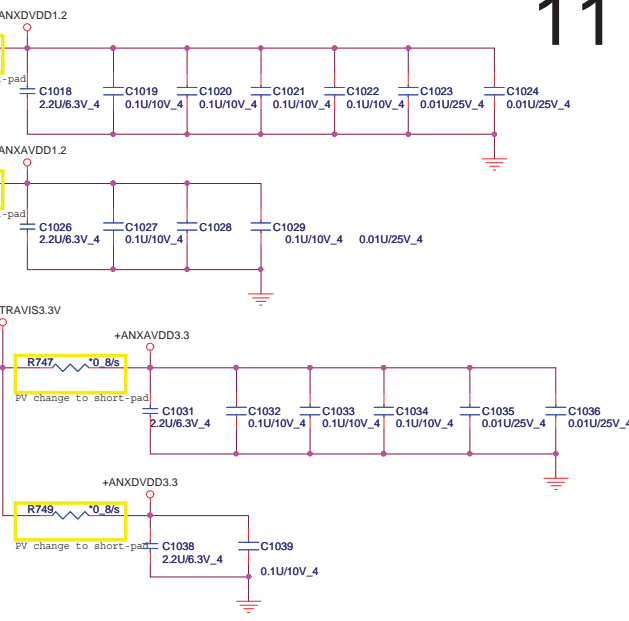
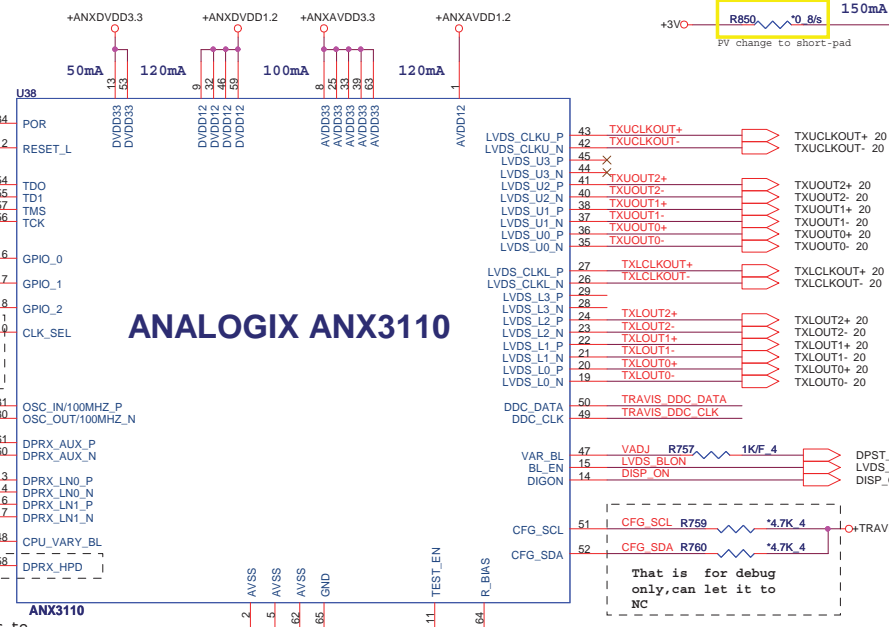
# ANX3110 Power Up Sequence



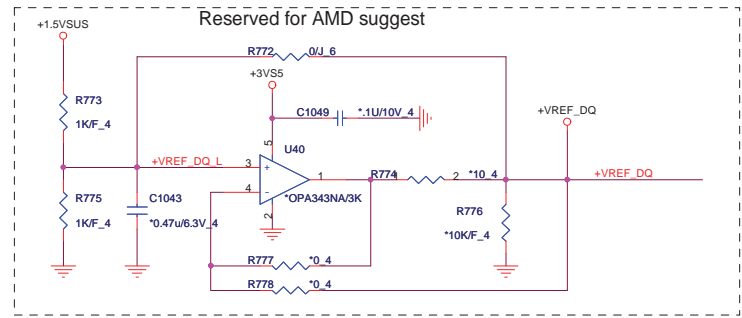
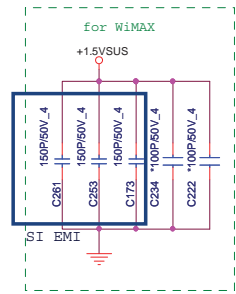
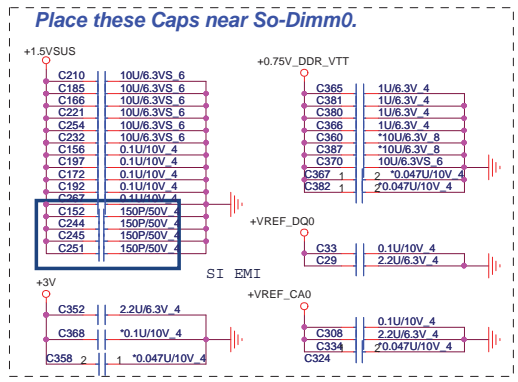
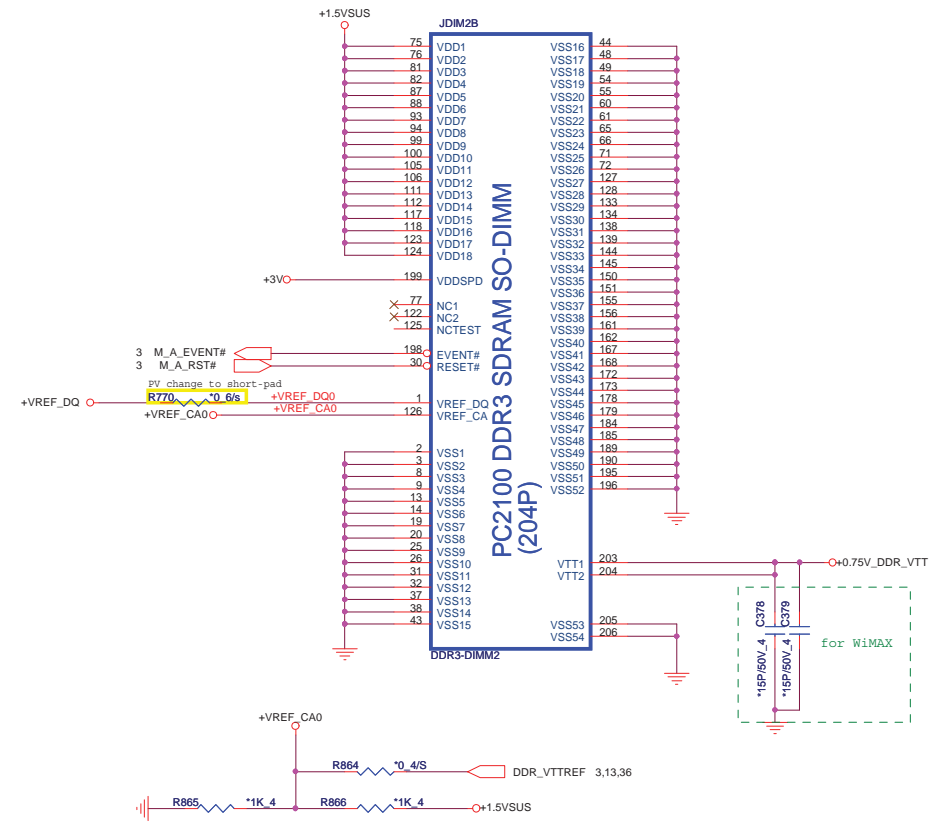
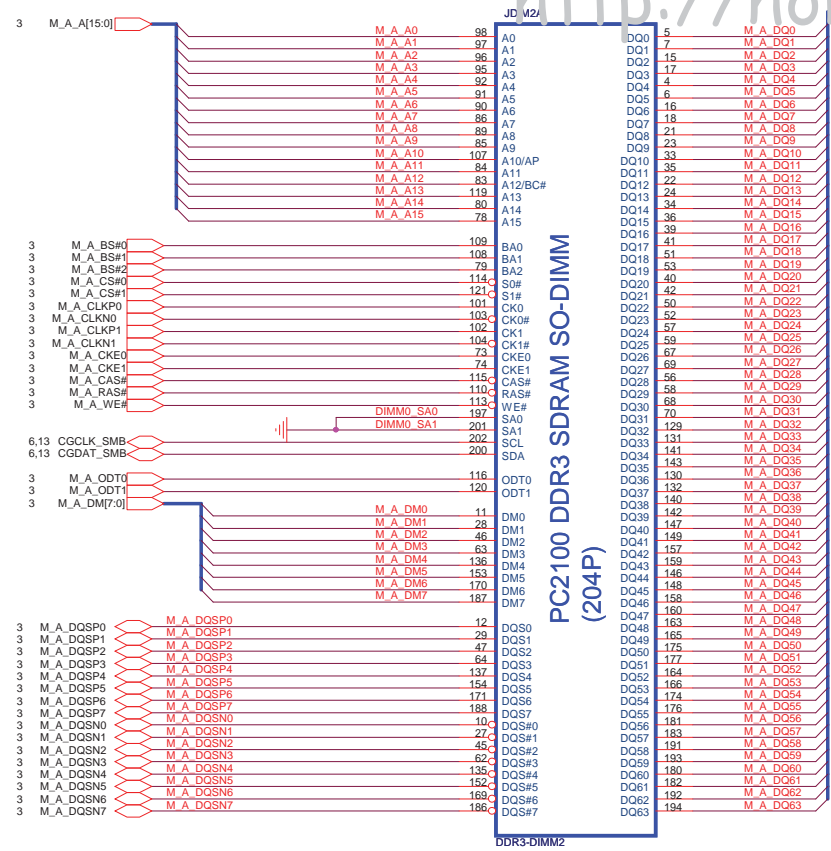
GPIO 0 : Define VAR\_BL & BL\_EN & DIGON H/W or S/W control power up timing  
 Pull Hi for H/W mode  
 ---chip have defined power up timing  
 Pull Low for S/W mode -- APU through DPRX port to program it



## ANALOGIX ANX3110



<b>PROJECT : R23</b> Quanta Computer Inc.		
Size Custom	Document Number ANX3110	Rev 1A
Date: Tuesday, May 03, 2011	Sheet 11 of 40	



13.36 +0.75V\_DDR\_VTT  
 2.3,4,5,13,36,37,39 +1.5VSUS  
 2,4,6,8,9,10,11,13,14,17,20,22,23,24,25,27,28,29,30,34,37,39 +3V

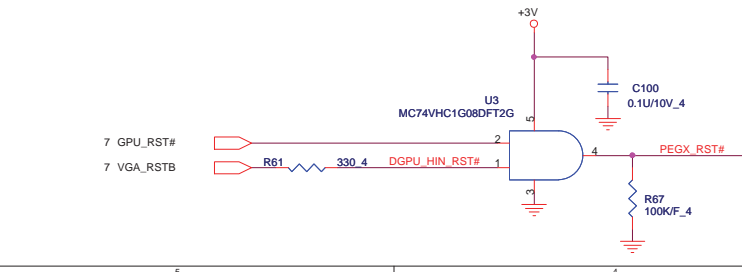
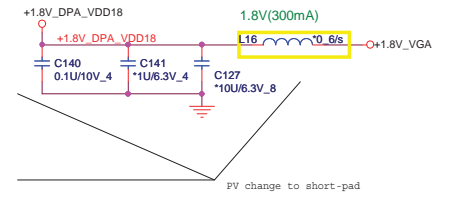
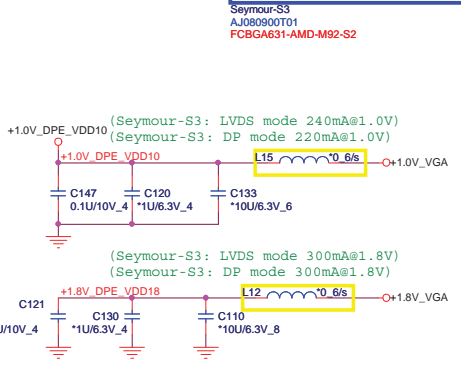
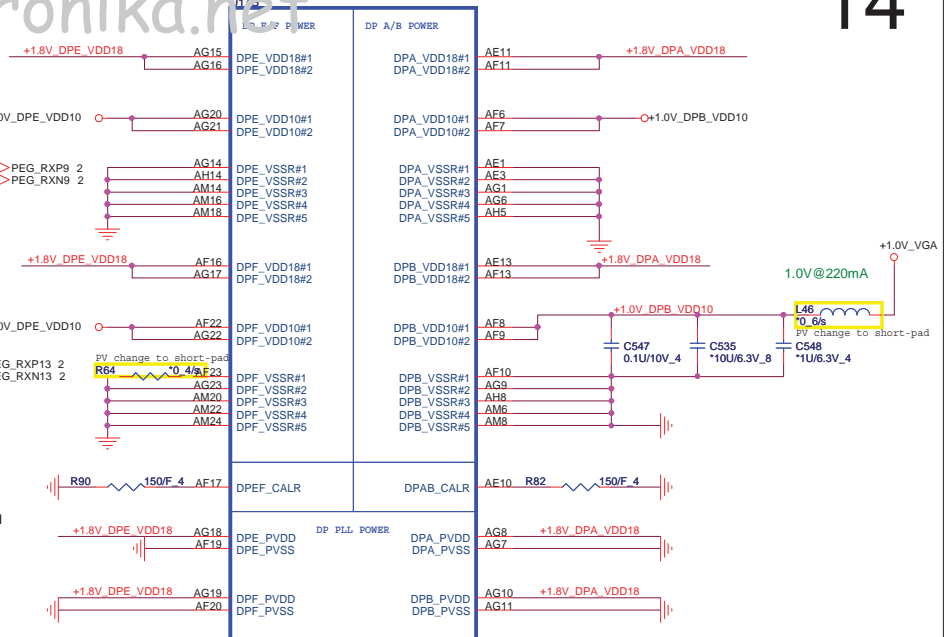
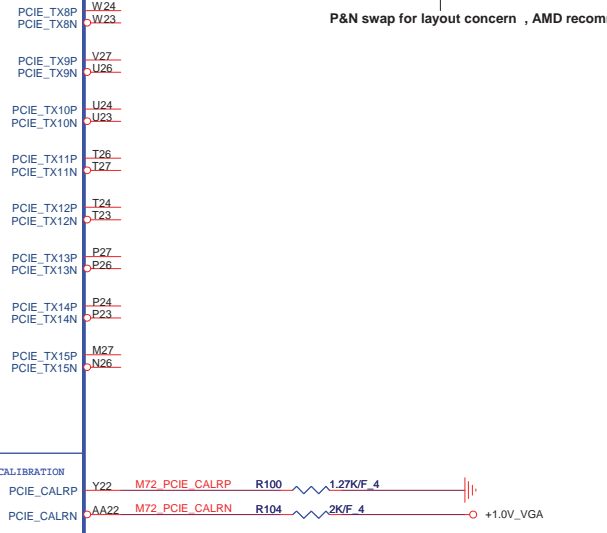
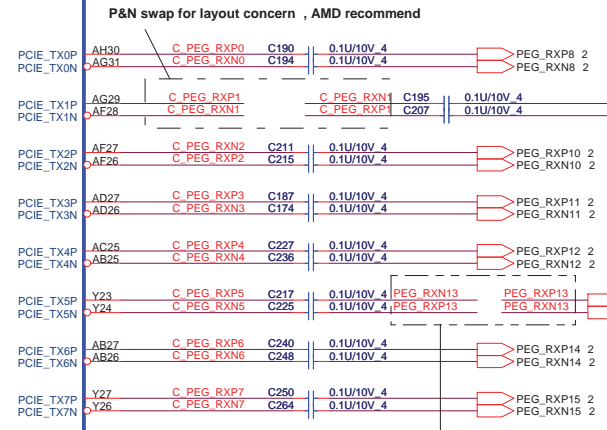
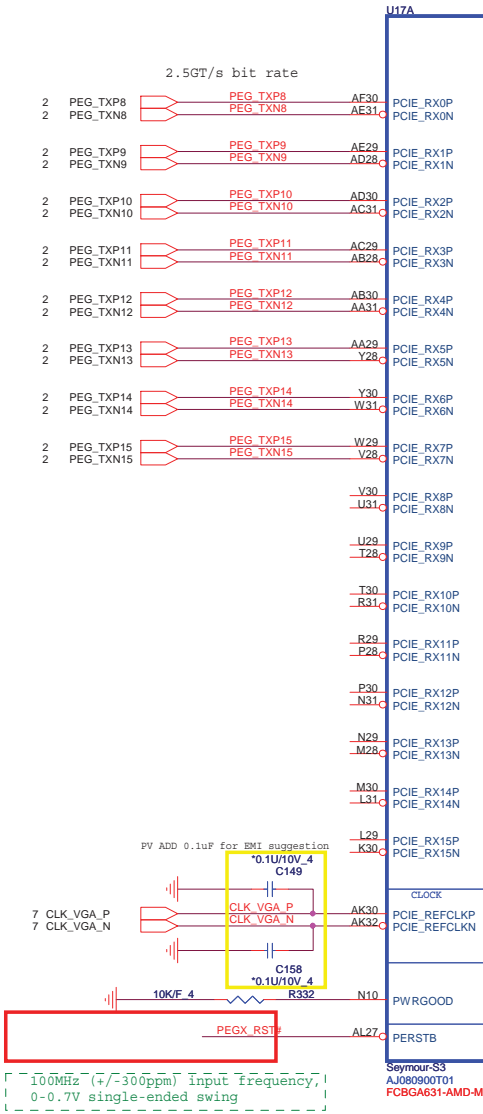
**PROJECT : R23**  
**Quanta Computer Inc.**

Size Custom Document Number **DDR3 DIMM-0** Rev 1A  
 Date: Tuesday, May 03, 2011 Sheet 12 of 40





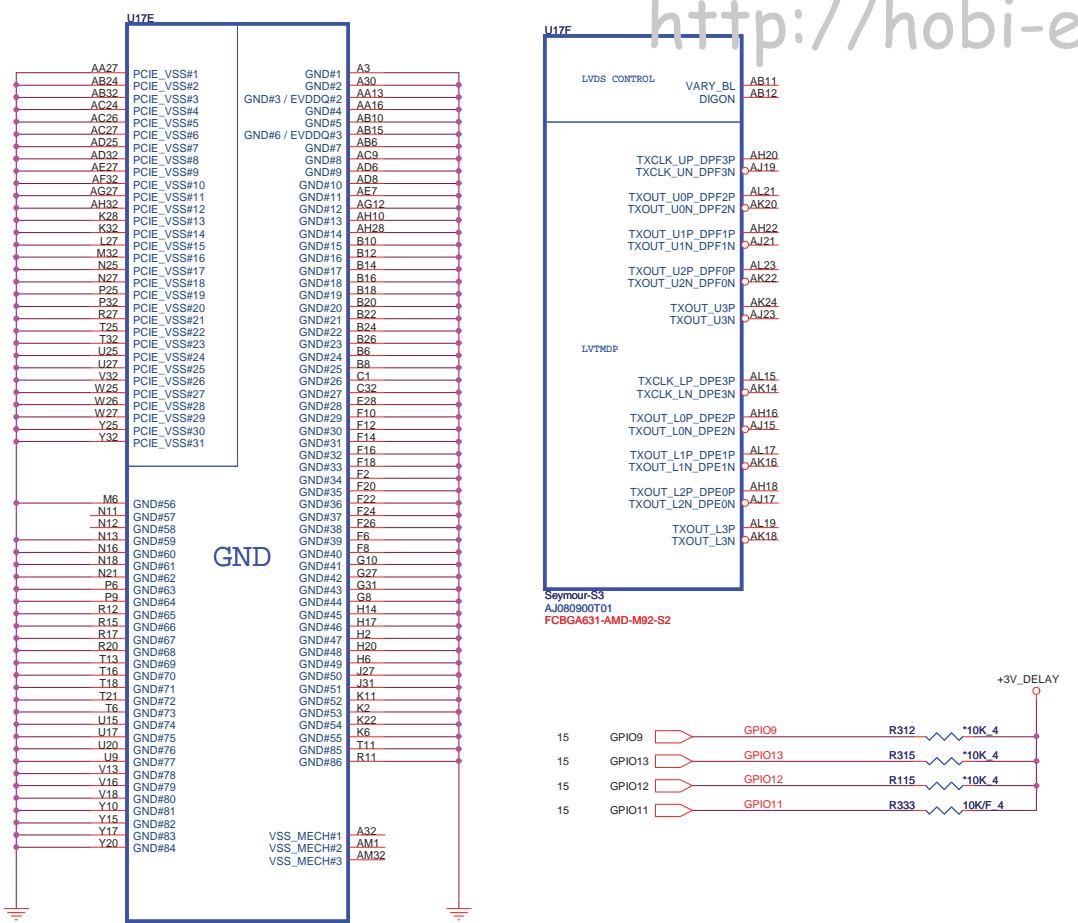
PCI EXPRESS INTERFACE



**PROJECT : R23**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>Seymour-PCIE_Interface</b>	Rev 1A
Date: Tuesday, May 03, 2011		Sheet 14 of 40





### CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
 0= DO NOT INSTALL RESISTOR  
 1= INSTALL 10K RESISTOR  
 X = DESIGN DEPENDANT  
 NA = NOT APPLICABLE

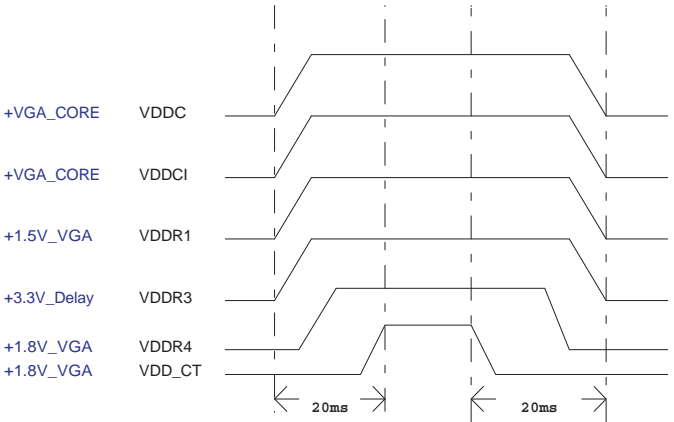
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	<b>Transmitter Power Savings Enable</b> 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	<b>PCI Express Transmitter De-emphasis Enable</b> 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

### AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		

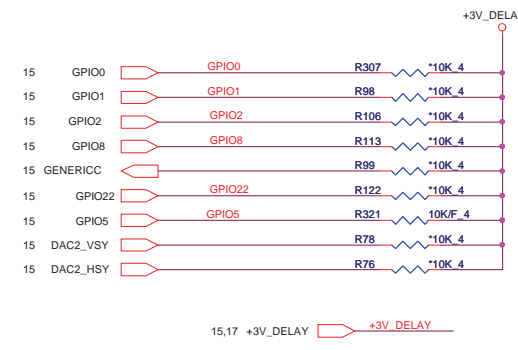
### Power Up/Down Sequence



### Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

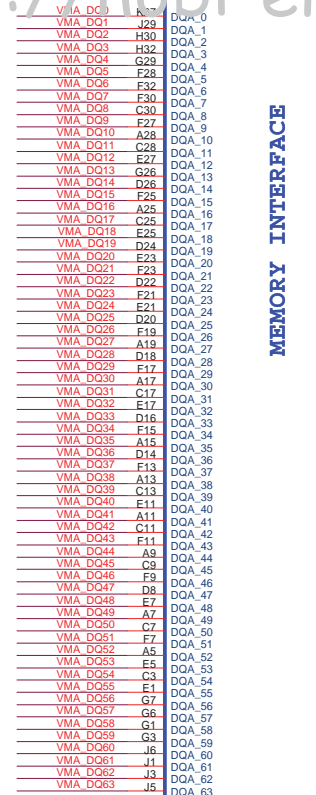
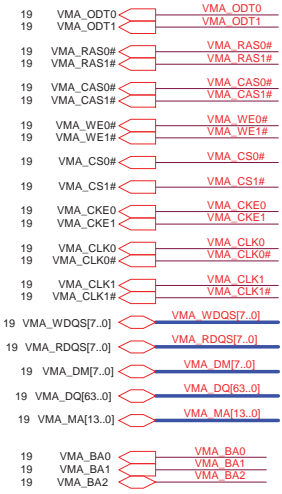
It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.



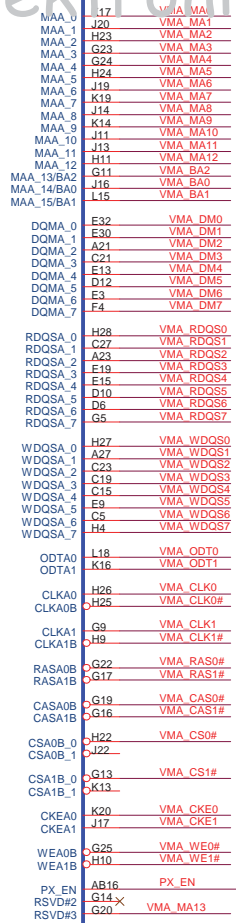
**PROJECT : R23**  
Quanta Computer Inc.

Size Custom	Document Number <b>Seymour GND / LVDS/ Straps</b>	Rev 1A
Date: Tuesday, May 03, 2011	Sheet 16	of 40



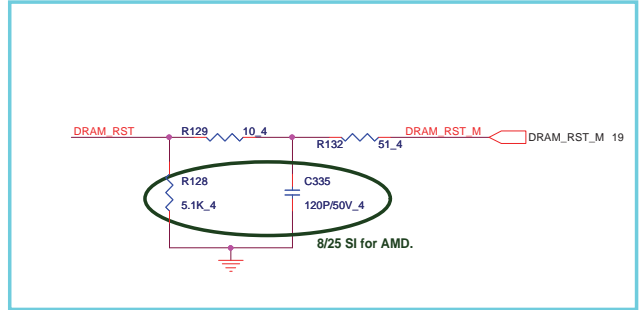
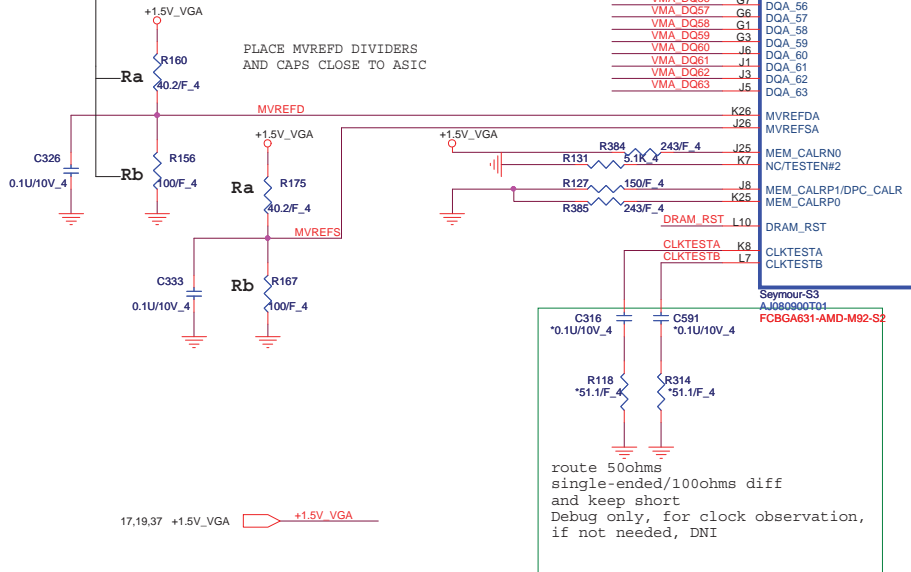


MEMORY INTERFACE



support 1Gbit  
VRAM ( 64M X 16 )

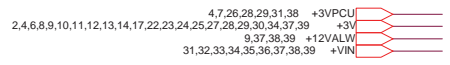
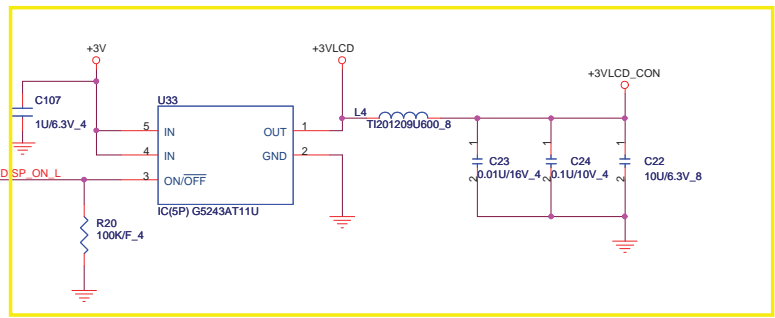
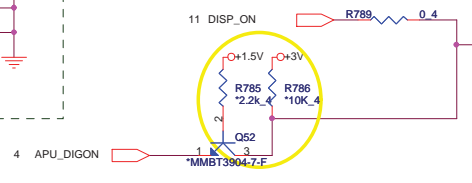
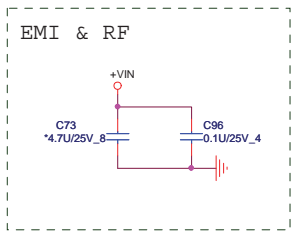
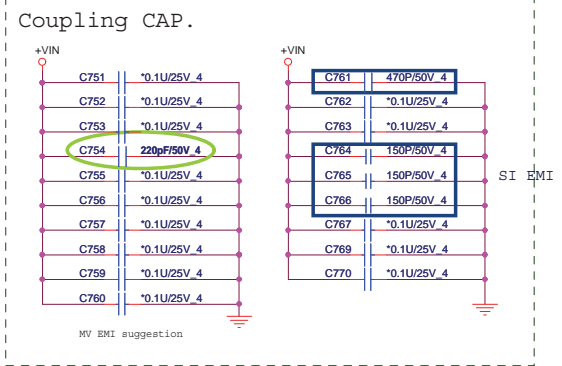
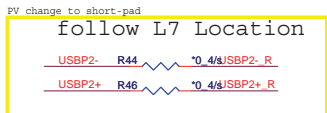
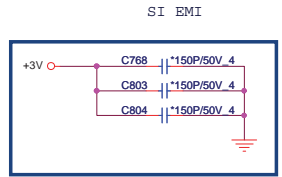
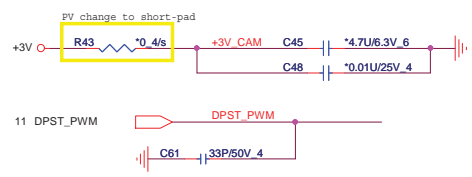
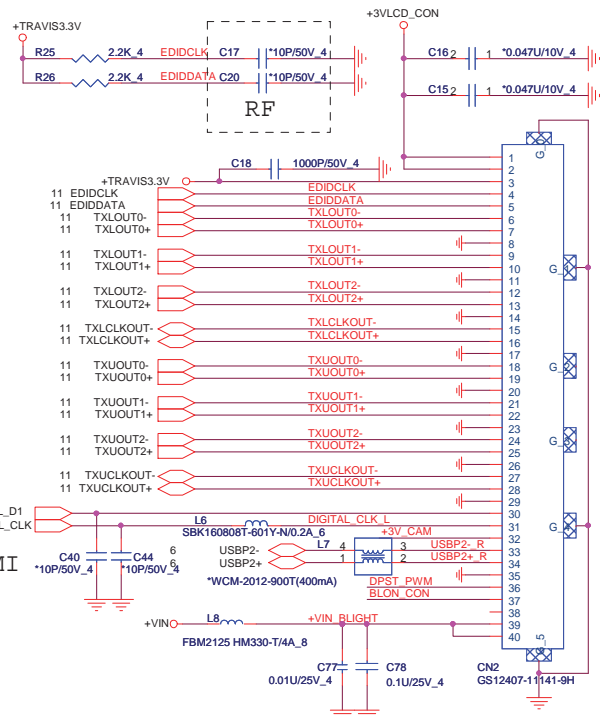
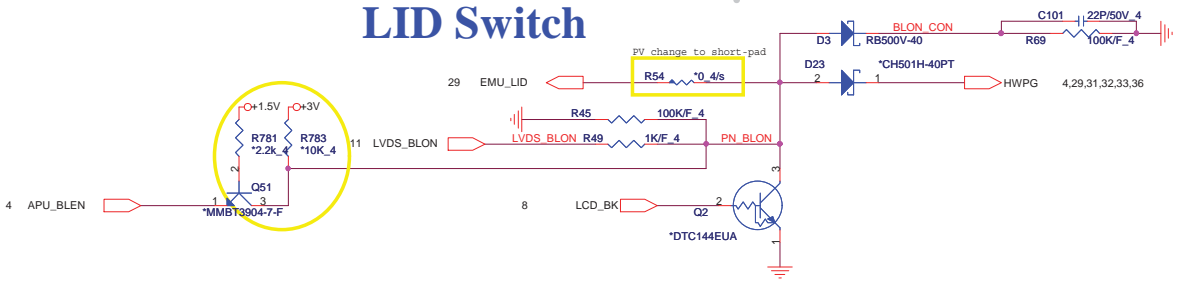
DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R







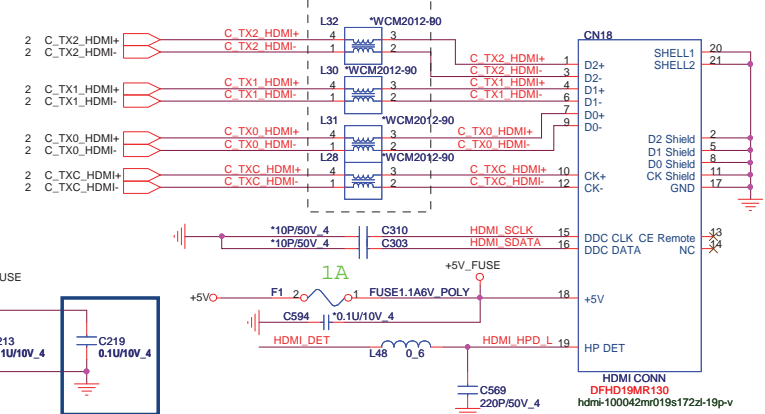
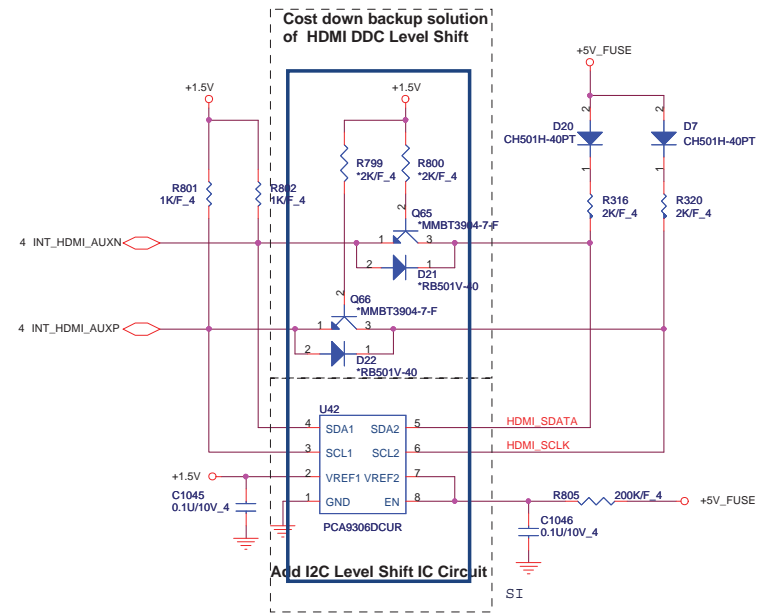
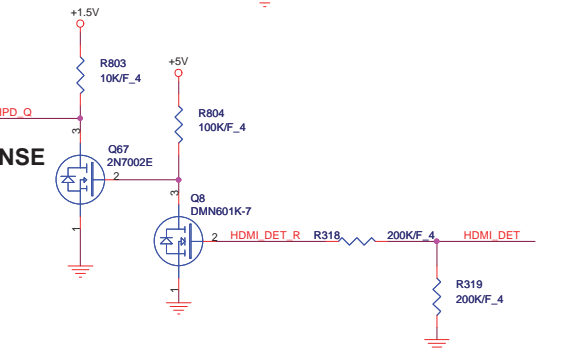
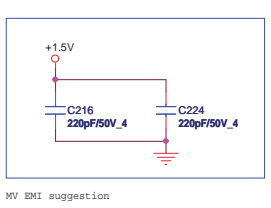
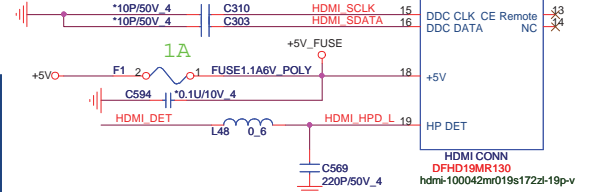
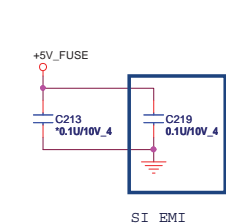
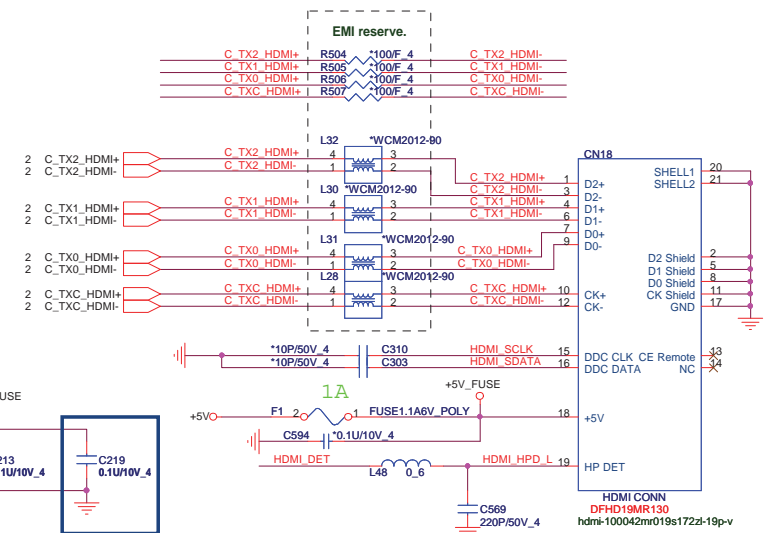
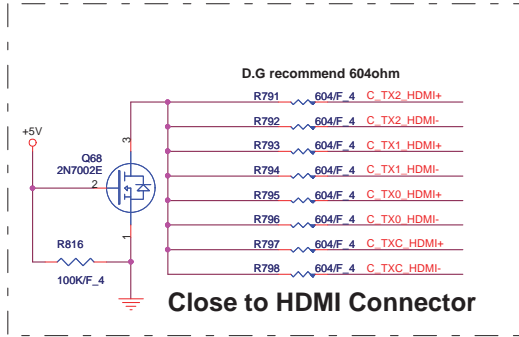
# LID Switch

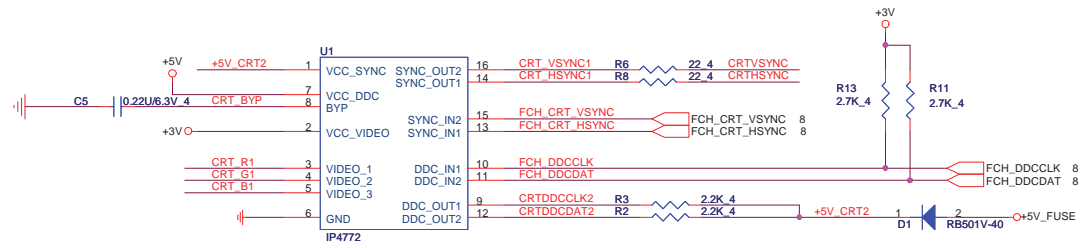
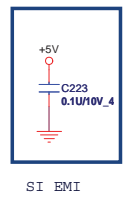
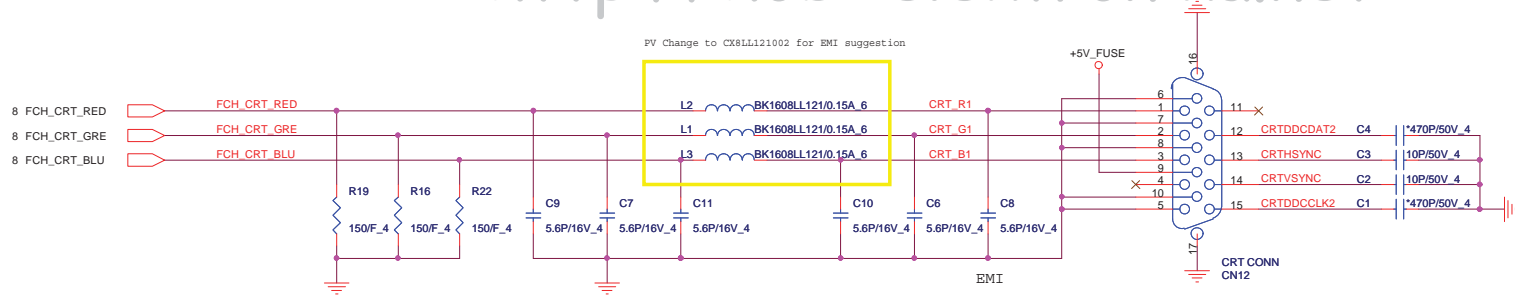


**PROJECT : R23**  
**Quanta Computer Inc.**

Size Custom Document Number LCD CONN/LID/CAM Rev 1A

Date: Tuesday, May 03, 2011 Sheet 20 of 40

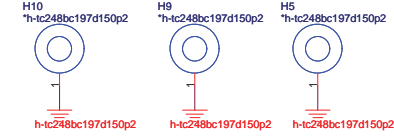
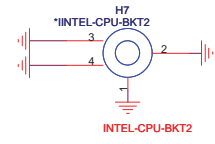
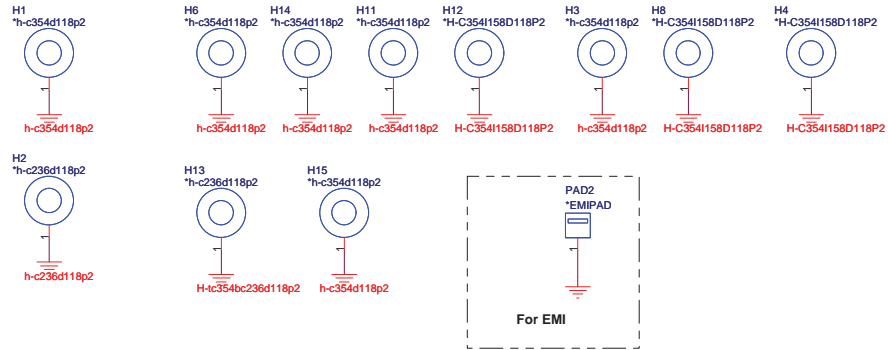




HOLE

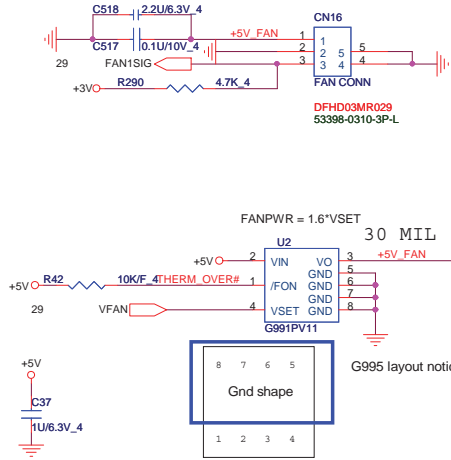
CPU

VGA

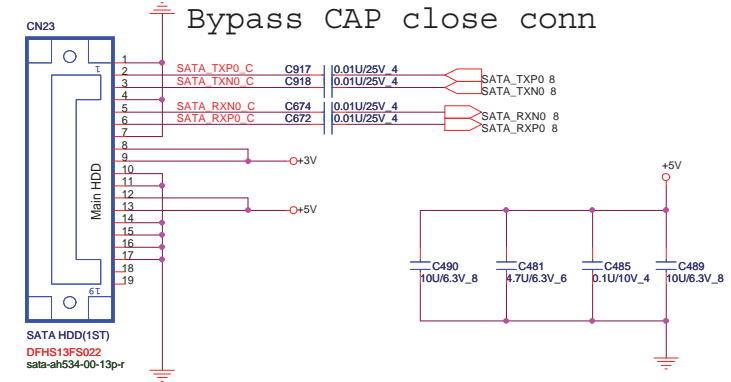


	<b>PROJECT : R23</b>		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number CRT,Hole	
Date: Tuesday, May 03, 2011		Sheet 22 of 40	

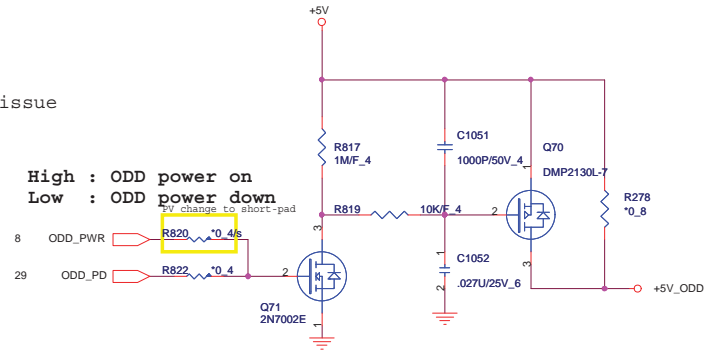
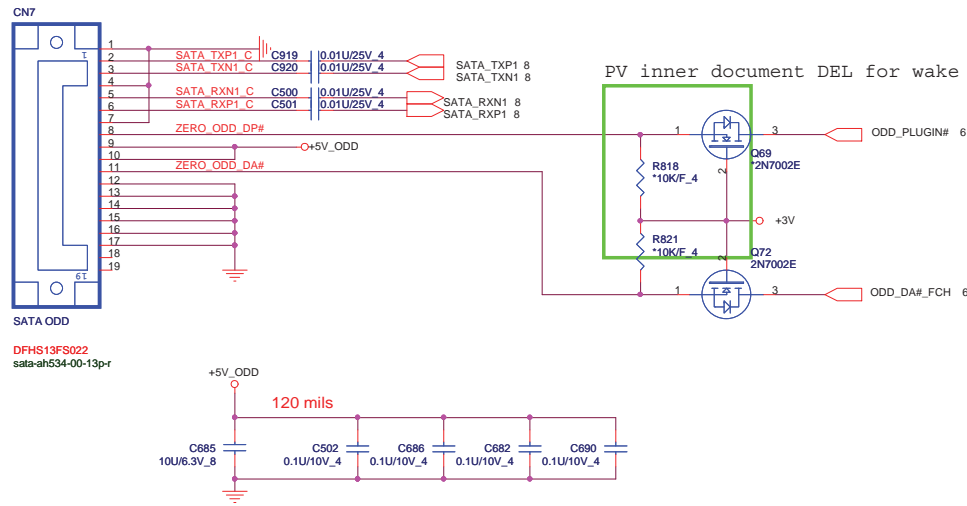
# CPU FAN



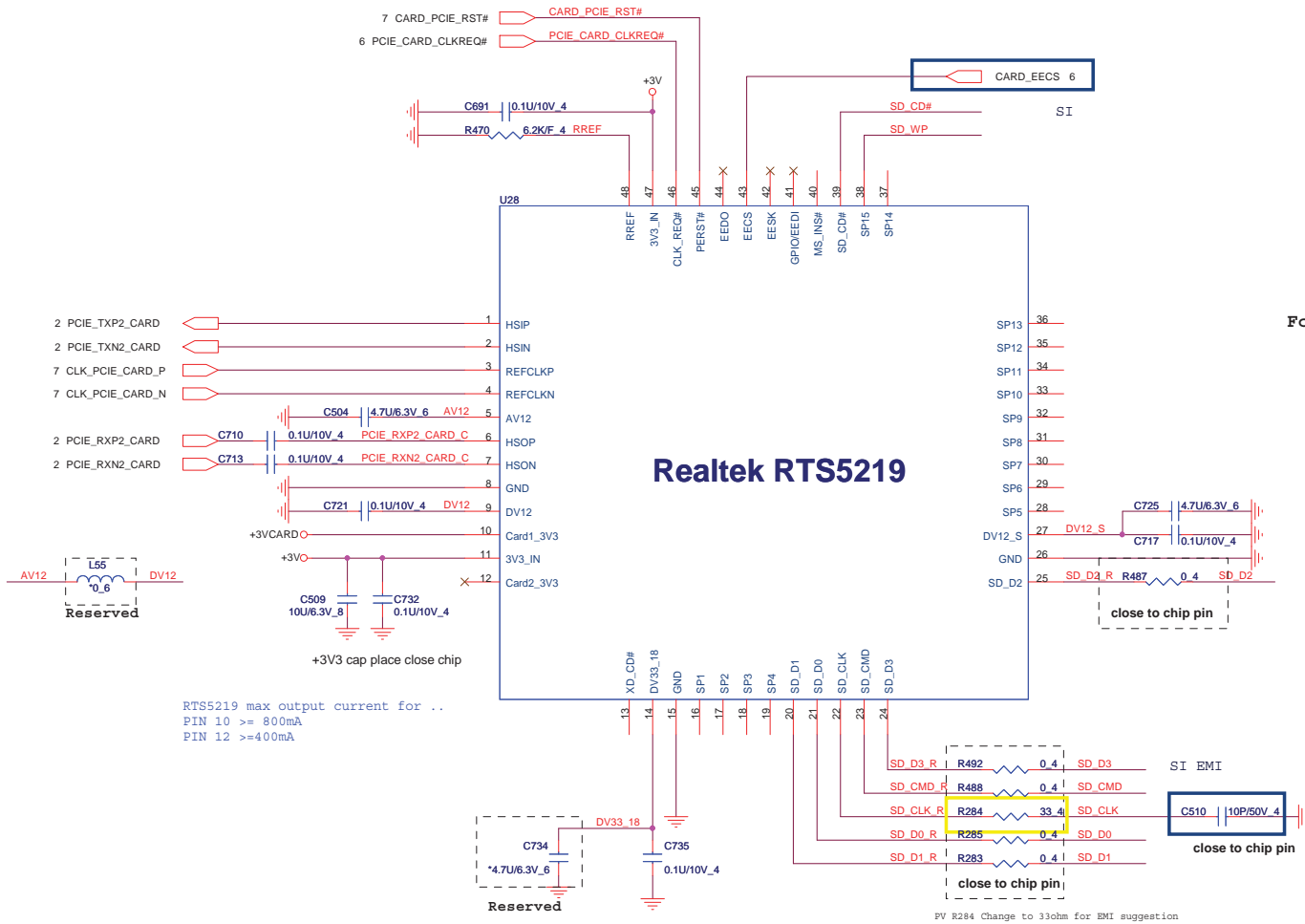
# SATA HDD CONNECTOR



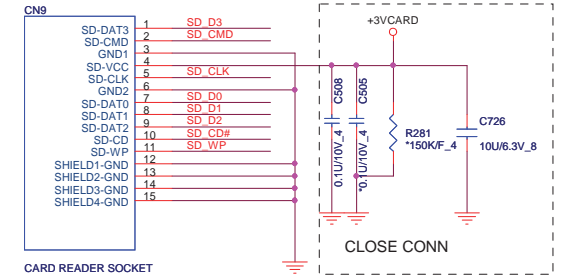
# SATA ODD CONNECTOR SATA ODD








Footprint lqfp48-9x9-5-1\_6h

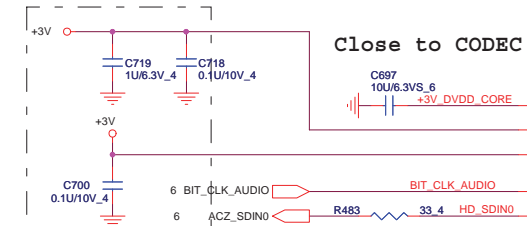


PV R284 Change to 33ohm for EMI suggestion

			<b>PROJECT : R23</b>	
			Quanta Computer Inc.	
Size Custom	Document Number <b>RTS5219 &amp; CR SOCKET &amp; HOLE</b>	Rev 1A		
Date: Tuesday, May 03, 2011		Sheet 24	of 40	

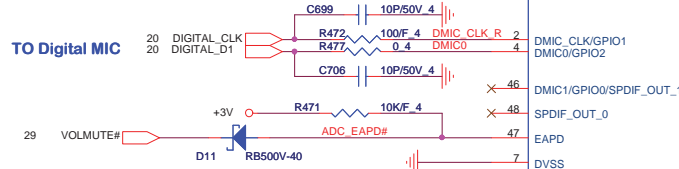
2,4,6,8,9,10,11,12,13,14,17,20,22,23,24,27,28,29,30,34,37,39 +3V  
8,11,17,21,22,23,28,30,39 +5V

Close to CODEC

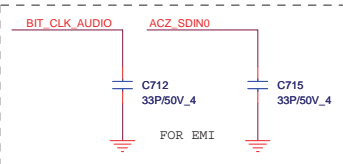
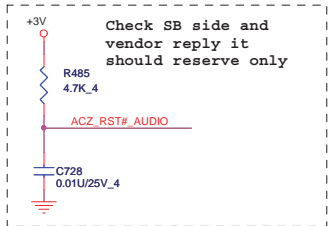


HDA Bus

TO Digital MIC



Close to CODEC

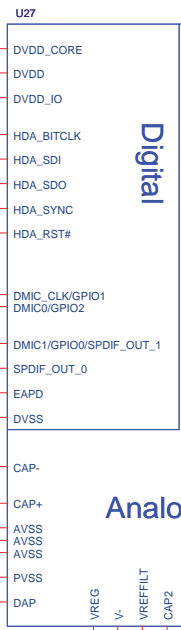


Close to CODEC

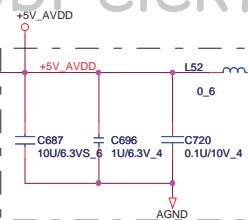


Digital

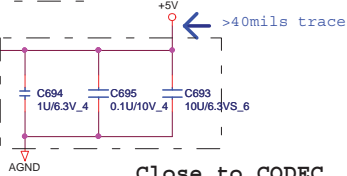
Analog



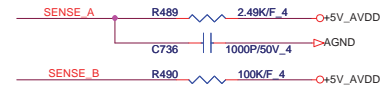
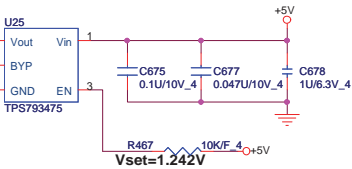
>40mils trace



Close to CODEC



Close to CODEC



>40mils trace

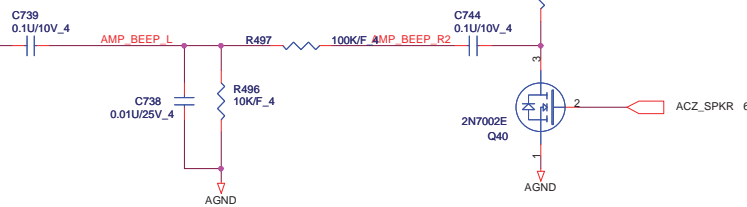
TO Headphone jack

TO Headphone jack

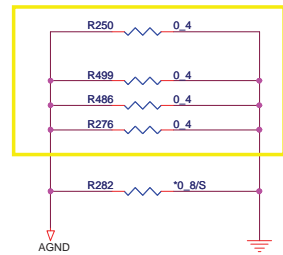
TO Audio Jack MIC

TO Internal Speakers

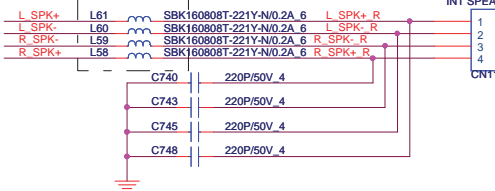
TO Internal Speakers



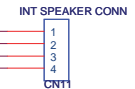
PV ADD 0ohm for EMI suggestion



EMI Request



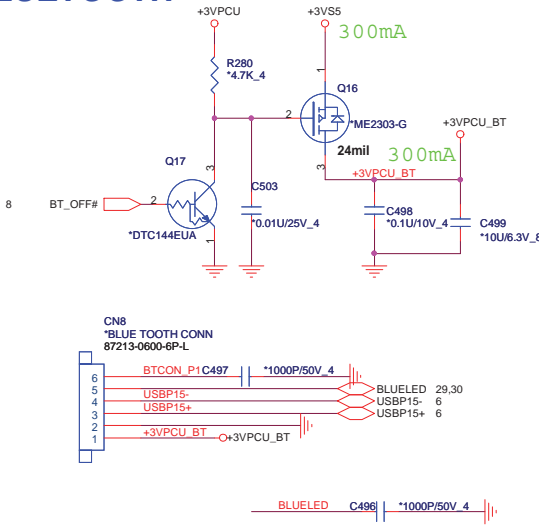
INT. SPEAKER



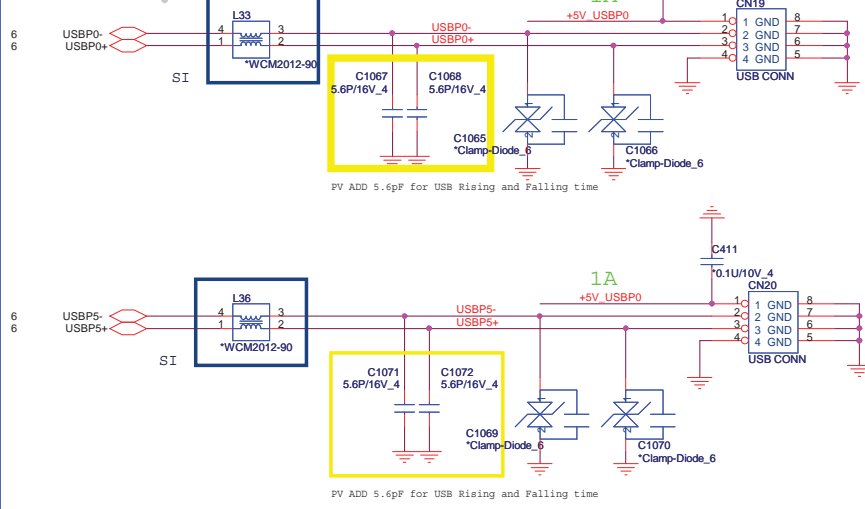
**PROJECT : R23**  
Quanta Computer Inc.

Size Custom	Document Number Azalia 92HD80	Rev 1A
Date: Tuesday, May 03, 2011		Sheet 25 of 40

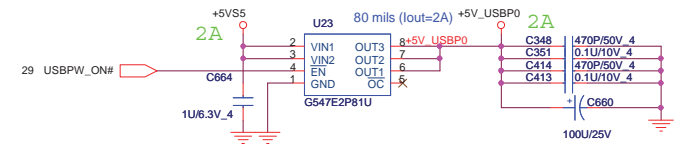
# BLUETOOTH



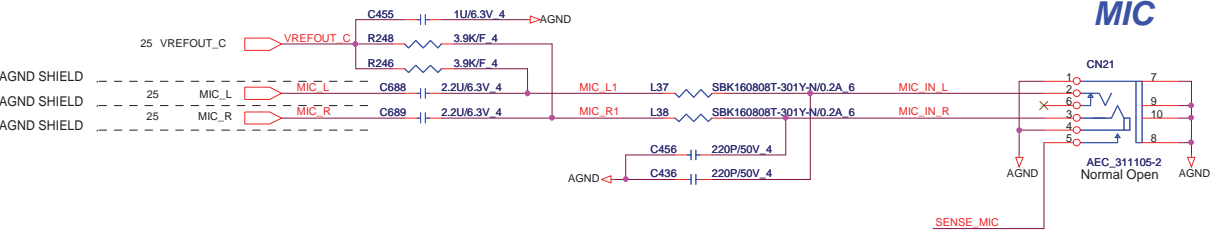
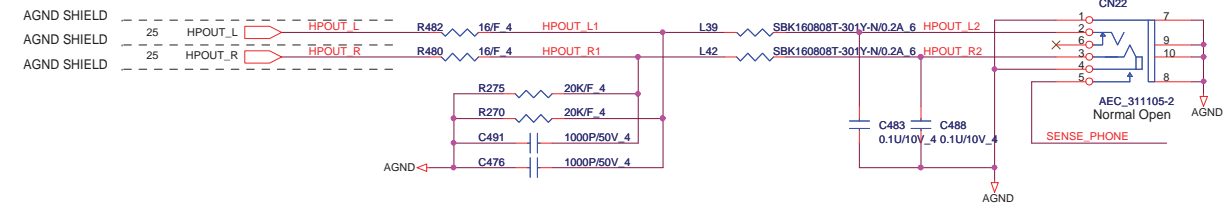
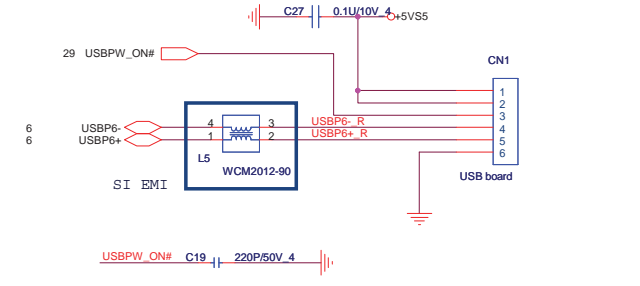
<http://hobi-elektronika.net>



# LEFT SIDE USB2



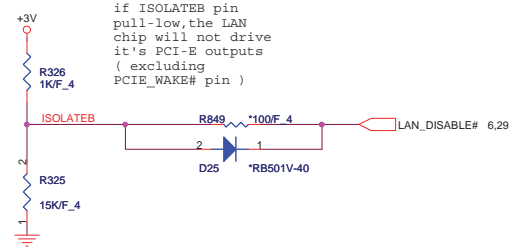
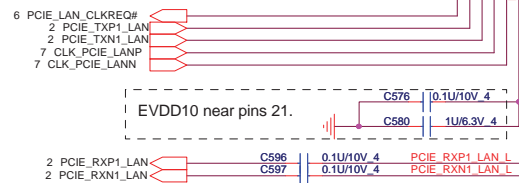
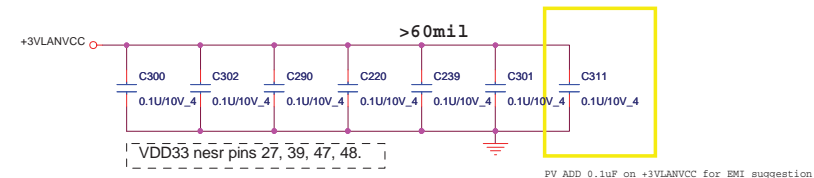
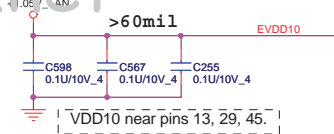
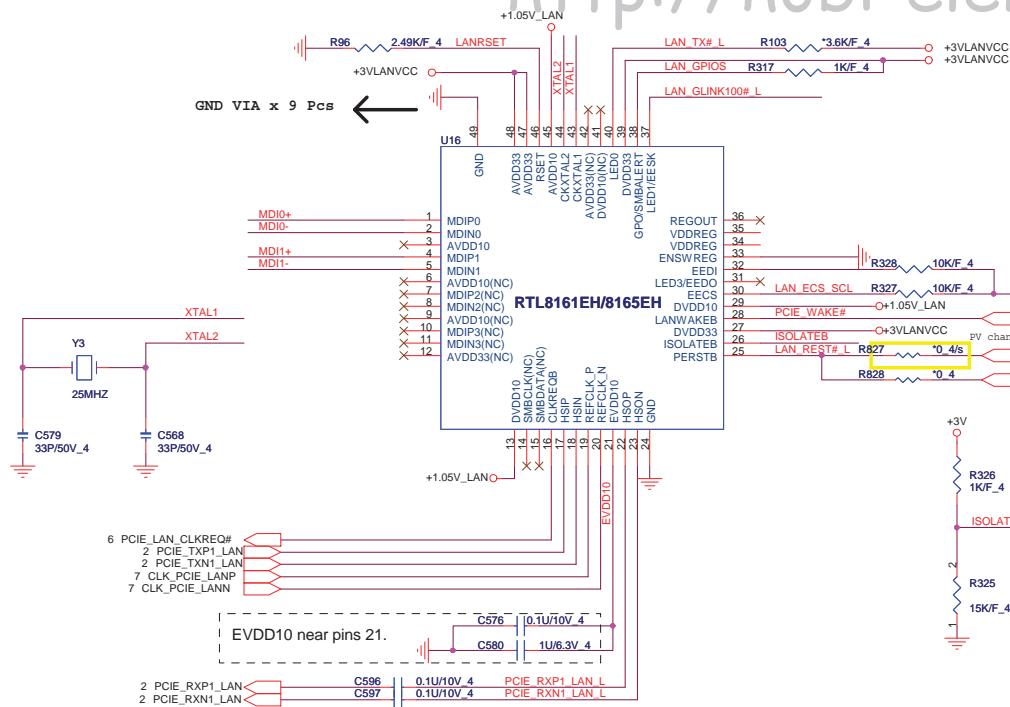
# Right SIDE USB1



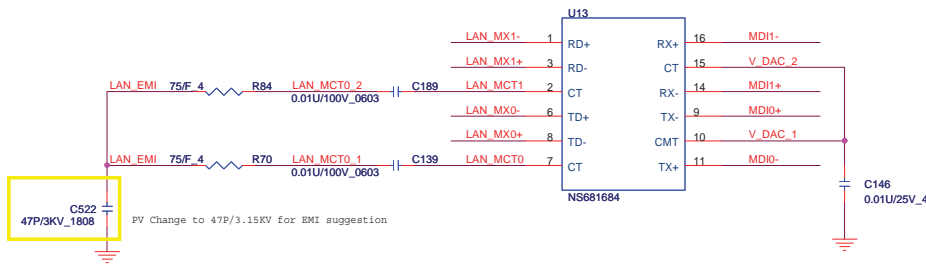
# Line out

# MIC

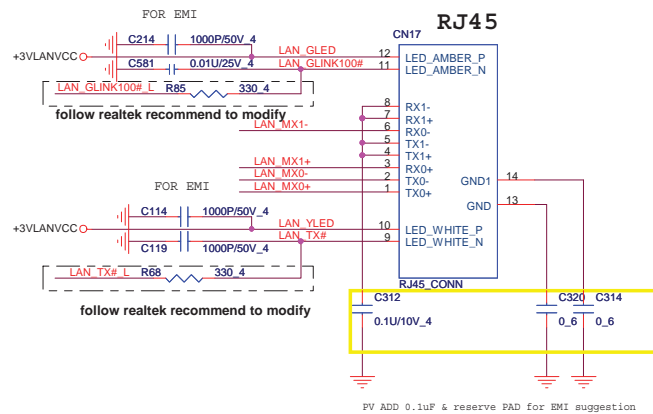
<b>PROJECT : R23</b> <b>Quanta Computer Inc.</b>		
Size Custom	Document Number <b>USB/BT/Audio Jack</b>	Rev 1A
Date: Tuesday, May 03, 2011	Sheet 26	of 40



### Transformer for 10/100



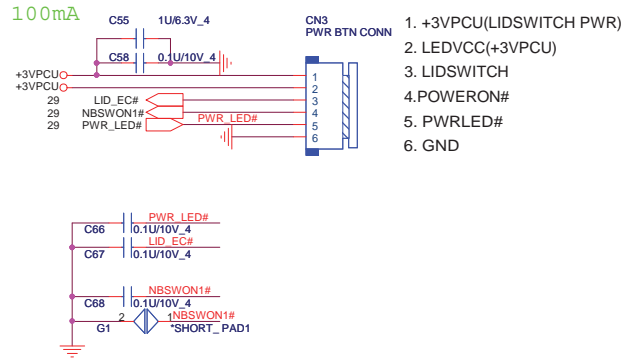
### Lan Con.



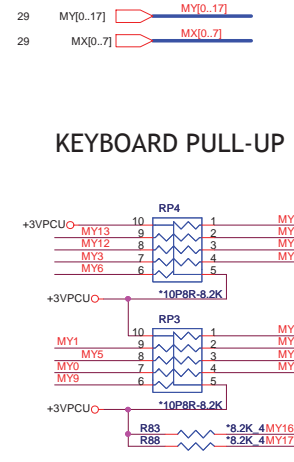
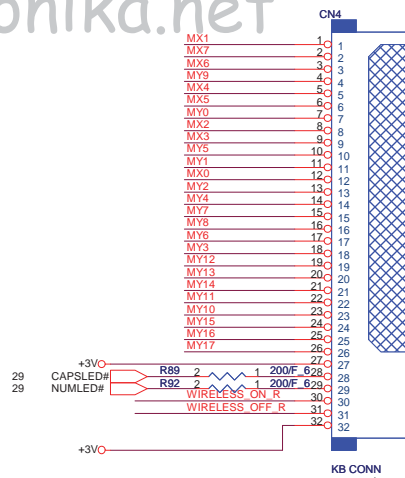
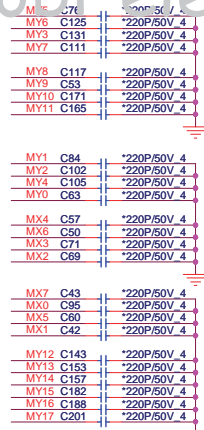
			<b>PROJECT : R23</b>		
			Quanta Computer Inc.		
Size Custom	Document Number	Rev			
	<b>RTL8165EH</b>	1A			
Date: Tuesday, May 03, 2011	Sheet 27	of 40			



# POWER BOTTON CONNECT



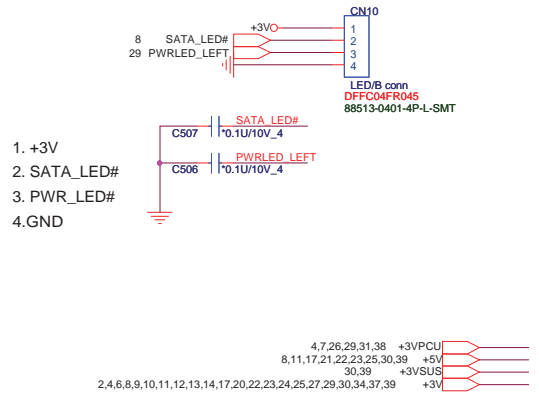
# KEYBOARD Con.



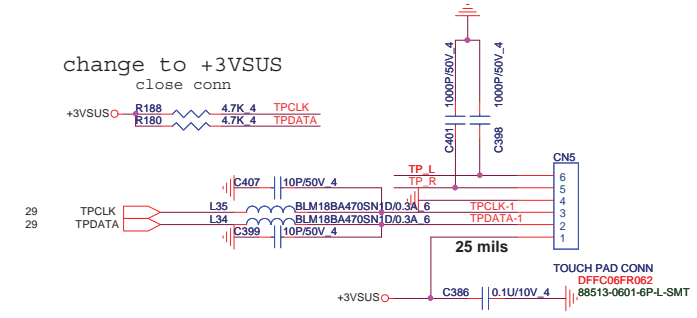
EC KB3930 has included K/B pull-up resistor and function



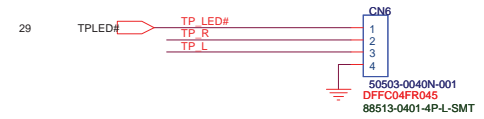
# LED Con.



# TOUCH PAD Con.

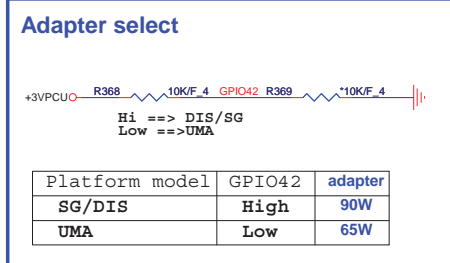
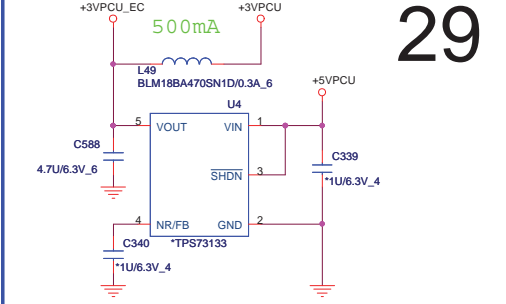
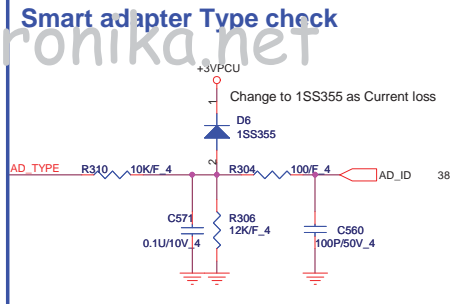
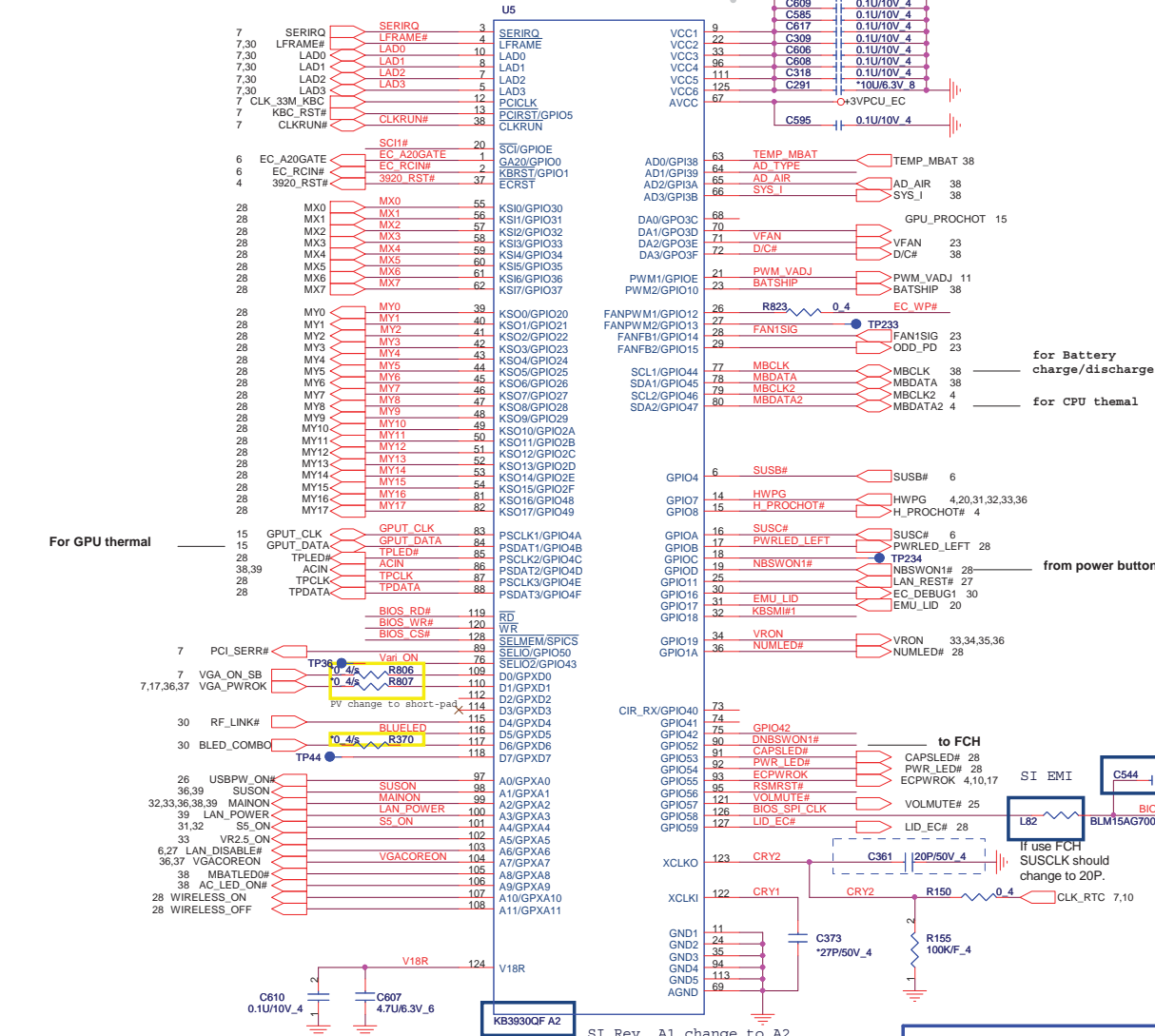


# To TOUCH PAD SW board

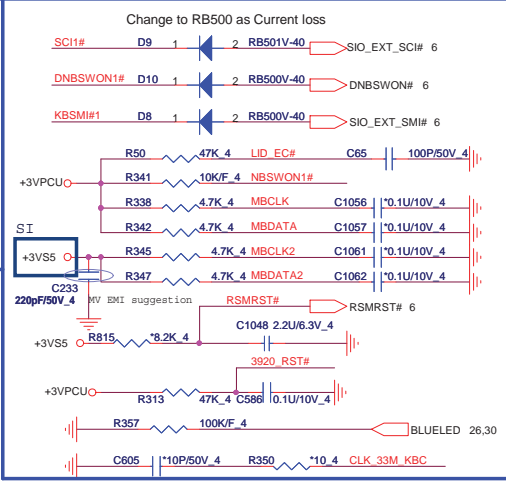


**PROJECT : R23**  
Quanta Computer Inc.

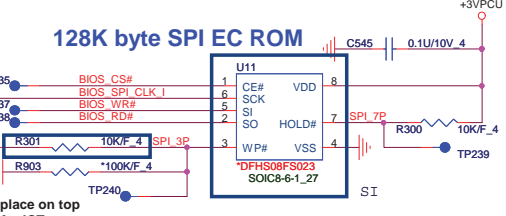
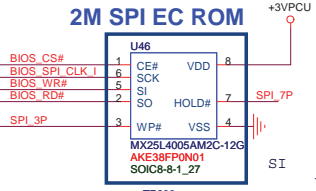
Size Custom	Document Number <b>LED/KB/SW/TP</b>	Rev 1A
Date: Tuesday, May 03, 2011   Sheet 28 of 40		



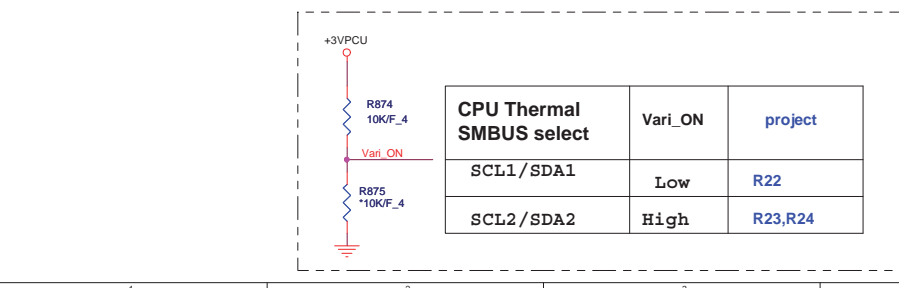
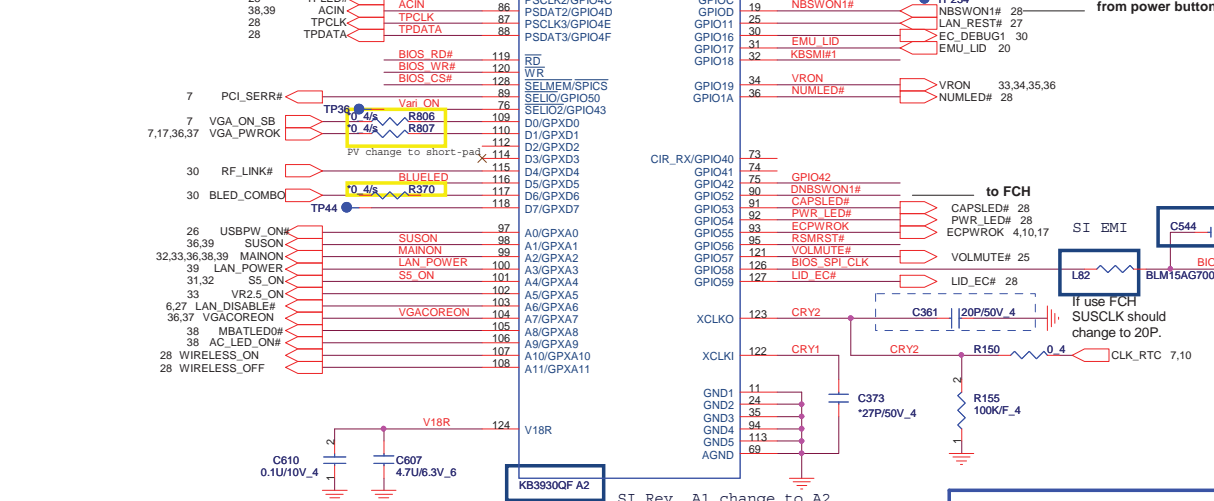
Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W



Vender	Size	P/N
AMIC	128 K	AKE35ZN0801
EON	128 K	AKE35FN0Q00
Socket		DFHS08FS023

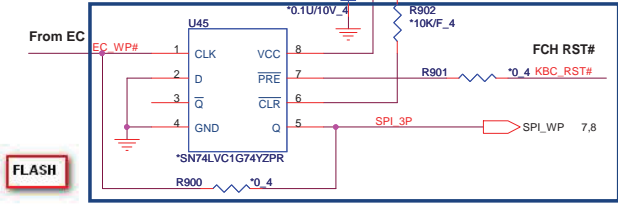


For GPU thermal



CPU Thermal SMBUS select	Vari_ON	project
SCL1/SDA1	Low	R22
SCL2/SDA2	High	R23,R24

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (1)	H (1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	Q̄ <sub>0</sub>



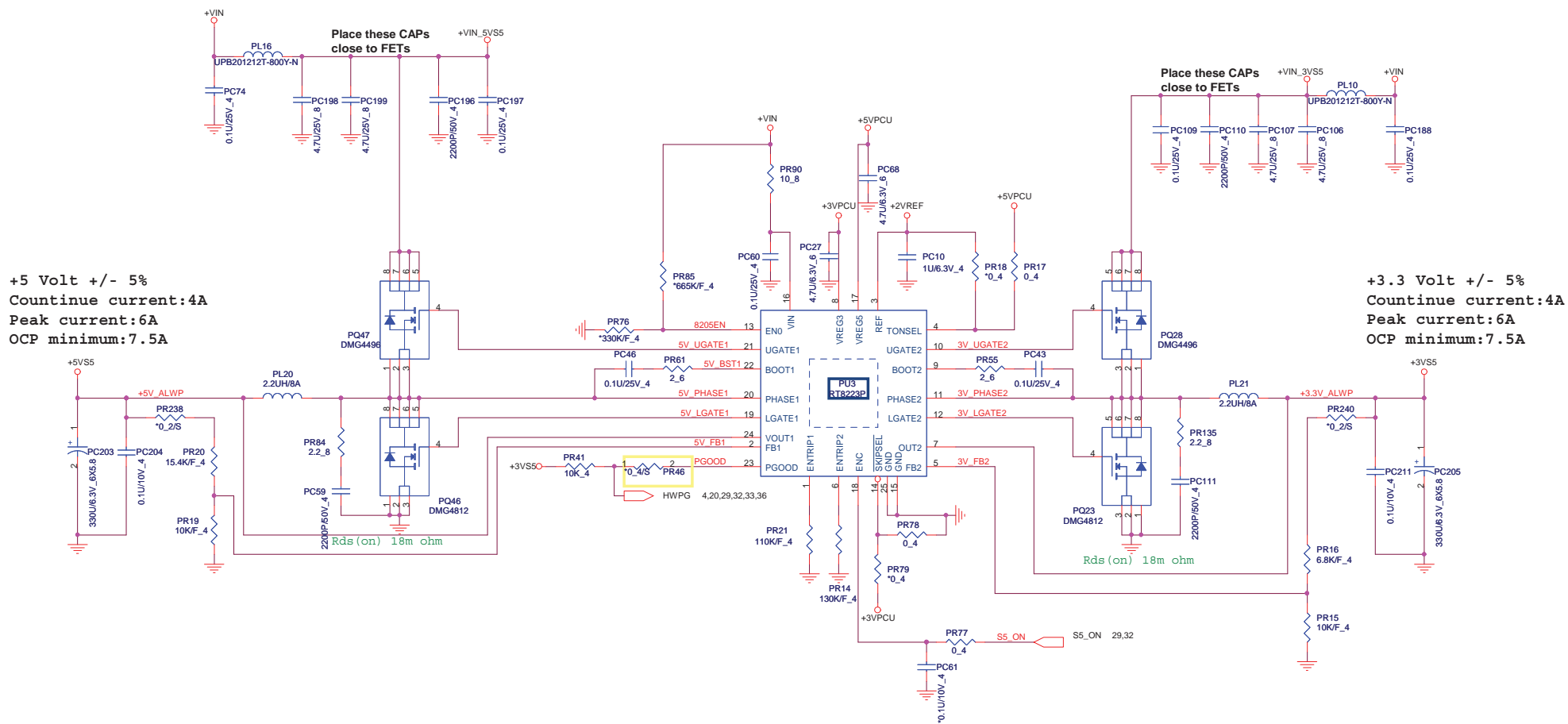
**PROJECT : R23**  
Quanta Computer Inc.


Size Custom    Document Number EC (KB3926)/ROM    Rev 1A

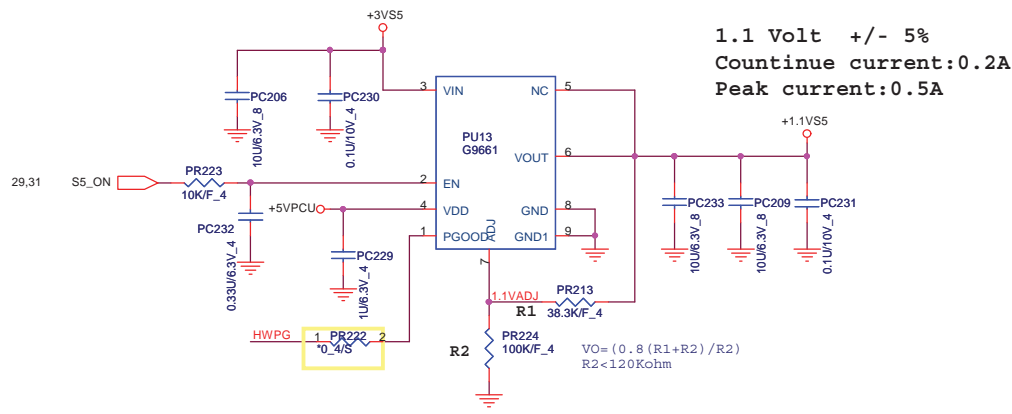
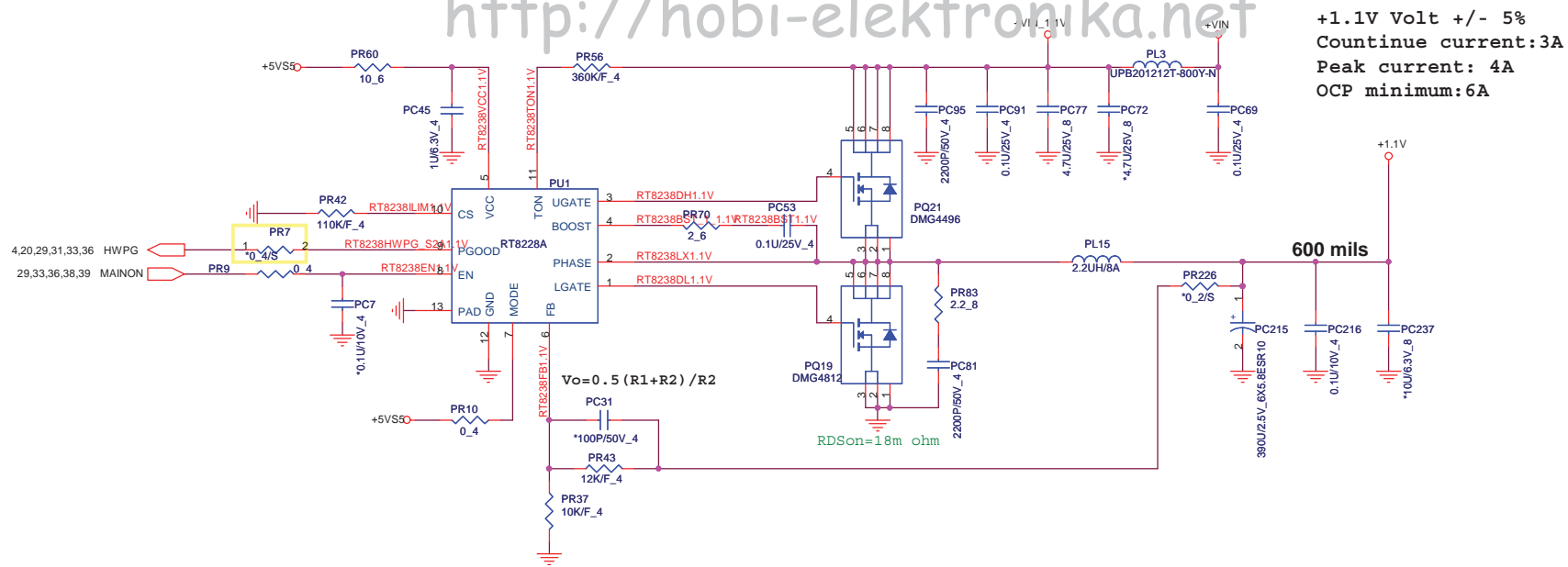
Date: Tuesday, May 03, 2011    Sheet 29 of 40

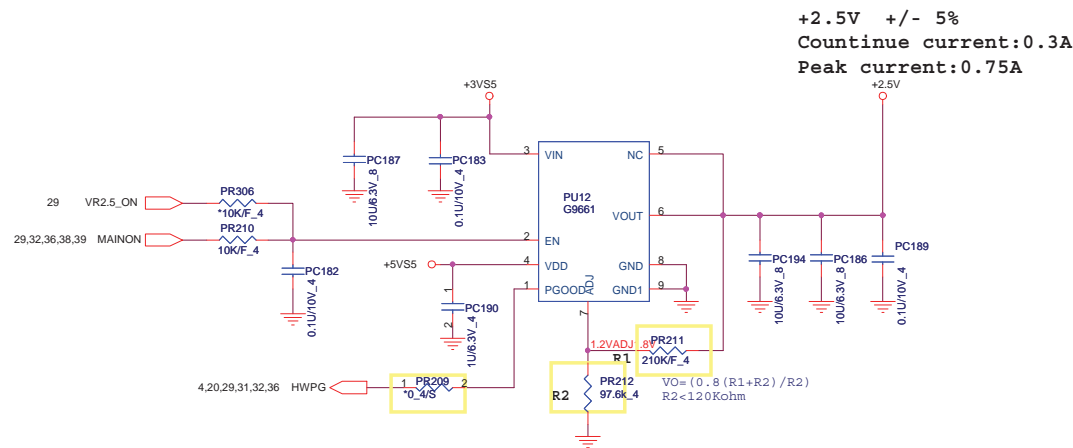
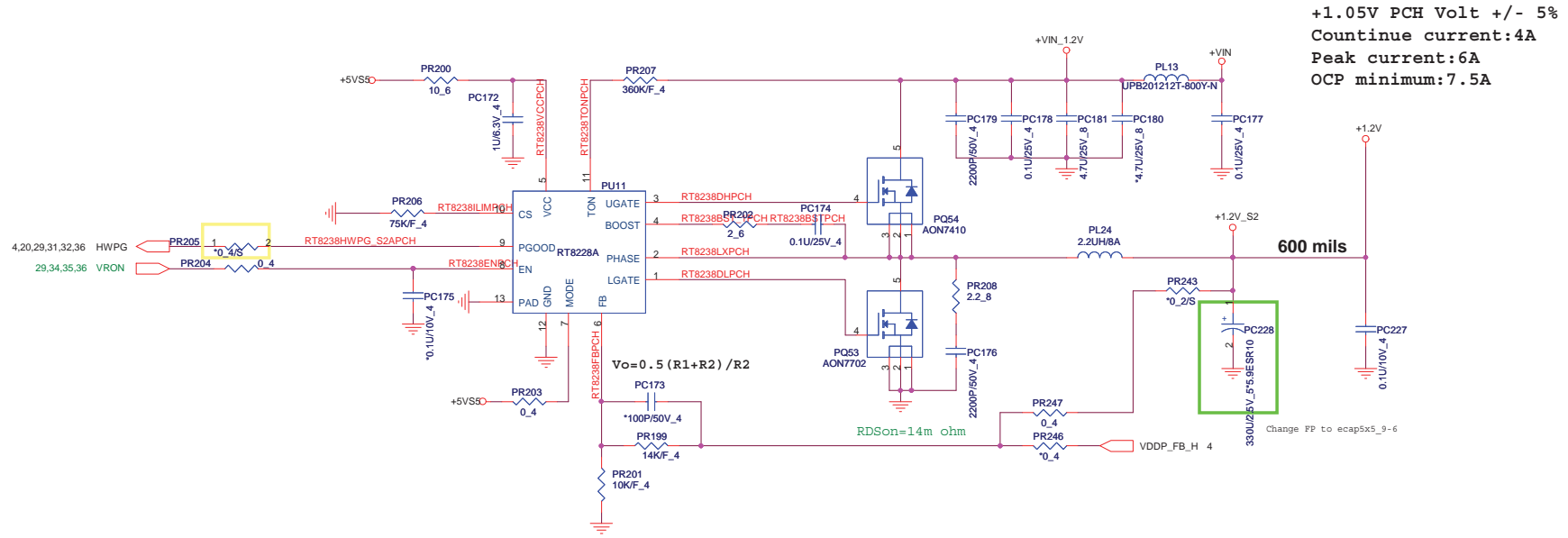





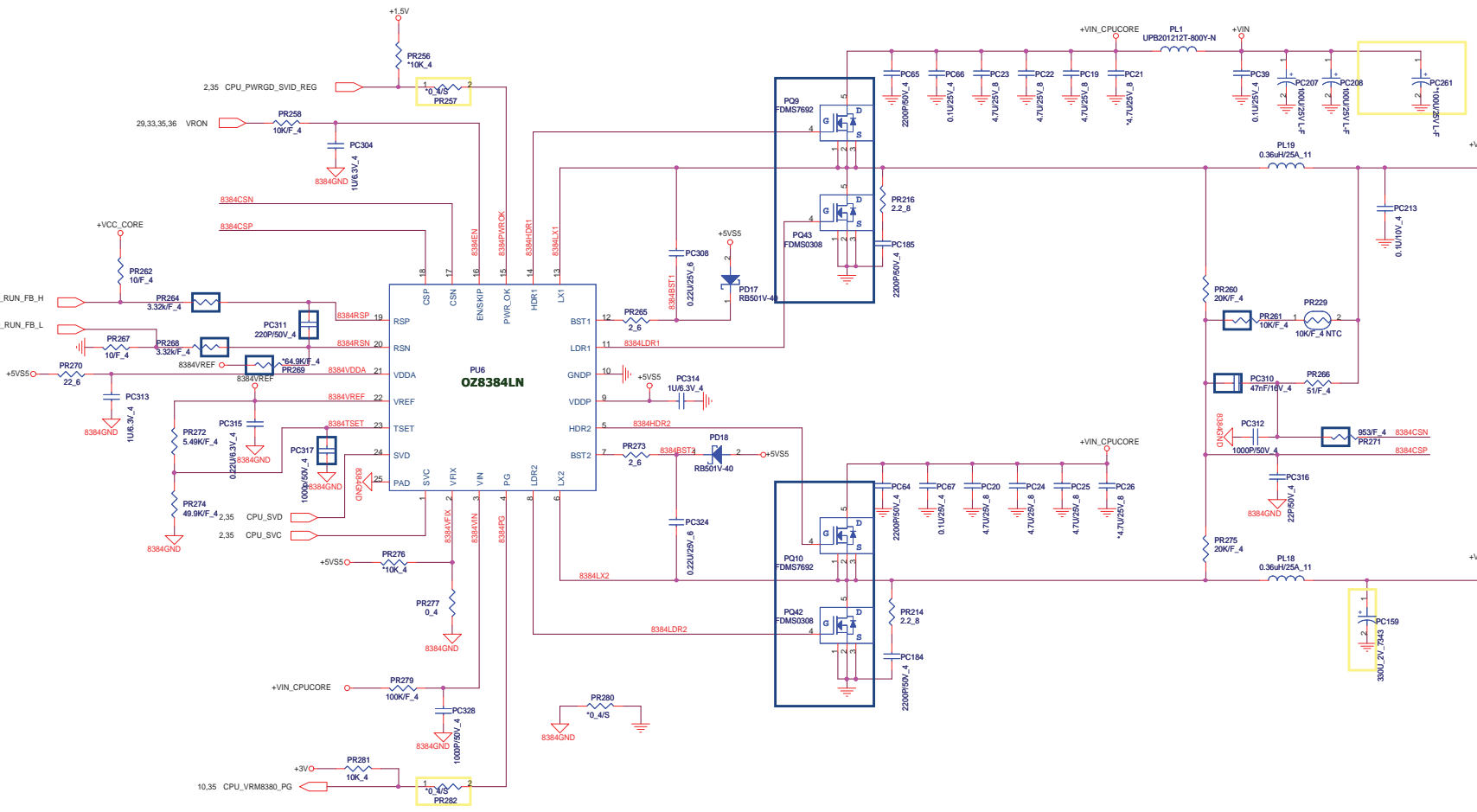


			<b>PROJECT : R23</b>	
			Quanta Computer Inc.	
Size Custom	Document Number <b>+5V/+3V (RT8206B)</b>	Rev 1A		
Date: Tuesday, May 03, 2011	Sheet 31	of	40	



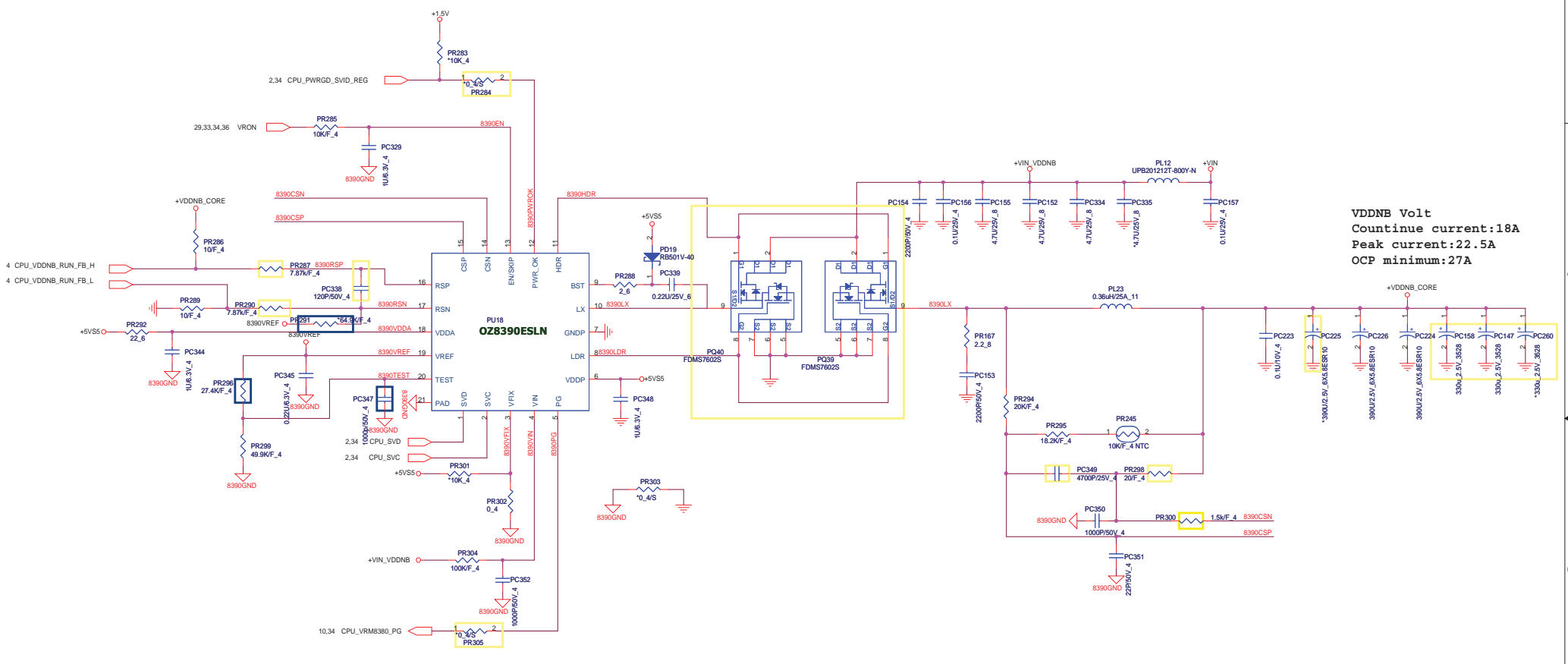


 <b>PROJECT : R23</b> <b>Quanta Computer Inc.</b>		



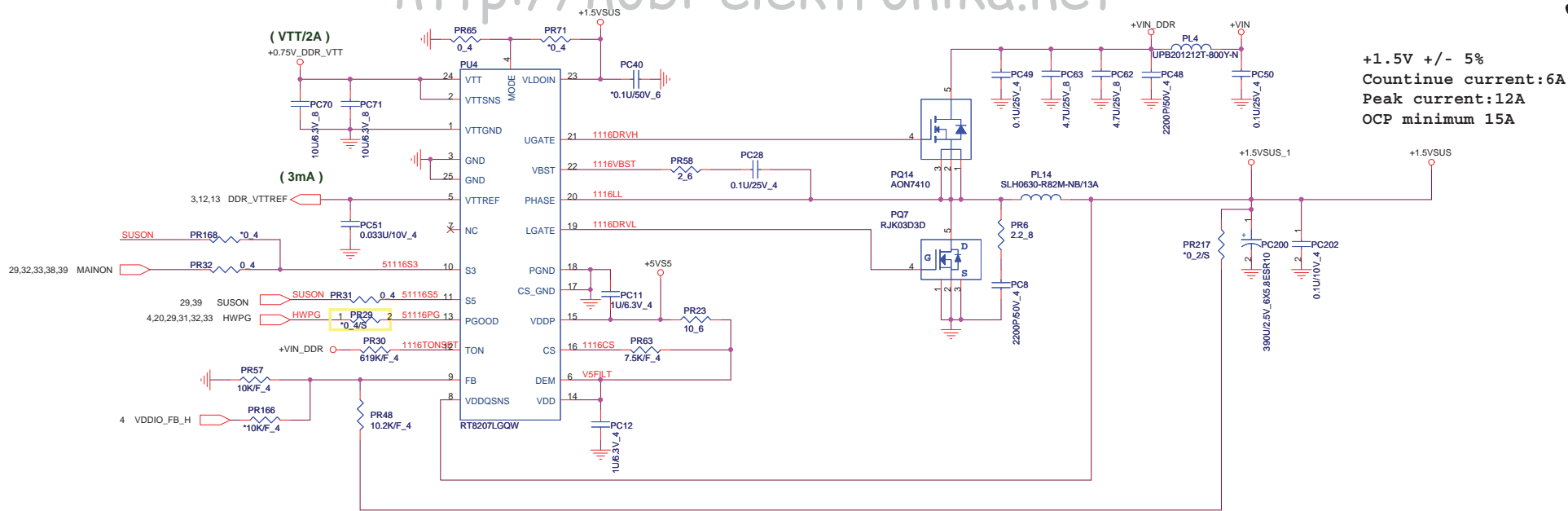
CPU CORE Volt  
Countinue current:36A  
Peak current:50A  
OCP minimum:55A

Change FP to ecapp5t\_9-6

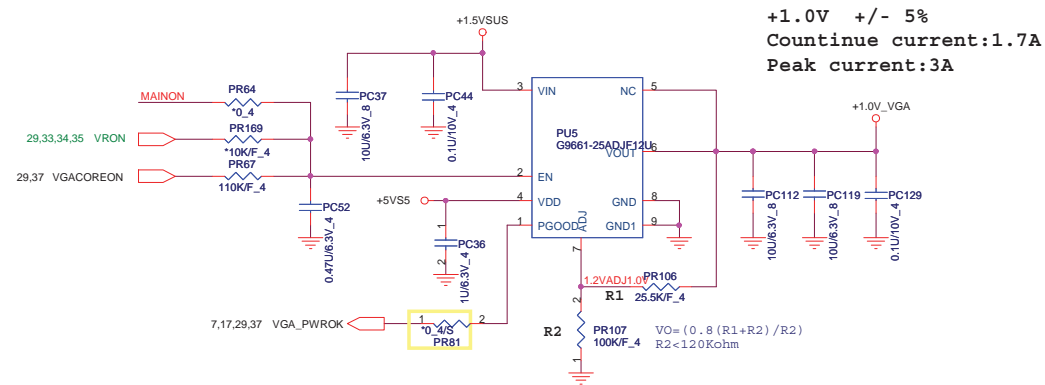
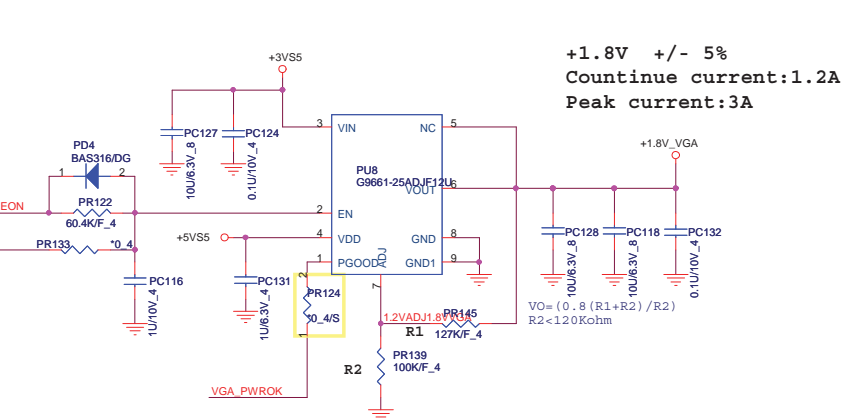


VDDNB Volt  
Countinue current:18A  
Peak current:22.5A  
OCP minimum:27A



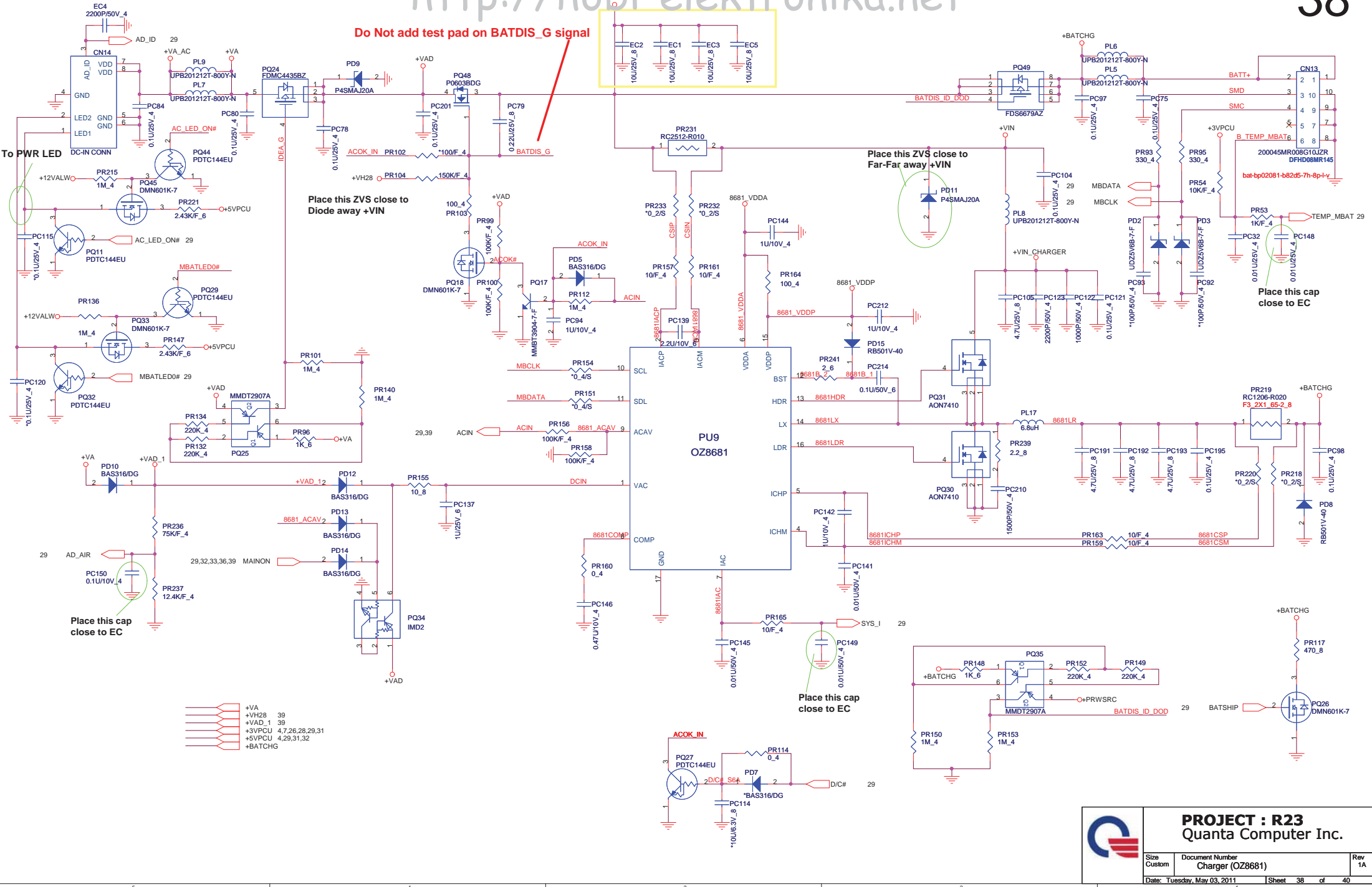


SG & Discrete Only




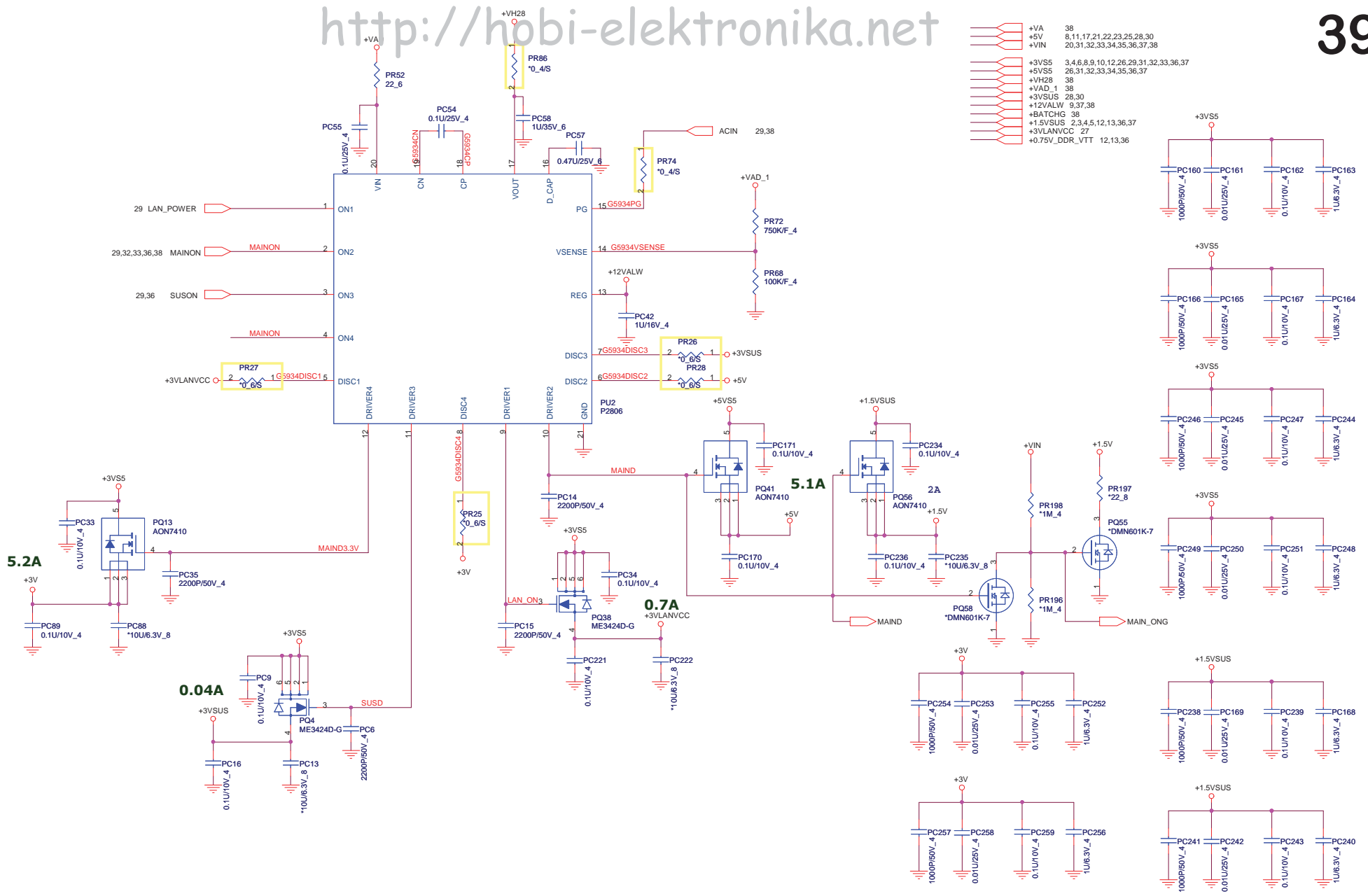


DC JACK 90W




- +VA
- +VH28 39
- +VAD\_1 39
- +3VPCU 4,7,26,28,29,31
- +5VPCU 4,29,31,32
- +BATCHG

		<b>PROJECT : R23</b>	
		Quanta Computer Inc.	
Size Custom	Document Number	Charger (OZ8681)	Rev 1A
Date: Tuesday, May 03, 2011		Sheet 38 of 40	



- +VA 38
- +5V 8,11,17,21,22,23,25,28,30
- +VIN 20,31,32,33,34,35,36,37,38
- +3VS5 3,4,6,8,9,10,12,26,29,31,32,33,36,37
- +5VS5 26,31,32,33,34,35,36,37
- +VH28 38
- +VAD\_1 38
- +3VSUS 28,30
- +12VALW 9,37,38
- +BATCHG 38
- +1.5VSUS 2,3,4,5,12,13,36,37
- +3VLANVCC 27
- +0.75V\_DDR\_VTT 12,13,36

 <b>PROJECT : R23</b> Quanta Computer Inc.			
			Size Custom
Date: Tuesday, May 03, 2011			Sheet 39 of 40