

PF1/2 BLOCK DIAGRAM

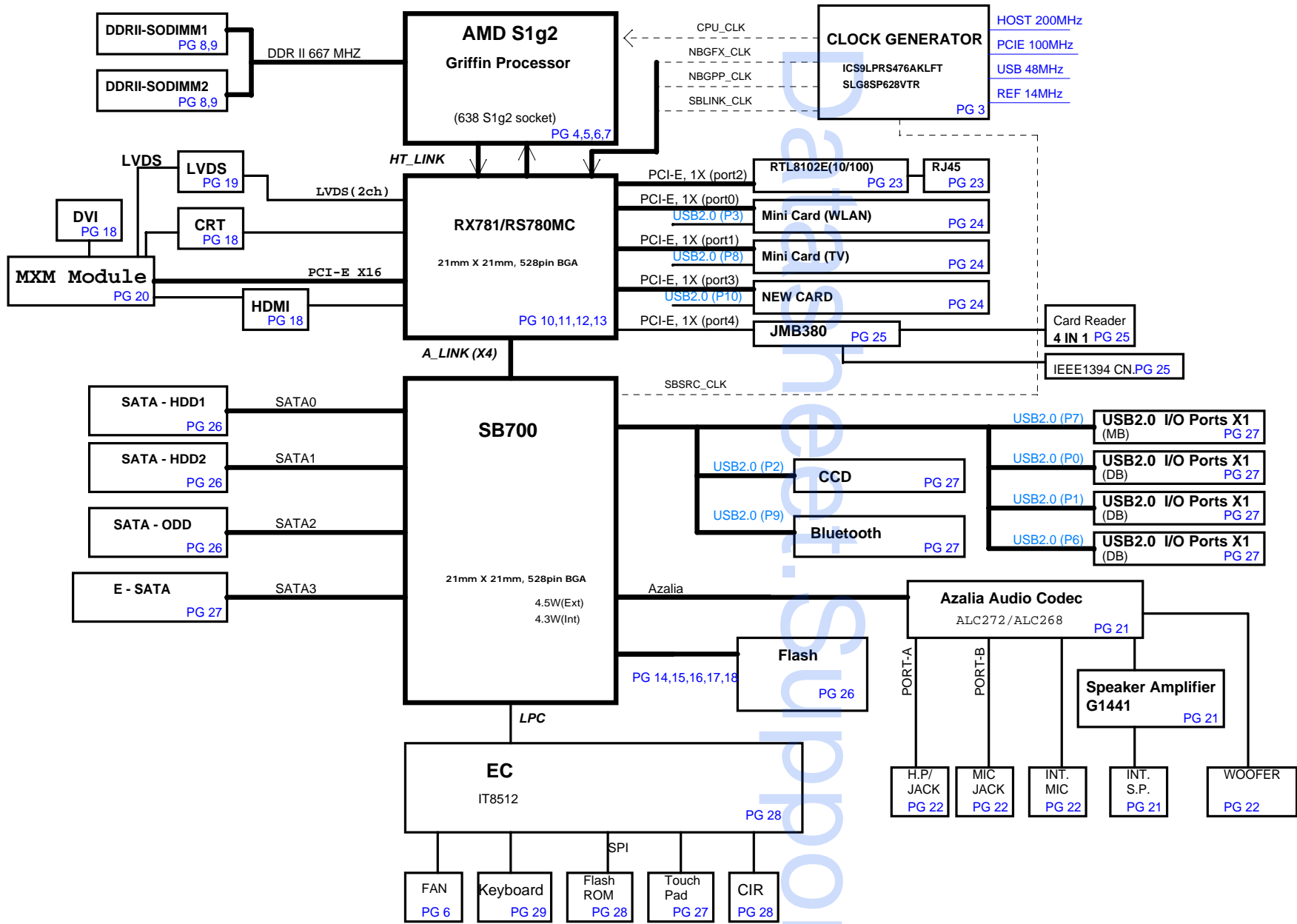
01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

Daughter Board

- MMB Board
- USB Board
- Touch Pad board
- Switch board



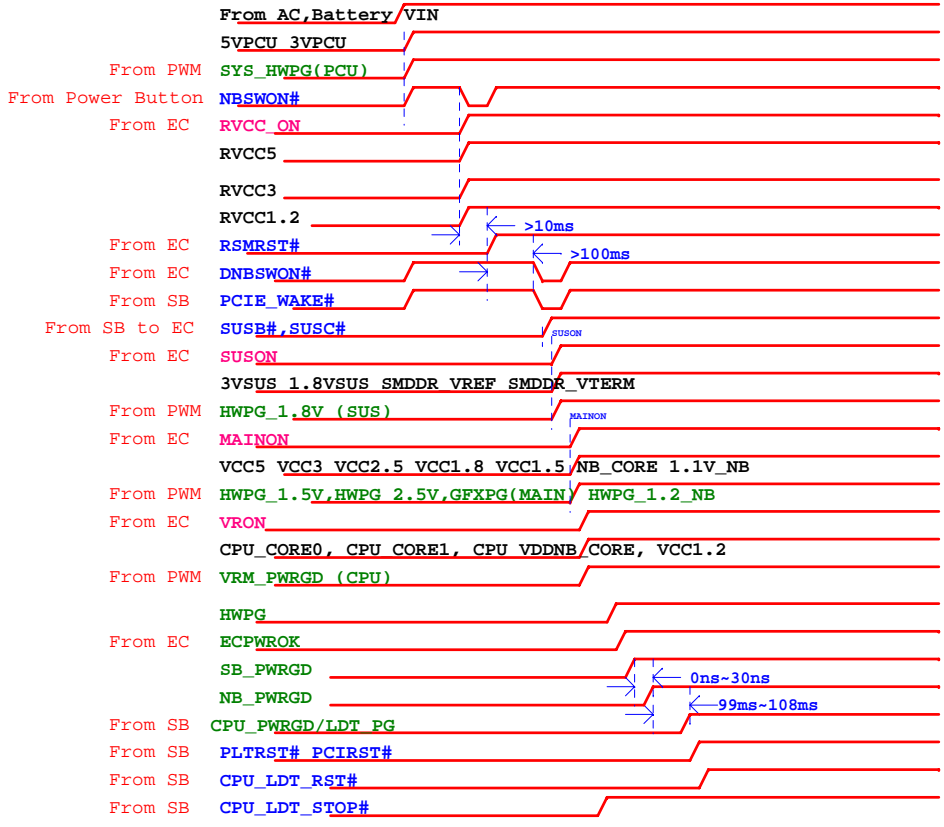
- CPU_CORE1
- CPU_CORE2
- CPU_VDDNB_CORE
- CPU CORE
- NB_CORE
- NB CORE (1.0~1.1V)
- RVCC1.2
- VCC1.2
- RVCC1.2
- VCC1.2
- 1.8VSUS
- VCC1.8
- SMDR_VTERM
- VCC1.5
- 1.1V_NB
- 1.8VSUS
- SMDR VTERM
- 3VPCU
- RVCC3
- 3VSUS
- VCC3
- 5VPCU
- 5VSUS
- VCC5
- VCC2.5
- 3V/5V

PROJECT : PF1
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	2A
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PF1 Power On Sequence

BOM naming rule



Items	Function	BTO	Name	Description
1	UMA	v	IV@	Internal VGA stuff
2	Discrete VGA	v	EV@	External VGA stuff
3	Subwoofer	v	WF@	Only for PF2P
4	IEEE 1394	v	EV@	External VGA model stuff
5	DVI-I	v	EV@	External VGA model stuff
6	D-SUB(CRT)	v	IV@	Internal VGA model stuff
7	HDMI	v	EV@	External VGA model stuff
8	CIR	v	CIR@	For PF1P and PF2P(M86)
9	TV		TV@	For PF1P and PF2P(M86)
10				
11				
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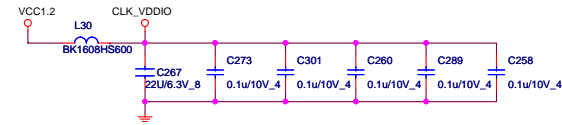
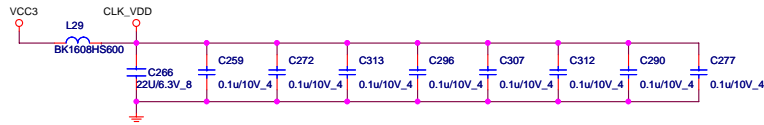
*Note: EC will sampling SUSB# & SUSC# every 5ms.

AMD SB700 SMBUS Table

	CLK GEN	RAM	Mini Card (TV)	Mini-card(WL)	New Card	HDMI
SB700 SDATA0/SCLK0(VCC3)	V	V	V	V	V	
SB700 SDATA1/SCLK1(3V_S5)						V
SB700 SDATA2/SCLK2(3V_S5)						
Power	VCC3	VCC3	VCC3	VCC3(Atheros)	VCC3	RVCC3
Reserve MOS ckt	V	V	V	V	V	V

EC SMBUS Table

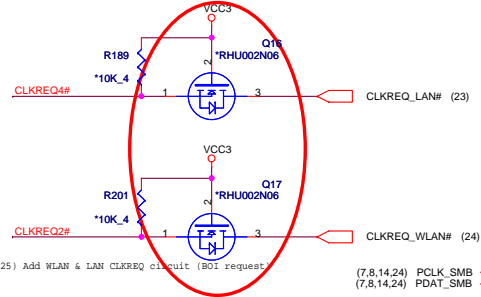
	Battery	CPU thermal Sensor	EC EEPROM	VGA thermal Sensor	Touch Sensor	HDMI	CEC
EC775 SDATA1/SCLK1(3VPCU)	V						
EC775 SDATA2/SCLK2(3VPCU)		V	V				
EC775 SDATA3/SCLK3(3VPCU)				V	V	V	
EC775 SDATA4/SCLK4(3VPCU)							
Power	3VPCU	VCC3	3VPCU	VCC3	3VPCU	5VPCU	
Reserve MOS ckt	X	V	X	V	X	V	



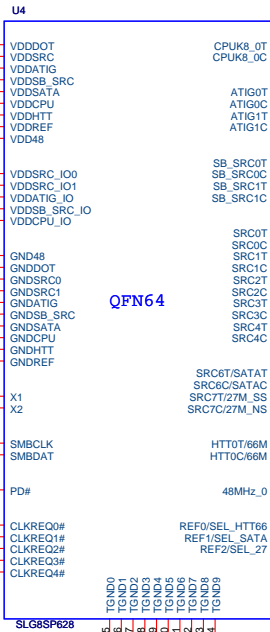
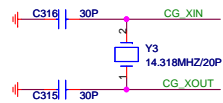
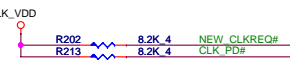
ICS9LPRS480 P/N : ALPRS480000
 SLG8SP628 P/N : AL8SP628000
 RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

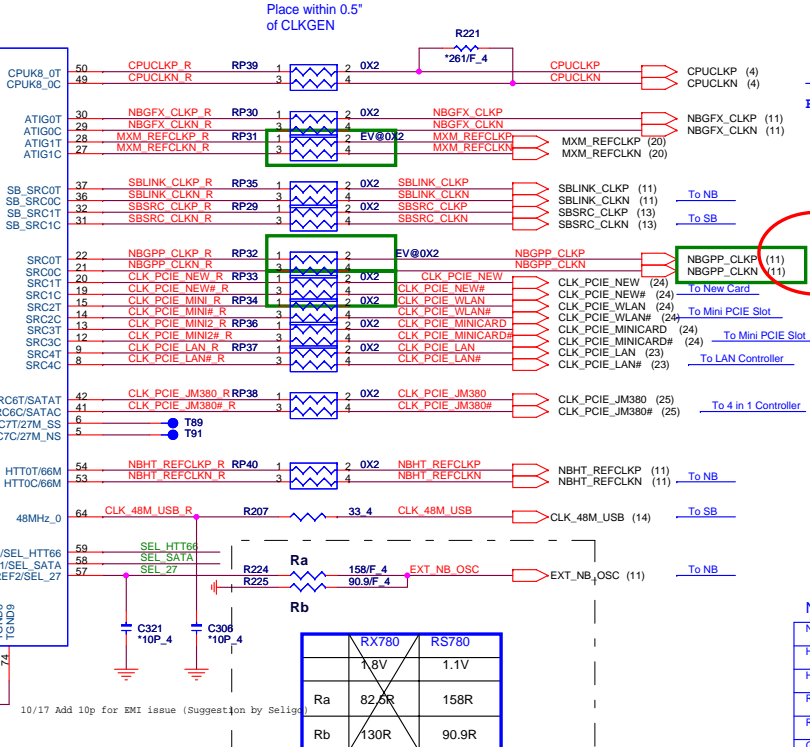
10/25 modify it



B: (10/25) Add WLAN & LAN CLKREQ circuit (BOI request)



QFN64



Place within 0.5" of CLKGEN

To CPU RS780/RX781 for VGA

To NB

To NB

To SB

To NB

To New Card

To Mini PCIe Slot

To Mini PCIe Slot

To LAN Controller

To 4 in 1 Controller

To NB

To NB

To SB

To NB

To NB

To NB

To NB

To NB

To NB

To NB

To NB

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To NB

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11/4 check RX781

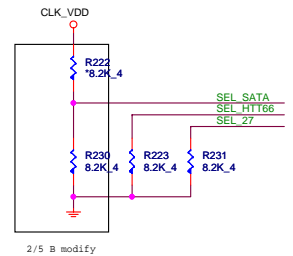


NB CLOCK INPUT TABLE

NB CLOCKS	RX781	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSPB_REFCLK	100M DIFF	100M DIFF

	RX780	RS780
Ra	82.6R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +/-1%(0402)L-F -->CS11302FB15
 RES CHIP 158 1/16W +/-1%(0402) -->CS11582FB00
 RES CHIP 90.9 1/16W +/-1%(0402) -->CS09025FB15
 RES CHIP 82.5 1/16W +/-1%(0402) -->CS08252FB11

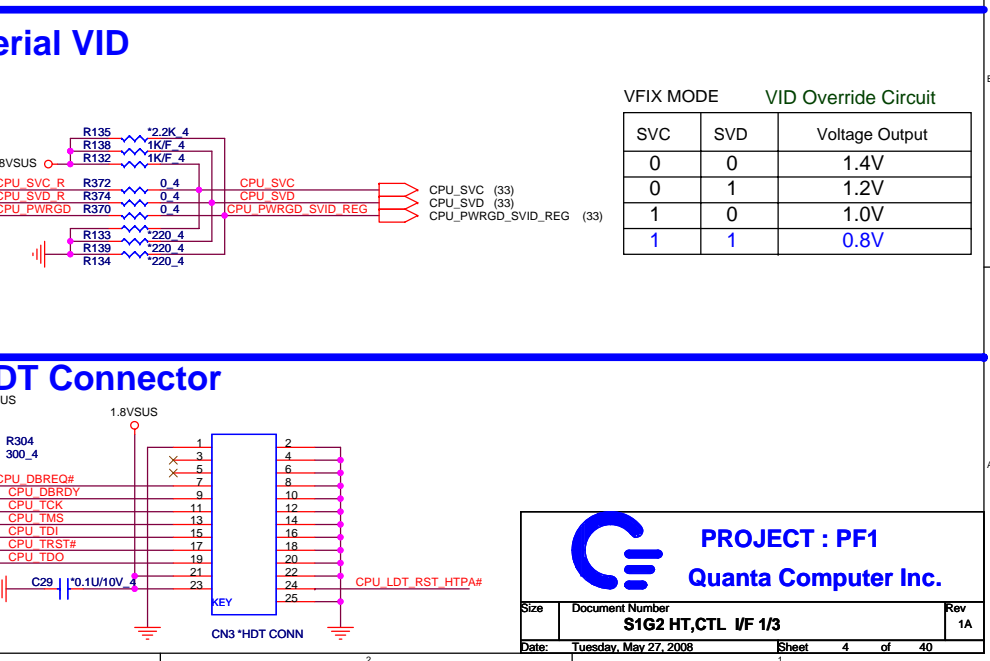
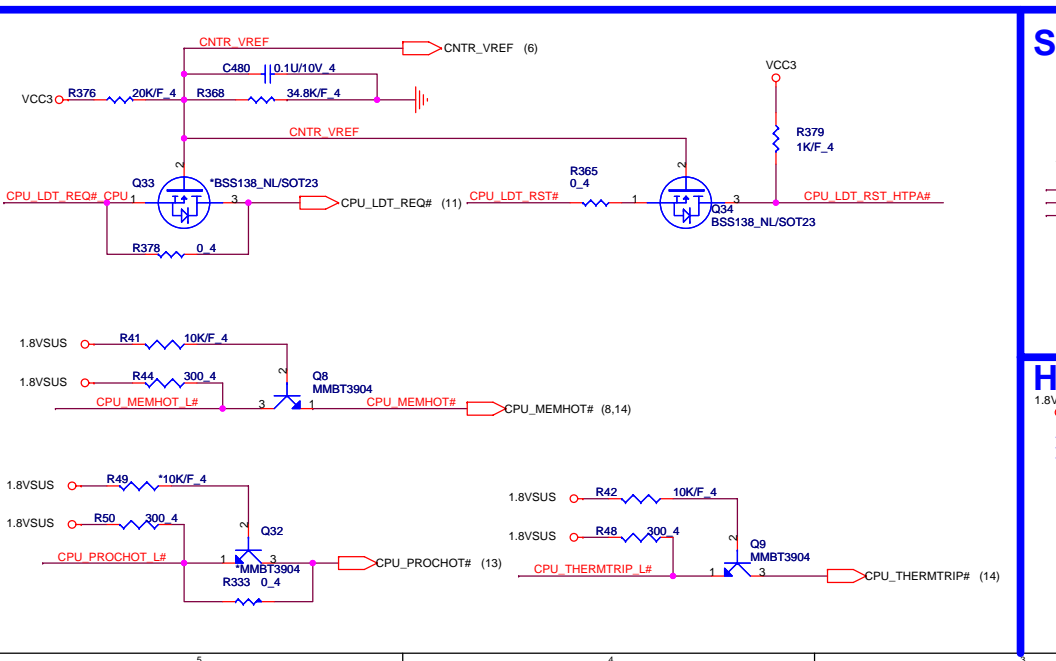
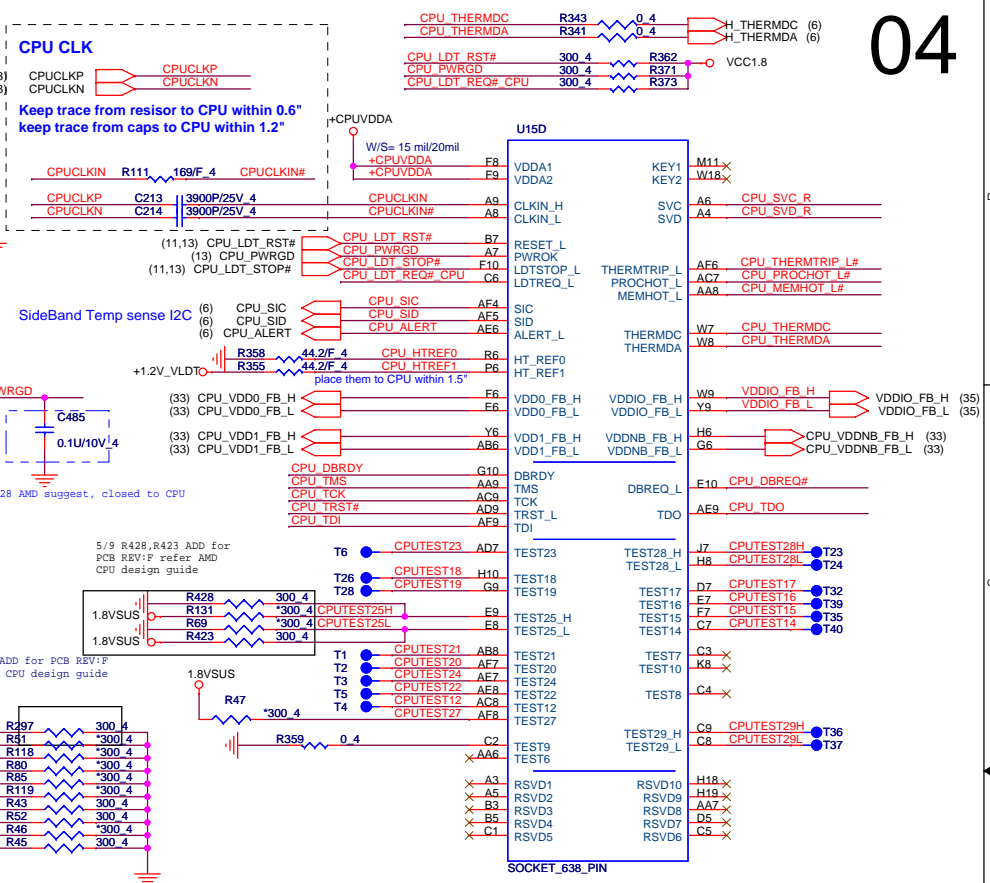
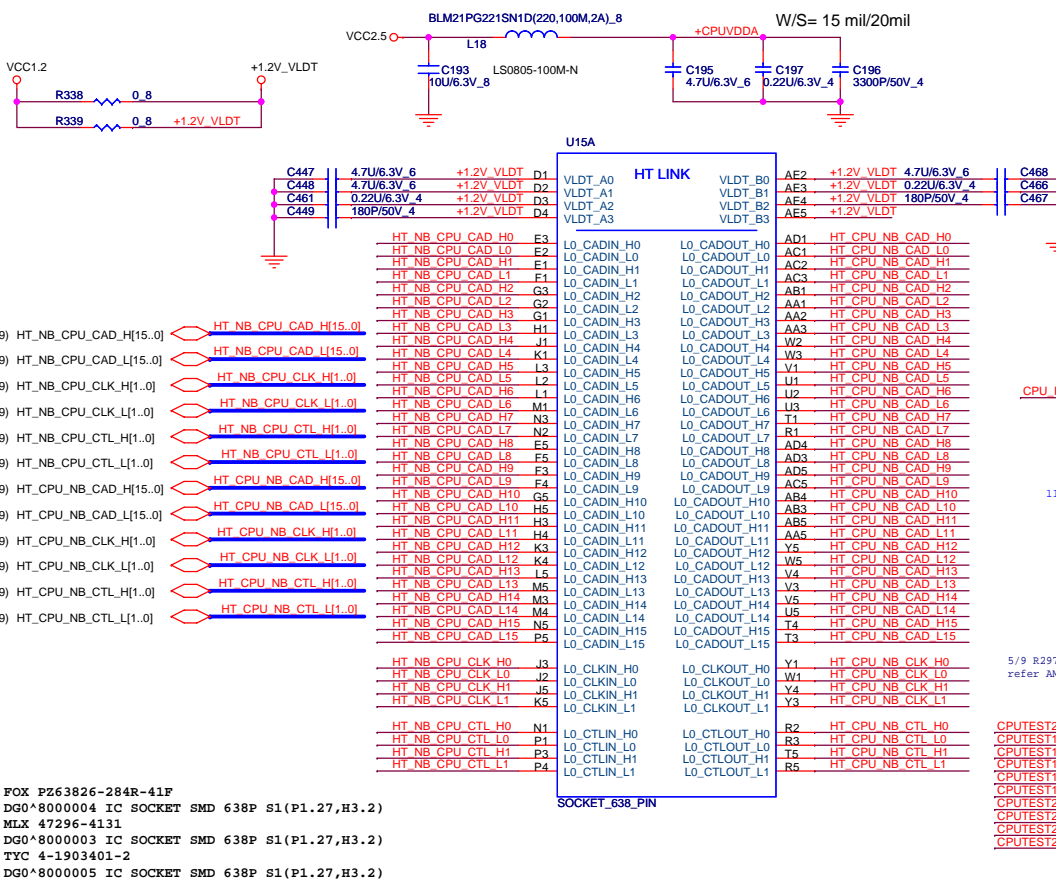


SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
SEL_HTT66	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
SEL_SATA	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
SEL_27	0*	100 MHz SRC clock

CLOCKS name	RX781	RS780	Clock pin function
NBGFX_CLKP NBGF_X_CLKN	RP30 STUFF	RP30 STUFF	to NB for VGA reference clock
MXM_REFCLKP MXM_REFCLKN	RP31 STUFF	RP31 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGP_P_CLKN	RP32 STUFF	RP32 NC	to NB for RX780 for PCIeX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP35 STUFF	RP35 STUFF	to NB for AC-LINK reference clock

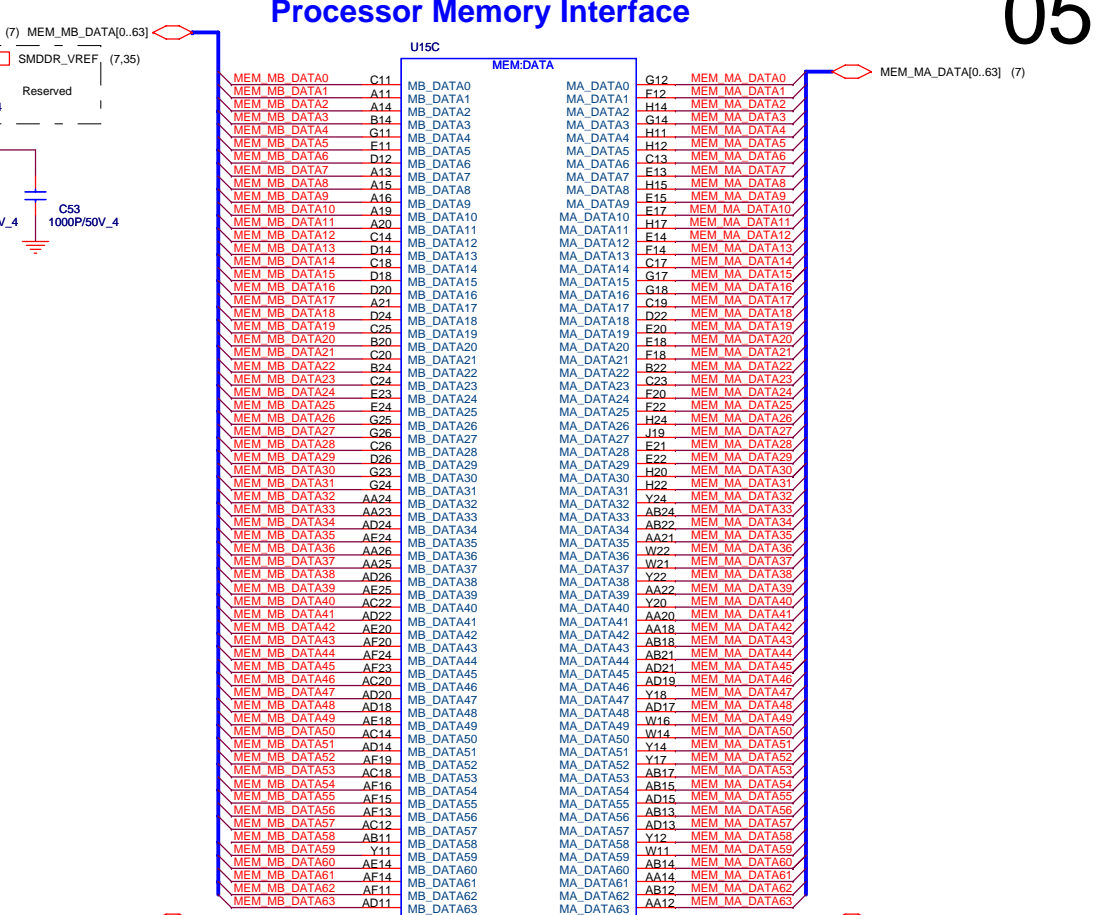
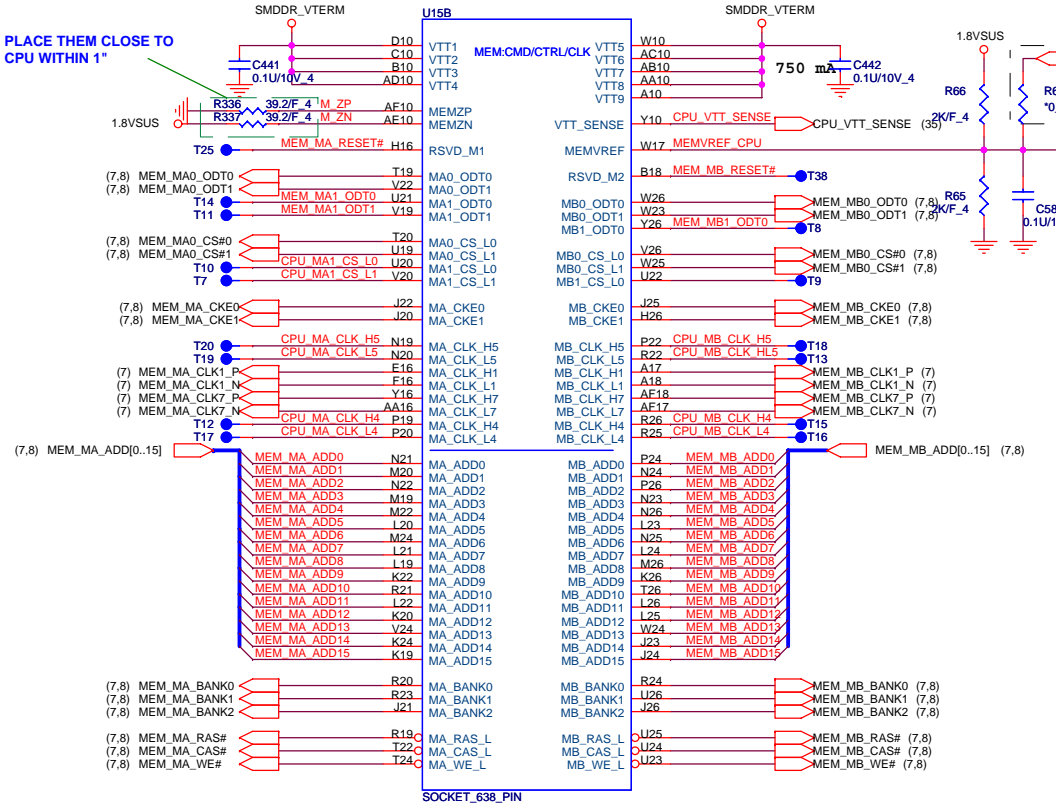
PROJECT : PF1
Quanta Computer Inc.

Size: Document Number:
CLOCK GENERATOR_SLG8SP628 Rev: 1A
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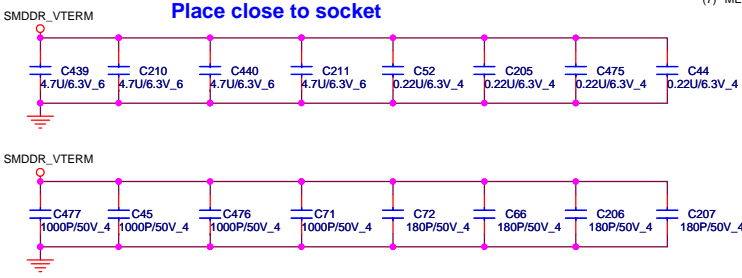


Processor Memory Interface

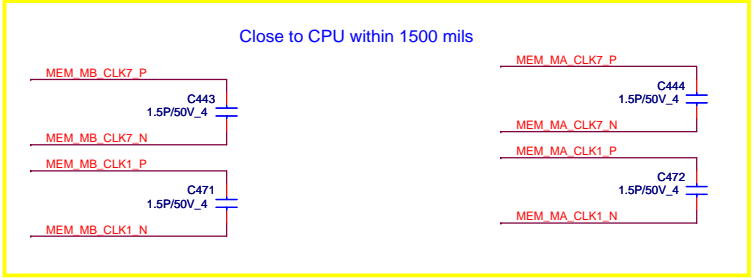
PLACE THEM CLOSE TO CPU WITHIN 1"



Place close to socket



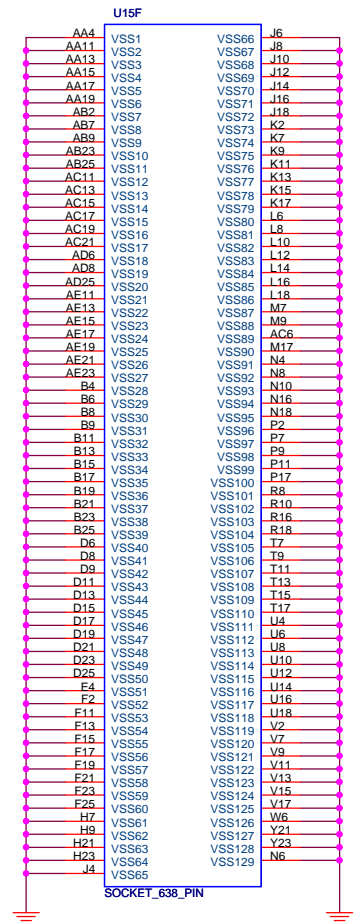
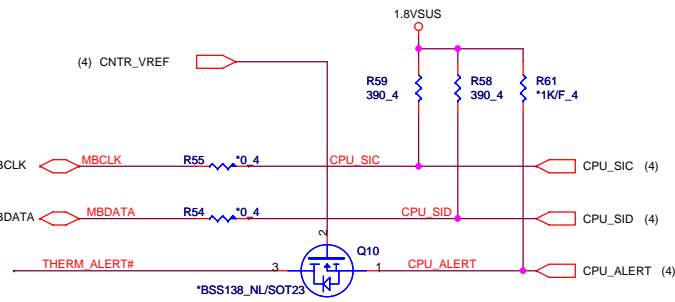
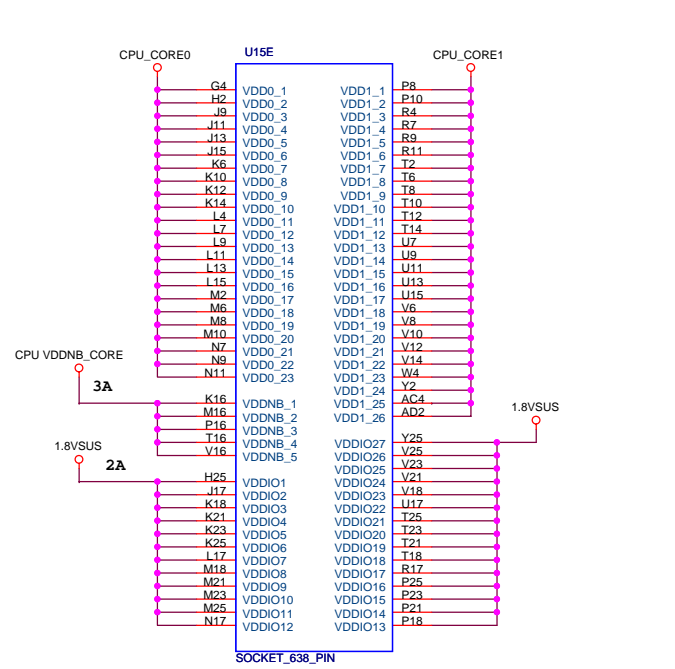
Close to CPU within 1500 mils



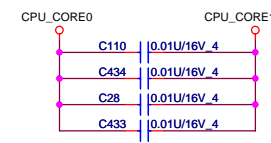
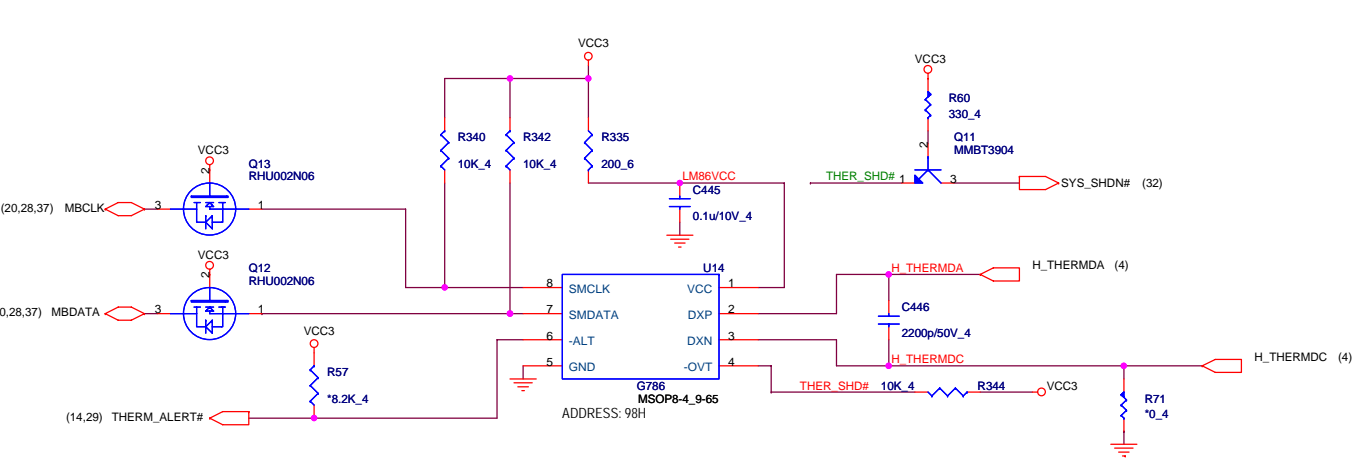
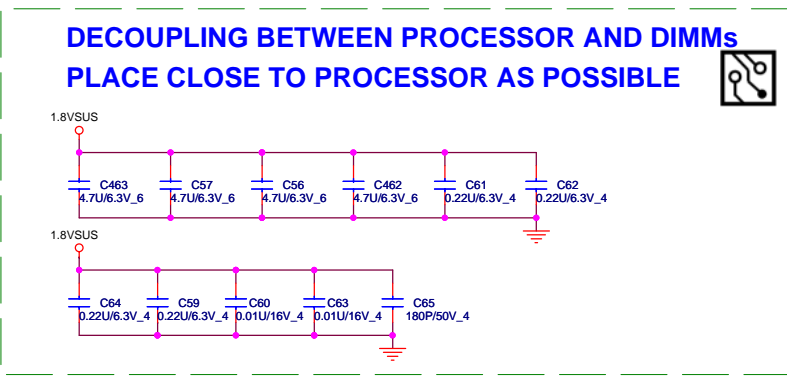
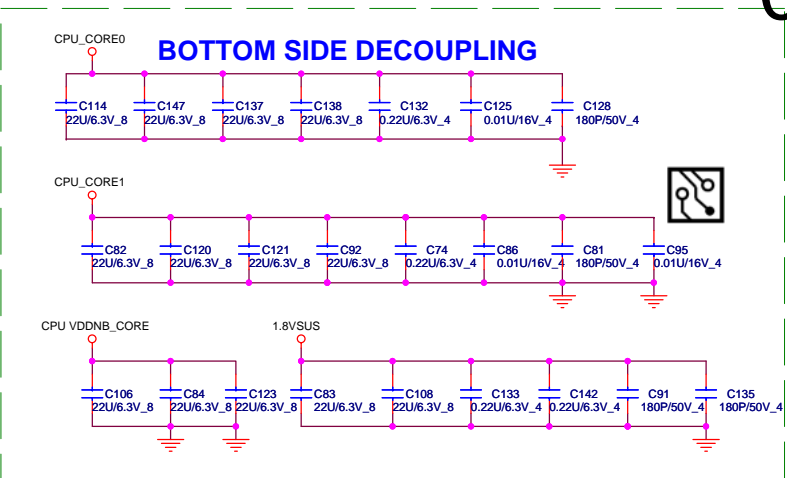
PROJECT : PF1
Quanta Computer Inc.

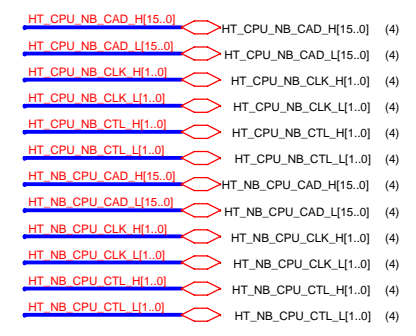
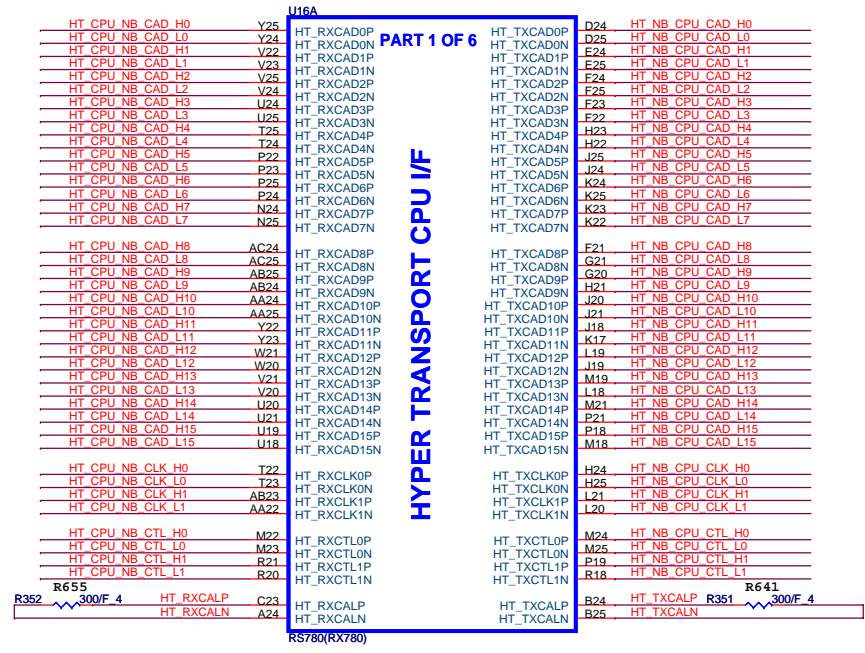
Size Document Number
S1G2 DDRII MEMORY I/F 2/3

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PROCESSOR POWER AND GROUND



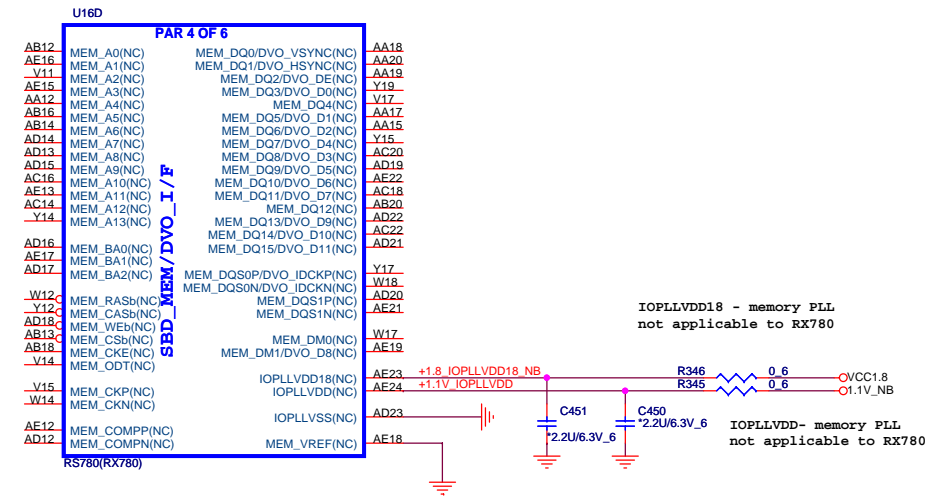


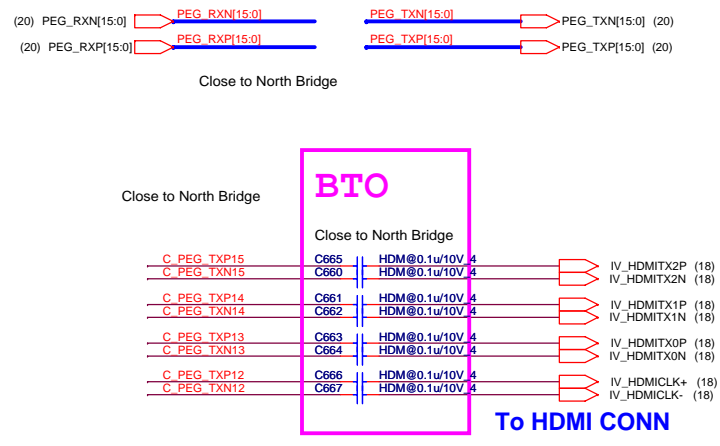
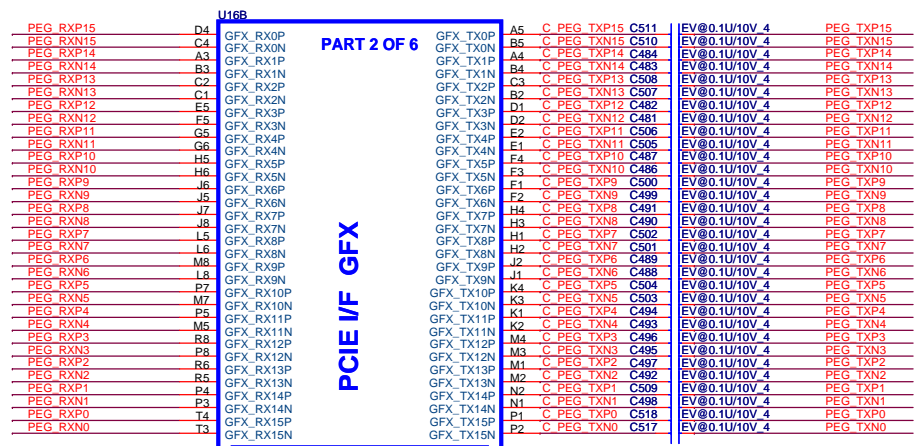
signals	RS780	RX781
HT_TXCALP	R351 300 ohm 1%	R351 1.21k ohm 1%
HT_RXCALP	R352 300 ohm 1%	R352 1.21k ohm 1%

RES CHIP 1.21k 1/16W +-1%(0402)
P/N : CS21212FB18

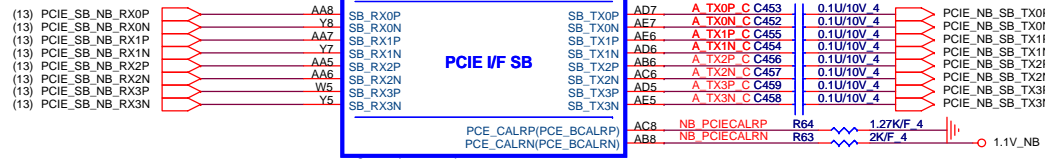
RES CHIP 300 1/16W +-1%(0402)
P/N : CS13002FB00

This block is for UMA RS780 only , RX781 can remove all component





- TO WLAN
- TO MINI CARD
- TO PCIE-LAN
- TO EPRESS CARD
- TO CARD READER



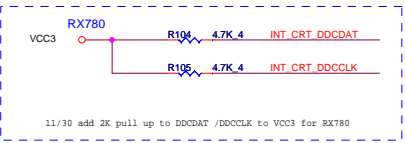
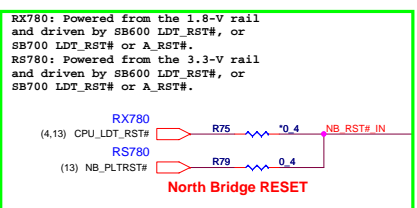
RS780(RX780)

RS780/RS740/RS780 difference table (PCIE LINK)

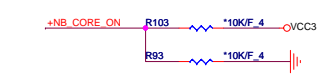
	RS740	RS780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



11/4 no stuff for RS780M/MC/RX781



selects Loading of straps from EEPROM

1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT



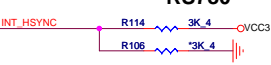
Enables Debug Bus access through memory T/O pads and GPIO.

0 : Enable RS780 , Default
1 : Disable RS780 (RS780 use VSYNCH#)

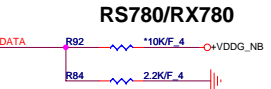


Indicates if memory Side port is available or not

0 : available RS780 , Default
1 : Not available RS780 (RS780 use HSYNCH#)



For extrnal EEPROM Debug only

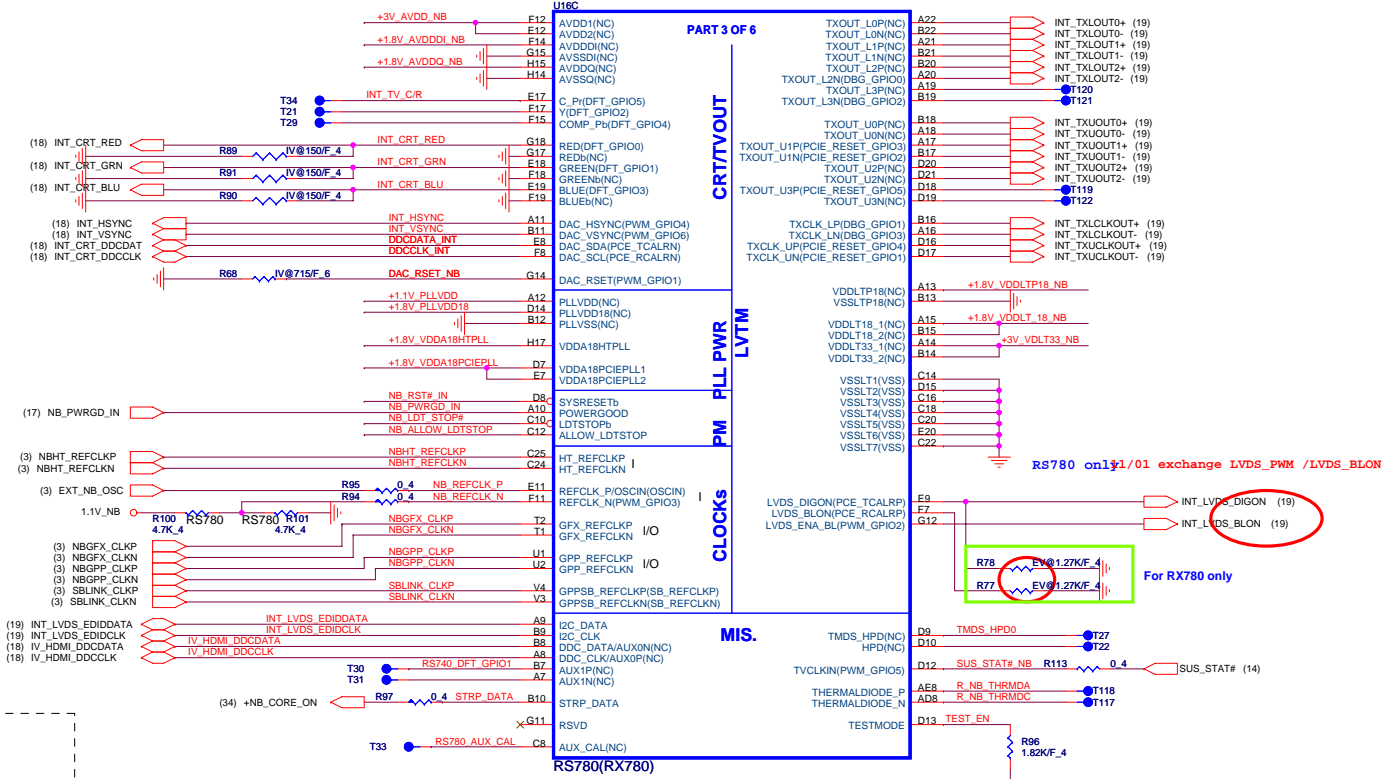


Enables Debug Bus access through memory T/O pads and GPIO.

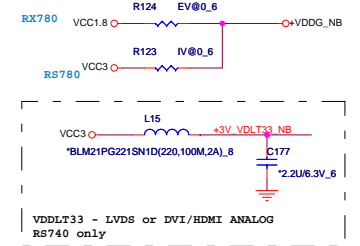
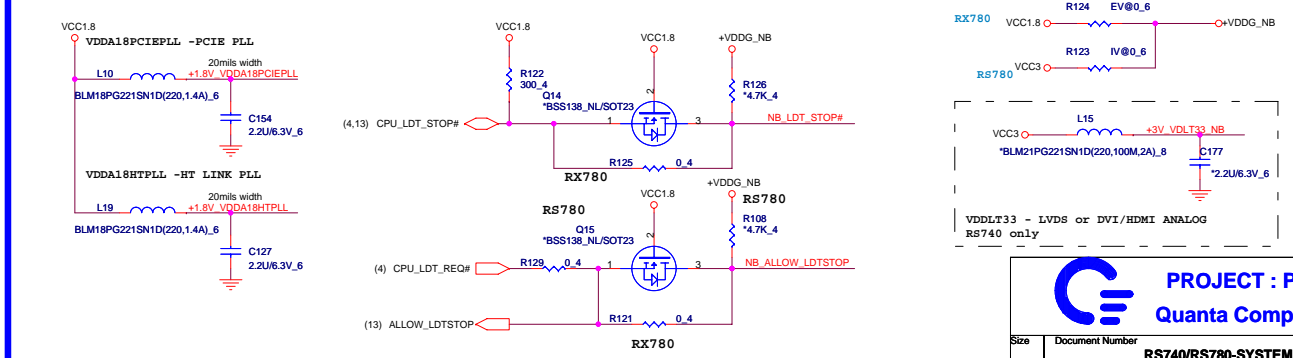
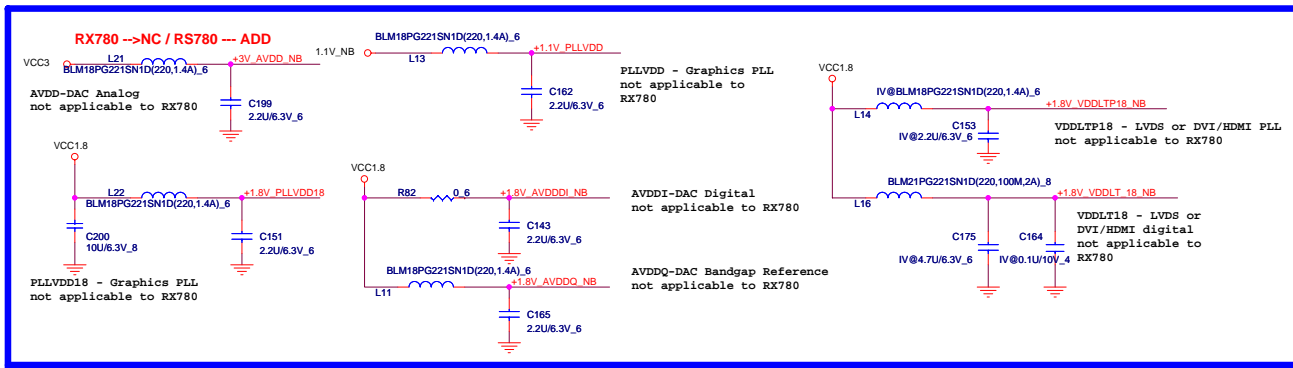
1 : Enable RX780 , Default
0 : Disable RX780

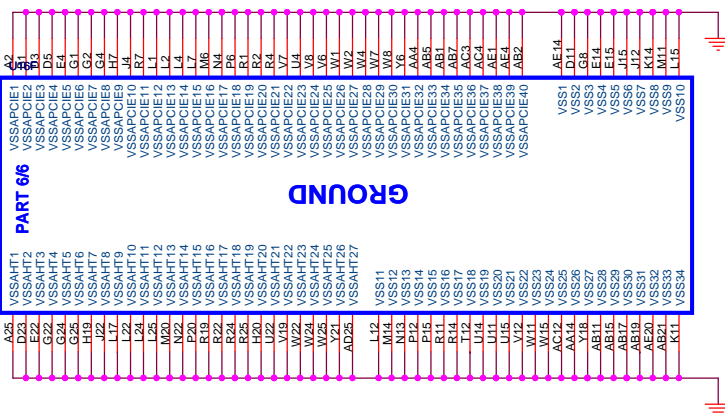


Reserved only



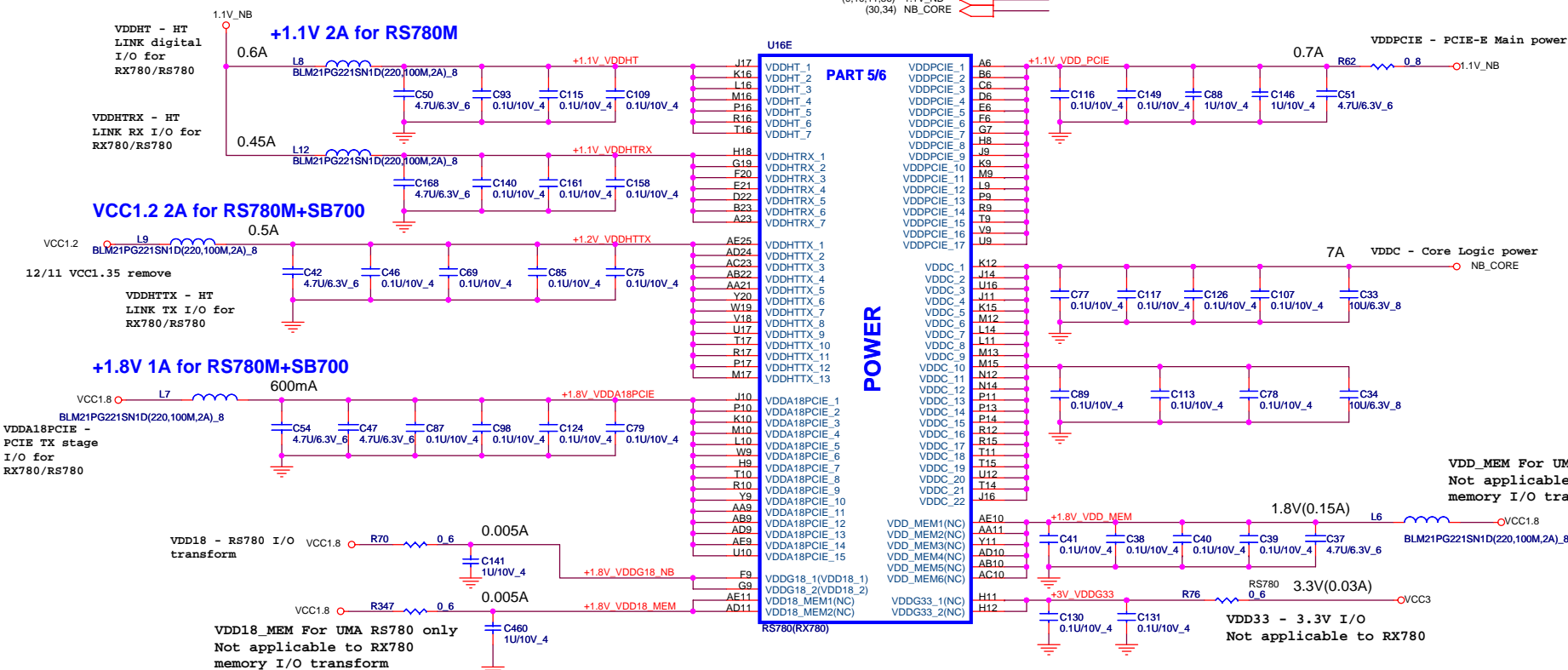
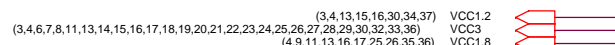
RS780 only 1/01 exchange LVDS_PWM / LVDS_B/LON





RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL33	NC	NC

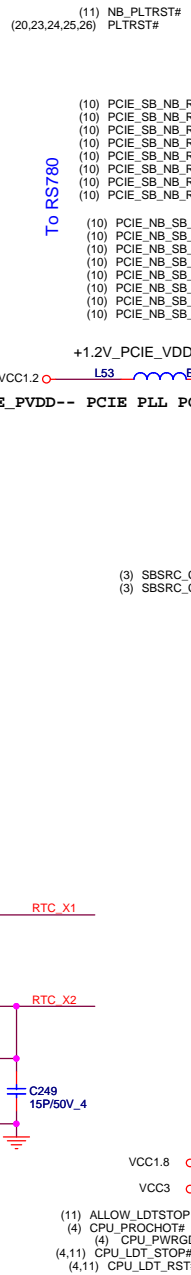


PROJECT : PF1
Quanta Computer Inc.

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PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U19



To RS780

SB700
Part 1 of 5

PCI EXPRESS INTERFACE

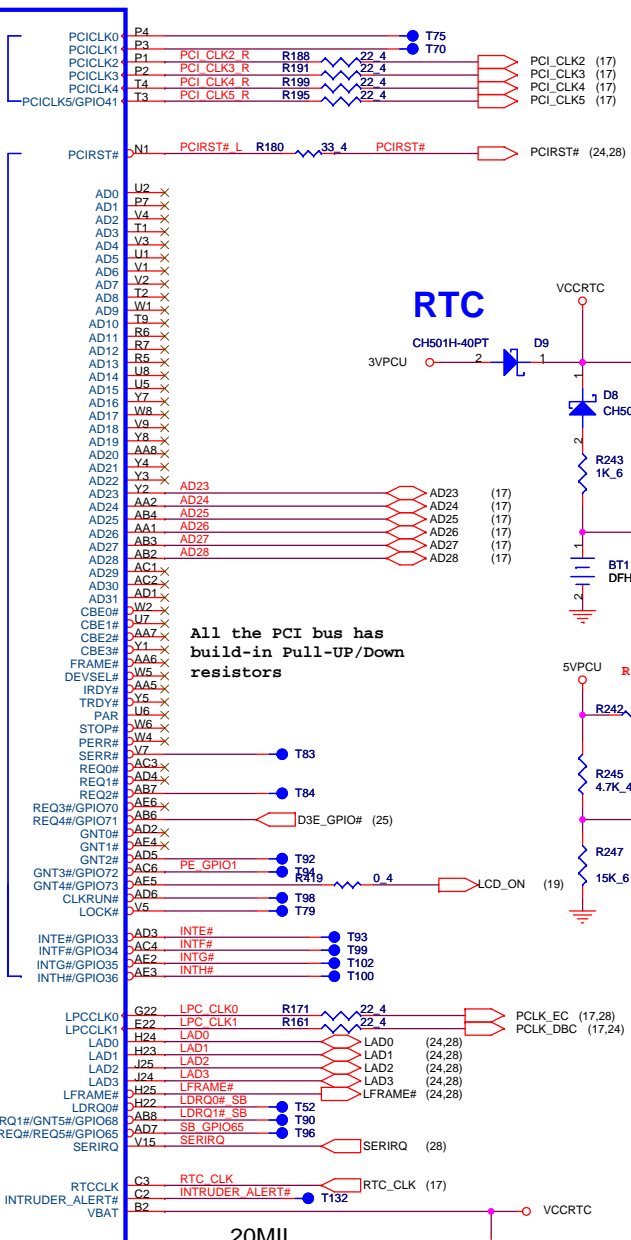
PCI INTERFACE

CLOCK GENERATOR

LPC

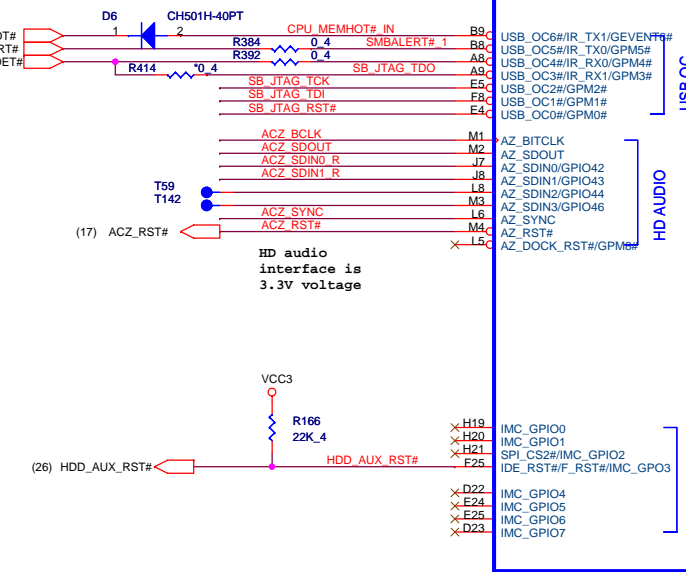
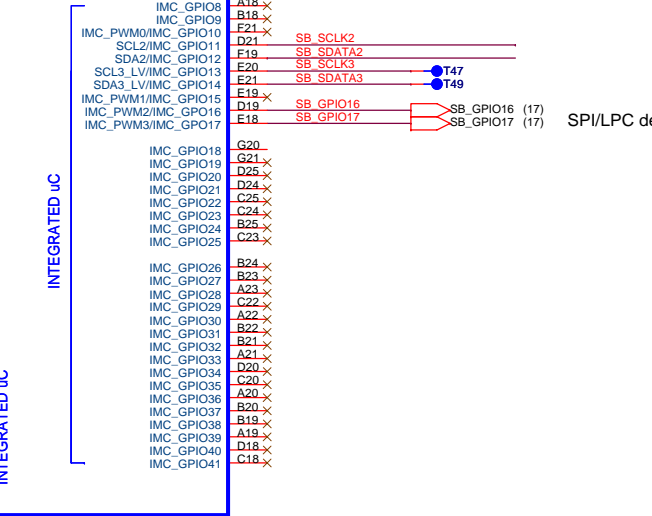
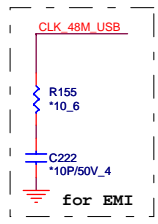
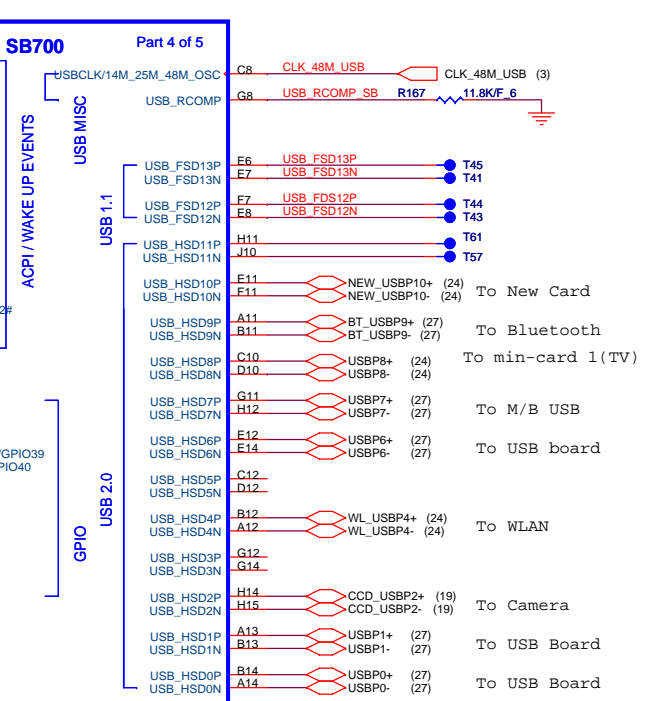
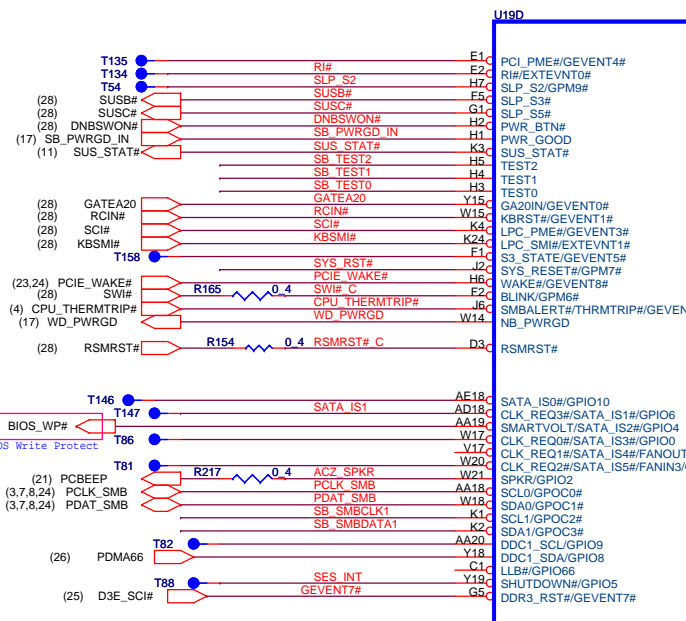
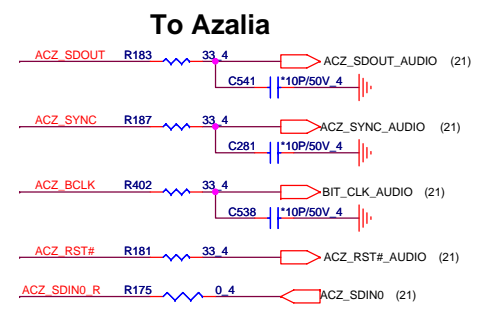
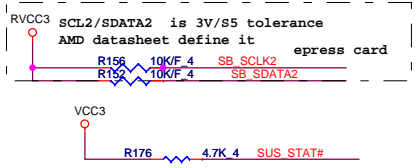
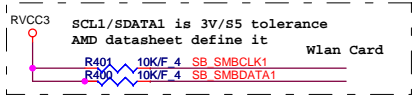
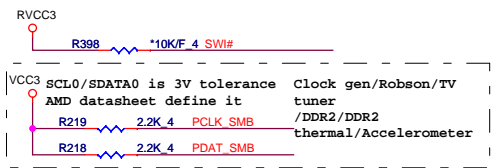
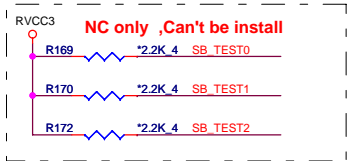
RTC

SB700
IC CTRL(528P) SB700 A11(218S7EAL11FG)
P/N : AJALA110T00



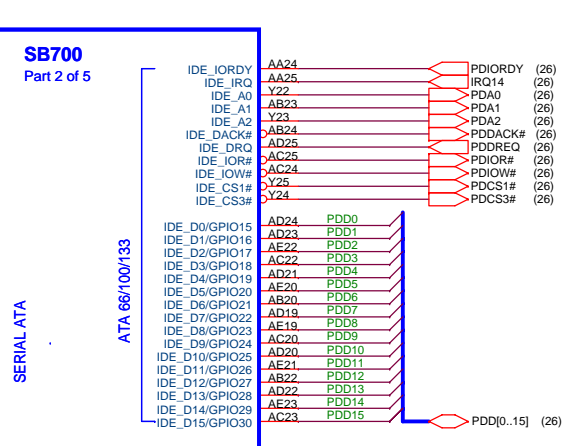
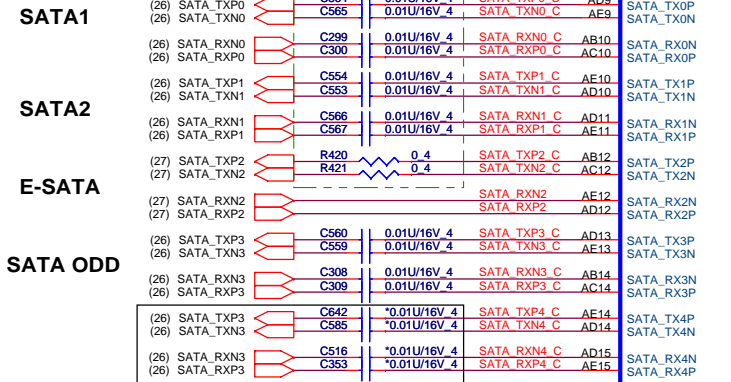
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	SB700-PCIE/PCI/CPULPC 1/4	1A
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SATA PORT 0,1,2,3
can support AHCI
mode

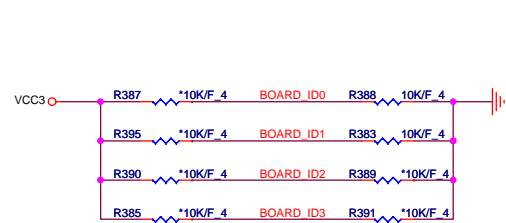
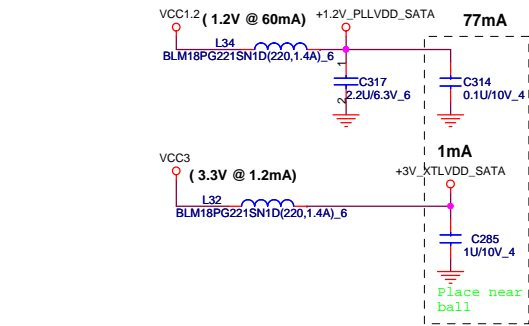
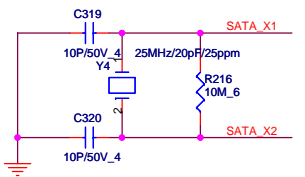
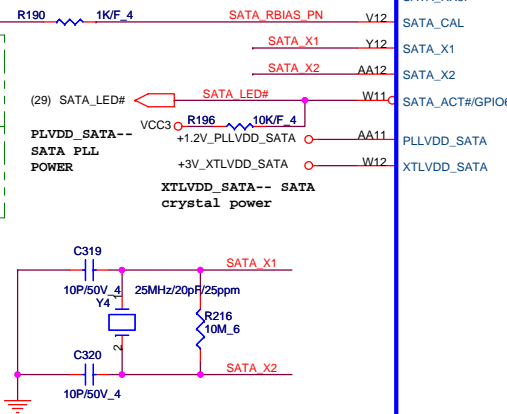
PLACE SATA AC COUPLING
CAPS CLOSE TO SB600



SATA PORT 4,5 are
only support IDE
mode

PLACE SATA CAL
RES VERY CLOSE
TO BALL OF SB700

NOTE:
R190 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK



11/23 Board ID define MXM
MB ID Selection Table

Board ID	ID4	ID3	ID2	ID1	ID0
15" UMA	x	x	0	0	0
15" M82	x	x	0	0	1
15" M86	x	x	0	1	1
17" UMA	x	x	1	0	0
17" M82	x	x	1	0	1
17" M86	x	x	1	1	1

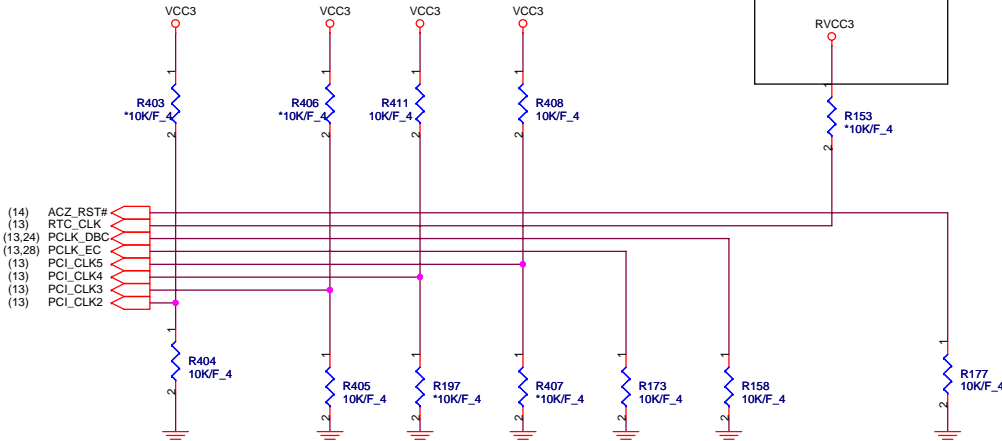
PROJECT : PF1
Quanta Computer Inc.

Size Document Number
SB700-SATA/IDE/HWM/SPI 3/4 Rev 1A

Date: Tuesday, May 27, 2008 Sheet 15 of 40

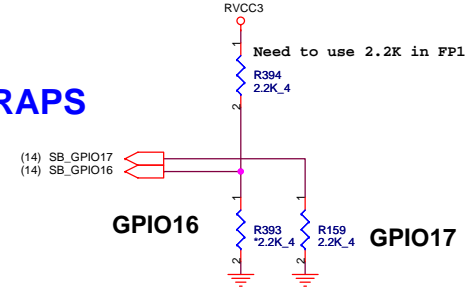


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



It must ready before RSMRST#

REQUIRED STRAPS

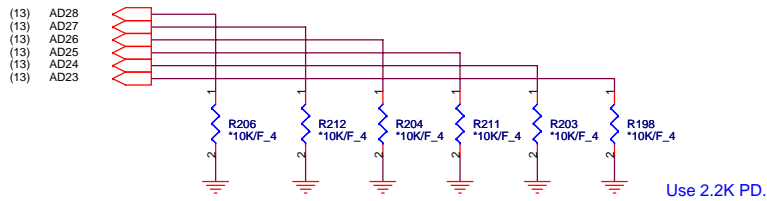


GPIO16 GPIO17

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

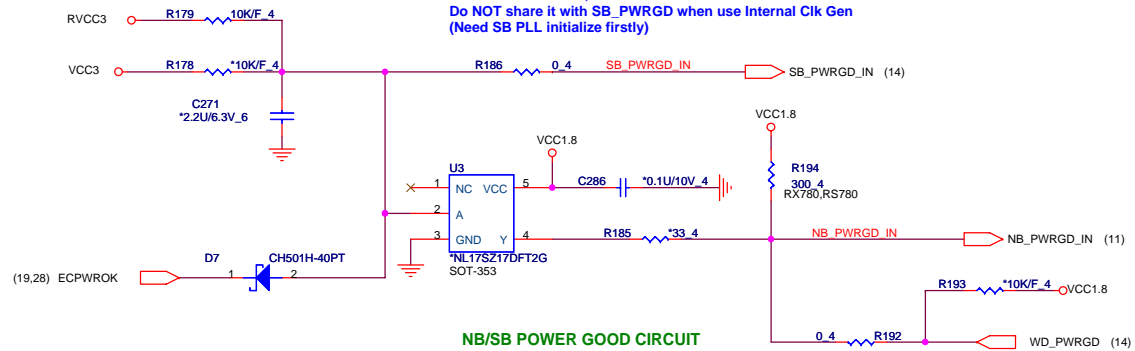
DEBUG STRAPS SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

Use 2.2K PD.

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



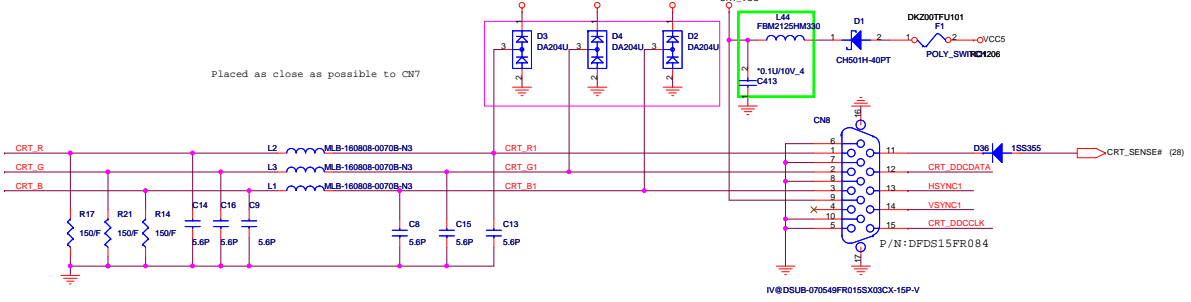
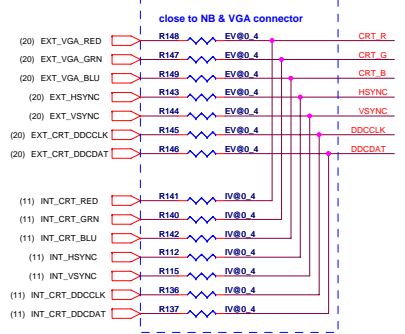
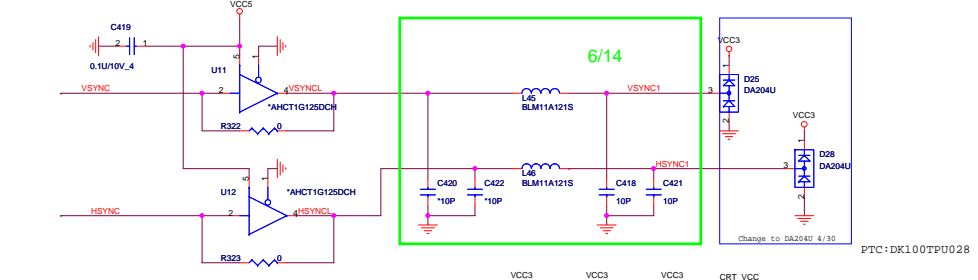
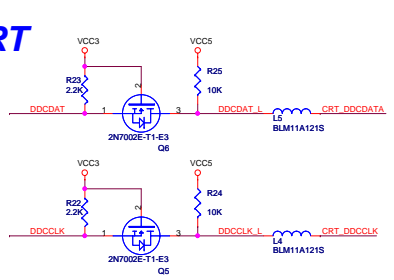
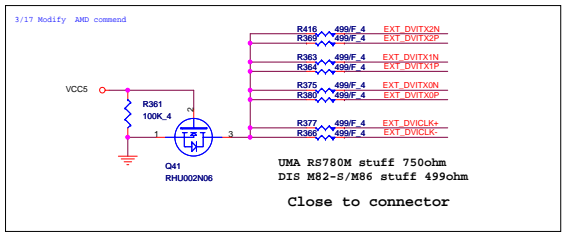
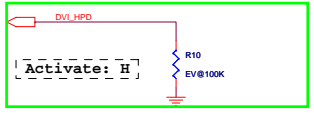
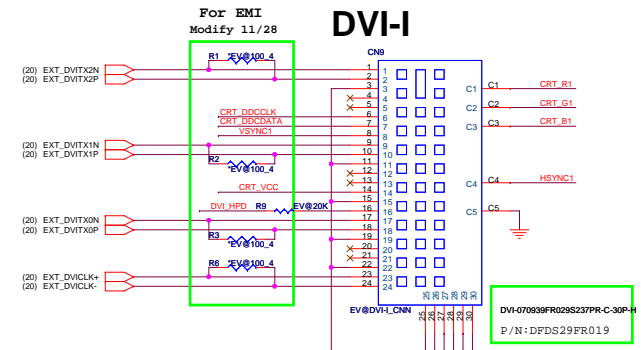
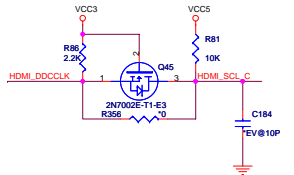
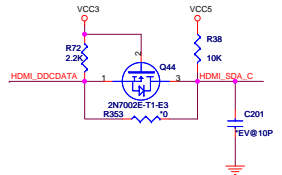
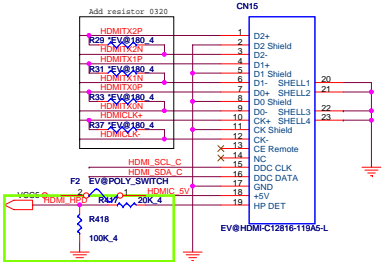
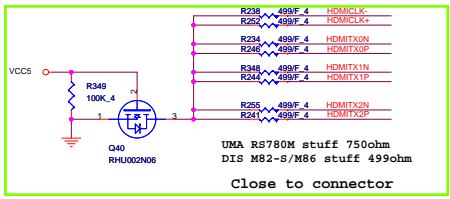
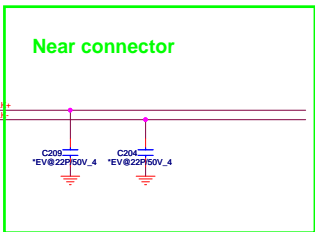
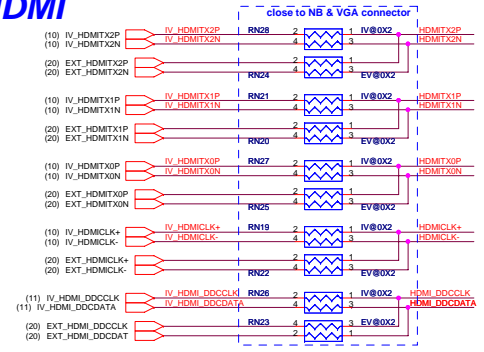
NB/SB POWER GOOD CIRCUIT

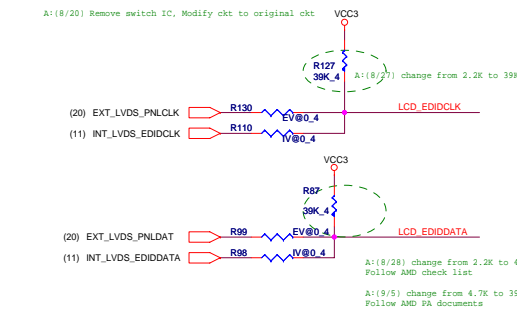
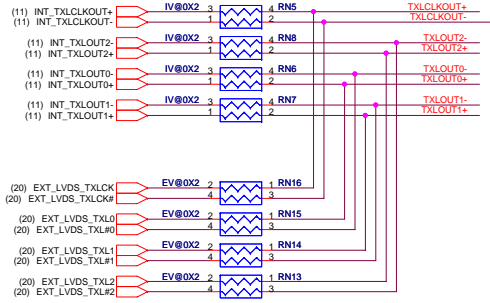
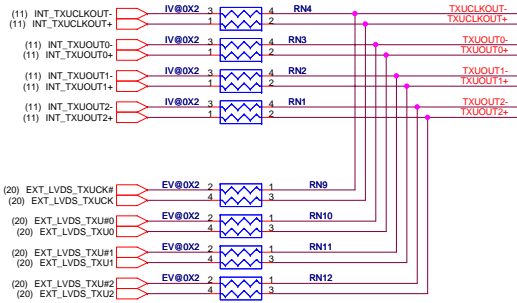
	U11	R230	R229	R245	R234
RX780	V	V	V	X	X
RS780M	V	V	V	X	X

AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

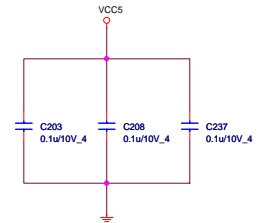
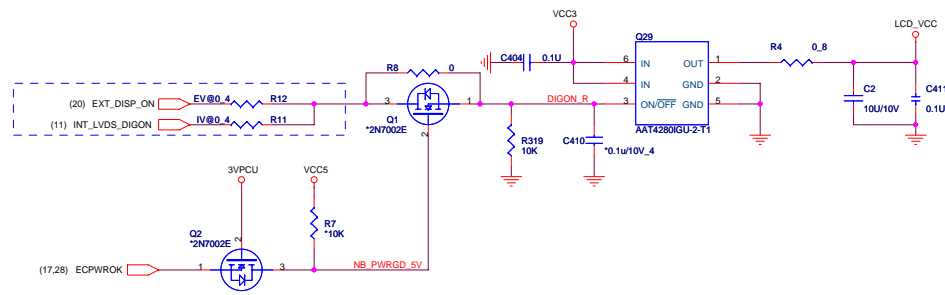
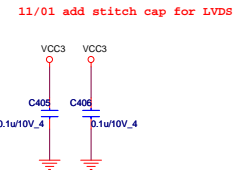
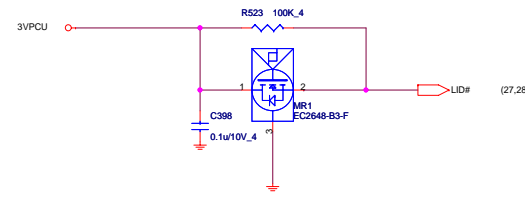


PROJECT : PF1
Quanta Computer Inc.

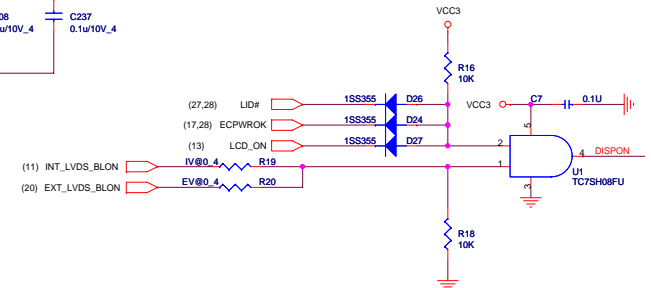
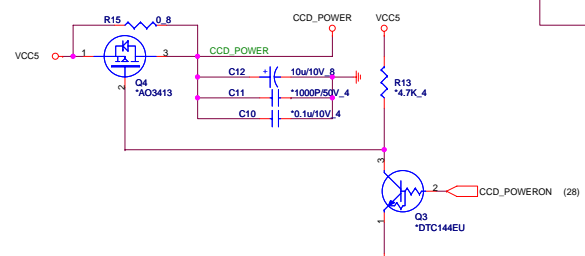




HALL SENSOR

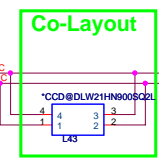
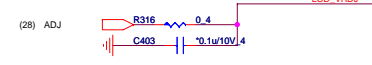
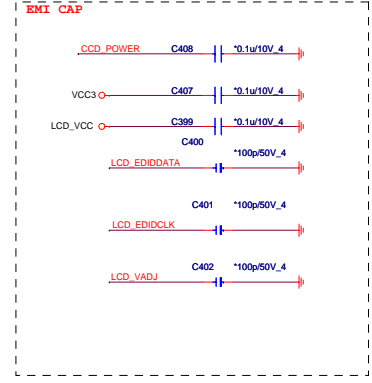
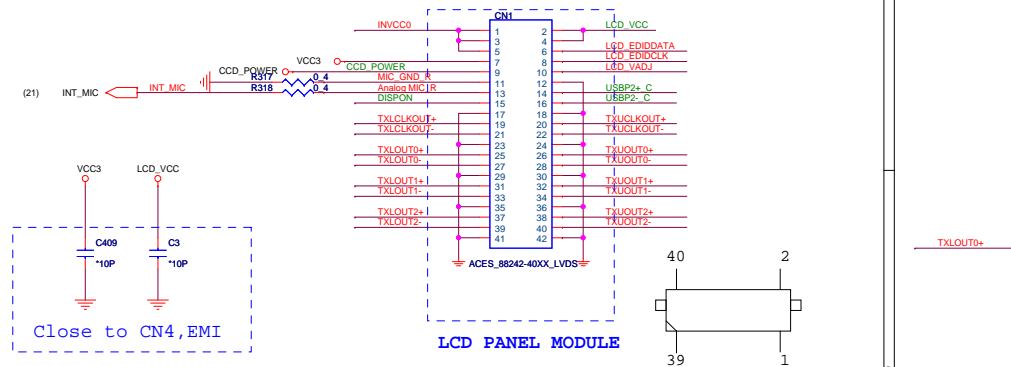


CAMERA MODULE

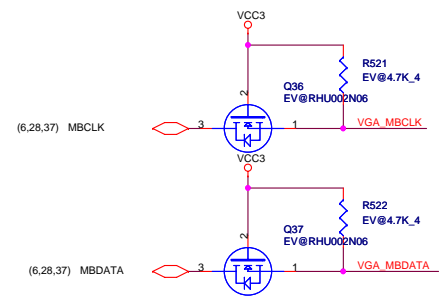
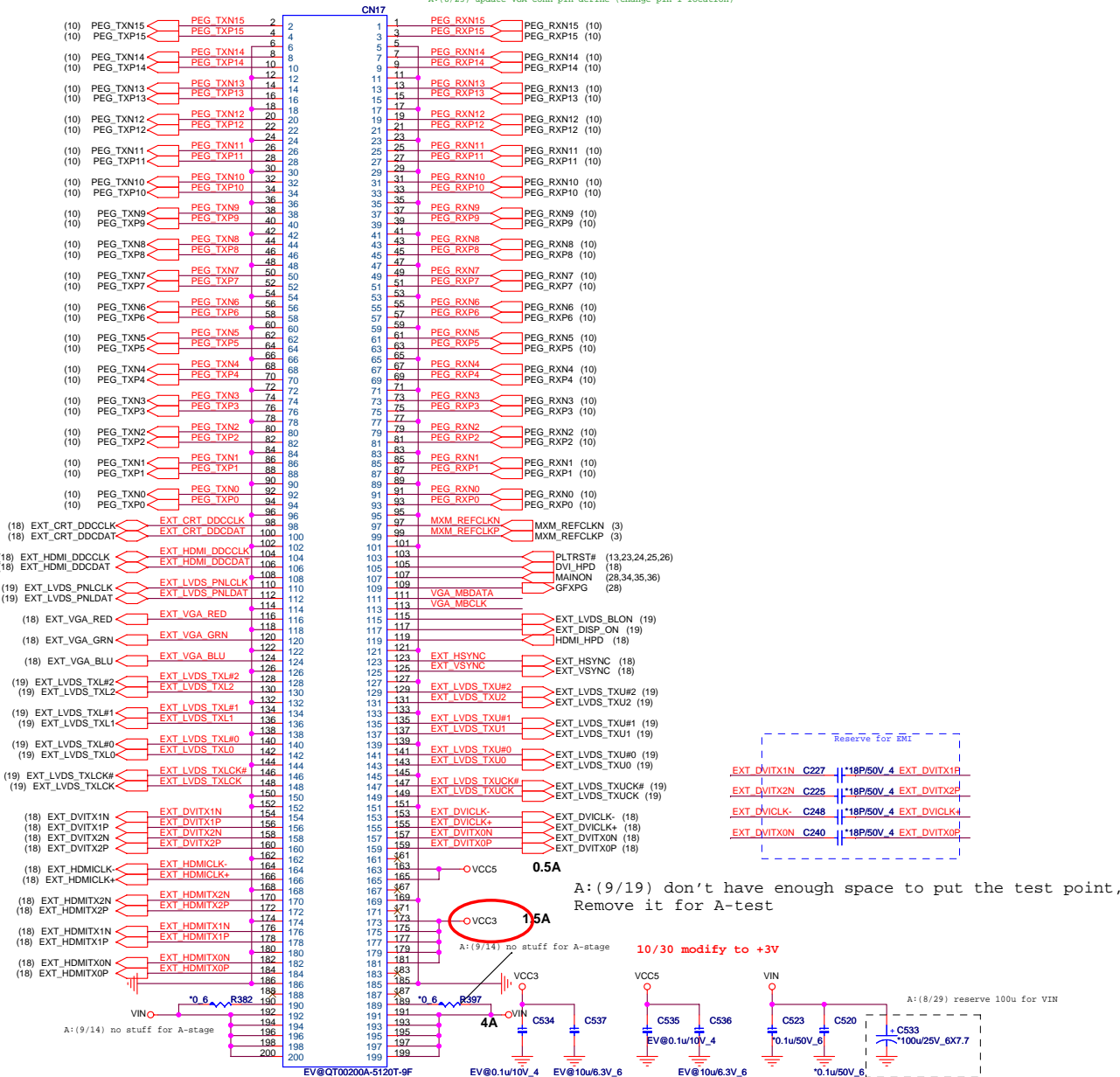


8/13 Change Size To 1206

10/22 update p/n From DFHS40PS825 to DFPW40MS000



A:(8/18) update VGA conn footprint base on allian information
A:(8/23) update VGA conn pin-define (change pin 1 location)



A:(9/19) don't have enough space to put the test point, Remove it for A-test

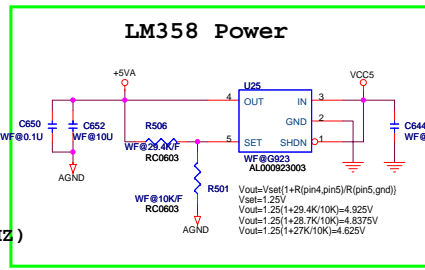
10/30 modify to +3V

A:(8/29) reserve 100u for VIN

PROJECT : PF1
Quanta Computer Inc.

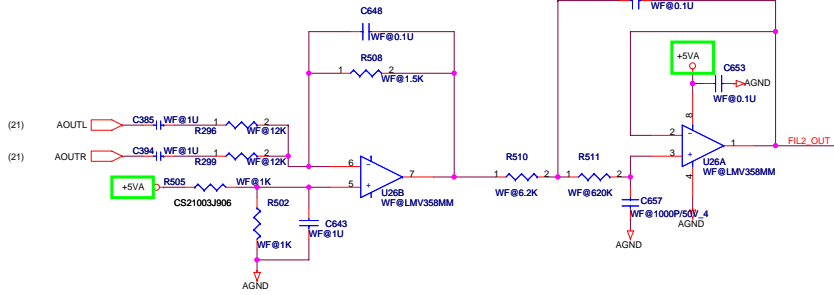
Size	Document Number	Rev
	MXM CONNECTOR / TV	2A
Date:	Tuesday, May 27, 2008	Sheet 20 of 40

Subwoofer



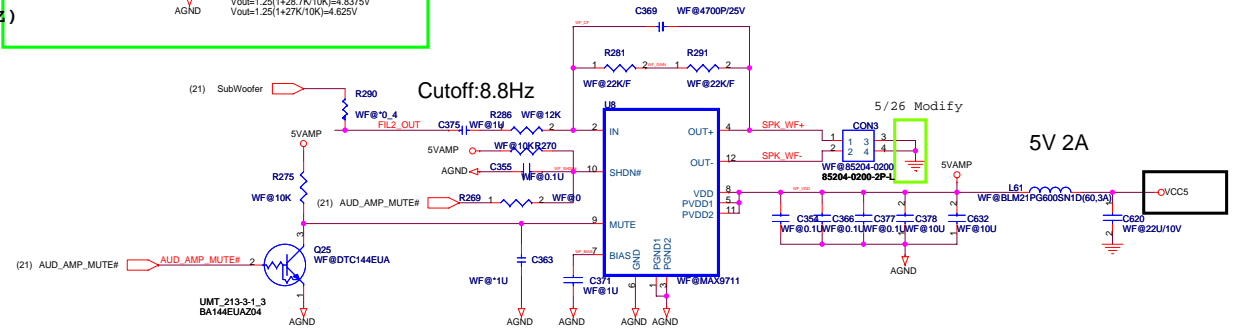
Mixer & 1nd order low pass filter(338Hz)

2nd order low pass filter(338Hz)



Cutoff:770Hz

Cutoff:8.8Hz

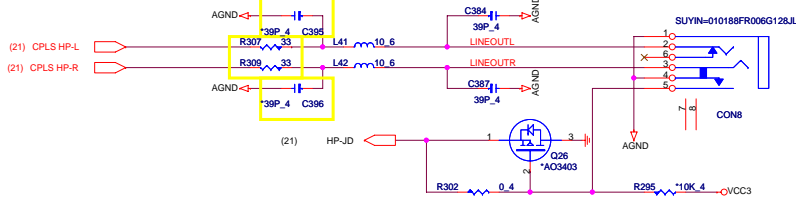


HP

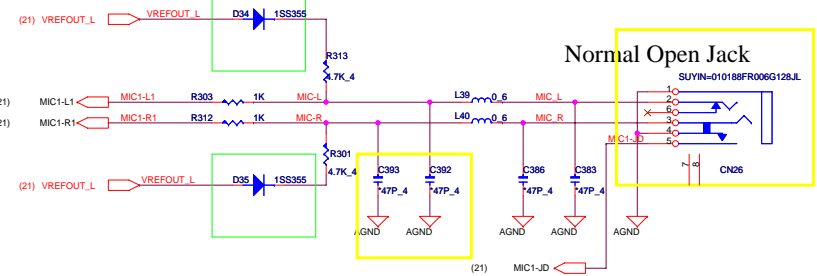
SYSTEM MIC

Normal Open Jack

HEADPHONE

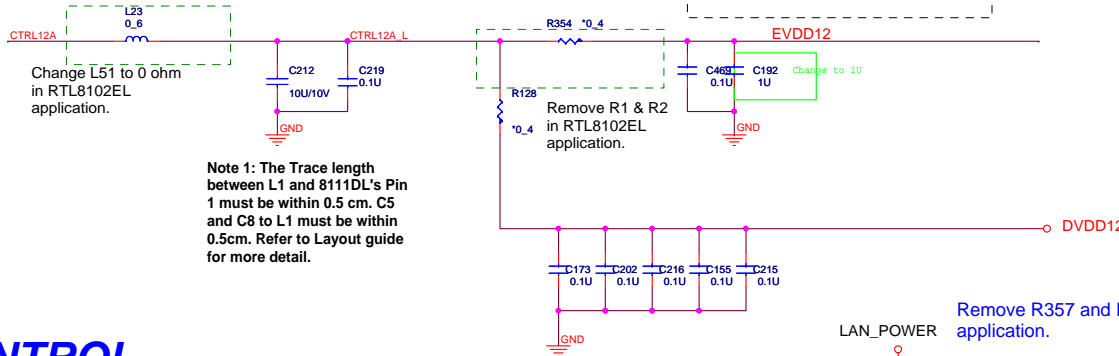
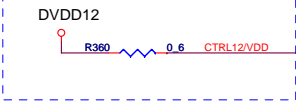


Add the diode to improve cross-talk 1/17



LAN_REALTEK_RTL8102E

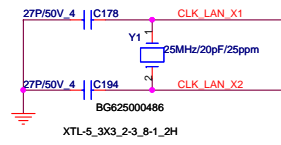
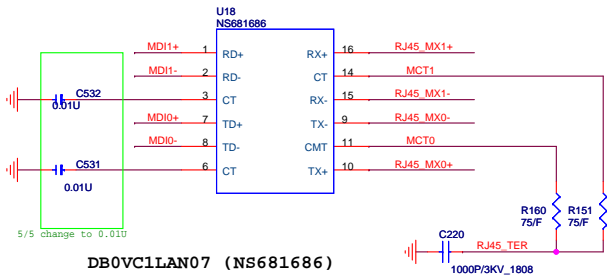
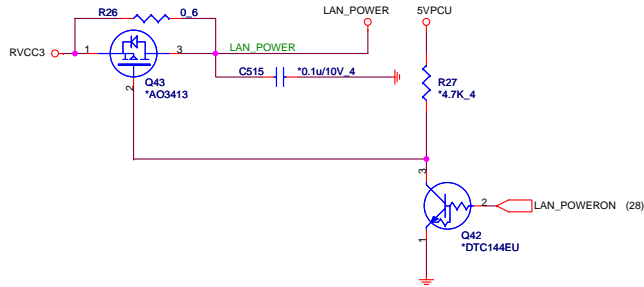
For RTL8102EL, use this block.



Change L51 to 0 ohm in RTL8102EL application.

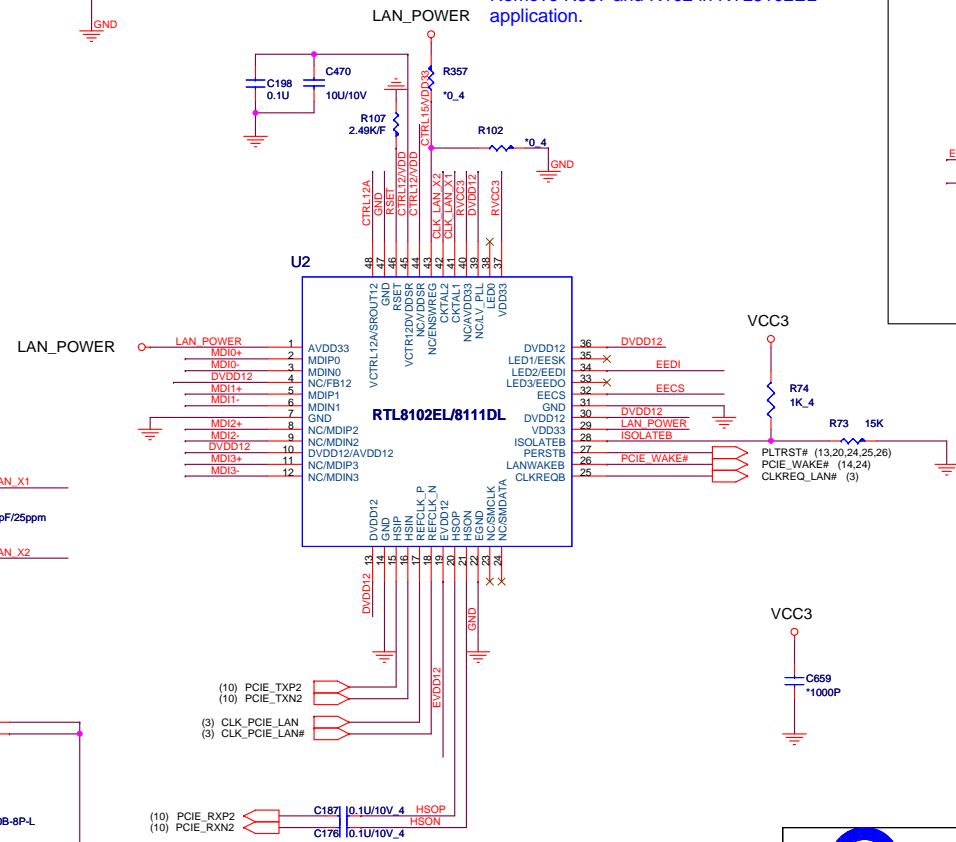
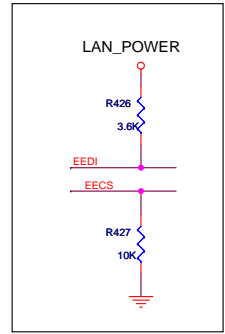
Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

LAN POWER CONTROL

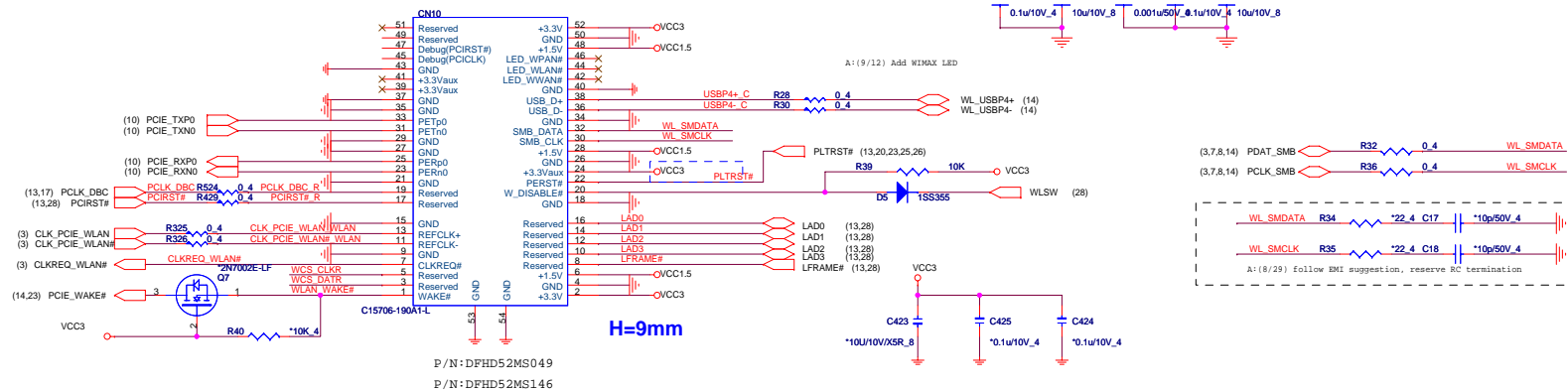


Remove R357 and R102 in RTL8102EL application.

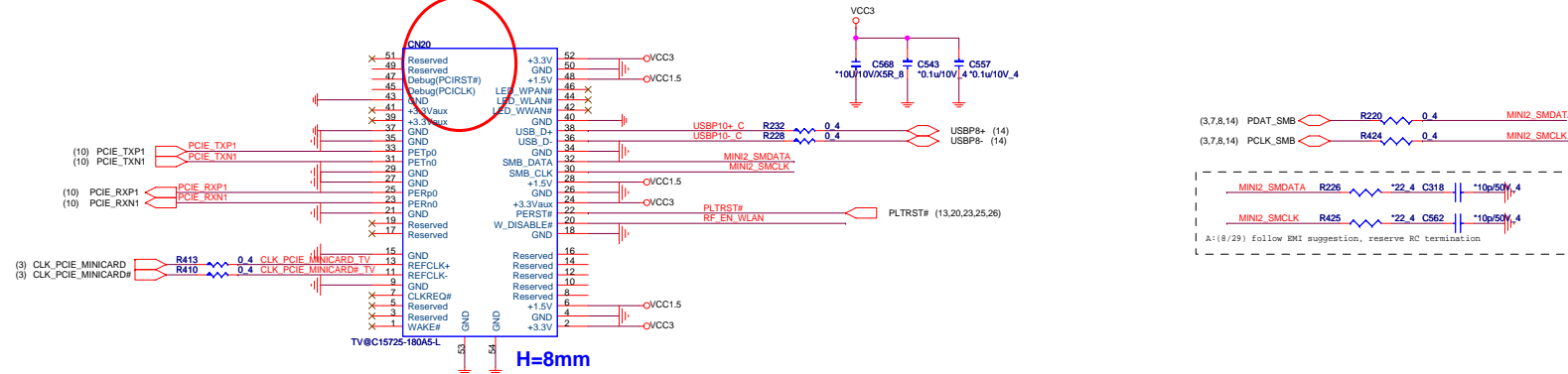
Fix PXE issue (ADD for B+)



MINI-Card I (WLAN)



MINI-Card II (TV)



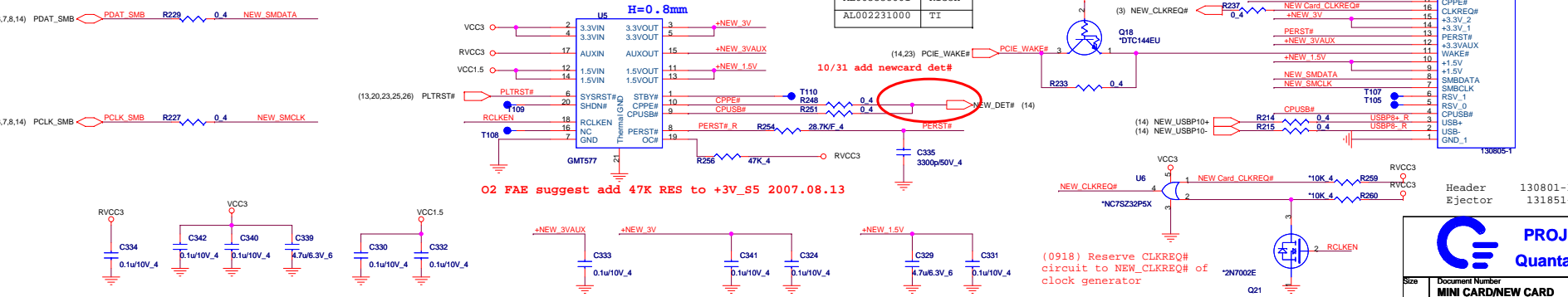
A: (9/7) per TI FAE suggestion:
 (1) Please keep all Input and Output capacitor value > 4.8uF (0.1uF +4.7uF)
 (2) Please put these caps closed to IC
 (3) R4101(pin 19,OC#) value should change to 2k ohm.

NEW CARD'S POWER SWITCH

CPPE# : (Internal Pull Up , active low when card support PCIe)
 CPUSB# : (Internal Pull Up , active low when card support USB)
 SHDN# : (Internal Pull Up)

New Card's Power Switch

QCI PN	Vendor
AL000577001	GMT
AL027C10003	OMC
AL005538001	Ricoh
AL002231000	TI

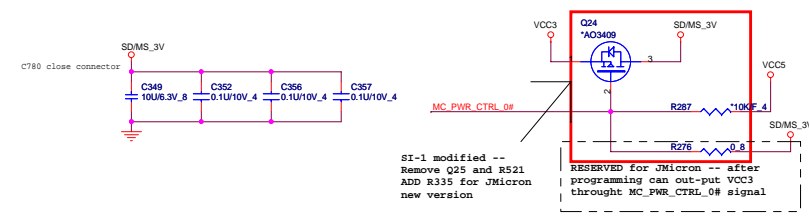
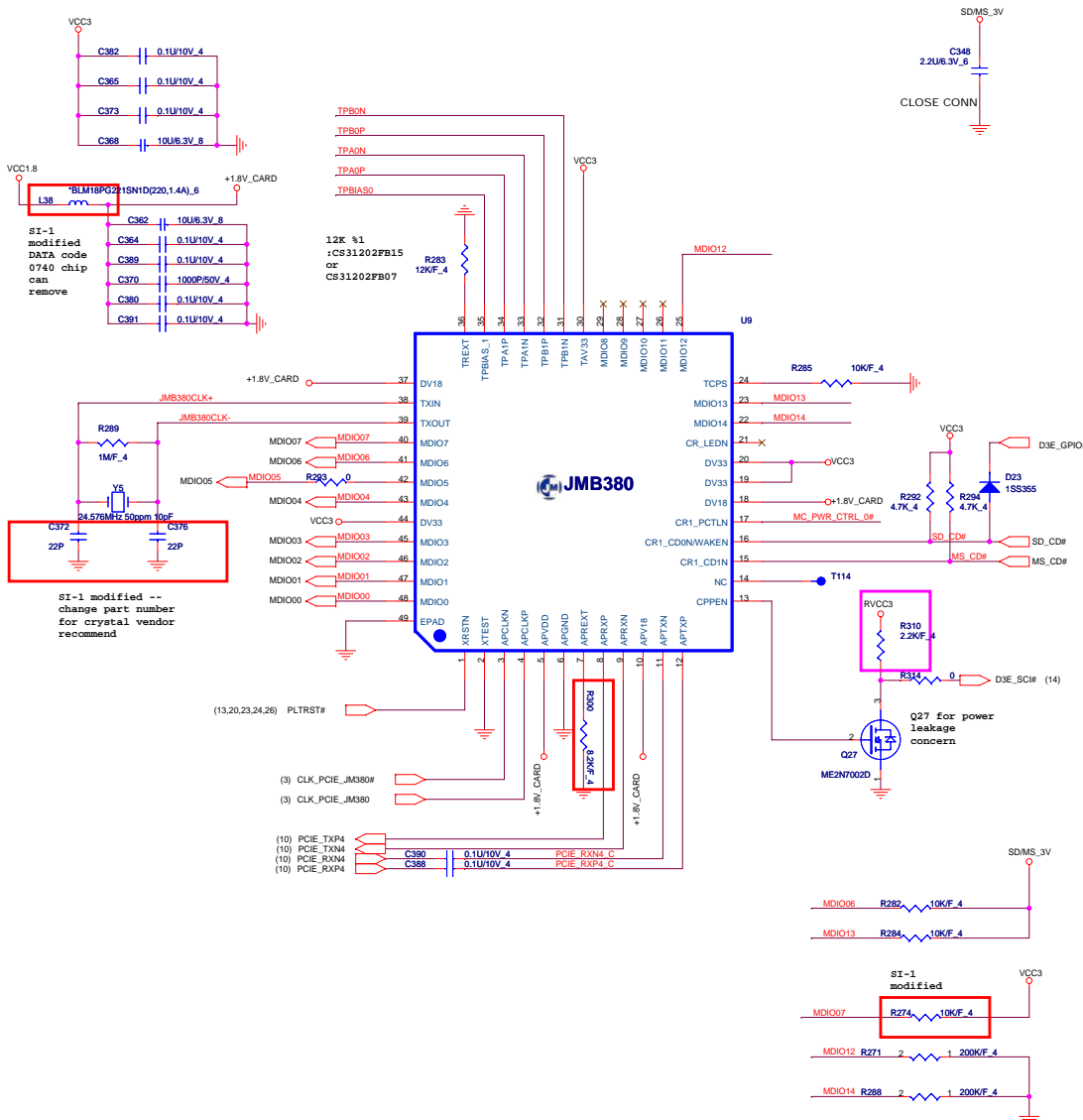


PROJECT : PF1
Quanta Computer Inc.

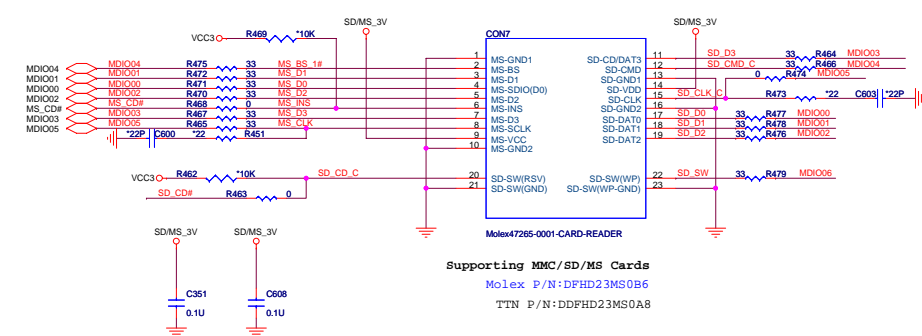
Header 130801-1 DFHD26MR074
 Ejector 131851-V FBBL5001010

Size Document Number
MINI CARD/NEW CARD
 Rev 2A

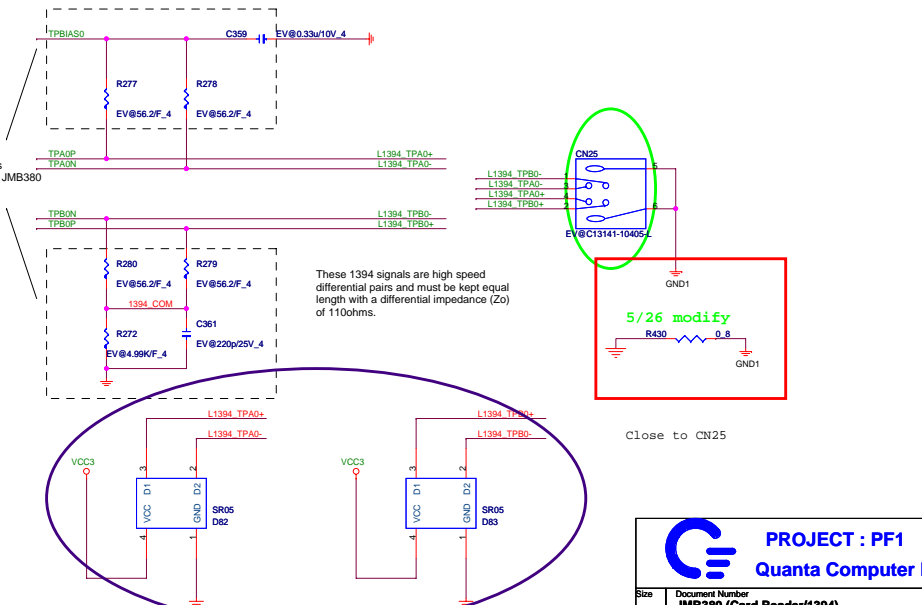
Date: Tuesday, May 27, 2008 Sheet 24 of 40

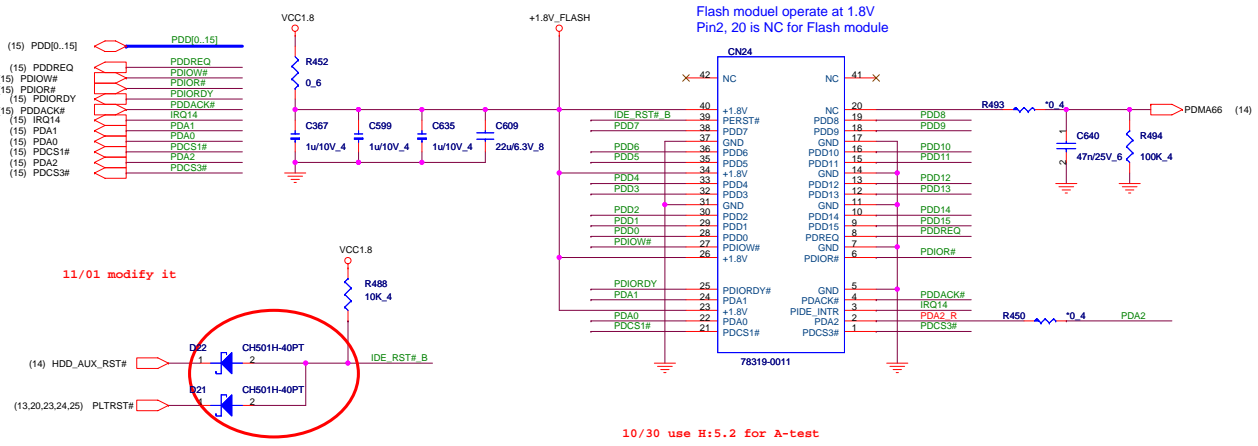


4 IN 1 CONN



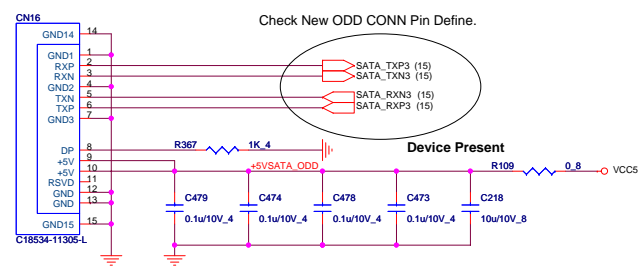
1394





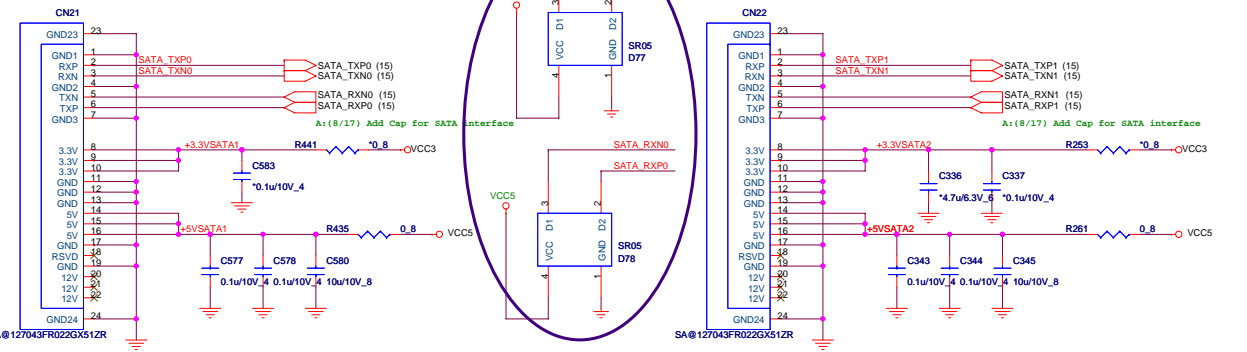
SATA ODD

9/28 change to SATA ODD conn to BD3G use

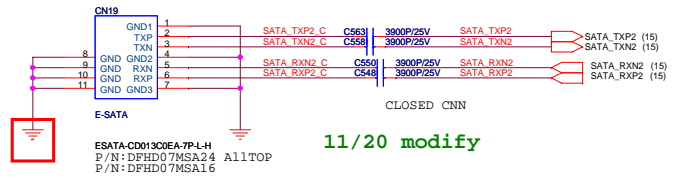


SATA HDD

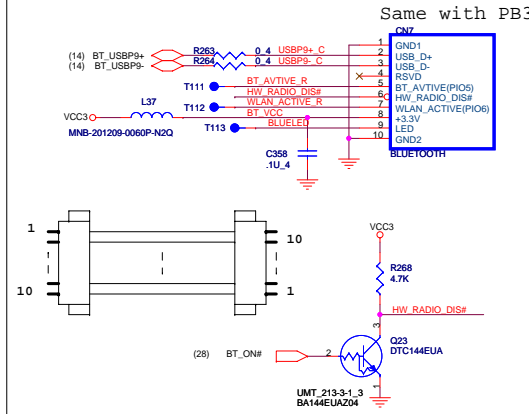
2'nd SATA HDD



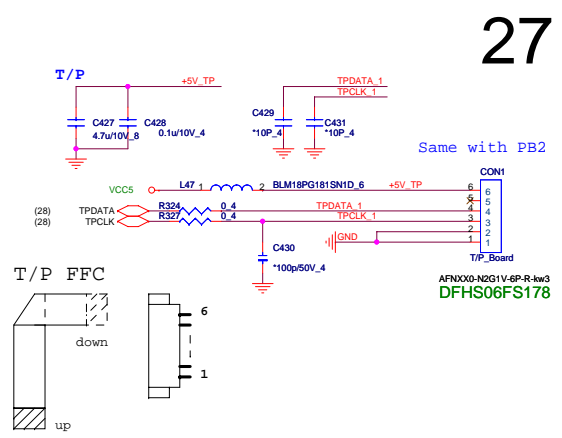
E-SATA CNN



BLUETOOTH MODULE CONNECTOR



To TP board

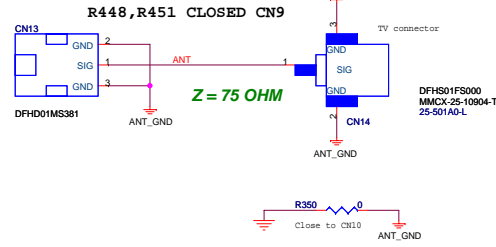


27

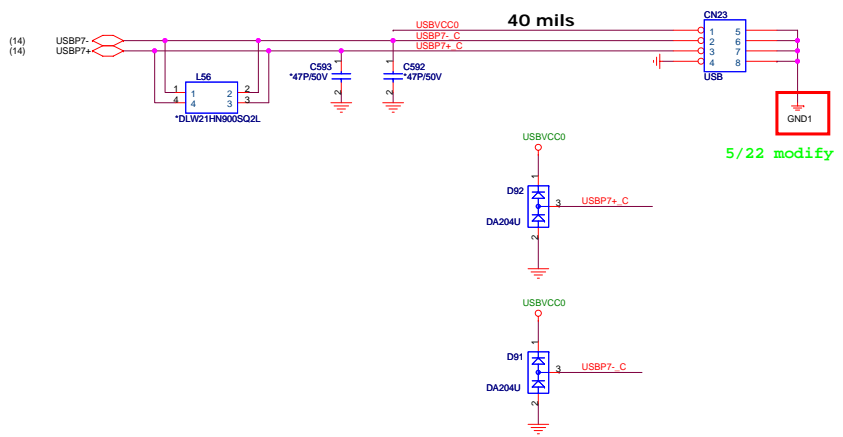
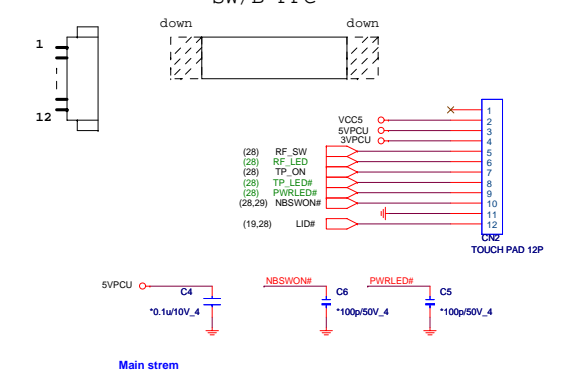
ON MB USB



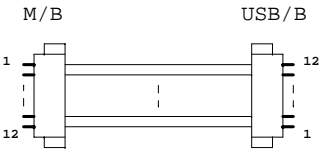
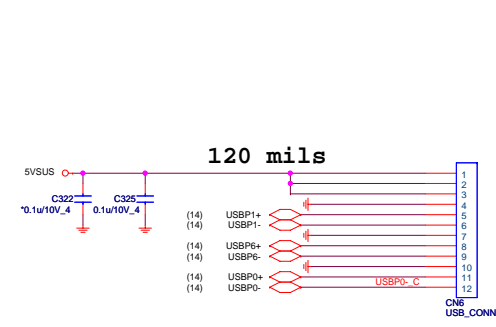
ANT. CONNECTOR

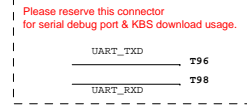
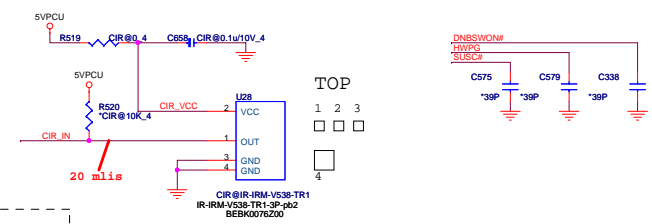
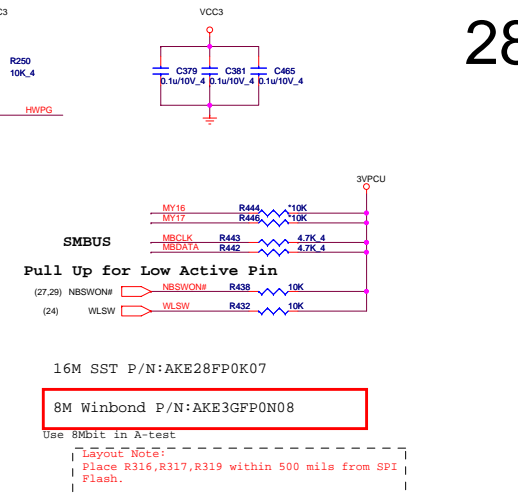
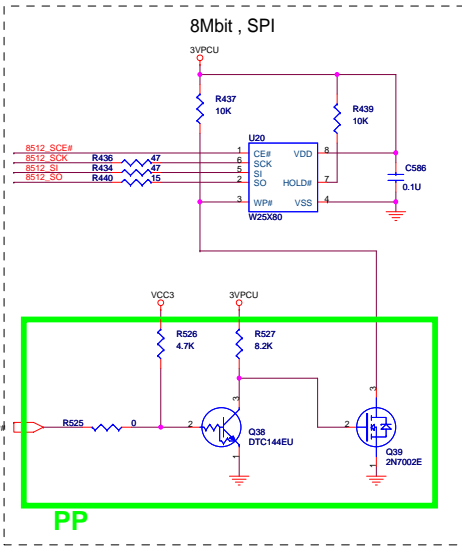
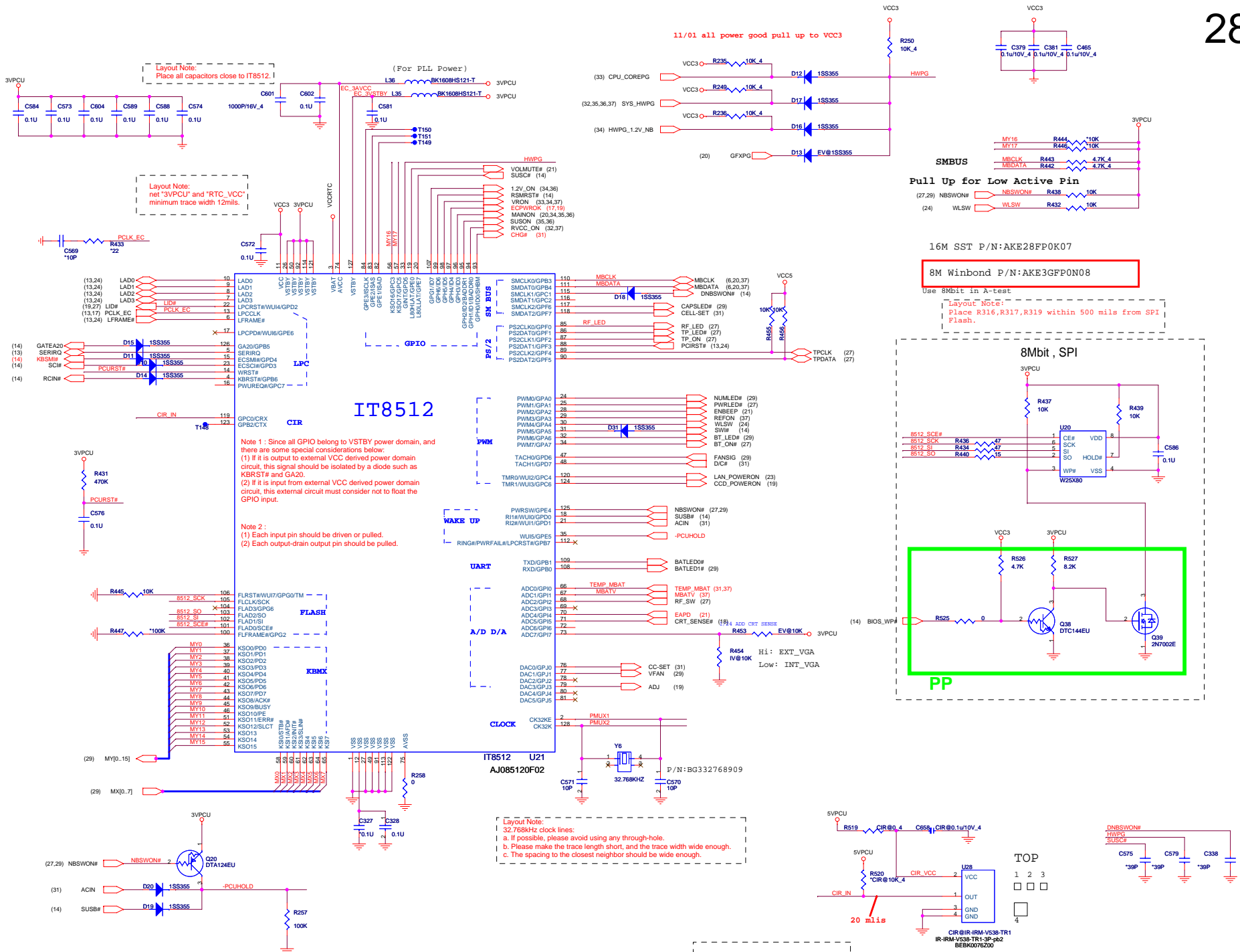


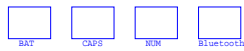
To SW board



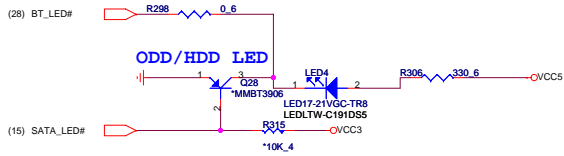
To USB board







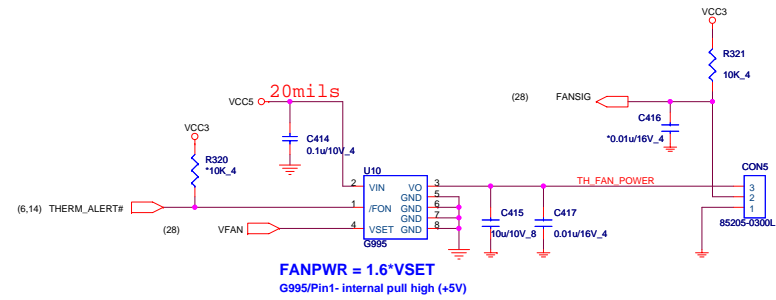
BATTERY CHARGE LED



CAPS LED



Number Lock LED



FANPWR = 1.6*VSET
G995/Pin1- internal pull high (+5V)

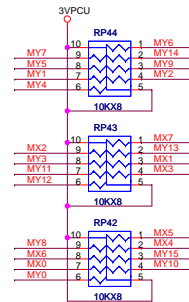
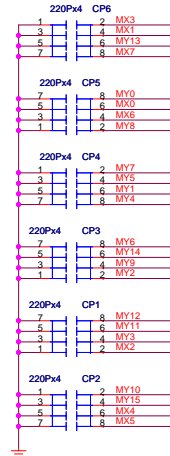
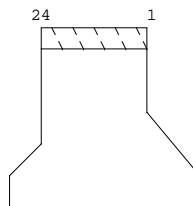
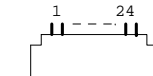
Keyboard CONN

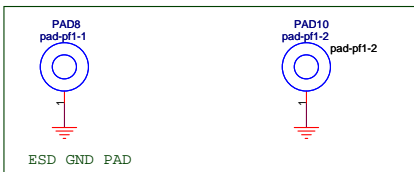
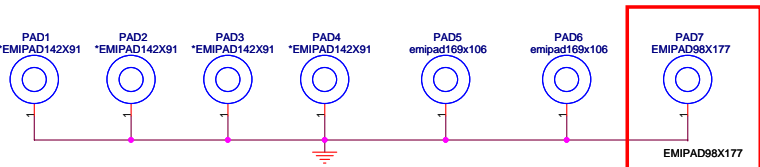
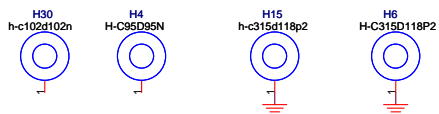
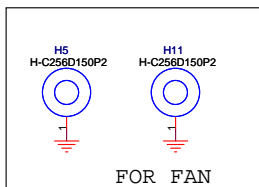
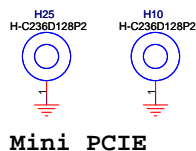
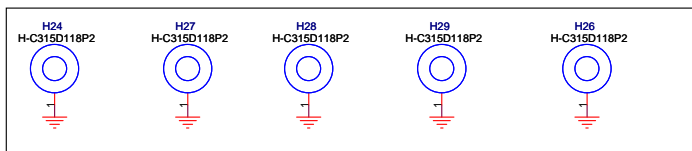
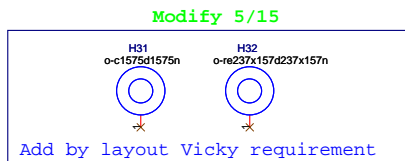
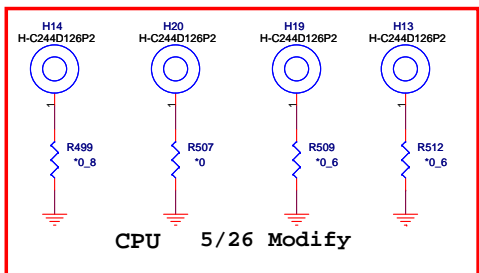
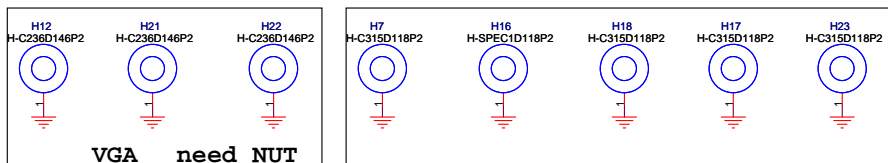
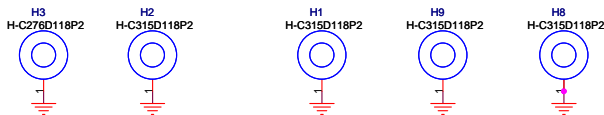


(28)	MY10	MY10	24	24
(28)	MY15	MY15	23	23
(28)	MX4	MX4	22	22
(28)	MX5	MX5	21	21
(28)	MY6	MY6	20	20
(28)	MX6	MX6	19	19
(28)	MY0	MY0	18	18
(28)	MX0	MX0	17	17
(28)	MY1	MY1	16	16
(28)	MX3	MX3	16	16
(28)	MY11	MY11	15	15
(28)	MX1	MX1	14	14
(28)	MY13	MY13	14	14
(28)	MX7	MX7	13	13
(28)	MY13	MY13	13	13
(28)	MX2	MX2	12	12
(28)	MY3	MY3	12	12
(28)	MY11	MY11	11	11
(28)	MY1	MY1	10	10
(28)	MY12	MY12	9	9
(28)	MY2	MY2	8	8
(28)	MY9	MY9	7	7
(28)	MY14	MY14	7	7
(28)	MY4	MY4	6	6
(28)	MY6	MY6	5	5
(28)	MY7	MY7	4	4
(28)	MY5	MY5	3	3
(28)	MY1	MY1	2	2
(28)	MY4	MY4	1	1

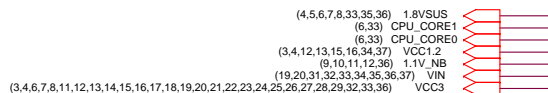
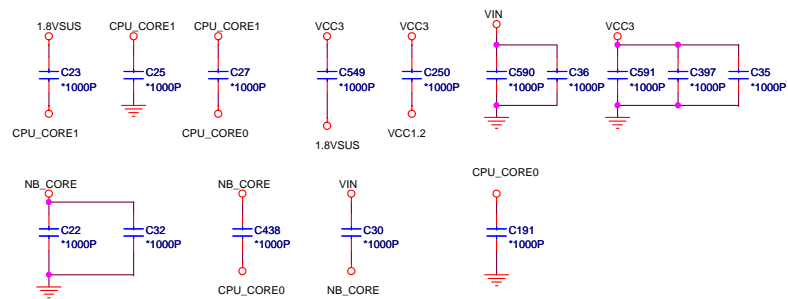
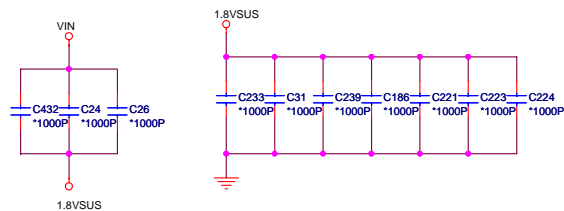
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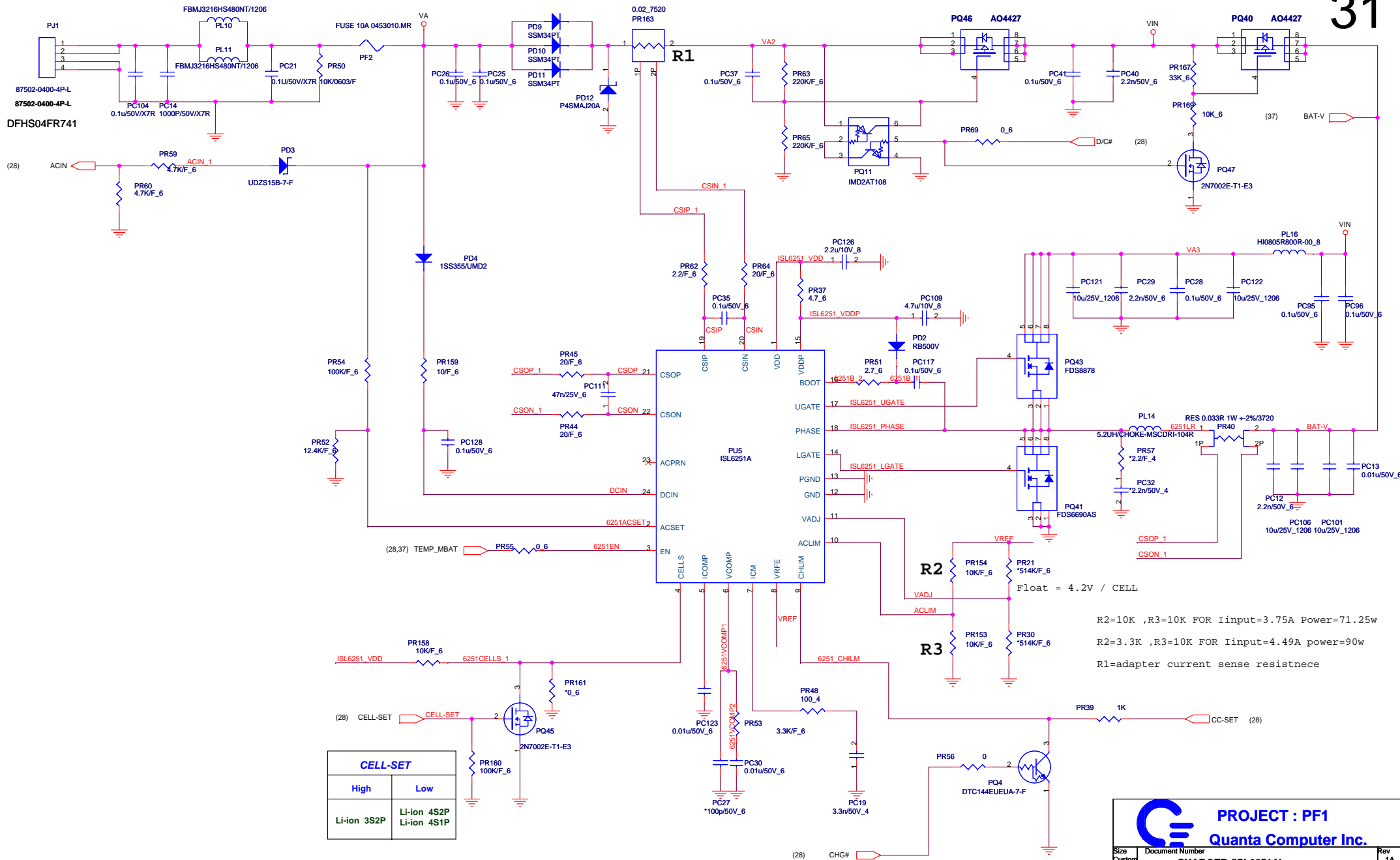
Bot contact





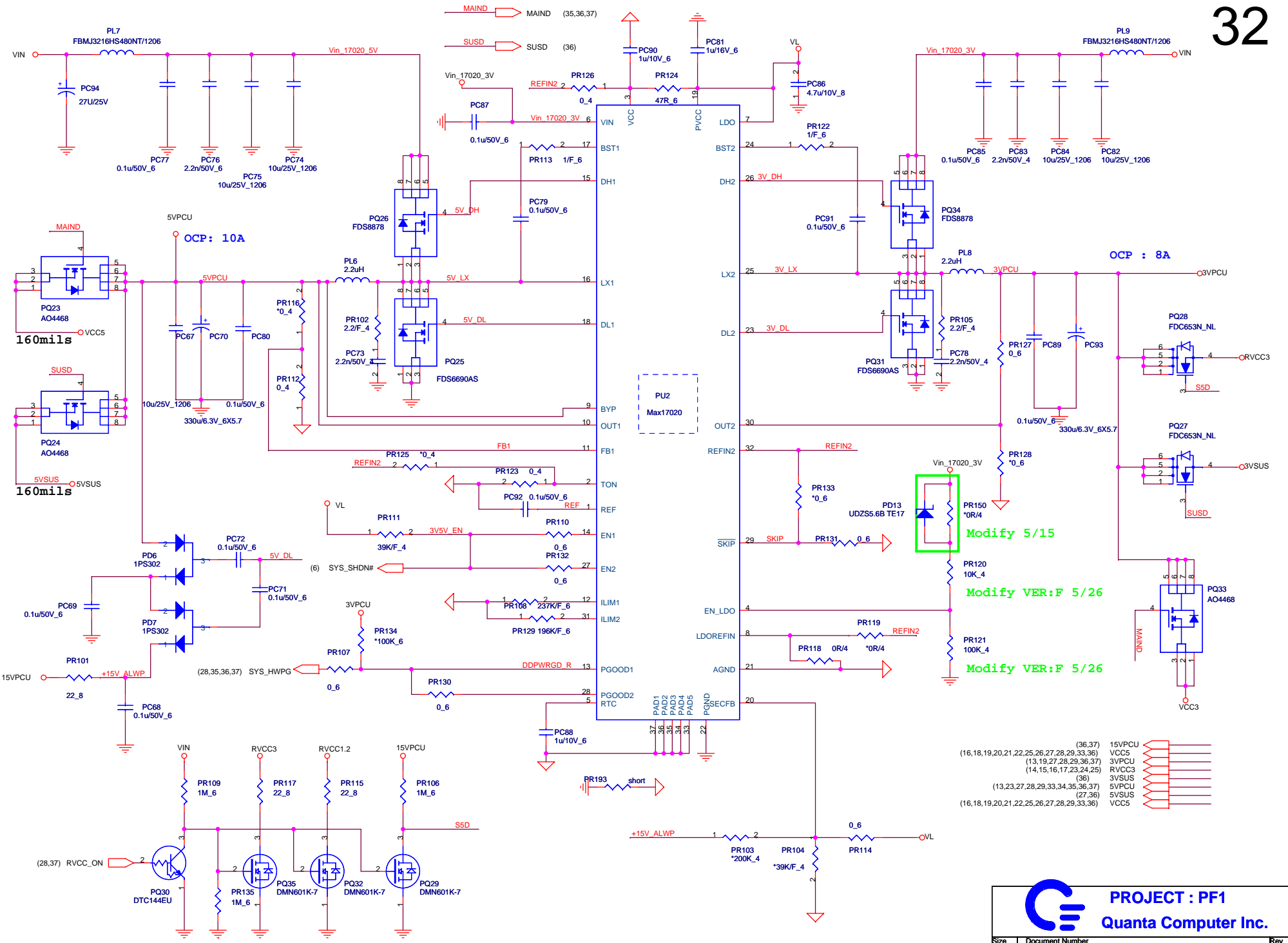
5/16 modify






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Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
Date: Tuesday, May 27, 2008	CHARGER (ISL6251A)	
	Sheet 31 of 40	

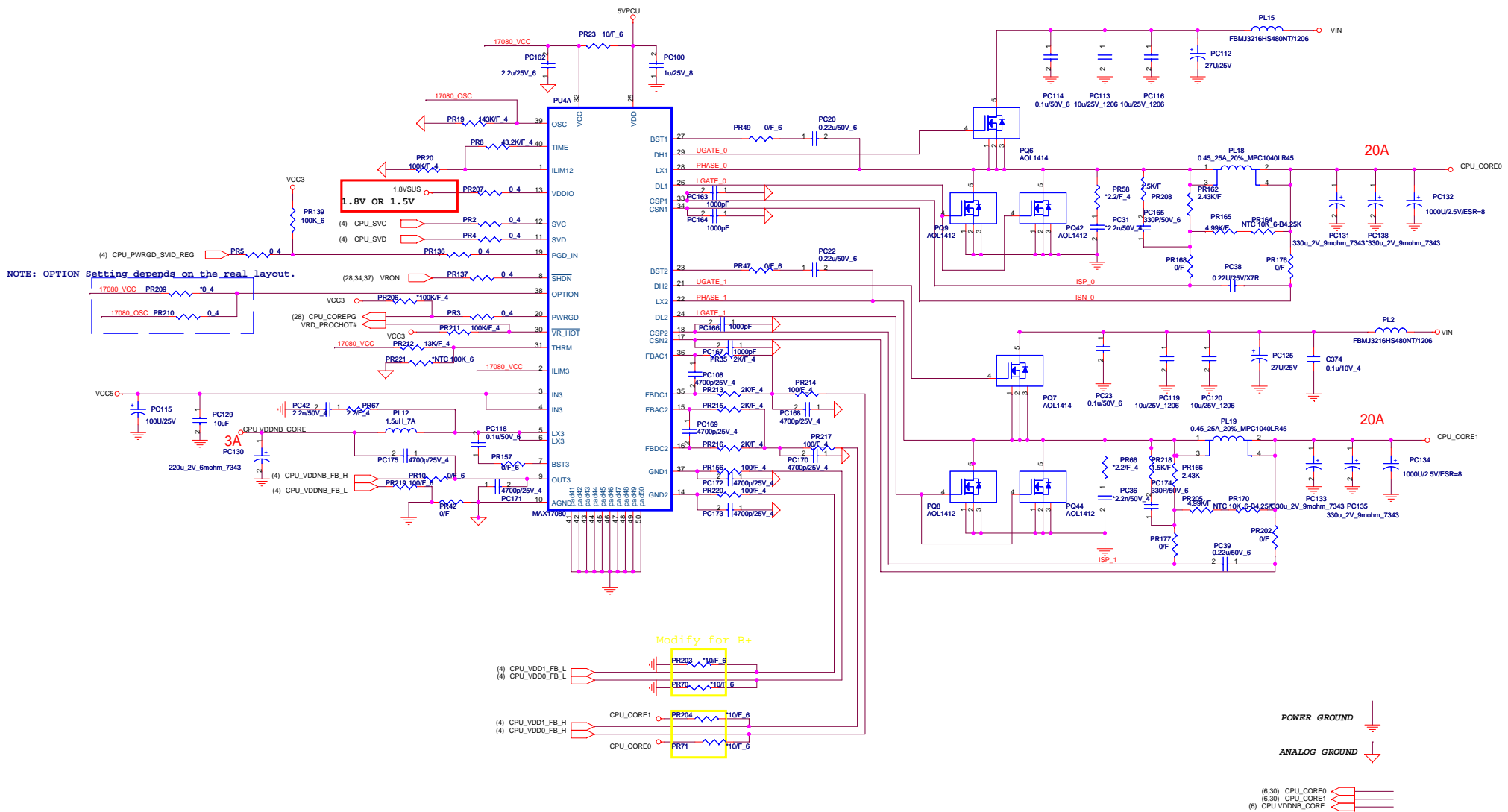


- (36,37) 15VPCU
- (16,18,19,20,21,22,25,26,27,28,29,33,36) VCC5
- (13,19,27,28,29,36,37) 3VPCU
- (14,15,16,17,23,24,25) RVCC3
- (35) 3VSUS
- (13,23,27,28,29,33,34,35,36,37) 5VPCU
- (27,36) 5VSUS
- (16,18,19,20,21,22,25,26,27,28,29,33,36) VCC5



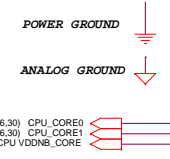
PROJECT : PF1
Quanta Computer Inc.

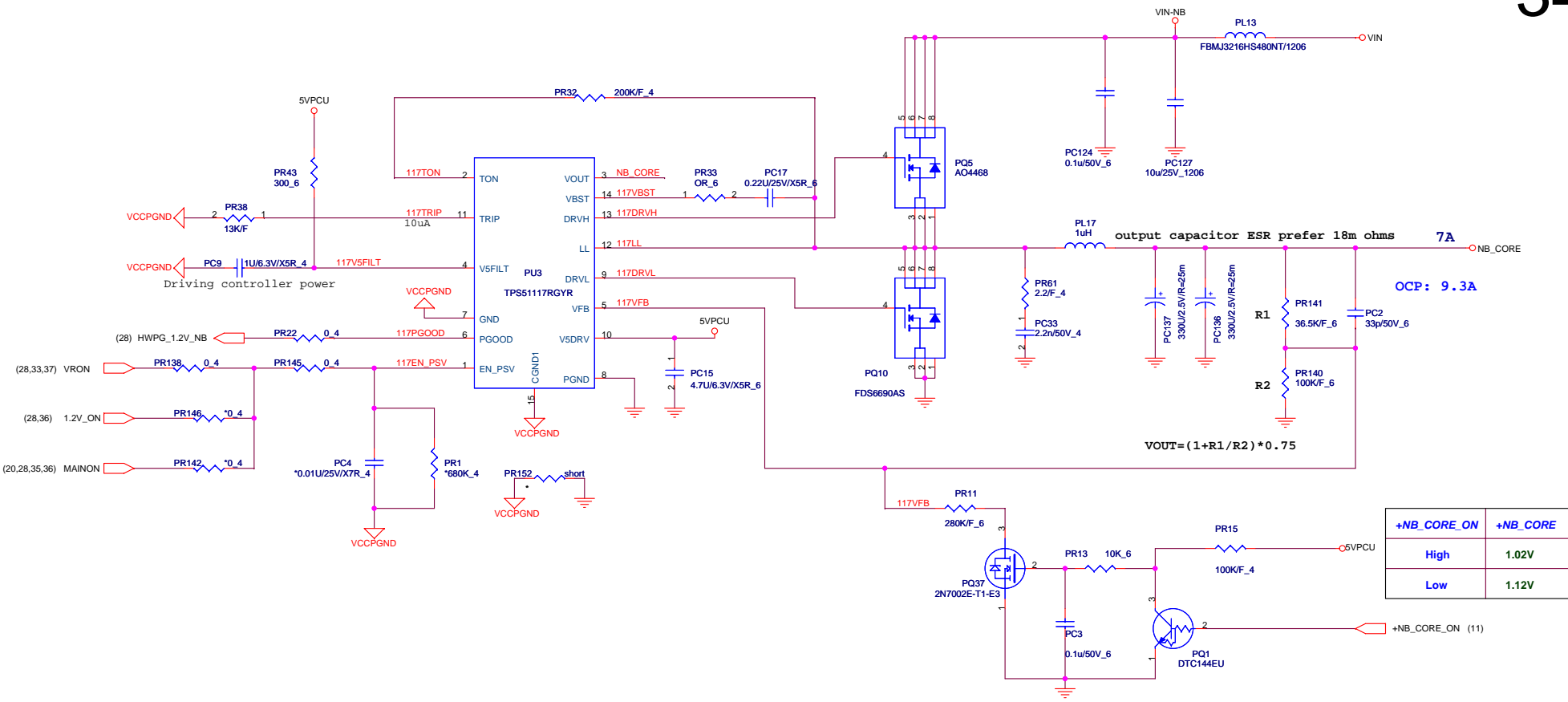
Size	Document Number	Rev
	SYSTEM 5V3V (ISL6237)	1A
Date:	Tuesday, May 27, 2008	Sheet 32 of 40



NOTE: OPTION Setting depends on the real layout.

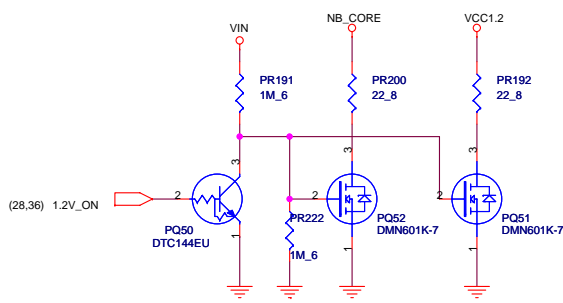
Modify for B+

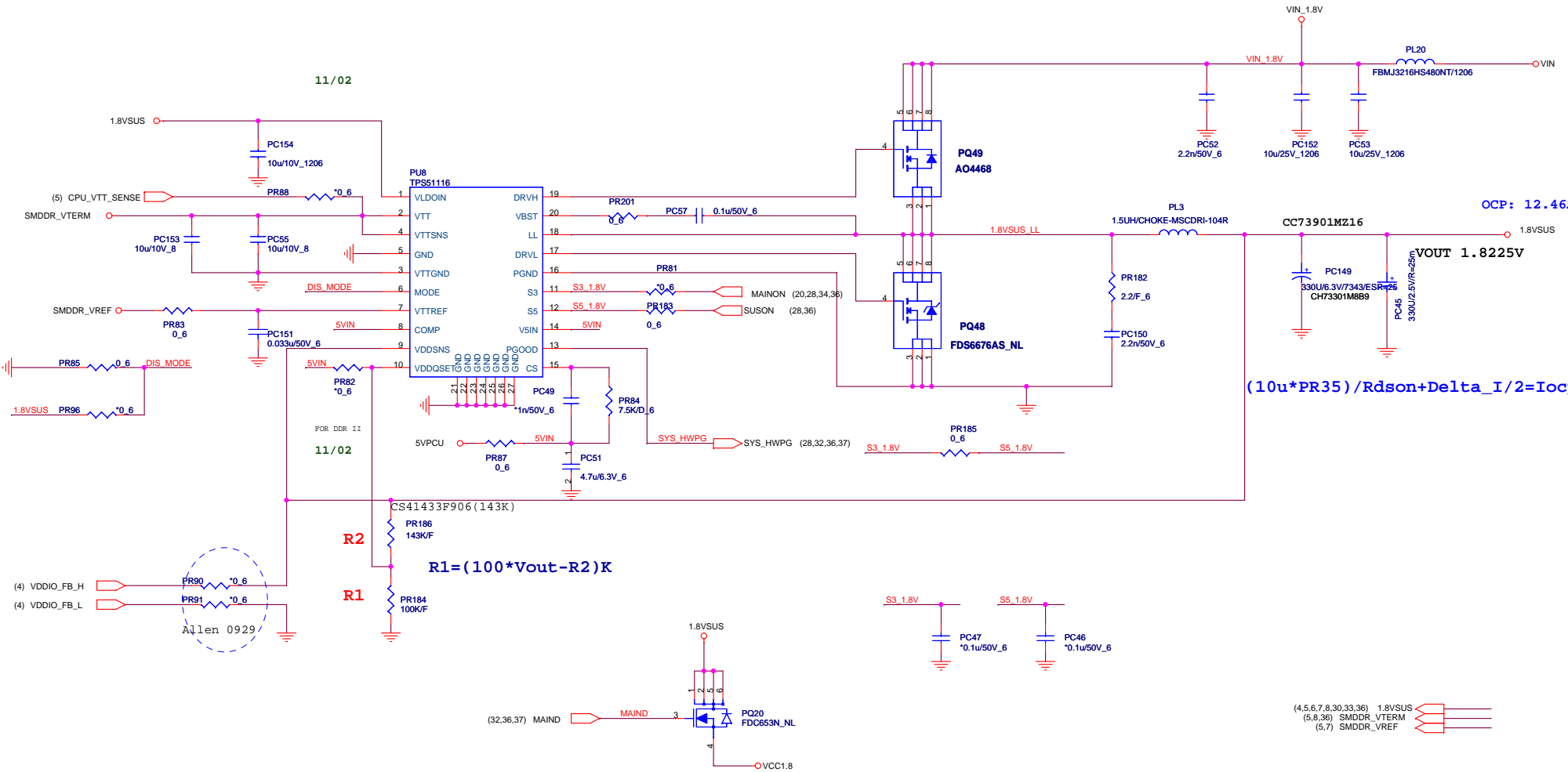




+NB_CORE_ON	+NB_CORE
High	1.02V
Low	1.12V

- (19,20,30,31,32,33,35,36,37) VIN
- (12,30) NB_CORE
- (3,4,12,13,15,16,30,37) VCC1.2
- (13,23,27,28,29,32,33,35,36,37) 5VPCU
- (3,4,6,7,8,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,32,33,36)
- VCC3



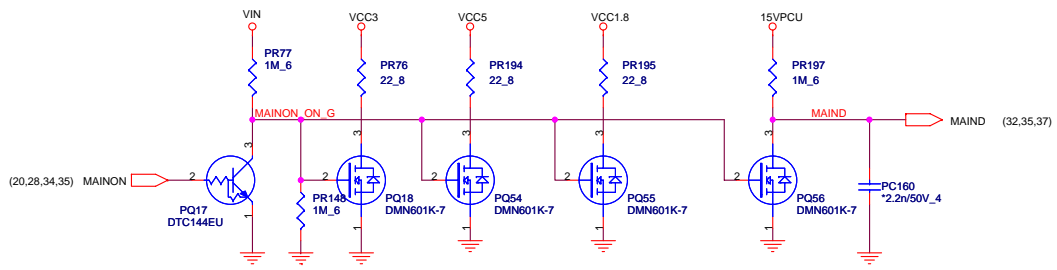
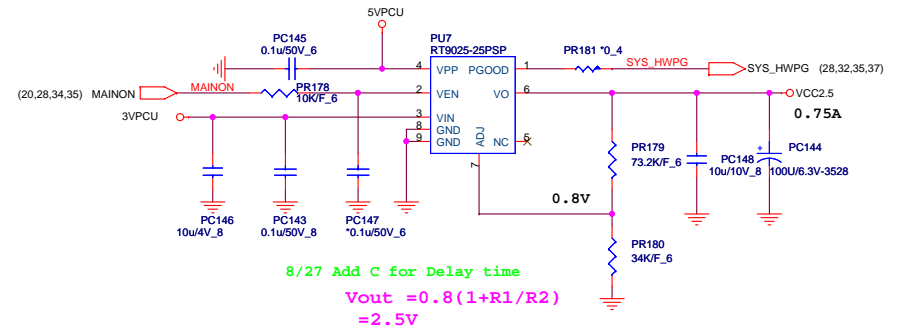
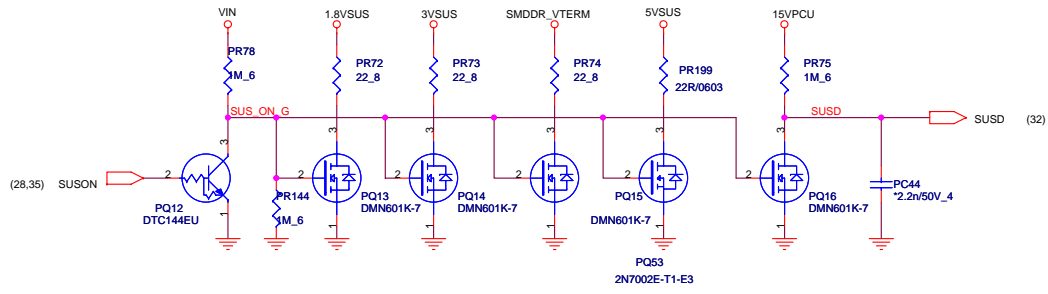
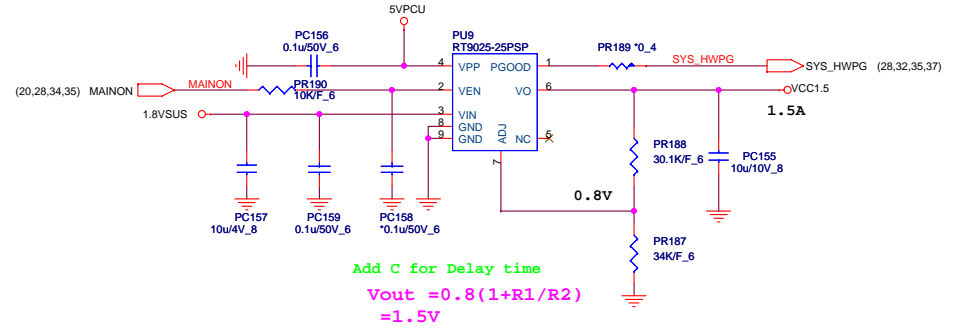
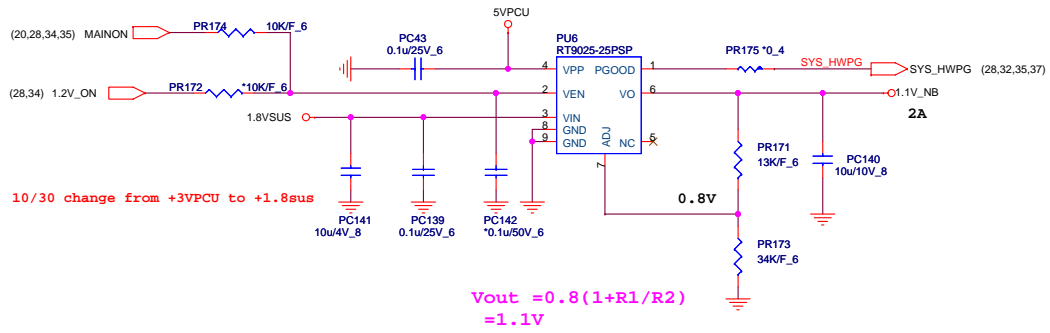


OCP: 12.46A

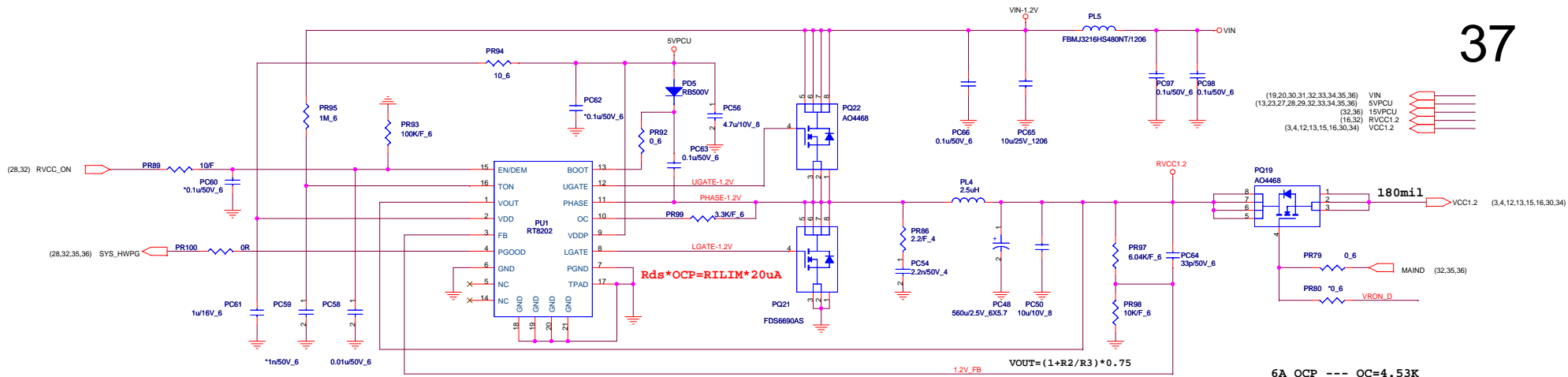
VOUT 1.8225V

$(10u * PR35) / R_{dson} + \Delta I / 2 = I_{ocp}$

$R1 = (100 * V_{out} - R2) K$

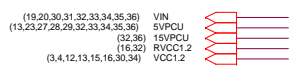


- (24) VCC1.5
- (4) VCC2.5
- (9,10,11,12) 1.1V_NB

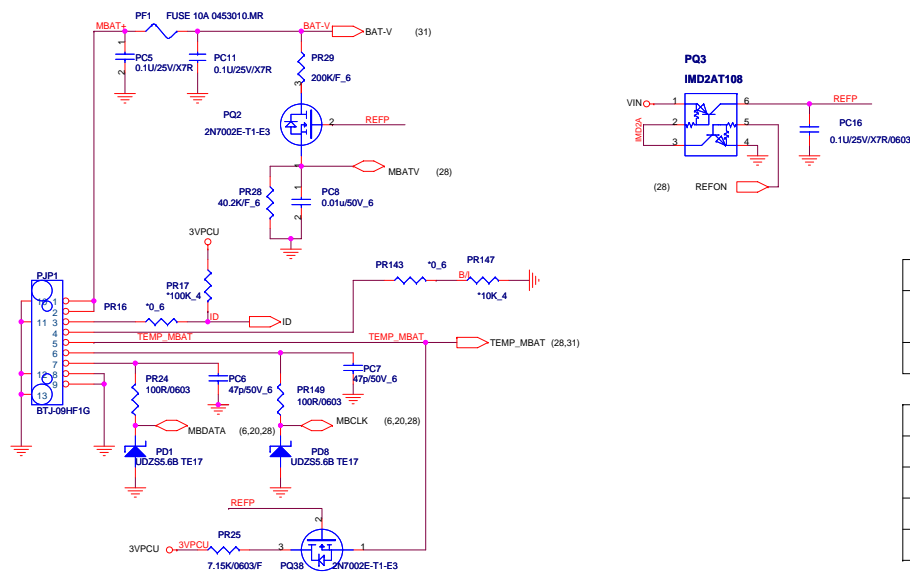
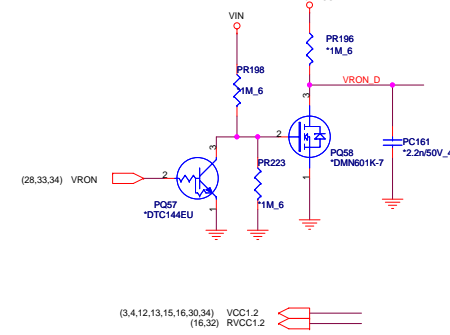


$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

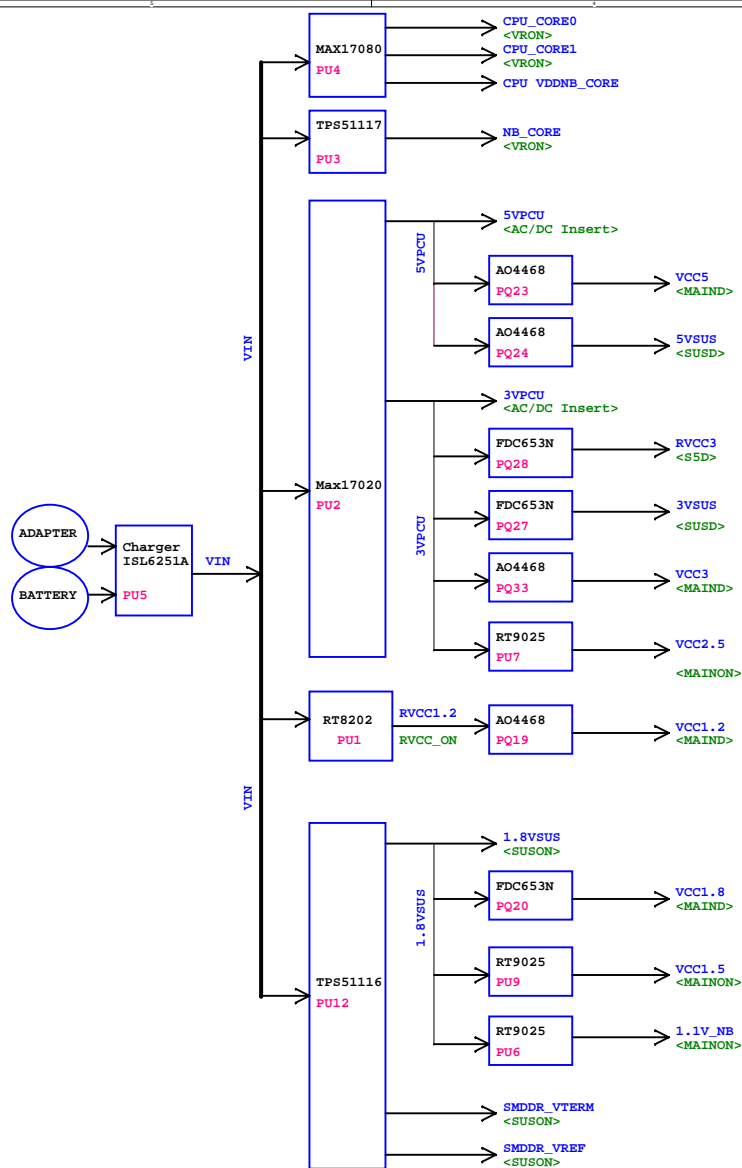


6A OCP --- OC=4.53K
FDS6690AS Rds=15mOhm



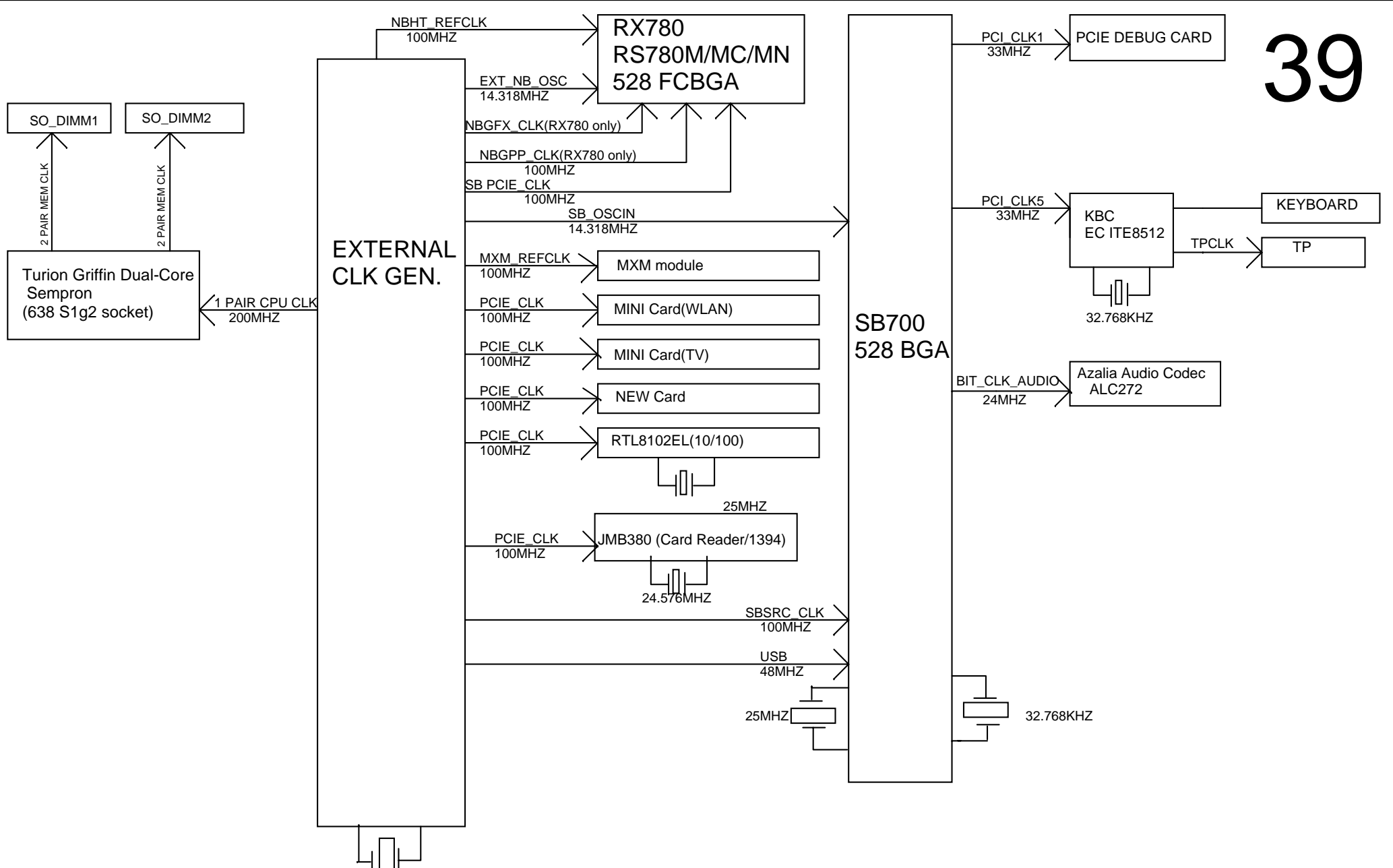
MBATV voltage :	
Li-ion 4s*P	$16.8V * 40.2 / (200 + 40.2) = 2.812V$ $12.0V * 40.2 / (200 + 40.2) = 2.008V$
Ni-MH 8S1P	$8.0V * 40.2 / (200 + 40.2) = 1.34V$

TEMP_MBAT voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V



Below table need be modify (waiting other schematic ready)

POWER	Distribution
VCC_CORE	CPU
5VPCU	Battery LED , Power LED , CIR , RTC
3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
NB_CORE	RS780MC
VCC5	CAMERA , Card Reader LED , ODD/HDD LED , T/P , T/sensor , CRT , HDMI , SB700 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
VCC3	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , DVI , REQUIRED STRAPS , DEBUG STRAPS , SB700 , RS780MC , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , Headphone , EC , LAN , Audio Codec
RVCC3	WLAN , NEW CARD , SB700 , MXM , LAN
3VSUS	SB700
VCC2.5	CPU
RVCC1.2	SB700
1.8VSUS	SB700 , DDR , CPU , HDT
VCC1.8	SB700 , LCD , LVDS , RS780MC
VCC1.2	SB700 , RS780MC , CPU , WLAN , TV , NEW CARD
SMDDR_VTERM	DDR , CPU
SMDDR_VREF	DDR
5VSUS	USB



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	Clock distribution diagram	2A

