NIPPON PRECISION CIRCUITS INC.

SM5819AF

6-channel DSD-PCM Converter

OVERVIEW

The SM5819AF is a 6-channel DSD data (64fs) to 4fs, 2fs or fs PCM data converter. During conversion, decimation filtering is performed using a filter with selectable fixed coefficients (3 sets). Also, DSD inputs and PCM outputs are available for use in master/slave clock mode operation, in a wide range of system configurations, making it easy to construct a multi-channel DSD/PCM reproduction system.

FEATURES

- 512fs (22.5792MHz, fs = 44.1kHz), 1:2 to 2:1 duty master clock
- DSD input and PCM output clock master/slave switching
- 3-system external data input (3-wire format), PCM output data/BCK/LRCK external input and internal filter output switching
  (BCK and LRCK are common to all 3 external PCM data inputs)
- Decimation filter coefficients
  - Fixed coefficients: 4fs-1/2fs-1/fs-1
- PCM output mute operation
- PCM output format: [MSB-first left-justified 32-bit] or [IIS 32-bit]
  (IIS 32-bit output bit clock frequency = 64 × word clock frequency)
- FIR filter coefficients
  - 64fs → 4fs/2fs/fs: 480th-order (6-channel)
  - ROM coefficients: 24 valid data bits (4-bit MSB extension at 4fs, 5-bit MSB extension at 2fs/fs)
- + 6dB DSD gain switching function
- External/Internal system clock output switching
- 3.3V (3.0 to 3.6V) and 2.5V (2.3 to 2.7V) power supplies
- – 40 to 85°C operating temperature range
- 48-pin QFP package

APPLICATIONS

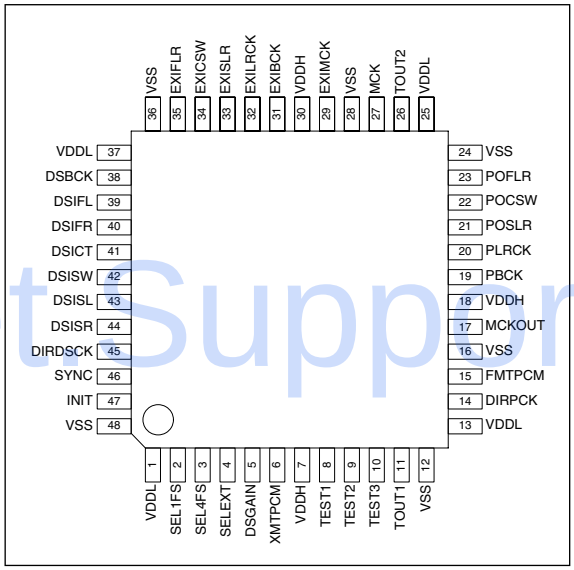
- Multi-channel SA-CD players
- SA-CD-compatible AV amplifiers

ORDERING INFORMATION

Device	Package
SM5819AF	48 -pin QFP

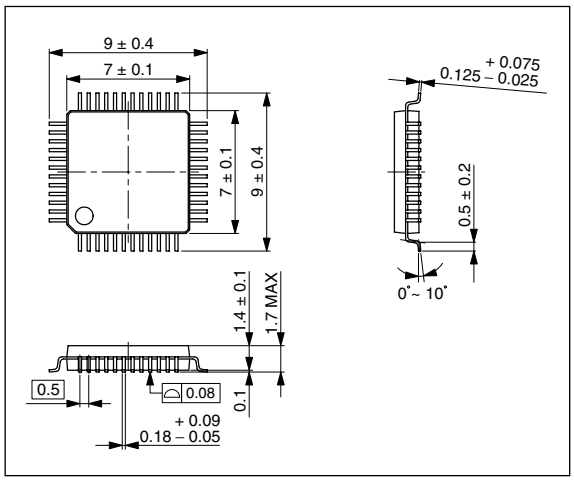
PINOUT

(Top view)



PACKAGE DIMENSIONS

(Unit: mm)



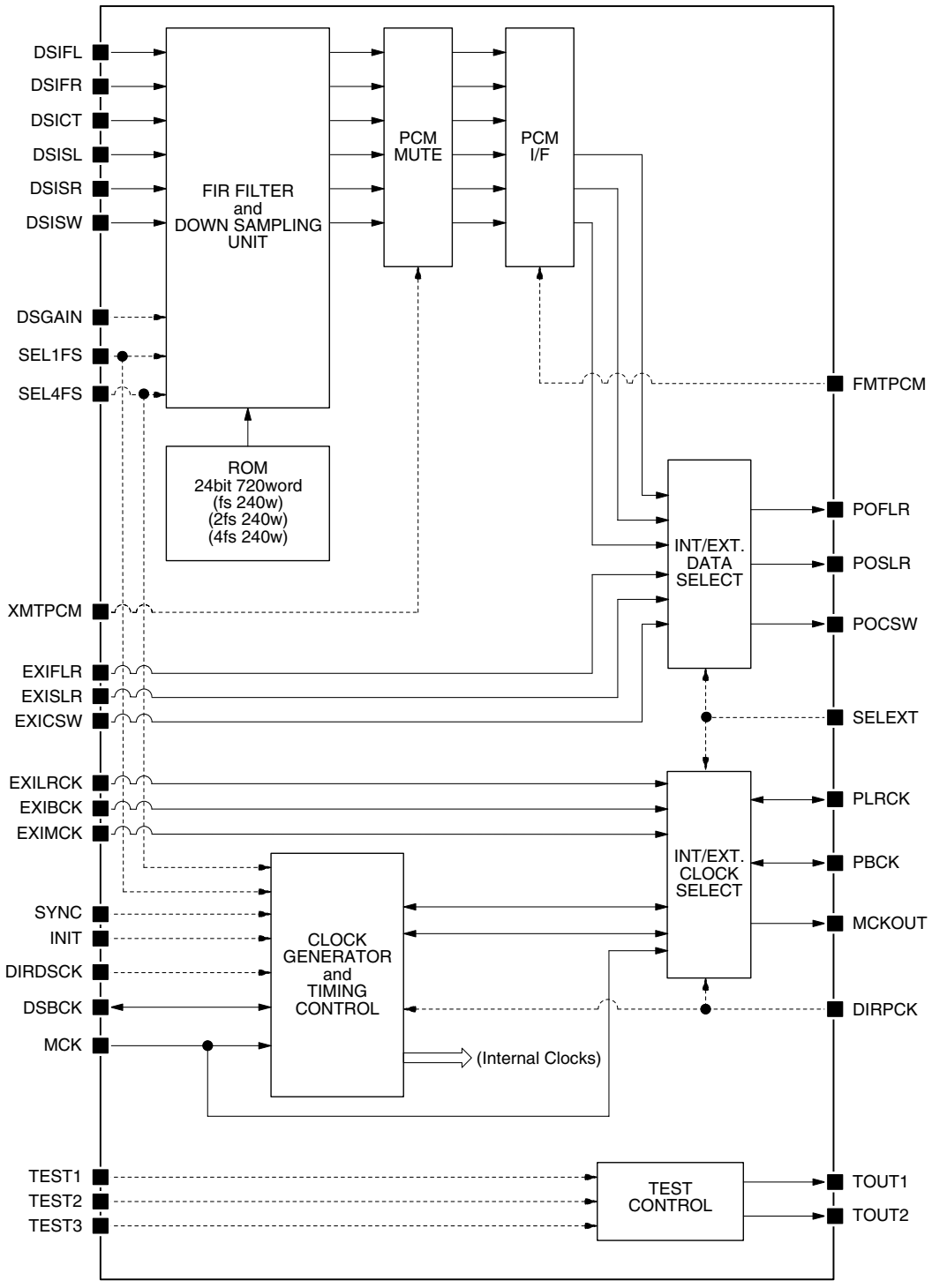
PIN DESCRIPTION

No.	Name	I/O	Property[1]	Input voltage	Description
1	VDDL	–	–	2.5V	Core power supply
2	SEL1FS	I	PD	3.3V	PCM output rate select 1 L: 2fs/4fs, H: fs
3	SEL4FS	I	PD	3.3V	PCM output rate select 2 L: 2fs, H: 4fs
4	SELEXT	I	PD	3.3V	fs/2fs/4fs output and external data output select L: fs/2fs/4fs data, H: external data (EXI**)
5	DSGAIN	I	PD	3.3V	DSD signal gain setting L: 100% modulation = 0dB, H: 50% modulation = 0dB
6	XMTPCM	I	PD	3.3V	PCM output mute control input L: Mute ON, H: Mute OFF
7	VDDH	–	–	3.3V	I/O power supply
8	TEST1	I	PD	3.3V	Test input 1 (must be open or tie LOW for normal operation)
9	TEST2	I	PD	3.3V	Test input 2 (must be open or tie LOW for normal operation)
10	TEST3	I	PD	3.3V	Test input 3 (must be open or tie LOW for normal operation)
11	TOUT1	O	–	–	Test output 1
12	VSS	–	–	–	Ground
13	VDDL	–	–	2.5V	Core power supply
14	DIRPCK	I	PD	3.3V	PCM output PBCK/PLRCK I/O select L: Output (master mode), H: Input (slave mode)
15	FMTPCM	I	PD	3.3V	PCM output format select L: MSB-first left-justified 32-bit, H: IIS 32-bit
16	VSS	–	–	–	Ground
17	MCKOUT	O	12mA	–	System clock output (selected by SELEXT)
18	VDDH	–	–	3.3V	I/O power supply
19	PBCK	I/O	S, 6mA	3.3V	PCM output BCK bit clock
20	PLRCK	I/O	S, 6mA	3.3V	PCM output LRCK word clock
21	POSLR	O	2mA	–	PCM data output: surround left/right-channel
22	POCSW	O	2mA	–	PCM data output: center/subwoofer channel
23	POFLR	O	2mA	–	PCM data output: front left/right-channel
24	VSS	–	–	–	Ground
25	VDDL	–	–	2.5V	Core power supply
26	TOUT2	O	–	–	Test output 2
27	MCK	I	–	3.3V	Master clock input: 512fs (22.5792MHz, fs = 44.1kHz)
28	VSS	–	–	–	Ground
29	EXIMCK	I	–	3.3V	External system clock input
30	VDDH	–	–	3.3V	I/O power supply
31	EXIBCK	I	S	3.3V	External PCM data BCK bit clock input
32	EXILRCK	I	S	3.3V	External PCM data LRCK word clock input
33	EXISLR	I	–	3.3V	External PCM data input: surround left/right-channel
34	EXICSW	I	–	3.3V	External PCM data input: center/subwoofer channel
35	EXIFLR	I	–	3.3V	External PCM data input: front left/right-channel
36	VSS	–	–	–	Ground
37	VDDL	–	–	2.5V	Core power supply
38	DSBCK	I/O	S, 6mA	3.3V	DSD data input bit clock. Controlled by DIRDSCK

No.	Name	I/O	Property[1]	Input voltage	Description
39	DSIFL	I	–	3.3V	DSD data input: front left-channel
40	DSIFR	I	–	3.3V	DSD data input: front right-channel
41	DSICT	I	–	3.3V	DSD data input: center channel
42	DSISW	I	–	3.3V	DSD data input: subwoofer channel
43	DSISL	I	–	3.3V	DSD data input: surround left-channel
44	DSISR	I	–	3.3V	DSD data input: surround right-channel
45	DIRDSCK	I	PD	3.3V	DSBCK I/O select L: input (slave), H: output (master)
46	SYNC	I	S, PU	3.3V	Forced synchronization input (active-HIGH edge)
47	INIT	I	S, PU	3.3V	Initialization input: Active-LOW, Resync on “L” → “H”
48	VSS	–	–	–	Ground

1. S = Schmitt, PU = pull-up resistor, PD = pull-down resistor, mA = output current

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage 1	V_{DDH}	– 0.3 to 4.0	V
Supply voltage 2	V_{DDL}	– 0.3 to 3.0	V
Input voltage (3.3V)	V_{IN}	– 0.3 to V_{DDH} + 0.5	V
Power dissipation	P_D	200	mW
Storage temperature range	T_{STG}	– 55 to 125	°C

Recommended Operating Conditions

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage 1	V_{DDH}	3.0 to 3.6	V
Supply voltage 2	V_{DDL}	2.3 to 2.7	V
Operating temperature	T_{OPR}	– 40 to 85	°C

DC Electrical Characteristics

V_{DDH} = 3.0 to 3.6V, V_{DDL} = 2.3 to 2.7V, V_{SS} = 0V, T_{OPR} = – 40 to 85°C unless otherwise noted.

Parameter		Pin	Symbol	Condition	Rating			Unit
					min	typ	max	
Current consumption 1		VDDH	I_{DDH}	All pins no load	–	–	5	mA
Current consumption 2		VDDL	I_{DDL}		–	–	30	mA
Input voltage	"H" level	(*1)	V_{IH}	V_{DDH} = 3.6V	2.0	–	–	V
	"L" level	(*1)	V_{IL}	V_{DDH} = 3.0V	–	–	0.8	V
Schmitt-trigger voltage	Positive	(*2)	V_{T+}		1.1	–	2.4	V
	Negative	(*2)	V_{T-}		0.6	–	1.8	V
Hysteresis voltage		(*2)	V_H		0.1	–	–	V
Output voltage	"H" level	(*3)	V_{OH}	I_{OH} = – 2mA (Type1) I_{OH} = – 6mA (Type2) I_{OH} = – 12mA (Type3)	V_{DDH} – 0.4	–	–	V
	"L" level	(*3)	V_{OL}	I_{OL} = 2mA (Type1) I_{OL} = 6mA (Type2) I_{OL} = 12mA (Type3)	–	–	0.4	V
Input leakage current		(*1, 2)	I_{LI}		– 5	–	5	µA
Pull-down resistor		(*4)	R_{PD}	$V_I = V_{DDH}$	60	120	288	kΩ
Pull-up resistor		(*5)	R_{PU}	$V_I = V_{SS}$	60	120	288	kΩ

Pin summary

(*1)	Input pins and bidirectional (input/output) pins in input mode
(*2)	Inputs with Schmitt characteristic and bidirectional (input/output) pins in input mode
(*3)	Output pins and bidirectional (input/output) pins in output mode Type 3: MCKOUT Type 2: DSBCK, PBCK, PLRCK Type 1: Outputs excluding those above
(*4)	Inputs with pull-down resistor
(*5)	Inputs with pull-up resistor

AC Electrical Characteristics

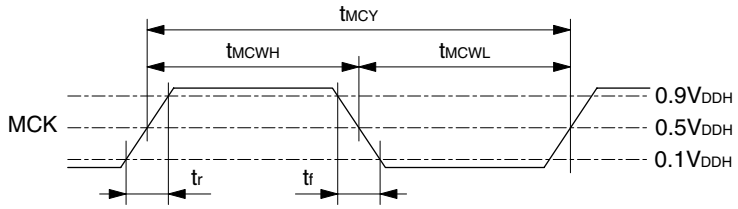
V_{DDH} = 3.0 to 3.6V, V_{DDL} = 2.3 to 2.7V, V_{SS} = 0V, T_{OPR} = – 40 to 85°C, fs = 44.1kHz unless otherwise noted. When DSBCK and PLRCK clocks are supplied by external clock input, their frequencies are related to the MCK input frequency by the following frequency divider ratios.

(DSBCK) cycle = 8 × MCK cycle (64fs)
(PLRCK) cycle [4fs mode] = 128 × MCK cycle (4fs)
(PLRCK) cycle [2fs mode] = 256 × MCK cycle (2fs)
(PLRCK) cycle [fs mode] = 512 × MCK cycle (fs)

System clock

■ MCK pin

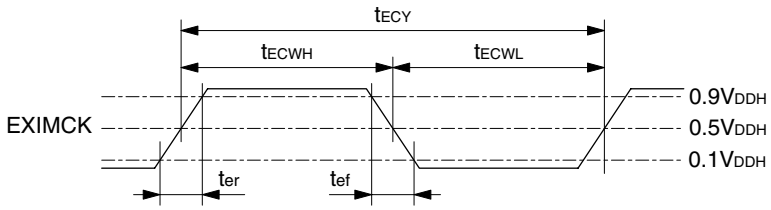
Parameter	Symbol	Rating			Unit
		min	typ	max	
"H"-level pulsewidth	t_{MCWH}	13	–	–	ns
"L"-level pulsewidth	t_{MCWL}	13	–	–	ns
Pulse cycle	t_{MCY}	40	44.29 (1/512fs)	–	ns
Rise/fall time	t_r , t_f	–	–	10	ns



External system clock

■ EXIMCK pin

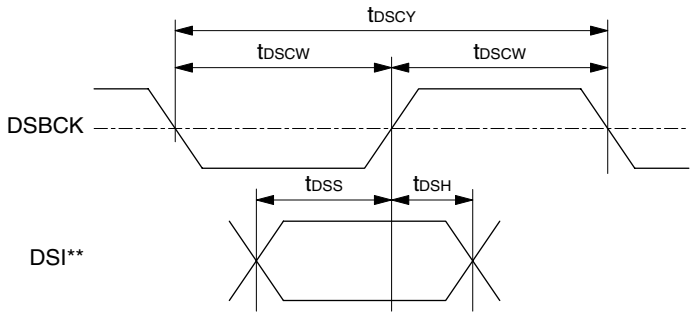
Parameter	Symbol	Rating			Unit
		min	typ	max	
"H"-level pulsewidth	t_{ECWH}	13	–	–	ns
"L"-level pulsewidth	t_{ECWL}	13	–	–	ns
Pulse cycle	t_{ECY}	40	–	–	ns
Rise/fall time	t_{er} , t_{ef}	–	–	10	ns



DSD input

- DSBCK pin
- DSIFL, DSIFR, DSISL, DSISR, DSICT, DSISW pins

Parameter	Symbol	Rating			Unit
		min	typ	max	
DSD clock pulsewidth	t_{DSCW}	150	177.16	–	ns
DSD clock pulse cycle	t_{DSCY}	300	354.31 (1/64fs)	–	ns
DSD data setup time	t_{DSS}	50	–	–	ns
DSD data hold time	t_{DSH}	50	–	–	ns



DSI**: DSIFL, DSIFR, DSISL, DSISR, DSICT, DSISW pins

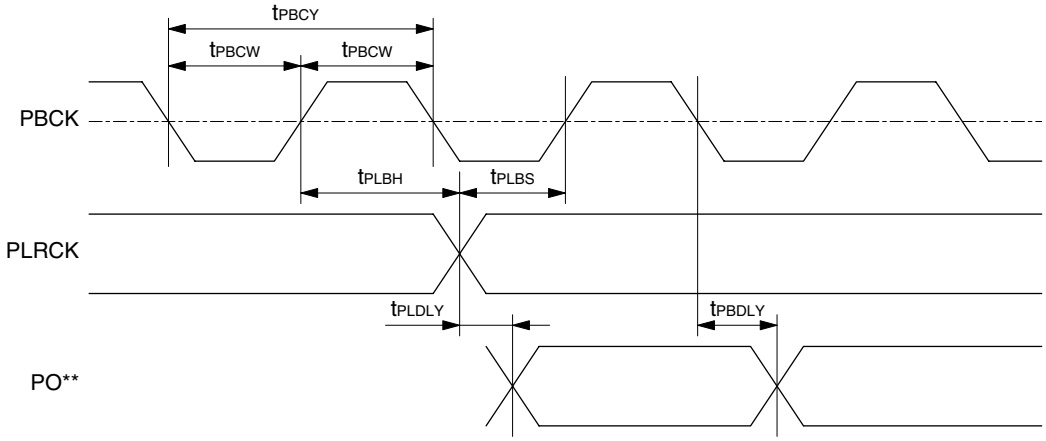
Note. DSD clock pulsewidth and DSD clock pulse cycle when DSBCK is in input mode.

Note. The data, with DSBCK timing above, enters the internal circuits on the falling edge of the MCK clock. Consequently, if the timing changes, the circuit must be resynchronized using INIT or SYNC.

PCM output

■ PLRCK, PBCK, POFLR, POSLR, POCSW pins

Parameter		Symbol	Rating			Unit
			min	typ	max	
BCK clock pulsewidth	4fs	t_{PBCW}	40	44.29	–	ns
	2fs		40	88.58	–	ns
	fs		40	177.15	–	ns
BCK clock pulse cycle	4fs	t_{PBCY}	80	88.58 (1/256fs)	–	ns
	2fs		80	177.15 (1/128fs)	–	ns
	fs		80	354.31 (1/64fs)	–	ns
Word CK setup time		t_{PLBS}	30	–	–	ns
Word CK hold time		t_{PLBH}	10	–	–	ns
Bit CK data delay time		t_{PBDLY}	0	–	15	ns
Word CK data delay time		t_{PLDLY}	0	–	15	ns



PO**: POFLR, POSLR, POCSW pins

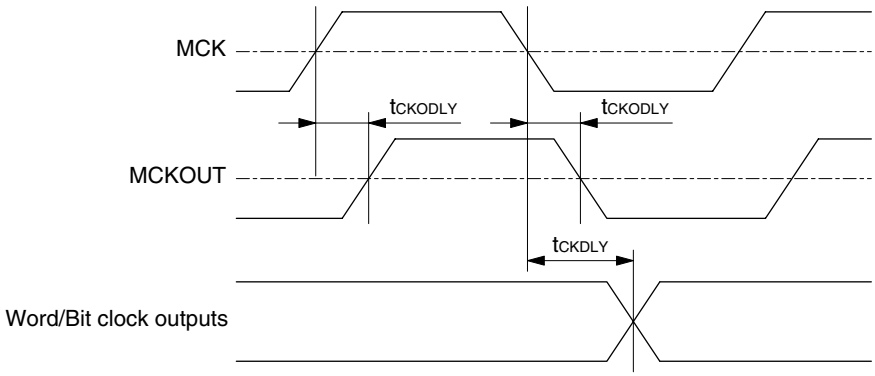
Note. The PCM output relationship applies when the external inputs (EXI**) are not in through mode.

Note. fs/2fs/4fs bit clock and word clock relationship applies when PBCK and PLRCK are in input mode.

Clock outputs

■ MCKOUT, DSBCK, PLRCK, PBCK pins

Parameter	Symbol	Rating			Unit
		min	typ	max	
MCKOUT output delay time	t_{CKODLY}	0	–	10	ns
Word/bit clock output delay time	t_{CKDLY}	0	–	10	ns



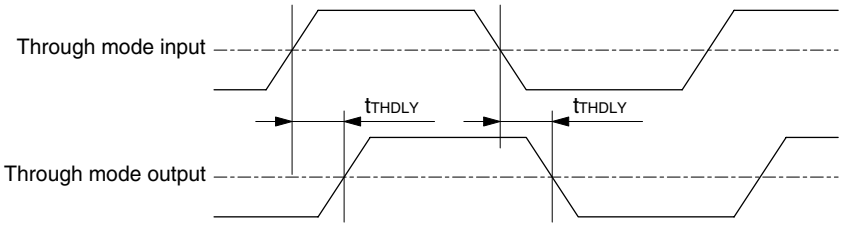
Note. Applies when MCK clock is output on MCKOUT in through mode.

Note. Applies when each word/bit clock on DSBCK, PBCK, PLRCK is in output mode.

Through-mode output

■ MCKOUT, PBCK, PLRCK, POFLR, POSLR, POCSW pins

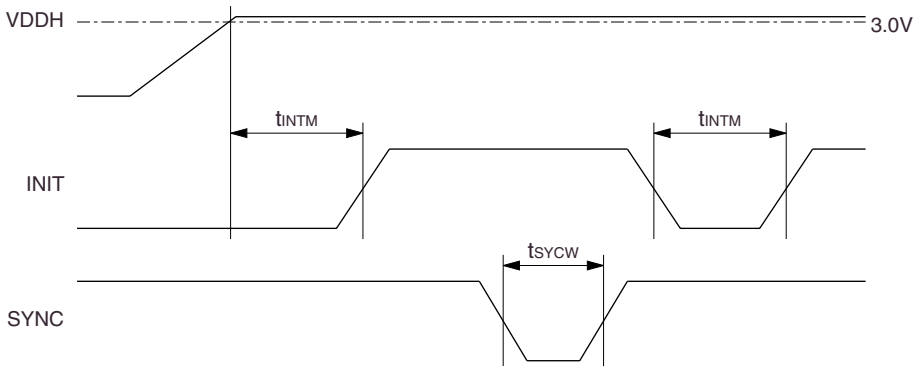
Through inputs	Through outputs	Condition	t_{THDLY} MAX	Unit
EXIMCK	MCKOUT	PCM outputs with external inputs selected	10	ns
EXIBCK	PBCK		10	ns
EXIWCK	PLRCK		10	ns
EXIFLR	POFLR		15	ns
EXISLR	POSLR		15	ns
EXICSW	POCSW		15	ns



Initialization and resynchronization

■ INIT, SYNC pins

Parameter	Symbol	Rating			Unit
		min	typ	max	
Initialization time	t_{INTM}	$6 \times t_{MCY}$	–	–	ns
Resynchronization pulsewidth	t_{SYCW}	$6 \times t_{MCY}$	–	–	ns

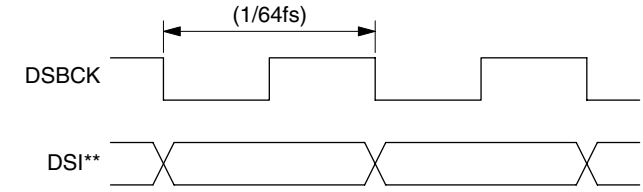


FUNCTIONAL DESCRIPTION

Data Input/Output Formats

DSD input format

DSD input data is read in on the rising edge of the DSBCK bit clock.

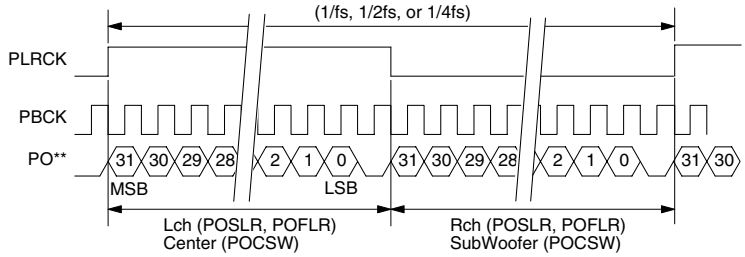


DSI**: DSIFL, DSIFR, DSISL, DSISR, DSICT, DSISW pins

PCM output format

The PCM output format can be assigned to either of two types below using FMTPCM. The output data is in 32-bit 2s complement form. The PLRCK and PBCK frequencies are set in response to the fs/2fs/4fs switch mode. However, when external inputs are selected, the inputs are passed to the output in through mode, regardless of the assigned format.

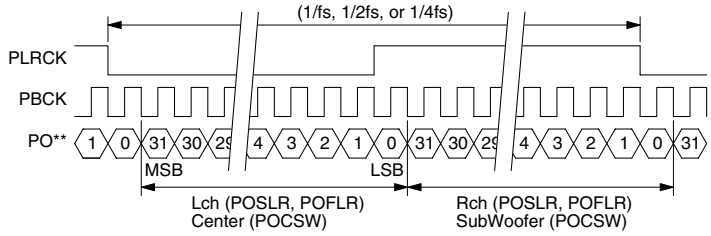
(1) MSB-first left-justified 32-bit (FMTPCM = "L")



PO**: POFLR, POSLR, POCSW pins

- If more than 32 bit clock cycles are input during a word clock cycle HIGH-level or LOW-level pulse, all bits after the 32nd bit are output as "0".
- When PLRCK and PBCK are set to output mode, the number of bit clock cycles during a word clock HIGH-level or LOW-level pulse is fixed at 32.

(2) IIS 32-bit (FMTPCM = "H")



PO**: POFLR, POSLR, POCSW pins

- In this format, there are 32 bit clock cycles per word clock cycle regardless of the input/output settings.

Data Output Selection

PCM output selection

The PCM output and decimation filter processing is set by SEL4FS, SEL1FS and SELEXT, as shown in the following table.

Setting			PCM output system				Clock output	Filter processing
SEL1FS	SEL4FS	SELEXT	POFLR	POSLR	POCSW	PLRCK PBCK	MCKOUT	
L	H	L	DSIFL DSIFR	DSISL DSISR	DSICT DSISW	4fs	MCK	4fs 480th-order
L	L	L	DSIFL DSIFR	DSISL DSISR	DSICT DSISW	2fs	MCK	2fs 480th-order
H	L or H	L	DSIFL DSIFR	DSISL DSISR	DSICT DSISW	fs	MCK	fs 480th-order
L or H	L or H	H	EXIFLR	EXISLR	EXICSW	EXILRCK EXIBCK	EXIMCK	Invalid

- The external data setting (SELEXT) has priority over the 4fs/2fs/fs selection setting (SEL1FS, SEL4FS).
- Also, the fs setting (SEL1FS) has priority over the 4fs/2fs setting (SEL4FS).

Clock Input/Output Selection and Resynchronization Operation

DSD clock input/output switching

The DSD input bit clock (DSBCK) can be switched between input and output by DIRDSCK.

Setting	I/O state
DIRDSCK	DSBCK
L	Input (Slave)
H	Output (Master)

PCM clock input/output switching

The PCM output word clock (PLRCK) and bit clock (PBCK) can be switched between input and output by DIRPCK.

Setting	I/O state
DIRPCK	PLRCK PBCK
L	Output (Master)
H	Input (Slave)

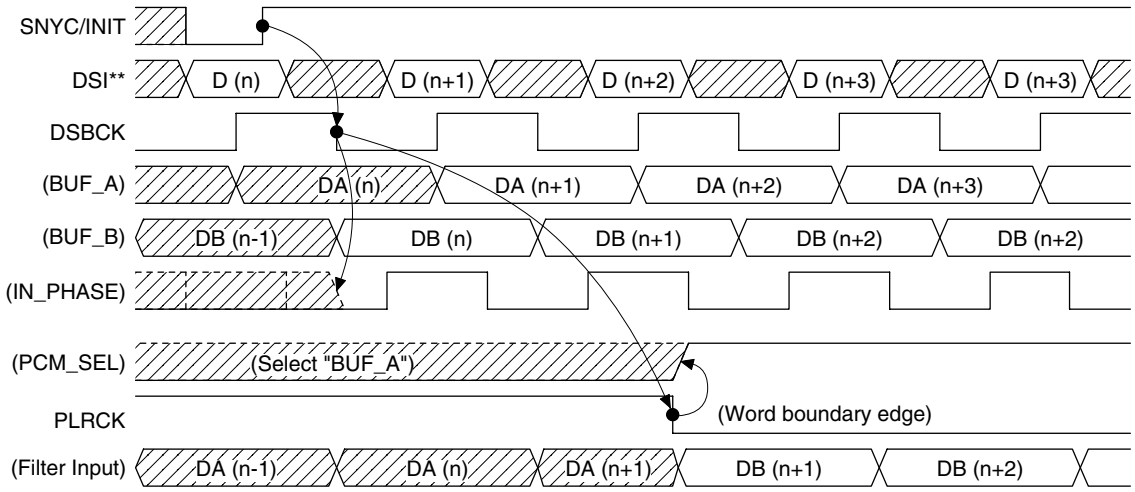
However, when external data is selected using SELEXT, the clocks PLRCK and PBCK are switched to outputs, regardless of the DIRPCK setting, thus care must be exercised with external connections.

Input clock sync operation and resynchronization

The internal computation and interface processing for data output is event driven, with the word boundary edge of the word clock as the trigger. This ensures the output signals are synchronized, regardless of the word clock and bit clock input/output settings.

The DSD input comprises data read into a buffer on the rising edge of the DSBCK bit clock (BUF_A) and data in another buffer internally delayed by half a bit clock cycle (BUF_B), and then a buffer is selected when the PCM output event occurs in order to avoid DSD input signal transitions.

Synchronization of whichever data buffer is selected occurs when the word boundary edge of the word clock is detected after the first DSBCK falling edge following a rising edge on INIT or SYNC.



DSI**: DSIFL, DSIFR, DSISL, DSISR, DSICT, DSISW pins

Figure 1. Input timing synchronization operation using INIT and SYNC

1) On the first DSBCK falling edge after a rising edge of SYNC or INIT, (IN_PHASE) is a phase reference signal for input data buffer selection.

2) Then, the input data buffer selected is determined by the logic level of IN_PHASE when the first PLRCK word boundary edge is detected.

When synchronization is adjusted using INIT or SYNC (resynchronization), 1 DSD data unit may be lost or repeated depending on the phase difference between input/output clocks.
The individual outputs should be muted by a minimum interval, given below, to avoid these data glitches.

[4fs PCM output] 36 clock cycles in PLRCK (4fs) mode

[2fs PCM output] 18 clock cycles in PLRCK (2fs) mode

[fs PCM output] 10 clock cycles in PLRCK (fs) mode

External input data and external system clock output switching

(1) Switching to external input data

When SELEXT is switched LOW to HIGH, the PCM data output is immediately switched to external input data.
PLRCK and PBCK are similarly switched immediately to EXILRCK and EXIBCK in through mode, respectively, regardless of the DIRPCK setting.

(2) Switching to external system clock

The MCKOUT system clock output can be switched between MCK and EXIMCK using SELEXT, as given below.

SELEXT = “L”: MCK output

SELEXT = “H”: EXIMCK output

Note that neither MCK nor EXIMCK clock should be stopped during the switching interval to prevent a micro-pulse being generated when switching.
The switching interval lasts from when SELEXT changes state until both clocks have made 4 transitions. During this interval, the LOW-level clock pulsewidth of the first clock is extended until the rising edge of the second clock occurs.
When the switching interval ends, the unused clock may then be stopped.

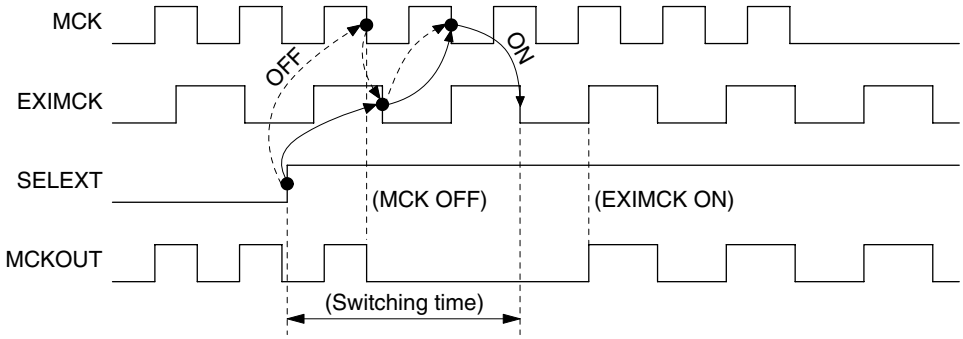


Figure 2. MCK → EXIMCK switching

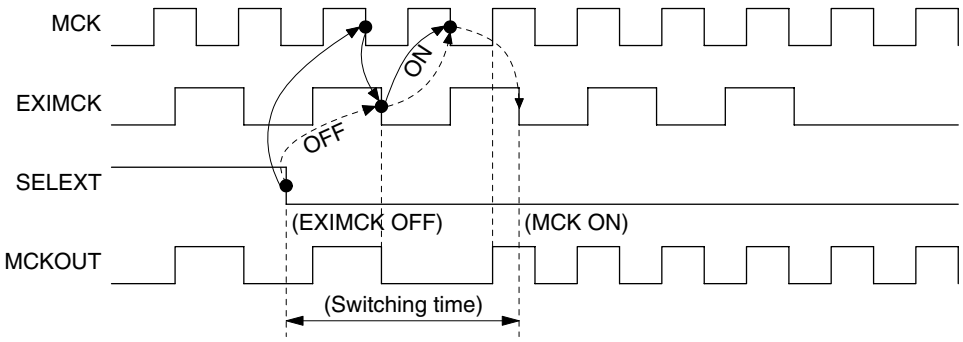


Figure 3. EXIMCK → MCK switching

DSD Gain Switching

The PCM output can be adjusted such that 0dB corresponds to 50% modulation level DSD input signal using DSGAIN, as given below.

DSGAIN = “L” : 100% modulation = 0dB (PCM)

DSGAIN = “H” : 50% modulation = 0dB (PCM) * with + 6dB internal amplification

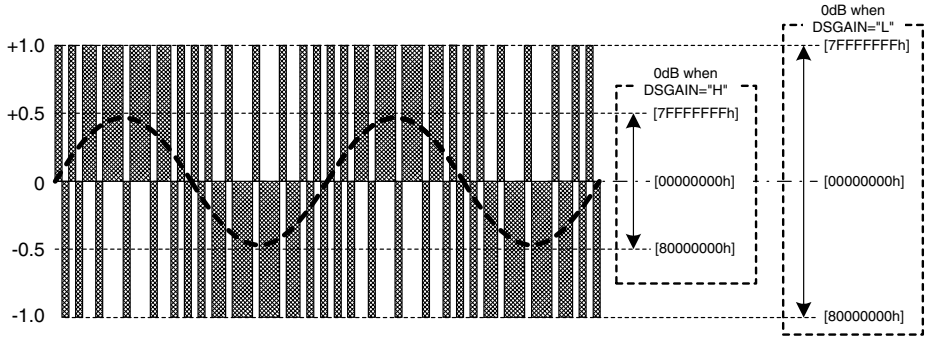


Figure 4. DSD modulation level

Note. When DSGAIN = “H”, note that any input DSD signal with modulation of 50% level or higher will be amplitude limited, resulting in output signal clipping.

Mute Function

The PCM outputs can be muted using XMTPCM, as given below. Muting is applied immediately before output.

When PCM muting is set ON, the PCM outputs are directly set to value “0”.

XMTPCM = “L” : all PCM outputs muting ON

XMTPCM = “H” : all PCM outputs muting OFF

The mute function is only active for internal computation of fs/2fs/4fs output. It is inactive for external input to output connection in through mode.

Initialization Operation

The power must be applied in order of VDDL and VDDH. Please avoid the continuous power supply injection of only VDDH. (less than 1 second)

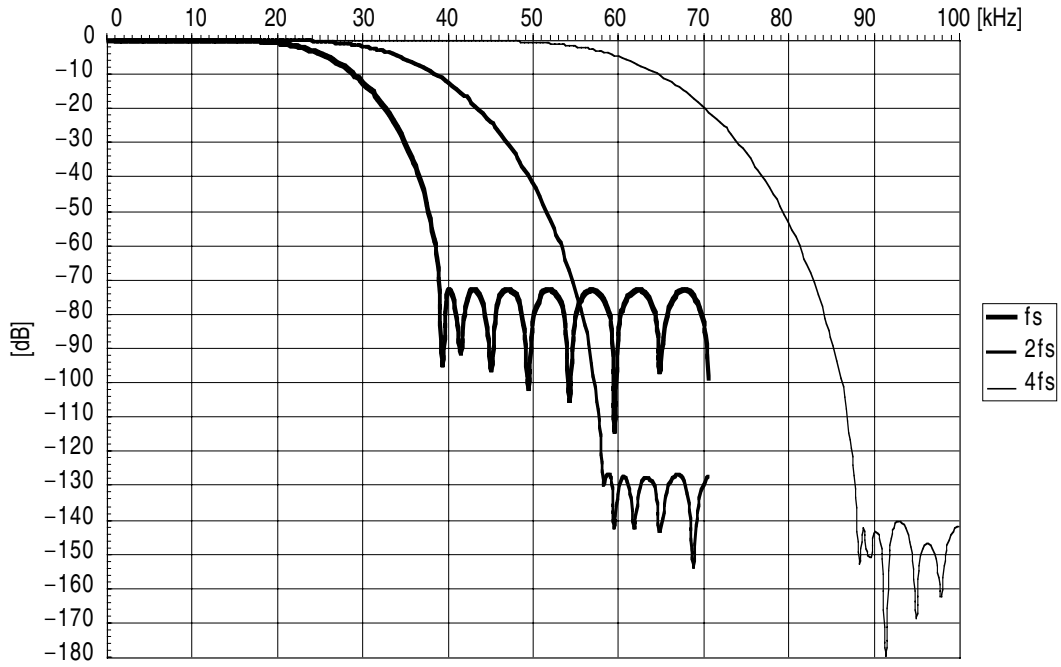
After power is applied, INIT must be held LOW for the rated interval to initialize the device. During initialization, the outputs have the following states.

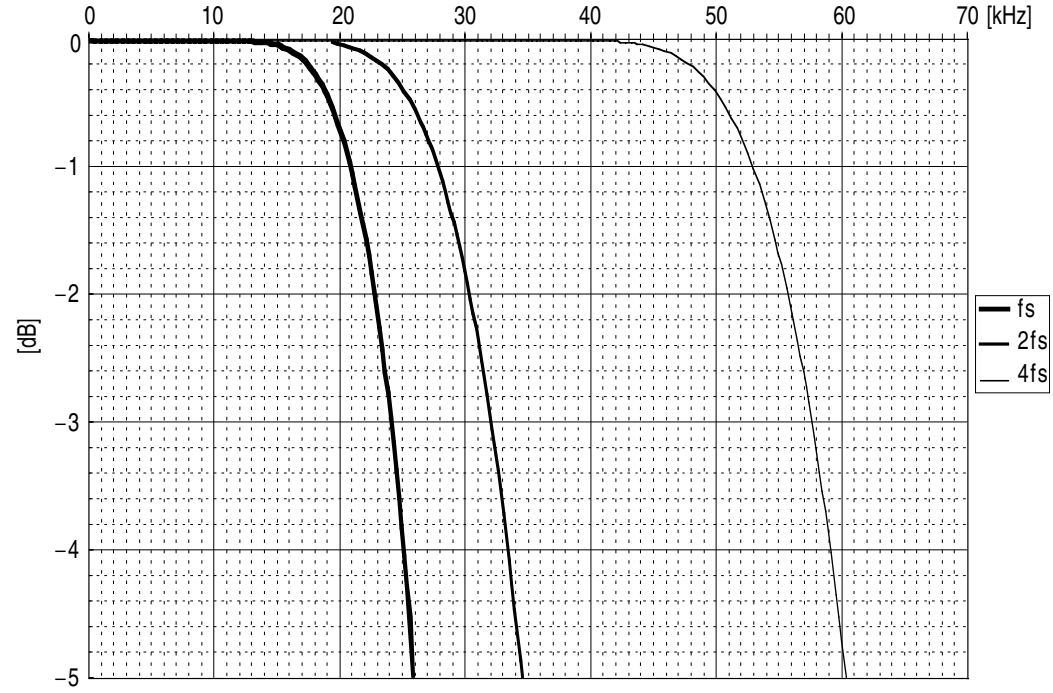
Pin	state
PCM data outputs	LOW in internal data output mode External input to output connection in through mode
DSBCK	HIGH in output (master) mode
PBCK	HIGH in internal data output mode External bit clock input to output connection in through mode
PLRCK	LOW in 32-bit left-justified output mode HIGH in IIS output mode External word clock input to output connection in through mode
MCKOUT	MCK or EXIMCK, whichever is currently selected.

When INIT goes HIGH, synchronization operation begins as described in the section “Input clock sync operation and resynchronization”.
Note that if the PCM signal muting is ON during initialization, muting operation continues until it is released.
The system clock input on MCK must be applied during initialization.

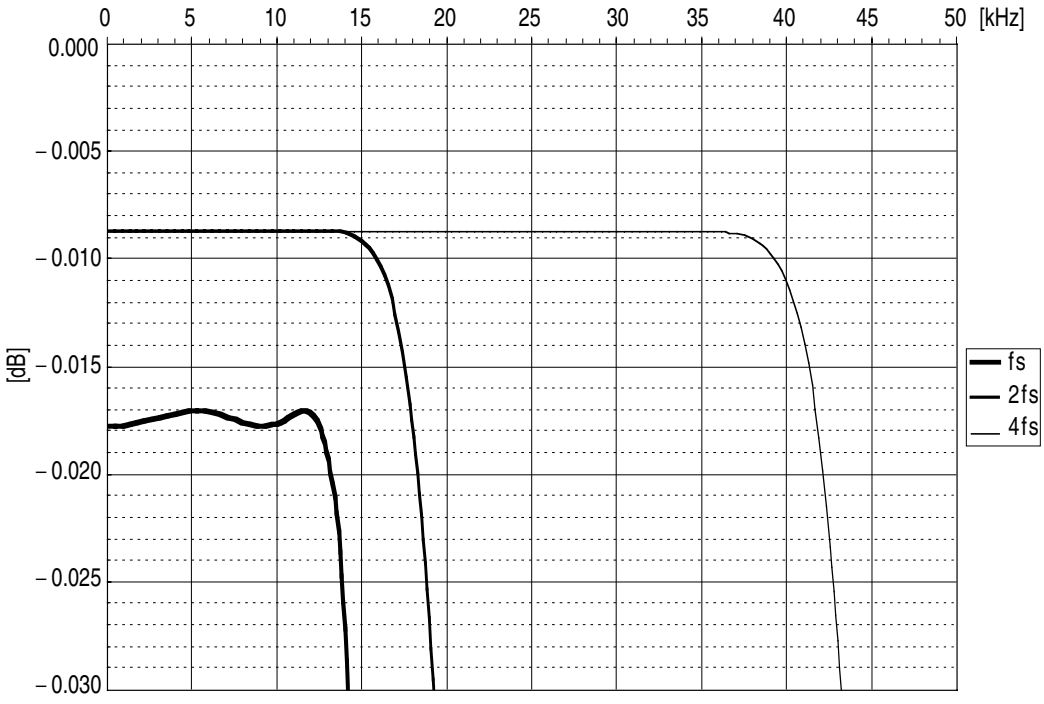
BUILT-IN FILTER CHARACTERISTICS

Filter Mode Cutoff Characteristics





Filter Mode Ripple Characteristics



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NPC
NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, Fukuzumi 2-chome, Koto-ku,
Tokyo 135-8430, Japan
Telephone: +81-3-3642-6661
Facsimile: +81-3-3642-6698
http://www.npc.co.jp/
Email: sales@npc.co.jp

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