2.5 VOLT HIGH-SPEED TeraSync™ FIFO 36-BIT CONFIGURATIONS 65,536 x 36, 131,072 x 36, 262,144 x 36

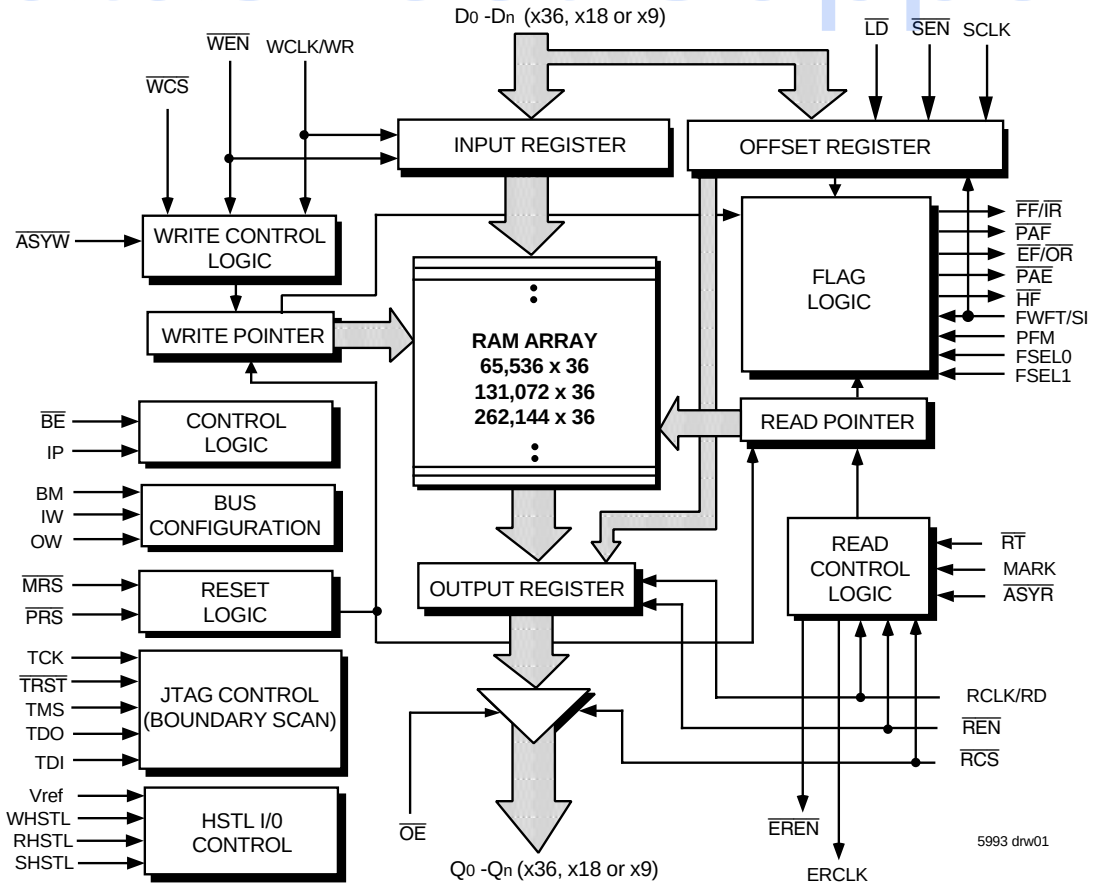
ADVANCE INFORMATION

IDT72T36105
IDT72T36115
IDT72T36125

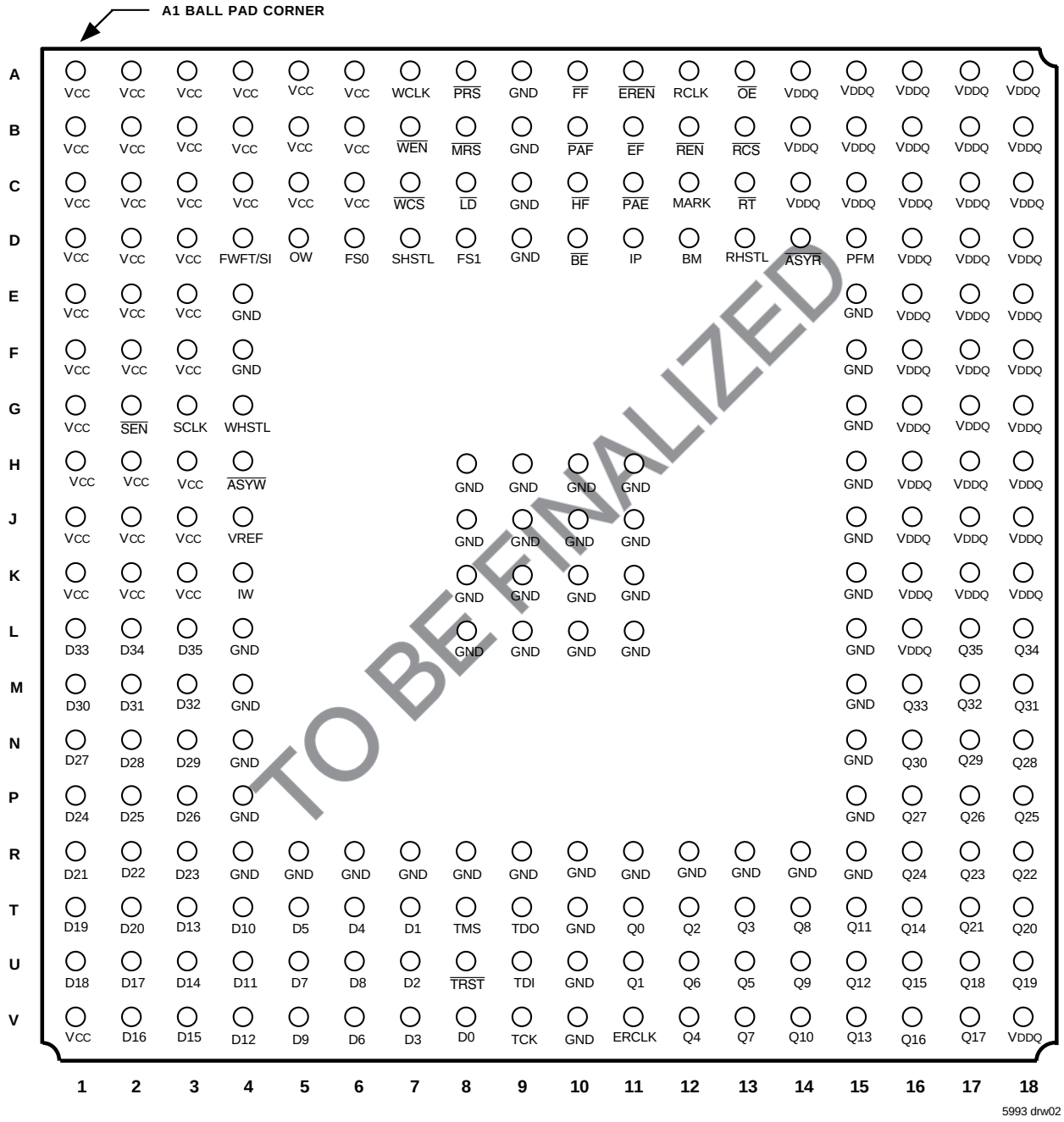
FEATURES:

- Choose among the following memory organizations:
  - IDT72T36105 — 65,536 x 36
  - IDT72T36115 — 131,072 x 36
  - IDT72T36125 — 262,144 x 36
- Up to 200 MHz Operation of Clocks
- Functionally compatible to the 32,768 x36 TeraSync devices
- User selectable HSTL/LVTTL Input and/or Output
- Read Enable & Read Clock Echo outputs aid high speed operation
- User selectable Asynchronous read and/or write port timing
- Mark & Retransmit, resets read pointer to user marked position
- Write Chip Select ($\overline{WCS}$) input disables Write Port HSTL inputs
- Read Chip Select ($\overline{RCS}$) synchronous to RCLK
- Programmable Almost-Empty and Almost-Full flags, each flag can default to one of eight preselected offsets
- Program programmable flags by either serial or parallel means
- Selectable synchronous/asynchronous timing modes for Almost-Empty and Almost-Full flags
- Separate SCLK input for Serial programming of flag offsets
- User selectable input and output port bus-sizing
  - *x36 in to x36 out*
  - *x36 in to x18 out*
  - *x36 in to x9 out*
  - *x18 in to x36 out*
  - *x9 in to x36 out*
- Big-Endian/Little-Endian user selectable byte representation
- Auto power down minimizes standby power consumption
- Master Reset clears entire FIFO
- Partial Reset clears data, but retains programmable settings
- Empty, Full and Half-Full flags signal FIFO status
- Select IDT Standard timing (using $\overline{EF}$ and $\overline{FF}$ flags) or First Word Fall Through timing (using $\overline{OR}$ and $\overline{IR}$ flags)
- Output enable puts data outputs into high impedance state
- JTAG port, provided for Boundary Scan function
- Available in 240-pin (19mm x 19mm)Plastic Ball Grid Array (PBGA)
- Easily expandable in depth and width
- Independent Read and Write Clocks (permit reading and writing simultaneously)
- High-performance submicron CMOS technology
- Industrial temperature range (–40°C to +85°C) is available

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PBGA: 1mm pitch, 19mm x 19mm (BB240-1, order code: BB)
TOP VIEW

DESCRIPTION:

The IDT72T36105/72T36115/72T36125 are exceptionally deep, extrememly high speed, CMOS First-In-First-Out (FIFO) memories with clocked read and write controls and a flexible Bus-Matching x36/x18/x9 data flow. These FIFOs offer several key user benefits:

- Flexible x36/x18/x9 Bus-Matching on both read and write ports
- A user selectable MARK location for retransmit
- User selectable I/O structure for HSTL or LVTTL
- Asynchronous/Synchronous translation on the read or write ports
- The first word data latency period, from the time the first word is written to an empty FIFO to the time it can be read, is fixed and short.
- High density offerings up to 9 Mbit

Bus-Matching TeraSync FIFOs are particularly appropriate for network, video, telecommunications, data communications and other applications that need to buffer large amounts of data and match busses of unequal sizes.

Each FIFO has a data input port (D_n) and a data output port (Q_n), both of which can assume either a 36-bit, 18-bit or a 9-bit width as determined by the state of external control pins Input Width (IW), Output Width (OW), and Bus-Matching (BM) pin during the Master Reset cycle.

The input port can be selected as either a Synchronous (clocked) interface, or Asynchronous interface. During Synchronous operation the input port is controlled by a Write Clock (WCLK) input and a Write Enable ($\overline{WEN}$) input. Data present on the Dn data inputs is written into the FIFO on every rising edge of WCLK when $\overline{WEN}$ is asserted. During Asynchronous operation only the WR input is used to write data into the FIFO. Data is written on a rising edge of WR, the $\overline{WEN}$ input should be tied to its active state, (LOW).

The input port can be selected for either 2.5V LVTTL or HSTL operation, this operation is selected by the state of the WHSTL input during a master reset. A Write Chip Select input ($\overline{WCS}$) is provided for use when the write port is in HSTL mode. During HSTL operation the $\overline{WCS}$ input can be used to disable write port inputs (data only).

The output port can be selected as either a Synchronous (clocked) interface, or Asynchronous interface. During Synchronous operation the output port is controlled by a Read Clock (RCLK) input and Read Enable ($\overline{REN}$) input. Data is read from the FIFO on every rising edge of RCLK when $\overline{REN}$ is asserted. During Asynchronous operation only the RD input is used to read data from the FIFO. Data is read on a rising edge of RD, the $\overline{REN}$ input should be tied to its active state, LOW. When Asynchronous operation is selected on the output port the FIFO must be configured for Standard IDT mode, also the $\overline{RCS}$ should be tied LOW and the $\overline{OE}$ input used to provide three-state control of the outputs, Qn.

The output port can be selected for either 2.5V LVTTL or HSTL operation, this operation is selected by the state of the RHSTL input during a master reset.

An Output Enable ($\overline{OE}$) input is provided for three-state control of the outputs. A Read Chip Select ($\overline{RCS}$) input is also provided, the $\overline{RCS}$ input is synchronized to the read clock, and also provides three-state control of the Qn data outputs. When $\overline{RCS}$ is disabled, the data outputs will be high impedance. During Asynchronous operation of the output port, $\overline{RCS}$ should be enabled, held LOW.

Echo Read Enable, $\overline{EREN}$ and Echo Read Clock, ERCLK outputs are provided. These are outputs from the read port of the FIFO that are required for high speed data communication, to provide tighter synchronization between the data being transmitted from the Qn outputs and the data being received by the input device. Data read from the read port is available on the output bus with respect to $\overline{EREN}$ and ERCLK, this is very useful when data is being read at high speed. The ERCLK and $\overline{EREN}$ outputs are non-functional when the Read port is setup for Asynchronous mode.

The frequencies of both the RCLK and the WCLK signals may vary from 0 to f_{MAX} with complete independence. There are no restrictions on the frequency of the one clock input with respect to the other.

There are two possible timing modes of operation with these devices: IDT Standard mode and First Word Fall Through (FWFT) mode.

In *IDT Standard mode,* the first word written to an empty FIFO will not appear on the data output lines unless a specific read operation is performed. A read operation, which consists of activating $\overline{REN}$ and enabling a rising RCLK edge, will shift the word from internal memory to the data output lines.

In *FWFT mode,* the first word written to an empty FIFO is clocked directly to the data output lines after three transitions of the RCLK signal. A $\overline{REN}$ does not have to be asserted for accessing the first word. However, subsequent words written to the FIFO do require a LOW on $\overline{REN}$ for access. The state of the FWFT/SI input during Master Reset determines the timing mode in use.

For applications requiring more data storage capacity than a single FIFO can provide, the FWFT timing mode permits depth expansion by chaining FIFOs in series (i.e. the data outputs of one FIFO are connected to the corresponding data inputs of the next). No external logic is required.

These FIFOs have five flag pins, $\overline{EF}/\overline{OR}$ (Empty Flag or Output Ready), $\overline{FF}/\overline{IR}$ (Full Flag or Input Ready), $\overline{HF}$ (Half-full Flag), $\overline{PAE}$ (Programmable Almost-Empty flag) and $\overline{PAF}$ (Programmable Almost-Full flag). The $\overline{EF}$ and $\overline{FF}$ functions are selected in IDT Standard mode. The $\overline{IR}$ and $\overline{OR}$ functions are selected in FWFT mode. $\overline{HF}$, $\overline{PAE}$ and $\overline{PAF}$ are always available for use, irrespective of timing mode.

$\overline{PAE}$ and $\overline{PAF}$ can be programmed independently to switch at any point in memory. Programmable offsets determine the flag switching threshold and can be loaded by two methods: parallel or serial. Eight default offset settings are also provided, so that $\overline{PAE}$ can be set to switch at a predefined number of locations from the empty boundary and the $\overline{PAF}$ threshold can also be set at similar predefined values from the full boundary. The default offset values are set during Master Reset by the state of the FSEL0, FSEL1, and $\overline{LD}$ pins.

For serial programming, $\overline{SEN}$ together with $\overline{LD}$ on each rising edge of SCLK, are used to load the offset registers via the Serial Input (SI). For parallel programming, $\overline{WEN}$ together with $\overline{LD}$ on each rising edge of WCLK, are used to load the offset registers via D_n. $\overline{REN}$ together with $\overline{LD}$ on each rising edge of RCLK can be used to read the offsets in parallel from Q_n regardless of whether serial or parallel offset loading has been selected.

During Master Reset ($\overline{MRS}$) the following events occur: the read and write pointers are set to the first location of the FIFO. The FWFT pin selects IDT Standard mode or FWFT mode.

The Partial Reset ($\overline{PRS}$) also sets the read and write pointers to the first location of the memory. However, the timing mode, programmable flag programming method, and default or programmed offset settings existing before Partial Reset remain unchanged. The flags are updated according to the timing mode and offsets in effect. $\overline{PRS}$ is useful for resetting a device in mid-operation, when reprogramming programmable flags would be undesirable.

It is also possible to select the timing mode of the $\overline{PAE}$ (Programmable Almost-Empty flag) and $\overline{PAF}$ (Programmable Almost-Full flag) outputs. The timing modes can be set to be either asynchronous or synchronous for the $\overline{PAE}$ and $\overline{PAF}$ flags.

If asynchronous $\overline{PAE}/\overline{PAF}$ configuration is selected, the $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of RCLK.

DESCRIPTION (CONTINUED)

If synchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected , the $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during MasterReset by the state of the Programmable Flag Mode (PFM) pin.

This device includes a Retransmit from Mark feature that utilizes two control inputs, MARK and , $\overline{RT}$ (Retransmit). If the MARK input is enabled with respect to the RCLK, the memory location being read at that point will be marked. Any subsequent retransmit operation, $\overline{RT}$ goes LOW, will reset the read pointer to this 'marked' location.

The device can be configured with different input and output bus widths as shown in Table 1.

A Big-Endian/Little-Endian data word format is provided. This function is useful when data is written into the FIFO in long word format (x36/x18) and read out of the FIFO in small word (x18/x9) format. If Big-Endian mode is selected, then the most significant byte (word) of the long word written into the FIFO will be read out of the FIFO first, followed by the least significant byte. If Little-Endian format is selected, then the least significant byte of the long word written into the FIFO will be read out first, followed by the most significant byte. The mode desired is configured during master reset by the state of the Big-Endian ($\overline{BE}$) pin. See Figure 5 for *Bus-Matching Byte Arrangement*.

The Interspersed/Non-Interspersed Parity (IP) bit function allows the user to select the parity bit in the word loaded into the parallel port (D_0-Dn) when programming the flag offsets. If Interspersed Parity mode is selected, then the FIFO will assume that the parity bit is located in bit positions D8, D17, D26 and D35 during the parallel programming of the flag offsets. If Non-Interspersed Parity mode is selected, then D8, D17 and D26 are assumed to be valid bits and D32, D33, D34 and D35 are ignored. IP mode is selected during Master Reset by the state of the IP input pin.

If, at any time, the FIFO is not actively performing an operation, the chip will automatically power down. Once in the power down state, the standby supply current consumption is minimized. Initiating any operation (by activating control inputs) will immediately take the device out of the power down state.

Both an Asynchronous Output Enable pin ($\overline{OE}$) and Synchronous Read Chip Select pin ($\overline{RCS}$) are provided on the FIFO. The Synchronous Read Chip Select is synchronized to the RCLK. Both the output enable and read chip select control the output buffer of the FIFO, causing the buffer to be either HIGH impedance or LOW impedance.

A JTAG test port is provided, here the FIFO has fully functional Boundary Scan feature, compliant with IEEE 1449.1 Standard Test Access Port and Boundary Scan Architecture.

The TeraSync FIFO has the capability of operating its ports (write and/or read) in either LVTTL or HSTL mode, each ports selection independent of the other. The write port selection is made via WHSTL and the read port selection via RHSTL. An additional input SHSTL is also provided, this allows the user to select HSTL operation for other pins on the device (not associated with the write or read ports).

The IDT72T36105/72T36115/72T36125 are fabricated using IDT's high speed submicron CMOS technology.

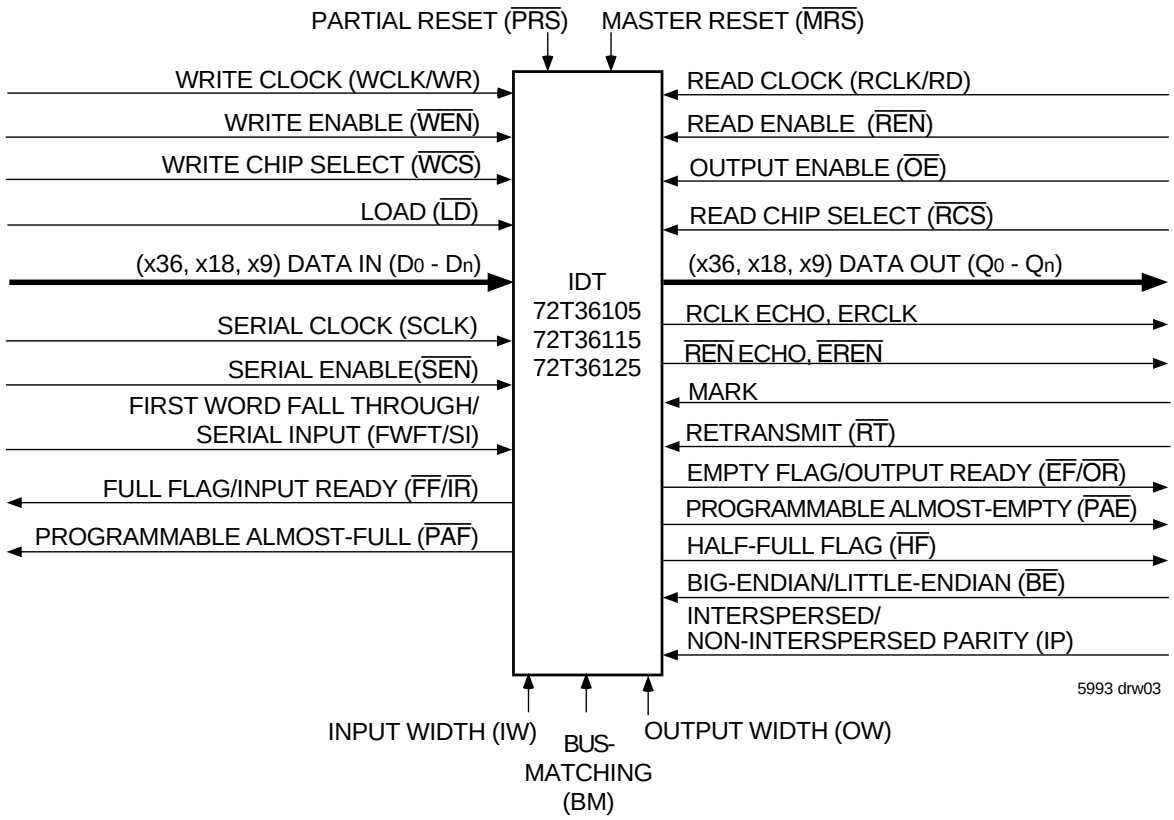


Figure 1. Single Device Configuration Signal Flow Diagram

TABLE 1 — BUS-MATCHING CONFIGURATION MODES

BM	IW	OW	Write Port Width	Read Port Width
L	L	L	x36	x36
H	L	L	x36	x18
H	L	H	x36	x9
H	H	L	x18	x36
H	H	H	x9	x36

NOTE:
1. Pin status during Master Reset.

PIN DESCRIPTION

Symbol	Name	I/O TYPE	Description
ASYR(1)	Asynchronous Read Port	LVTTL INPUT	A HIGH on this input during Master Reset will select Synchronous read operation for the output port. A LOW will select Asynchronous operation. If Asynchronous is selected the FIFO must operate in IDT Standard mode.
ASYW(1)	Asynchronous Write Port	LVTTL INPUT	A HIGH on this input during Master Reset will select Synchronous write operation for the input port. A LOW will select Asynchronous operation.
$\overline{BE}$(1)	Big-Endian/ Little-Endian	LVTTL INPUT	During Master Reset, a LOW on $\overline{BE}$ will select Big-Endian operation. A HIGH on $\overline{BE}$ during Master Reset will select Little-Endian format.
BM(1)	Bus-Matching	LVTTL INPUT	BM works with IW and OW to select the bus sizes for both write and read ports. See Table 1 for bus size configuration.
D_0–D_{35}	Data Inputs	HSTL-LVTTL INPUT	Data inputs for a 36-, 18- or 9-bit bus. When in 18- or 9-bit mode, the unused input pins are in a don't care state.
$\overline{EF}$/$\overline{OR}$	Empty Flag/ Output Ready	HSTL-LVTTL OUTPUT	In the IDT Standard mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether or not the FIFO memory is empty. In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ indicates whether or not there is valid data available at the outputs.
ERCLK	RCLK Echo	HSTL-LVTTL OUTPUT	Read clock Echo output, only available when the Read is setup for Synchronous mode.
$\overline{EREN}$	Read Enable Echo	HSTL-LVTTL OUTPUT	Read Enable Echo output, only available when the Read is setup for Synchronous mode.
$\overline{FF}$/$\overline{IR}$	Full Flag/ Input Ready	HSTL-LVTTL OUTPUT	In the IDT Standard mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether or not the FIFO memory is full. In the FWFT mode, the $\overline{IR}$ function is selected. $\overline{IR}$ indicates whether or not there is space available for writing to the FIFO memory.
FSEL0(1)	Flag Select Bit 0	LVTTL INPUT	During Master Reset, this input along with FSEL1 and the $\overline{LD}$ pin, will select the default offset values for the programmable flags $\overline{PAE}$ and $\overline{PAF}$. There are up to eight possible settings available.
FSEL1(1)	Flag Select Bit 1	LVTTL INPUT	During Master Reset, this input along with FSEL0 and the $\overline{LD}$ pin will select the default offset values for the programmable flags $\overline{PAE}$ and $\overline{PAF}$. There are up to eight possible settings available.
FWFT/ SI	First Word Fall Through/Serial In	HSTL-LVTTL INPUT	During Master Reset, selects First Word Fall Through or IDT Standard mode. After Master Reset, this pin functions as a serial input for loading offset registers. If Asynchronous operation of the read port has been selected then the FIFO must be set-up in IDT Standard mode.
$\overline{HF}$	Half-Full Flag	HSTL-LVTTL OUTPUT	$\overline{HF}$ indicates whether the FIFO memory is more or less than half-full.
IP(1)	Interspersed Parity	LVTTL INPUT	During Master Reset, a LOW on IP will select Non-Interspersed Parity mode. A HIGH will select Interspersed Parity mode.
IW(1)	Input Width	LVTTL INPUT	This pin, along with OW and BM, selects the bus width of the write port. See Table 1 for bus size configuration.
$\overline{LD}$	Load	HSTL-LVTTL INPUT	This is a dual purpose pin. During Master Reset, the state of the $\overline{LD}$ input along with FSEL0 and FSEL1, determines one of eight default offset values for the $\overline{PAE}$ and $\overline{PAF}$ flags, along with the method by which these offset registers can be programmed, parallel or serial (see Table 2). After Master Reset, this pin enables writing to and reading from the offset registers.
MARK	Mark for Retransmit	HSTL-LVTTL INPUT	When this pin is asserted the current location of the read pointer will be marked. Any subsequent Retransmit operation will reset the read pointer to this position.
$\overline{MRS}$	Master Reset	HSTL-LVTTL INPUT	$\overline{MRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Master Reset, the FIFO is configured for either FWFT or IDT Standard mode, Bus-Matching configurations, Synchronous/Asynchronous operation of the read or write port, one of eight programmable flag default settings, serial or parallel programming of the offset settings, Big-Endian/Little-Endian format, zero latency timing mode, interspersed parity, and synchronous versus asynchronous programmable flag timing modes.
$\overline{OE}$	Output Enable	HSTL-LVTTL INPUT	$\overline{OE}$ provides Asynchronous three-state control of the data outputs, Q_n. During a Master or Partial Reset the $\overline{OE}$ input is the only input that provide High-Impedance control of the data outputs.
OW(1)	Output Width	LVTTL INPUT	This pin, along with IW and BM, selects the bus width of the read port. See Table 1 for bus size configuration.
$\overline{PAE}$	Programmable Almost-Empty Flag	HSTL-LVTTL OUTPUT	$\overline{PAE}$ goes LOW if the number of words in the FIFO memory is less than offset n, which is stored in the Empty Offset register. $\overline{PAE}$ goes HIGH if the number of words in the FIFO memory is greater than or equal to offset n.
$\overline{PAF}$	Programmable Almost-Full Flag	HSTL-LVTTL OUTPUT	$\overline{PAF}$ goes HIGH if the number of free locations in the FIFO memory is more than offset m, which is stored in the Full Offset register. $\overline{PAF}$ goes LOW if the number of free locations in the FIFO memory is less than or equal to m.

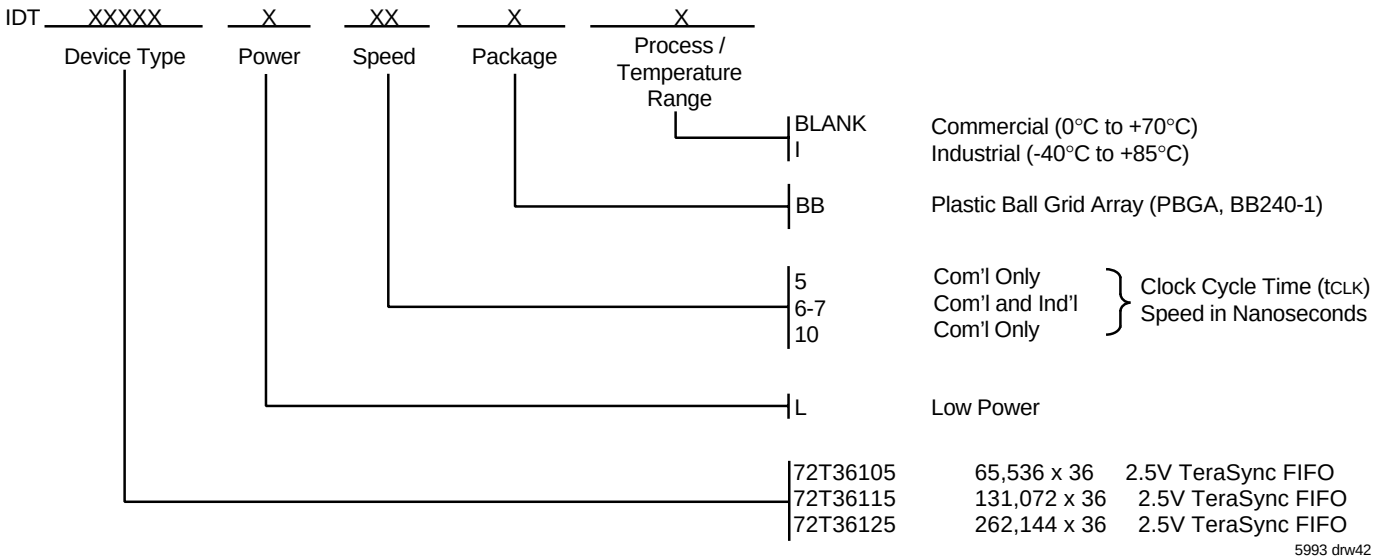
NOTE:
1. Inputs should not change state after Master Reset.

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O TYPE	Description
PFM[1]	Programmable Flag Mode	LVTTL INPUT	During Master Reset, a LOW on PFM will select Asynchronous Programmable flag timing mode. A HIGH on PFM will select Synchronous Programmable flag timing mode.
$\overline{PRS}$	Partial Reset	HSTL-LVTTL INPUT	$\overline{PRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Partial Reset, the existing mode (IDT or FWFT), programming method (serial or parallel), and programmable flag settings are all retained.
Q_0–Q_{35}	Data Outputs	HSTL-LVTTL OUTPUT	Data outputs for an 36-, 18- or 9-bit bus. When in 18- or 9-bit mode, any unused output pins should not be connected. Outputs are not 5V tolerant regardless of the state of $\overline{OE}$ and $\overline{RCS}$.
RCLK/ RD	Read Clock/ Read Stobe	HSTL-LVTTL INPUT	If Synchronous operation of the read port has been selected, when enabled by $\overline{REN}$, the rising edge of RCLK reads data from the FIFO memory and offsets from the programmable registers. If $\overline{LD}$ is LOW, the values loaded into the offset registers is output on a rising edge of RCLK. If Asynchronous operation of the read port has been selected, a rising edge on RD reads data from the FIFO in an Asynchronous manner. $\overline{REN}$ should be tied LOW.
$\overline{RCS}$	Read Chip Select	HSTL-LVTTL INPUT	$\overline{RCS}$ provides synchronous control of the read port and output impedance of Qn, synchronous to RCLK. During a Master Reset or Partial Reset the $\overline{RCS}$ input is don't care, if $\overline{OE}$ is LOW the data outputs will be Low-Impedance regardless of $\overline{RCS}$.
$\overline{REN}$	Read Enable	HSTL-LVTTL INPUT	If Synchronous operation of the read port has been selected, $\overline{REN}$ enables RCLK for reading data from the FIFO memory and offset registers. If Asynchronous operation of the read port has been selected, the $\overline{REN}$ input should be tied LOW.
RHSTL[1]	Read Port HSTL Select	LVTTL INPUT	This pin is used to select HSTL or 2.5v LVTTL outputs for the FIFO. If HSTL inputs are required, this input must be tied HIGH. Otherwise it should be tied LOW.
$\overline{RT}$	Retransmit	HSTL-LVTTL INPUT	$\overline{RT}$ asserted on the rising edge of RCLK initializes the READ pointer to zero, sets the $\overline{EF}$ flag to LOW ($\overline{OR}$ to HIGH in FWFT mode) and doesn't disturb the write pointer, programming method, existing timing mode or programmable flag settings. If a mark has been set via the MARK input pin, then the read pointer will jump to the 'mark' location.
SCLK	Serial Clock	HSTL-LVTTL INPUT	A rising edge on SCLK will clock the serial data present on the SI input into the offset registers providing that $\overline{SEN}$ is enabled.
$\overline{SEN}$	Serial Enable	HSTL-LVTTL INPUT	$\overline{SEN}$ enables serial loading of programmable flag offsets.
SHSTL	System HSTL Select	LVTTL INPUT	All inputs not associated with the write or read port can be selected for HSTL operation via the SHSTL input.
TCK[2]	JTAG Clock	HSTL-LVTTL INPUT	Clock input for JTAG function. TMS and TDI are sampled on the rising edge of TCK. Data is output on TDO on the falling edge.
$\overline{TRST}$[2]	JTAG Reset	HSTL-LVTTL INPUT	$\overline{TRST}$ is an asynchronous reset pin for the JTAG controller.
TMS	JTAG Mode Select	HSTL-LVTTL INPUT	TMS is a serial input pin. Bits are serially loaded on the rising edge of TCK, which selects 1 of 5 modes of operation for the JTAG boundary scan.
TDI	Test Data Input	HSTL-LVTTL INPUT	During JTAG boundary scan operation test data is serially loaded via TDI on the rising edge of TCK. This is also the data for the Instruction Register, ID Register and Bypass Register.
TDO	Test Data Output	HSTL-LVTTL OUTPUT	During JTAG boundary scan operation test data is serially output via TDO on the falling edge of TCK. This output is in High-Z except when shifting, while in SHIFT-DR and SHIFT-IR controller states.
$\overline{WEN}$	Write Enable	HSTL-LVTTL INPUT	When Synchronous operation of the write port has been selected, $\overline{WEN}$ enables WCLK for writing data into the FIFO memory and offset registers. If Asynchronous operation of the write port has been selected, the $\overline{WEN}$ input should be tied LOW.
$\overline{WCS}$	Write Chip Select	HSTL-LVTTL INPUT	This pin disables the write port data inputs when the device write port is configured for HSTL mode. This provides added power savings.
WCLK/ WR	Write Clock/ Write Strobe	HSTL-LVTTL INPUT	If Synchronous operation of the write port has been selected, when enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the FIFO. If Asynchronous operation of the write port has been selected, WR writes data into the FIFO on a rising edge in an Asynchronous manner, ($\overline{WEN}$ should be tied to its active state).
WHSTL[1]	Write Port HSTL Select	LVTTL INPUT	This pin is used to select HSTL or 2.5V LVTTL inputs for the FIFO. If HSTL inputs are required, this input must be tied HIGH. Otherwise it should be tied LOW.
Vcc	+2.5v Supply	I	These are Vcc supply inputs and must be connected to the 2.5V supply rail.
GND	Ground Pin	I	These are Ground pins an dmust be connected to the GND rail.
Vref	Reference Voltage	I	This is a Voltage Reference input and must be connected to a voltage level determined from the table, "Recommended DC Operating Conditions". This provides the reference voltage when using HSTL class inputs. If HSTL class inputs are not being used, this pin should be tied LOW.
V_{DDQ}	O/P Rail Voltage	I	This pin should be tied to the desired voltage rail for providing power to the output drivers.

NOTES:
1. Inputs should not change state after Master Reset.
2. If the JTAG feature is not being used, TCK and $\overline{TRST}$ should be tied LOW.

ORDERING INFORMATION



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