

**LAYER 1 : TOP**  
**LAYER 2 : SGND**  
**LAYER 3 : IN1**  
**LAYER 4 : IN2**  
**LAYER 5 : SVCC**  
**LAYER 6 : BOT**

**DDRIII-SODIMM1**    DDRIII 800/1066 MT/s  
1333MT/s CFD only  
PAGE 12

**DDRIII-SODIMM2**    DDRIII 800/1066 MT/s  
1333MT/s CFD only  
PAGE 13

**CPU**  
Auburndale 35W  
Clarkfield 45W  
PAGE 3~6

**nVIDIA**  
N10M-GE 128 Bit  
N10P-GE 969p  
PAGE 14~20

HDMI CON PAGE 22  
CRT PAGE 22  
LCD CONN PAGE 21

**Cable Docking**

- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 32

**SYSTEM POWER RT8206B**  
PAGE 35

**VCCP +1.1VT(RT8208A) AND PCH 1.05V(RT8204)**  
PAGE 36

**CPU CORE ISL6251A**  
PAGE 41

**VGACORE(1.025V) RT8208A**  
PAGE 38

**DDR III SMD DR\_VTERM 1.5V/1.5VSUS(RT8207)**  
PAGE 39

**SYSTEM CHARGER(ISL6251AHAZ-T)**  
PAGE 40

Keyboard PAGE 31  
Touch Pad PAGE 29

Capacitive Sense SW PAGE 32

**ENE KBC KB3926 D2**  
PAGE 29

GMT G9931P1U  
FAN PAGE 32    SPI PAGE 29

**SATA - HDD**    SATA0 150MB    PAGE 31

**SATA - CD-ROM**    SATA1 150MB    PAGE 31

**SATA - 2ndHDD**    SATA4 150MB    PAGE 31

**E-SATA**    SATA5 150MB    PAGE 30

Accelerometer LIS3LV02DL PAGE 25    **SMBUS**

**PCH Ibex-M**  
PAGE 7~11

**CLOCK GEN 9LRS3197**  
PAGE 2

Mini PCI-E Card x2  
Express Card x1  
Cable Docking x1

**USB2.0**    4,7,10,11

0,1,8,9    5    3    2

**USB2.0 Ports X4** PAGE 30    **BlueTooth** PAGE 30    **Webcam** PAGE 30    **Fingerprint** PAGE 30

**PCI-E**    24.576MHz

X1    X1    X1    X1    X1

**Mini PCI-E Card** WWAN/TV PAGE 34    **Mini PCI-E Card** Wireless LAN PAGE 34    **LAN** Realtek RTL8111DL GigaLAN PAGE 27    **Express Card** PAGE 31    **JMICRO 380** PAGE 23

**IEEE1394** PAGE 23    **Memory CardReader** PAGE 23

**RJ45** PAGE 27

**ONFI**

**Braidwood** PAGE 33    **SPI** PAGE 7    **MDC CONN** PAGE 32

**Analog** IDT92HD75B3 PAGE 24

**AUDIO Amplifier** TPA6047A4 PAGE 25    **AUDIO Amplifier** TPA3007D1 PAGE 26

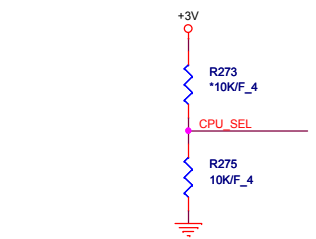
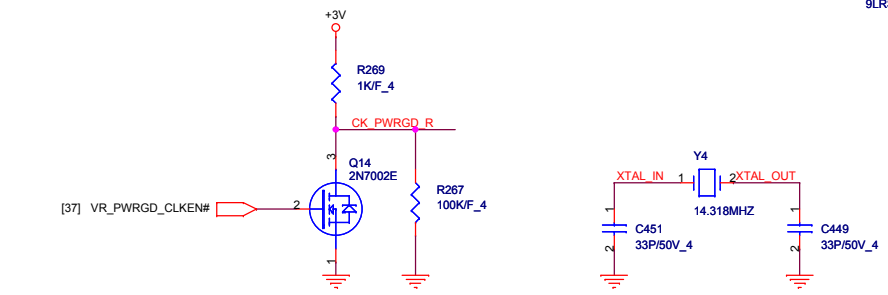
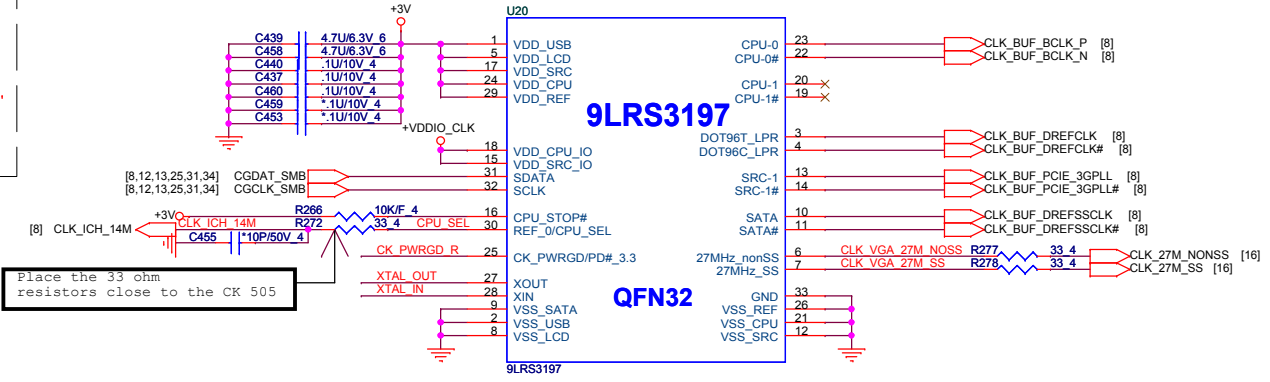
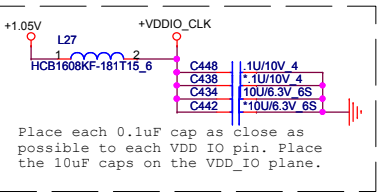
microphone PAGE 24    Audio Jacks (Phone/ MIC) PAGE 24    Jack to Speaker PAGE 25    Jack to Sub-Woofer PAGE 26

**PROJECT : UP67**  
Quanta Computer Inc.

**NB5**

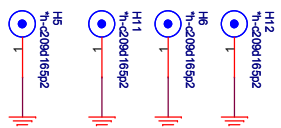
Size Custom    Document Number **BLOCK DIAGRAM**    Rev 1A

Date: Monday, October 26, 2009    1 Sheet 1 of 45

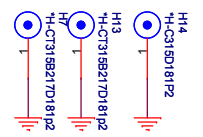


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

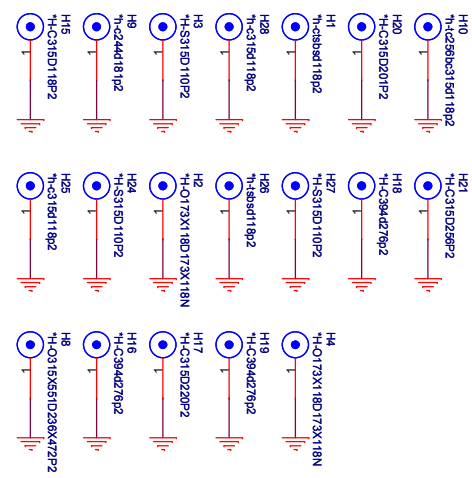
**CPU bracket Hole.**



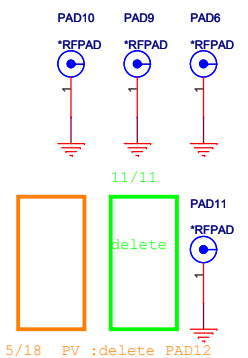
**VGA bracket Hole.**



**M/B Screw Hole**



**RF PAD**



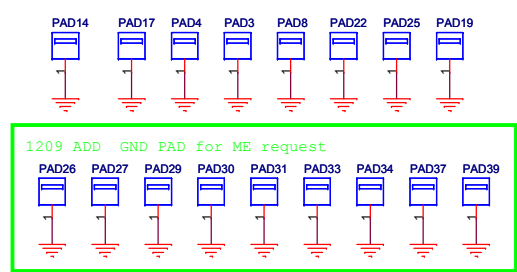
**ME PAD**



**Routed spring**

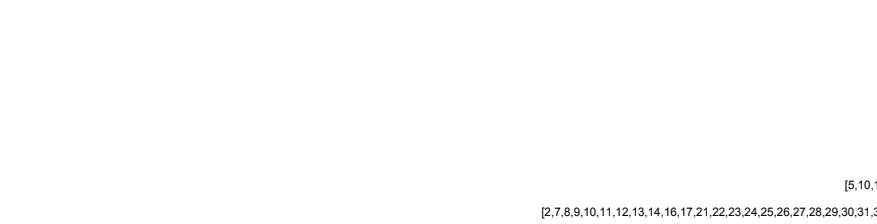
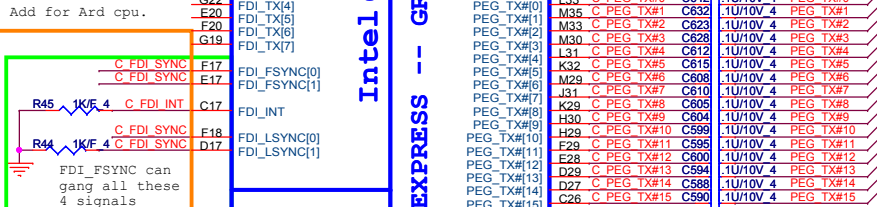
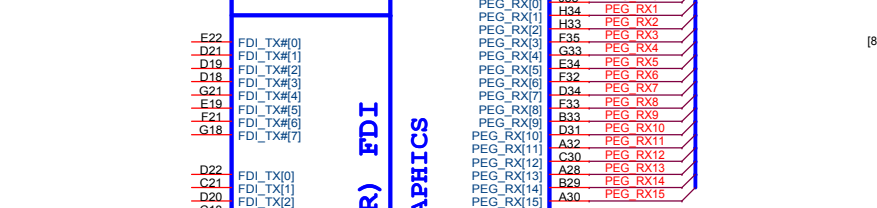
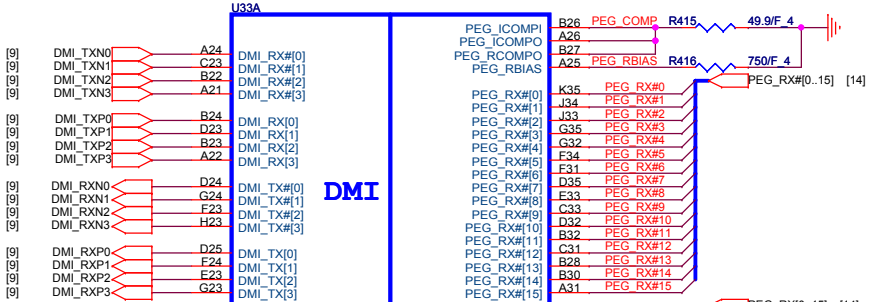


**ME-Ground Pad**

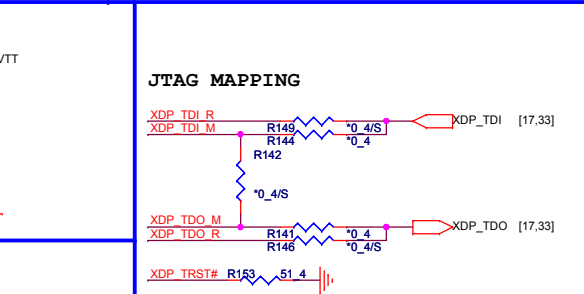
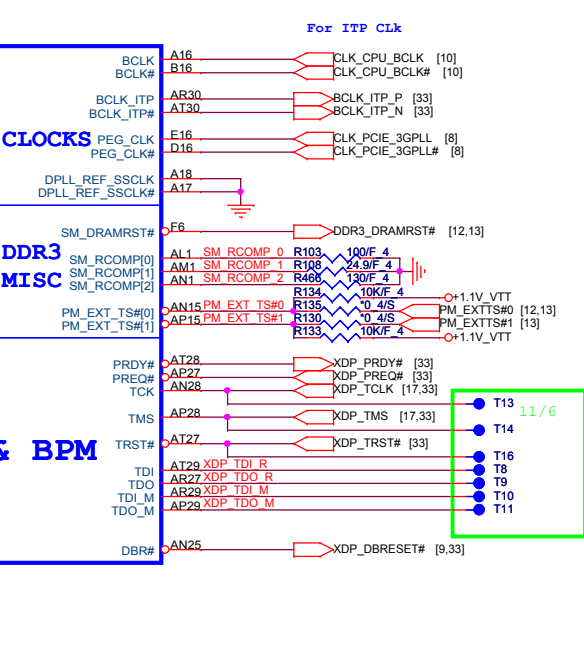
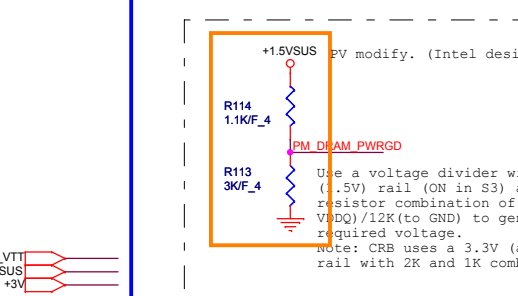
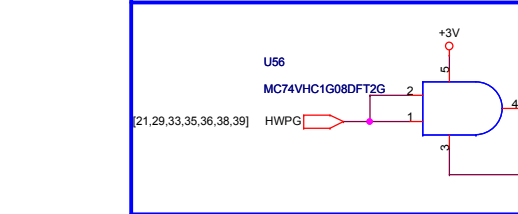
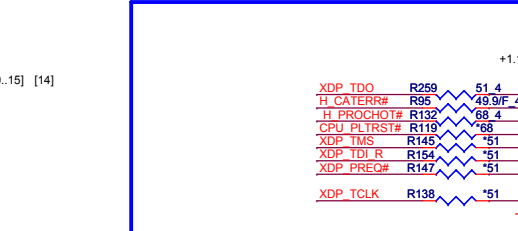
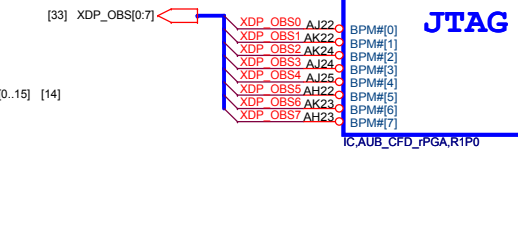
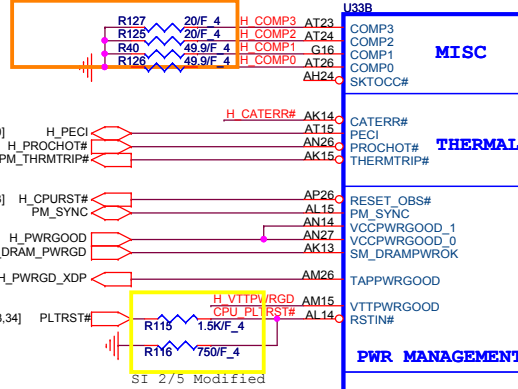


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Quanta Computer Inc.

Size Custom	Document Number <b>CLOCK &amp; Screw Holes</b>	Rev 1A
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6/1: Add for Ard cpu.



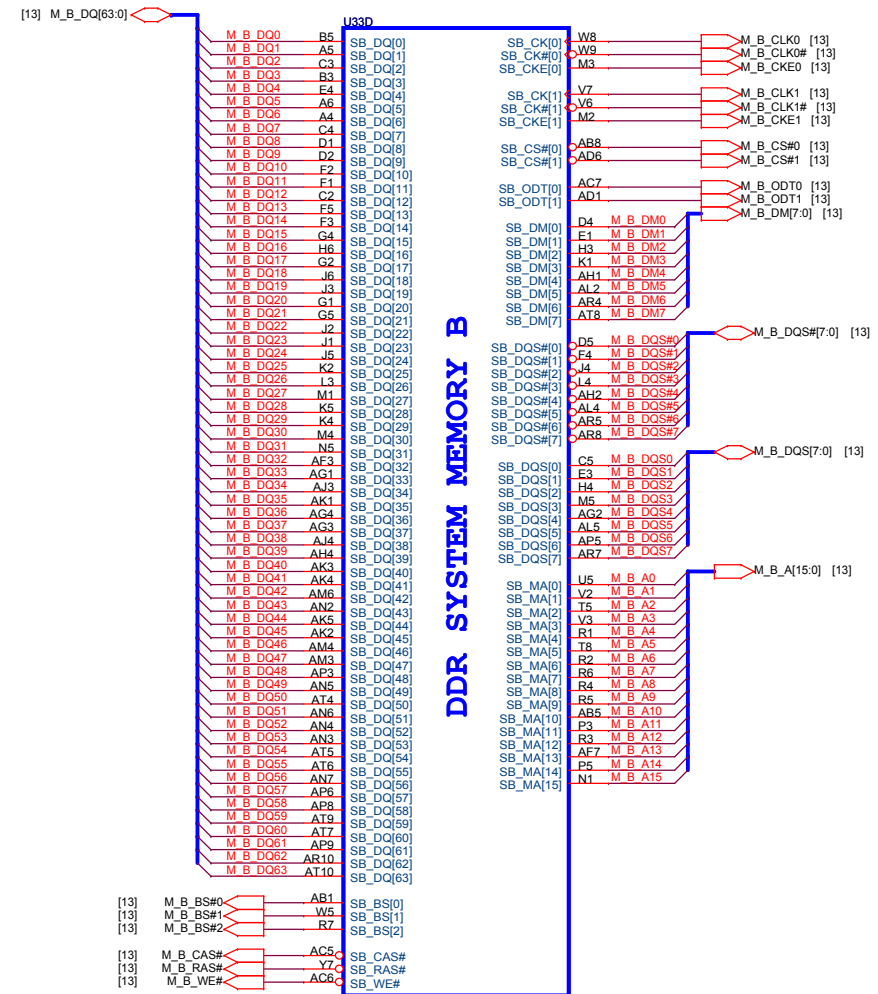
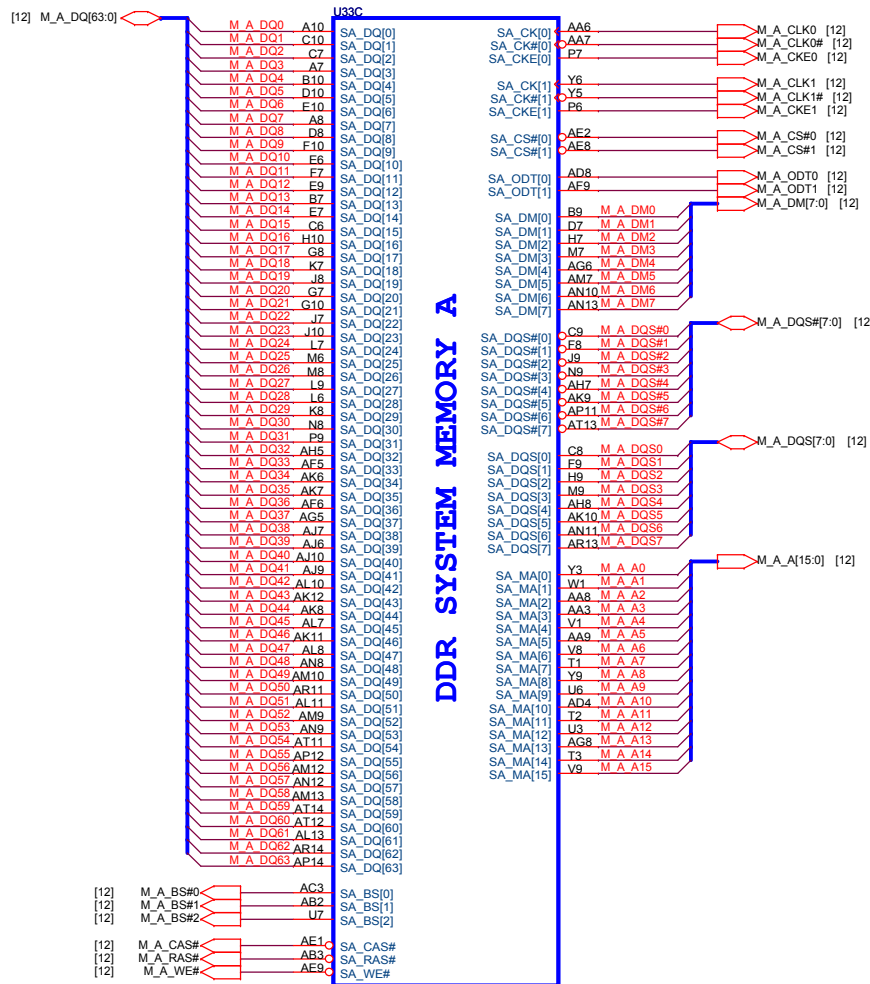
Scan Chain (Default)	STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only	STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only	STUFF -> R512, R90 NO STUFF -> R97, R84, R89

**NB5**

**PROJECT : UP67**  
Quanta Computer Inc.

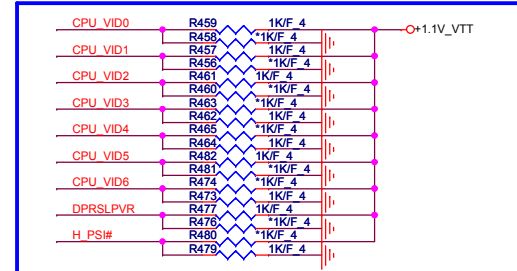
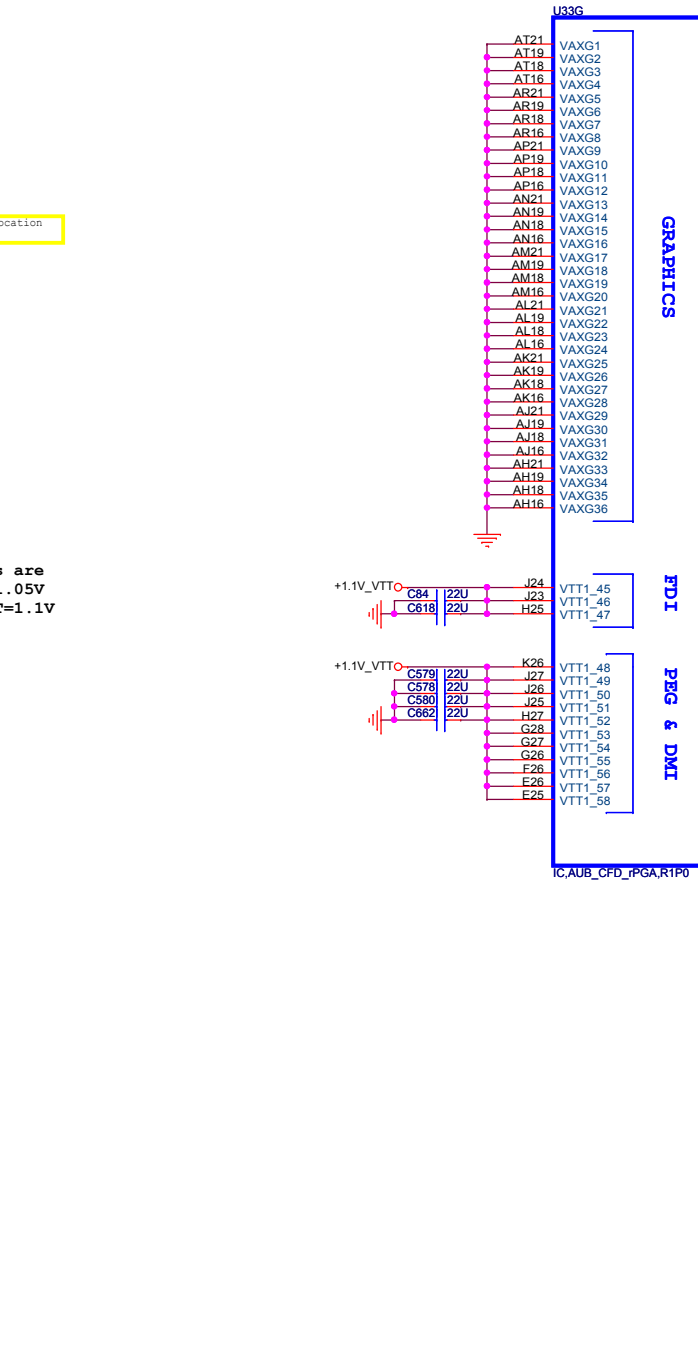
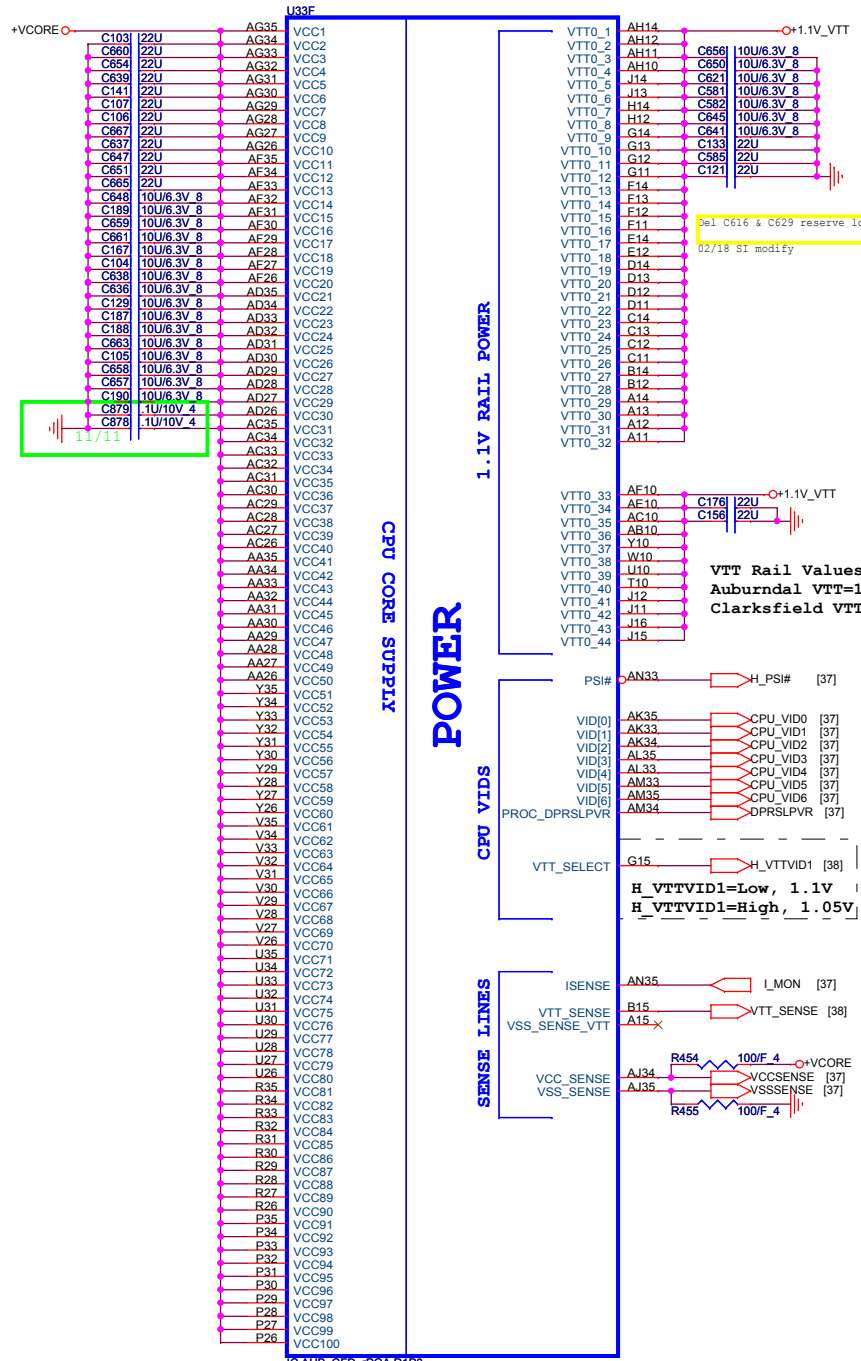
Size Custom	Document Number <b>PROCESSOR 1/4(HOST&amp;PEX)</b>	Rev 1A
Date: Monday, October 26, 2009		Sheet 3 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



- [12] M\_A\_BS#0 AC3 SA\_BS[0]
- [12] M\_A\_BS#1 AB2 SA\_BS[1]
- [12] M\_A\_BS#2 U7 SA\_BS[2]
- [12] M\_A\_CAS# AE1 SA\_CAS#
- [12] M\_A\_RAS# AB3 SA\_RAS#
- [12] M\_A\_WE# AE9 SA\_WE#

- [13] M\_B\_BS#0 AB1 SB\_BS[0]
- [13] M\_B\_BS#1 W5 SB\_BS[1]
- [13] M\_B\_BS#2 R7 SB\_BS[2]
- [13] M\_B\_CAS# AC5 SB\_CAS#
- [13] M\_B\_RAS# Y7 SB\_RAS#
- [13] M\_B\_WE# AC6 SB\_WE#



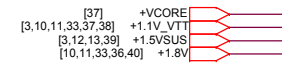
HFM\_VID : Max 1.4V  
LFM\_VID : Min 0.65V

**PROJECT : UP67**  
**Quanta Computer Inc.**

**NB5**

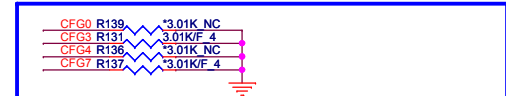
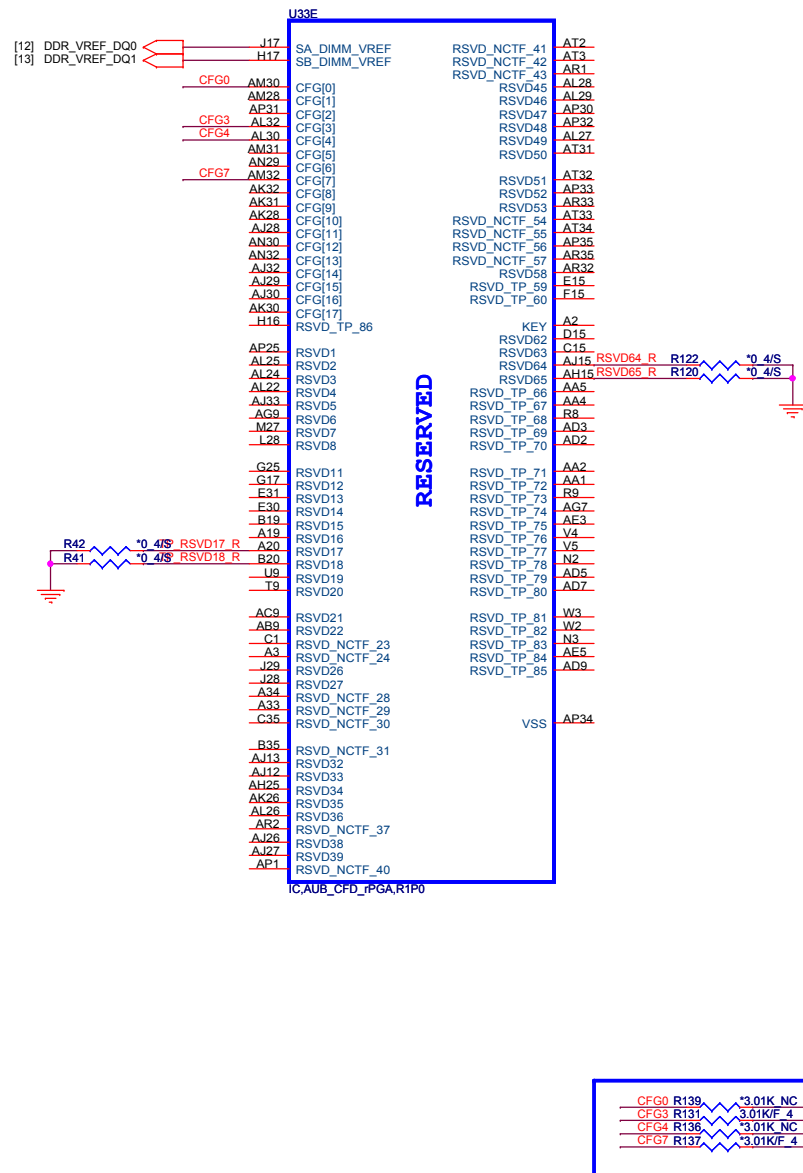
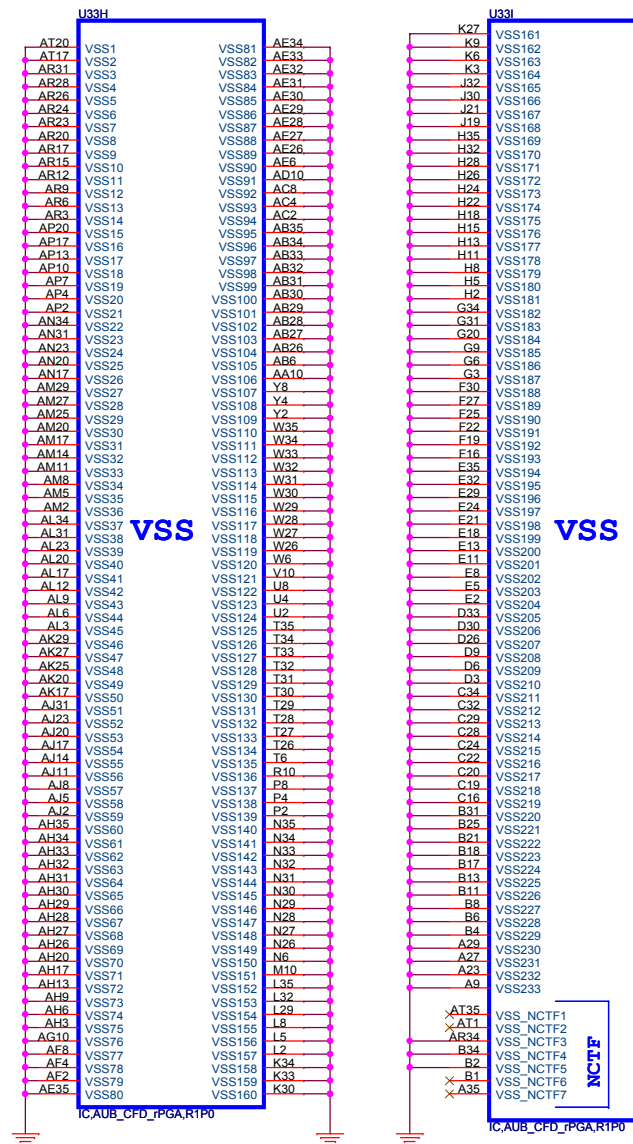
Size Custom Document Number **PROCESSOR 3/4(POWER)** Rev 1A

Date: Monday, October 26, 2009 | Sheet 5 of 45



# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

# AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

CFG[ 1:0 ] - PCI\_Epress Configuration Select  
 \* 11= 1 x 16 PEG  
 \* 10= 2 x 8 PEG

**PROJECT : UP67**  
 Quanta Computer Inc.

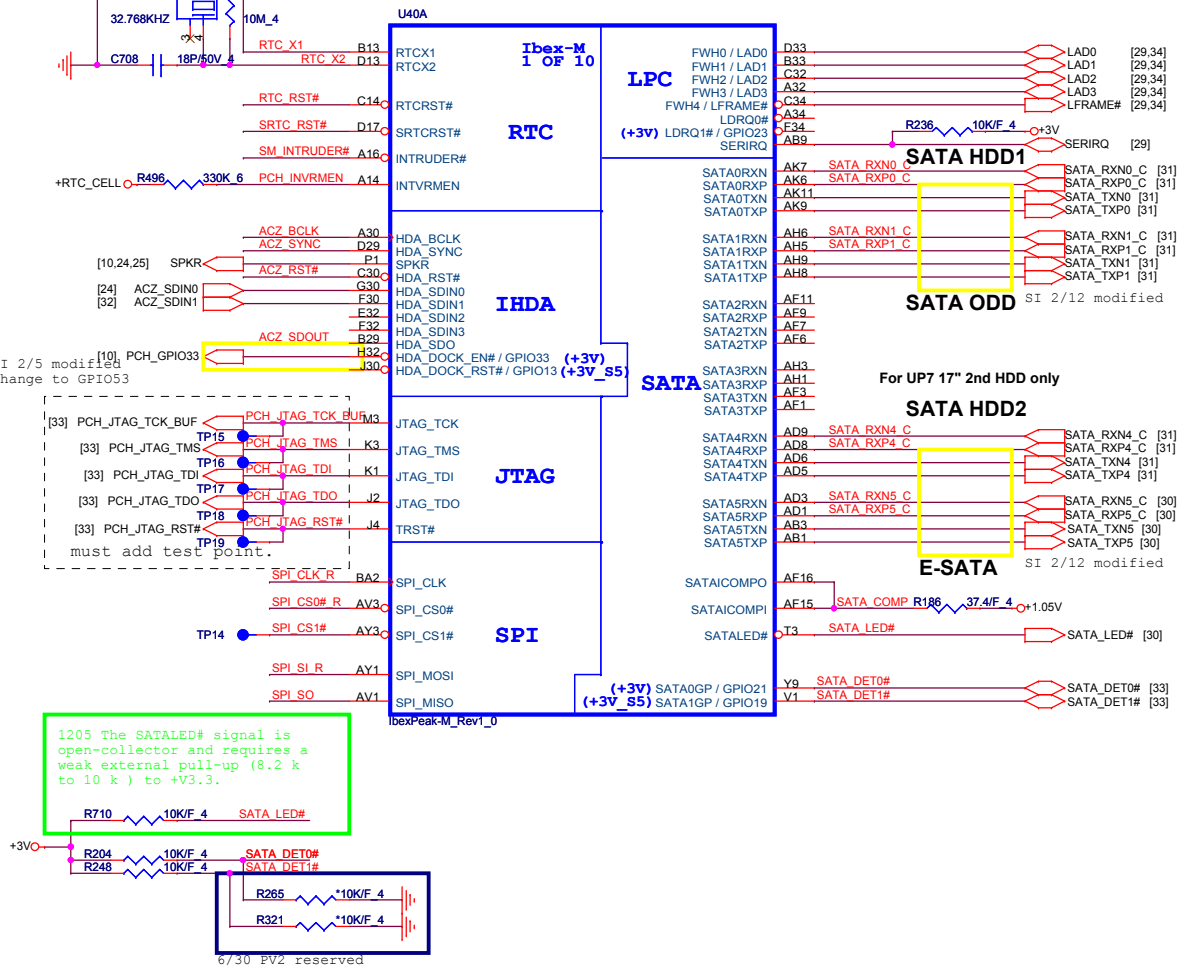
**NB5**

Size Custom Document Number **PROCESSOR 4/4(GND)** Rev 1A  
 Date: Monday, October 26, 2009 | Sheet 6 of 45

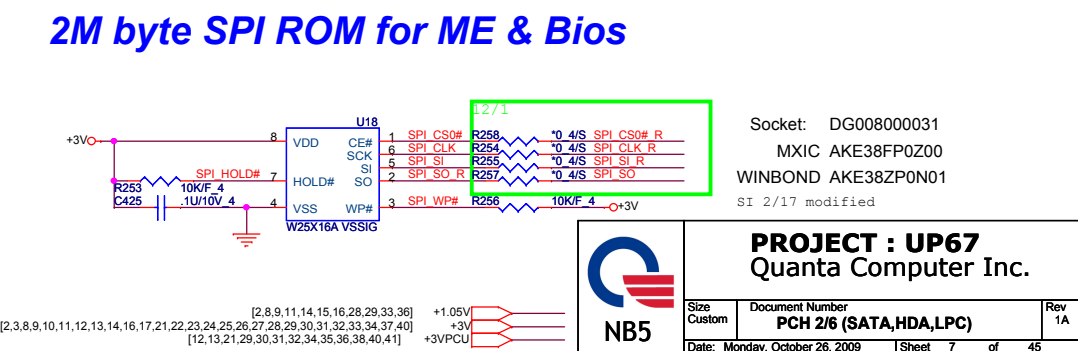
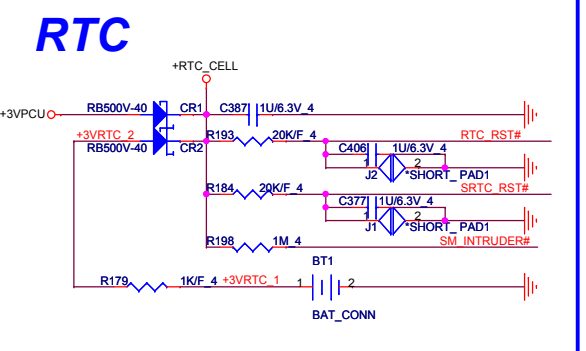
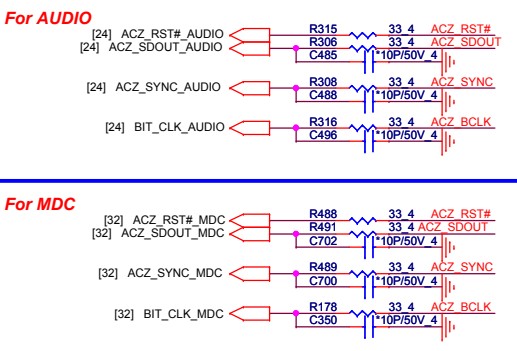
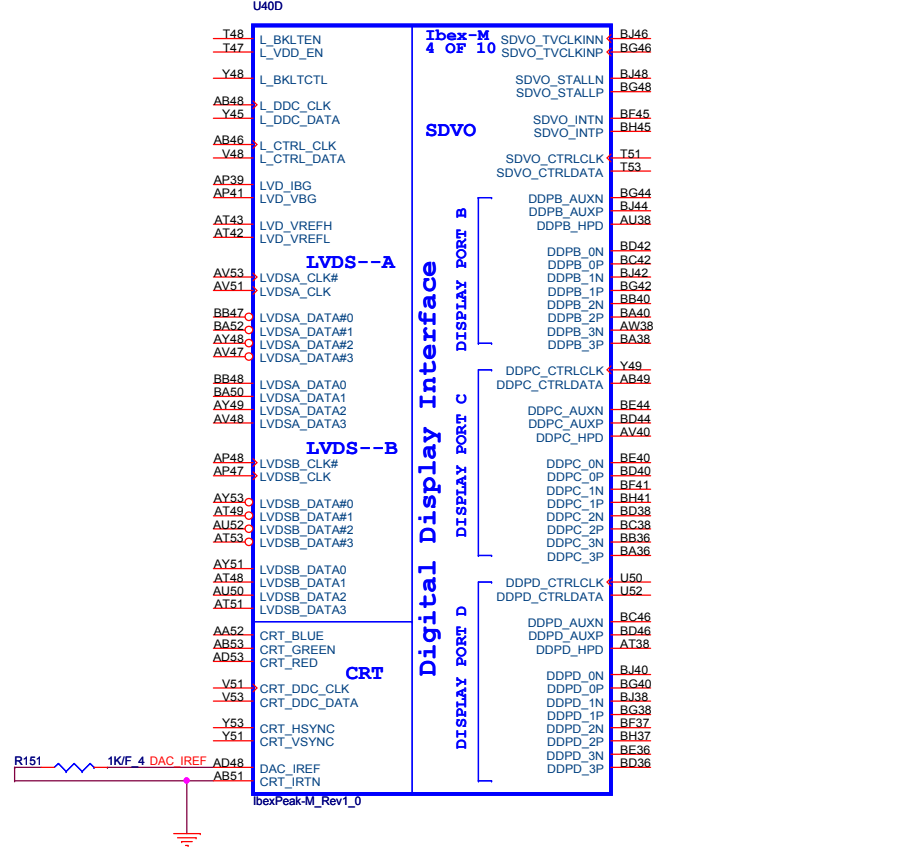


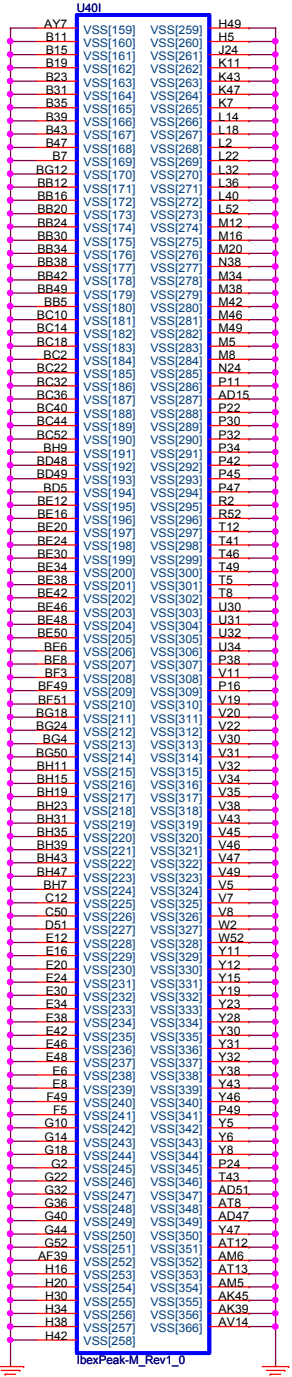
INTVRMEN - Integrated SUS 1.1V VRM Enable High - Enable Internal VRs

### IBEX PEAK-M (HDA,JTAG,SATA)

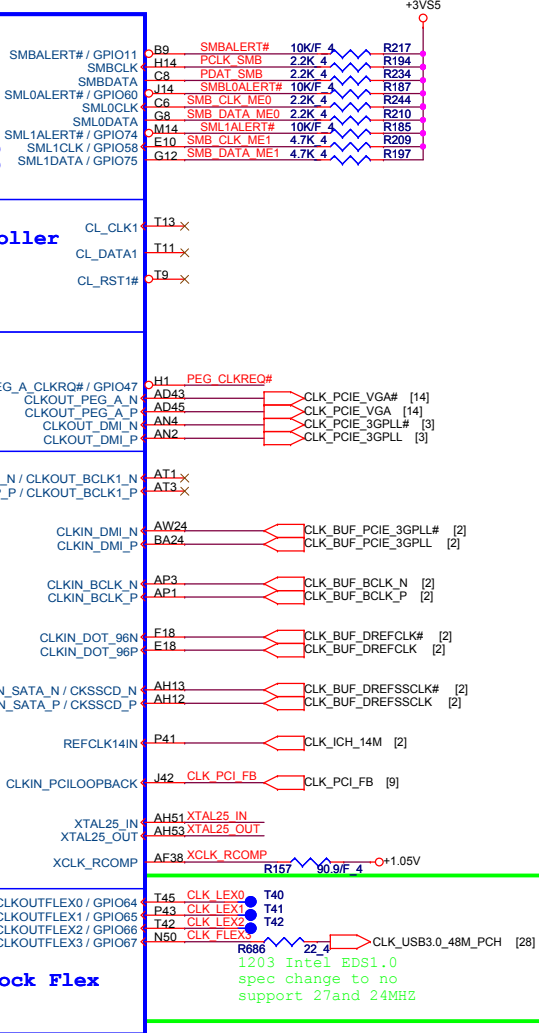
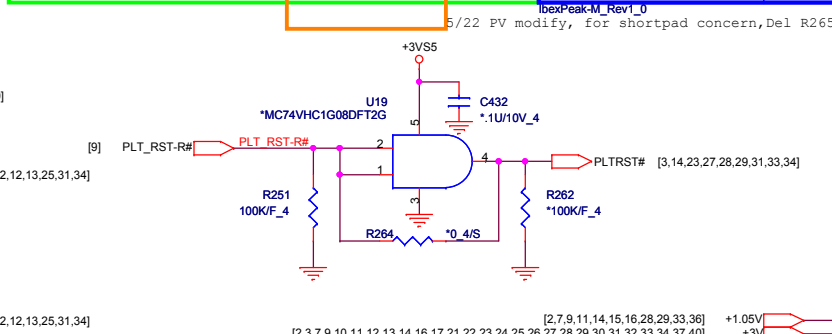
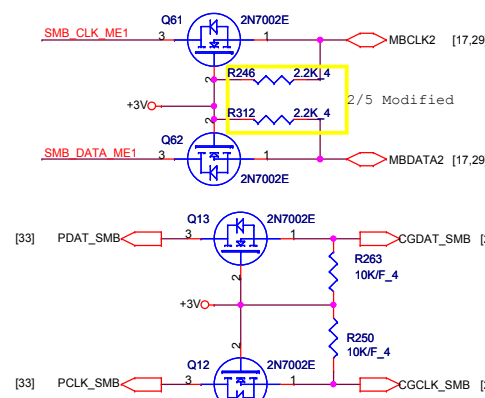
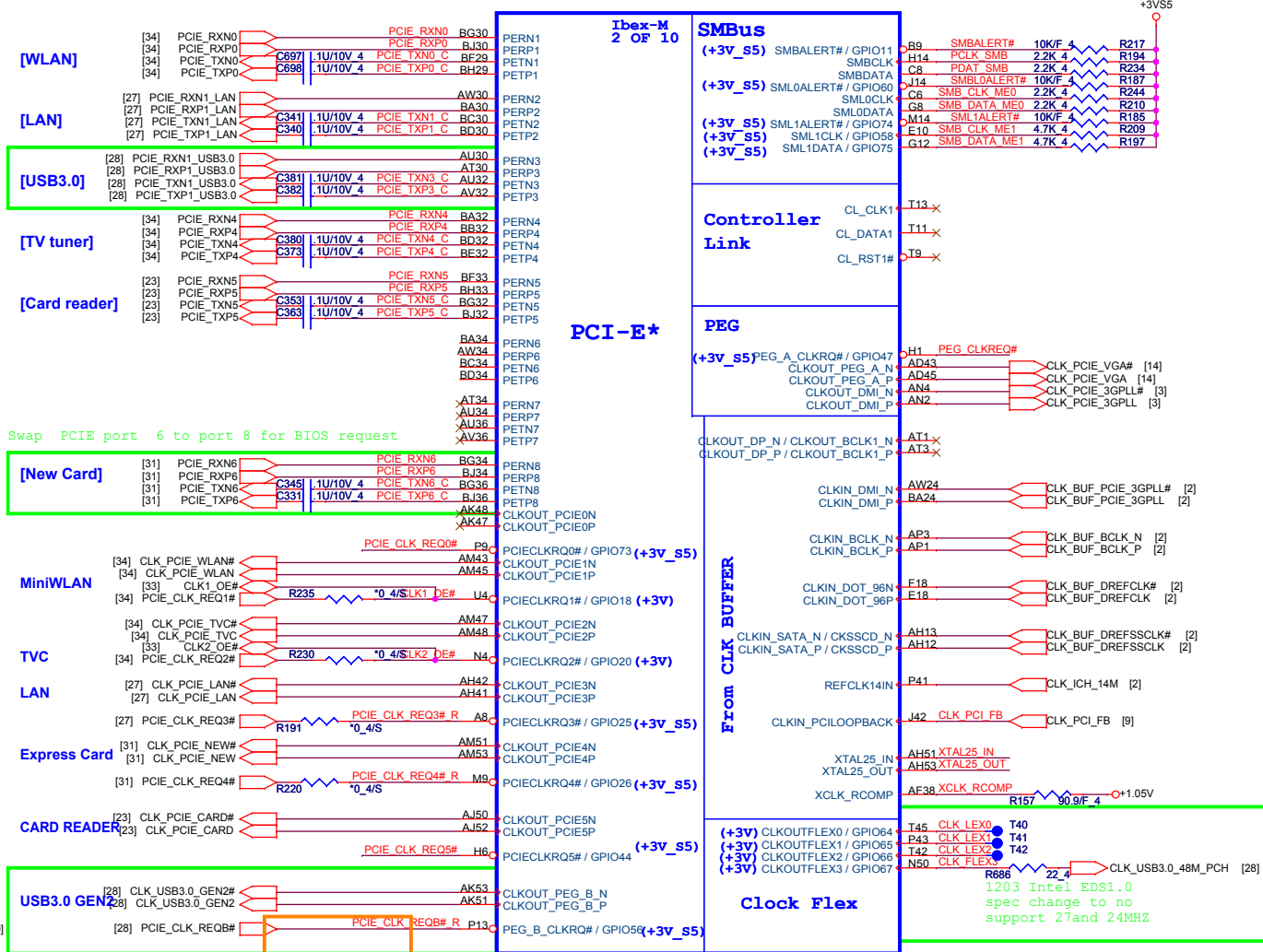


### IBEX PEAK-M (LVDS,DDI)





IBEX PEAK-M (PCI-E, SMBUS, CLK)



**PROJECT : UP67**  
Quanta Computer Inc.

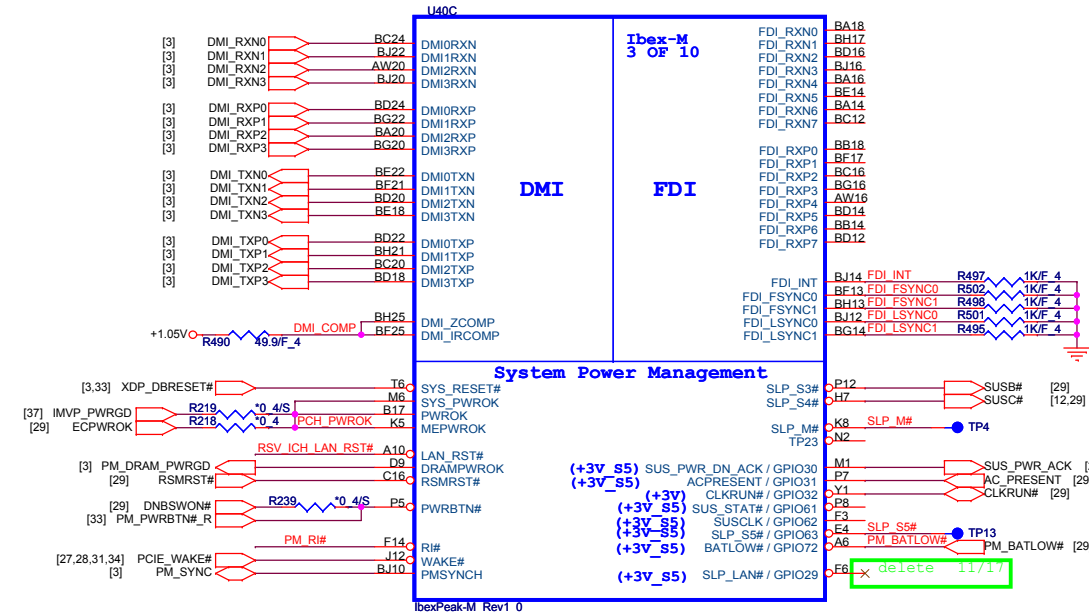
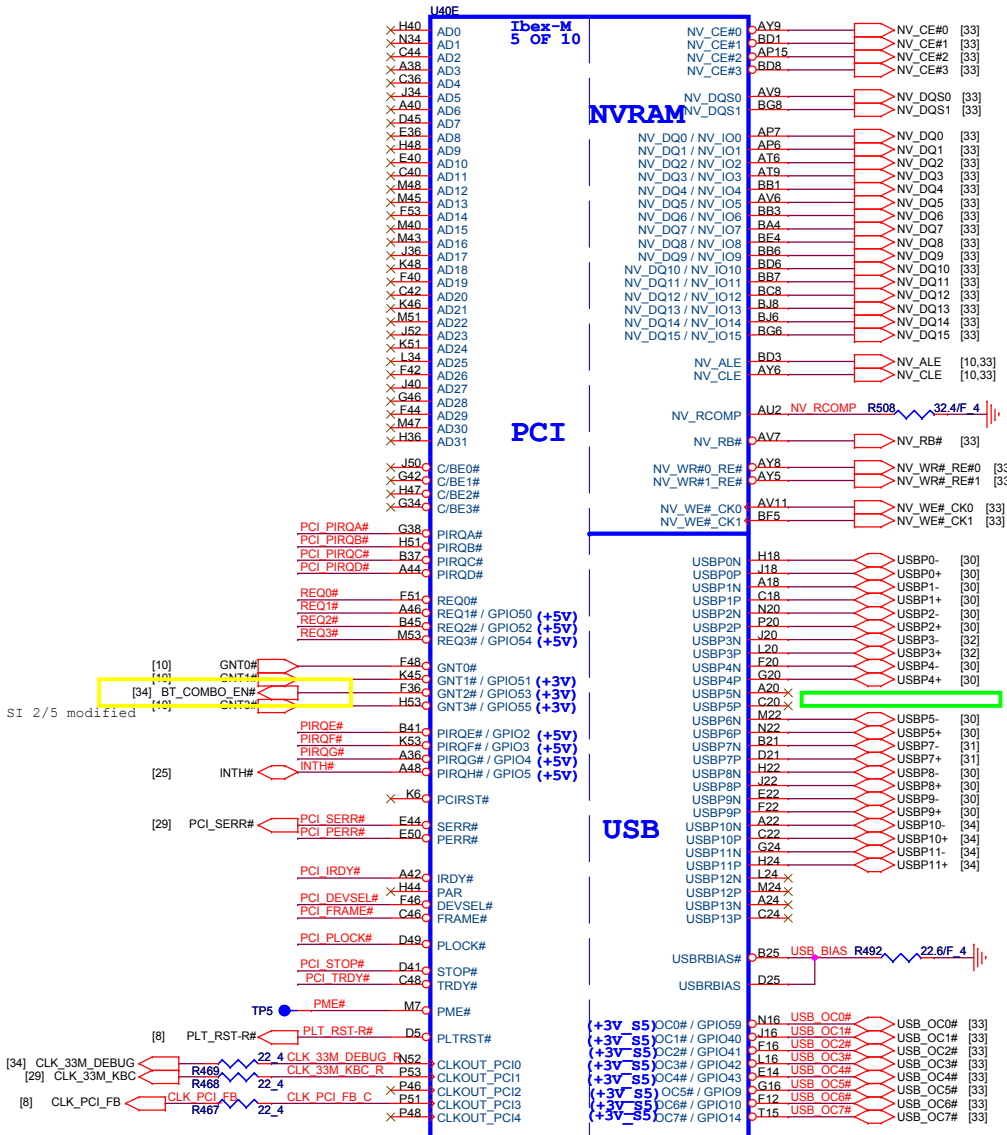
Size Custom Document Number **PCH 3/6 (PCI,ONFI,USB,CK)** Rev 1A

Date: Monday, October 26, 2009 | Sheet 8 of 45



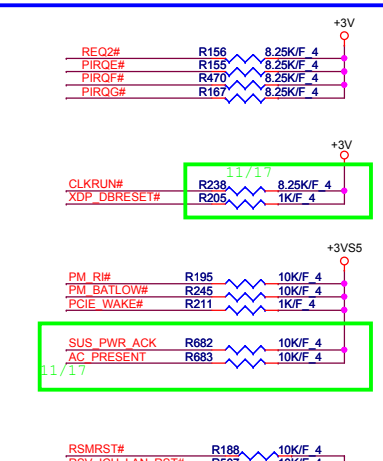
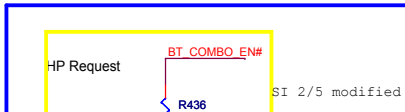
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)



SI 2/5 modified

1209 swap to port 6 from BIOS request



IbexPeak-M\_Rev1\_0

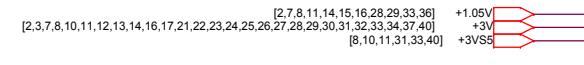
IbexPeak-M\_Rev1\_0

delete 11/17



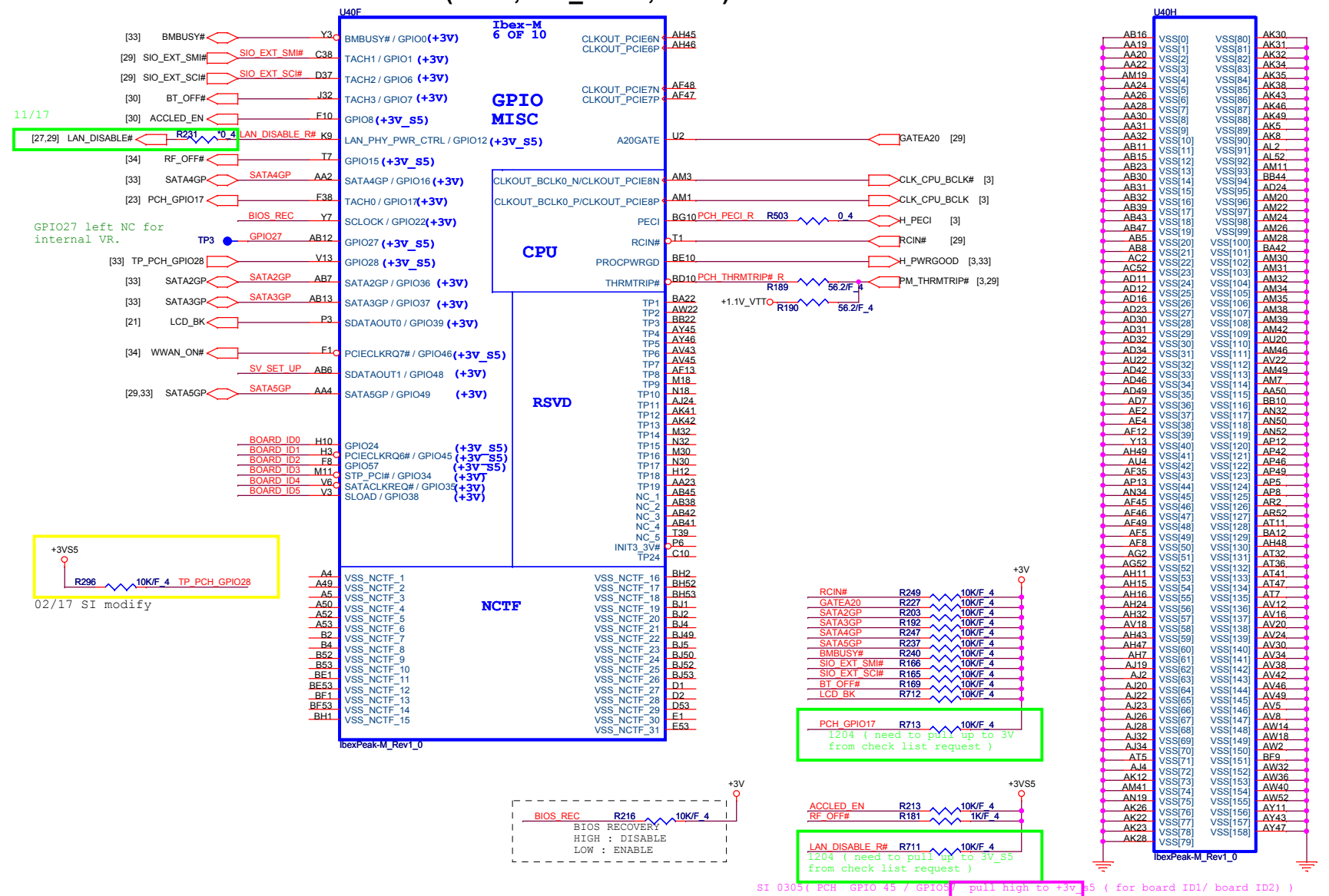
PROJECT : UP67  
Quanta Computer Inc.

Size Custom	Document Number <b>PCH 6/6 (GND)/ Braidwood</b>	Rev 1A
Date: Monday, October 26, 2009	Sheet 9 of 45	



# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)

# IBEX PEAK-M (GND)



[9] GNT3# \*10K NC

**A16 swap override Strap/Top-Block Swap Override jumper**

GNT3#

Low = A16 swap override/Top-Block Swap Override enabled  
High = Default

SV\_SET\_UP R223 10K/F 4  $\rightarrow$  +3V

SV\_SET\_UP

1-X High = Strong (Default)

[9] GNT0# \*1K/F 4

[9] GNT1# \*1K/F 4

BIOS boot from SPI  
SI 2/5 modified

**Boot BIOS Strap**

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

[9,33] NV\_ALE \*1K/F 4

[9,33] NV\_CLE \*1K/F 4  $\rightarrow$  +1.8V

**Danbury Technology Enabled**

NV\_ALE

High = Enable  
Low = Disable

**DMI Termination Voltage**

NV\_CLE

Set to Vcc when LOW  
Set to Vcc/2 when HIGH

**No Reboot Strap**

[7,24,25] SPKR \*1K/F 4  $\rightarrow$  +3V

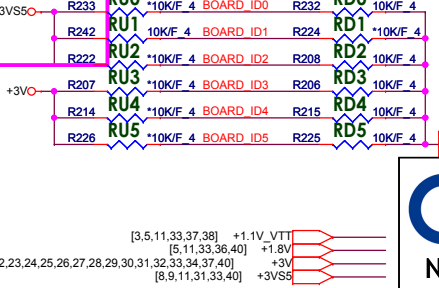
[7] PCH\_GPIO33 \*100K/F 4

SI 2/5 modified

**BOARD ID SETTING**

Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RDO (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RDO (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RDO (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UP6/7	0=UP6 1=UP7					
UMA/Dis.		0=UMA 1=Dis.				
Project name			0=Jones/Cujo 2.0 (Clarkfield) 10=Jones/Cujo 2.1 (Auburndate UMA)			
ROM Size				0= 2M 1= 4M		



**PROJECT : UP67**  
Quanta Computer Inc.

**NB5**

Size Custom Document Number PCH 4/6 (GPIO & Strap) Rev 1A

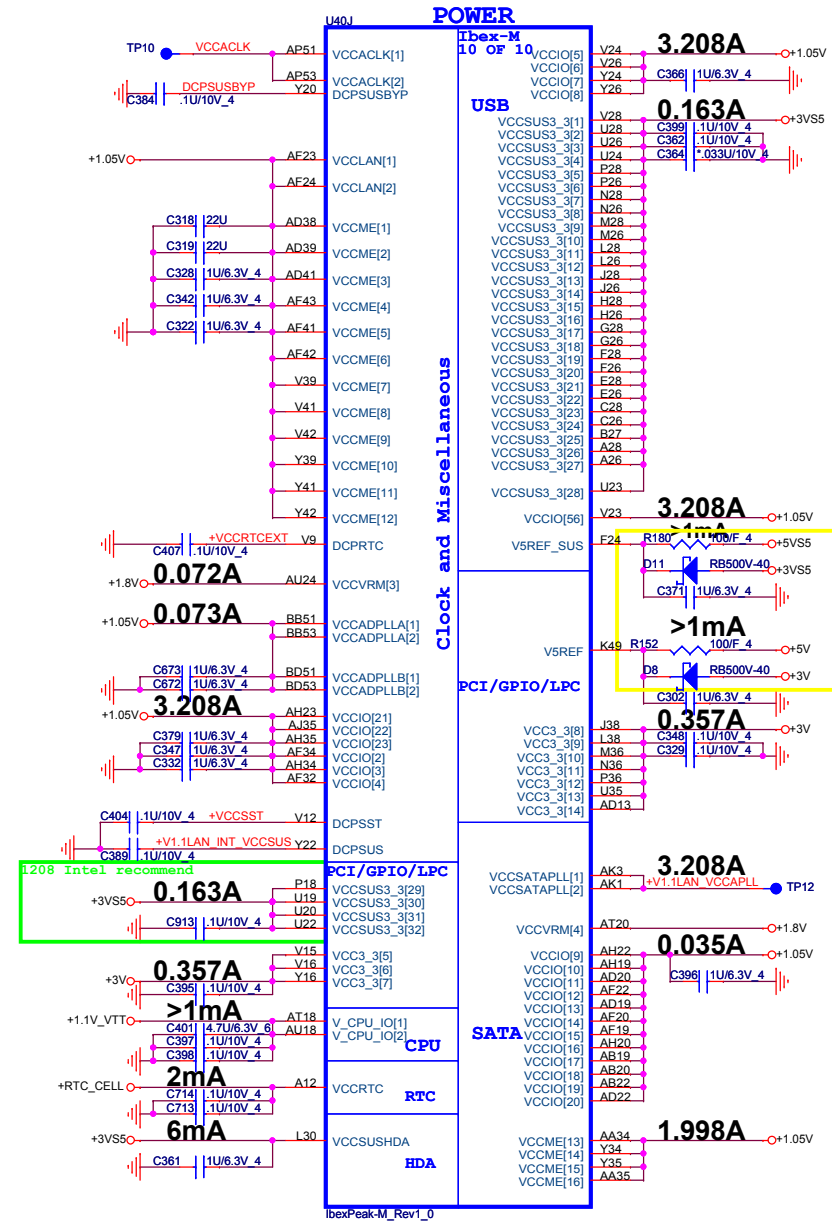
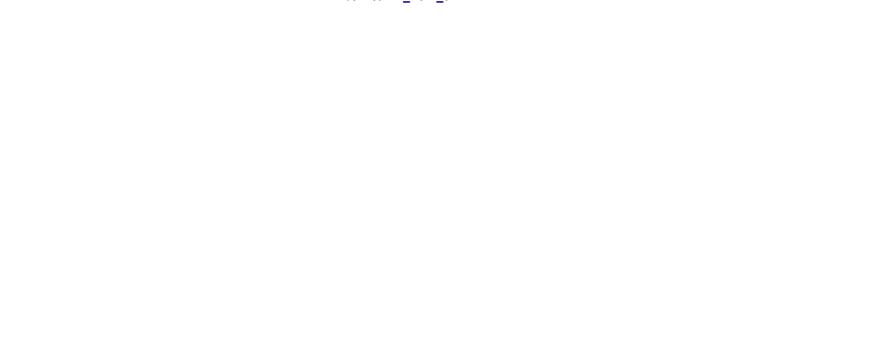
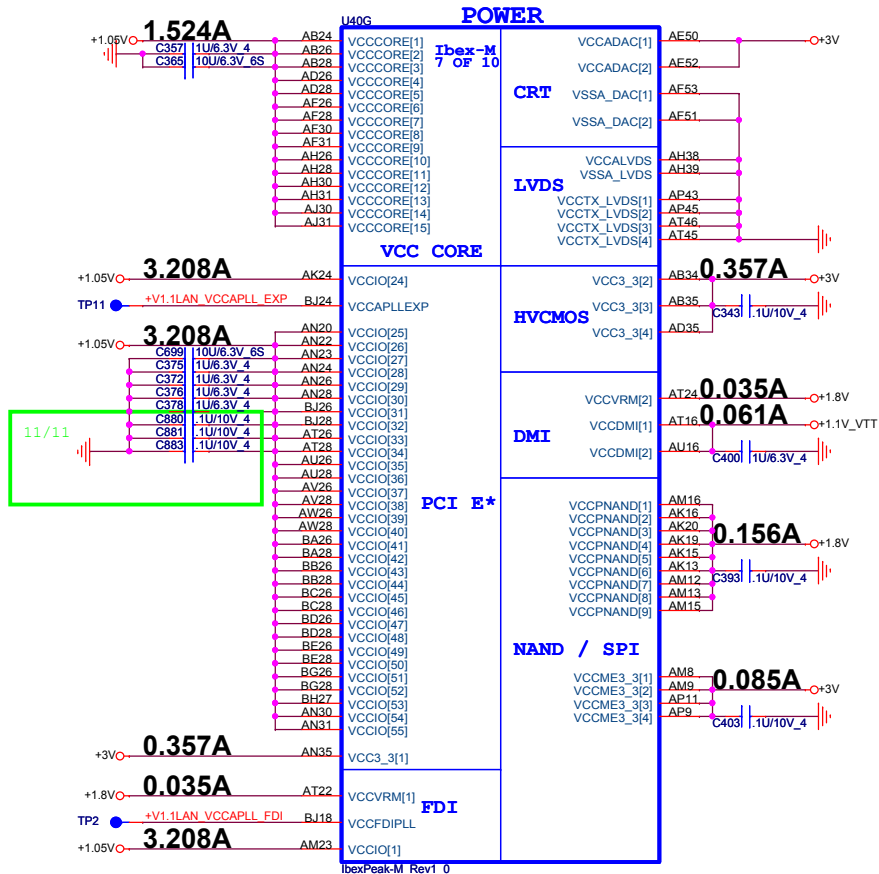
Date: Monday, October 26, 2009 | Sheet 10 of 45

[3,5,11,33,37,38] +1.1V\_VTT0 +1.1V\_VTT0

[5,11,33,36,40] +1.8V +1.8V

[2,3,7,8,9,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V +3V

[8,9,11,31,33,40] +3VSS +3VSS



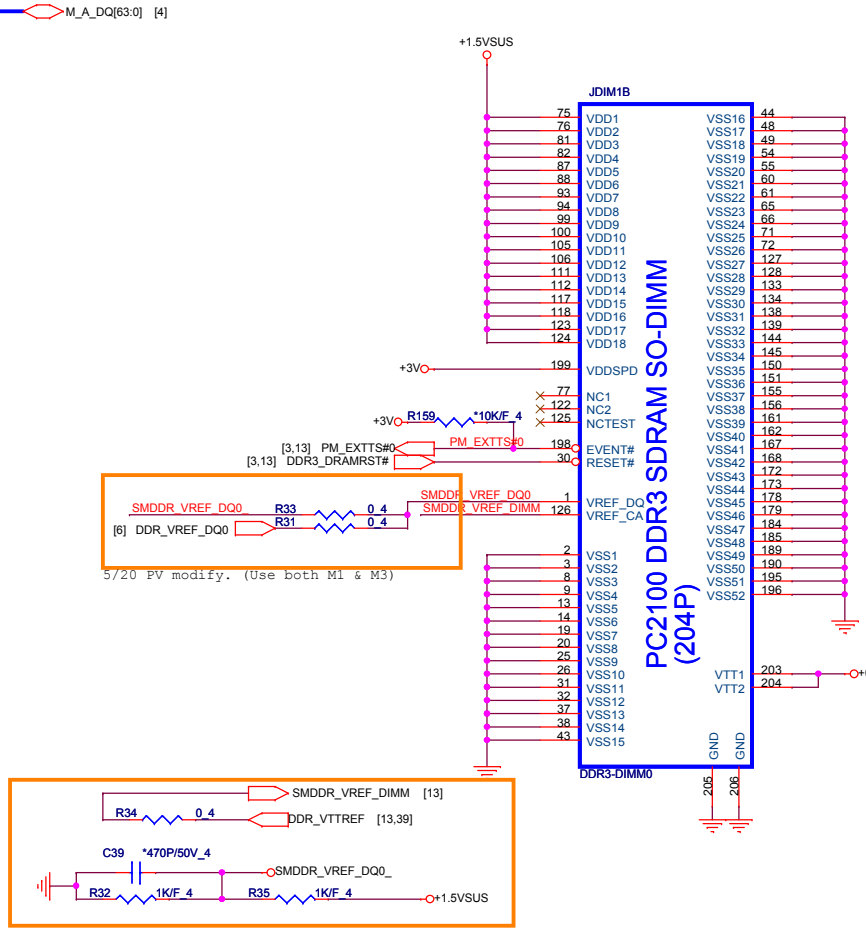
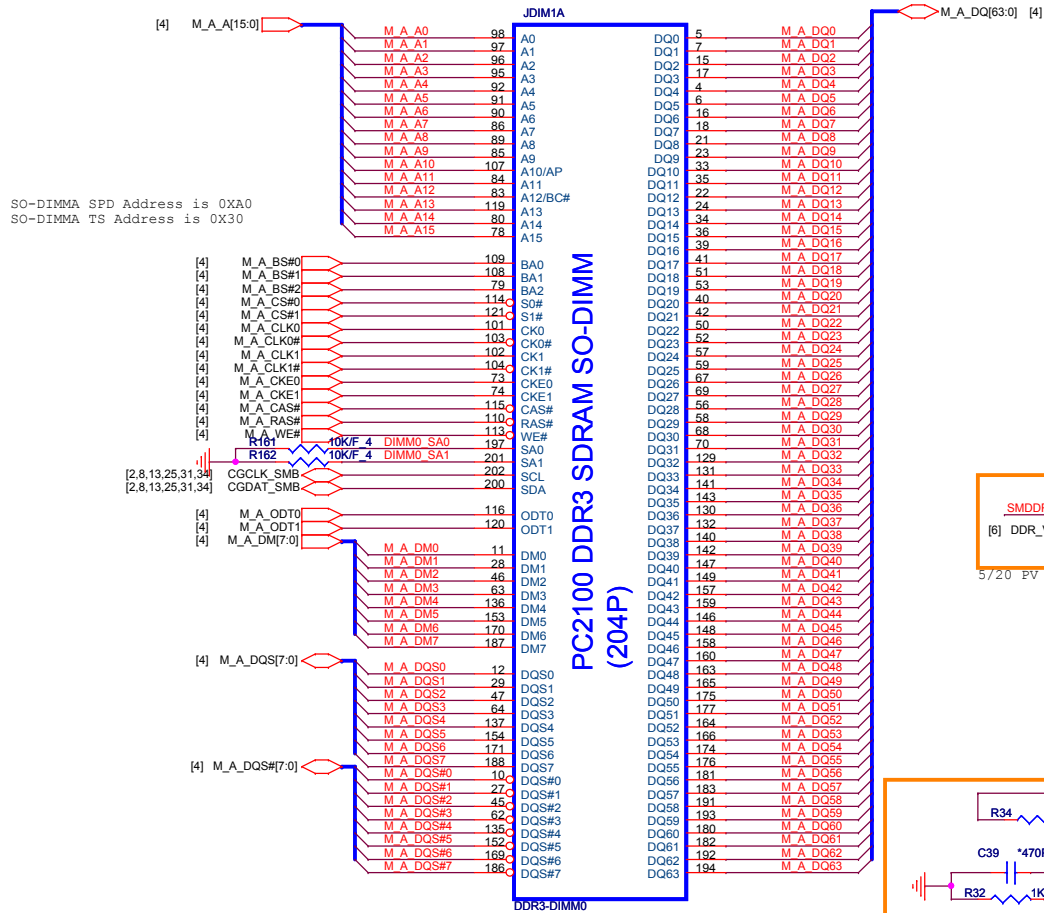
[2,7,8,9,14,15,16,28,29,33,36]	+1.05V	
[3,5,10,33,37,38]	+1.1V_VTT	
[5,10,33,36,40]	+1.8V	
[2,3,7,8,9,10,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40]	+3V	
[8,9,10,31,33,40]	+3VS5	
[21,22,24,25,30,31,32,34,40]	+5V	
[40]	+5VS5	

**PROJECT : UP67**  
**Quanta Computer Inc.**

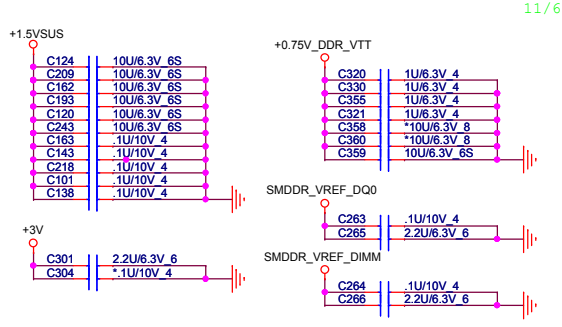
**NB5**

Size: Custom  
 Document Number: PCH 5/6 (POWER)  
 Date: Monday, October 26, 2009 | Sheet 11 of 45

Rev 1A

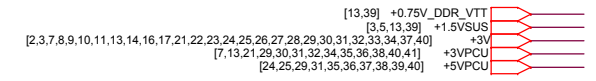


Place these Caps near So-Dimm0.



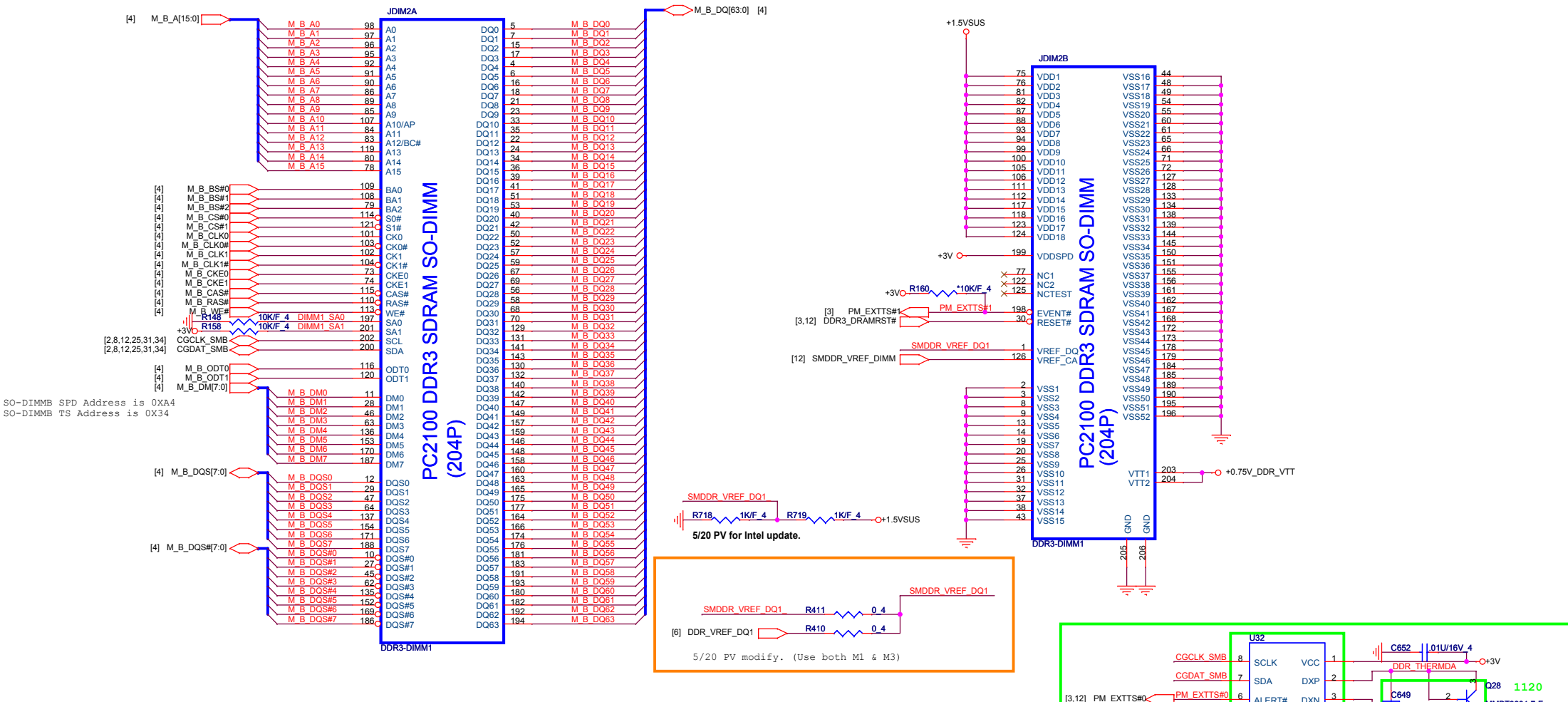
5/20: NA for INT recommend

reserve only...  
can let it NC at this block components if DB stage not trouble found



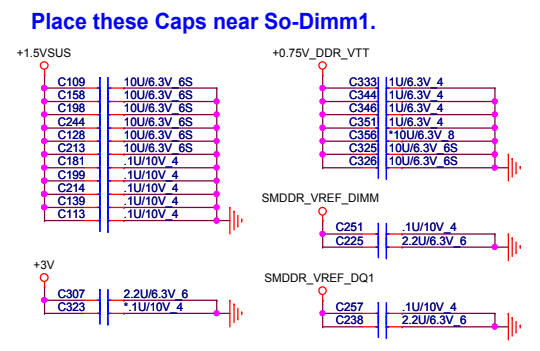
**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>DDR3 DIMM-0</b>	Rev 1A
Date: Monday, October 26, 2009   Sheet 12 of 45		

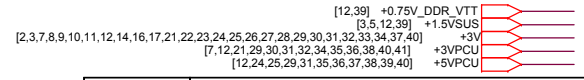
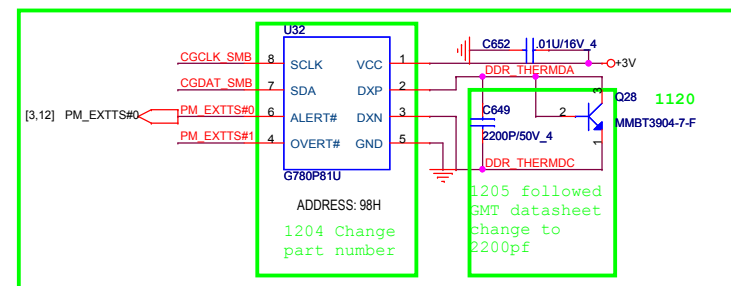


SO-DIMM SPD Address is 0XA4  
SO-DIMM TS Address is 0X34

5/20: NA for for INT recommend



reserve only..  
can let it NC at this block components if DB stage not trouble found



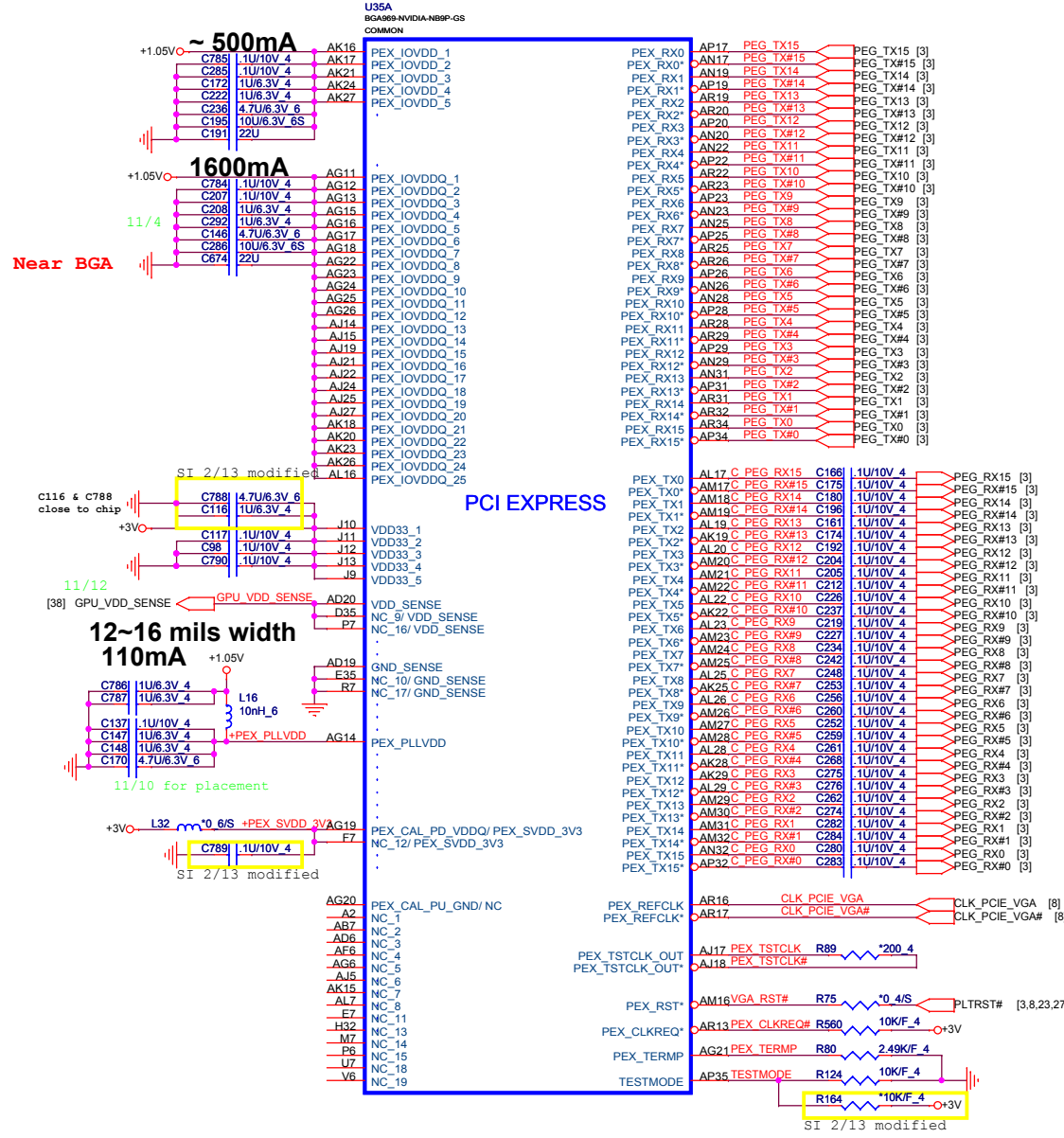
**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom    Document Number **DDR3 DIMM-1**    Rev 1A

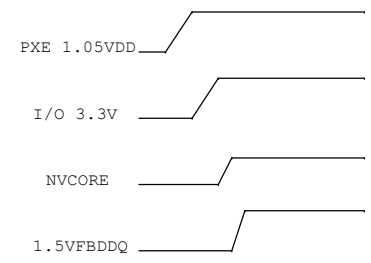
Date: Monday, October 26, 2009    Sheet 13 of 45



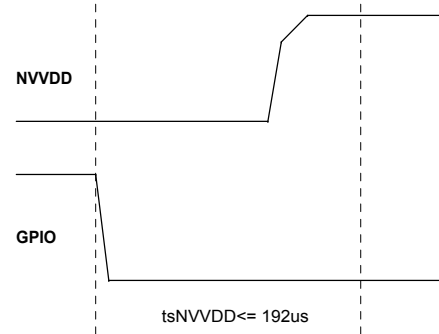
PEX\_IOVDD+PEX\_IOVDDQ+PEX\_PLLVDD >2.2A



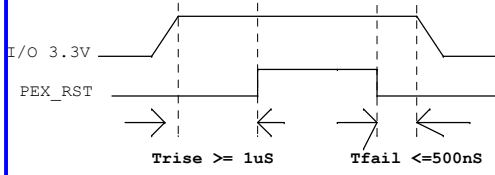
### power up sequence



### NB9M: VGACORE +0.90V (Normal) , +1.09V NVVDD Maximum Settling Time

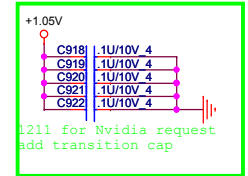


### PEX\_RST timing



### VGA Thermal Circuit

0514: PV modify  
Delete Reserved thermal circuit



[2,3,7,8,9,10,11,12,13,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] [2,7,8,9,11,15,16,28,29,33,36] +1.05V  
+3V

**PROJECT : UP67**  
Quanta Computer Inc.

Size Custom Document Number N10X (PCIE I/F) 1/5 Rev 1A

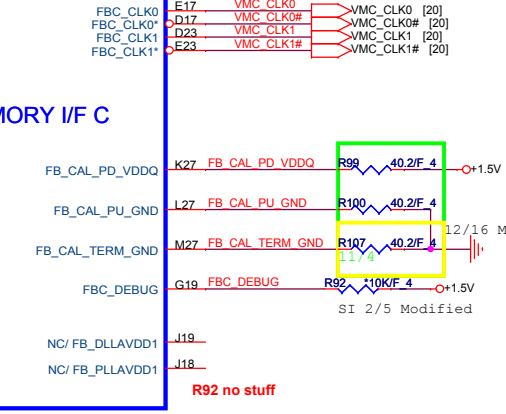
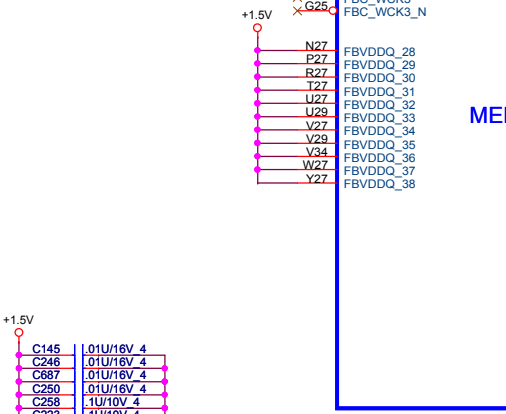
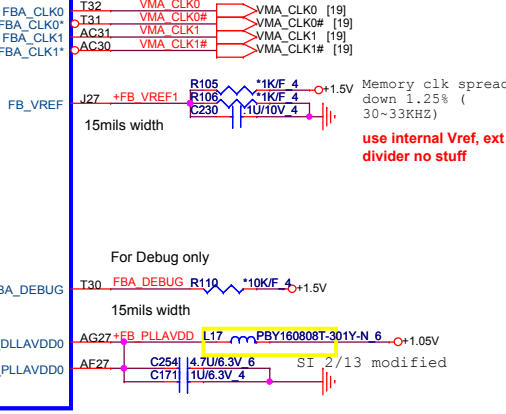
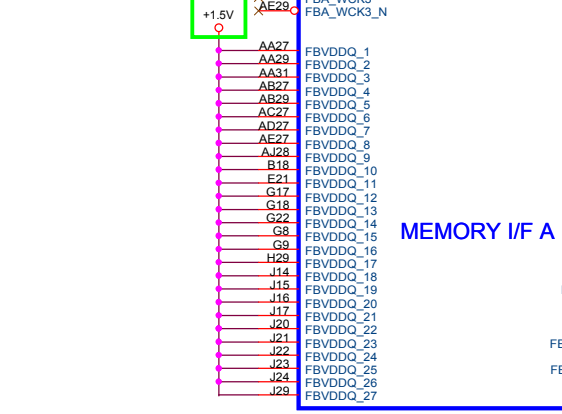
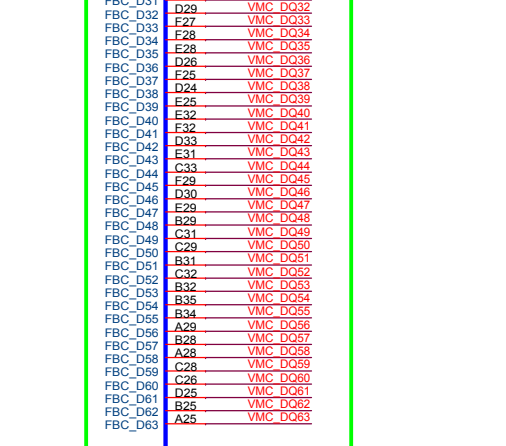
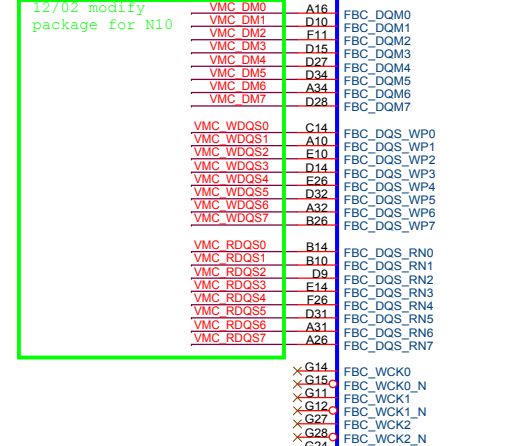
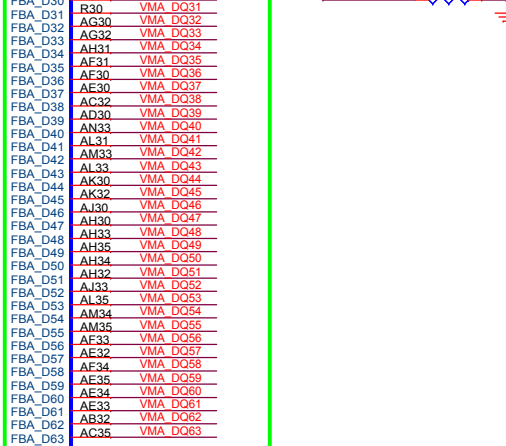
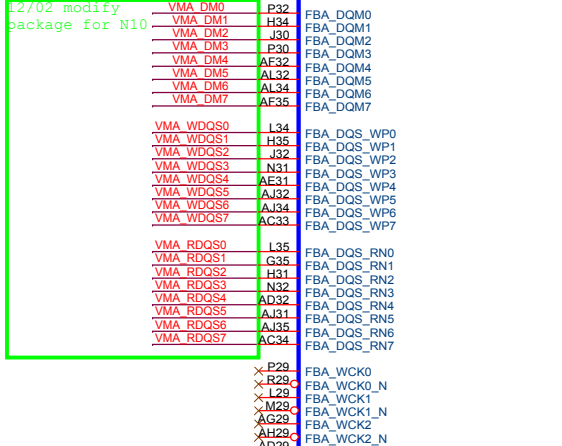
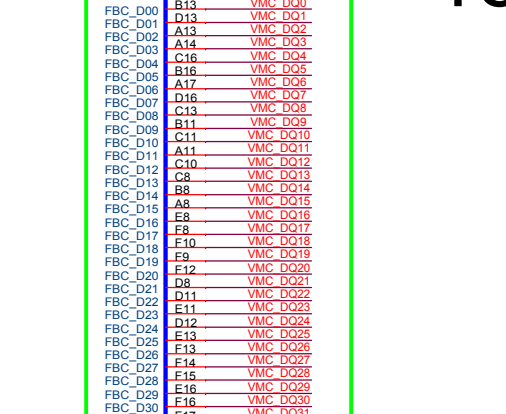
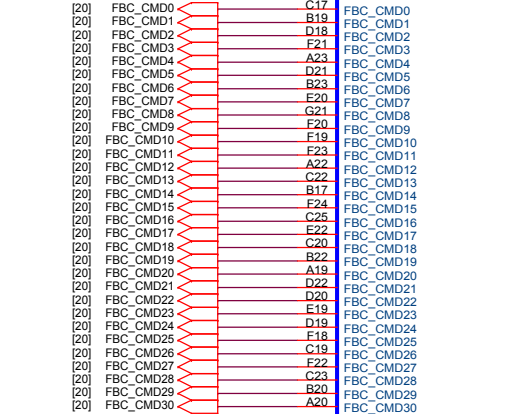
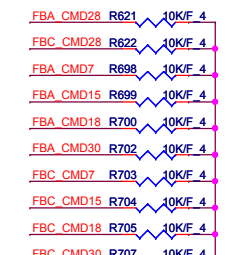
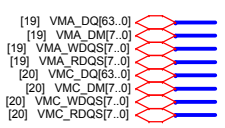
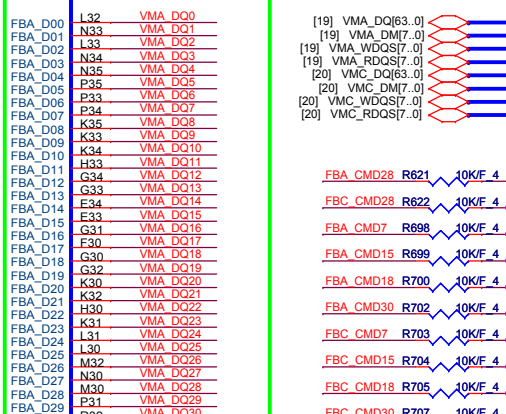
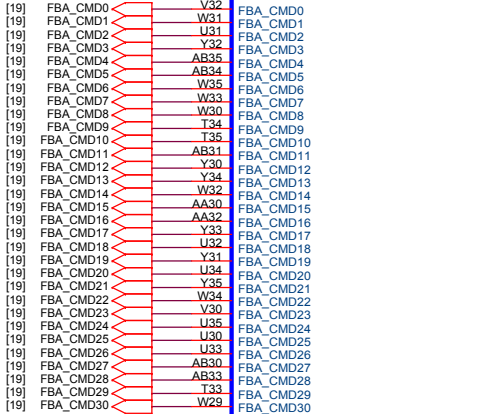
Date: Monday, October 26, 2009 | Sheet 14 of 45

U35B  
BG969-NVIDIA-NBSP-GS  
COMMON

12/02 modify  
package for N10

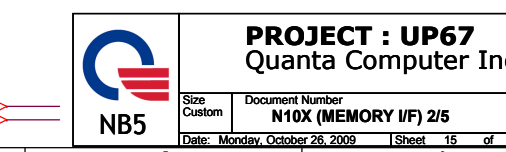
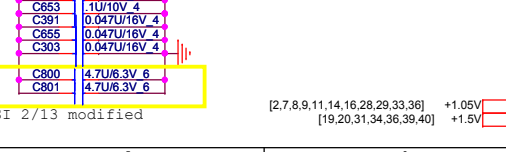
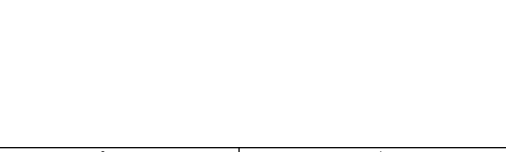
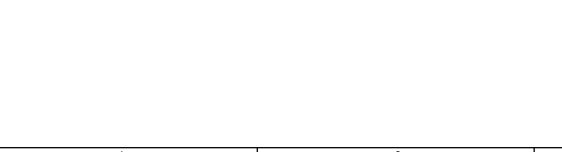
U35C  
BG969-NVIDIA-NBSP-GS  
COMMON

12/02 modify  
package for N10



MEMORY I/F A

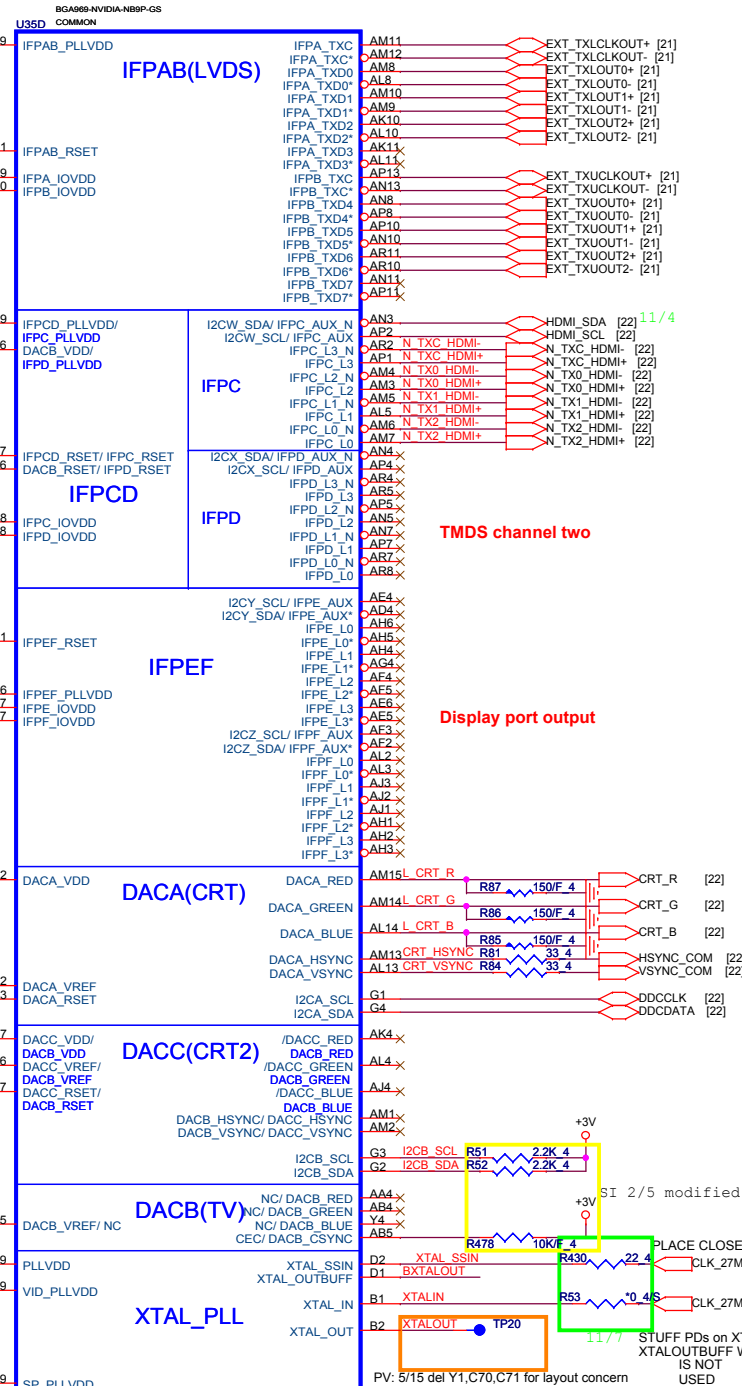
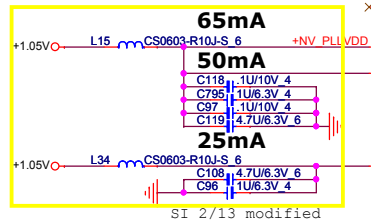
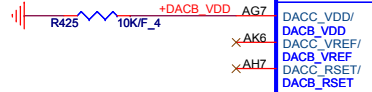
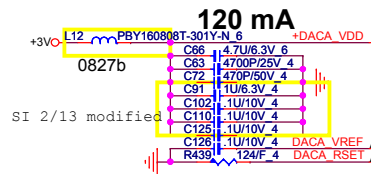
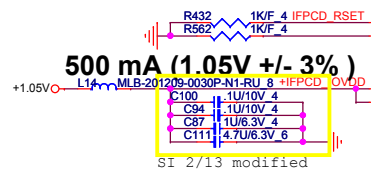
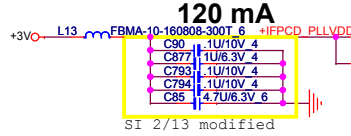
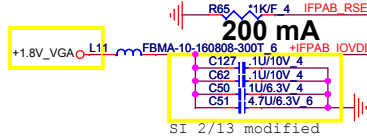
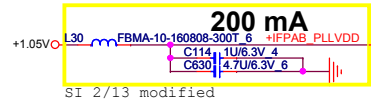
MEMORY I/F C



**PROJECT : UP67**  
Quanta Computer Inc.

Size Custom Document Number **N10X (MEMORY I/F) 2/5** Rev 1A

Date: Monday, October 26, 2009 | Sheet 15 of 45

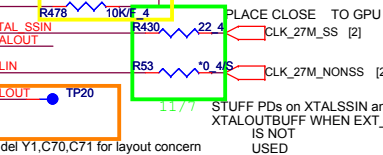


LVDS clk spread : Center +/-0.5% ( 30-33KHz)

TMDs channel two

Display port output

SI 2/5 modified



10 KΩ pull-down only if no spread chip used.

PV: 5/15 del Y1,C70,C71 for layout concern

[2,7,8,9,11,14,15,28,29,33,36] [5,10,11,33,36,40]

[2,3,7,8,9,10,11,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40]

**PROJECT : UP67**  
**Quanta Computer Inc.**

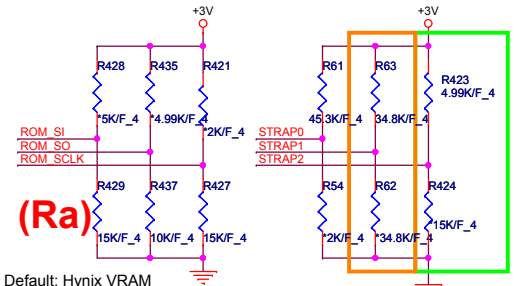
Size Custom Document Number **N10X (DISPLAY) 3/5** Rev 2A

Date: Monday, October 26, 2009 Sheet 16 of 45

SEE Datasheet for details on N10P Straps!

CHIP	PCI_DEVID:	STRAP2
N10P-GE	0x0A28	1000 PU 5K
N10M-GE	0x0A68	1000 PU 5K

PCI\_DEVID[4]/SUBVENDOR 1211 DEVICE ID CHANGE



### Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

```
CS31002PB26 (RES CHIP 10K 1/16W +-1% (0402))
CS31502PB08 (RES CHIP 15K 1/16W +-1% (0402))
CS32002PB02 (RES CHIP 20K 1/16W +-1% (0402))
```

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0		
ROM_SO	NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	USER[0]	1111

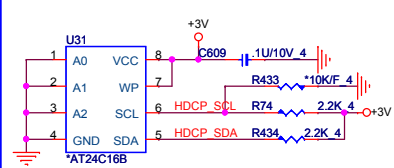
VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-EC12	PD 20K
0110		Reserved		
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

## GPIO ASSIGNMENTS

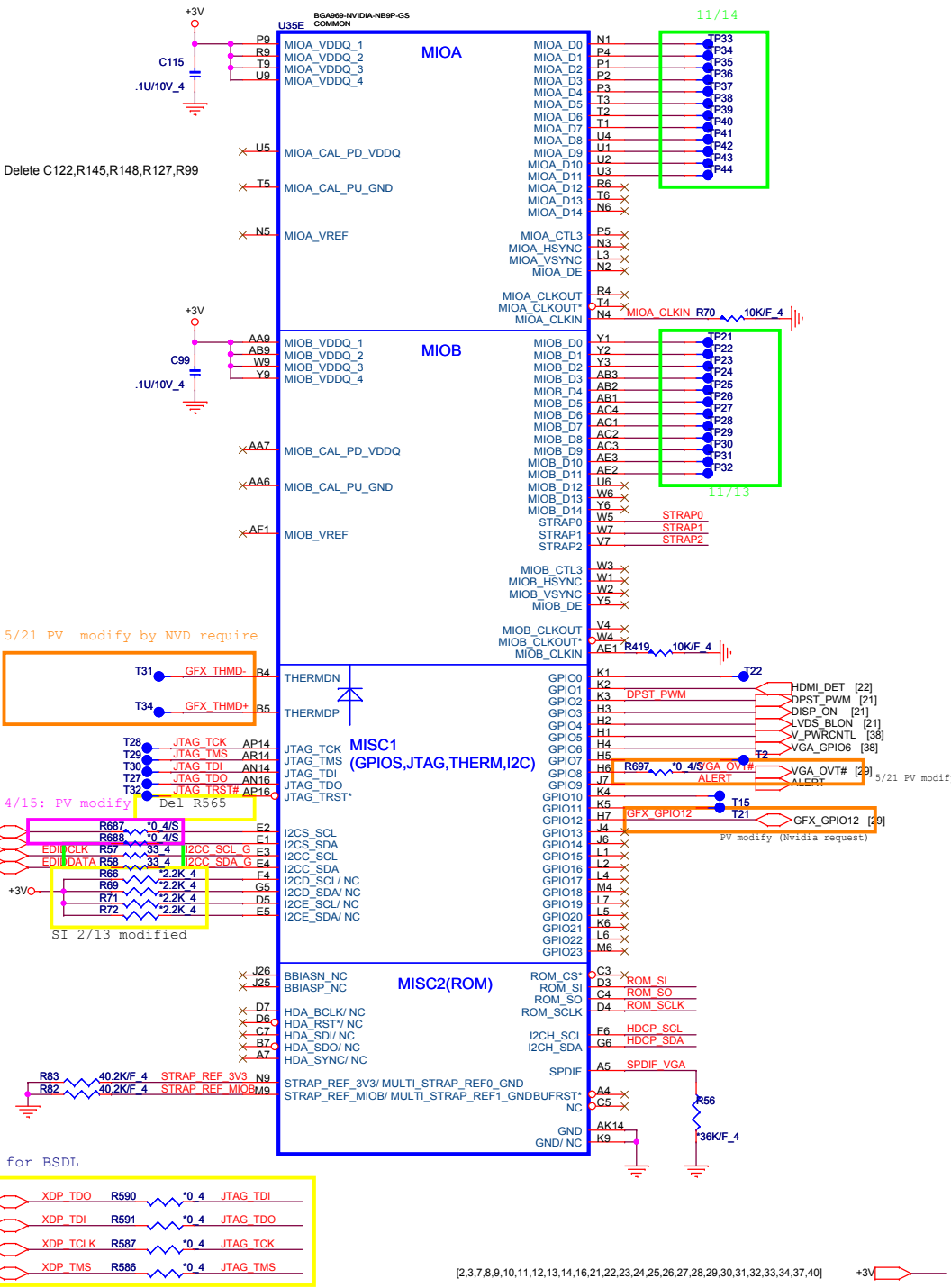
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

## HDCP ROM



Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

DHCP ROM	
HDCP_SCL	Low: Crypto ROM
	Hi: I2C ROM



Reserve for BSDL

XDP_TDO	XDP_TDO	R590	*0.4	JTAG TDI
XDP_TDI	XDP_TDI	R591	*0.4	JTAG TDO
XDP_TCLK	XDP_TCLK	R587	*0.4	JTAG TCK
XDP_TMS	XDP_TMS	R586	*0.4	JTAG TMS

[2,3,7,8,9,10,11,12,13,14,16,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40]

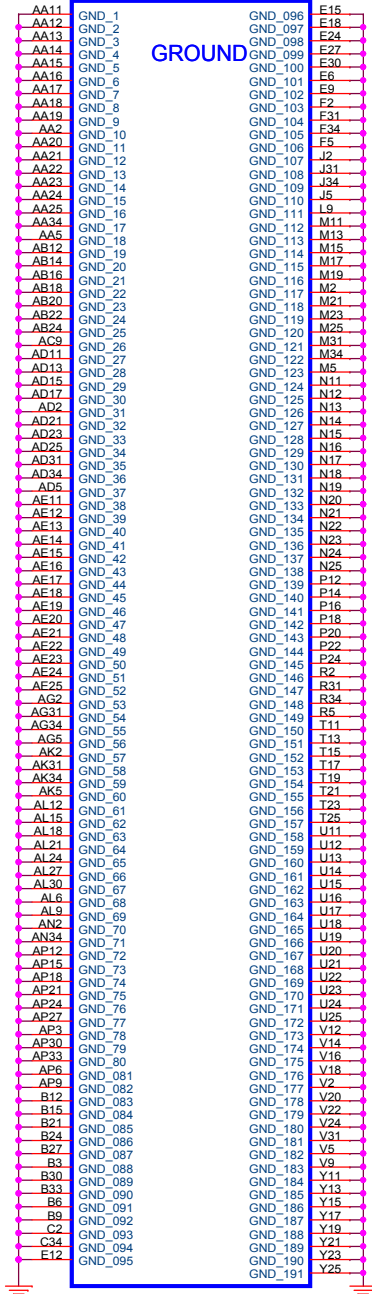
### PROJECT : UP67

### Quanta Computer Inc.

Size Custom	Document Number	Rev
	<b>N10X (GPIO &amp; STRAPS) 4/5</b>	2A
Date: Monday, October 26, 2009		Sheet 17 of 45

U35G

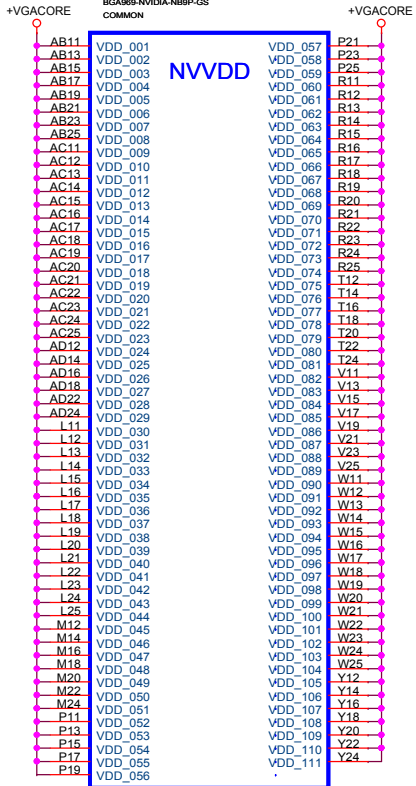
BGA969-NVidia-NB9P-GS  
COMMON



GROUND

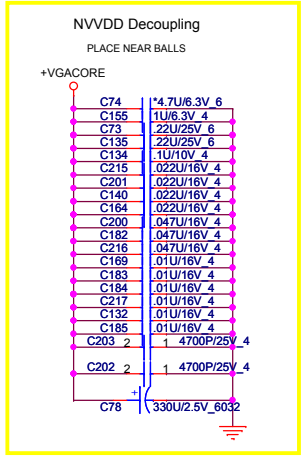
U35F

BGA969-NVidia-NB9P-GS  
COMMON



NVVDD

02/16 SI modify



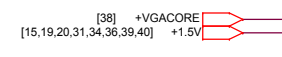
Del all VRAM termination (RP16~RP75)

SI 2/5 modified

**PROJECT : UP67**  
Quanta Computer Inc.

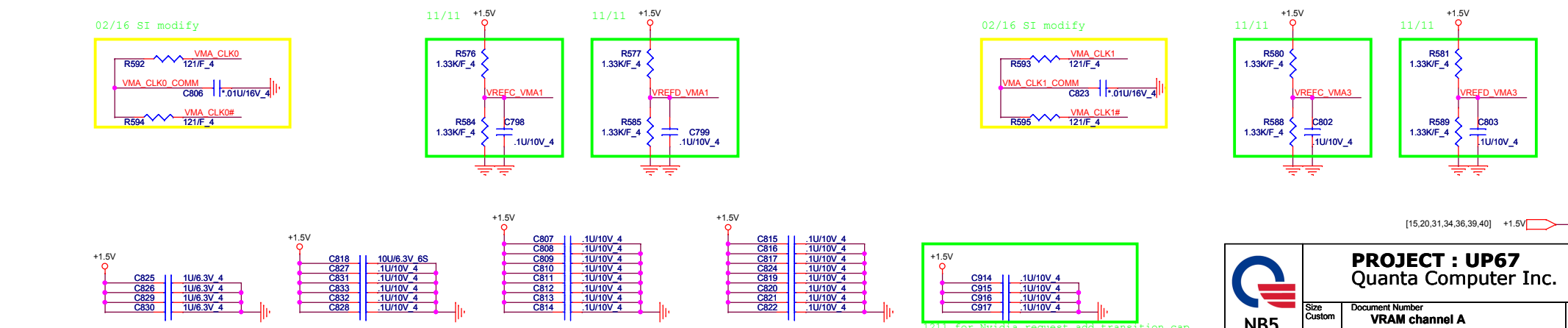
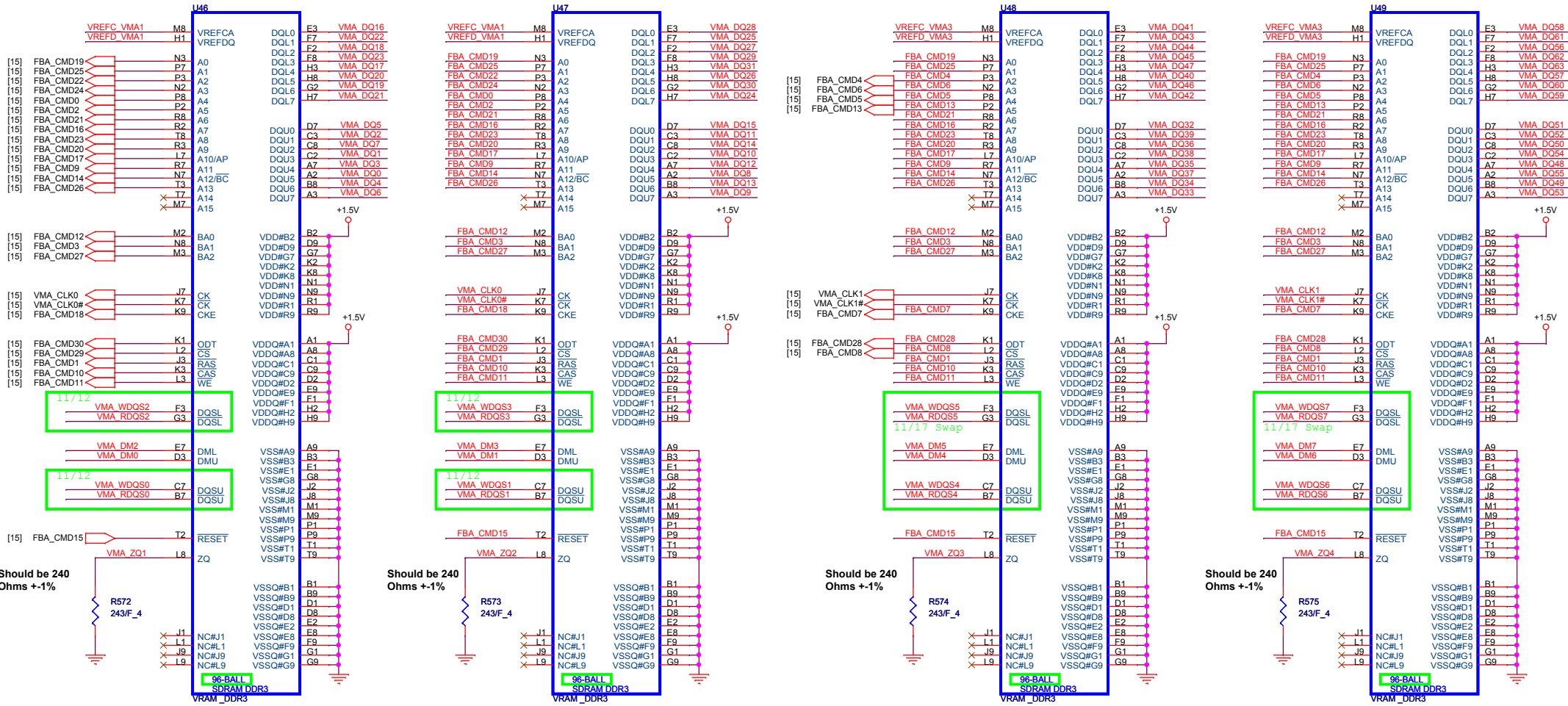
Size Custom Document Number **N10X (POWER & GND) 5/5** Rev 2A

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# CHANNEL A: 256MB/512MB DDR3



**NB5**

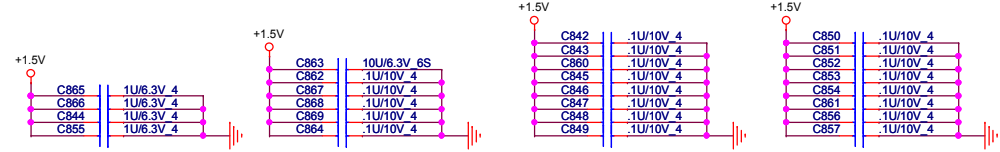
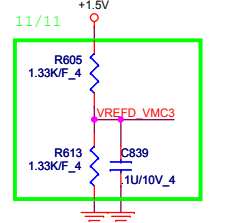
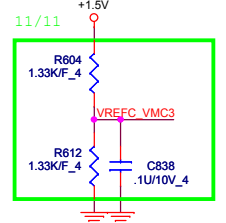
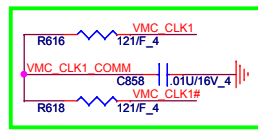
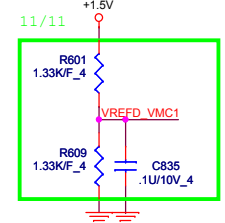
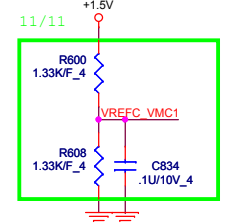
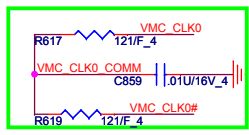
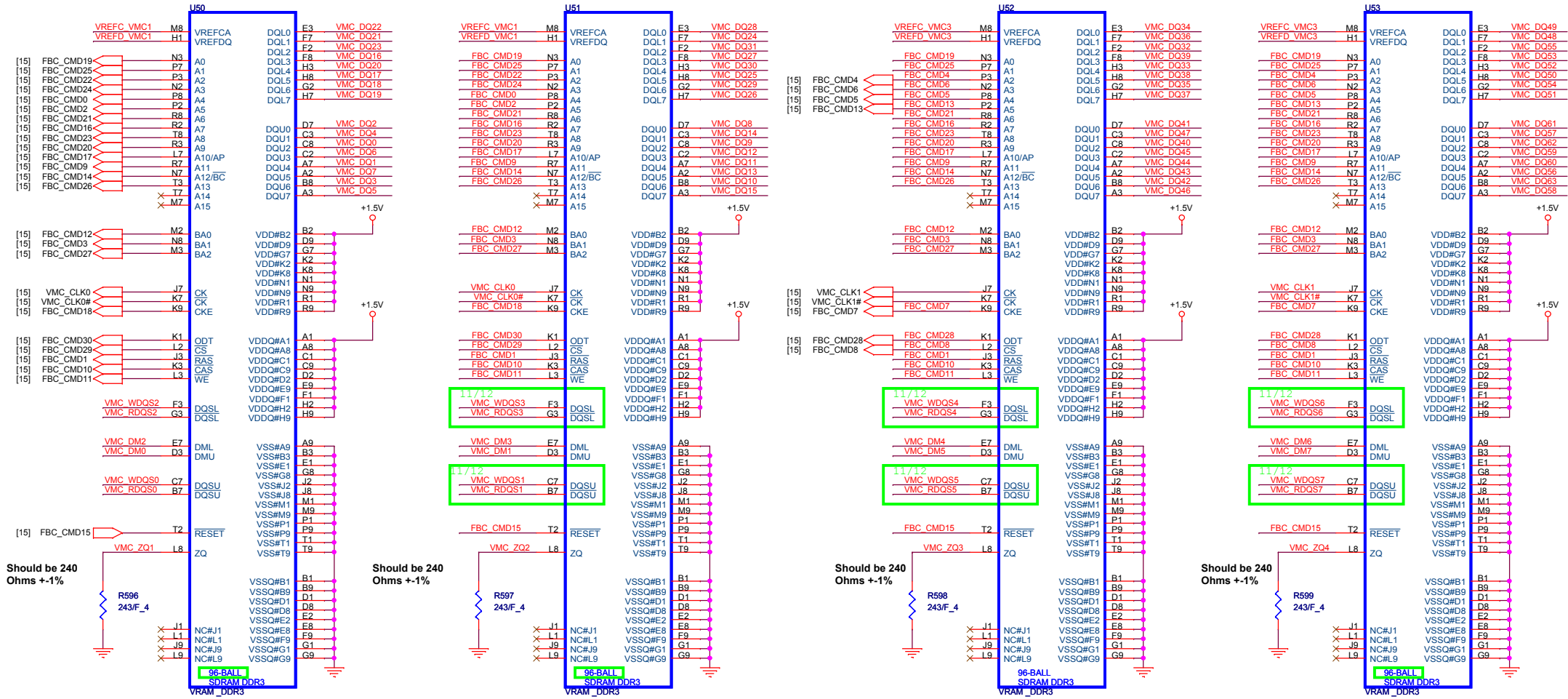
**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom	Document Number	Rev 1A
	<b>VRAM channel A</b>	
Date: Monday, October 26, 2009	Sheet 19	of 45

1211 for Nvidia request add transition cap

# CHANNEL B: 256MB/512MB DDR3

[15] VMC\_DQ[63..0]  
[15] VMC\_DM[7..0]  
[15] VMC\_WDQS[7..0]  
[15] VMC\_RDQS[7..0]

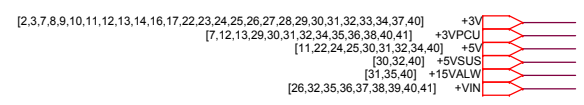
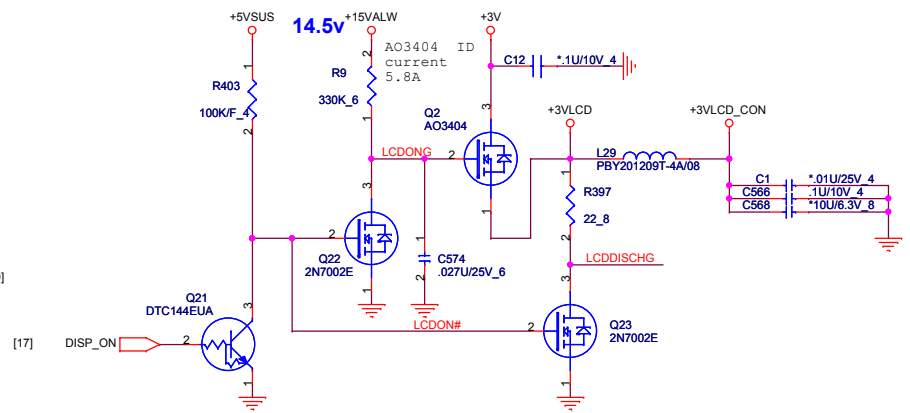
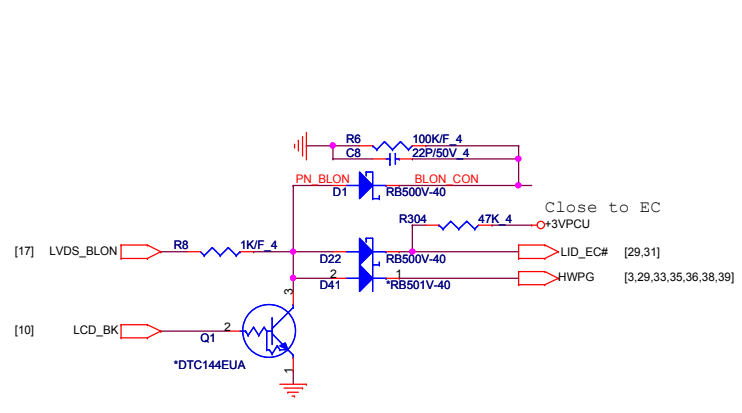
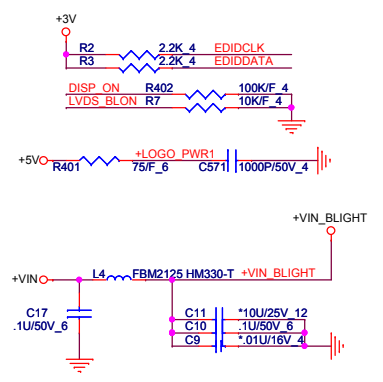
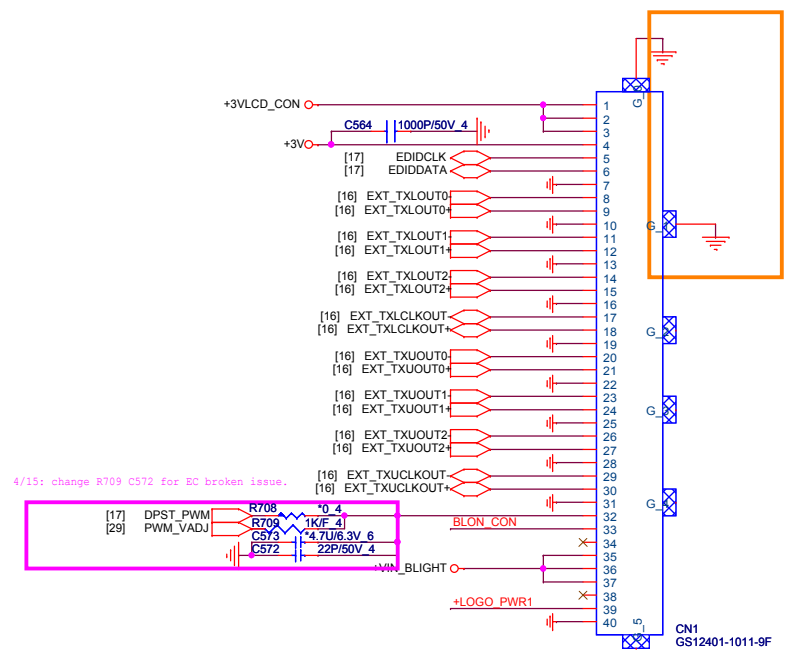


[15,19,31,34,36,39,40] +1.5V

**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>VRAM channel B</b>	Rev 1A
Date: Monday, October 26, 2009   Sheet 20 of 45		

5/20: change PIN 41, PIN42 to GND pad for EMI.



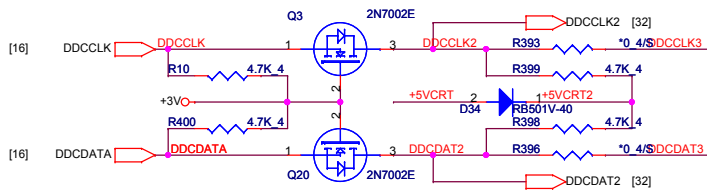
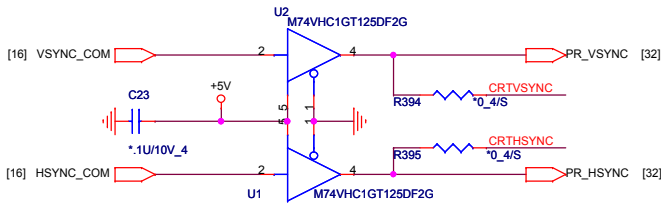
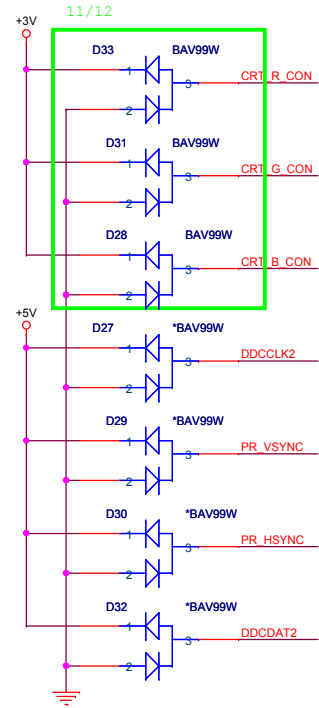
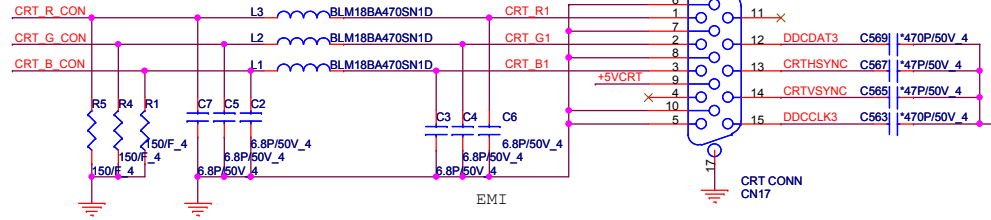
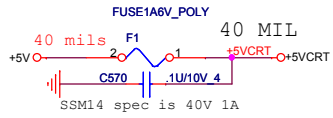
**PROJECT : UP67**  
Quanta Computer Inc.

Size Custom Document Number  
**LCD CONN/LID function**

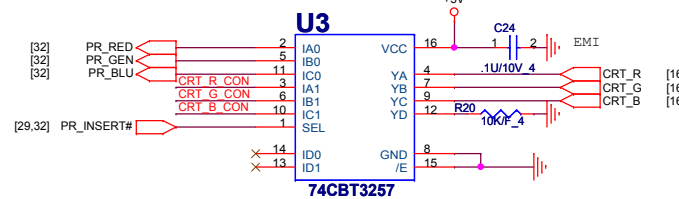
Date: Monday, October 26, 2009 Sheet 21 of 45

Rev 1A

### CRT PORT

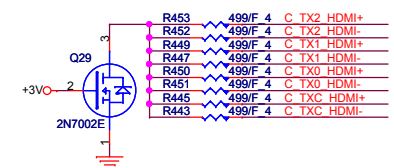
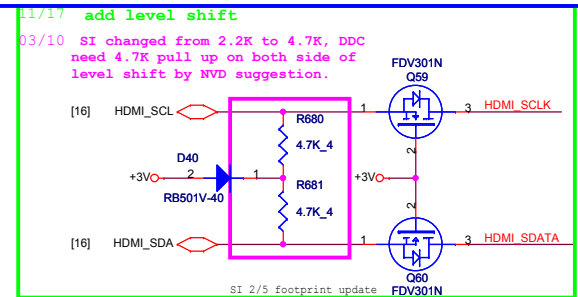
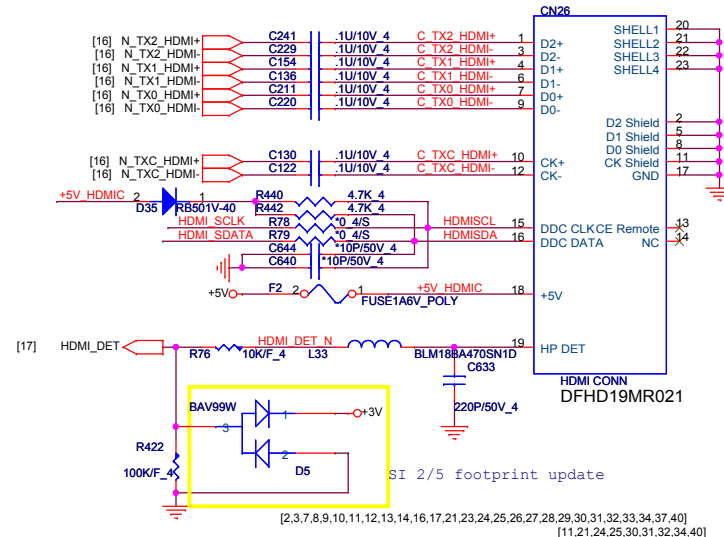


### CRT SWITCH



inputs	function
/E SET	
L L	Y - port 0
L H	Y - port 1
H X	Disconnect

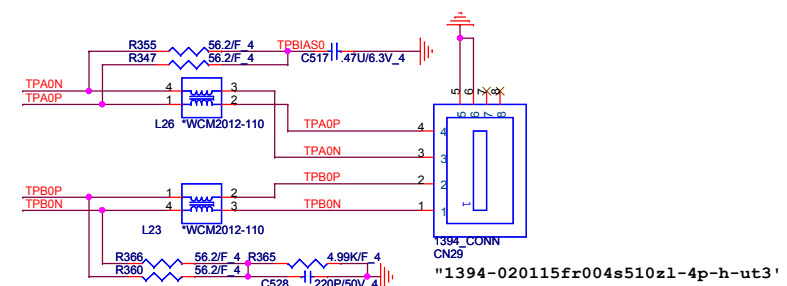
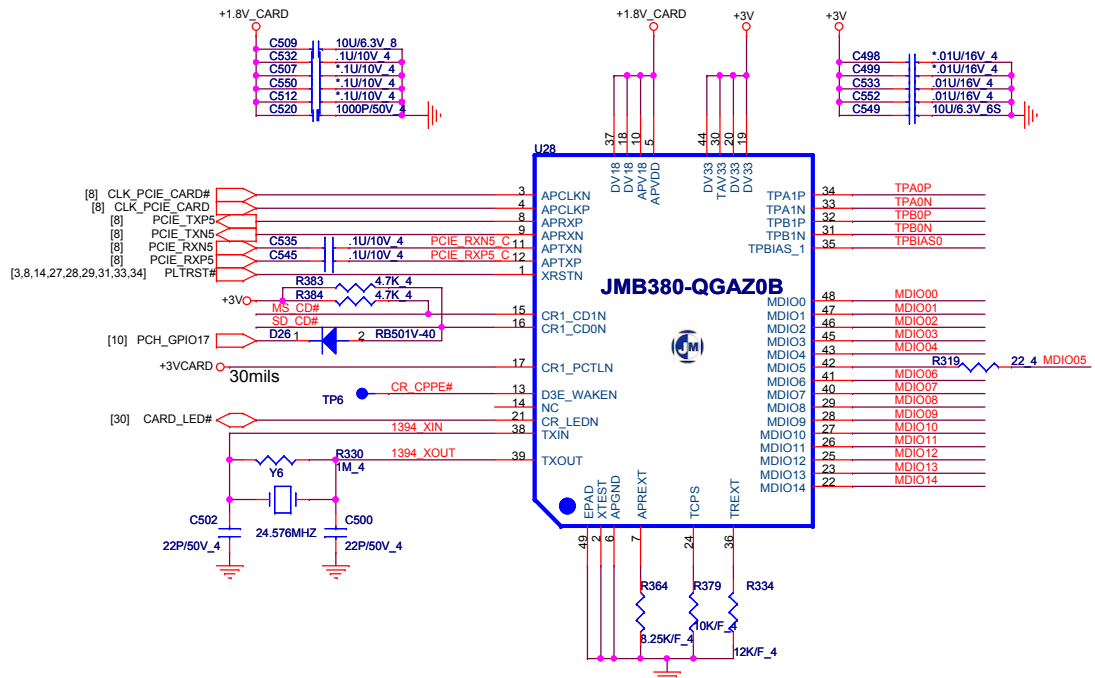
### HDMI PORT



**PROJECT : UP67**  
Quanta Computer Inc.

**NB5**

Size Custom	Document Number CRT/HDMI Conn	Rev 1A
Date: Monday, October 26, 2009		Sheet 22 of 45

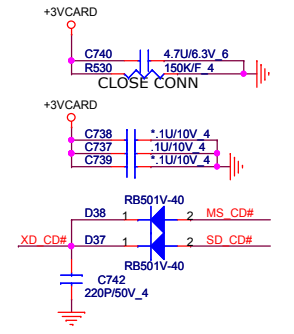
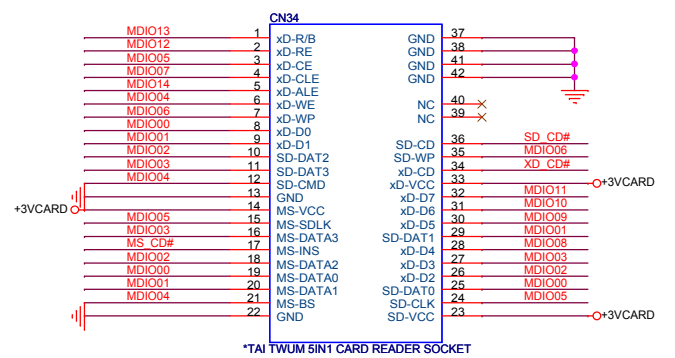
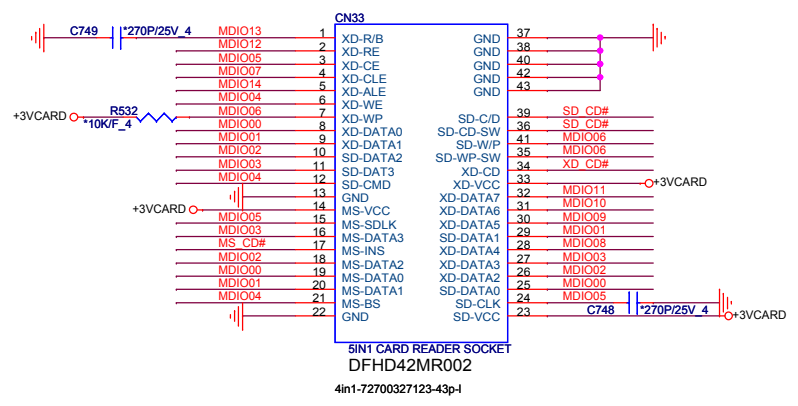


"1.394-020115fr004s510z1-4p-h-ut3"

**JMB 380 Note:**

SD/MMC	MS	XD
MDIO0	SD DAT0	MS D0
MDIO1	SD DAT1	MS D1
MDIO2	SD DAT2	MS D2
MDIO3	SD DAT3	MS D3
MDIO4	SD CMD	MS BS
MDIO5	SD CLK	MS SCLK
MDIO6	SD WP	XD WP#
MDIO7		XD CLE
MDIO8	SD DAT4	XD D4
MDIO9	SD DAT5	XD D5
MDIO10	SD DAT6	XD D6
MDIO11	SD DAT7	XD D7
MDIO12		XD RE#
MDIO13		XD RB#
MDIO14		XD LE
CR1_LEDN	SD1 LED#	MS1 LED#
CR1_PCTLN	SD1 PCTL#	MS1 PCTL#
CR1_CD0	SD1 CD#	MS1 CD#
CR1_CD1		MS1 CD#

**5 IN1 CARD READER  
XD, MMC/SD, MS/MSP**



**PROJECT : UP67**  
**Quanta Computer Inc.**

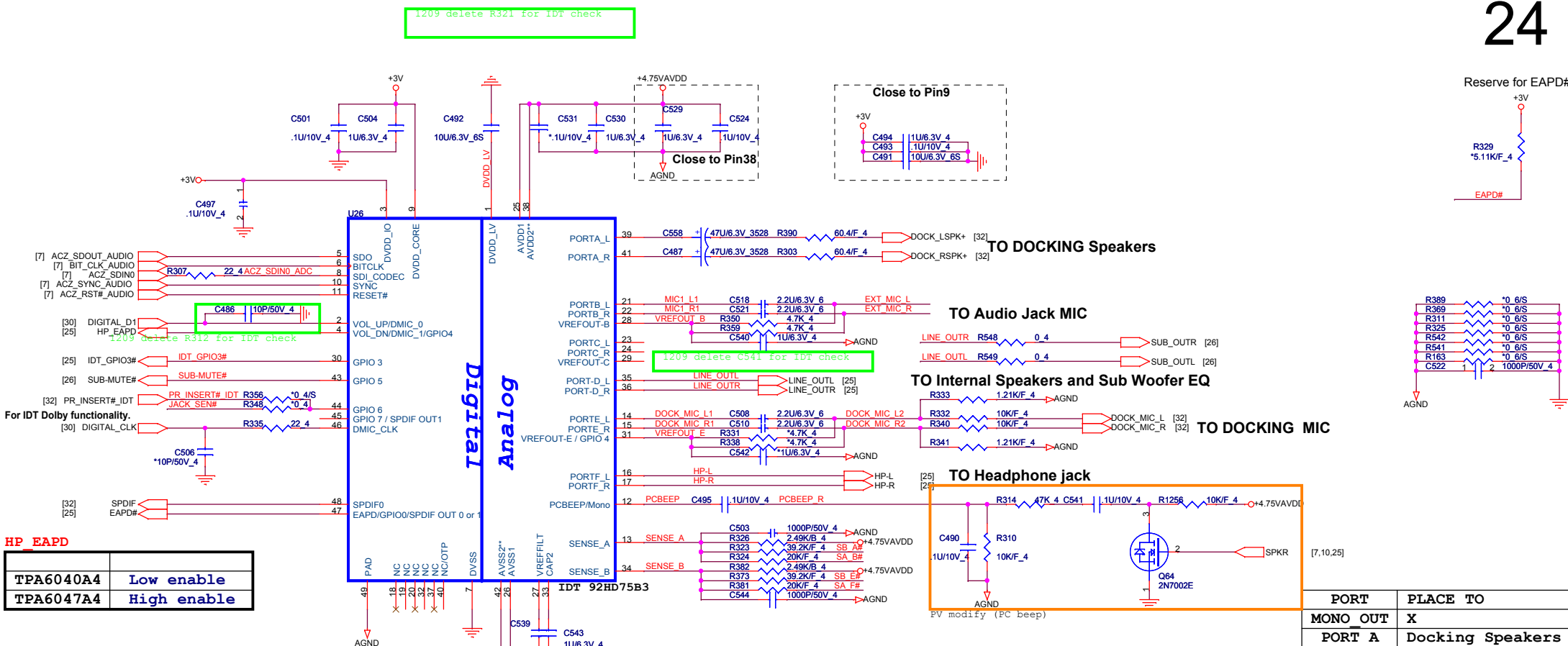
Size Custom Document Number  
**JMB380 & CR SOCKET**

Date: Monday, October 26, 2009 | Sheet 23 of 45

Rev 1A



Reserve for EAPD#



**HP\_EAPD**

TPA6040A4	Low enable
TPA6047A4	High enable

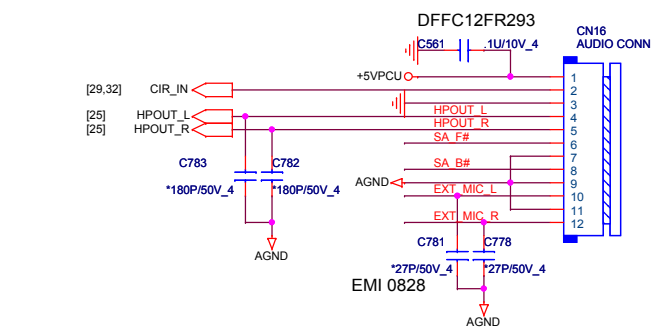
<b>Codec</b>	<b>92HD71</b>	<b>92HD75</b>
R571	POP	NA
C716	NA	POP
R449 R510	5.11K	2.49K

5.11K P/N: CS25112FB15

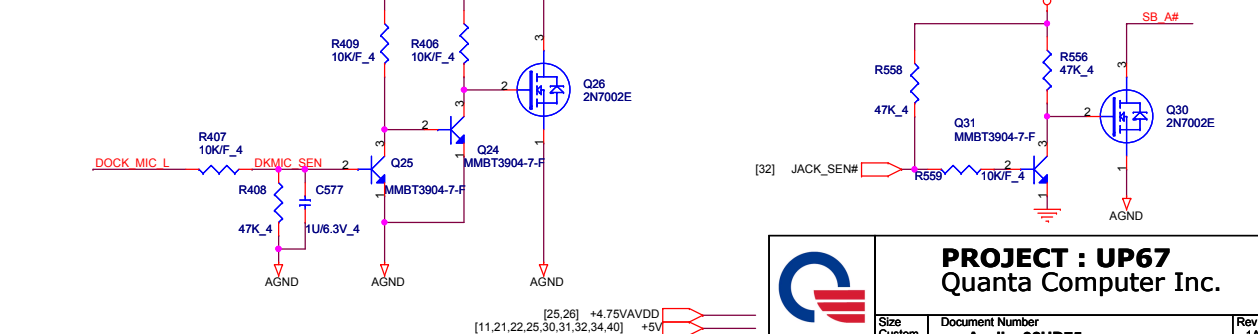
PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC

SA\_A# -->DOCK HP  
 SA\_B# -->EXT MIC  
 SB\_E# -->DOCK MIC  
 SA\_F# -->EXT HP  
 Audio JACK: Normal Open

## TO AUDIO/B CON.



## DOCK MIC DETECT

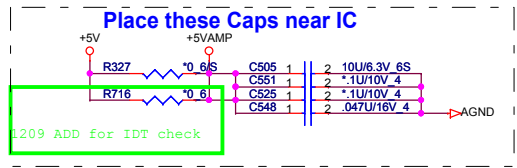
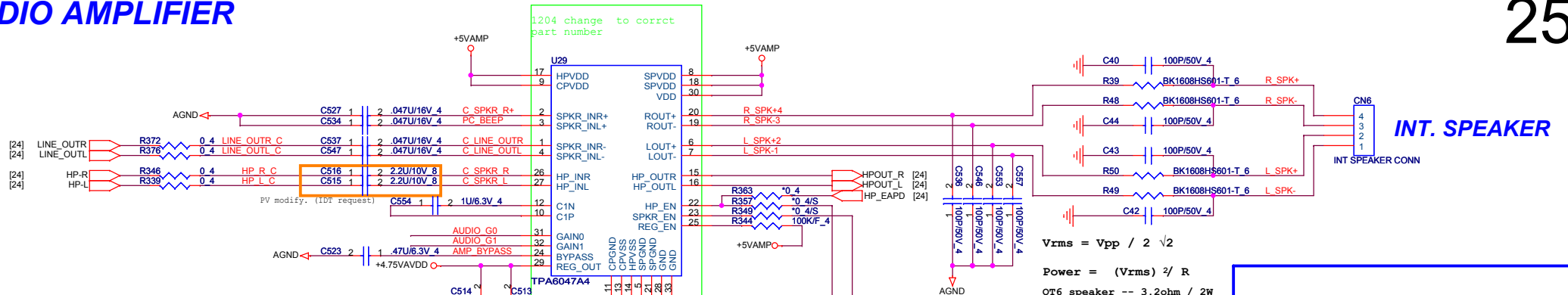


**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>Azalia 92HD75</b>	Rev 1A
Date: Monday, October 26, 2009		Sheet 24 of 45

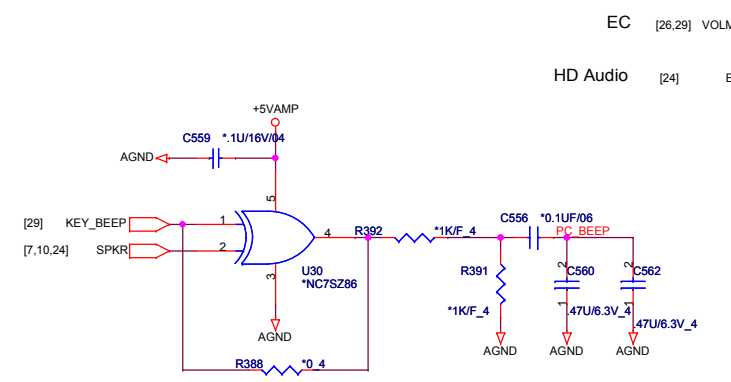
[11,21,22,25,30,31,32,34,40] +5V  
 [12,25,29,31,35,36,37,38,39,40] +5VPCU  
 [2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,25,26,27,28,29,30,31,32,33,34,37,40] +3V

# AUDIO AMPLIFIER



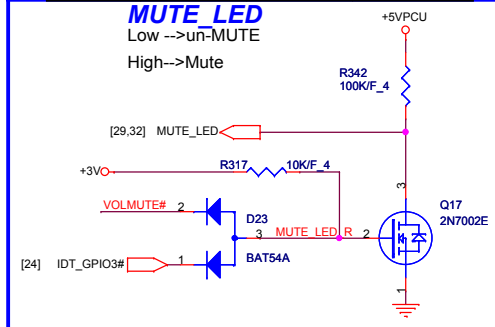
**6040A Gain Table**

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K



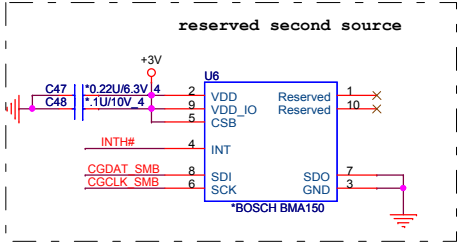
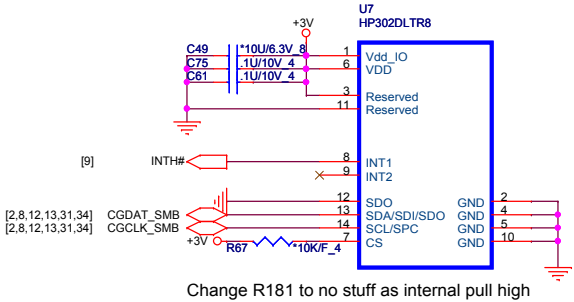
**PIN23 SPKR\_EN**

TPA6040A4	Low enable
TPA6047A4	High enable

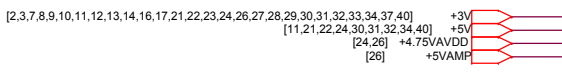


## Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi, BIOS need to programming 22h to change status from active Hi to low



Pin 12: Low 38hex  
Pin 12: unconnected/floating 3Ahex

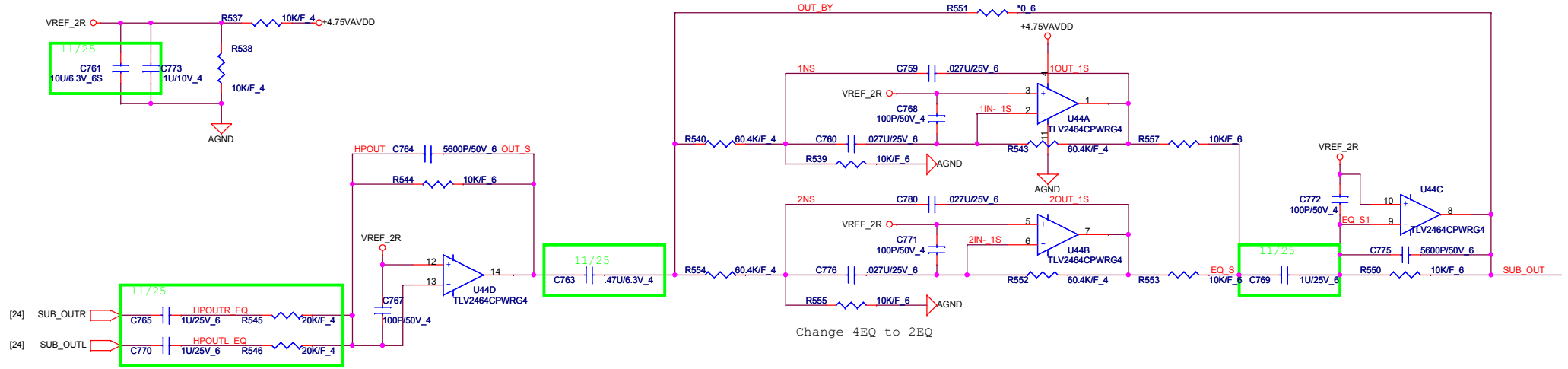


**PROJECT : UP67**  
Quanta Computer Inc.

Size Custom Document Number AMP\_TPA6047/Accelerometer Rev 1A

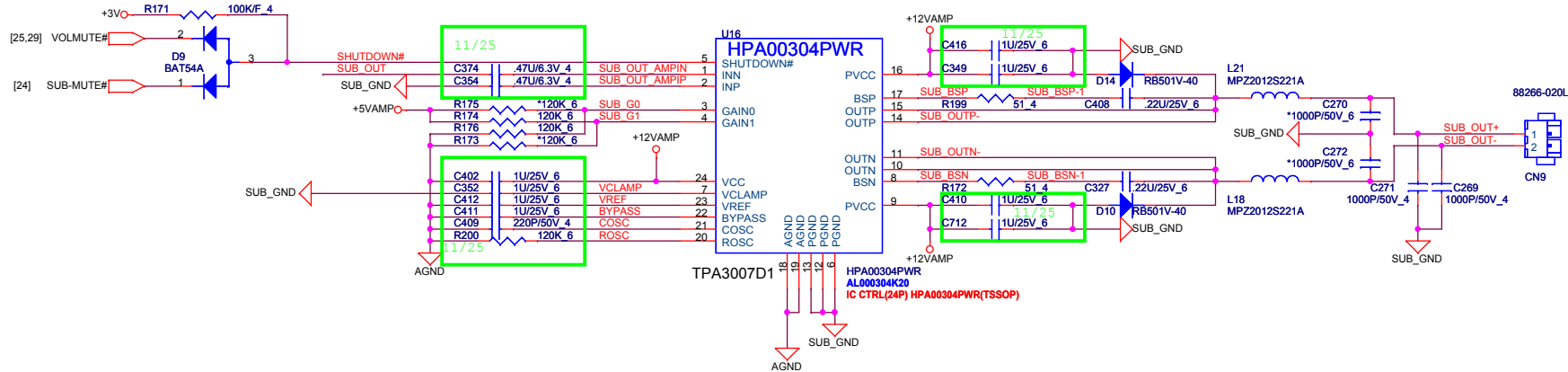
Date: Monday, October 26, 2009 | Sheet 25 of 45

# EQ FOR SUBWOOFER



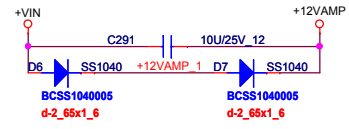
MODEL	UP7
R316	60.4K/F_6
R319	60.4K/F_6
R330	60.4K/F_6
R314	60.4K/F_6
C509	0.027U/25V_6
C510	0.027U/25V_6
C529	0.027U/25V_6
C543	0.027U/25V_6

Change 4EQ to 2EQ



## Sub-Woofer power

GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

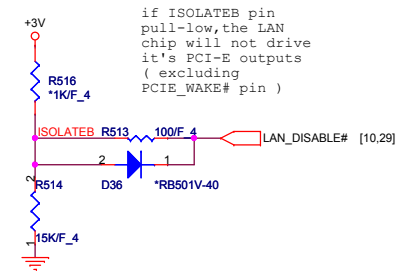
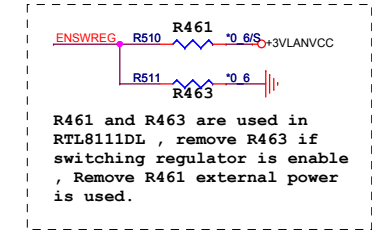
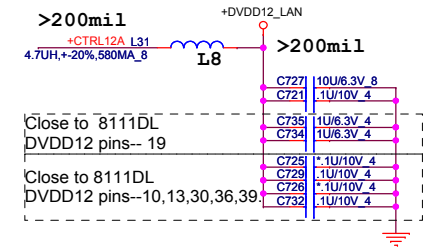
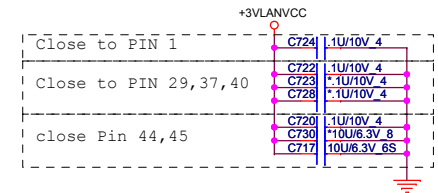
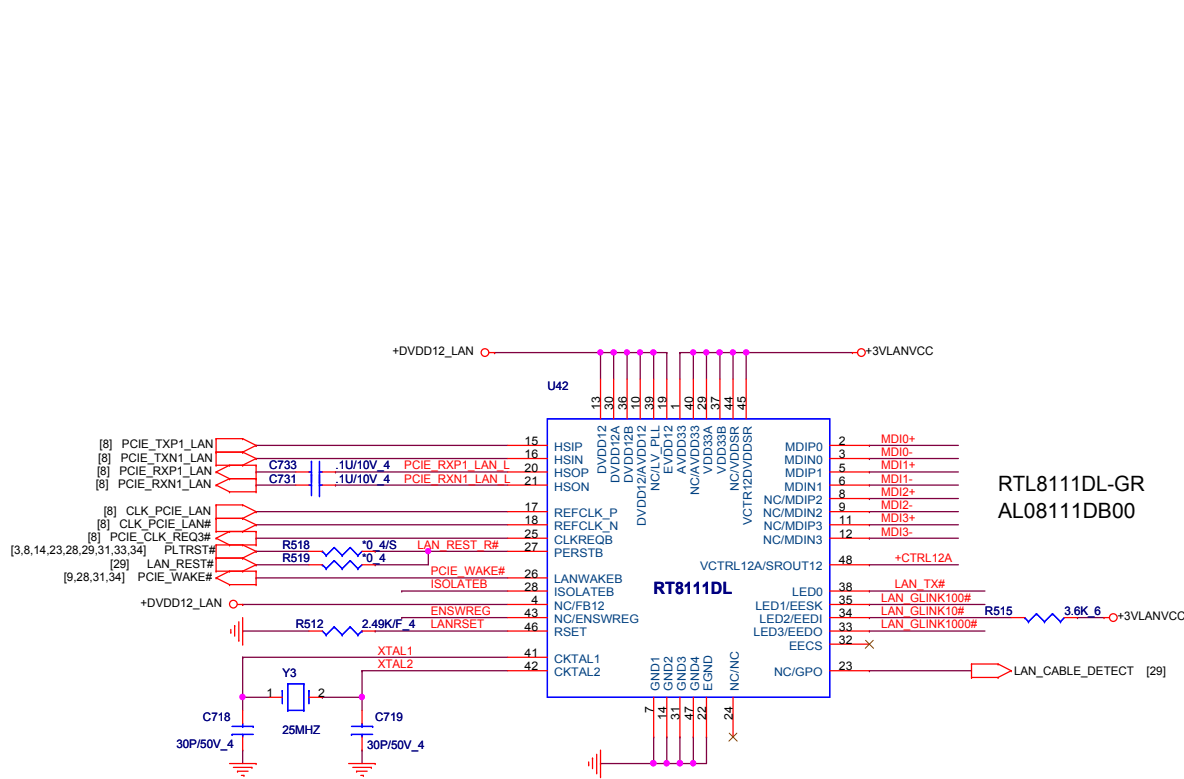


[25] +4.75VAVDD  
 [25] +5VAMP  
 [21,32,35,36,37,38,39,40,41] +VIN  
 [2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,27,28,29,30,31,32,33,34,37,40] +3V

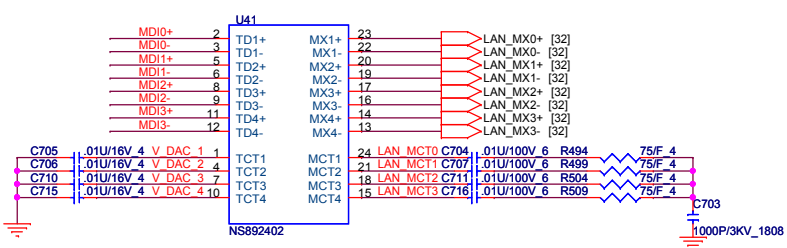
**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom    Document Number **SUBWOOFER (EQ & AMP.)**    Rev 1A

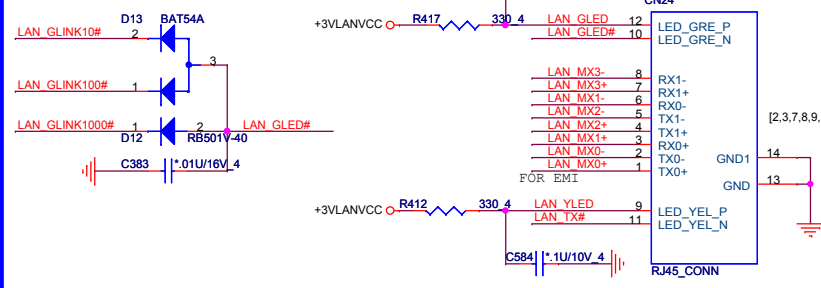
Date: Monday, October 26, 2009    Sheet 26 of 45



**Transformer for 10/100/1000**



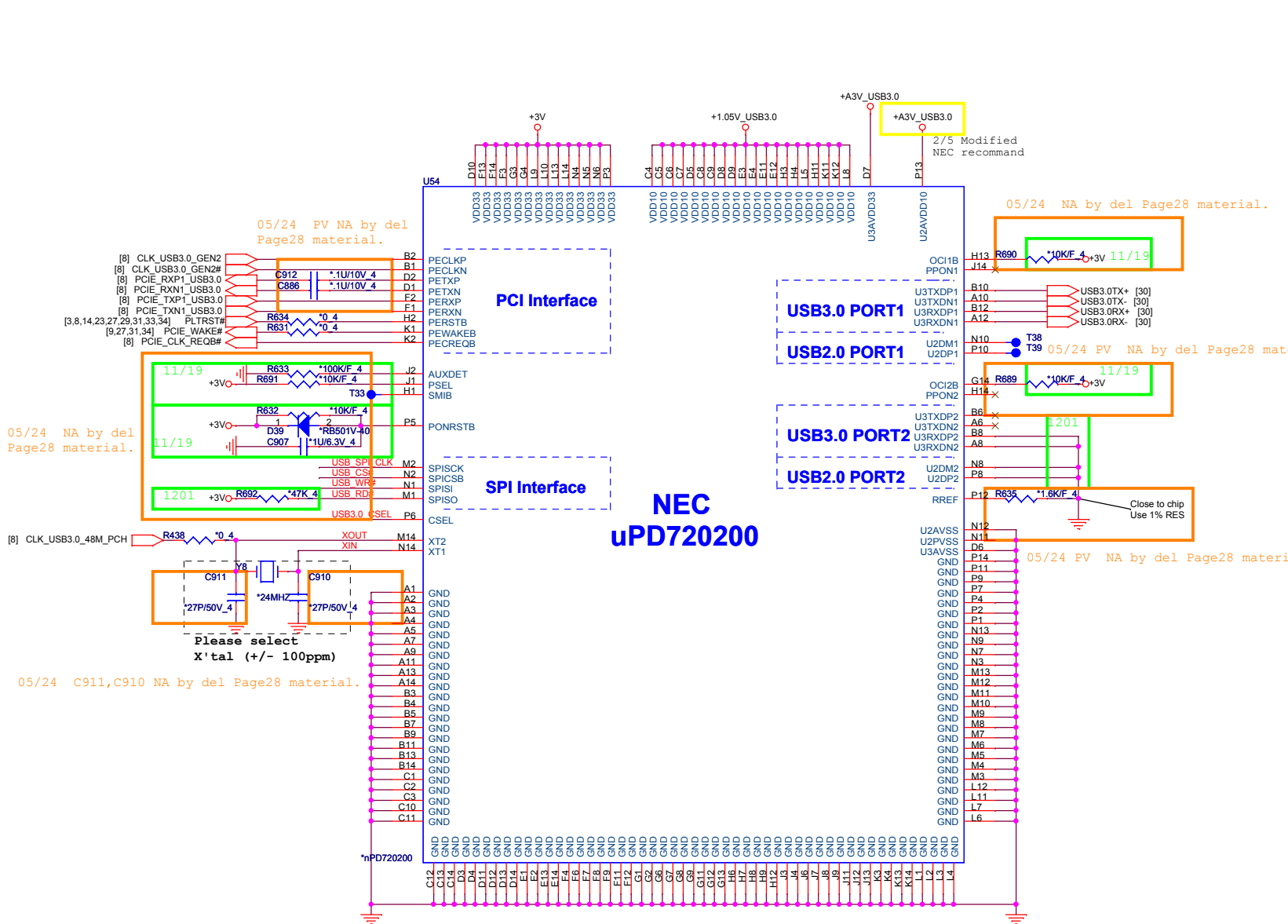
**Lan Con.**



**PROJECT : UP67**  
Quanta Computer Inc.

Size Custom Document Number  
**RTL8111DL/8103E/RJ45** Rev 1A

Date: Monday, October 26, 2009 | Sheet 27 of 45



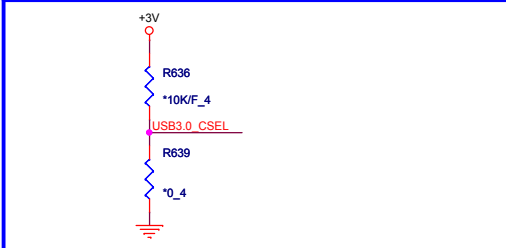
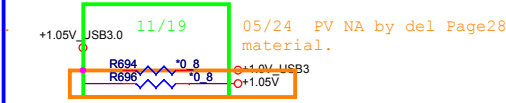
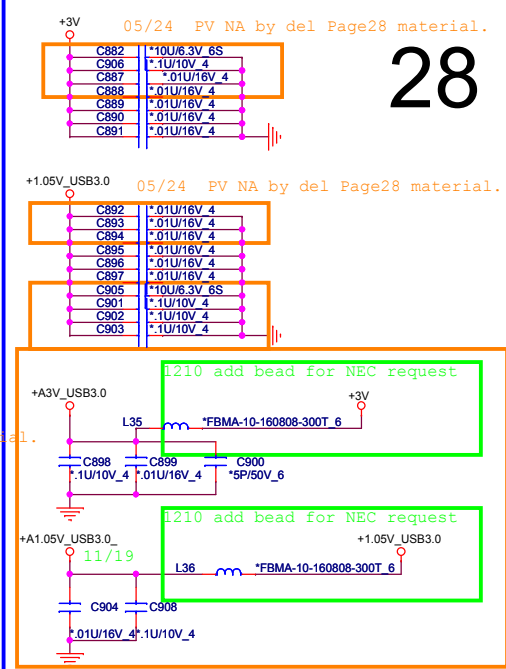
05/24 PV NA by del Page28 material.

05/24 NA by del Page28 material.

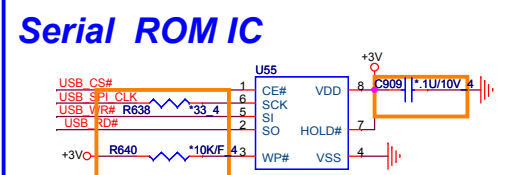
05/24 NA by del Page28 material.

05/24 C911,C910 NA by del Page28 material.

05/24 PV NA by del Page28 material.



Clock select signal	
USB3.0_CSEL	High = External 48Mhz
	Low = 24MHz X'tal

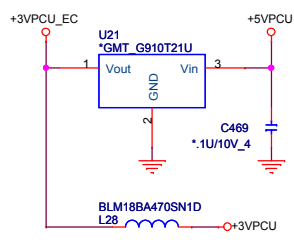
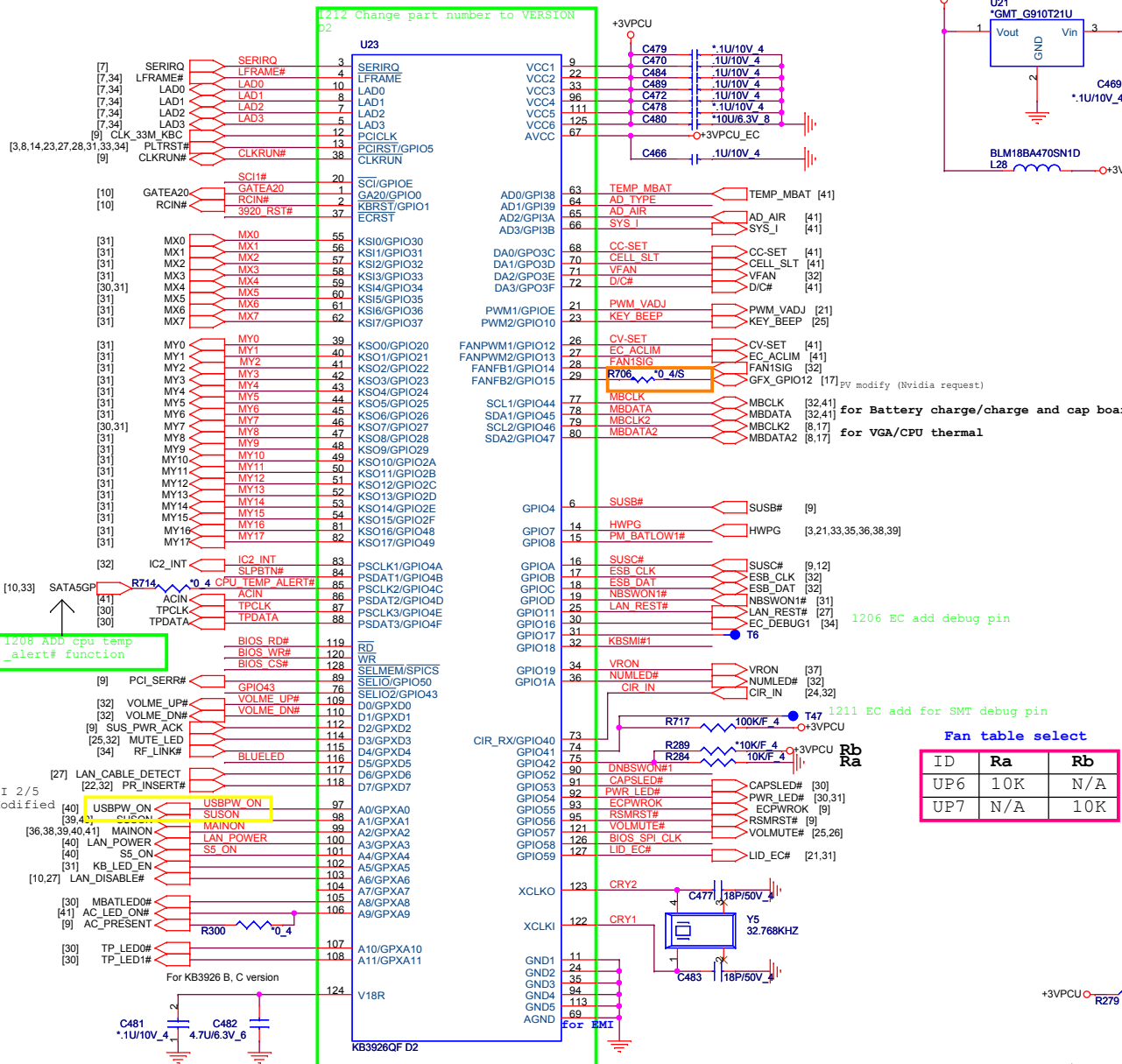


NEC recommends to use serial ROM IC "AT25Fxxx Series"

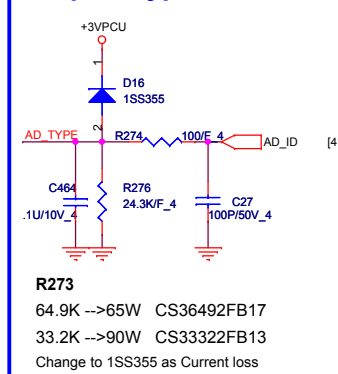
**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>NEC USB3.0 nPD720200</b>	Rev 1A
Date: Monday, October 26, 2009   Sheet 28 of 45		

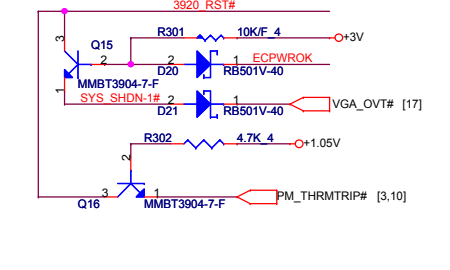




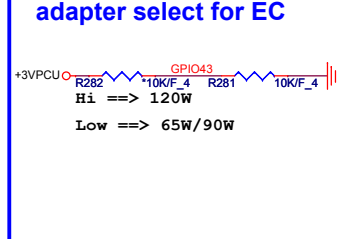
## adapter Type check



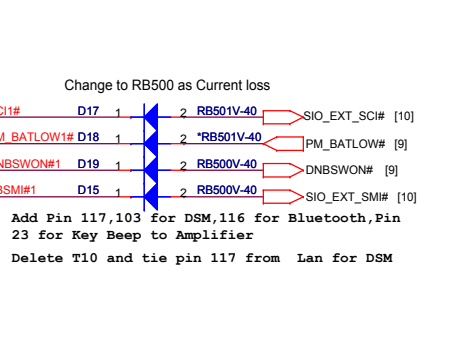
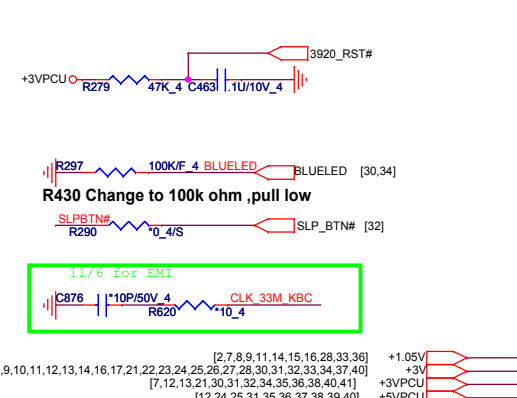
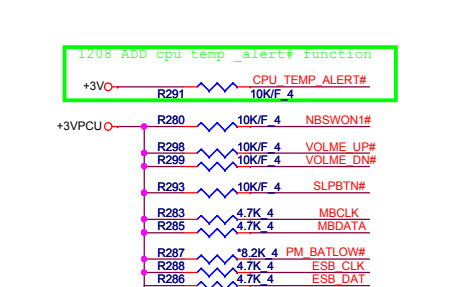
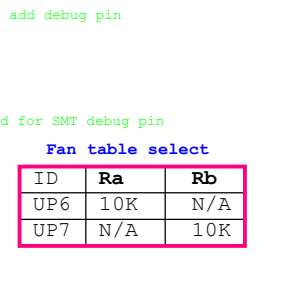
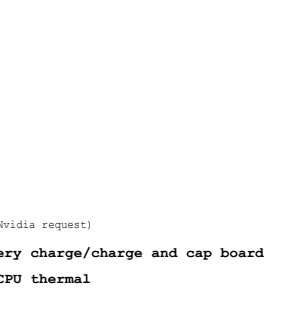
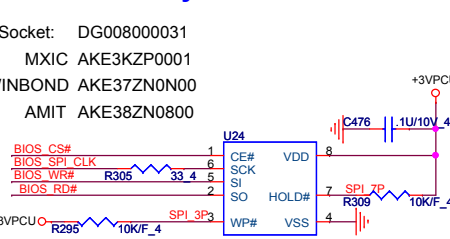
## thermal shutdown circuit



## adapter select for EC



## 512K byte SPI EC ROM



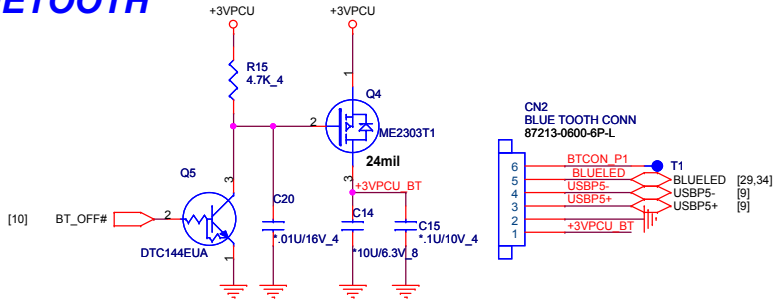
**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom Document Number **KB3926/ROM/TP** Rev 1A

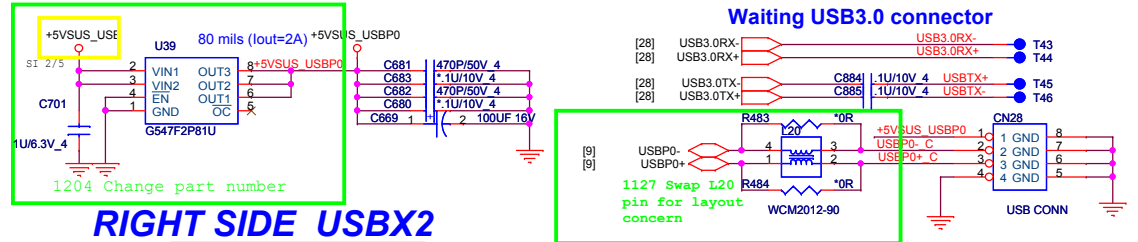
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[2,7,8,9,11,14,15,16,28,33,36] +1.05V  
 [2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,30,31,32,33,34,37,40] +3V  
 [7,12,13,21,30,31,32,34,35,36,38,40,41] +3VPCU  
 [12,24,25,31,35,36,37,38,39,40] +5VPCU

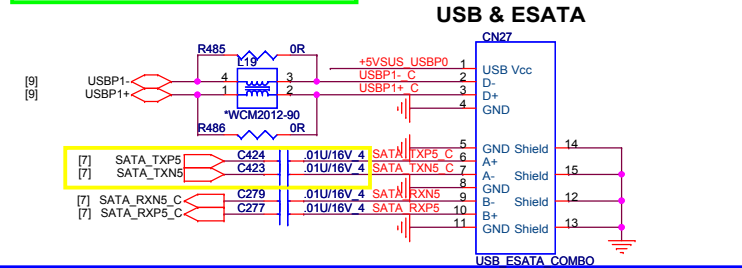
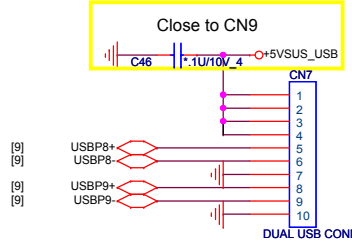
**BLUETOOTH**



**LEFT SIDE USBX1 and E-SATA/USB COMBO**

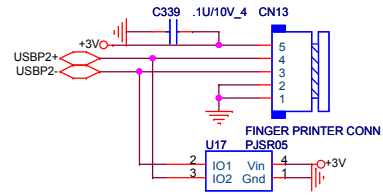


**RIGHT SIDE USBX2**



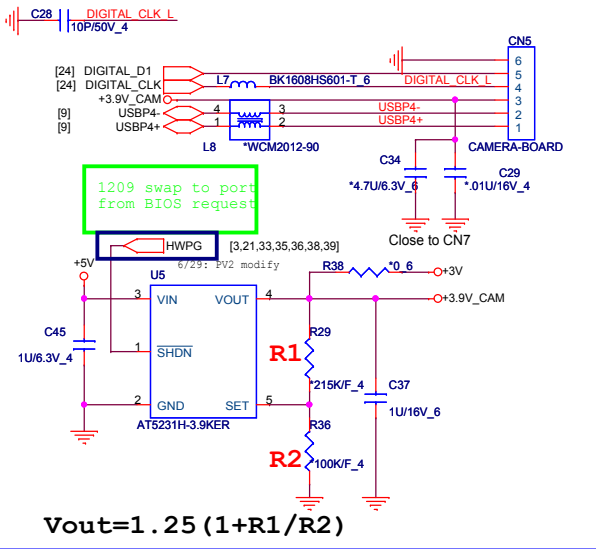
**USB fingerprint CON**

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

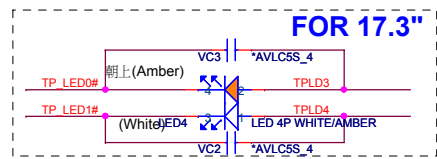
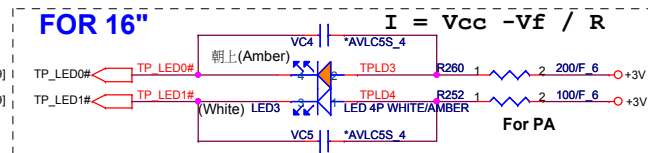
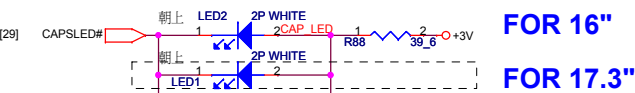
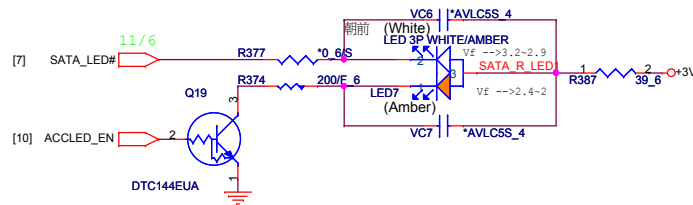


**USB CAMERA /DIGITAL MIC CONNECT**

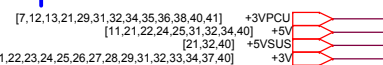
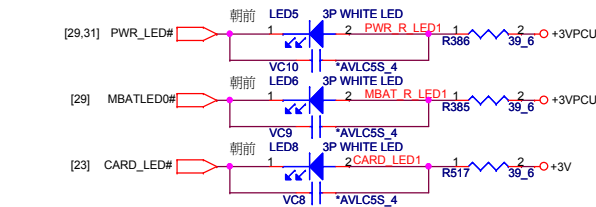
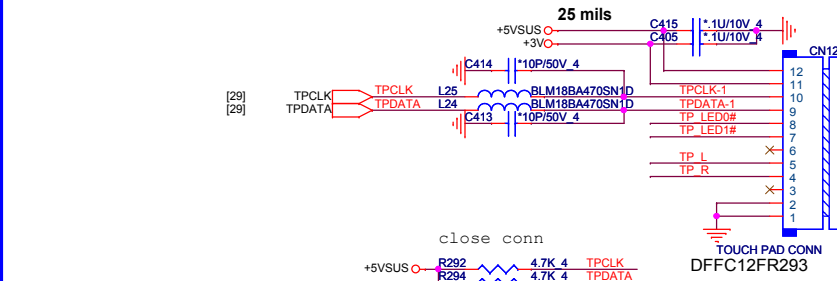
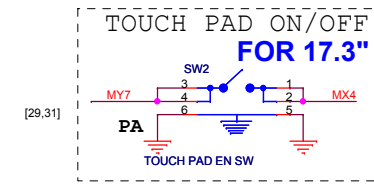
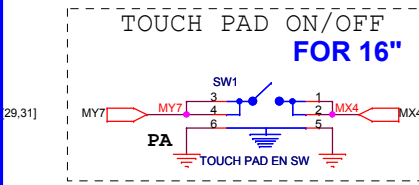
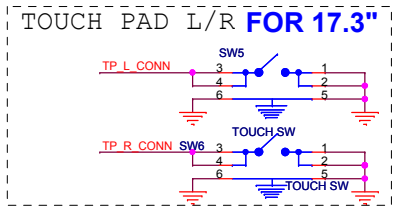
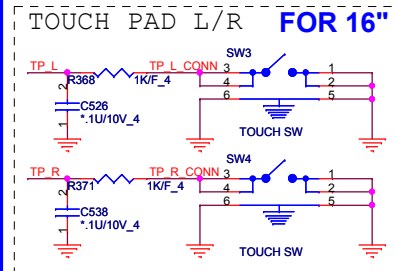
Add for EMI solution



**LED**



**TOUCH PAD CONNECTOR & ON/OFF BOTTOM**

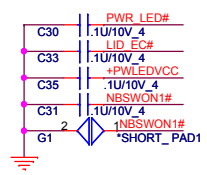
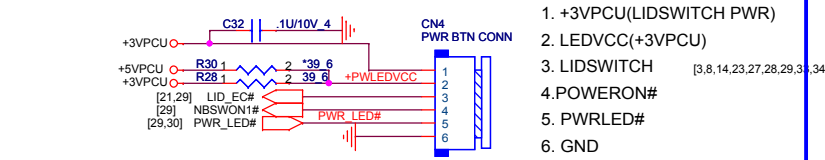


**PROJECT : UP67**  
**Quanta Computer Inc.**

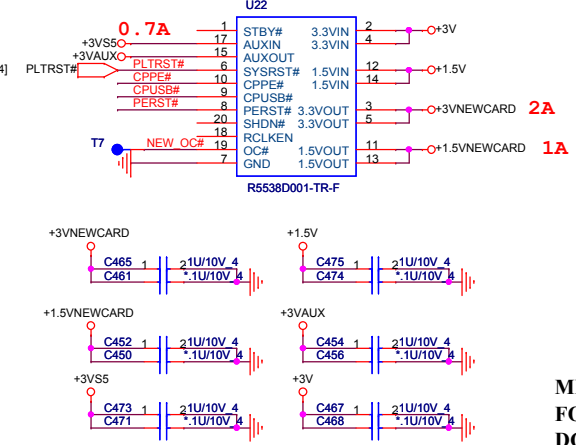
Size: Custom    Document Number: **BT/WCF/ESATA/USB/LED**    Rev: 1A

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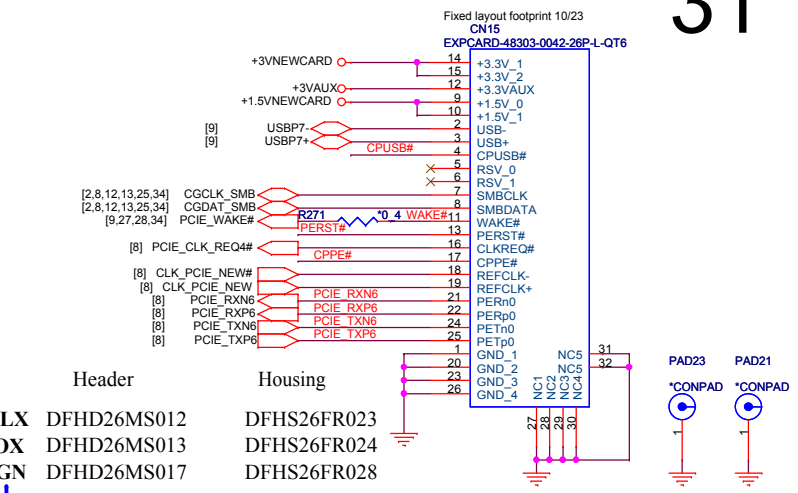
# POWER BOTTON CONNECT



# NEWCARD

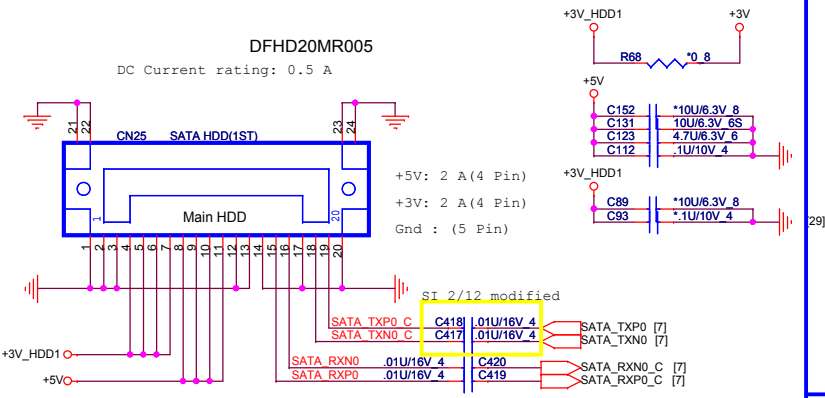


# NEWCARD (PCIEXPRESS\*1 + USB\*1)

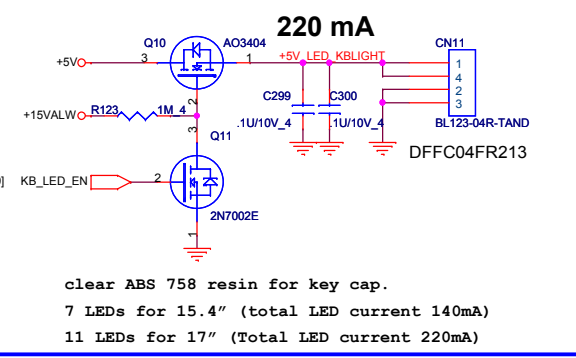


31

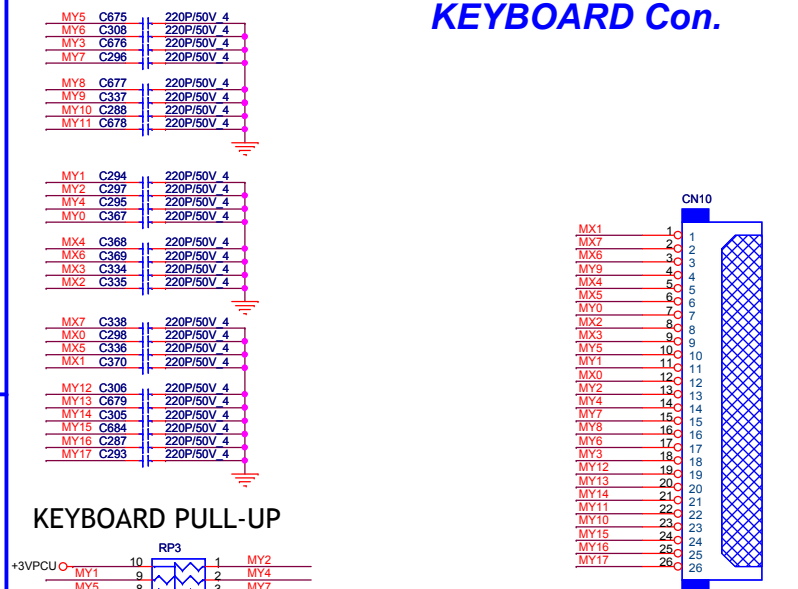
# SATA HDD CONNECTOR



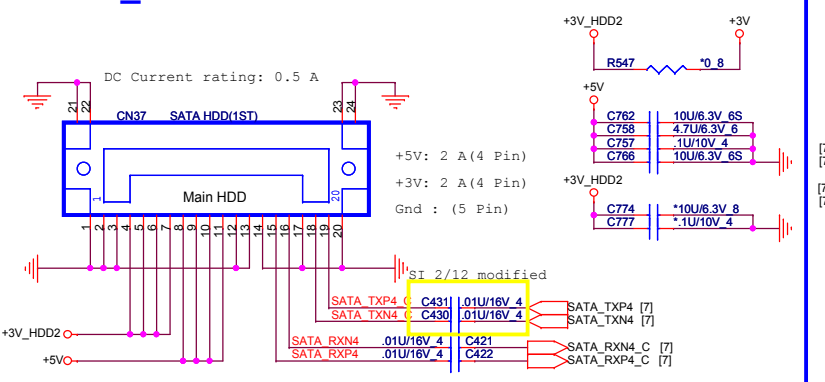
# Backlight Keyboard Con.



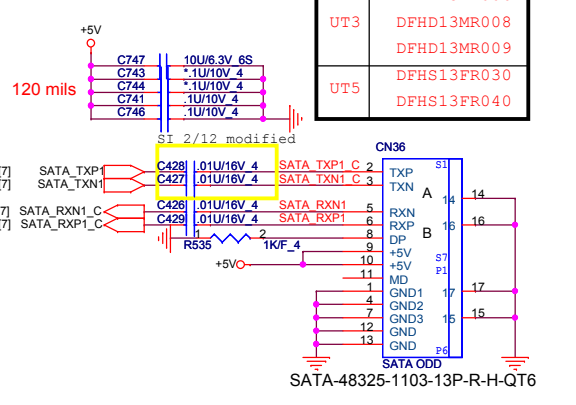
# KEYBOARD Con.



# SATA\_2 CONNECTOR



# SATA CD-ROM



UT3	DFHD13MR006
	DFHD13MR008
	DFHD13MR009
UT5	DFHS13FR030
	DFHS13FR040

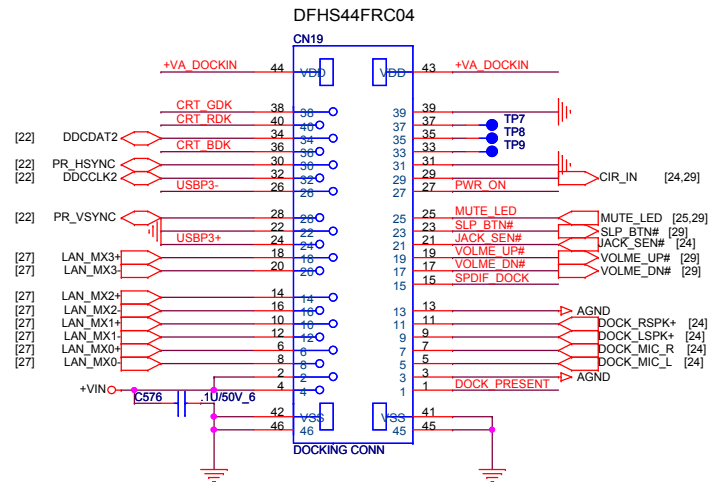
**PROJECT : UP67**  
 Quanta Computer Inc.

NB5

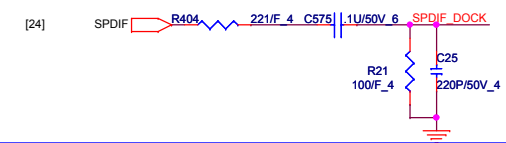
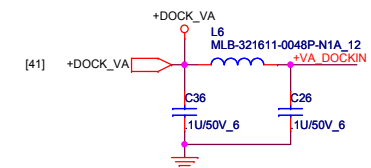
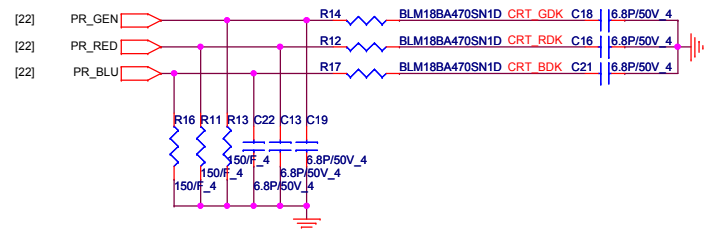
Size Custom Document Number ODD/HDD/NEW CARD/PW/KB Rev 1A

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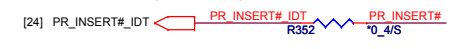
# CABLE DOCK



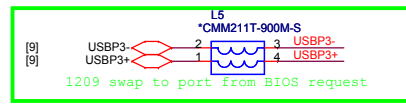
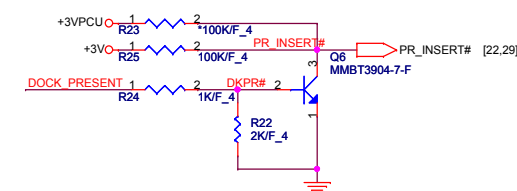
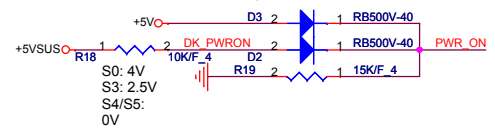
Delete CX08T470000 as CRT rising time and falling time request



For IDT Dolby functionality.

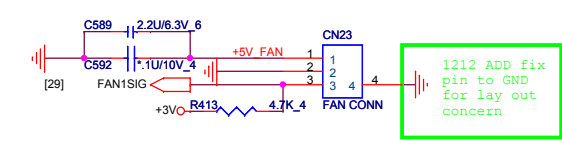


Change to RB500 as Current loss



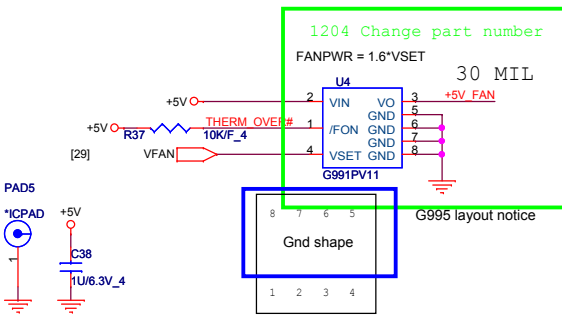
6/1 : PV For EMI request

## CPU FAN

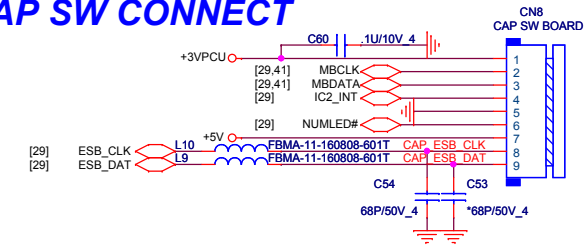


1212 ADD fix pin to GND for lay out concern

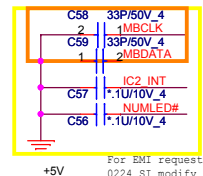
## DFHD03MR008



## CAP SW CONNECT

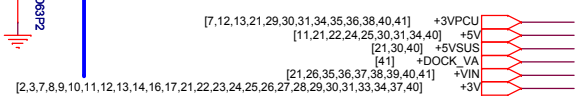
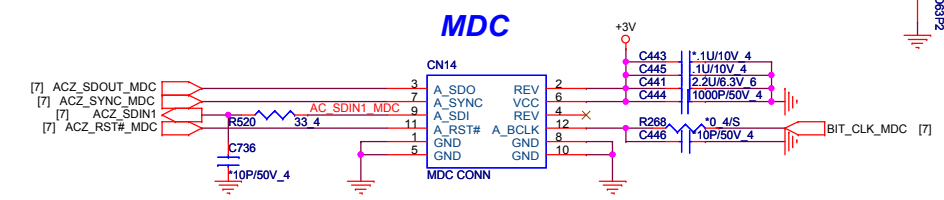


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP\_INT
5. GND
6. NUM LOCK LED
7. +5V\_LED
8. ESB\_CLK
9. ESB\_DAT



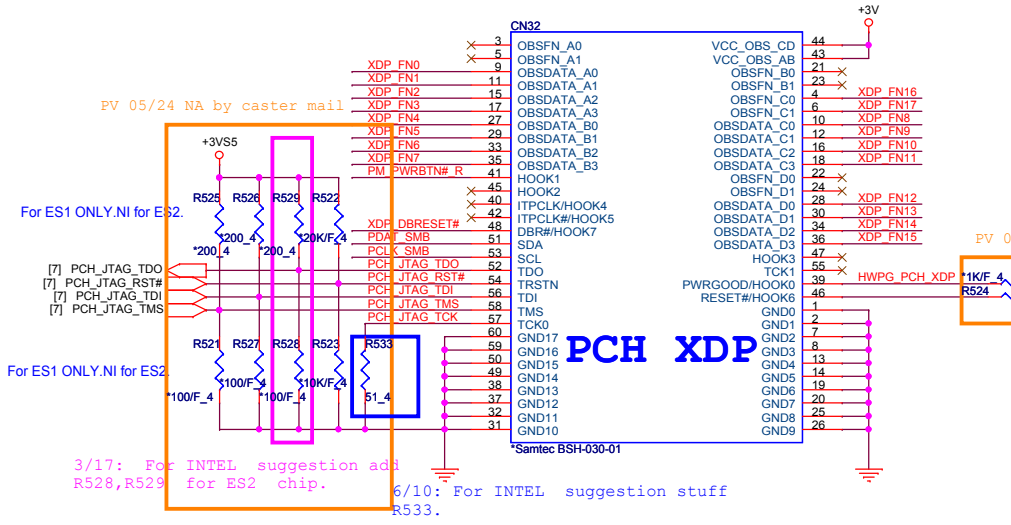
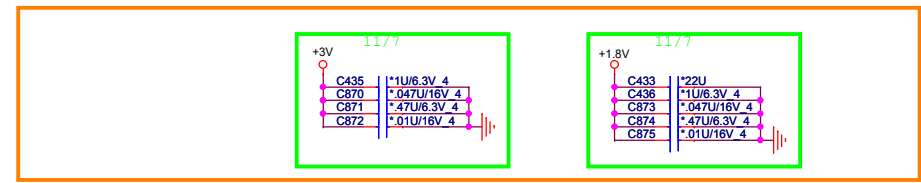
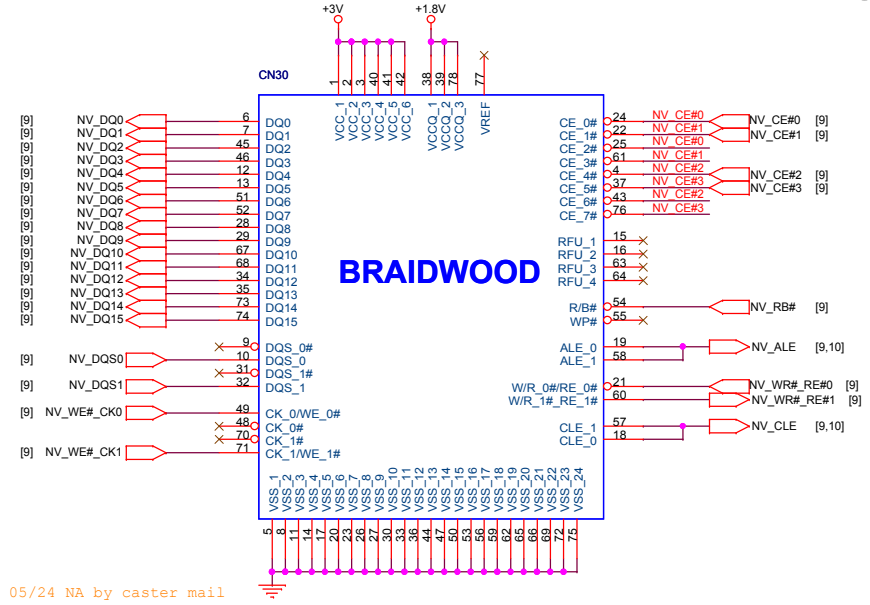
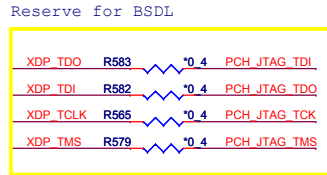
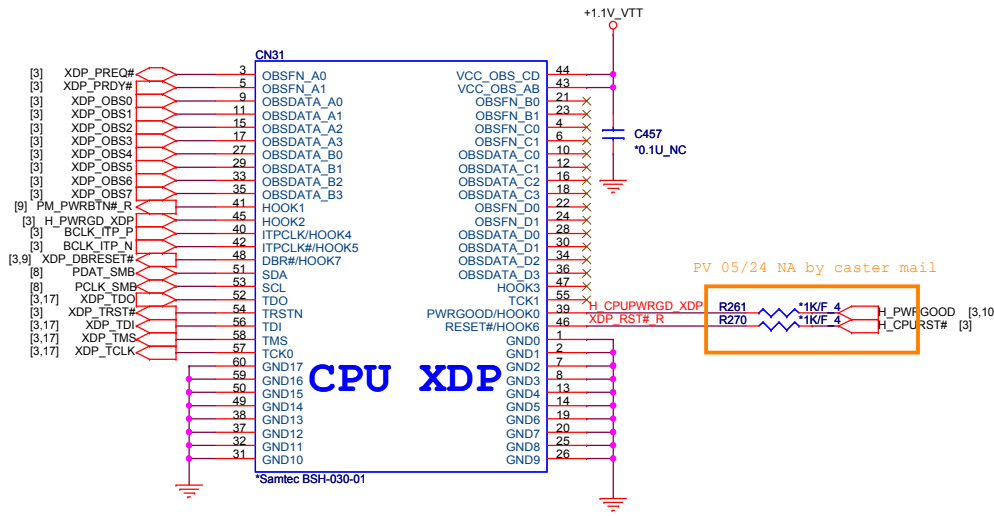
For EMI request 0224 S1 modify

## Modem CONN

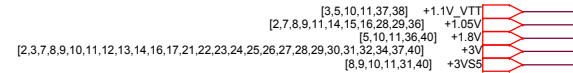
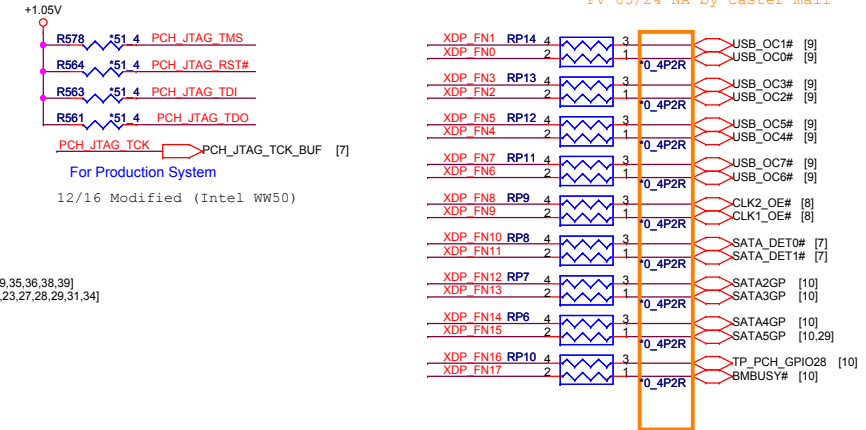


**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>DOCKING/FAN/CAP/MDC</b>	Rev 1A
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3/17: For INTEL suggestion add R528,R529 for ES2 chip.  
 6/10: For INTEL suggestion stuff R533.



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**Quanta Computer Inc.**

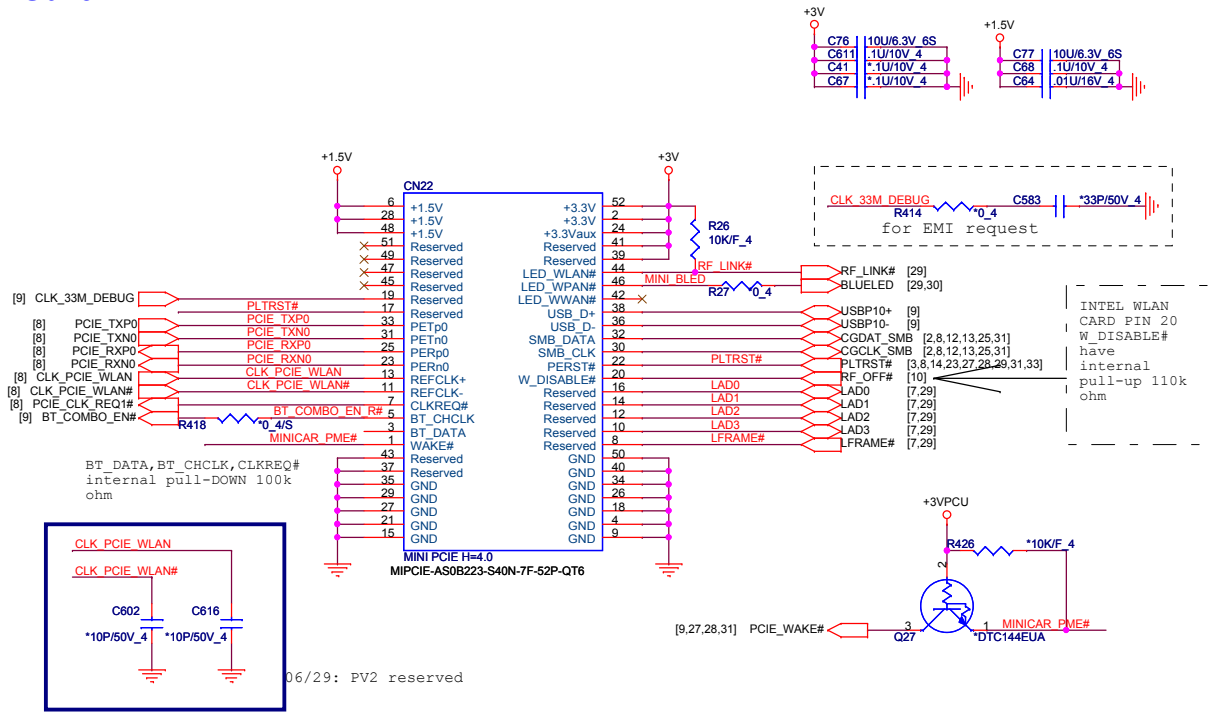
**NB5**

Size Custom Document Number XDP/BRAIDWOOD Rev 1A

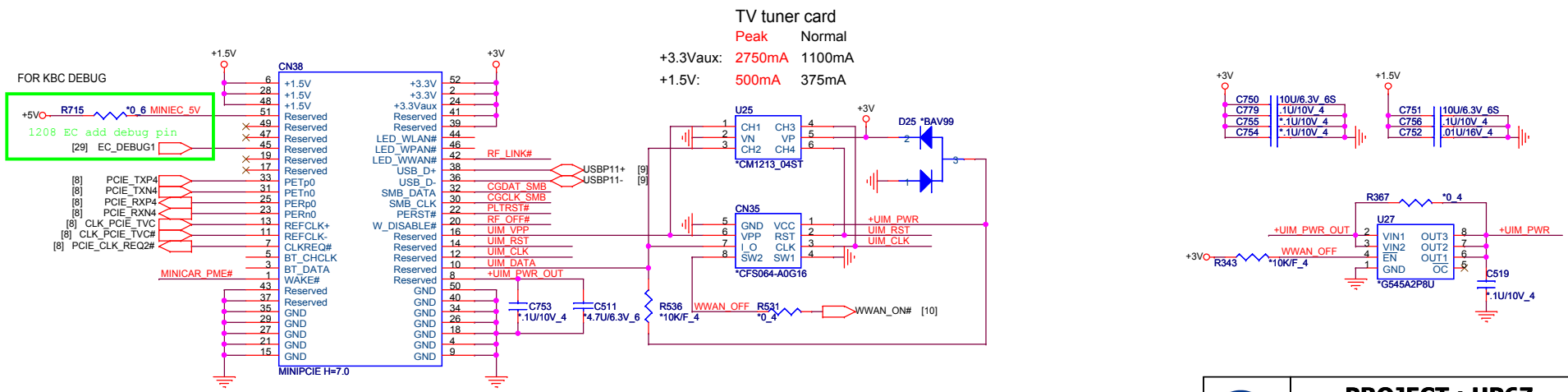
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# Mini PCI-E Card 1 WLAN



# Mini PCI-E Card 2 TV Tuner or WWAN



TV tuner card  
 Peak Normal  
 +3.3Vaux: 2750mA 1100mA  
 +1.5V: 500mA 375mA

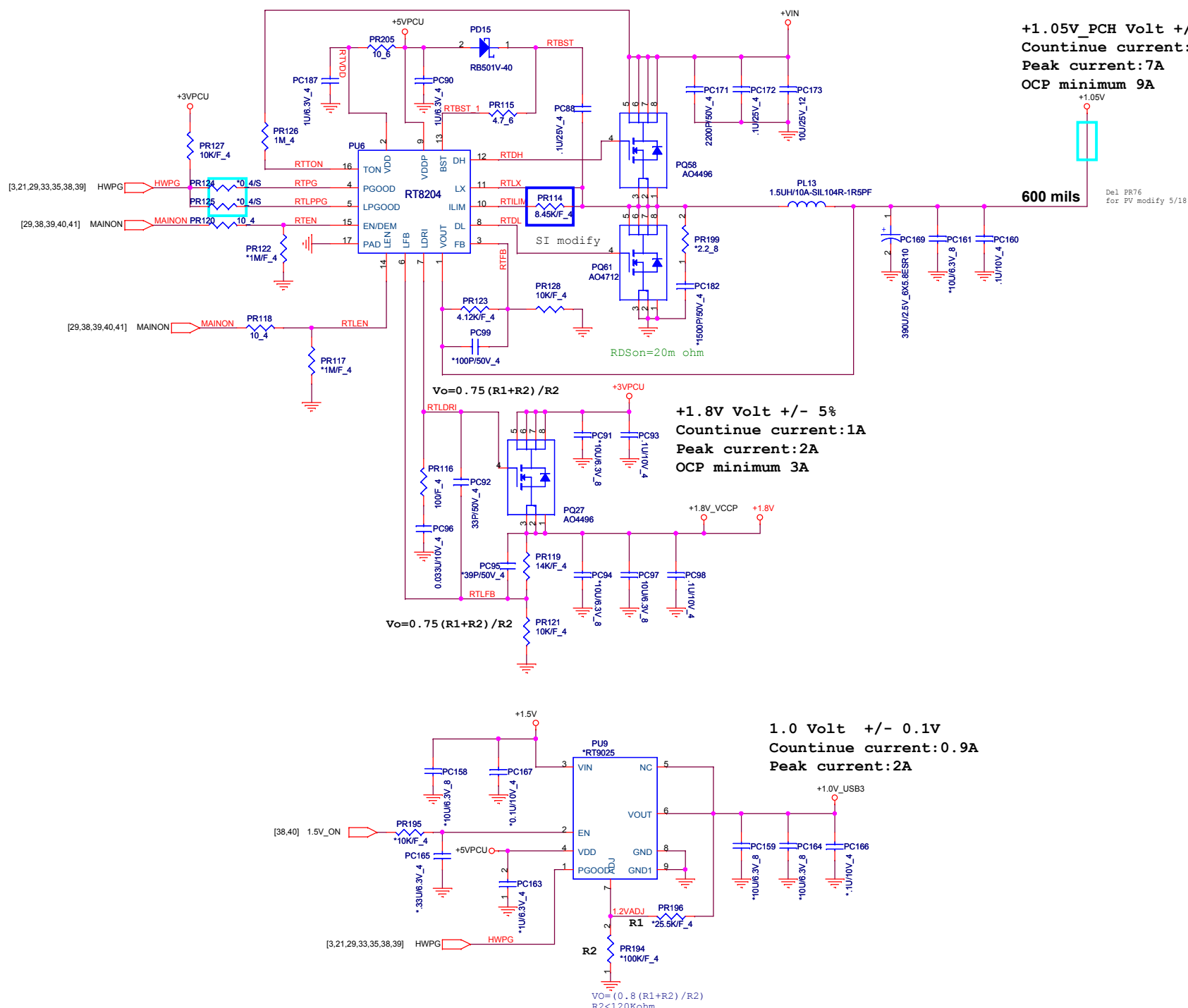
[15,19,20,31,36,39,40] +1.5V  
 [2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40] +3V  
 [7,12,13,21,29,30,31,32,35,36,38,40,41] +3VPCU  
 [11,21,22,24,25,30,31,32,40,41] +5V


**PROJECT : UP67**  
**Quanta Computer Inc.**

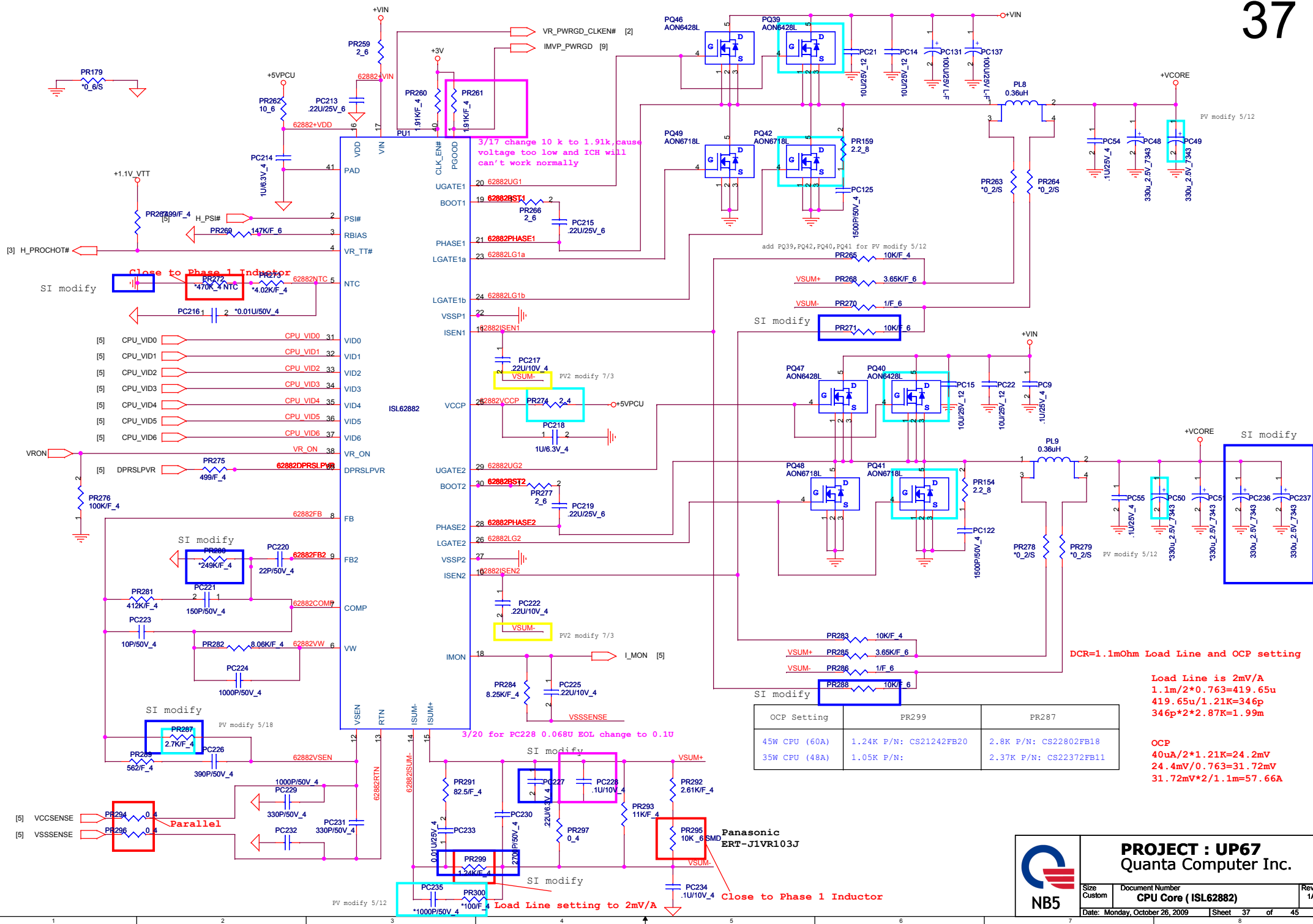
Size Custom    Document Number **MINI PCI-E CONN X2**    Rev 1A

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	<b>PROJECT : UP67</b> <b>Quanta Computer Inc.</b>		Rev 1A
	Size Custom	Document Number <b>+5V/+3V (RT8206B)</b>	



OCP Setting	PR299	PR287
45W CPU (60A)	1.24K P/N: CS21242FB20	2.8K P/N: CS22802FB18
35W CPU (48A)	1.05K P/N:	2.37K P/N: CS22372FB11

DCR=1.1mOhm Load Line and OCP setting

Load Line is 2mV/A  
 $1.1m/2 * 0.763 = 419.65u$   
 $419.65u / 1.21K = 346p$   
 $346p * 2 * 2.87K = 1.99m$

OCP  
 $40uA / 2 * 1.21K = 24.2mV$   
 $24.2mV / 0.763 = 31.72mV$   
 $31.72mV * 2 / 1.1m = 57.66A$

**PROJECT : UP67**  
Quanta Computer Inc.

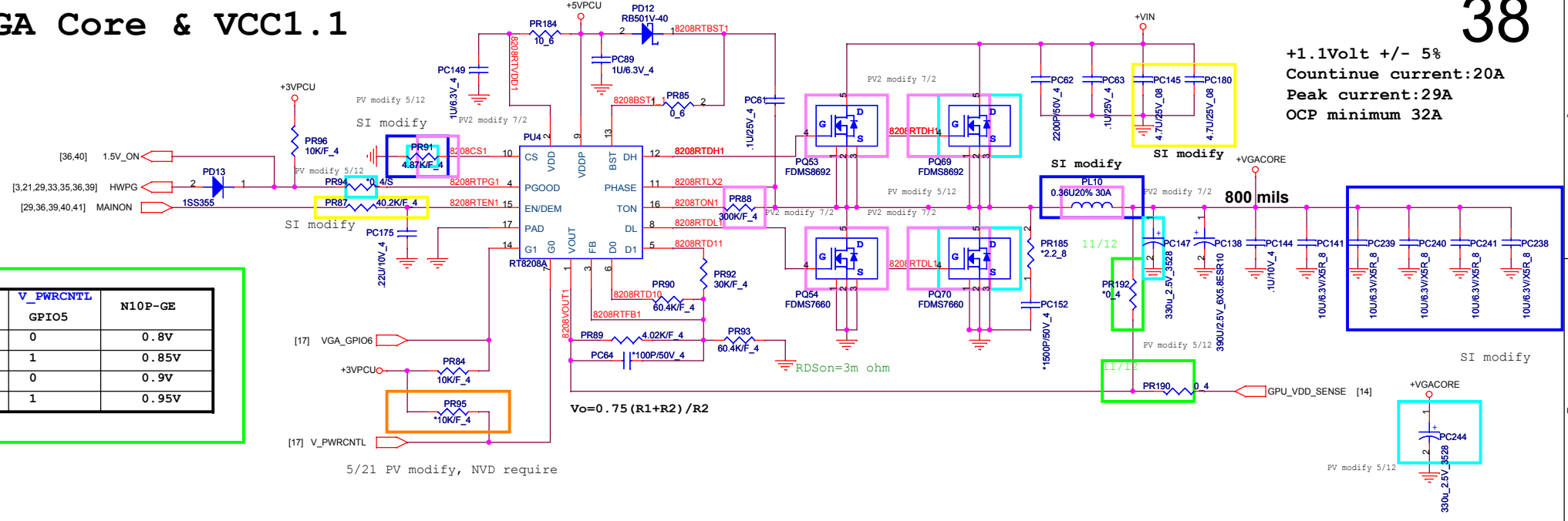
Size Custom	Document Number <b>CPU Core (ISL62882)</b>	Rev 1A
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# VGA Core & VCC1.1

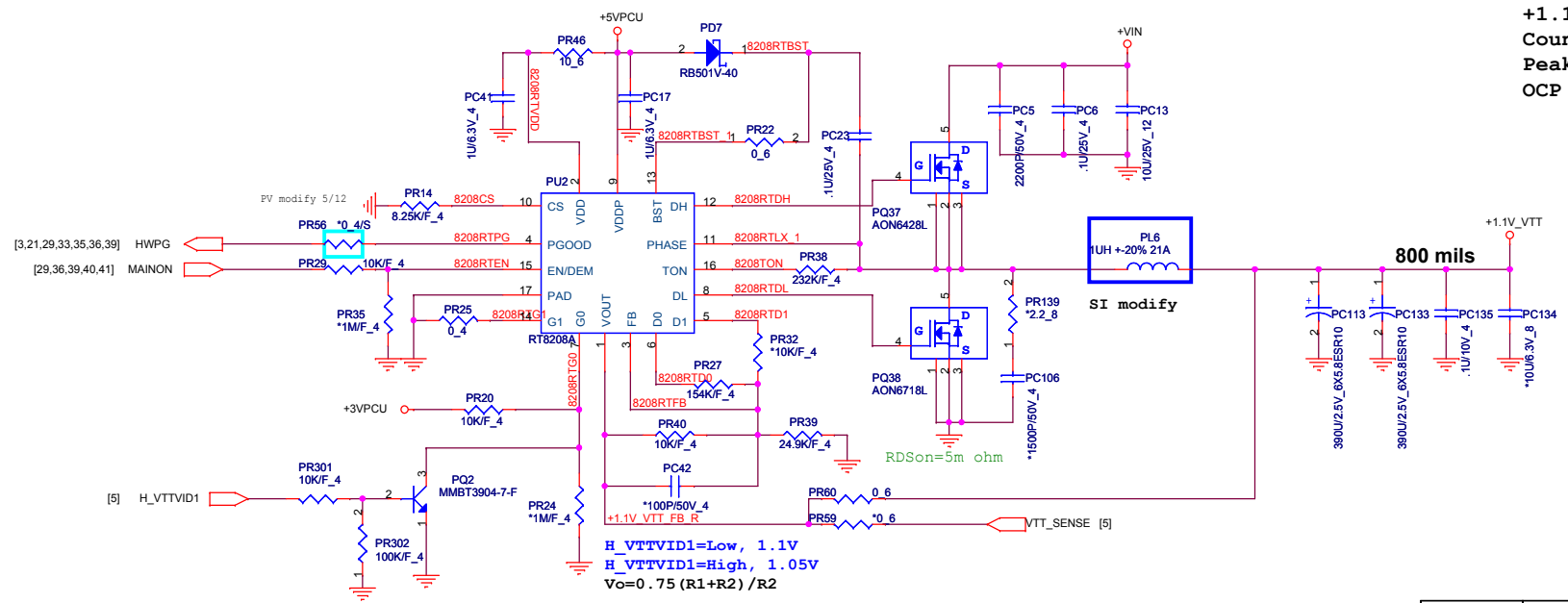
**+1.1Volt +/- 5%**  
**Countinue current:20A**  
**Peak current:29A**  
**OCp minimum 32A**

11/13

VGA_GPIO6	V_PWRCNTL	N10P-GE
GPIO6	GPIO5	
0	0	0.8V
0	1	0.85V
1	0	0.9V
1	1	0.95V

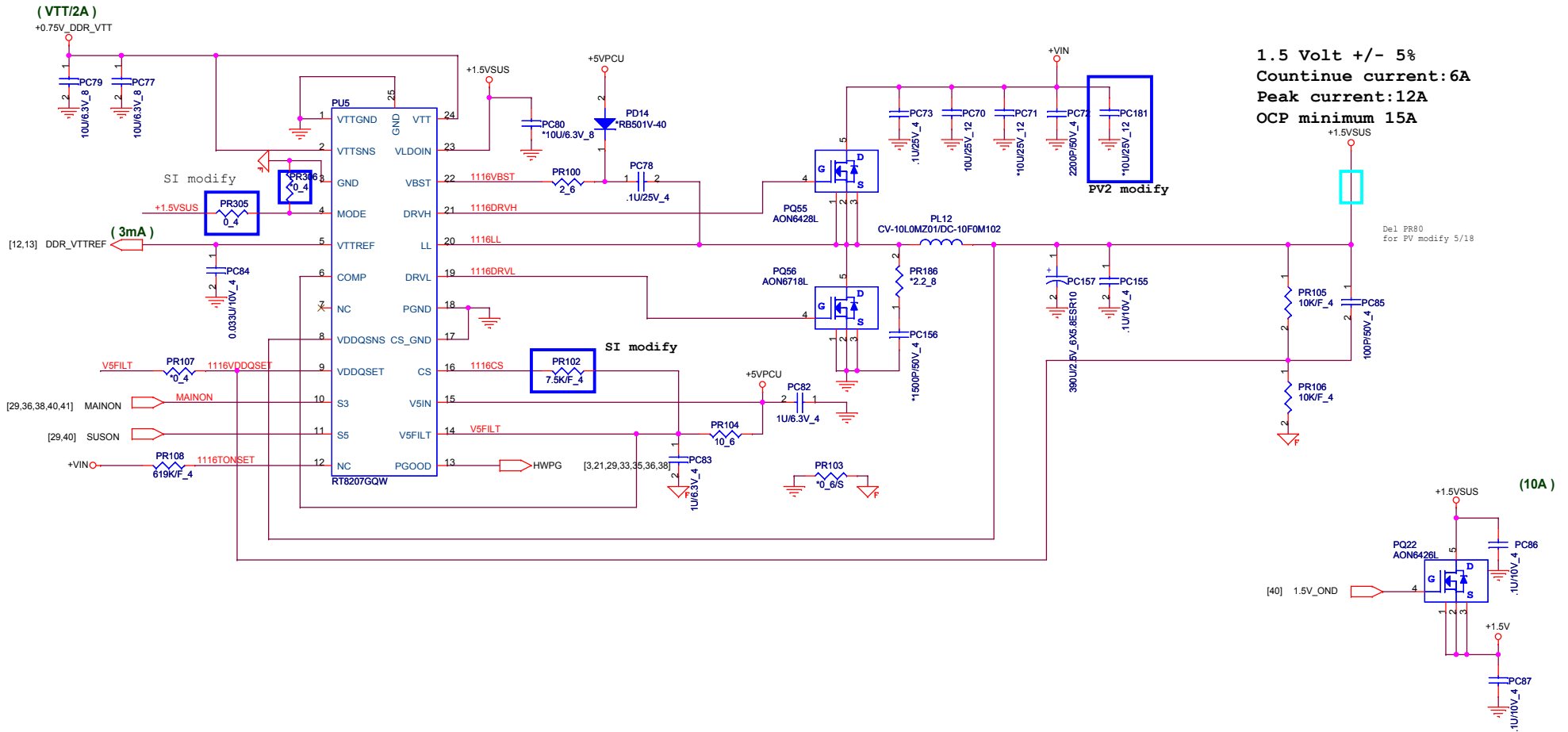


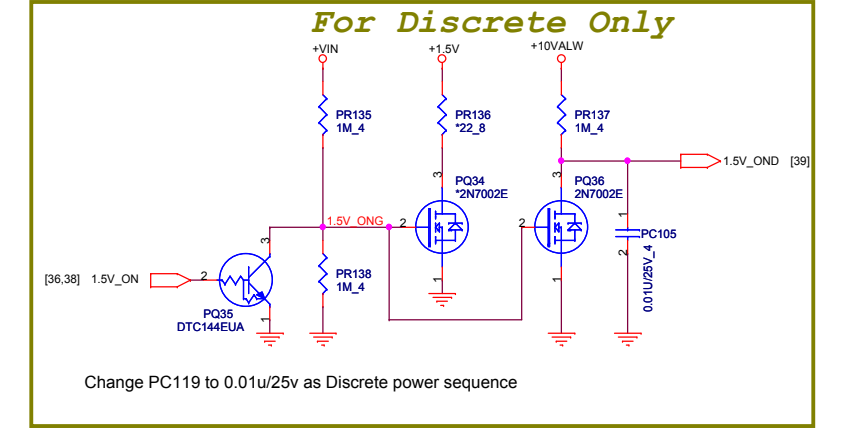
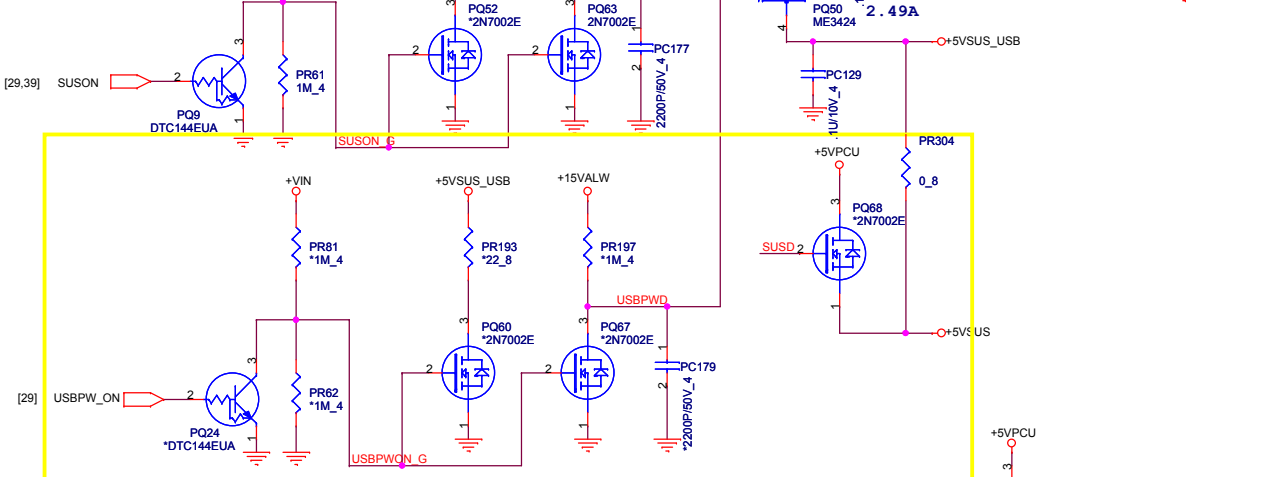
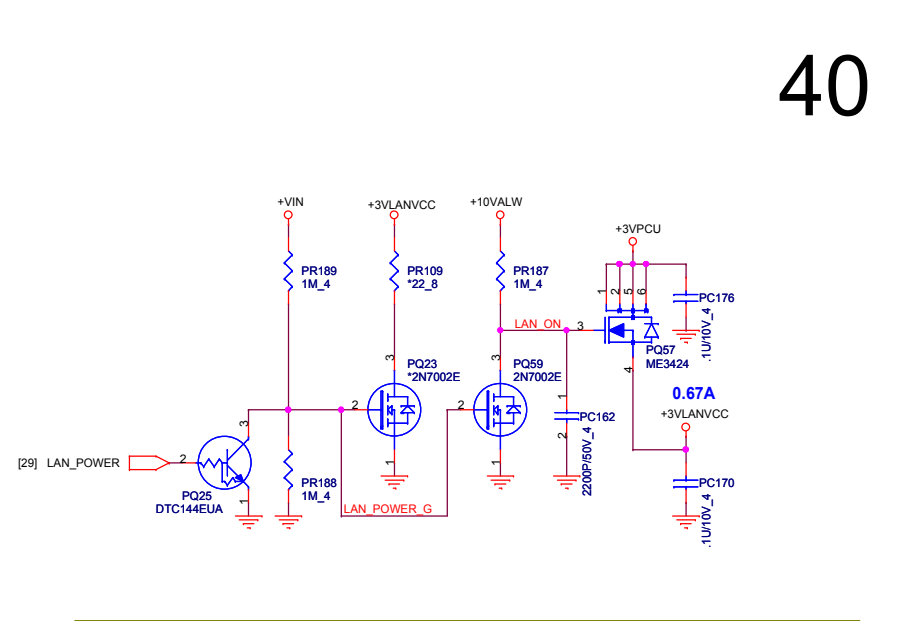
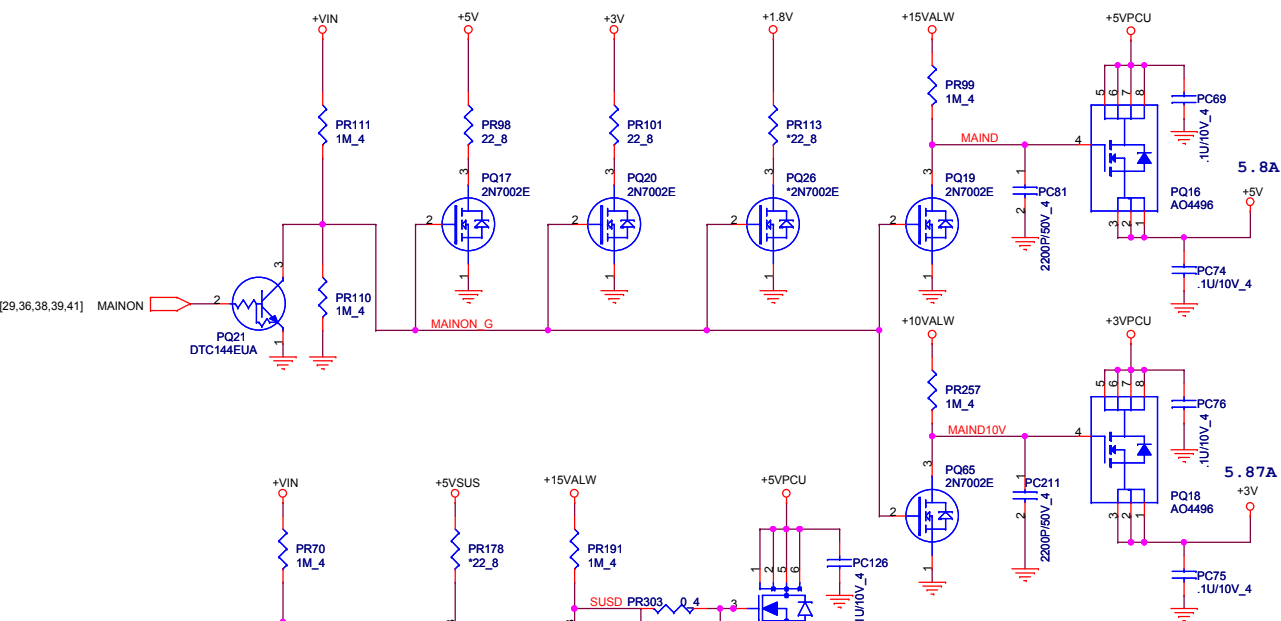
**+1.1V\_PCH Volt +/- 5%**  
**Countinue current:12A**  
**Peak current:15A**  
**OCp minimum 18A**



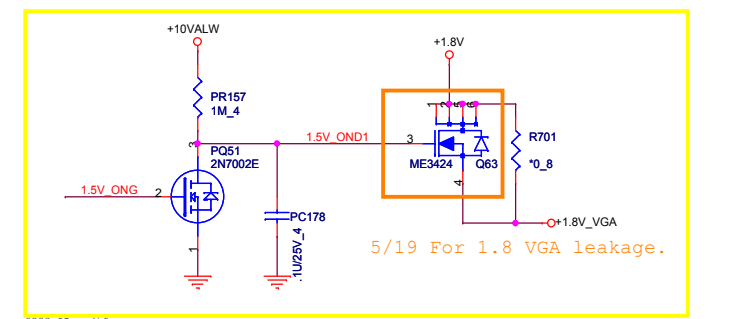
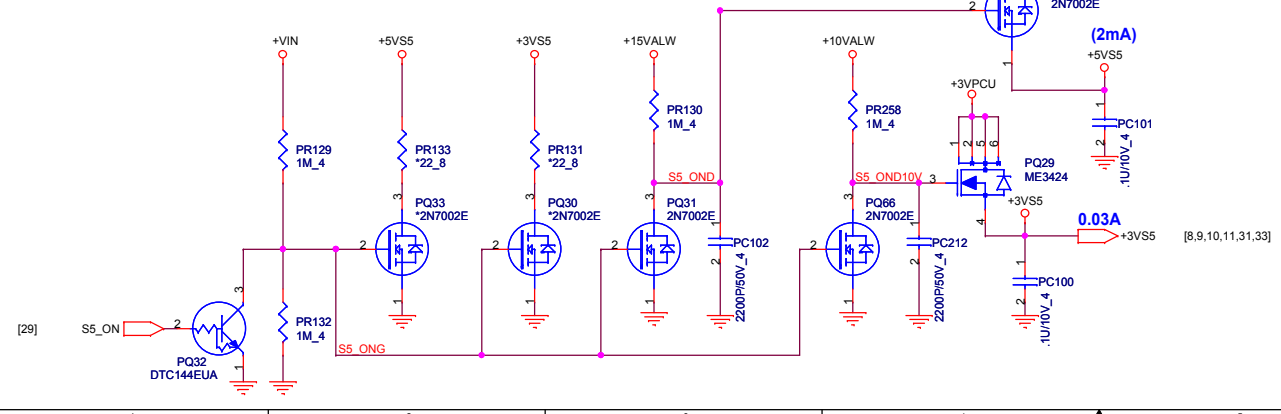
	<b>PROJECT : UP67</b> <b>Quanta Computer Inc.</b>		Rev 1A	
	Size Custom	Document Number <b>+1.1V_VTT/VGA Core (RT8208)</b>		Date: Monday, October 26, 2009   Sheet 38 of 45







*Reserve for Wake from USB*

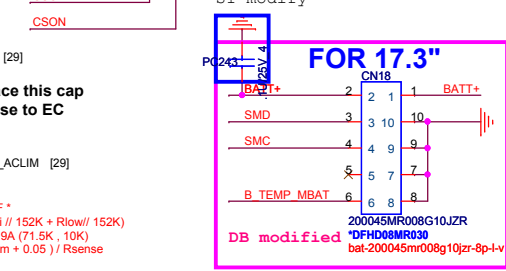
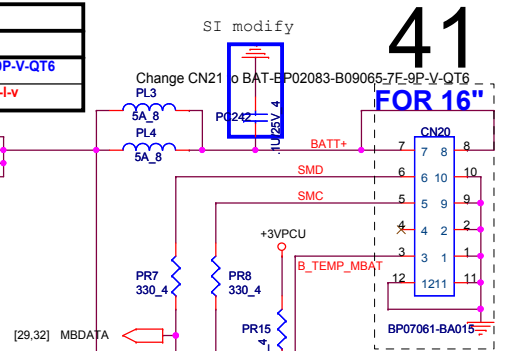
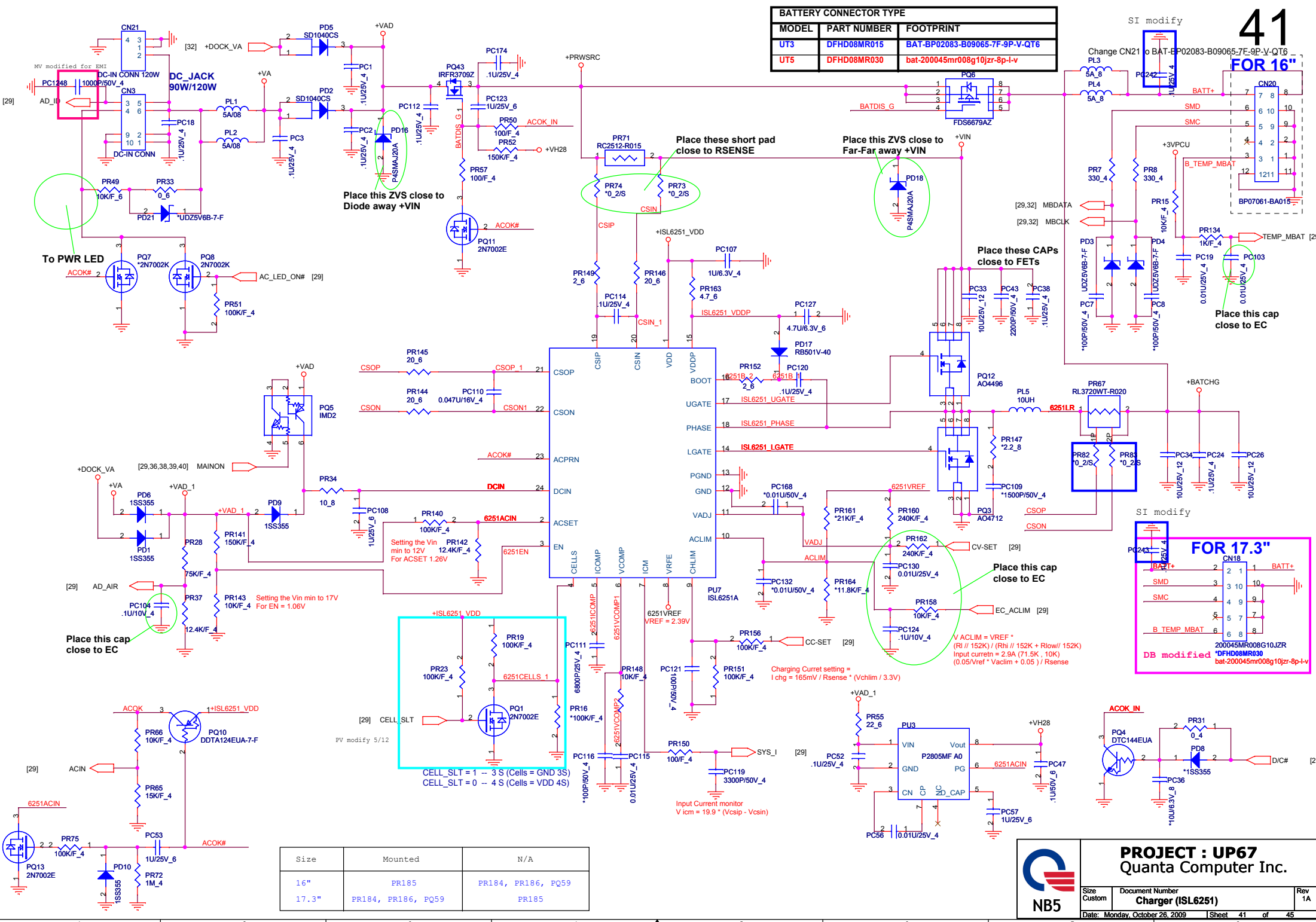


0223 S1 modify  
To meet GPU power sequence

	<b>PROJECT : UP67</b>
	<b>Quanta Computer Inc.</b>
	Size Custom Document Number DISCHARGE/3VS5/5VSS/LAN Rev 1A
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BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT3	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT5	DFHD08MR030	bat-200045mr008g10jzr-8p-l-v

41  
FOR 16"



Place these short pad close to RSENSE

Place this ZVS close to Far-Far away +VIN

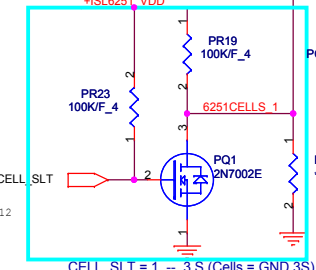
Place this ZVS close to Diode away +VIN

Place these CAPs close to FETs

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC



Charging Current setting =  $I_{chg} = 165mV / R_{sense} * (V_{chlim} / 3.3V)$

Input Current monitor  $V_{icm} = 19.9 * (V_{csip} - V_{csin})$

Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

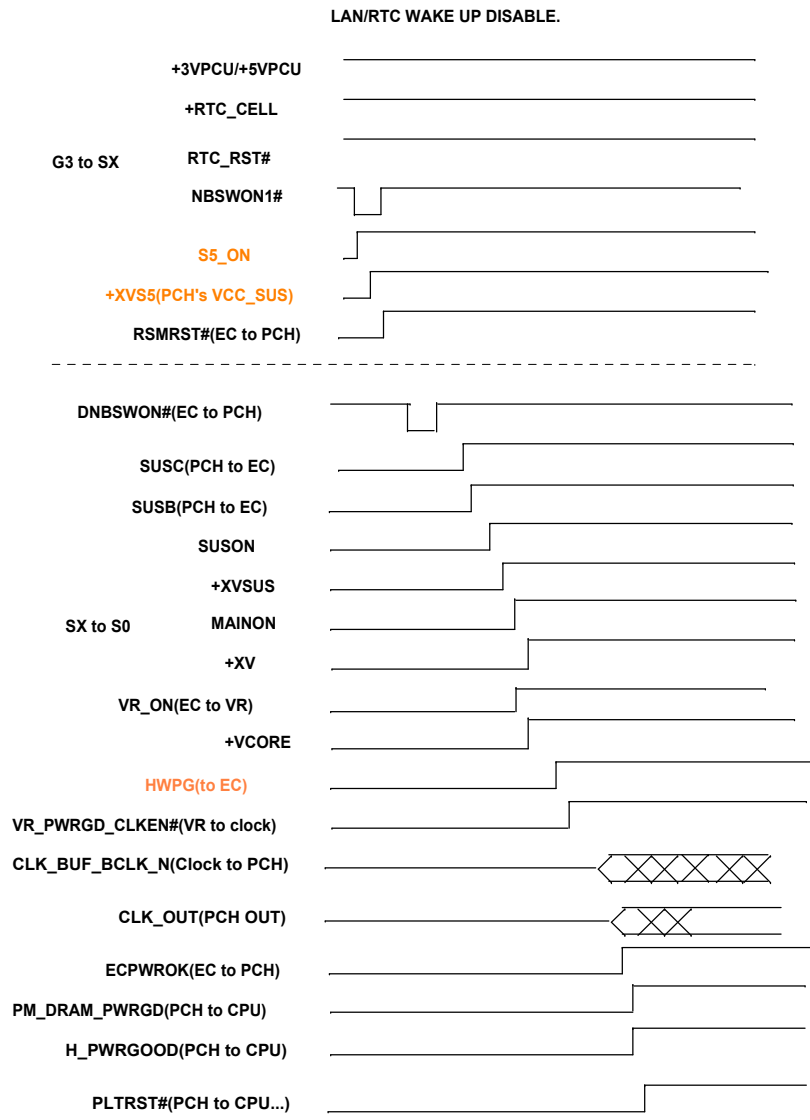
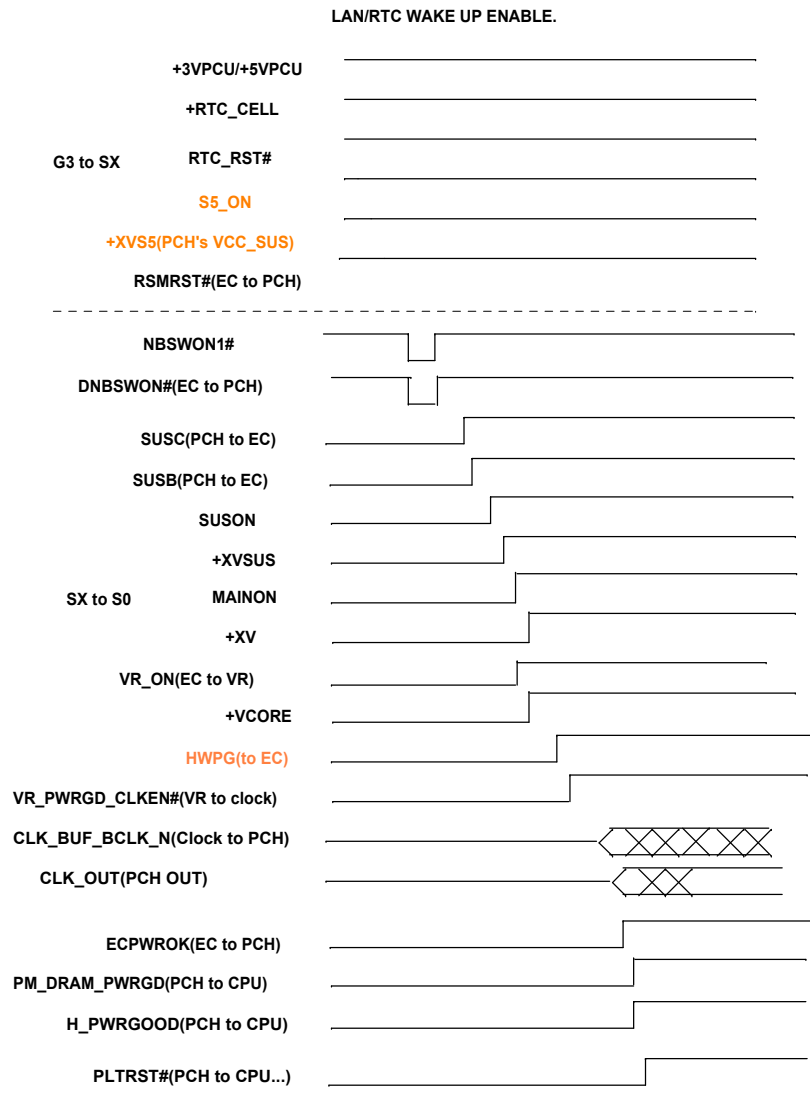
**PROJECT : UP67**  
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NB5

Size Custom Document Number Changer (ISL6251) Rev 1A

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# Power up sequence



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	Size Custom	Document Number <b>Power up sequence</b>	Date: Monday, October 26, 2009   Sheet 42 of 45