LA-2251

Compal confidential

Schematics Document

DT TRANSPORT or Prescott uFCPGA with Sis661FX+Sis963L core logic

2004-05-17

REV:1.0

Compal Electronics, Inc.			
Title: Cover Sheet			
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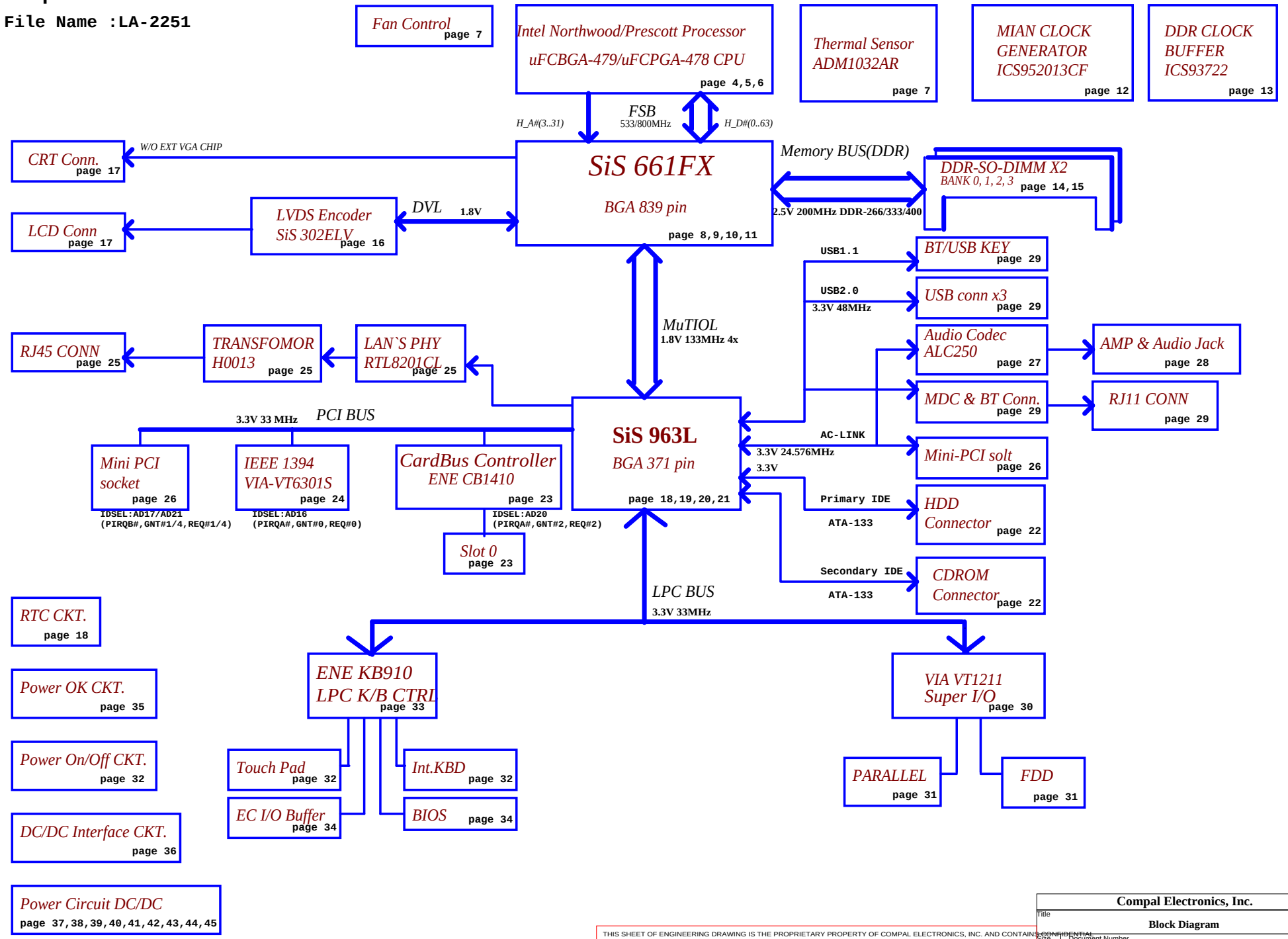
File Name :LA-2251



Compal Electronics, Inc.		
Title: Block Diagram		
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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V	The voltage(1.2V) for Processor VID select	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON*	ON*
+1.8VS	1.8V switched power rail for SIS M661FX NB.	ON	OFF	OFF
+2.5V	2.5V system power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail for DDR Clock Buffer	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
AGP BUS	AGP_DEVSEL	N/A	A
SOUTHBRIDGE	AD13 (INT.)	N/A	N/A
USB	AD14 (INT.)	N/A	E/F/H
AC97	AD13 (INT.)	N/A	C
ATA 100	AD13 (INT.)	N/A	A
ETHERNET	AD15 (INT.)	N/A	D
1394	AD16	0	A
LAN	AD19	3	D
CARD BUS	AD20	2	A
Wireless LAN(MINI PCI)	AD17/AD21	1/4	B

Note: PLACE CLOSE TO M661FX, USE 10/10 WIDTH/SPACE

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build

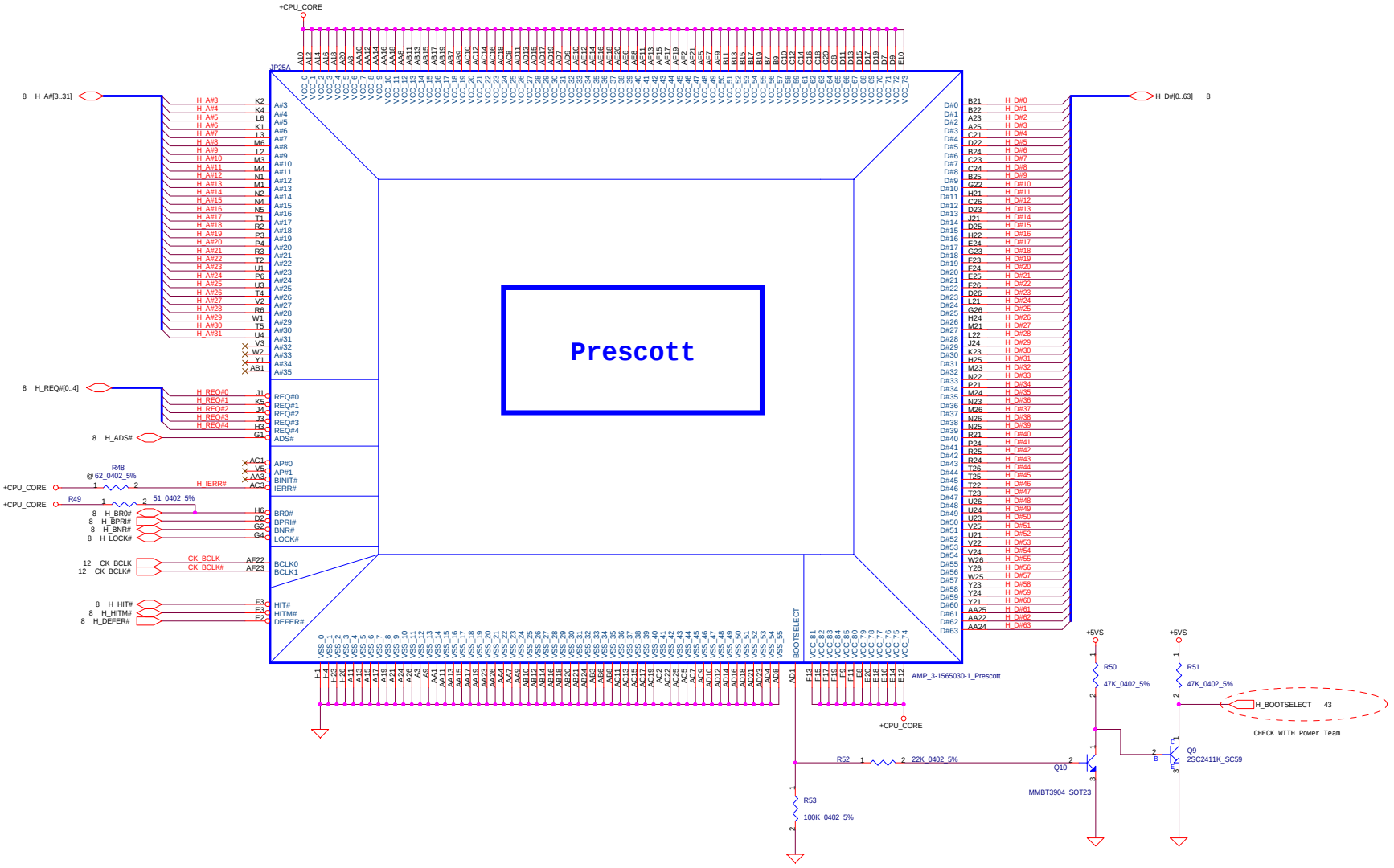
FIR@ : means just build when FIR Module build in .

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	



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Title: Prescott Processor in uFCPGA478		
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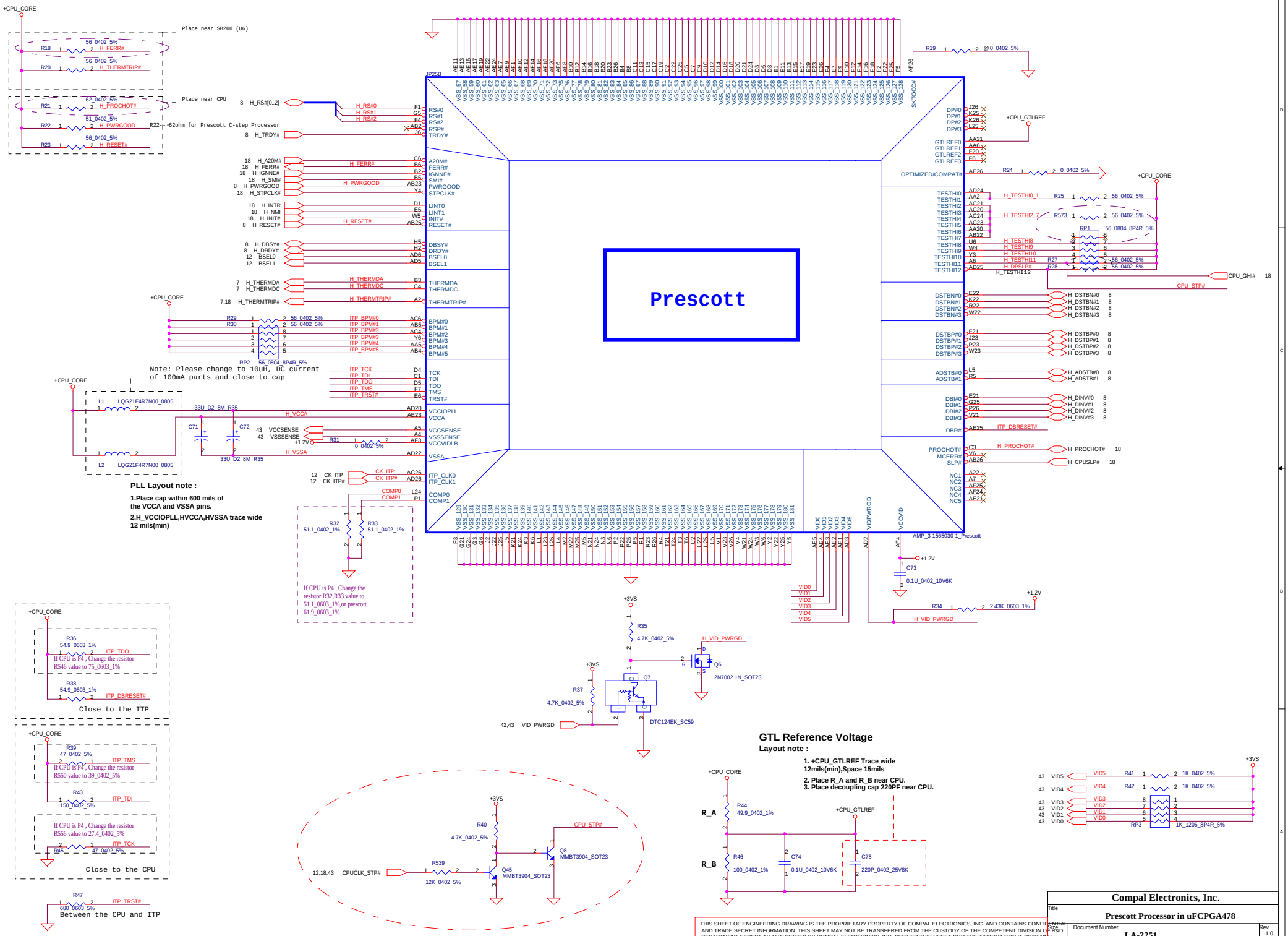

Compal Electronics, Inc.	
Title	Prescott Processor in uFCPGA478
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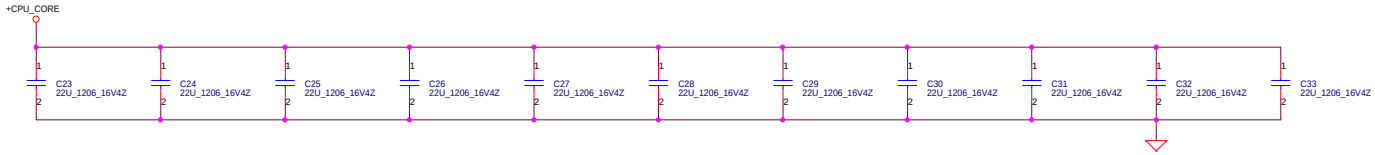
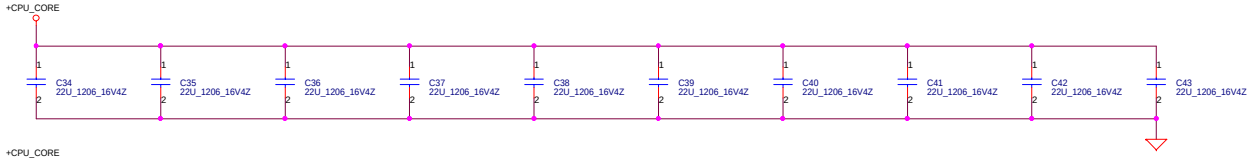
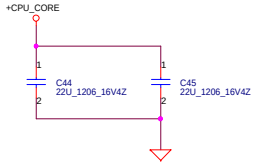
Place 11 North of Socket(Stuff 6)

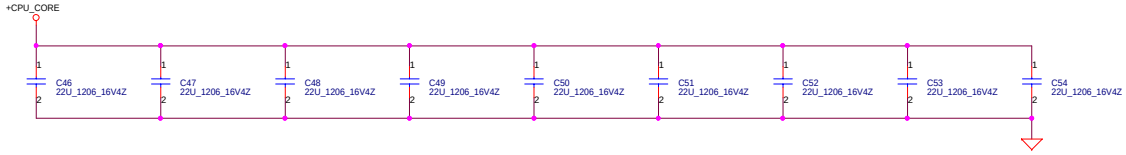


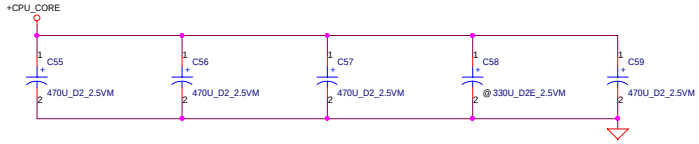
Place 12 Inside Socket(Stuff all)

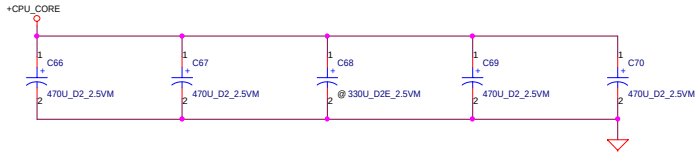




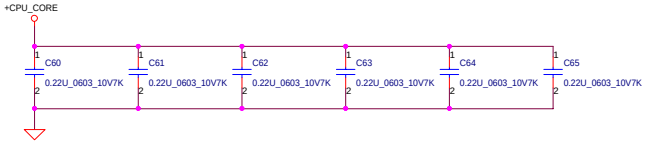
Place 9 South of Socket(Unstuff all)







Place Inside Socket around the edge



Compal Electronics, Inc.		
Title: CPU Decoupling		
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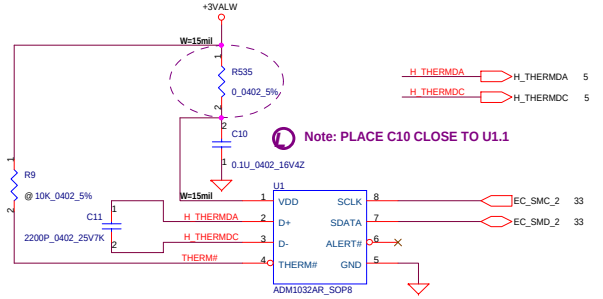
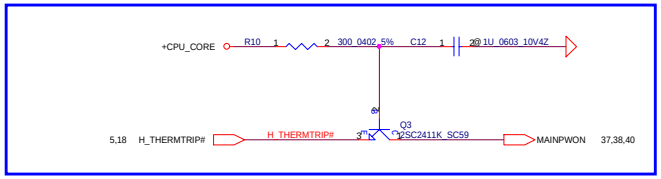
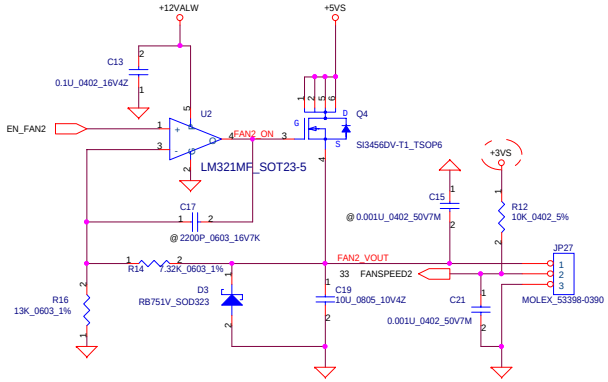
Thermal Sensor ADM1032AR



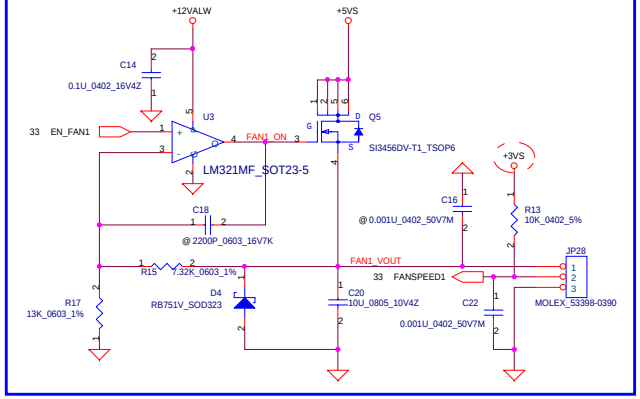
Address:1001_100X



FAN CONN. 2
Fan Control circuit



FAN CONN.1
Fan Control circuit



Compal Electronics, Inc.		
Title: CPU Thermal Sensor&FAN CTRL		
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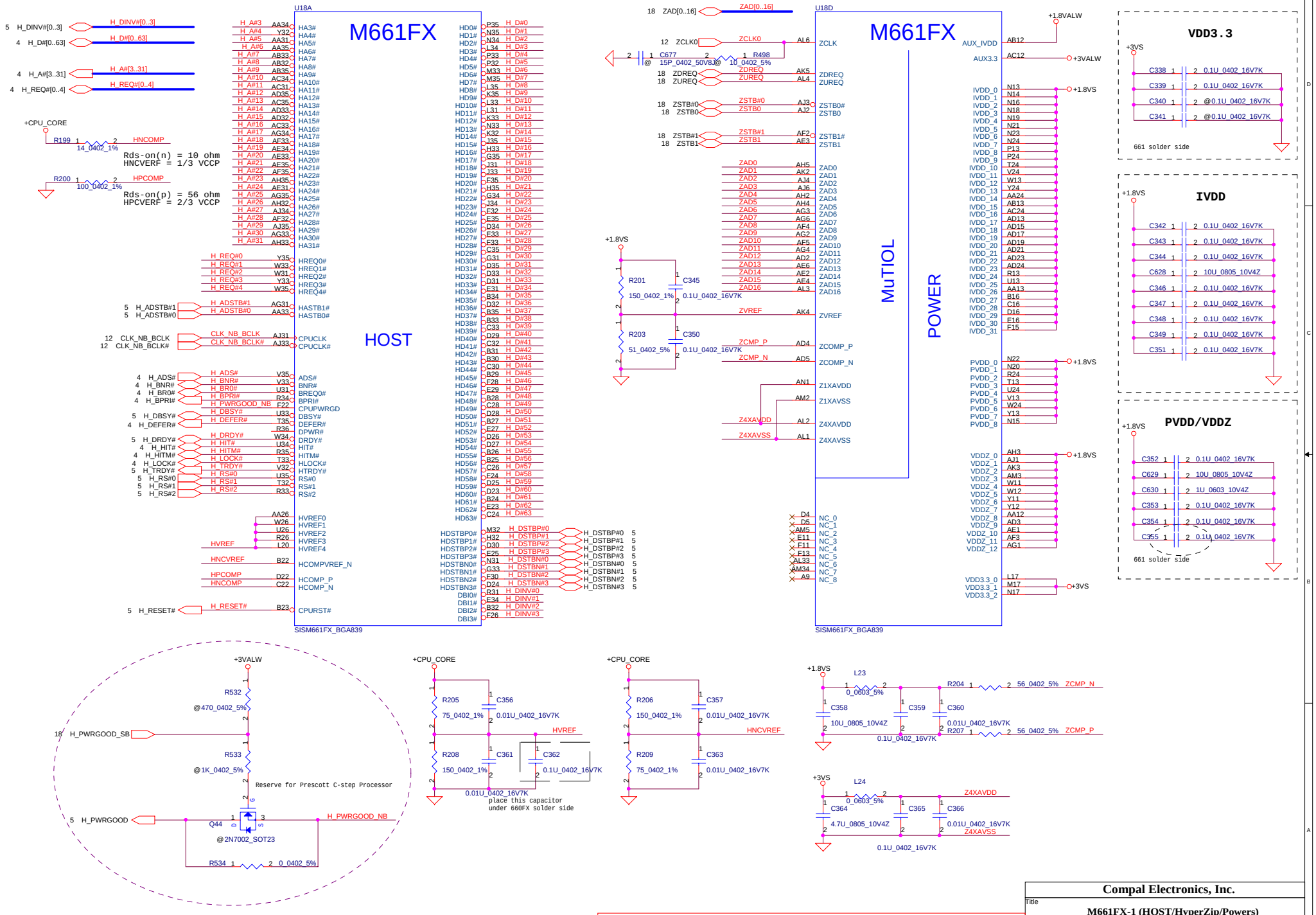

Compal Electronics, Inc.	
Title	M661FX-1 (HOST/HyperZip/Powers)
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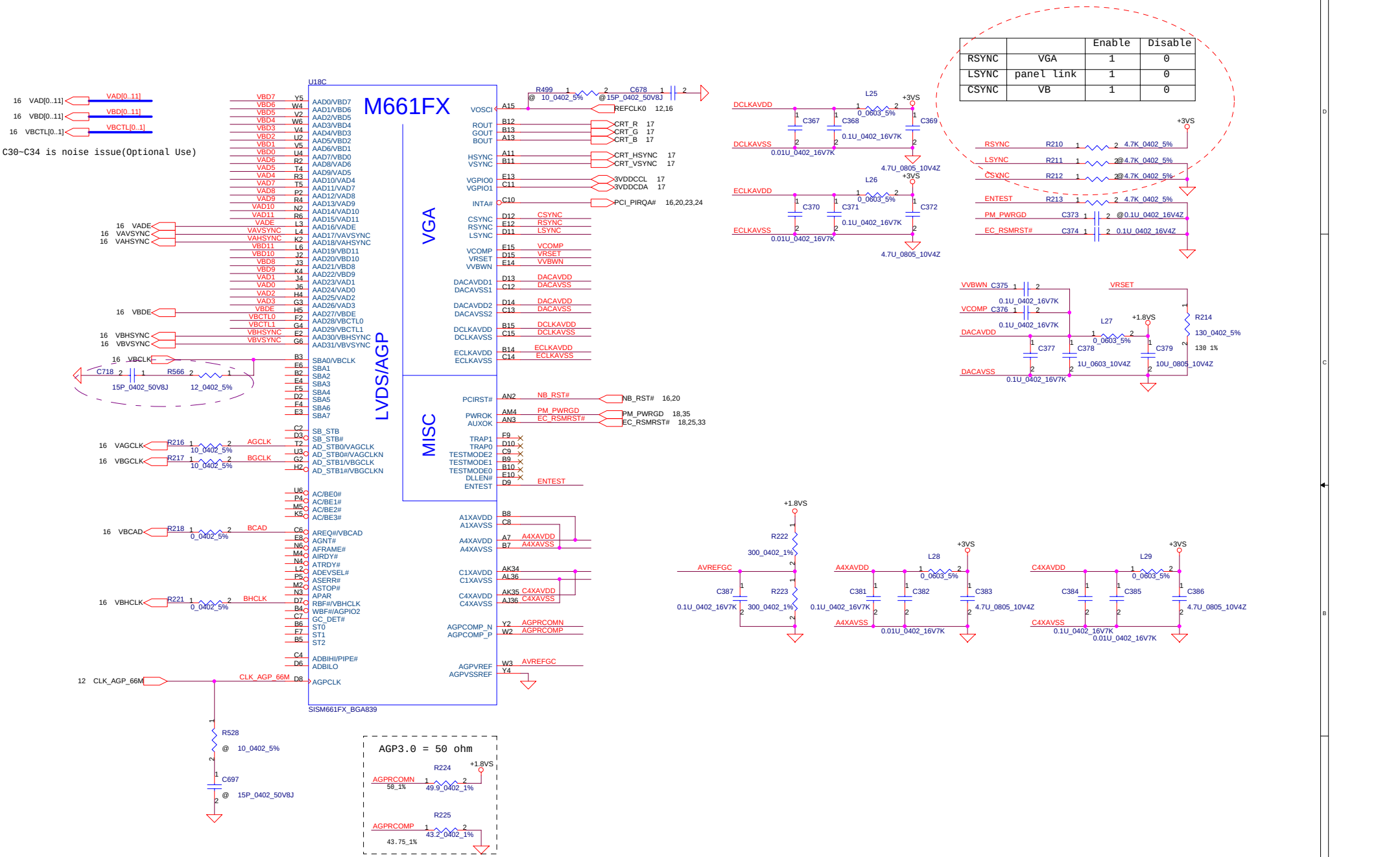

Compal Electronics, Inc.	
Title	M661FX-1 (LVDS/AGP/VGA/MISC)
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Note: PLACE CLOSE TO DIMM0,and between NB chip and DIMM0

RP48 10_0404_4P2R_5%
DDRA_DQ3 1 4 DDRA_SDQ3
DDRA_DQ4 2 3 DDRA_SDQ4

RP35 10_0404_4P2R_5%
DDRA_DQ32 1 4 DDRA_SDQ32
DDRA_DQ36 2 3 DDRA_SDQ36

RP51 10_0404_4P2R_5%
DDRA_DQ1 1 4 DDRA_SDQ1
DDRA_DQ0 2 3 DDRA_SDQ0

RP38 10_0404_4P2R_5%
DDRA_DQ33 1 4 DDRA_SDQ33
DDRA_DQ37 2 3 DDRA_SDQ37

RP53 10_0404_4P2R_5%
DDRA_DQ6 1 4 DDRA_SDQ6
DDRA_DQ7 2 3 DDRA_SDQ7

RP41 10_0404_4P2R_5%
DDRA_DQ38 1 4 DDRA_SDQ38
DDRA_DQ34 2 3 DDRA_SDQ34

RP55 10_0404_4P2R_5%
DDRA_DQ5 1 4 DDRA_SDQ5
DDRA_DQ2 2 3 DDRA_SDQ2

RP44 10_0404_4P2R_5%
DDRA_DQ35 1 4 DDRA_SDQ35
DDRA_DQ39 2 3 DDRA_SDQ39

DDRA_DQS0 2 R241 1 DDRA_SDQS0 10_0402_5%
DDRA_DQS4 2 R226 1 DDRA_SDQS4 10_0402_5%
DDRA_DM0 2 R243 1 DDRA_SDM0 10_0402_5%
DDRA_DM4 2 R229 1 DDRA_SDM4 10_0402_5%

RP36 10_0404_4P2R_5%
DDRA_DQ8 1 4 DDRA_SDQ8
DDRA_DQ13 2 3 DDRA_SDQ13

RP49 10_0404_4P2R_5%
DDRA_DQ45 1 4 DDRA_SDQ45
DDRA_DQ40 2 3 DDRA_SDQ40

RP39 10_0404_4P2R_5%
DDRA_DQ9 1 4 DDRA_SDQ9
DDRA_DQ12 2 3 DDRA_SDQ12

RP52 10_0404_4P2R_5%
DDRA_DQ42 1 4 DDRA_SDQ42
DDRA_DQ41 2 3 DDRA_SDQ41

RP42 10_0404_4P2R_5%
DDRA_DQ10 1 4 DDRA_SDQ10
DDRA_DQ15 2 3 DDRA_SDQ15

RP54 10_0404_4P2R_5%
DDRA_DQ43 1 4 DDRA_SDQ43
DDRA_DQ44 2 3 DDRA_SDQ44

RP45 10_0404_4P2R_5%
DDRA_DQ14 1 4 DDRA_SDQ14
DDRA_DQ11 2 3 DDRA_SDQ11

RP56 10_0404_4P2R_5%
DDRA_DQ47 1 4 DDRA_SDQ47
DDRA_DQ46 2 3 DDRA_SDQ46

DDRA_DQS1 2 R227 1 DDRA_SDQS1 10_0402_5%
DDRA_DQS5 2 R242 1 DDRA_SDQS5 10_0402_5%
DDRA_DM1 2 R228 1 DDRA_SDM1 10_0402_5%
DDRA_DM5 2 R244 1 DDRA_SDM5 10_0402_5%

RP57 10_0404_4P2R_5%
DDRA_DQ20 1 4 DDRA_SDQ20
DDRA_DQ17 2 3 DDRA_SDQ17

RP66 10_0404_4P2R_5%
DDRA_DQ54 1 4 DDRA_SDQ54
DDRA_DQ48 2 3 DDRA_SDQ48

RP59 10_0404_4P2R_5%
DDRA_DQ18 1 4 DDRA_SDQ18
DDRA_DQ21 2 3 DDRA_SDQ21

RP68 10_0404_4P2R_5%
DDRA_DQ53 1 4 DDRA_SDQ53
DDRA_DQ49 2 3 DDRA_SDQ49

RP61 10_0404_4P2R_5%
DDRA_DQ16 1 4 DDRA_SDQ16
DDRA_DQ22 2 3 DDRA_SDQ22

RP70 10_0404_4P2R_5%
DDRA_DQ50 1 4 DDRA_SDQ50
DDRA_DQ55 2 3 DDRA_SDQ55

RP63 10_0404_4P2R_5%
DDRA_DQ19 1 4 DDRA_SDQ19
DDRA_DQ23 2 3 DDRA_SDQ23

RP72 10_0404_4P2R_5%
DDRA_DQ51 1 4 DDRA_SDQ51
DDRA_DQ52 2 3 DDRA_SDQ52

DDRA_DM2 2 R249 1 DDRA_SDM2 10_0402_5%
DDRA_DQS6 2 R258 1 DDRA_SDQS6 10_0402_5%
DDRA_DQS2 2 R253 1 DDRA_SDQS2 10_0402_5%
DDRA_DM6 2 R261 1 DDRA_SDM6 10_0402_5%

RP65 10_0404_4P2R_5%
DDRA_DQ30 1 4 DDRA_SDQ30
DDRA_DQ28 2 3 DDRA_SDQ28

RP58 10_0404_4P2R_5%
DDRA_DQ56 1 4 DDRA_SDQ56
DDRA_DQ58 2 3 DDRA_SDQ58

RP67 10_0404_4P2R_5%
DDRA_DQ31 1 4 DDRA_SDQ31
DDRA_DQ25 2 3 DDRA_SDQ25

RP60 10_0404_4P2R_5%
DDRA_DQ62 1 4 DDRA_SDQ62
DDRA_DQ61 2 3 DDRA_SDQ61

RP69 10_0404_4P2R_5%
DDRA_DQ29 1 4 DDRA_SDQ29
DDRA_DQ24 2 3 DDRA_SDQ24

RP62 10_0404_4P2R_5%
DDRA_DQ63 1 4 DDRA_SDQ63
DDRA_DQ60 2 3 DDRA_SDQ60

RP71 10_0404_4P2R_5%
DDRA_DQ27 1 4 DDRA_SDQ27
DDRA_DQ26 2 3 DDRA_SDQ26

RP64 10_0404_4P2R_5%
DDRA_DQ59 1 4 DDRA_SDQ59
DDRA_DQ57 2 3 DDRA_SDQ57

DDRA_DQS3 2 R257 1 DDRA_SDQS3 10_0402_5%
DDRA_DQS7 2 R250 1 DDRA_SDQS7 10_0402_5%
DDRA_DM3 2 R260 1 DDRA_SDM3 10_0402_5%
DDRA_DM7 2 R254 1 DDRA_SDM7 10_0402_5%

DDRA_SDM[0..7] DDRA_SDM[0..7] 14,15
DDRA_SDQ[0..63] DDRA_SDQ[0..63] 14,15
DDRA_SDQS[0..7] DDRA_SDQS[0..7] 14,15
DDRA_SMA[0..15] DDRA_SMA[0..15] 14,15

U18B
M661FX
MEMORY
SISM661FX_BGA839

DDRA_DQ0	AN35	MD0	MA0	AR23	DDRA_ADD0
DDRA_DQ1	AP36	MD1	MA1	AN23	DDRA_ADD1
DDRA_DQ2	AK33	MD2	MA2	AN22	DDRA_ADD2
DDRA_DQ3	AM33	MD3	MA3	AM23	DDRA_ADD3
DDRA_DQ4	AN34	MD4	MA4	AL23	DDRA_ADD4
DDRA_DQ5	AK32	MD5	MA5	AL26	DDRA_ADD5
DDRA_DQ6	AR34	MD6	MA6	AN26	DDRA_ADD6
DDRA_DQ7	AN33	MD7	MA7	AN27	DDRA_ADD7
DDRA_DQ8	AM32	MD8	MA8	AR27	DDRA_ADD8
DDRA_DQ9	AL31	MD9	MA9	AR28	DDRA_ADD9
DDRA_DQ10	AR31	MD10	MA10	AP22	DDRA_ADD10
DDRA_DQ11	AL30	MD11	MA11	AN18	DDRA_ADD13
DDRA_DQ12	AN32	MD12	MA12	AR22	DDRA_ADD14
DDRA_DQ13	AR33	MD13	MA13	AP28	DDRA_ADD11
DDRA_DQ14	AN31	MD14	MA14	AM27	DDRA_ADD12
DDRA_DQ15	AM31	MD15	TEST1	AT14	DDRA_ADD15
DDRA_DQ16	AP30	MD16			
DDRA_DQ17	AR30	MD17			
DDRA_DQ18	AM29	MD18	DQS0/CSB0#	AP34	DDRA_DQS0
DDRA_DQ19	AL27	MD19	DQS1/CSB1#	AP32	DDRA_DQS1
DDRA_DQ20	AN30	MD20	DQS2/CSB2#	AR29	DDRA_DQS2
DDRA_DQ21	AN29	MD21	DQS3/CSB3#	AR25	DDRA_DQS3
DDRA_DQ22	AL28	MD22	DQS4/CSB4#	AR20	DDRA_DQS4
DDRA_DQ23	AN28	MD23	DQS5/CSB5#	AR16	DDRA_DQS5
DDRA_DQ24	AP26	MD24	DQS6/CSB6#	AR13	DDRA_DQS6
DDRA_DQ25	AN25	MD25	DQS7/CSB7#	AR10	DDRA_DQS7
DDRA_DQ26	AR24	MD26			
DDRA_DQ27	AL24	MD27			
DDRA_DQ28	AL25	MD28	SRAS#	AL17	DDRA_RAS#
DDRA_DQ29	AR26	MD29	SCAS#	AR19	DDRA_CAS#
DDRA_DQ30	AM25	MD30	SWE#	AN19	DDRA_WE#
DDRA_DQ31	AN24	MD31			
DDRA_DQ32	AN21	MD32			
DDRA_DQ33	AP20	MD33	CS0#	AM17	DDRA_CS#0
DDRA_DQ34	AN20	MD34	CS1#	AL16	DDRA_CS#1
DDRA_DQ35	AL18	MD35	CS2#	AN17	DDRA_CS#2
DDRA_DQ36	AM21	MD36	CS3#	AR17	DDRA_CS#3
DDRA_DQ37	AR21	MD37	CS4#	AP18	
DDRA_DQ38	AL19	MD38	CS5#	AR18	
DDRA_DQ39	AM19	MD39			
DDRA_DQ40	AL15	MD40			
DDRA_DQ41	AL14	MD41	CKE0	AP4	DDRA_CKE0
DDRA_DQ42	AN15	MD42	CKE1	AT3	DDRA_CKE1
DDRA_DQ43	AR15	MD43	CKE2	AR3	DDRA_CKE2
DDRA_DQ44	AN16	MD44	CKE3	AP3	DDRA_CKE3
DDRA_DQ45	AM15	MD45	CKE4	AR2	
DDRA_DQ46	AN14	MD46	CKE5	AN4	
DDRA_DQ47	AL13	MD47			
DDRA_DQ48	AM13	MD48	S3AUXSW#	AP2	S3AUXSW#
DDRA_DQ49	AL12	MD49			
DDRA_DQ50	AL11	MD50	FWDSDCLKO	AL21	ADCLKO
DDRA_DQ51	AR12	MD51	DRAMTEST	AL22	
DDRA_DQ52	AP14	MD52			
DDRA_DQ53	AR14	MD53	DLLAVDD	AL35	DLLAVDD
DDRA_DQ54	AN13	MD54			
DDRA_DQ55	AP12	MD55	DLLAVSS	AL34	DLLAVSS
DDRA_DQ56	AL10	MD56			
DDRA_DQ57	AR11	MD57	DDRAVDD	AM35	DDRAVDD
DDRA_DQ58	AM9	MD58			
DDRA_DQ59	AR9	MD59	DDRAVSS	AN36	DDRAVSS
DDRA_DQ60	AM11	MD60			
DDRA_DQ61	AN11	MD61	TRAP2	AP1	
DDRA_DQ62	AP10	MD62			
DDRA_DQ63	AN9	MD63			
			DDRVREFA	AF16	DDRVREFA
DDRA_DM0	AR35	DQM0	DDRVREFB	AF23	DDRVREFB
DDRA_DM1	AR32	DQM1			
DDRA_DM2	AL29	DQM2	DDRCOMP_P	AR8	DDRCOMP
DDRA_DM3	AP24	DQM3	DDRCOMP_N	AP8	DDRCOMN
DDRA_DM4	AL20	DQM4			
DDRA_DM5	AP16	DQM5			
DDRA_DM6	AN12	DQM6			
DDRA_DM7	AN10	DQM7			

R245 1 2 4.7K_0402_5% +3VALW
S3AUXSW# S3AUXSW# 33
R246 1 2 22_0402_5% FWDSDCLKO FWDSDCLKO 13
C398 1 2 @10P_0402_50V8J

Note: PLACE CLOSE TO DIMM0,and between NB chip and DIMM0

RP34 0_0404_4P2R_5%
DDRA_ADD13 1 4 DDRA_SMA13
DDRA_ADD10 2 3 DDRA_SMA10

RP37 0_0404_4P2R_5%
DDRA_ADD1 1 4 DDRA_SMA1
DDRA_ADD3 2 3 DDRA_SMA3

RP40 0_0404_4P2R_5%
DDRA_ADD0 1 4 DDRA_SMA0
DDRA_ADD2 2 3 DDRA_SMA2

RP43 0_0404_4P2R_5%
DDRA_ADD5 1 4 DDRA_SMA5
DDRA_ADD7 2 3 DDRA_SMA7

RP46 0_0404_4P2R_5%
DDRA_ADD4 1 4 DDRA_SMA4
DDRA_ADD6 2 3 DDRA_SMA6

RP47 0_0404_4P2R_5%
DDRA_ADD8 1 4 DDRA_SMA8
DDRA_ADD11 2 3 DDRA_SMA11

RP50 0_0404_4P2R_5%
DDRA_ADD9 1 4 DDRA_SMA9
DDRA_ADD12 2 3 DDRA_SMA12

RP102 0_0404_4P2R_5%
DDRA_ADD15 1 4 DDRA_SMA15
DDRA_ADD14 2 3 DDRA_SMA14

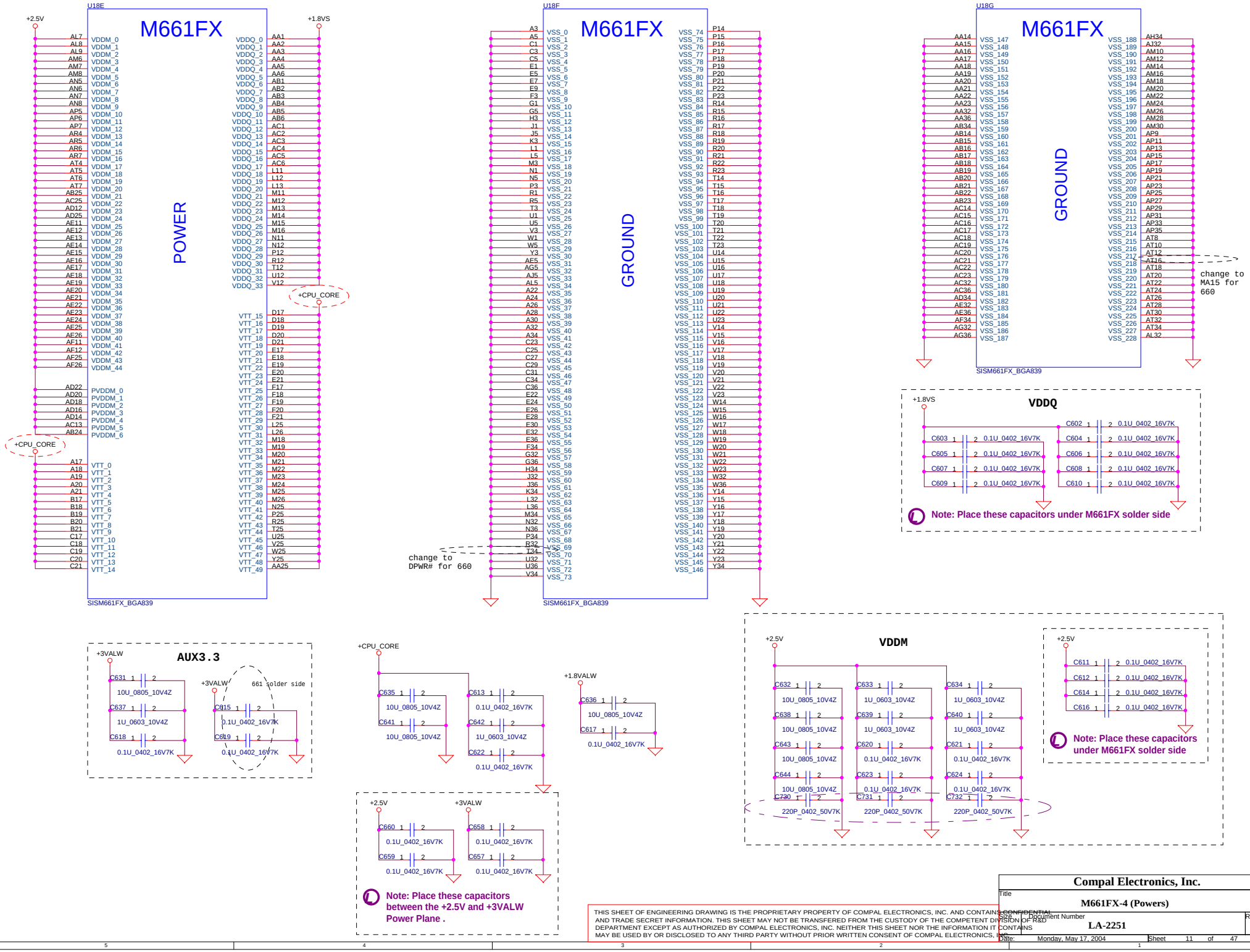
DDRA_RAS#	R230	0_0402_5%	DDR_RAS#	DDR_RAS# 14,15
DDRA_CAS#	R231	0_0402_5%	DDR_CAS#	DDR_CAS# 14,15
DDRA_WE#	R232	0_0402_5%	DDR_WE#	DDR_WE# 14,15
DDRA_CKE0	R233	0_0402_5%	DDR_CKE0	DDR_CKE0 14,15
DDRA_CKE1	R234	0_0402_5%	DDR_CKE1	DDR_CKE1 14,15
DDRA_CKE2	R235	0_0402_5%	DDR_CKE2	DDR_CKE2 14,15
DDRA_CKE3	R236	0_0402_5%	DDR_CKE3	DDR_CKE3 14,15
DDRA_CS#0	R237	0_0402_5%	DDR_CS#0	DDR_CS#0 14,15
DDRA_CS#1	R238	0_0402_5%	DDR_CS#1	DDR_CS#1 14,15
DDRA_CS#2	R239	0_0402_5%	DDR_CS#2	DDR_CS#2 14,15
DDRA_CS#3	R240	0_0402_5%	DDR_CS#3	DDR_CS#3 14,15

40 ohms R259 +2.5V DDRCOMN 40.2_0402_1%
40 ohms R264 DDRCOMP 40.2_0402_1%

+2.5V 0.01U_0402_16V7K C391 R255 150_0402_1% DDRVREFB C396 R262 150_0402_1% 0.01U_0402_16V7K
+2.5V 0.01U_0402_16V7K C392 R256 150_0402_1% DDRVREFA C397 R263 150_0402_1% 0.01U_0402_16V7K

+3VS L30 0_0603_5% DLLAVDD C388 0.1U_0402_16V7K C389 0.01U_0402_16V7K C390 10U_0805_10V4Z DLLAVSS
+3VS L31 0_0603_5% DDRAVDD C393 0.1U_0402_16V7K C394 0.01U_0402_16V7K C395 10U_0805_10V4Z DDRAVSS

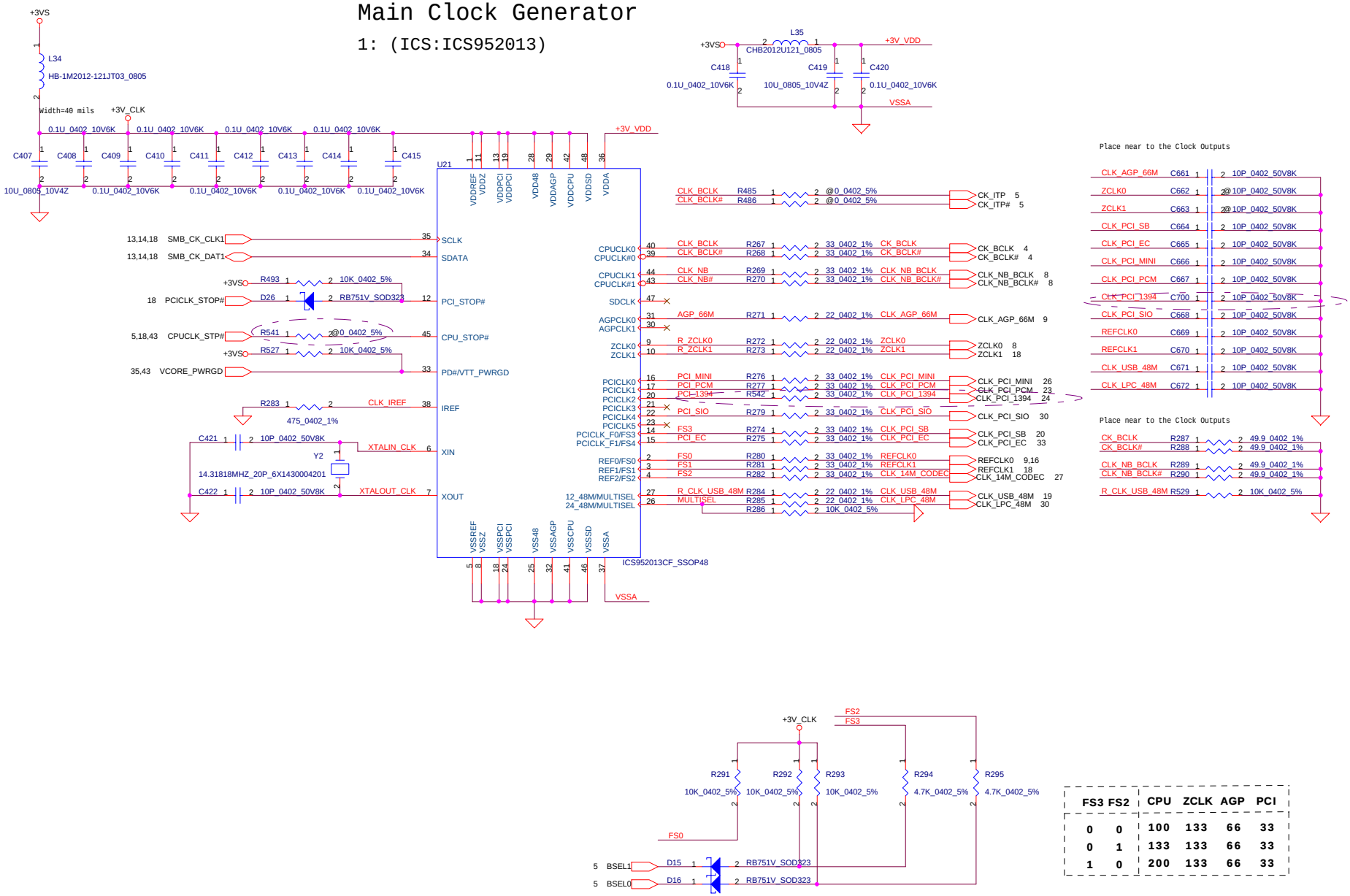
Compal Electronics, Inc.
Title: M661FX-2 (MEMORY for DDR)
Size: C | Document Number: LA-2251 | Rev: 1.0
Date: Monday, May 17, 2004 | Sheet 10 of 47



Compal Electronics, Inc.		
Title: M661FX-4 (Powers)		
Size: C	Document Number: LA-2251	Rev: 1.0
Date: Monday, May 17, 2004	Sheet 11 of 47	

Main Clock Generator

1: (ICS:ICS952013)



FS3	FS2	CPU	ZCLK	AGP	PCI
0	0	100	133	66	33
0	1	133	133	66	33
1	0	200	133	66	33

Compal Electronics, Inc.

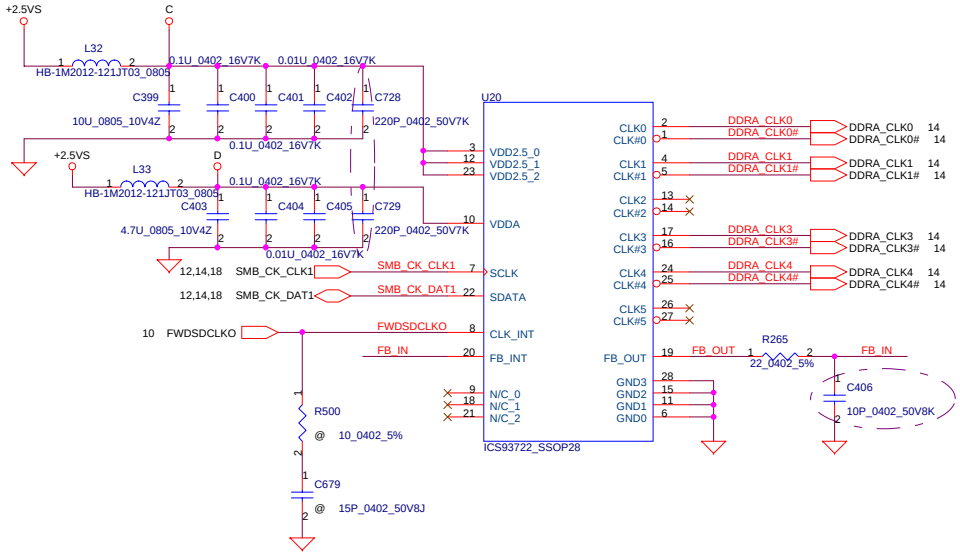
Title: **Clock Generator**

Size: C | Document Number: **LA-2251** | Rev: 1.0

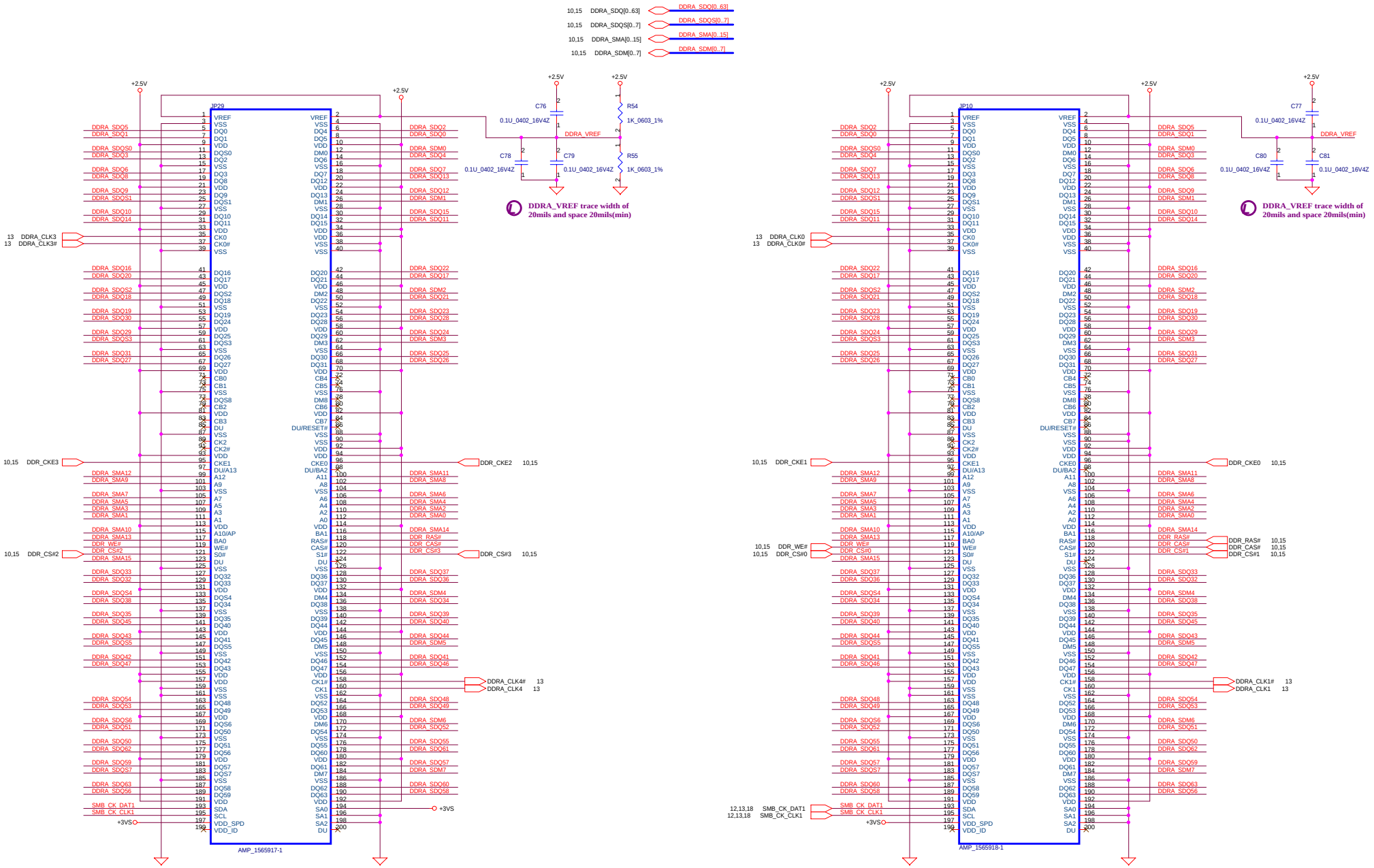
Date: Monday, May 17, 2004 | Sheet 12 of 47

Clock Buffer (DDR)

1:(ICS:ICS93722)

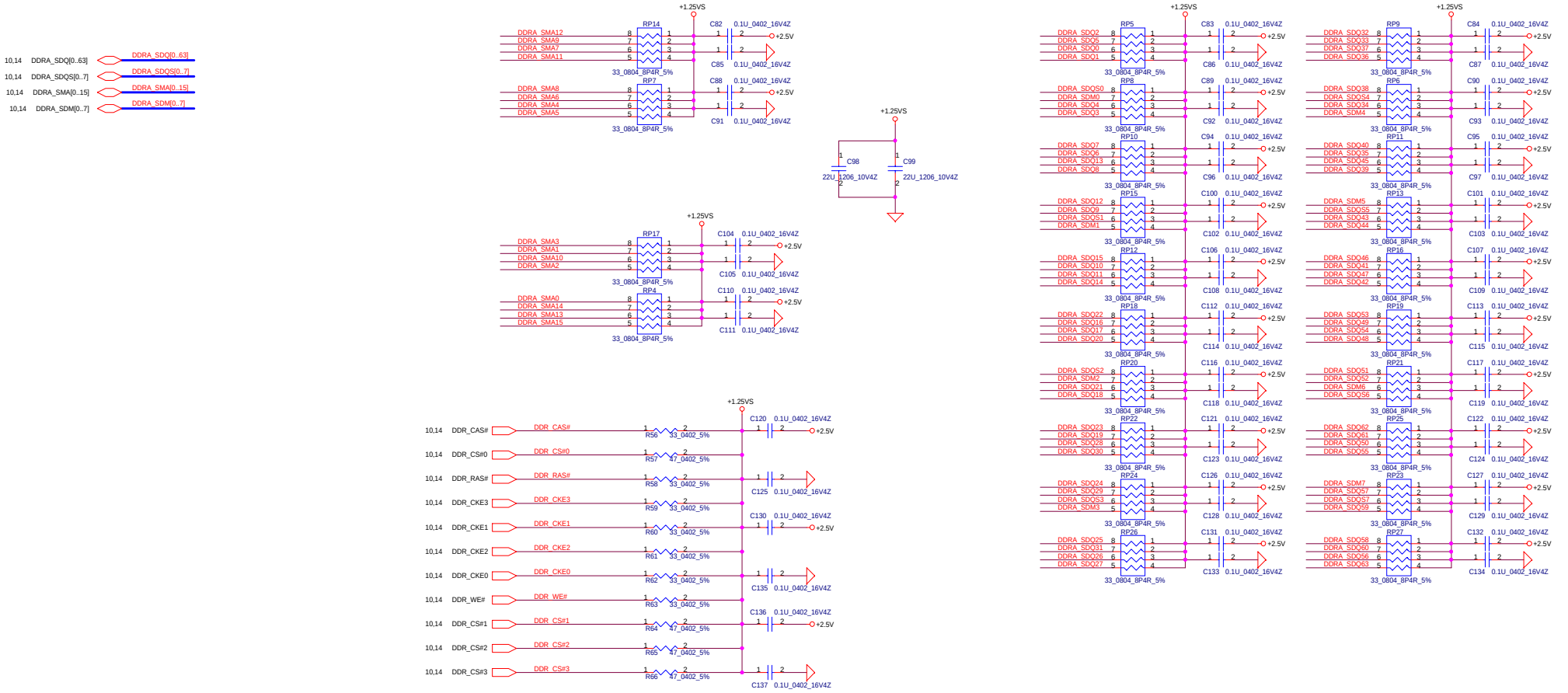


Compal Electronics, Inc.		
Title: DDR Clock Buffer		
Size: C	Document Number: LA-2251	Rev: 1.0
Date: Monday, May 17, 2004	Sheet 13 of 47	

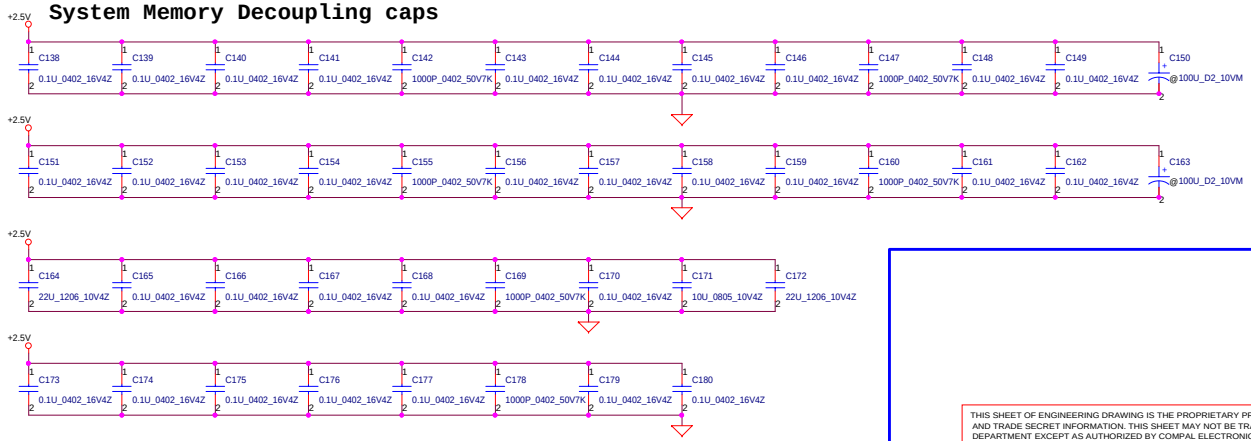


Compal Electronics, Inc.		
Title: DDR-SODIMM SLOT1		
Size:	Document Number: LA-2251	Rev: 1.0
Date: Monday, May 17, 2004	Sheet 14 of 47	

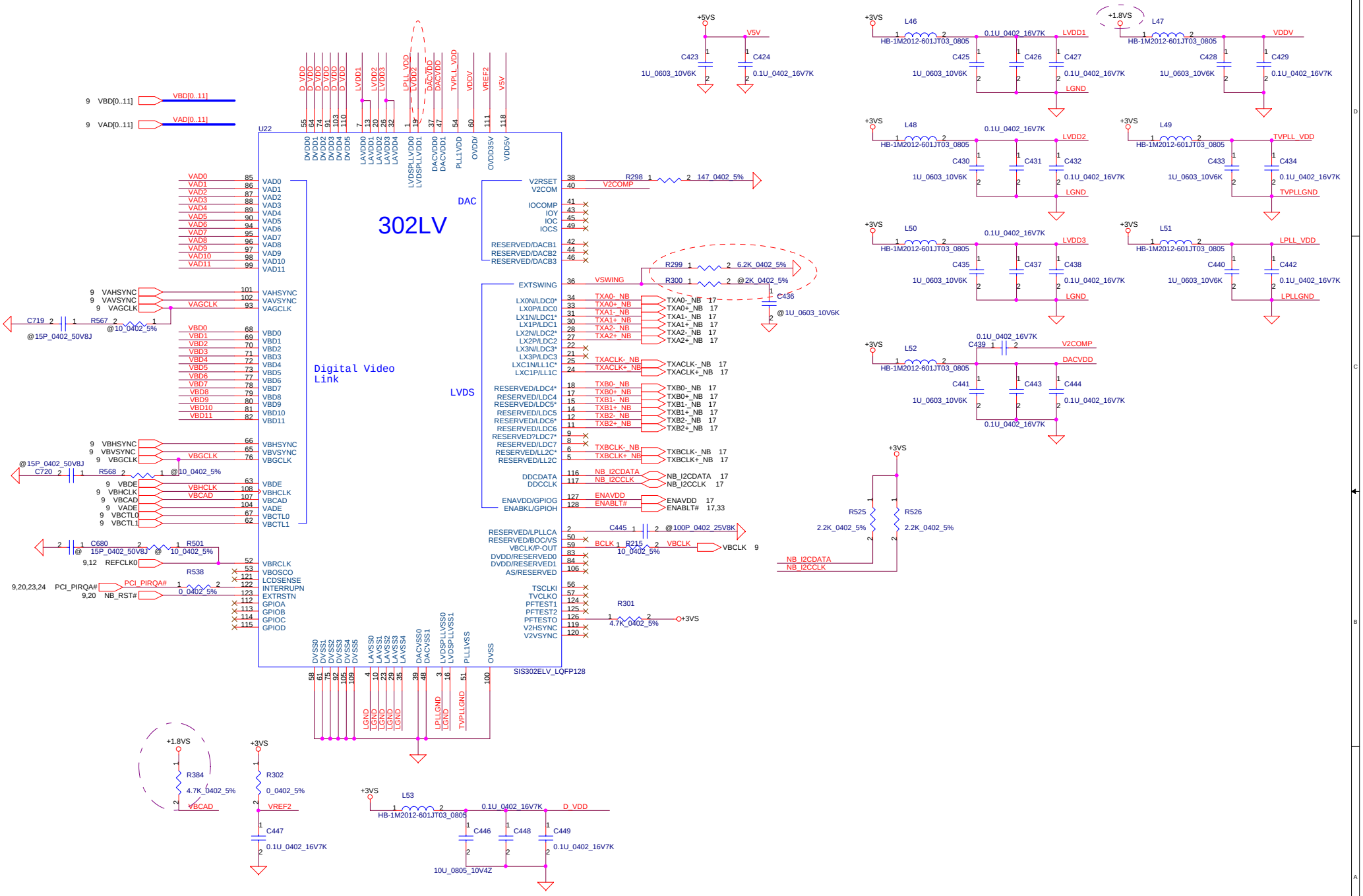
DDR Termination resistors & Decoupling caps



System Memory Decoupling caps



Compal Electronics, Inc.		
Title: DDR Termination Resistors		
Size:	Document Number: LA-2251	Rev: 1.0
Date: Monday, May 17, 2004	Sheet 15 of 47	



Compal Electronics, Inc.	
Title	LVDS/TV ENCODER
Size	C
Document Number	LA-2251
Rev	1.0
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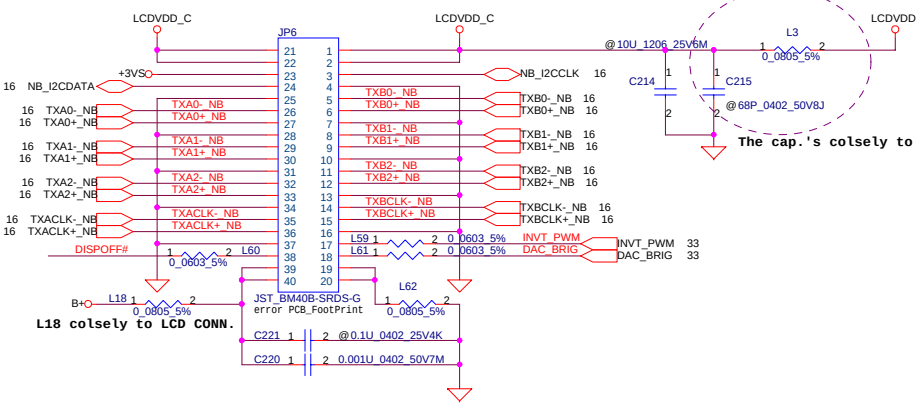
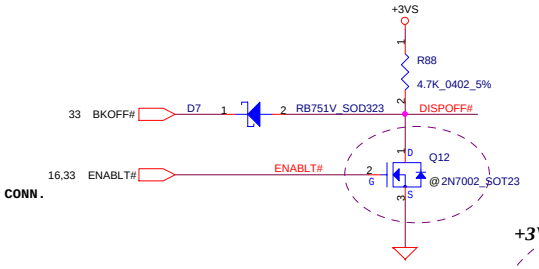
Sheet	16 of 47

LCD CONN

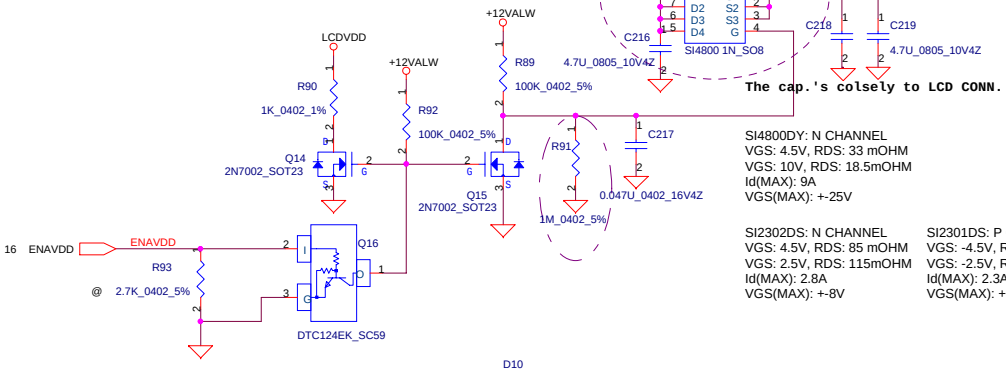


L18 colsely to LCD CONN.

The cap.'s colsely to LCD CONN.



+3VS to LCDVDD Transfer



The cap.'s colsely to LCD CONN.

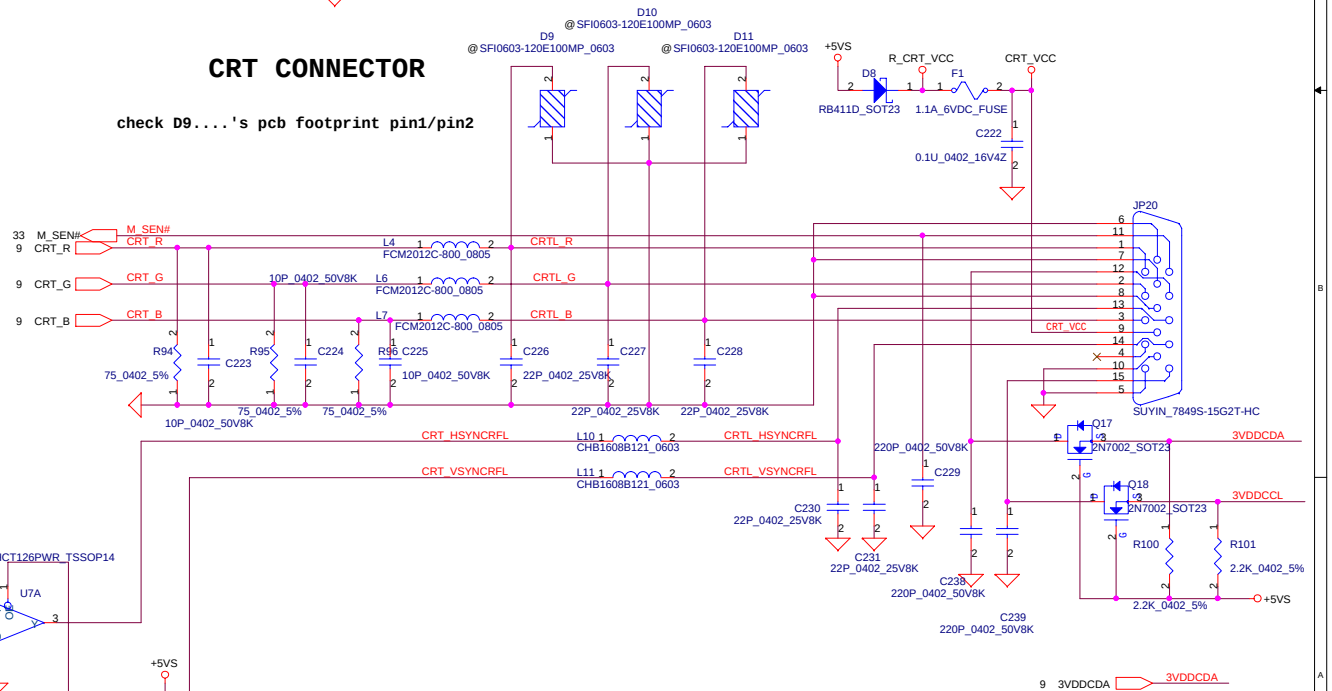
SI4800DY: N CHANNEL
VGS: 4.5V, RDS: 33 mOHM
VGS: 10V, RDS: 18.5mOHM
Id(MAX): 9A
VGS(MAX): +-25V

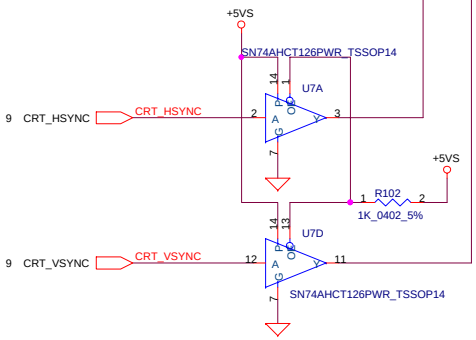
SI2302DS: N CHANNEL
VGS: 4.5V, RDS: 85 mOHM
VGS: 2.5V, RDS: 115mOHM
Id(MAX): 2.8A
VGS(MAX): +-8V

SI2301DS: P CHANNEL
VGS: -4.5V, RDS: 130 mOHM
VGS: -2.5V, RDS: 190mOHM
Id(MAX): 2.3A
VGS(MAX): +-8V

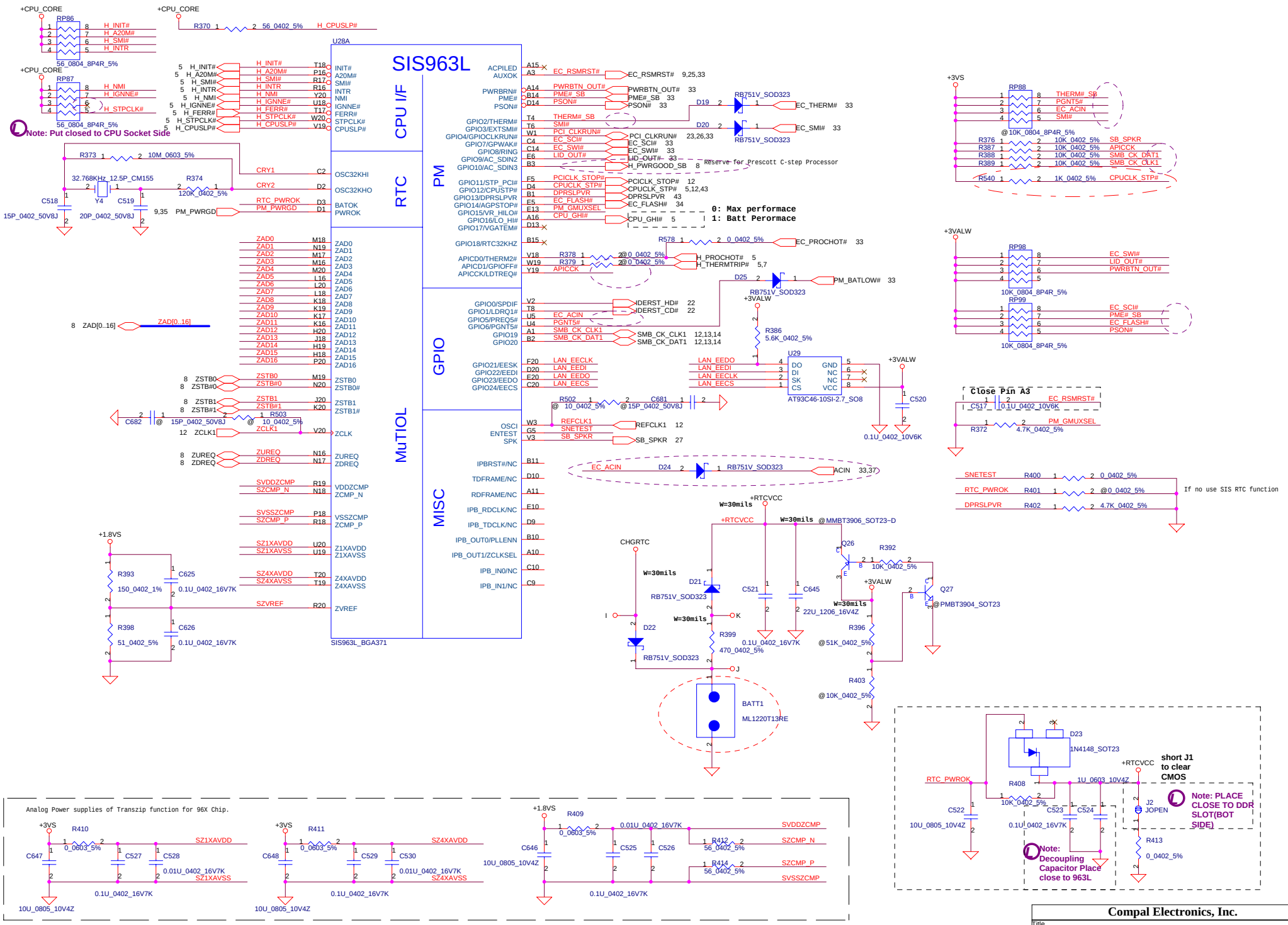
CRT CONNECTOR

check D9....'s pcb footprint pin1/pin2

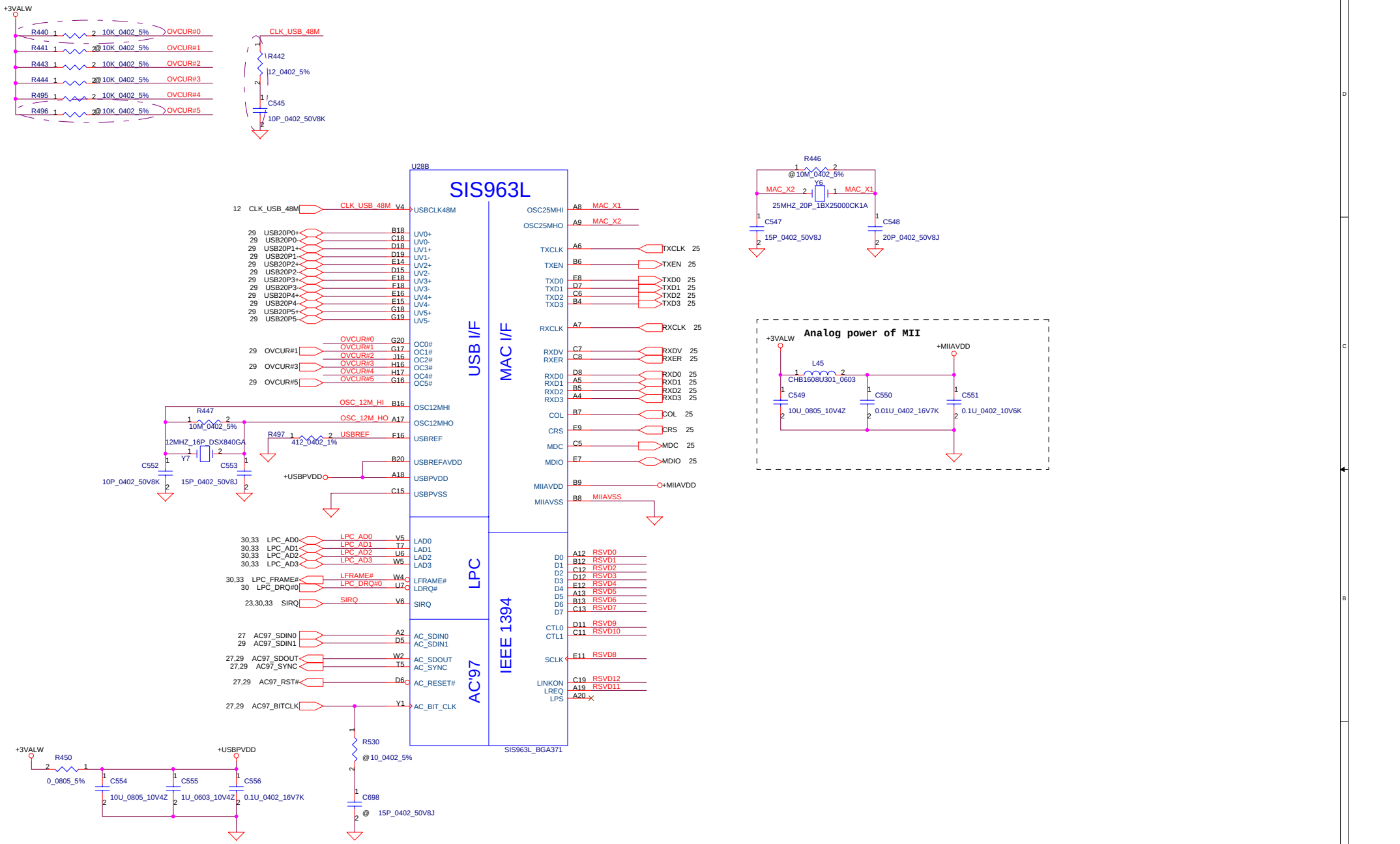




Compal Electronics, Inc.		
Title: LCD/Inverter BD & CRT CONN.		
Size: C	Document Number: LA-2251	Rev: 1.0
Custom		
Date: Monday, May 17, 2004	Sheet 17 of 47	



Compal Electronics, Inc.	
Title	963L-1 (HOST/MuTIOL/RTC/GPIO/MISC)
Size	Document Number: LA-2251
Rev	1.0
Date:	Monday, May 17, 2004
Sheet	18 of 47

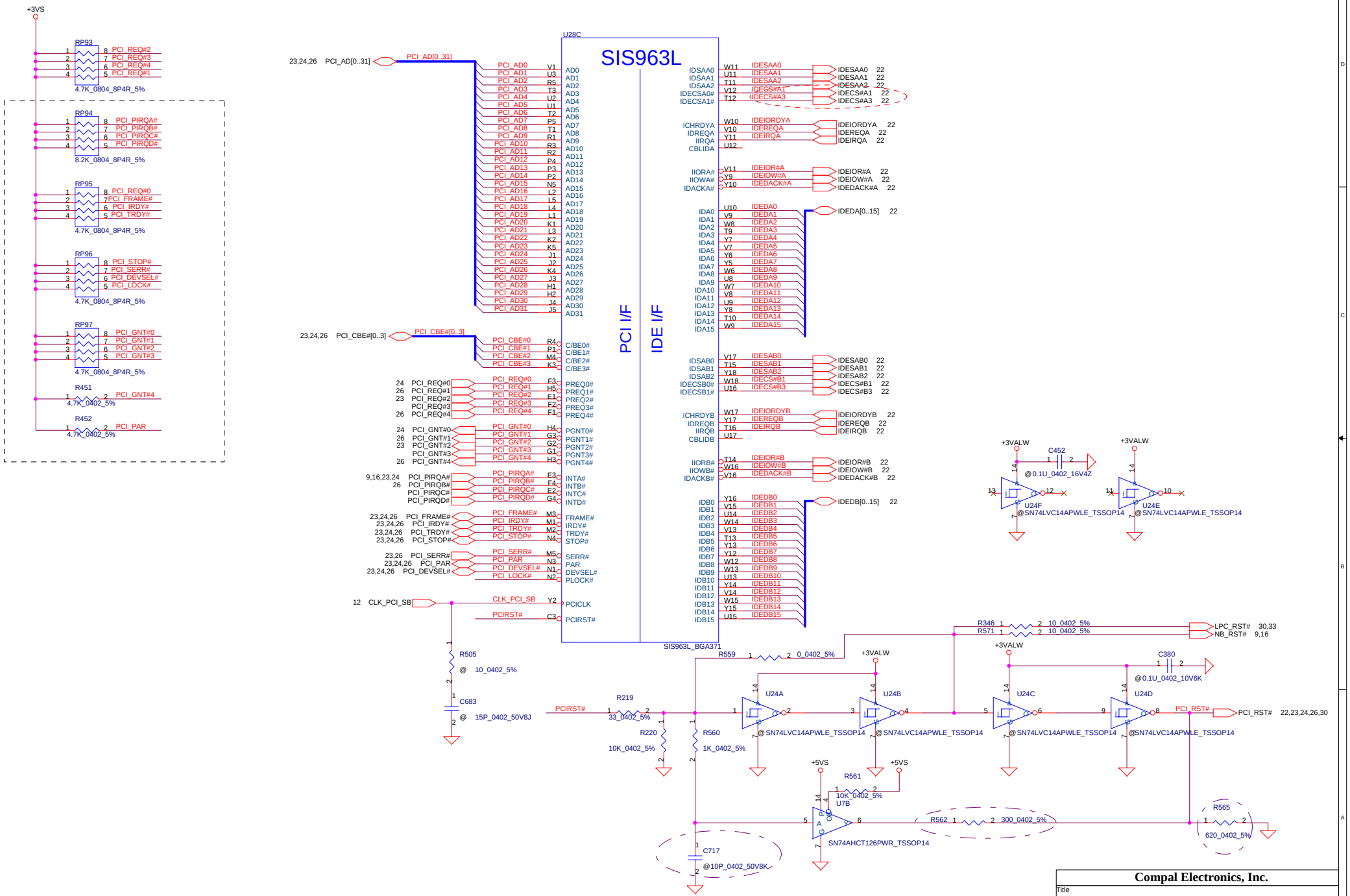


Compal Electronics, Inc.

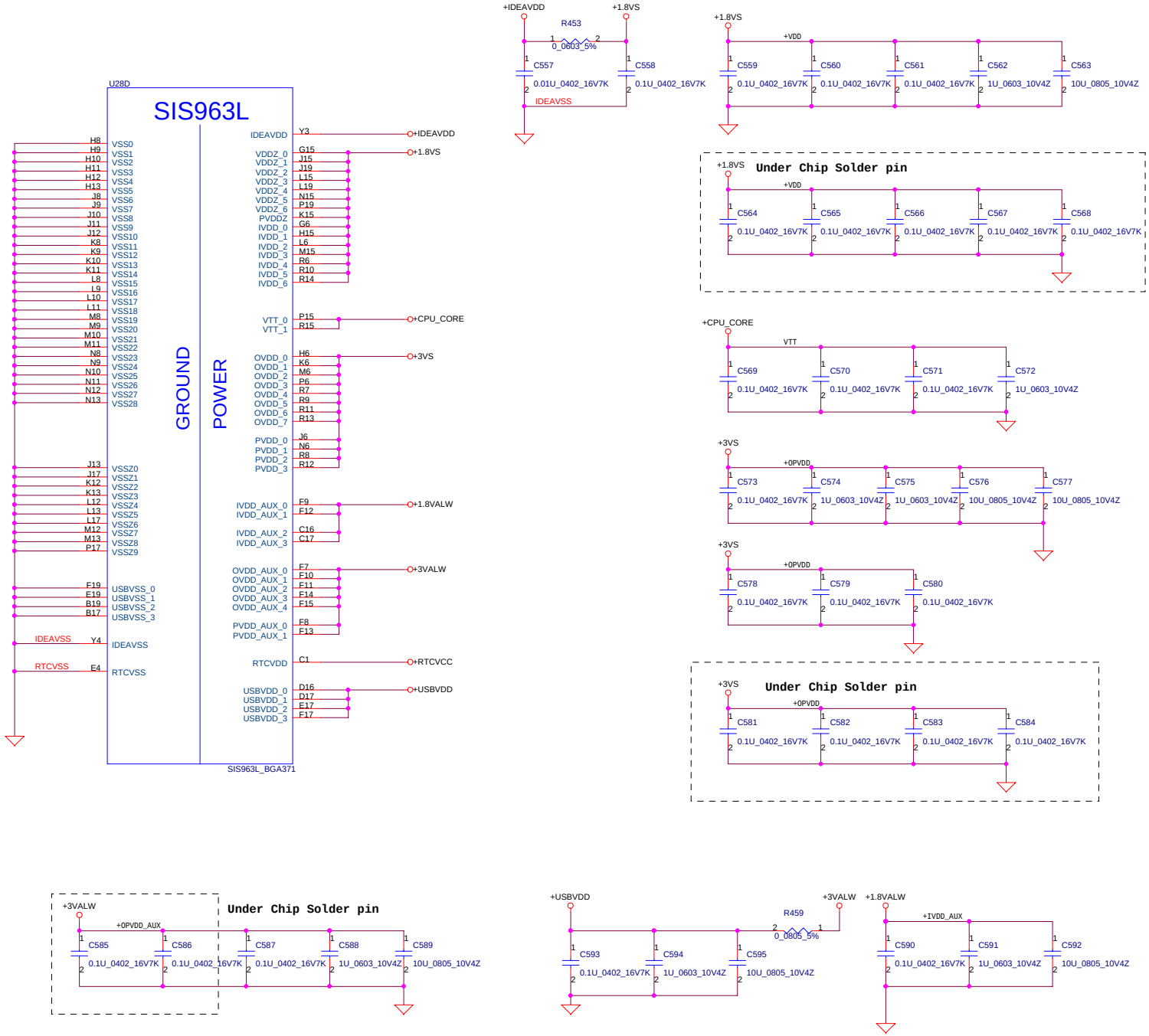
Title: **963L-2 (USB/LPC/AC97/1394/MAC)**

Size: C | Document Number: **LA-2251** | Rev: 1.0

Date: Monday, May 17, 2004 | Sheet 19 of 47



Compal Electronics, Inc.	
Title	963L-3 (PCI/IDE)
Size C	Document Number LA-2251
Rev	1.0
Date: Monday, May 17, 2004	Sheet 20 of 47



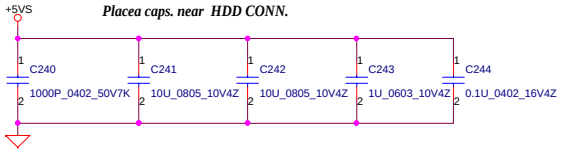
Compal Electronics, Inc.

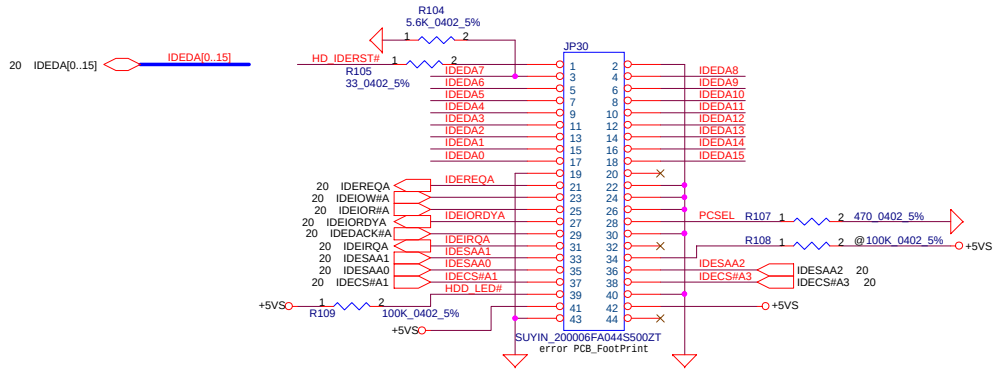
Title: **963L-3 (POWER)**

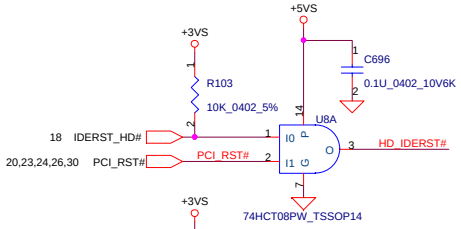
Size: C | Document Number: **LA-2251** | Rev: 1.0

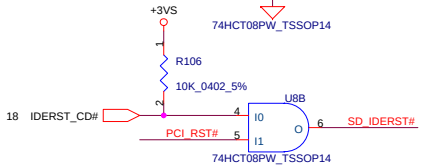
Date: Monday, May 17, 2004 | Sheet 21 of 47

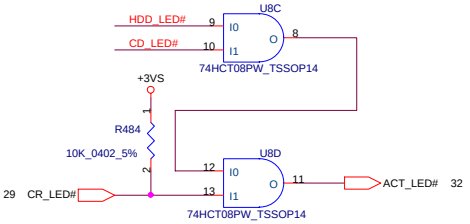
Placea caps. near HDD CONN.

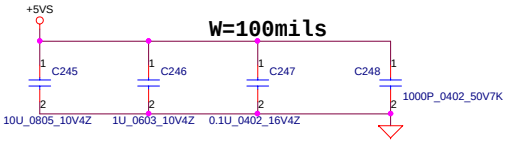






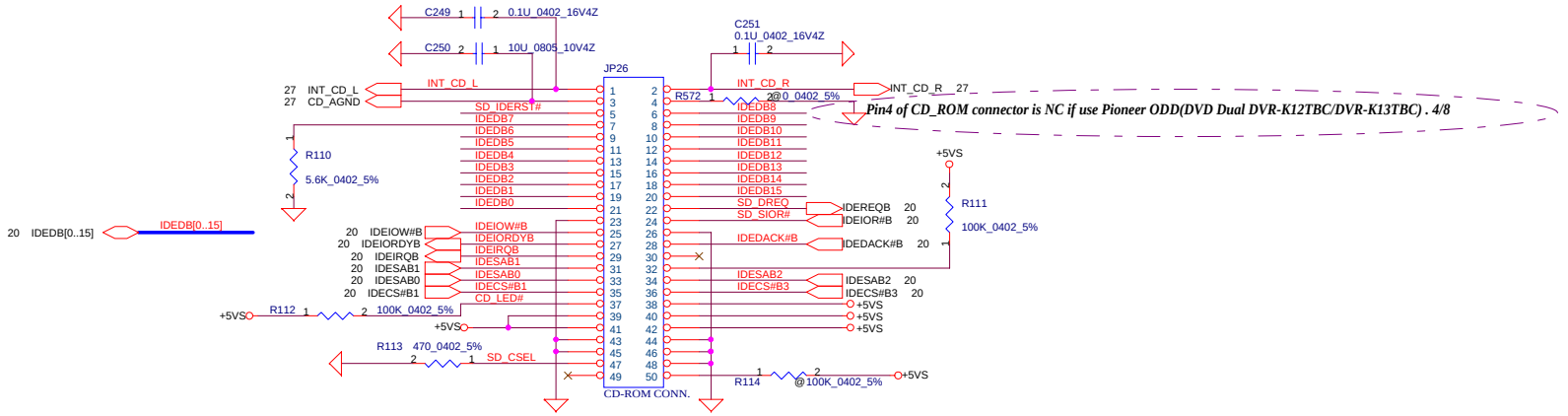






Placea caps. near CDROM CONN.

+5VS for CD trace to CONN W=100mils



	EXIT0	EXIT1
CD-ROM	0	0
2'nd HDD	0	1
NONE	1	1

Compal Electronics, Inc.

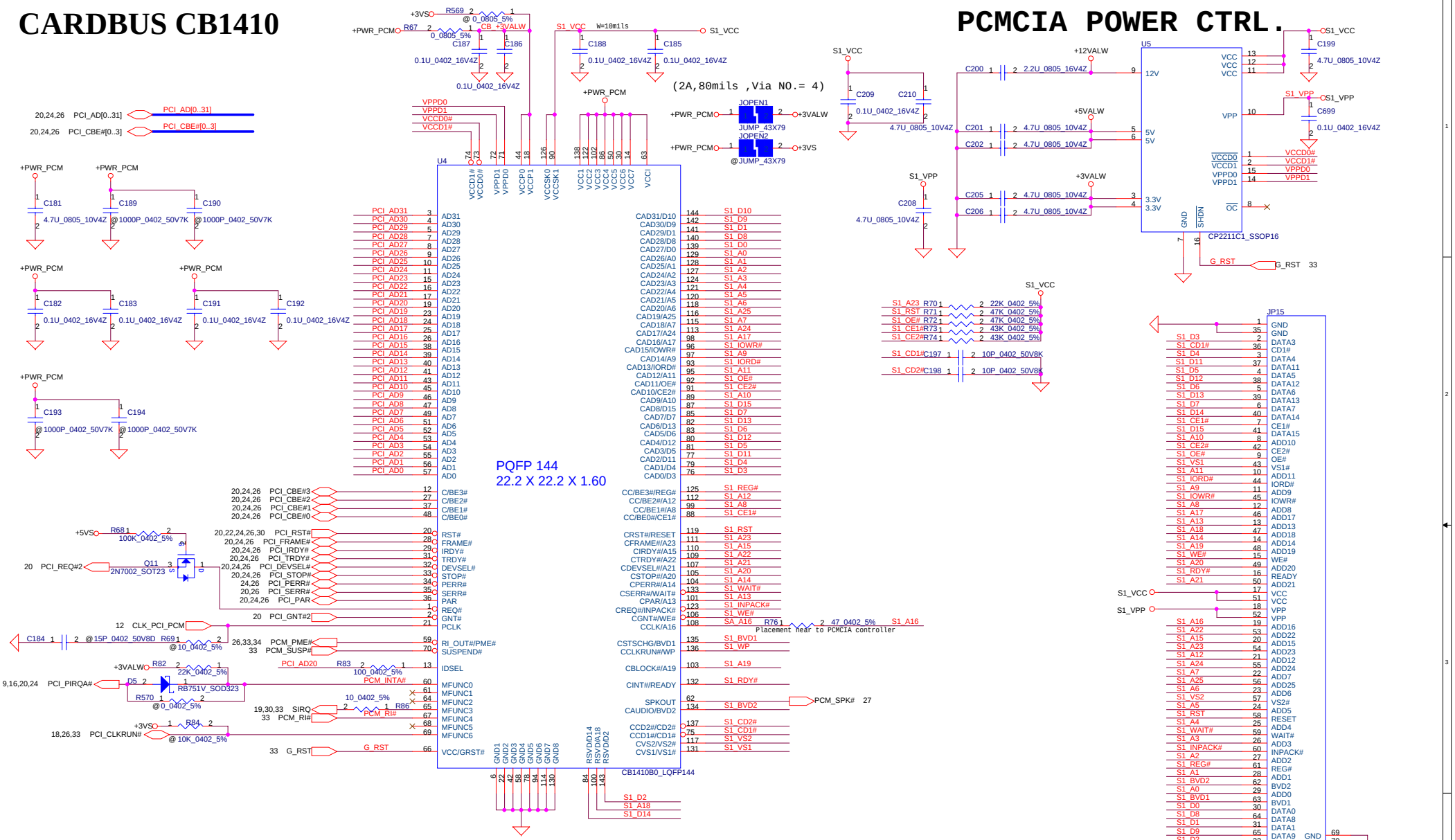
Title: **HDD & CDROM Connector**

Size: C | Document Number: **LA-2251** | Rev: 1.0

Date: Monday, May 17, 2004 | Sheet 22 of 47

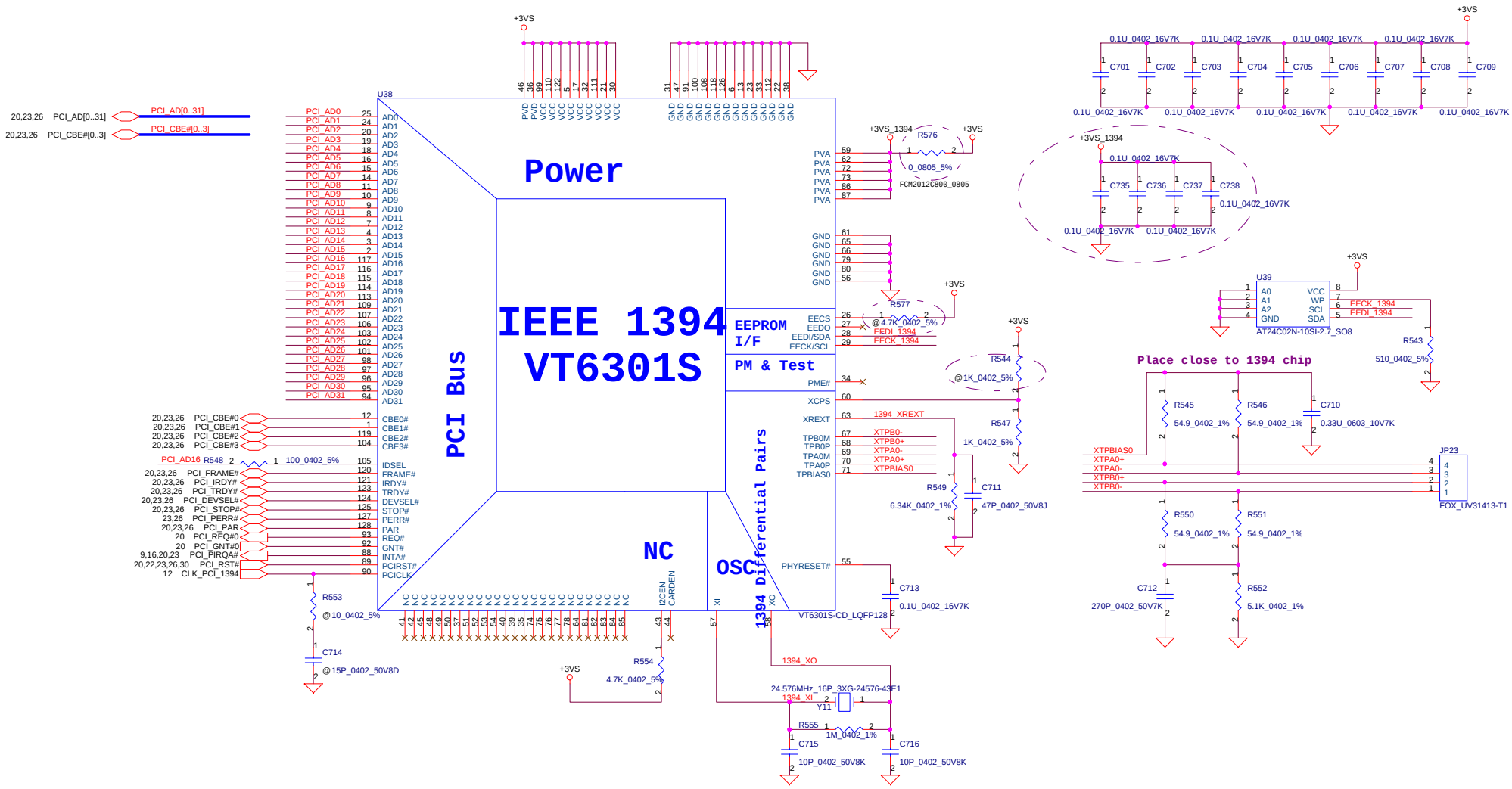
CARDBUS CB1410

PCMCIA POWER CTRL.

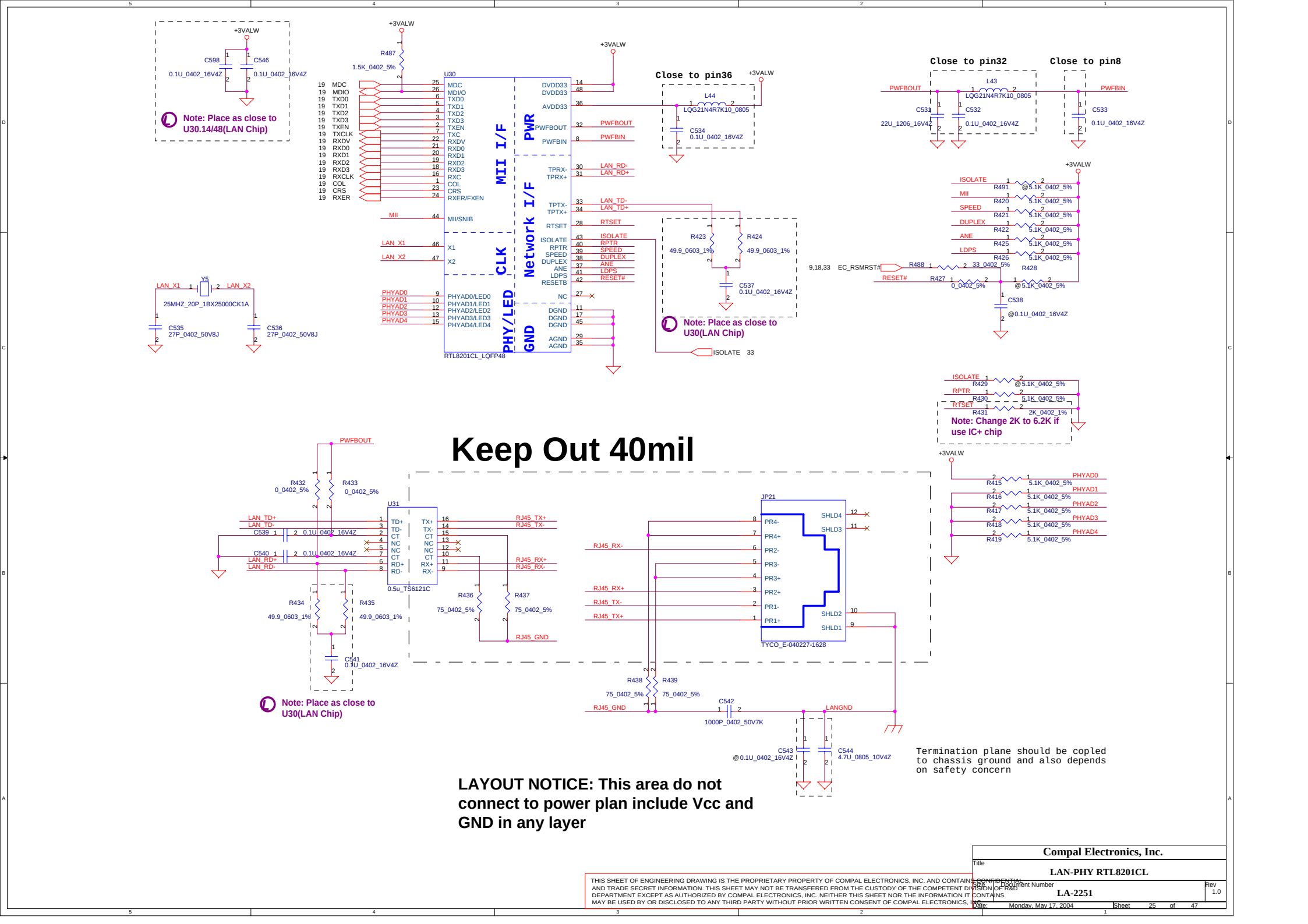


CARDBUS SOCKET

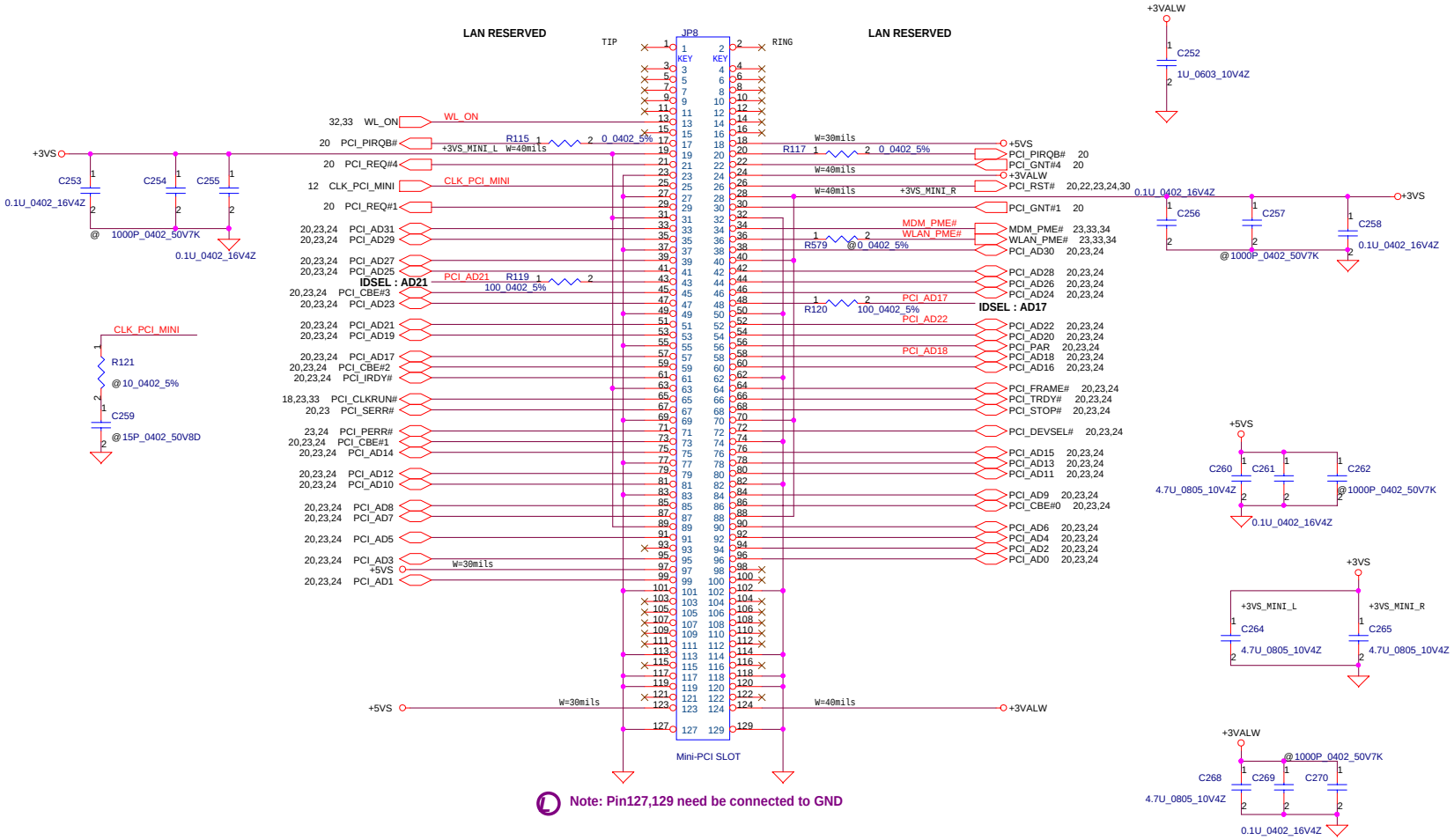
Compal Electronics, Inc.	
Title	CardBus Controller CB1410/CardBus Socket/Power Switch
Size	Document Number: LA-2251
Rev	1.0
Date: Monday, May 17, 2004	Sheet 23 of 47



Compal Electronics, Inc.	
Title	IEEE1394 Controller & PHY-VIA VT6301S
Size: C	Document Number: LA-2251
Rev: 1.0	
Date: Monday, May 17, 2004	Sheet 24 of 47



Compal Electronics, Inc.	
Title	LAN-PHY RTL8201CL
Size: C	Document Number: LA-2251
Rev	1.0
Date: Monday, May 17, 2004	Sheet 25 of 47



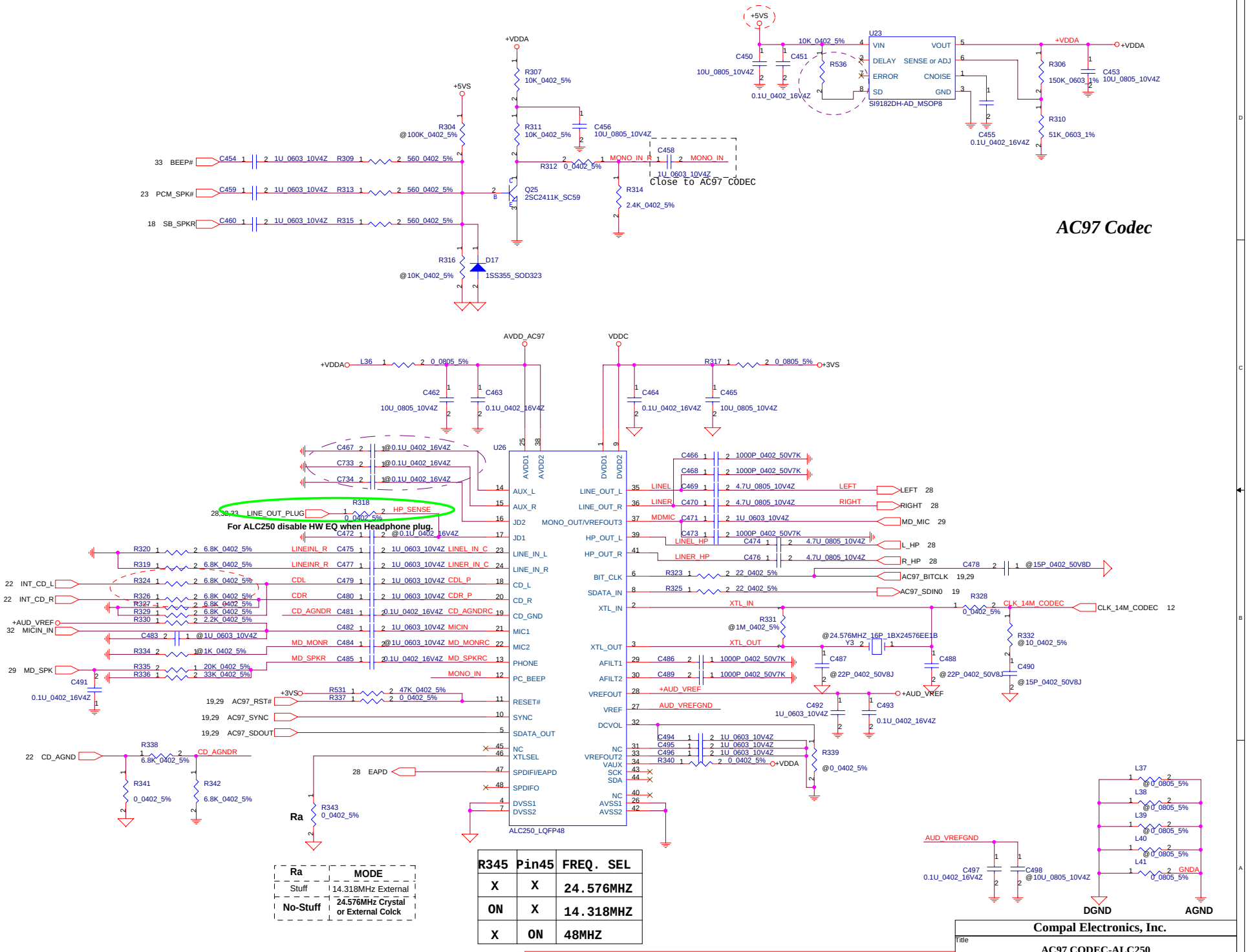
Compal Electronics, Inc.

Title: **Mini PCI Slot**

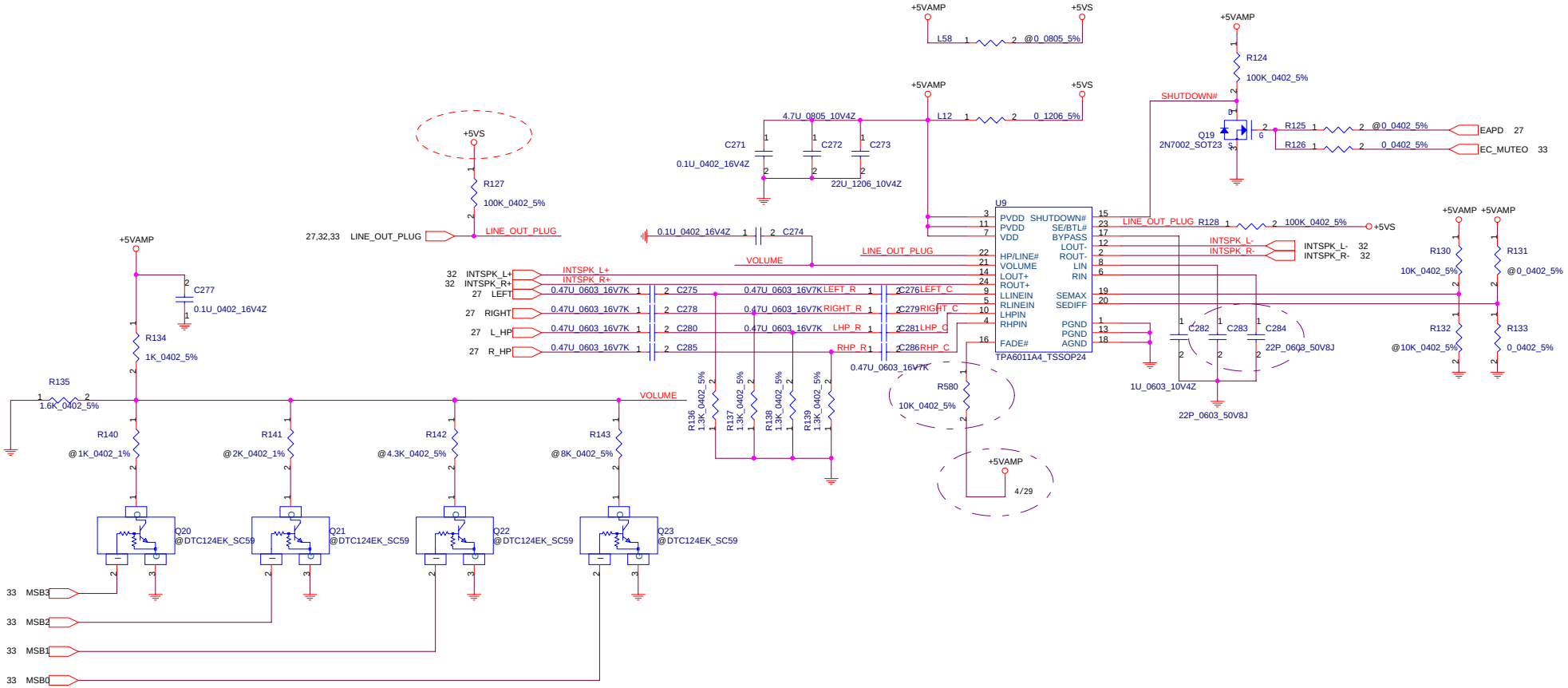
Size: C | Document Number: **LA-2251** | Rev: 1.0

Date: Monday, May 17, 2004 | Sheet 26 of 47

AC97 Codec



Compal Electronics, Inc.	
Title	AC97 CODEC-ALC250
Size: C	Document Number: LA-2251
Rev	1.0
Date: Monday, May 17, 2004	Sheet 27 of 47



MSB3	MSB2	MSB1	MSB0	Vo	BTL (dB)	SE (dB)
0	0	0	0	0		
0	0	0	1	4.7225	20	14
0	0	1	0	4.47	20	14
0	0	1	1	4.34	20	14
0	1	0	0	4.0485	20	14
0	1	0	1	3.86	20	14
0	1	1	0	3.719	20	14
0	1	1	1	3.56		
1	0	0	0	3.4	14	8
1	0	0	1	3.272	12	6
1	0	1	0	3.1659	10	4
1	0	1	1	3.05	8	2
1	1	0	0	2.938	6	0
1	1	0	1	2.84		
1	1	1	0	2.76		
1	1	1	1	2.67		

Compal Electronics, Inc.
Title: AMP & Audio Jack
Size: C
Document Number: LA-2251
Rev: 1.0
Date: Monday, May 17, 2004
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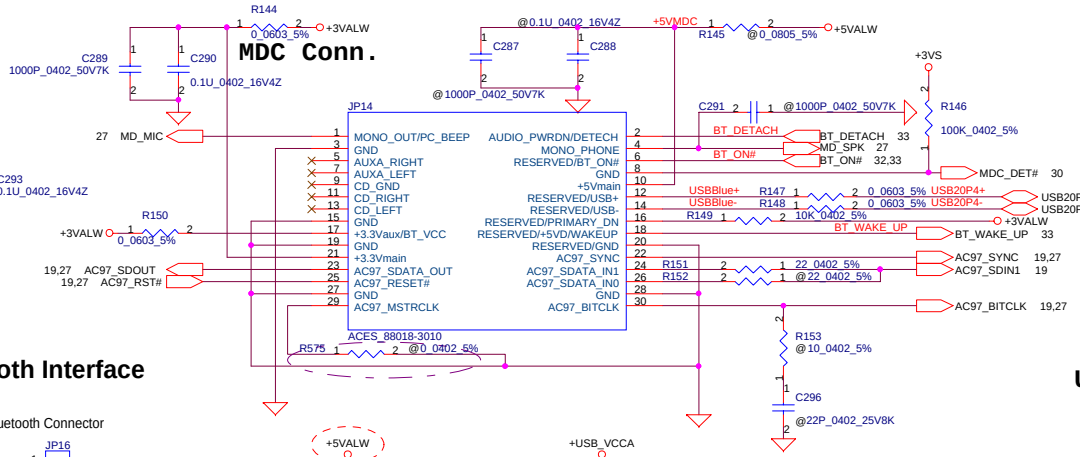
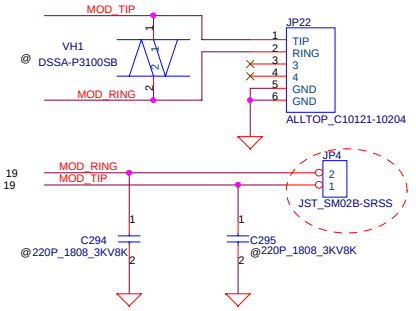
MDC Note
Pin 1 is NC for Pctel and connexant MDC modem
Pin 2 is NC for Pctel and connexant MDC modem

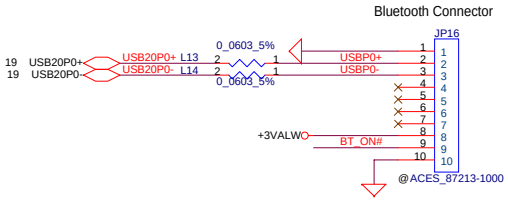
MDC Conn.

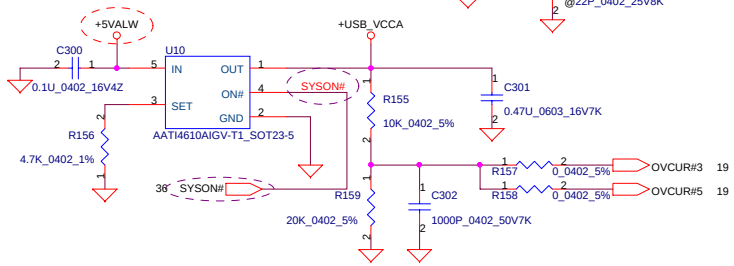


RJ11 CONN.

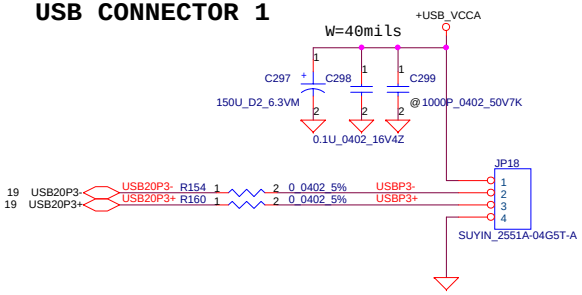


BlueTooth Interface

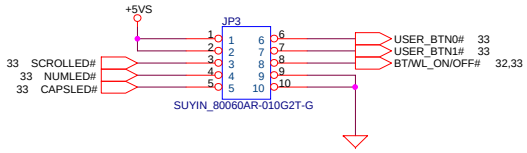


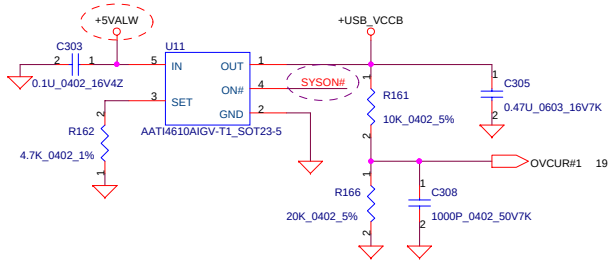


USB CONNECTOR 1



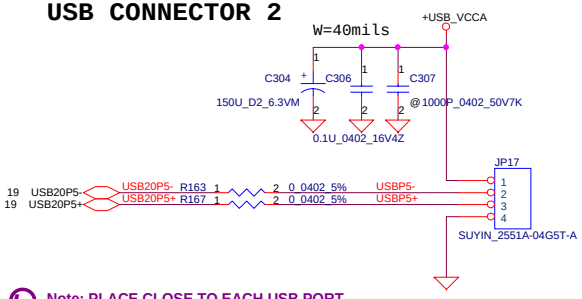
SWITCH BOARD CONN.





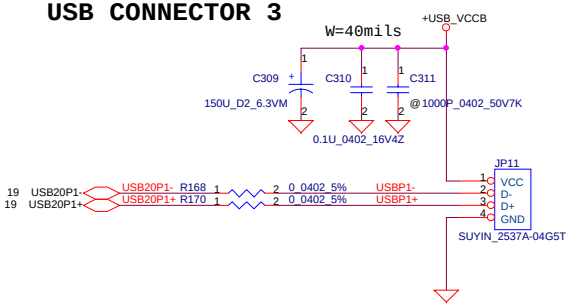
Note: PLACE CLOSE TO EACH USB PORT

USB CONNECTOR 2

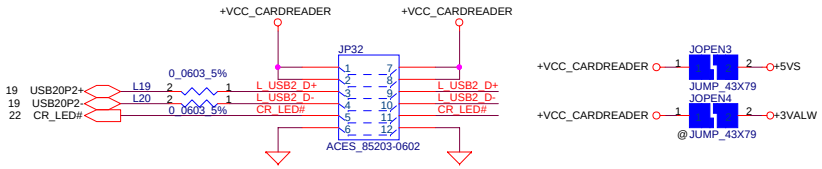


Note: PLACE CLOSE TO EACH USB PORT

USB CONNECTOR 3



5 IN 1 CONN



Compal Electronics, Inc.	
Title	MDC , Bluetooth & USB CONN.
Size	Document Number: LA-2251
Rev	1.0
Date:	Monday, May 17, 2004
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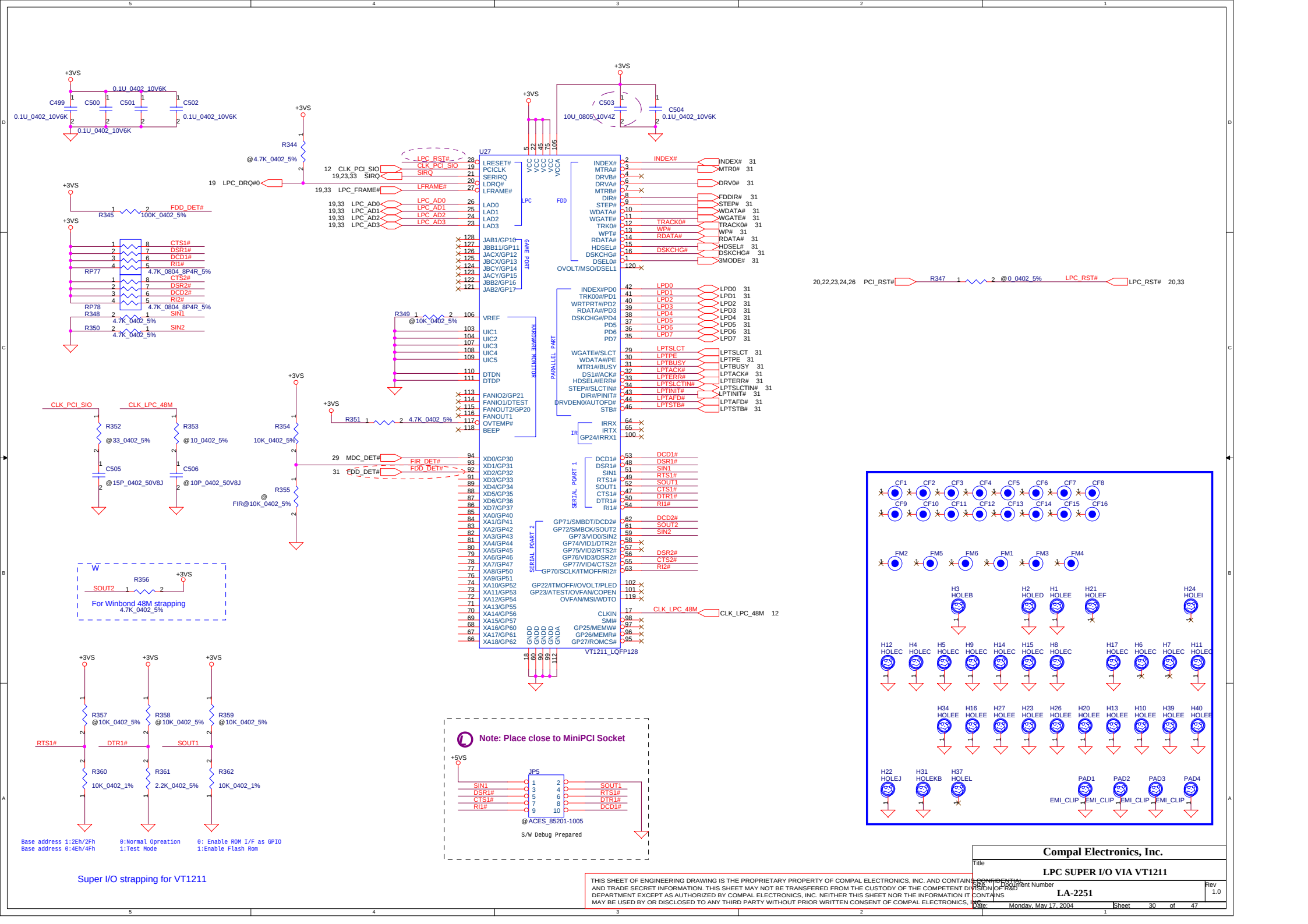

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Compal Electronics, Inc.	
Title	LPC SUPER I/O VIA VT1211
Size	Document Number: LA-2251
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Date:	Monday, May 17, 2004
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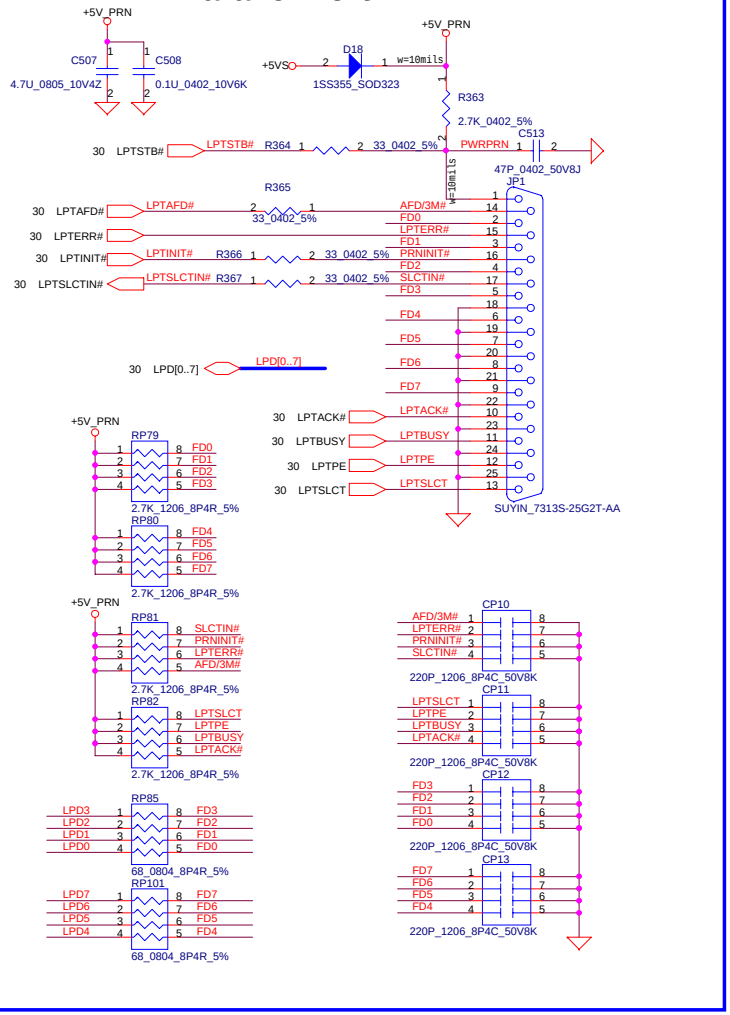
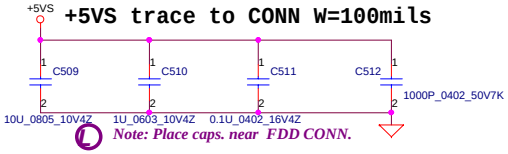
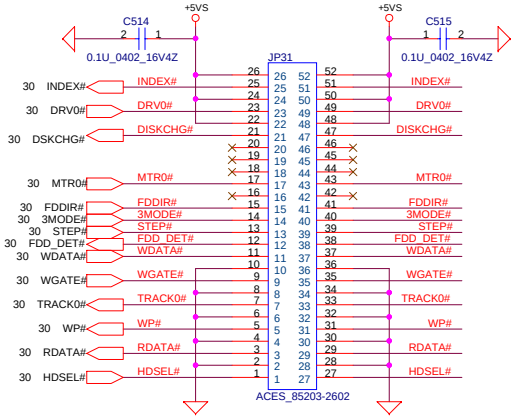
Parallel Port

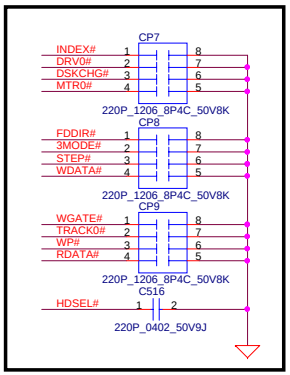


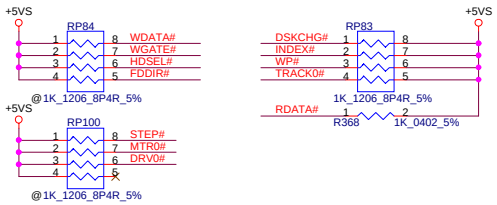
FDD CONN.





EMI Requirement





Compal Electronics, Inc.

Title: Parallel port and FDD Conn.

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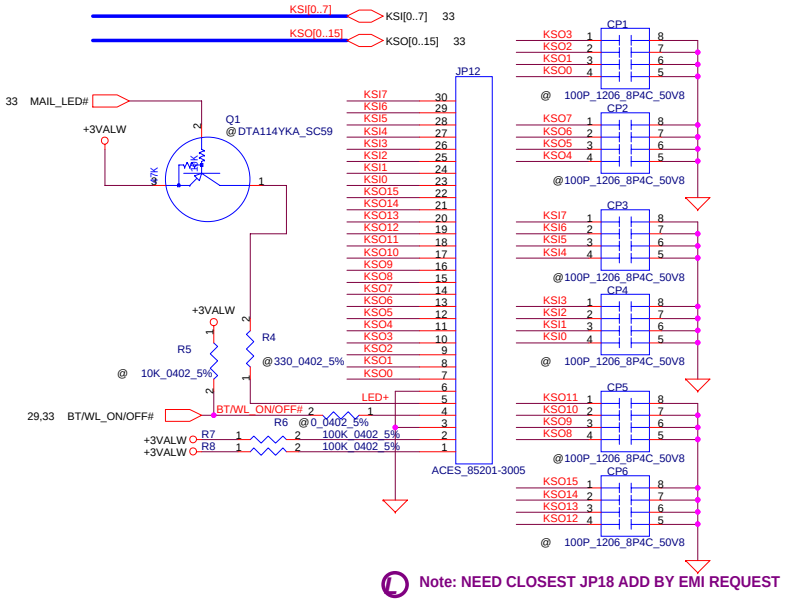
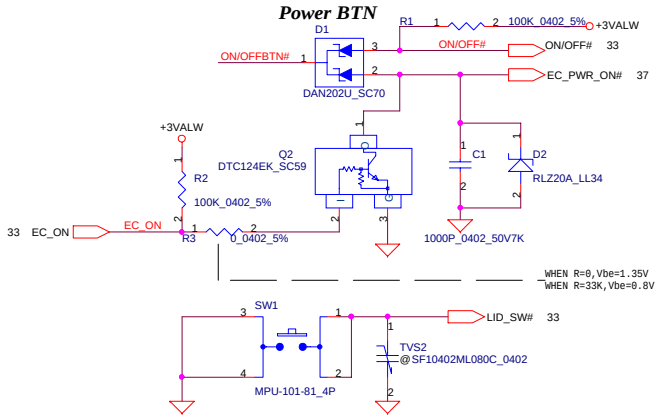
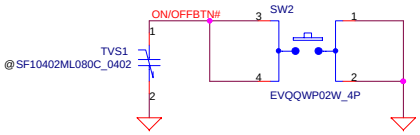
INT_KBD CONN.



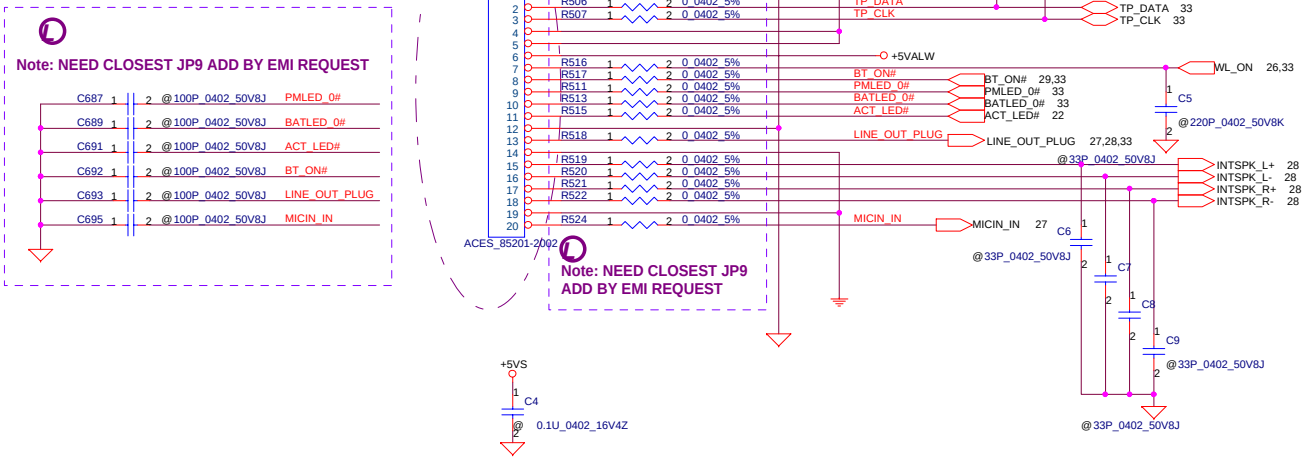
Note: NEED CLOSEST JP18 ADD BY EMI REQUEST

Power BTN





Touch Pad & Status LED Conn.



Compal Electronics, Inc.	
Title	KBD,ON/OFF,T/P & LED
Size: C	Document Number: LA-2251
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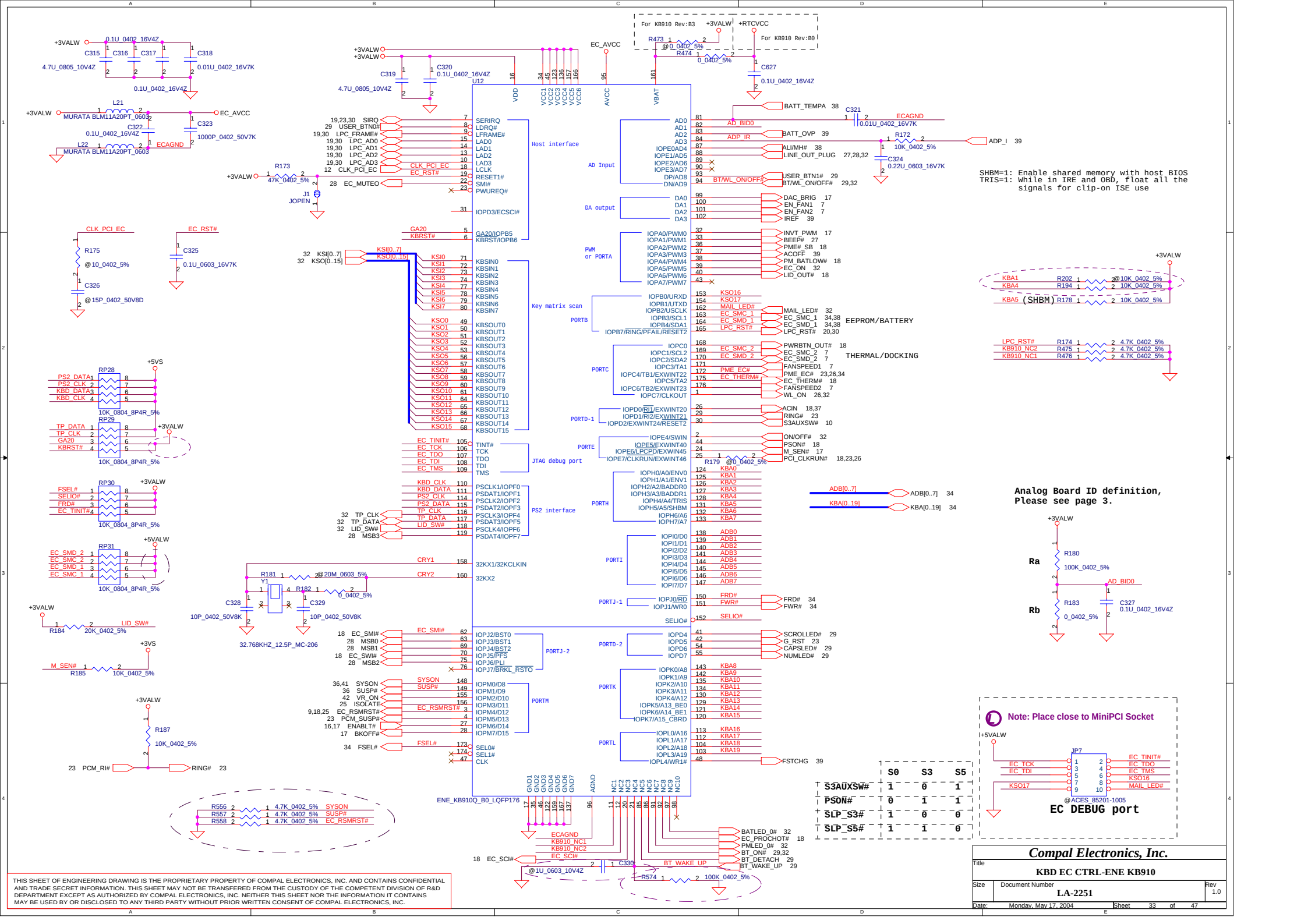
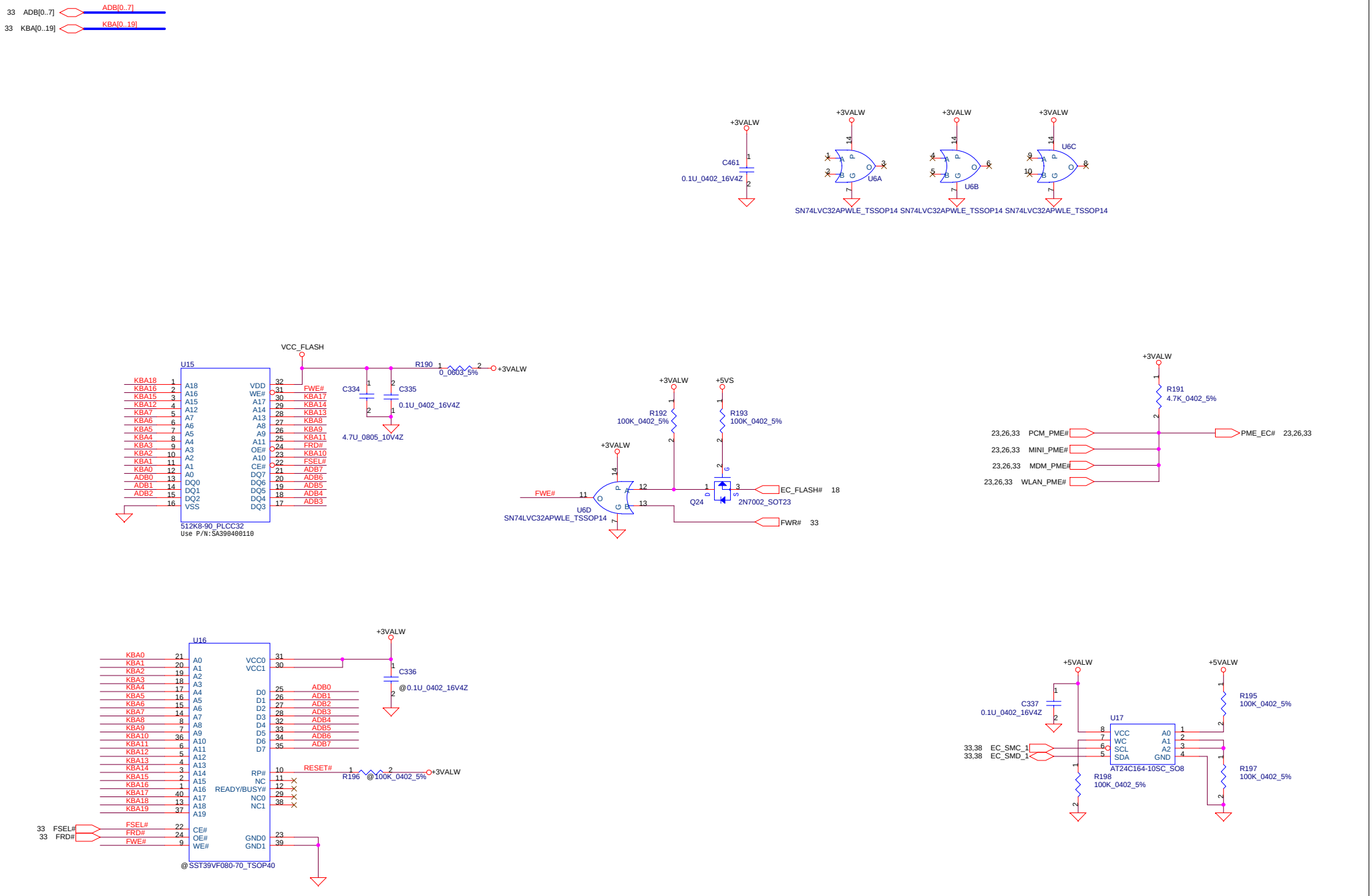
Date: Monday, May 17, 2004	Sheet 32 of 47



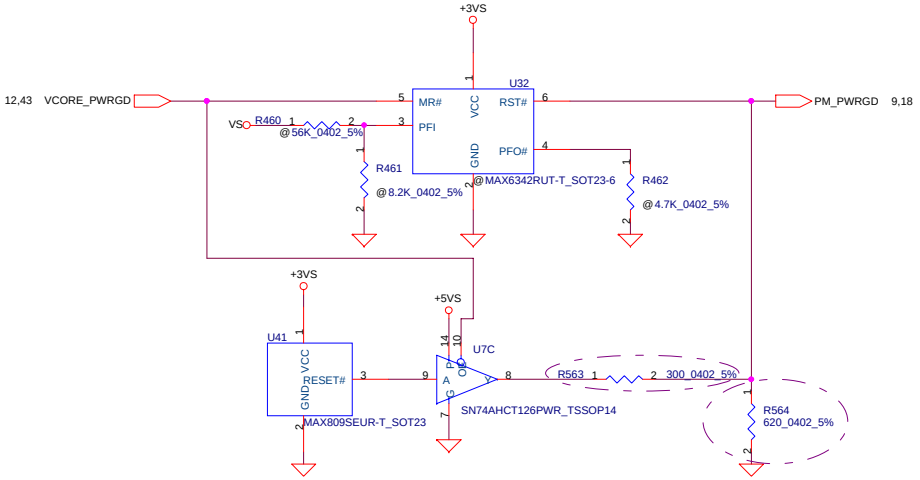


Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size: | Document Number: **LA-2251** | Rev: 1.0

Date: Monday, May 17, 2004 | Sheet 34 of 47



Compal Electronics, Inc.

Title: **RESET & PS2 Connector**

Size: C | Document Number: **LA-2251** | Rev: 1.0

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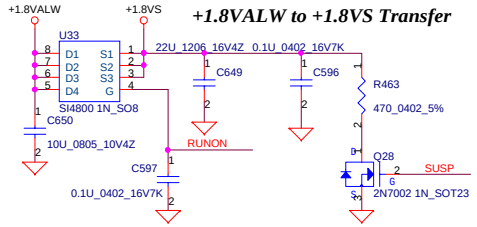
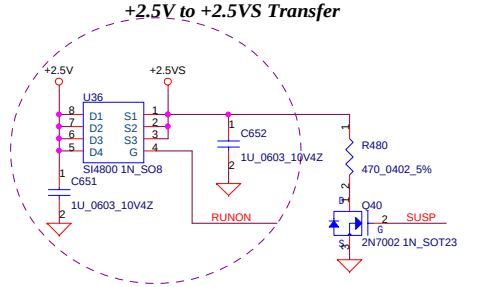
1.8VALW/+1.5VS Power direct provide

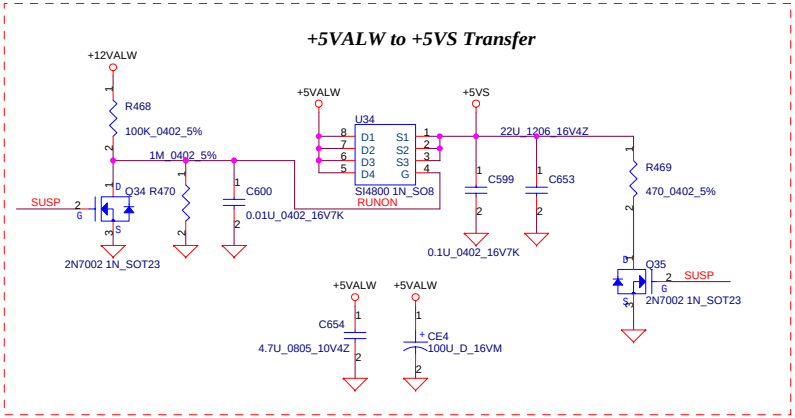
+1.8VALW to +1.8VS Transfer



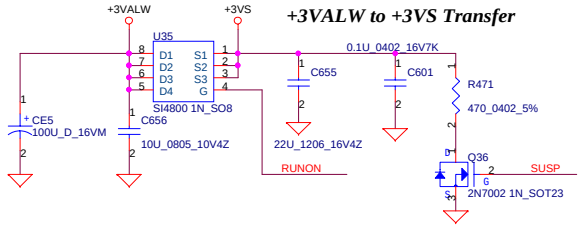
+2.5V to +2.5VS Transfer

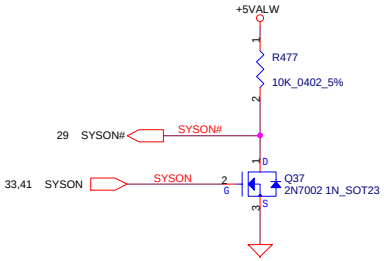


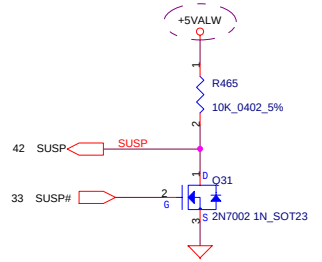
+5VALW to +5VS Transfer

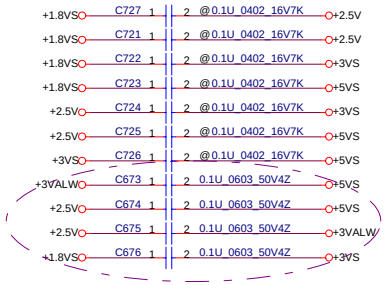


+3VALW to +3VS Transfer

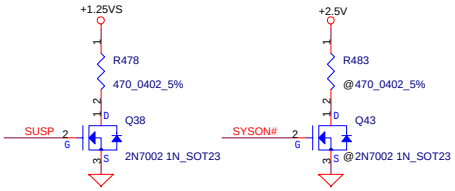








Discharge circuit



Compal Electronics, Inc.

Title: **DC/DC Circuits**

Size: C | Document Number: **LA-2251** | Rev: 1.0

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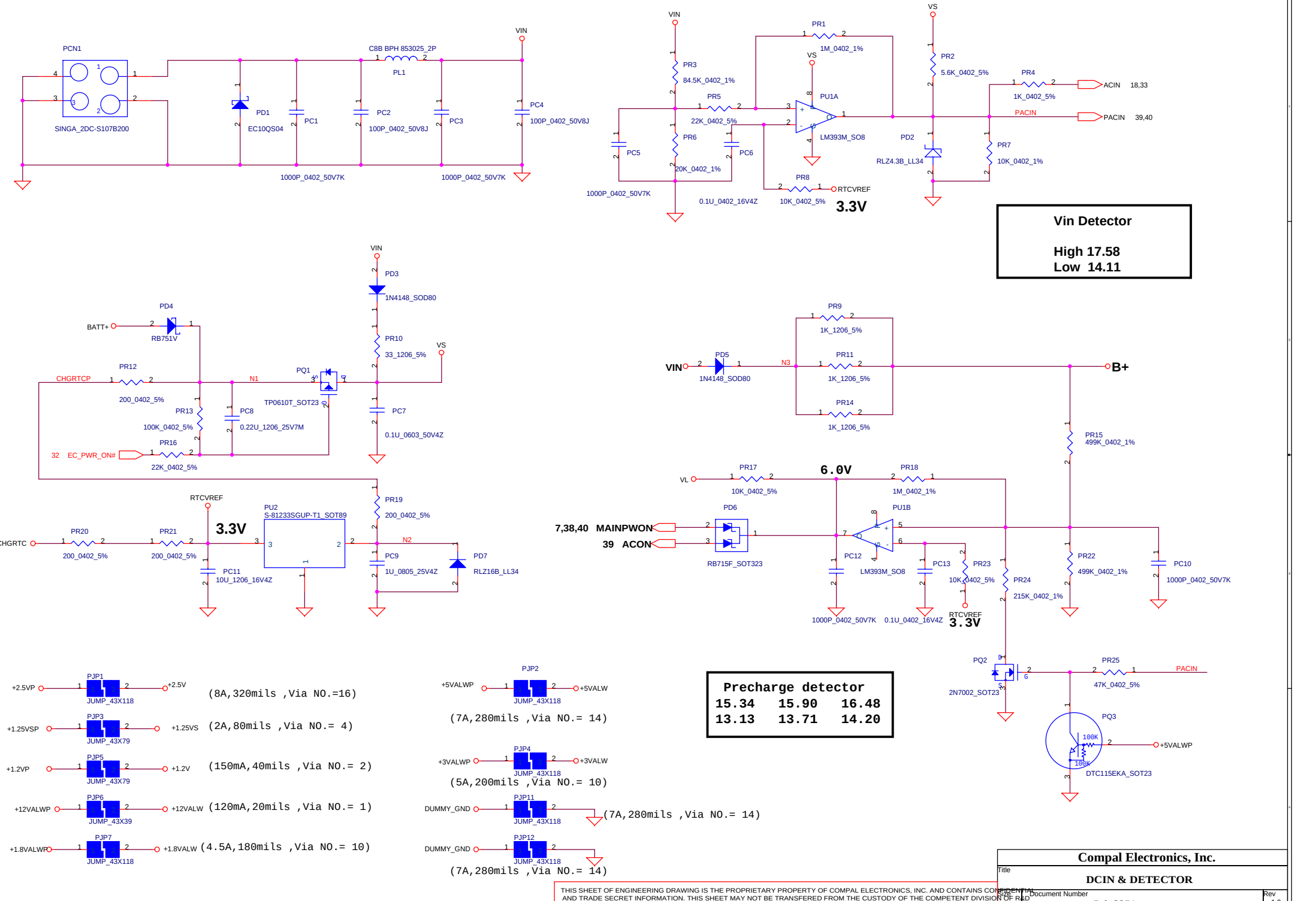

Compal Electronics, Inc.	
Title	DCIN & DETECTOR
Size	Document Number: LA-2251
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Date:	Monday, May 17, 2004
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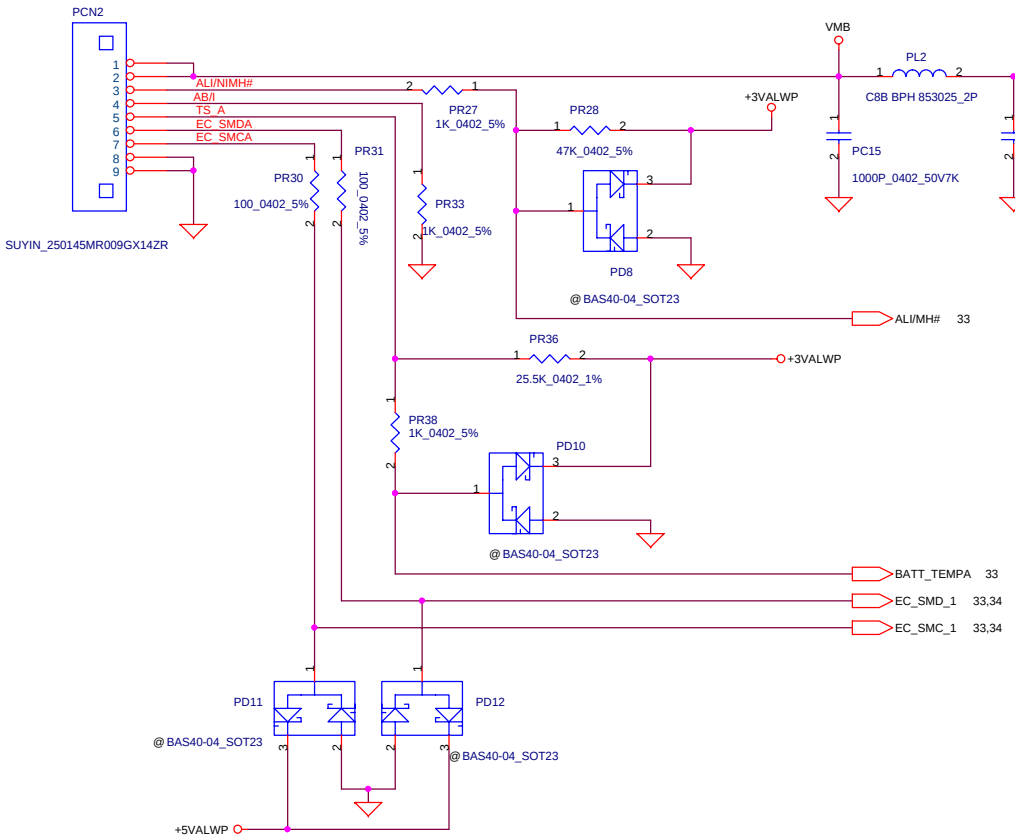
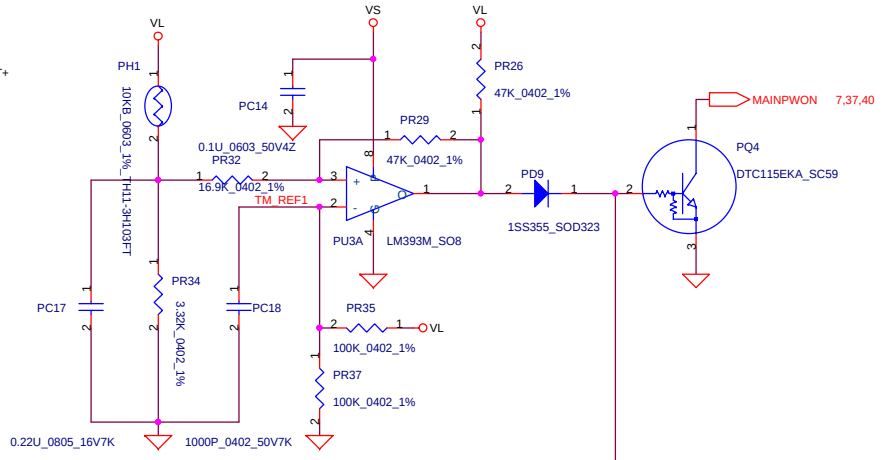
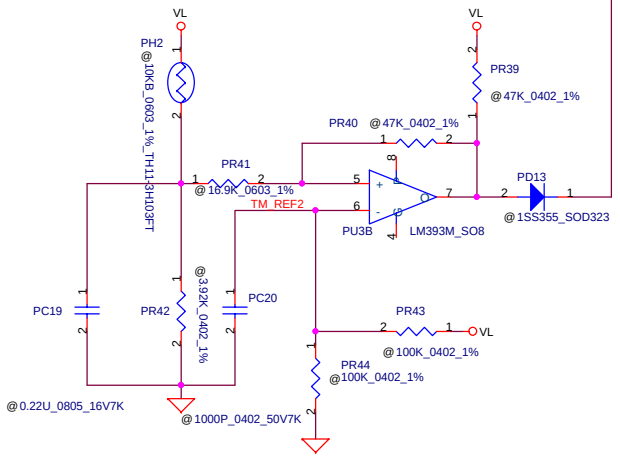
CHANGE CONNECTER



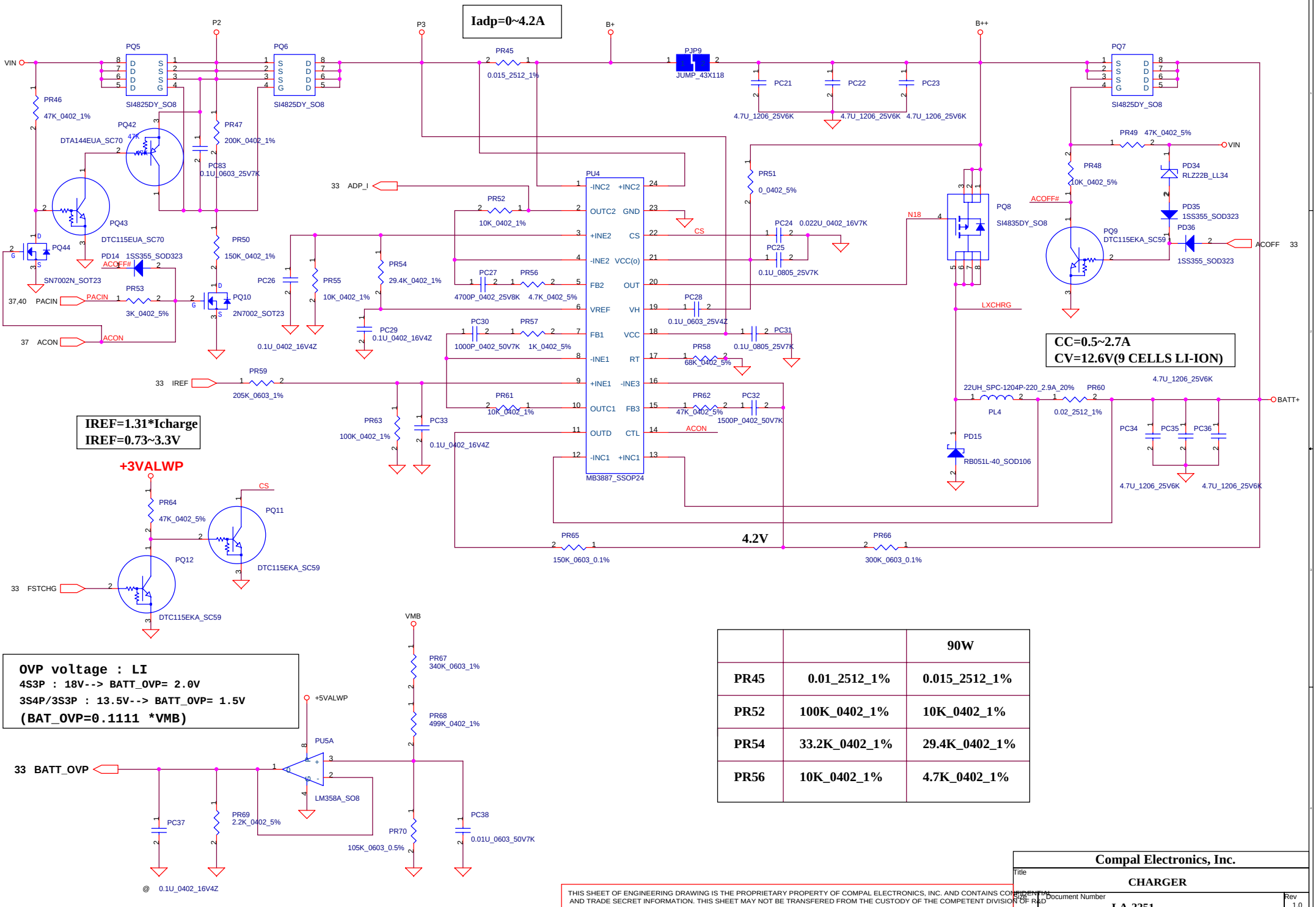
PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 78 degree C
Recovery at 45 degree C



Compal Electronics, Inc.	
Title	BATTERY CONN / OTP
Size	Document Number LA-2251 Rev 1.0
Date: Monday, May 17, 2004	Sheet 38 of 47



OVP voltage : LI
4S3P : 18V--> BATT_OVP= 2.0V
3S4P/3S3P : 13.5V--> BATT_OVP= 1.5V
(BAT_OVP=0.1111 *VMB)

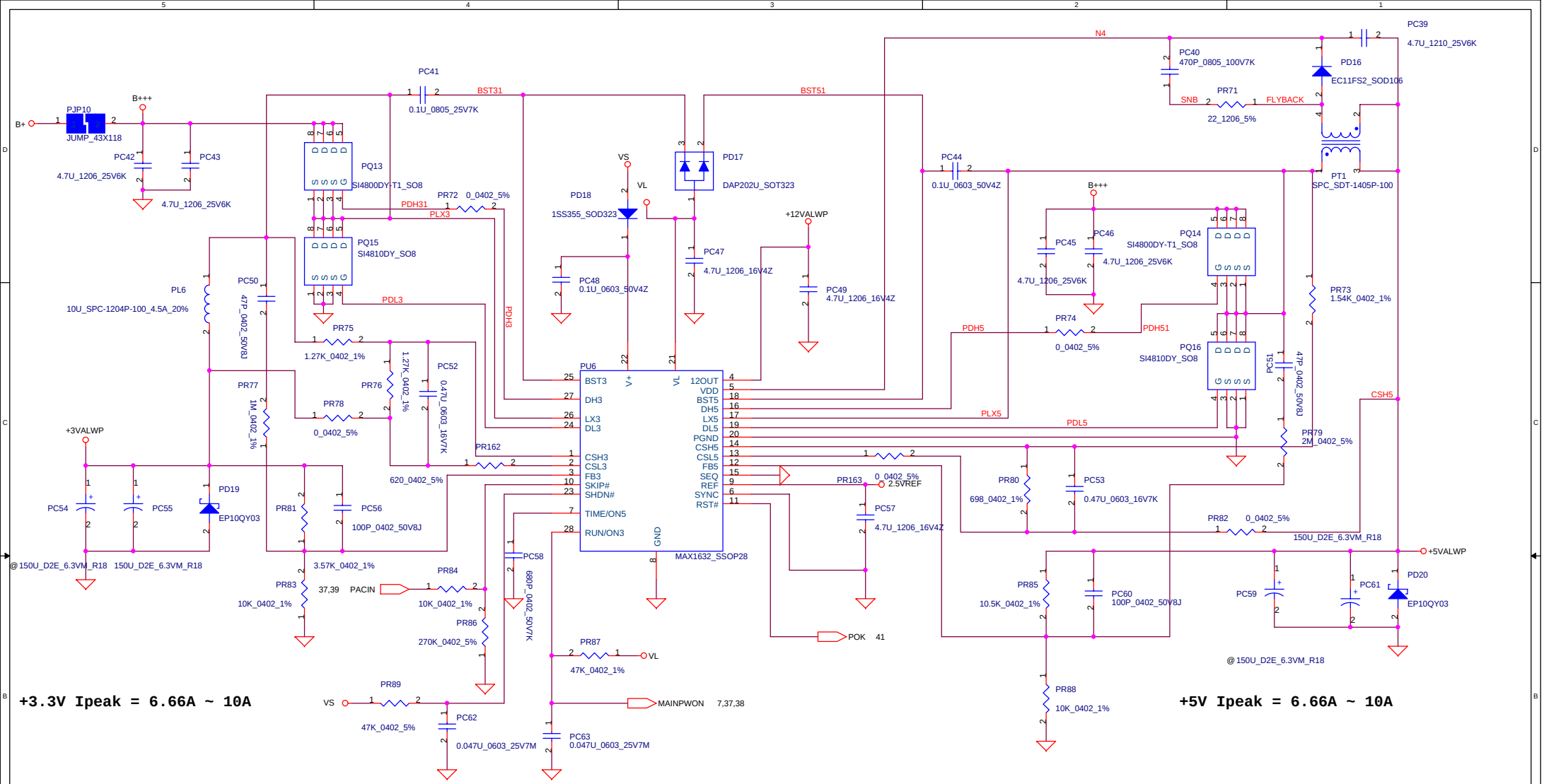
		90W
PR45	0.01_2512_1%	0.015_2512_1%
PR52	100K_0402_1%	10K_0402_1%
PR54	33.2K_0402_1%	29.4K_0402_1%
PR56	10K_0402_1%	4.7K_0402_1%

Compal Electronics, Inc.

Title: CHARGER

Size: Document Number: LA-2251 Rev: 1.0

Date: Monday, May 17, 2004 Sheet 39 of 47



Compal Electronics, Inc.	
Title	5V/3.3V/12V
Size	Document Number: LA-2251
Rev	1.0
Date:	Monday, May 17, 2004
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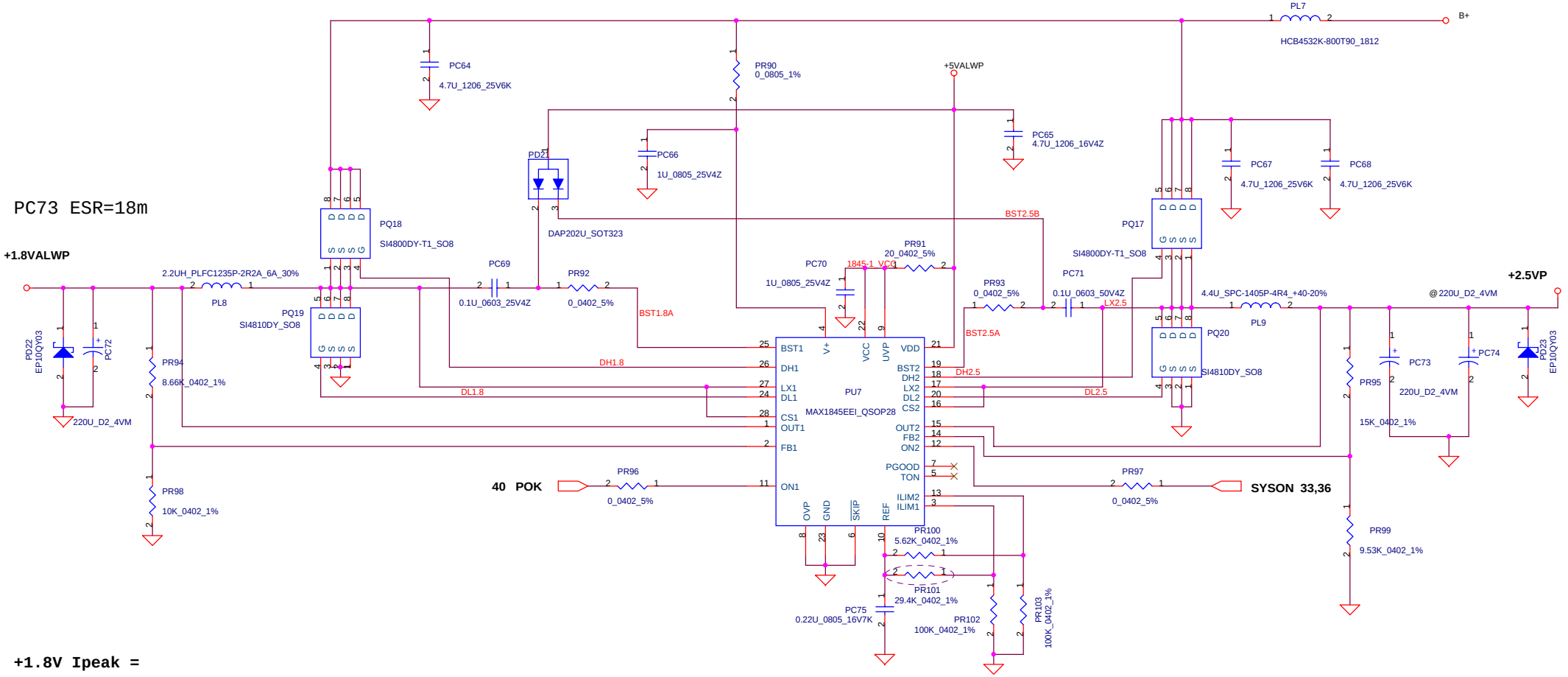
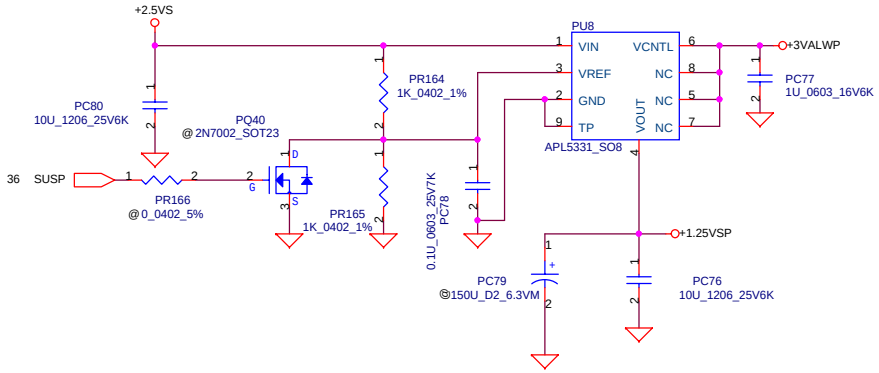
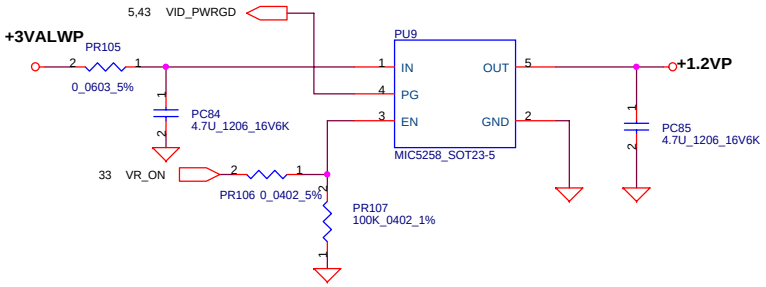


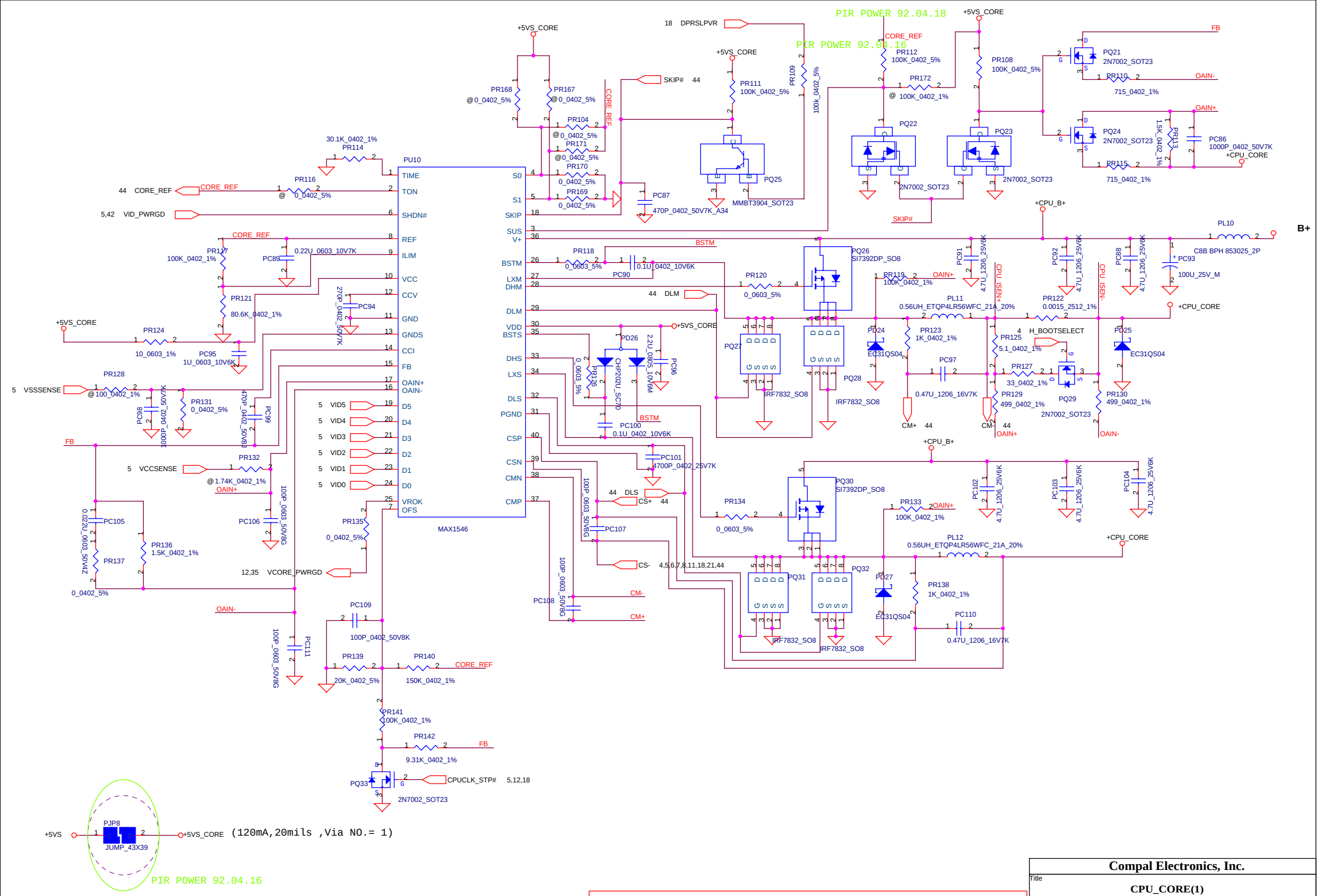
Compal Electronics, Inc.		
Title: DDR/2.5V/1.8V		
Size:	Document Number: LA-2251	Rev: 1.0
Date: Monday, May 17, 2004	Sheet 41 of 47	



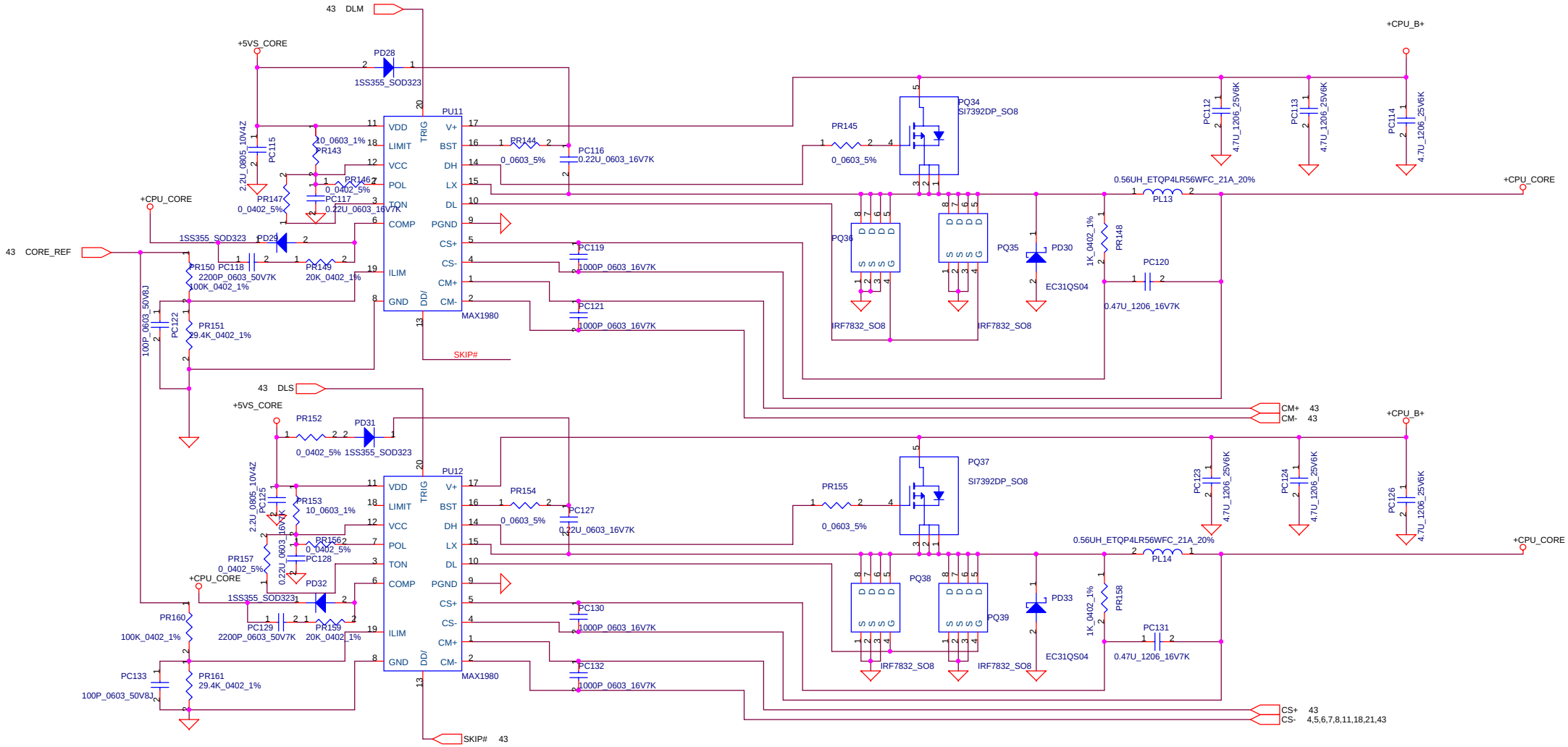


Compal Electronics, Inc.

Title	1.25V/1.2V	
Size	Document Number LA-2251	Rev 1.0
Date: Monday, May 17, 2004	Sheet 42 of 47	



Compal Electronics, Inc.	
Title	CPU_CORE(1)
Size: C	Document Number: LA-2251
Rev	1.0
Date: Monday, May 17, 2004	Sheet 43 of 47



120W	POP	PD28,PC115,PR143,PR144,PC116PR146,PR147,PC117,PD29,PR149,PC118 PR150,PR151,PC122,PU11,PC119,PC121,PQ34,PQ36,PQ35,PD30,PL13,PR148,PC120
90W	UNPOP	PD28,PC115,PR143,PR144,PC116PR146,PR147,PC117,PD29,PR149,PC118 PR150,PR151,PC122,PU11,PC119,PC121,PQ34,PQ36,PQ35,PD30,PL13,PR148,PC120

Compal Electronics, Inc.

Title: +CPU_CORE(2)

Size: A | Document Number: LA-2251 | Rev: 1.0

Date: Monday, May 17, 2004 | Sheet 44 of 47

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Description	Rev.
1	41	Wrong net	12/23/2003	Compal	Modify control signal for 2.5VSP & 1.8VALWP	0.2
2	43	For C3,C4 function	12/23/2003	Compal	Add 0 0402 5% Location is PR104,PR167,PR168,PR169,PR170,PR171.Add 100k 0402 5% Location PR172	0.2
3	43	Power	12/25/2003	Compal	Add PU13,PR173,PR174,PR175,PC81,PR176,PR177,PR179,PQ41,PR178,PC82 for monitor CPU POWER	0.2
4	39,40 41,43	For EMI cost down	02/13/2004	Compal	Del PL3,PL5,PL7,PL10 and add jump on it's location	0.2
5	39	Power	02/26/2004	Compal	Add component for charger 使背對背快速TURN OFF	0.2
6	41	Power	04/12/2004	Compal	Add PL7 avoid B+ noise interference	0.2
7	43	Power	04/12/2004	Compal	Add PL10 avoid B+ noise interference	0.2
8	43	Power	04/12/2004	Compal	Delete PU13,PR174,PR173,PR175,PC81,PR176,PR177,PQ41,PR178,PR179,PC82 for EC measure V_CORE power function	0.2
9	43	Power	04/12/2004	Compal	Change PR110,PR115 from 1K to 715 and change PR113,PR136 from 2.7k to 1.5k for modify load line from 2.5m to 1.5m	0.2

Compal Electronics, Inc.			
Title: Changed-List History-1			
Size	Document Number: LA-2251	Rev: 1.0	
Date: Monday, May 17, 2004	Sheet 45 of 47		

DFY30 from Pre-DB Step to DB-Step LA-2251 REV:0.0 -> 0.1 Modify <92.12.08.~93.02.05. >

1. Pull High 2.2Kohm_0402 from NB_I2CDATA/NB_I2CCLK to +3VS for panel I2C sense function . <Page 16> 92.12.25.
-Add R525,R526(2.2Kohm_0402) and related net . (Modify CKT,BOM&Layout)

2. Add Prescott C-step Processor reserve schematic . <Page 8,18> 92.12.30.
-Reserve R532(@470ohm_0402),R533(@1Kohm_0402),Q44(@2N7002),add R534(0ohm_0402) and related net . (Modify CKT,BOM&Layout)

3. Update ICS952013 CLK GEN. U21 CIS library . <Page 12> 92.12.31.
-Update U21(ICS952013) . (Modify CKT&Layout)

4. Remove ISOLATE function selection resistors for cost down . <Page 25> 92.12.31.
-Remove R49,R429(from 5.1K_0402_5% to @5.1K_0402_5%) . (Modify CKT&BOM)

5. Modify Prescott C-step Processor reserve schematic . <Page 18> 92.12.31.
-Modify net (H_PWRGOOD_SB and EC_ACIN) connection with U28 . (Modify CKT&Layout)

6. Add Pull High schematic for KBC ENE-KB910 . <Page 33> 92.12.31.
-Reserve R202(@10K_0402) for KBA1 . (Modify CKT&Layout)
-Add R194(10K_0402) for KBA4 . (Modify CKT,BOM&Layout)

7. Modify Material for CIS/BOM match . <Page 12> 92.12.31.
-Change C407.C419(from SE077106M00(1206) to SE053106Z00(0805)) . (Modify CKT&BOM)

8. Modify SB GPIO connection and PH/PL states . <Page 18> 93.01.02.
-Add R387,R388,R389(10Kohm_0402);Del R375(51Kohm_0402),R376,R382,R383(10Kohm_0402) . (Modify CKT,BOM&Layout)

9. Add RC temination for Thermal IC ADM1032 recommend . <Page 7> 93.01.05.
-Add R535(0ohm_0402) between +3VALW and U1.1 . (Modify CKT,BOM&Layout)

10. Change AATI4610's enable pin from SYSON to SYSON# . <Page 29> 93.01.05.
-Change U10.4 and U11.4's net from SYSON to SYSON# . (Modify CKT&Layout)

11. Change BIOS IC's P/N and wait CIS updated . <Page 34> 93.01.05.
-Change U15's P/N from SA390400100 to SA390400110 . (Modify CKT&BOM)

12. Remove Modem related EMI/Safety reserve material for cost down . <Page 29> 93.01.05.
-Remove VH1(@DSSA-P3100SB),C294,C295(@220P_1808_3KV8K) . (Modify CKT&BOM)

BOM Release

13. Change SI2306 to SI4800 for Cost Down . <Page 36> 93.01.07.
-Del Q30(SI2306DS),Add U36(SI4800) and modify related net connection . (Modify CKT,BOM&Layout)

14. Change U25F to U24F for Cost Down . <Page 27> 93.01.07.
-Del U25 , Change U25F to U24F(74LVC14) and modify related net connection . (Modify CKT,BOM&Layout)

15. Correct LCDVDD/B+ EMI solution . <Page 17> 93.01.08. **Net-In 8nd .**
-Change L3(from FBM-L11-*_0805 to 0ohm_0805),Add L18(FBM-L11-*_0805) between B+ and JP2.1,remove C215(@68P_0402),Remove Q12(@2N7002) . (Modify CKT,BOM&Layout)

16. Modify the CPU related schematic for Cost Down . <Page 5> 93.01.08.
-Del R26(56ohm_0402) and change the net(H_TESTHI2_7) to RP1.1 PH . (Modify CKT,BOM&Layout)

17. Correct the NET Name for EC define clear . <Page 10,12,18,33> 93.01.08.
-Change the NET from SLP_S3# to S3AUXSW# . (Modify CKT&Layout)
-Change the D26.1&U28.F5's NET from PCI_STOP# to PCICLK_STOP# . (Modify CKT&Layout)
-Change the NET from SLP_S5# to PSON# . (Modify CKT&Layout)

18. Change PCIPIRQ connection . <Page 26> 93.01.08.
-Change R115.1 from PCI_PIRQC# to PCI_PIRQB,R117.2 from PCI_PIRQD# to PCI_PIRQB . (Modify CKT&Layout)

19. Modify AC97_Codec related schematic . <Page 27> 93.01.08.
-Add R537(0ohm_0402) between U24.12 and C454.1,add R536(10Kohm_0402) between U23.4 and U23.8 . (Modify CKT,BOM&Layout)

20. Short all Jopen Pad Named JSH? for GerberOut Prepared . <Page 8,9,18> 93.01.08.
-Short JSH1~9(JOPEN) . (Modify CKT&Layout)

21. Remove some parts abot EMI related for cost down . <Page 23,26,27,29,> 93.01.12.
-Remove R69,R121,R153(@10ohm_0402),C184,C259,C478(@15P_0402),C296(@22P_0402) . (Modify CKT&BOM)

22. Remove some parts abot EE related for cost down . <Page 29,> 93.01.12.
-Remove C299,C307,C311(@1000P_0402_50V) . (Modify CKT&BOM)

23. Remove some parts abot USB related for Function Trial . <Page 19> 93.01.12.
-Remove R440,R441,R444(@10K_0402) . (Modify CKT&BOM)

24. Modify Material P/N for BOM correction . <Page 8,9,10,18,19,21> 93.01.12.
-Modify C356,C357,C360,C361,C363,C366,C367,C370,C382,C385,C389,C391,C392,C394,C396,C397, C402,C405,C526,C528,C530,C550,C557,C600(from P/N:SE076103Z00 to SE076103K00) . (Modify CKT&BOM)

25. Modify Material P/N for Purchase Dept. Recommend . <Page 25> 93.01.12.
-Modify C542(from P/N:SE068102K00 to SE074102K00) . (Modify CKT&BOM)

26. Remove some material EMI related for Cost Down . <Page 7,17,23,26,27,32,> 93.01.13.
-Remove C15,C16(@0.001U_0402_50V),C189,C190,C193,C194,C254,C257,C262,C267,C270(@1000P_0402_50V), C2,C3(@22P_0402_25V),C4(@0.1U_0402_16V),C5(@220P_0402_50V),C6,C7,C8,C9(@33P_0402_50V),CP1~CP6 (@100P_1206_8P4C_50V8) . (Modify CKT&BOM)
-Change L18(from KC FBM-L11-201209-221LMAT_0805 to 0ohm_0805),L36(from HB-1M2012-121JT03_0805 to 0ohm_0805) . (Modify CKT,BOM&Layout)

27. Modify Material P/N for BOM items simplify (Cost is the same) . <Page 25> 93.01.14.
-Modify C531(22U_1206_16V from P/N:SE021226Z10 to SE021226Z00) . (Modify CKT&BOM)

A-TEST SMT BUILT

DFY30 from DB-Step to Pre SI-Step LA-2251 REV:0.1 -> 0.2 Modify <93.02.06.~93.03.08. >

28. Modify "CPUCLK_STP#" related schematic for Risk fixed and Cost Down . <Page 5,12,18> 93.02.16.
-Add Q45(SB339040100) , R539(SD028120200) , R540(SD028100100) and R541(SD028000000);del D27(SC1B751V005) & R278(SD028100200) and modify the related schematic . (Modify CKT,BOM&Layout)

29. Modify "PWRBTN_OUT#" related schematic for Cost Down . <Page 18> 93.02.16.
-Modify "PWRBTN_OUT#" related schematic and del R381(SD028100200) . (Modify CKT,BOM&Layout)

30. Change "FANSPEED1" and "FANSPEED2" pull high power source from +5VS to +3VS for power saving . <Page 7> 93.02.16.
-Change R12.1 and R13.1's connection from +5VS to +3VS . (Modify CKT&Layout)

31. LCD Connector combined with Inverter Connector for cost down . <Page 17> 93.02.16.
-Modify the related schematic and del JP2 . (Modify CKT,BOM&Layout)

32. Remove TV-OUT function . <Page 17> 93.02.16.
-Modify the related schematic and del D12,D13,D14,L5,L8,L9,C232C233,C234,C235,C236,C237,R97,R98,R99,JP19 . (Modify CKT,BOM&Layout)

33. Modify PCMCIA spec from 2 slots to 1 slot . <Page 23> 93.02.16.
-Change U4 CB1420 to CB1410 and U5 CP2216 to CP2211 , del R85,D6,R75,C195,C196,R77~R81,C211,C212,C213, C204,C203,C207,R87 , add C699 . (Modify CKT,BOM&Layout)

34. Change SI2302 to SI4800 for Cost Down . <Page 17> 93.02.16.
-Change Q13(P/N: SB523020005) to U40(P/N: SB548000100) and modify the related schematic (Modify CKT,BOM&Layout)

35. Add IEEE1394 function and related schematic/material . <Page 24> 93.02.16.
-Add C701,C702,C703,C704,C705,C706,C707,C708,C709,C713,C710,C711,C712,C714,C715,C716,JP23,R543,R547, R544,R545,R546,R550,R551,R548,R549,R552,R553,R554,R555,U38,U39,X1 and modify the related schematic . (Modify CKT,BOM&Layout)

36. Change JP9 from P/N: SP010019210 to SP010009910 for cost down . <Page 32> 93.02.16.
-Change JP9 from P/N: SP010019210 to SP010009910 , del R508,R509,R510,R523,C684,C685,C686,C694 and modify the related schematic . (Modify CKT,BOM&Layout)

37. Modify BIOS pin definition and remove BIOS beffer IC for cost down plan . <Page 33,34> 93.02.16.
-Del U13,U14,RP33,C331,RP32,R186,R189,C333,C332,R188 and modify the related schematic . (Modify CKT,BOM&Layout)

38. LED function re-defined for cost down plan . <Page 32,33> 93.02.20.
-Del C688,C690,R512,R514, and modify the related schematic . (Modify CKT,BOM&Layout)

39. Issue BEEP# from EC pin directly for cost down plan . <Page 27> 93.02.22.
-Move U6,U24 location ; Del R305,R308,R303(@),R537,C457 and modify the related schematic . (Modify CKT,BOM&Layout)

40. Add EMI request schematic for Inverter related reserved . <Page 17> 93.02.22.
-Add L59,L60,L61,L62(close to JP6) and modify the related schematic . (Modify CKT,BOM&Layout)

41. Add pull down design for "SYSON","SUSP#","EC_RSMRST#" floating risk . <Page 33> 93.02.22.
-Add R556,R557,R558(close to U12) and modify the related schematic . (Modify CKT,BOM&Layout)

42. Modify the "PCI_RST#" related schematic for Cost Down verified and prepared . <Page 20> 93.02.23.
-Add R559,R560,C717,R561,R562,R565; (Remove U24,C380,C452(@)) and modify the related schematic . (Modify CKT,BOM&Layout)

43. Change Reset IC from MAX6342RUT to MAX809SEUR for Cost Down . <Page 35> 93.02.23.
-Add U41,R563,R564 ; (Remove U32,R460,R461,R462(@)) and modify the related schematic . (Modify CKT,BOM&Layout)

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DFY30 from DB-Step to Pre SI-Step LA-2251 REV:0.1 -> 0.2 Modify <93.02.06.~93.03.09. >

44. Reserve EMI request design for LVDS clock related signal . <Page 9,16> 93.02.23.
-Add R566(@),C718(@),R567(@),R568(@),C719(@),C720(@),move R215 (close to U22) and modify the related schematic . (Modify CKT&Layout)

45. Create +PWR_PCM for U4(CB1410) core power +3VALW and +3VS power source option . <Page 23> 93.02.25.
-Modify the related schematic to change +3VALW to +PWR_PCM . (Modify CKT&Layout)

46. Reserve +3VS power source option for U4(CB1410) pin18&44 . <Page 23> 93.02.25.
-Add R569(@),R570(@)(close to U4) and modify the related schematic . (Modify CKT&Layout)

47. Reserve some CAPs for Power Plane through mode risk improved . <Page 36> 93.02.25.
-Add C721~C726(@) and modify the related schematic . (Modify CKT&Layout)

48. Cancel VGA_GND for EMI request . <Page 16,17> 93.03.02.
-Del L54,L55,L56,L57 and modify the related schematic . (Modify CKT,BOM&Layout)

49. Remove MiniPCI Modem function . <Page 26> 93.03.02.
-Del R123 , C266(@),C267(@),R122(@),C263(@) and modify the related schematic . (Modify CKT,BOM&Layout)

50. Remove MiniPCI Modem function . <Page 27> 93.03.03.
-Del R333, Remove R334,C484(Close to Pin22) and modify the related schematic . (Modify CKT,BOM&Layout)

51. Modify Pull High Resistor Value from 100K to 10K for standard design . <Page 12> 93.03.03.
-Modify R527 from 100Kohm to 10Kohm . (Modify CKT&BOM)

52. Remove some parts because remove ACER keyboard function . <Page 32> 93.03.03.
-Remove Q1,R4,R5,R6 . (Modify CKT&BOM)

53. Add the Pull High Resistor to enable the VGA tuned function for SIS request . <Page 09> 93.03.03.
-Add R210 (P/N: SD028470100/ S RES 1/16W 4.7K +-5% 0402) . (Modify CKT&BOM)

54. Modify the resistor's value to 1Mohm for SI4800 design . <Page 17> 93.03.03.
-Change R91(P/N: SD028150300 to SD028100400) . (Modify CKT&BOM)

55. Modify NB_RST# related and change LPC_RST# resistor value for signal quality improved . <Page 20> 93.03.09.
-Change R346(0ohm->10ohm) ; Add R571(10ohm) . (Modify CKT,BOM&Layout)

56. Change SIS302ELV pin60 level latch power source from +3VS to +1.8VS(same as SIS661FX U18.W3 power source) for SIS Design Change . <Page 16> 93.03.09.
-Change L47.1's power source from +3VS to +1.8VS . (Modify CKT&Layout)

BOM Release .

57. Modify PCI_RST# related and change PCI_RST# resistor value for signal rising time risk fixed . <Page 20> 93.03.18.
-Change R562(1Kohm->300ohm);R565(2Kohm->620ohm);Remove C717(10PF_0402).(Modify CKT&BOM)

58. Modify PM_PWRGD related and change PM_PWRGD resistor value for signal rising time risk fixed . <Page 35> 93.03.18.
-Change R563(1Kohm->300ohm) ; R564(2Kohm->620ohm) . (Modify CKT&BOM)

~~**59. Pull Down BT_WAKE_UP signal . <Page 33> 93.03.19.**~~
~~-Add C330(100K_0603ohm,SD0131003T1) . (Modify CKT&BOM)~~

60. Change Material to meet Layout Size . <Page 30> 93.03.19.
-Change C503(10U_1206->10U_0805)(SE054106Z10->SE054106Z10) . (Modify CKT&BOM)

61. Disconnect CPUCLK_STP# to CLK GEN . <Page 12> 93.03.19.
-Remove R541(@0ohm) . (Modify CKT&BOM)

62. Update PCMCIA SOCKET JP15 Library . <Page 23> 93.03.22.
-Update JP15 CIS library . (Modify CKT&Layout)

~~**63. Correct H_FERR# have double Pull High problem . <Page 05> 93.04.05.**~~
~~-Remove R18(56ohm) . (Modify CKT&BOM)~~

64. Modify JP26 pin4 connection for Pioneer ODD(DVD Dual DVR-K12TBC/DVR-K13TBC) used . <Page 22> 93.04.08.
-Reserve R572(@0ohm_0402) . (Modify CKT,BOM&Layout)

65. Add Decoupling Capacitor 220PF close to DDR Clock Buffer for EMI request . <Page 13> 93.04.10.
-Add C728,C729(220PF_0402) close to U20 . (Modify CKT,BOM&Layout)

66. Add Decoupling Capacitor 220PF close to NB M661FX VDDM for EMI request . <Page 11> 93.04.10.
-Add C730,C731,C732(220PF_0402) close to U18 . (Modify CKT,BOM&Layout)

67. Modify H_TESTHI2_7 Pull-High Resistor connection for Layout placement issue . <Page 05> 93.04.10.
-Add R573(56ohm_0402) close to JP25 . (Modify CKT,BOM&Layout)

68. Del H19 for PCB space free . <Page 30> 93.04.10.
-Del H19 . (Modify CKT&Layout)

69. Modify Audio Codec pins connection related to fix the noise issue . <Page 27> 93.04.12.
-Remove C467(@0.1UF_0402) . (Modify CKT&BOM)
-Reserve C733,C734(@0.1UF_0402) . (Modify CKT&Layout)

~~**70. Modify JP32 power source pins connection for new CardReader Board cost down and SB chip power issue fixed . <Page 29> 93.04.12.**~~
~~-Change JP32.1&JP32.7 from +5VS to +3VALW ; JP32.2&JP32.8 from +5VS to +3VS . (Modify CKT&Layout)~~

71. Modify the USB ports definition and related connection for SB USB power source issue improved . <Page 19,29> 93.04.12.
-Change USB ports from P0 to P3 ; P3 to P5 ; P5 to P4 ; P4 to P0 . (Modify CKT&Layout)
-Remove OVCUR#5 R496(@10K_0402) , Add OVCUR#0 R440(10K_0402) . (Modify CKT&BOM)

72. Add BT_WAKE_UP Pull Down resistor . <Page 33>93.04.12.
-Add R574(100Kohm_0402) . (Modify CKT,BOM&Layout)

73. Add some material to BOM for EMI request . <Page 9,13,19>93.04.15.
-Add C406,C545(10PF_0402) . (Modify CKT&BOM)
-Add R566,R442(12ohm_0402) . (Modify CKT&BOM)
-Add C718(15PF_0402) . (Modify CKT&BOM)

74. Modify H_PROCHOT# connection and add EC_PROCHOT# pin for Throttling function control by EC . <Page 5,18,33>93.04.19.
-Add R21 (62ohm_0402)(Because SB Int. PH disconnection) . (Modify CKT&BOM)
-Remove R378(0_0402) ; Add R578(0_0402) to connect CPU and EC CTRL(U12.92) . (Modify CKT,BOM&Layout)

75. Correct H_FERR# have double Pull High problem . <Page 18> 93.04.19.
-Del RP87.6(H_FERR# connection) . (Modify CKT&Layout)

76. Modify IEEE1394 related schematic for the Vendor VIA recommend . <Page 24> 93.04.19.
-Add R576(0ohm_0805) . (Modify CKT,BOM&Layout)
-Add C735,C736,C737,C738(0.1UF_0402) . (Modify CKT,BOM&Layout)
-Remove R544(1Kohm_0402) . (Modify CKT&BOM)
-Connect R550.2,R551.2,R552.1&C712.1 . (Modify CKT&Layout)

77. Disconnect JP8.36(WLAN_PME#) for normal design . <Page 26> 93.04.19.
-Reserve R579(@0ohm_0402) . (Modify CKT&Layout)

78. Change VBCAD's Pull-High Power Source from +3VS to +1.8VS for the vendor SIS recommend . <Page 16> 93.04.19.
-Change R384.1's connection from +3VS to +1.8VS . (Modify CKT&Layout)

79. Modify JP32 power source pins connection for new CardReader Board cost down and SB chip power issue fixed option . <Page 29> 93.04.19.
-Change JP32.1/2/7/8 from +5VS only to+5VS(JOPEN3)/+3VALW(JOPEN4) option . (Modify CKT,BOM&Layout)

80. Disconnect MDC Connector JP14.29 for power consumption save . <Page 29> 93.04.19.
-Reserve R575(@0_0402) between JP14.29 and GND . (Modify CKT&Layout)

81. Modify LPC_RST# and NB_RST# related resistor value to fix signal quality issue . <Page 20> 93.03.18.
-Change R346(0ohm_0402->10ohm_0402) ; Add R571(10ohm_0402) . (Modify CKT,BOM&Layout)

DFY30 from PV-Step to Pre MV-Step LA-2251 REV:0.3 -> 1.0 Modify <93.04.19.~93.05.27. >

82. Modify Audio AMP LIN/RIN CAPs' value to improve audio noise issue . <Page 28> 93.04.29.
-Change C283,C284 from 0.47UF_0603 to 22PF_0603 . (Modify CKT&BOM)

83. Modify Audio AMP FADE# pin define to improve audio noise issue . <Page 28> 93.04.29.
-Change U9.16(FADE#)'s connection from AGND to +5VAMP by 10Kohm resistor(R580_0402) . (Modify CKT,BOM&Layout)

84. Change EC_SMD_2/EC_SMC_2's pull high power source from +3VALW to +5VALW because ENE_KB910 SMBUS1/2 use the same power level . <Page 33> 93.05.05.
-Change RP31.7/RP31.8 from +3VALW to +5VALW . (Modify CKT&Layout)

85. Modify SI102221K05 to SI102221K10 for material shortage issue . <Page 31> 93.05.13.
-Change CP7,CP8,CP9 from SI102221K05 to SI102221K10 . (Modify CKT&BOM)

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