CS5171/2/3/4

1.5A 260kHz/520kHz Boost Regulators

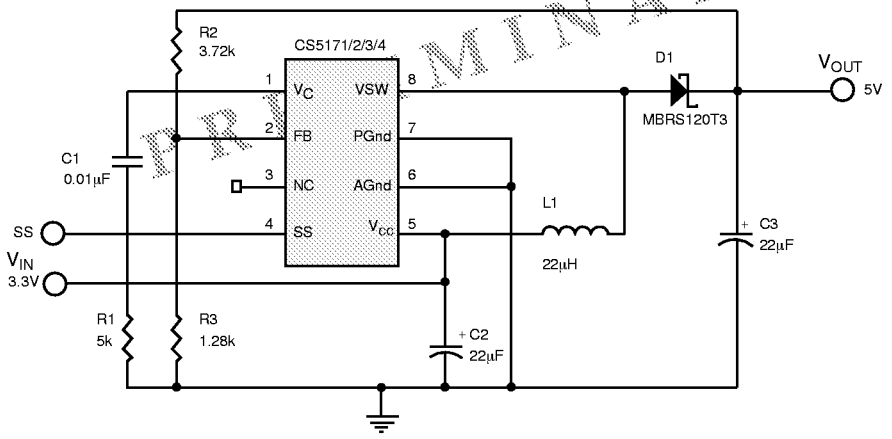
Description

The CS5171/2/3/4 are 260kHz/520kHz switching regulators with a 1.5A high efficiency integrated switch. These parts operate over a wide input voltage range of 2.7V to 30V. The flexibility of the design allows the chips to be operated in most power supply configurations, such as boost, flyback, forward, inverting, and sepic. The IC's utilize current mode architecture, which allows excellent load and line regulation as well as a practical means for current limit. Combining high frequency operation with a highly integrated regulator circuit provides for an extremely compact power supply solution. The circuit design includes provisions for features such as frequency synchronization, shutdown, and feedback controls for either positive or negative voltage regulation. These parts are pin to pin compatible with LT1372/1373.

Part Number	Frequency	Feedback Voltage Polarity
CS5171	260kHz	positive
CS5172	260kHz	negative
CS5173	520kHz	positive
CS5174	520kHz	negative

Application Diagram

3.3V to 5V/400mA Boost Converter

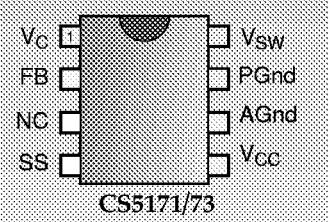


Features

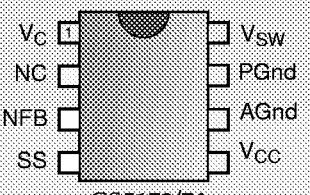
- Integrated power switch: 1.5A guaranteed
- Wide input range: 2.7V to 30V
- High frequency allows for small components
- Minimum external components
- Easy external synchronization
- Built in overcurrent protection
- Thermal shutdown with hysteresis
- Regulates either positive or negative outputs
- Shut down current: 50µA maximum
- Available in 8 pin SON
- Pin to pin compatible with LT1372/1373
- Wide ambient temperature range: –40°C to 85°C

Package Options

8 Lead SO Narrow



CS5171/73



CS5172/74

Cherry Semiconductor Corporation
2000 South County Trail, East Greenwich, RI 02818
Tel: (401)885-3600 Fax: (401)885-5786
Email: info@cherry-semi.com
Web Site: www.cherry-semi.com

Absolute Maximum Ratings

PIN SYMBOL	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
V_{CC}	IC Power Input	40V	-0.3V	N/A	200mA
SS	Shutdown/Sync	40V	-0.3V	1mA	1mA
V_C	Compensation Capacitor	6V	-0.3V	10mA	10mA
FB (CS5171/3 only)	Voltage Feedback Input	10V	-0.3V	1mA	1mA
NFB (CS5172/4 only)	Negative Feedback Input (transient, 10ms)	10V	-10V	1mA	1mA
PGnd	Power Ground	0.3V	-0.3V	4A	10mA
AGnd	Analog Ground	0V	0V	N/A	10mA
V_{SW}	Switch Input	40V	-0.3V	10mA	4A

Junction Temperature Range, T_J ..... -40°C to 150°C
Storage Temperature Range, $T_{STORAGE}$ ..... -65° to 150°C
Lead Temperature Soldering: Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak
ESD, Human Body Model 2kV
ESD, Machine Model 200V

Electrical Characteristics: -40°C < T_A < 85°C; -40°C < T_J < 125°C; 2.7V < V_{CC} < 30V; For all CS5171/2/3/4 specifications unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Positive and Negative Error Amplifiers					
FB Reference Voltage (CS5171/3 only)	V_C tied to FB measure at FB	1.257	1.276	1.295	V
NFB Reference Voltage (CS5172/4 only)	V_C = 0.8V	-2.60	-2.50	-2.44	V
FB Input Current (CS5171/3 only)	FB = V_{REF} = 1.250V	-1	0	1	µA
NFB Input Current (CS5172/4 only)	NFB = -2.5V	-15	-10	-5	µA
FB Reference Voltage Line Regulation (CS5171/3 only)	V_C = 0.8V		.01	.03	%/V
NFB Reference Voltage Line Regulation (CS5172/4 only)	V_C = 0.8V		.01	.05	%/V
Positive and Negative Error Amp Transconductance	Note 1	400	600	800	µMho
Positive Error Amp Gain	Note 1	200	500		V/V
Negative Error Amp Gain	Note 1	100	180	320	V/V
V_C Source Current	FB = 1V or NFB = -1.875V, V_C = 1.5V	25	50	90	µA

Electrical Characteristics: -40°C < T_A < 85°C; -40°C < T_J < 125°C; 2.7V < V_{CC} < 30V; For all CS5171/2/3/4 specifications unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Positive and Negative Error Amplifiers continued					
V_C Sink Current	FB = 1.5V or NFB = -3.125V, V_C = 1.5V	200	625	1500	µA
V_C High Clamp Voltage	FB = 1V or NFB = -1.875V	1.5	1.7	1.9	V
V_C Low Clamp Voltage	FB = 1.5V or NFB = -3.125V, V_C sinks 50µA	0.35	0.5	0.65	V
V_C Threshold	0% duty cycle	0.4	0.6	0.8	V
■ Oscillator					
Base Operating Frequency	CS5171/2, FB = 1V or NFB = -2V	240	260	280	kHz
Reduced Operating Frequency	CS5171/2, FB = 0V or NFB = 0V	30	52	70	kHz
Base Operating Frequency	CS5173/4, FB = 1V or NFB = -2V	480	520	560	kHz
Reduced Operating Frequency	CS5173/4, FB = 0V or NFB = 0V	60	104	140	kHz
Maximum Duty Cycle		90	94	98	%
NFB Frequency Shift Threshold	Frequency reduces to 20% of the base frequency	-1.8	-1.2	-0.8	V
FB Frequency Shift Threshold	Frequency reduces to 20% of the base frequency	0.36	0.40	0.44	V
■ Sync/Shutdown					
Sync Range	CS5171/2	280		500	kHz
Sync Range	CS5173/4	560		1000	kHz
Sync Pulse Transition Threshold	Rise time = 20ns	2.5			V
SS Bias Current	SS = 0V SS = 5V		-3 3	-8 8	µA µA
Shutdown Threshold		0.6	1.3	2	V
Shutdown Delay	SS = 5V to 0V, V_C < 0.8V	12	36	100	µs
■ Power Switch					
Switch Saturation Voltage	I_{SWITCH} = 1.5A I_{SWITCH} = 10mA		0.8 0.09	1.0 0.3	V
Switch Current Limit	50% duty cycle 80% duty cycle	1.6 1.5	1.9 1.7	2.4 2.2	A A
Minimum Pulse Width	FB = 0V, I_{SW} = 2.5A, NFB = 3.0V	100	180	200	ns

Electrical Characteristics: -40°C < T_A < 85°C; -40°C < T_J < 125°C; 2.7V < V_{CC} < 30V; For all CS5171/2/3/4 specifications unless otherwise stated.

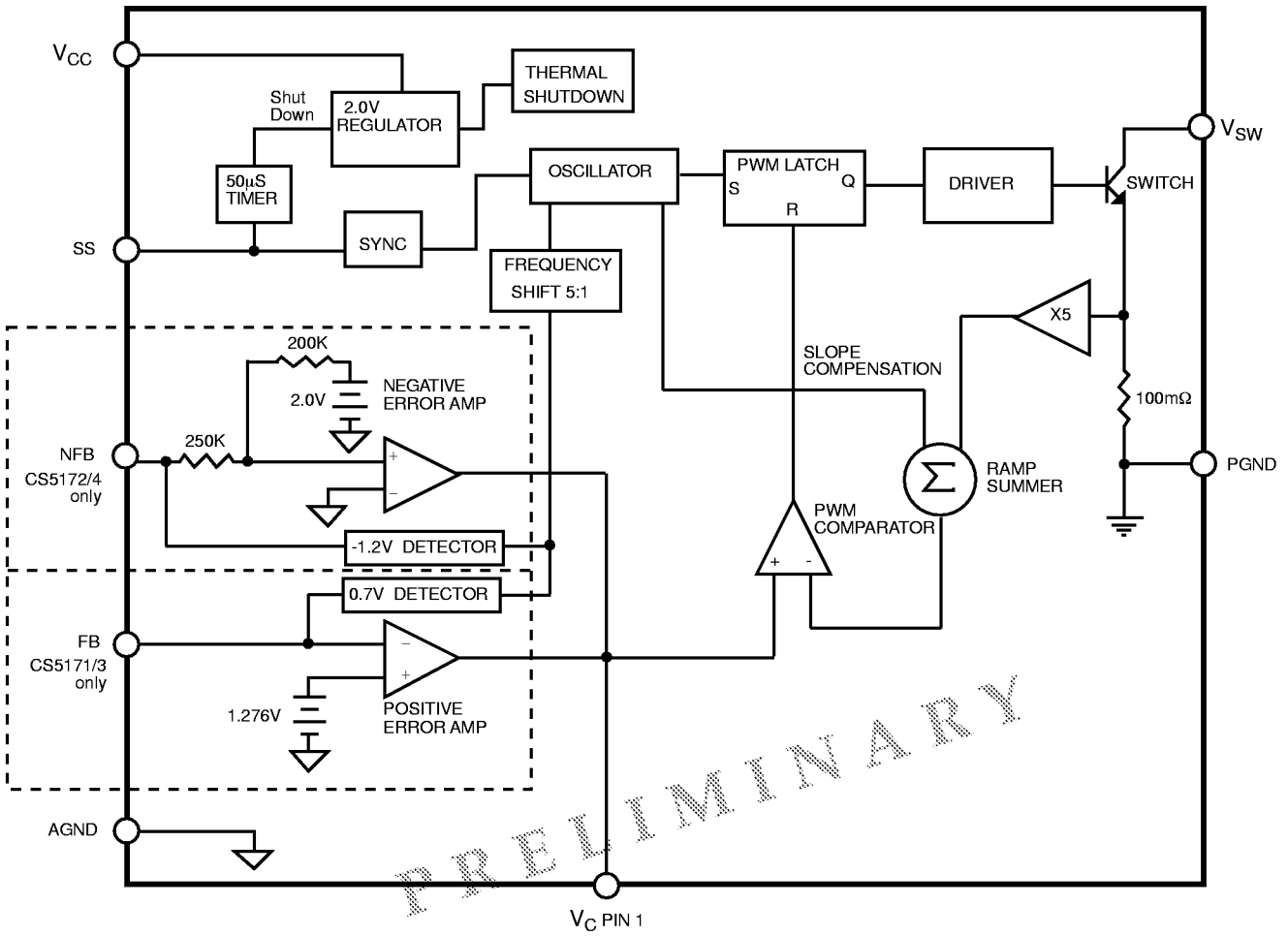
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Power Switch: continued					
$\Delta I_{CC}/\Delta IV_{SW}$	$0 < I_{SW} < 1.5A$		10	20	mA/A
Switch Leakage	$V_{SW} = 40V$, $V_{CC} = 0V$		20	1000	µA
■ General					
Operating Current	$I_{SW} = 0$		5.5	11	mA
Shutdown Mode Current	$V_C < 0.8\ V_{SS} = 0V$		12	50	µA
Minimum Operation Input Voltage	V_{SW} switching, maximum $I_{SW} = 10mA$		2.45	2.70	V
Thermal Shutdown	Note 1	150	180	210	°C
Thermal Hysteresis	Note 1		25		°C

Note 1: Guaranteed by design, not 100% tested in production.

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
1	V_C	Loop compensation pin. The V_C pin is the output of the error amplifier and is used for loop compensation, current limit and soft start. Loop compensation can be implemented by a simple RC network as shown in the application diagram as R1 and C1.
2 (CS5171/3 only)	FB	Positive regulator feedback pin. This pin provides sensing of a positive voltage output and is referenced to 1.276V. When the voltage at this pin falls below 0.7V, chip switching frequency reduces to 20% of the nominal frequency.
2 (CS5172/4 only)	NC	No connection.
3 (CS5171/3 only)	NC	No connection.
3 (CS5172/4 only)	NFB	Negative regulator feedback pin. This pin provides sensing of a negative voltage output and is referenced to -2.5V. When the voltage at this pin goes above –1.2V, chip switching frequency reduces to 20% of the nominal frequency. Leave it floating when only regulating a positive voltage.
4	SS	Synchronization and shut down pin. This pin may be used to synchronize the part to nearly twice the base frequency. A TTL low will shut the part down and put it into low current mode. If synchronization is not used this pin should be tied high or left floating for normal operation.
5	V_{CC}	Input power supply pin. This pin supplies power to the part and should have a bypass capacitor attached.
6	AGnd	Analog ground. Provides a clean ground for the controller circuitry. This pin should not be in the path of large currents and the output voltage sensing resistors should be connected to this ground pin. This pin is connected to the IC substrate.
7	PGnd	Power ground. Provides ground to the emitter of the power switching transistor. Connection to a good ground plane is essential.
8	V_{SW}	High current switch pin. This pin connects internally to the collector of the power switch. The open voltage across the power switch can be as high as 40V. To minimize radiation, use a trace as short as practical.

Block Diagram



Application Information

Theory Of Operation

Current Mode Control

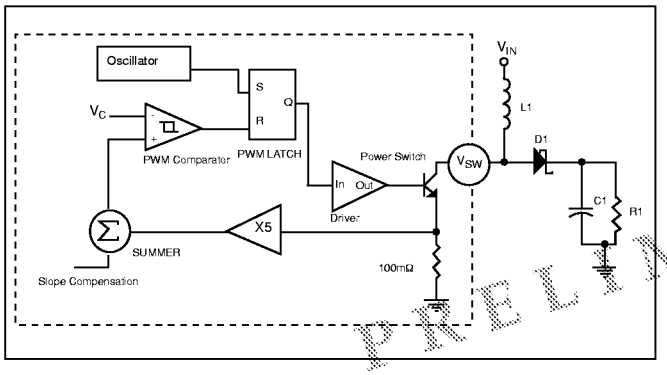


Figure 1. Current Mode Control Scheme

The CS517X family incorporates a current mode control scheme, in which the PWM ramp signal is derived from power switch current. This ramp signal is compared to the output of the error amplifier to control the on time of the power switch. The oscillator is only used here as a fixed frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over the conventional voltage mode controller. First, derived directly from the inductor, the ramp signal will respond immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly suffered in voltage mode. The second benefit comes from inherent pulse-by-pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows both simpler compensation and a higher gain bandwidth over a comparable voltage mode circuit.

Without discrediting its apparent merits, current mode control comes with its own peculiar problems, mainly, subharmonic oscillation at duty cycle over 50%. The CS517X family solves this problem by adopting slope compensation in which a fixed ramp generated by the oscillator is

added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Oscillator and Shutdown

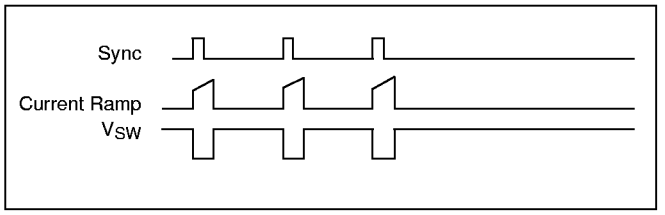


Figure 2. Timing Diagram of Sync and Shut Down.

The oscillator is trimmed to guarantee an 8% frequency accuracy. As shown in Figure 1, the output of the oscillator turns on the power switch at a frequency of 260kHz (CS5171/2) or 520kHz (CS5173/4). The power switch is turned off by the output of the PWM Comparator. The maximum duty cycle can be as high as 90%.

A TTL compatible sync input at the SS pin is capable of syncing up to 1.8 times the base oscillator frequency. As shown in Figure 2, in order to sync to a higher frequency, a positive transition turns on the power switch before the output of the oscillator does so. The sync signal also resets the oscillator. The sync operation allows multiple power supplies to operate at the same frequency. A logic low sustained for typically 50μs at the SS pin will shut down the ICs and reduce the supply current to 50μA.

An additional feature includes frequency shift to 20% of the nominal frequency when either the NFB or FB pins trigger the threshold. During overload, power up, or short circuit conditions, the minimum switch on time is limited by the PWM comparator blanking period. Extra switch off time reduces the minimum duty cycle to protect external components and the IC itself.

As previously mentioned, this block also produces a ramp for the slope compensation to improve regulator stability.

Error Amplifier

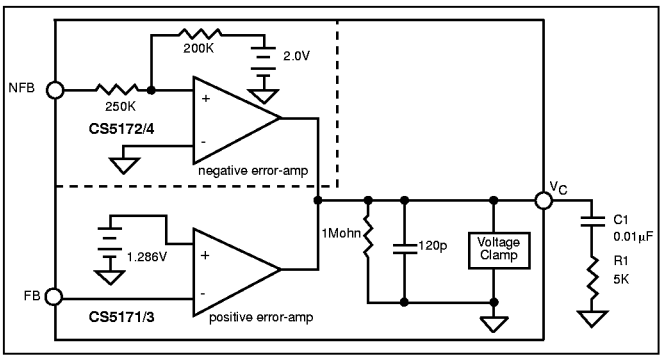


Figure 3. Error amplifier equivalent circuit.

For CS5172/4, the NFB pin is internally referenced to -2.5V with approximately a 250kΩ input impedance. For CS5171/3, the FB pin is directly connected to the inverting input of the positive error amplifier whose non-inverting input is fed by the 1.276V reference. Both amplifiers are transconductance amplifiers with high output impedance of approximately 1MΩ as shown in Figure 3. The V_C pin is connected to the output of the error amplifiers and is internally clamped between 0.6V and 1.7V. A typical connection at the V_C pin includes a capacitor in series with a resistor to ground, forming a pole/zero for loop compensation.

An external shunt can be connected between the V_C pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

Switch Driver and Power Switch

The switch driver takes a control signal from the logic section to drive the output power switch. The switch is grounded through emitter resistors (100mΩ total) to the PGnd pin. The PGnd is not connected to the IC substrate to isolate switching noise from the analog ground. The peak switching current is clamped by an internal circuit. The clamp current is guaranteed to be greater than 1.5A and varies with duty cycle due to slope compensation. The power switch can withstand a maximum voltage of 40V on the collector (V_{SW} pin). The saturation voltage of the switch is less than 1V to minimize power dissipation. Additionally, a 100ns blanking period is placed at the rising edge of the current slope to prevent mis-triggering of the PWM Comparator. This is necessary due to the turn-on current ringing.

Short Circuit Condition

When a short circuit condition happens in a boost circuit, the inductor current will increase during the whole switching cycle, causing excessive current to be drawn from the input power supply. Since control ICs don't have the means to limit load current, an external current limit circuit (such as fuses and relays) has to be implemented to protect the load, power supply and ICs.

In a flyback regulator application, the frequency shift built into the ICs will prevent the damage to the chip and external components. This feature will reduce the minimum duty cycle and allow the transformer secondary side to absorb enough energy before the switch turns back on.

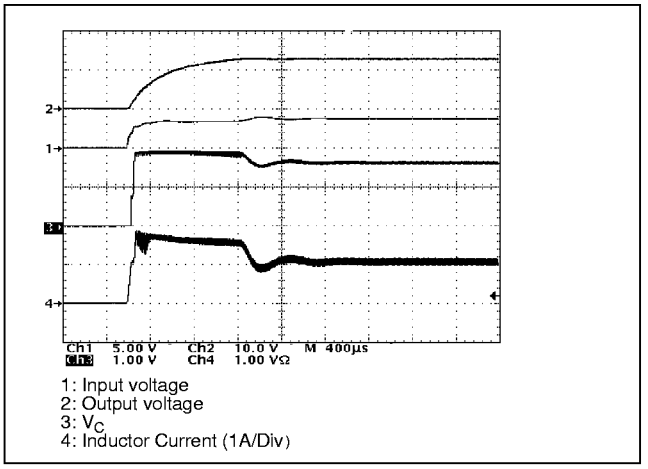


Figure 4. Start up waveforms of the boost converter shown in the Application Diagram. LOAD = 50Ω

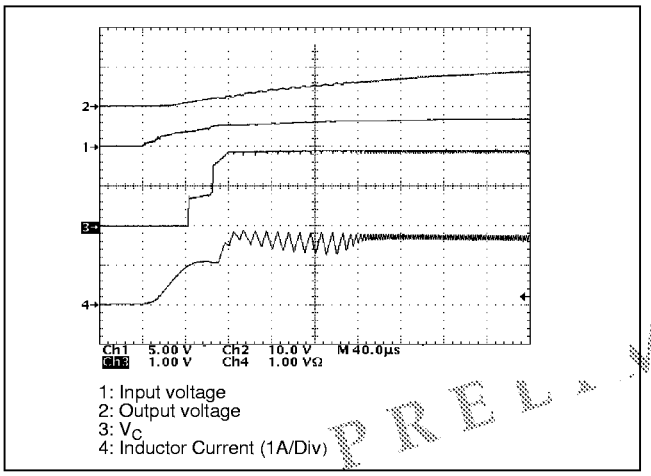


Figure 5: First several cycles of the start up waveforms shown in Figure 5.

The CS517X can be activated by either connecting the V_{CC} pin to a voltage source or enabling the SS pin. Start up waveforms shown in Figure 4 and Figure 5 are measured in the boost converter demonstrated in the Application Diagram. Recorded after the input voltage is turned on, these waveforms clearly show the various phases during this power up transition. Figure 4 shows the whole start up period, while Figure 5 zeros in on the very first several switching cycles.

When the input voltage at the V_{CC} pin is below the minimum threshold voltage, the V_{SW} pin is high impedance. Therefore, current conducts directly from the input power source to the output through the inductor and diode. This phase is identified in Figure 5 as the first current swing. When the V_{CC} pin voltage rises above the threshold, the V_{SW} pin starts to switch to PGnd. Detecting a low output voltage at the FB pin, the built-in frequency shift feature reduces the switching frequency to 20% of the nominal value. This increases switch off time during each switching cycle and reduces the average current. The peak current in this phase is clamped by the internal current limit. By applying a voltage clamp or soft start circuit at the V_C pin, this peak current can be further limited. When the feedback voltage at the FB pin rises above 0.7V, the frequency increases to its nominal value. In this phase, the peak current decreases while the output voltage continues approaching the targeted value. Finally, after a settling period, the system enters steady-state operation.

Component Selection

Frequency Compensation

At the V_C pin, a RC network shall connect in series to perform loop frequency compensation. Along with the transconductance amplifier output impedance, the RC network forms two pole and one zero system to optimize dynamic performance while maintaining stability. The locations of poles and zero are:

$$fp1 = \frac{1}{2\pi R_O C_1} \quad f_Z = \frac{1}{2\pi R_1 C_1} \quad fp2 = \frac{1}{2\pi R_1 C_O}$$

Where

f_Z: frequency of zero

fp1, fp2: frequency of poles

R_O: Transconductance amplifier output resistor ≅ 1MΩ

C_O: Equivalent output capacitor ≅ 120p

Negative Voltage Feedback

Since the negative error amplifier has finite input impedance as shown in Figure 6, its induced error has to be considered. If a voltage divider is used to scale down the negative output voltage for the NFB pin, the equation for calculating output voltage is:

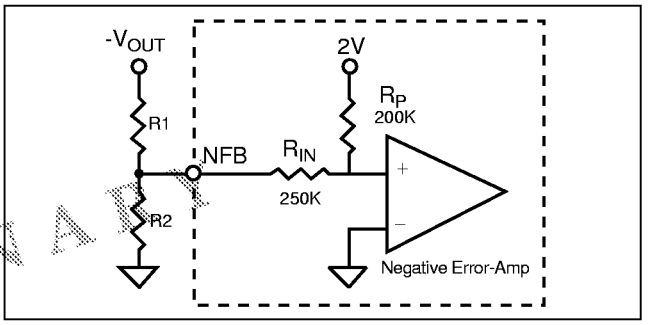


Figure 6: Negative Error Amplifier and N_{FB} pin

$$-V_{OUT} = \left(\frac{-2.5(R1 + R2)}{R2}\right) - 10\mu A \times R1$$

Application Information: continued

It is shown that if R1 is less than 10K, the deviation from the design target will be less than 0.1V. If the tolerances of the negative voltage reference and NFB pin input current are considered, the possible offset of the output V_{OFFSET} varies in the range of:

$$\left(\frac{-0.05\,(R1 + R2)}{R2}\right) - (15\mu A \times R1) \le V_{OFFSET} \le$$

$$\left(\frac{0.05\,(R1 + R2)}{R2}\right) - (5\mu A \times R1)$$

V_{SW} Voltage Limit

In the boost circuit the V_{SW} pin maximum voltage is set by the maximum output voltage plus output diode forward voltage. The diode forward voltage is typically 0.5V for Schottky diodes and 0.8V for ultrafast recovery diodes

$$V_{SW(MAX)} = V_{OUT(MAX)} + V_F$$

where:

V_F output diode forward voltage.

In the flyback circuit, the peak V_{SW} voltage is governed by:

$$V_{SW(MAX)} = V_{IN(MAX)} + (V_{OUT} + V_F) \times N$$

where N: transformer turns ratio primary over secondary.

When the power switch turns off there exists a voltage spike superimposed on top of the steady-state voltage. Usually this voltage spike is caused by transformer leakage inductance charging stray capacitance between the V_{SW} and PGnd pins. To prevent the voltage at the V_{SW} pin from exceeding the maximum rating, a transient voltage suppressor in series with a diode is paralleled with the primary windings. Another method of clamping switch voltage is to connect a transient voltage suppressor between the V_{SW} pin and ground.

Magnetic Component Selection

When choosing a magnetic component, one has to consider factors such as peak current, core and ferrite material, output voltage ripple, EMI, temperature range, physical size and cost. In boost circuits, the average inductor current is output current times voltage gain (V_{OUT}/V_{IN}), assuming 100% energy transfer efficiency. In continuous conduction mode, inductor ripple current is

$$I_{RIPPLE} = \frac{V_{IN}(V_{OUT}-V_{IN})}{(f)(L)(V_{OUT})}$$

Where f is 260kHz for CS5171/2 and 520kHz for CS5173/4. The peak inductor current is equal to average current plus half of the ripple current, which should not cause inductor saturation. The above equation can also be referenced on selecting the value of the inductor based on the tolerance of the ripple current in the circuits. Small ripple current provides the benefits of small input capacitors and greater output current capability. A core geometry, like a rod or barrel, is prone to generating high magnetic field radiation, but is relatively cheap and small. Other core geometry, such as a toroid, provides a closed magnetic loop to prevent EMI.

Input Capacitor Selection

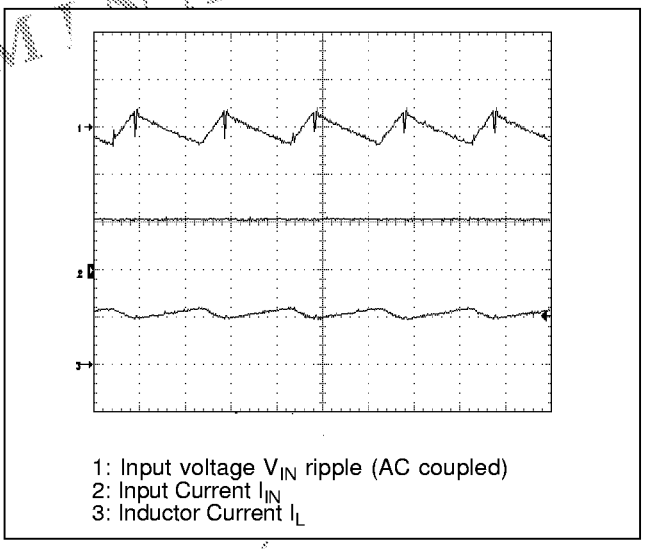


Figure 7a: Typical input voltage and current ripple waveforms.

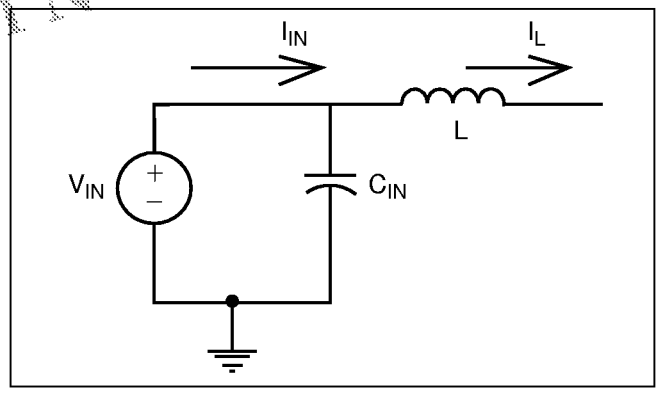


Figure 7b: Typical input voltage and current ripple waveforms.

In boost circuits, the inductor becomes part of the input filter shown in Figure 7b. In continuous mode, the input current waveform is triangular and does not contain a large

pulsed current, as shown in Figure 7a. This reduces the requirements imposed on the input capacitor selection. During continuous conduction mode, the peak to peak inductor ripple current is given in the previous section. As we can see from Figure 7, the product of the inductor current ripple and the input capacitor's effective series resistor (ESR) determine the V_{IN} ripple. In most applications, capacitors in the range of 10μF to 100μF with an ESR less than 0.3Ω work well up to a full 1.5A switch current.

The situation is different in a flyback circuit. The input current is discontinuous and a significant pulsed current is witnessed by the input capacitors. Therefore, there are two requirements for capacitors in a flyback regulator, energy storage and filtering. To maintain a stable voltage supply to the chip, a storage capacitor larger than 20μF with low ESR is required. In addition, a small bypass capacitor may be necessary to reduce the noise generated by the inductor. To reduce the noise, insert a 1.0μF ceramic capacitor between V_{IN} and ground as close as possible to the chip.

Output Capacitor Selection

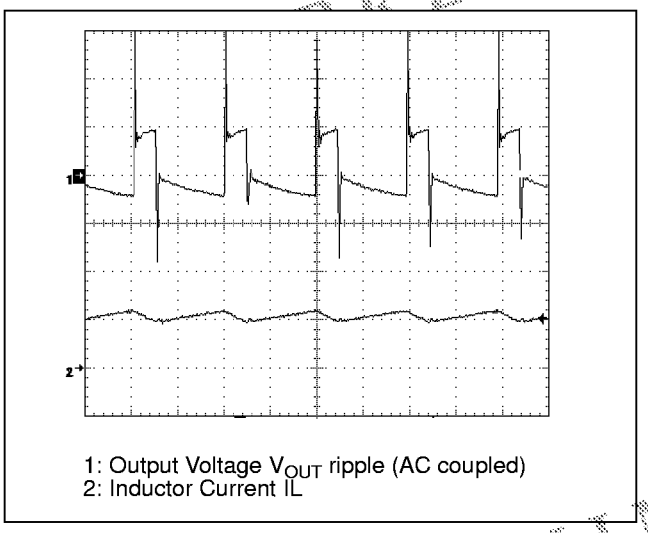


Figure 8: Typical output voltage ripple.

By examining the waveforms shown in Figure 8, we can see that the output voltage ripple comes from two major sources, namely, capacitor ESR and the charging/discharging of the output capacitor. In boost circuits, when the power switch turns off, I_L flows into the output capacitor causing an instant $\Delta V = I_{IN} \times ESR$. At the same time, current I_L-I_{OUT} charges the capacitor and increases the output voltage gradually. When the power switch is turned on, I_L is shunted to the ground and I_{OUT} discharges the output capacitor. When the I_L ripple is small enough, I_L can be treated as the constant and is equal to input current I_{IN}. Summing up, the output voltage peak-peak ripple can be calculated by:

$$V_{OUT(RIPPLE)} = \frac{(I_{IN}\text{-}I_{OUT})(1\text{-}D)}{(C_{OUT})(f)} + \frac{I_{OUT}D}{(C_{OUT})(f)} + I_{IN} \times ESR$$

The equation can be expressed more conveniently in terms of V_{IN}, V_{OUT} and I_{OUT} for design purposes as follows:

$$V_{OUT(RIPPLE)} = \frac{I_{OUT}(V_{OUT}\text{-}V_{IN})}{V_{OUT}} \times \frac{1}{(C_{OUT})(f)} +$$

$$\frac{(I_{OUT})(V_{OUT})(ESR)}{V_{IN}}$$

The capacitor RMS ripple current is:

$$I_{RIPPLE} = \sqrt{(I_{IN}\text{-}I_{OUT})^2(1\text{-}D) + (I_{OUT})^2(D)} = I_{OUT}\sqrt{\frac{V_{OUT}\text{-}V_{IN}}{V_{IN}}}$$

Although the above equations apply only for boost circuits, similar equations can be derived for flyback circuits.

Circuit Layout Guidelines

In any switching power supply, circuit layout is very important for proper operation. Rapidly switching currents combined with trace inductance generates voltage transitions that can cause problems. Therefore the following guidelines should be followed in the layout.

1. In boost circuits, high AC current circulates within the loop composed of the diode, output capacitor, and on-chip power transistor. The length of associated traces and leads should be kept as short as possible. In the flyback circuit, high AC current loops exist on both sides of the transformer. On the primary side, the loop consists of the input capacitor, transformer, and on-chip power transistor, while the transformer, rectifier diodes, and output capacitors form another loop on the secondary side. Just as in the boost circuit, all traces and leads containing large AC currents should be kept short.
2. Separate the low current signal grounds from the power grounds. Use single point grounding or ground plane construction for the best results.
3. Locate the voltage feedback resistors as near the IC as possible to keep the sensitive feedback wiring short. Connect feedback resistors to the low current analog ground.

Additional Application Circuits

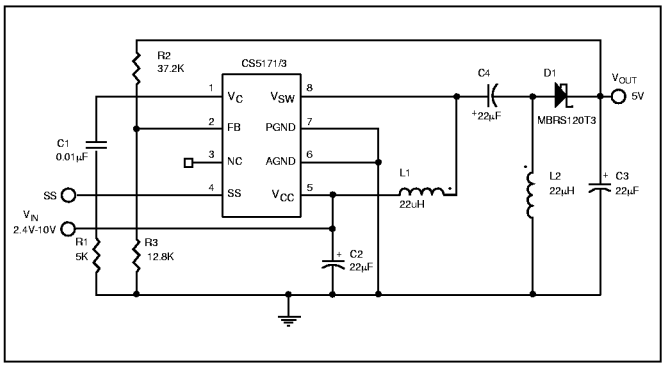


Figure 9: 2.4V-10V to 5V Sepic Converter.

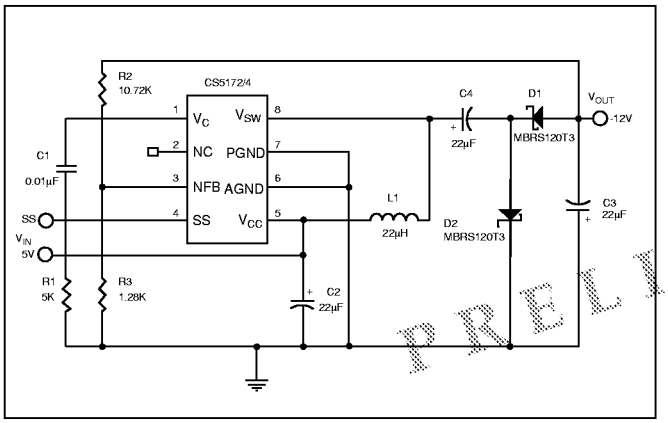


Figure 10: 5V to -12V Inverting Converter.

Package Specification

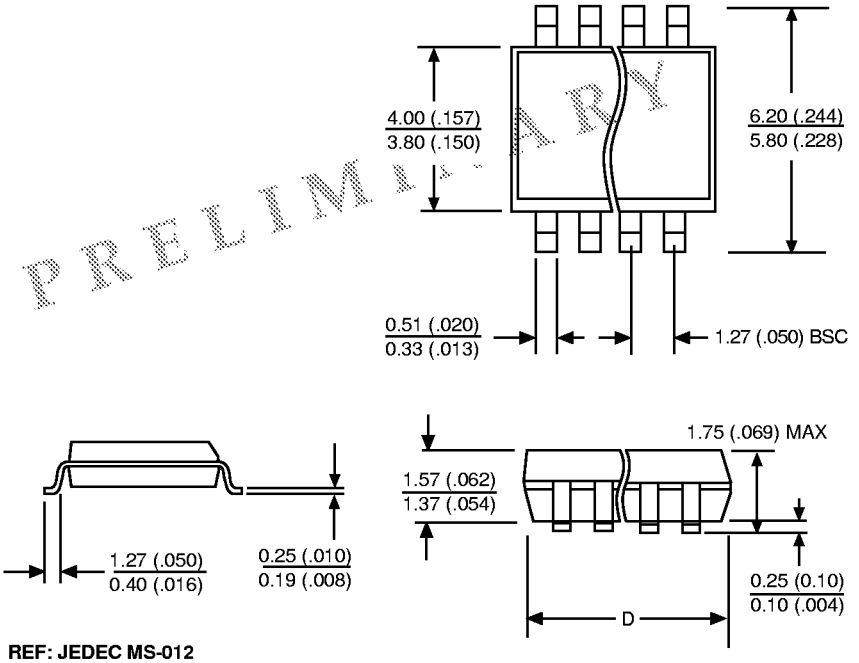
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8 Lead SO Narrow	5.00	4.80	.197	.189

PACKAGE THERMAL DATA

Thermal Data		8L SO Narrow	
$R_{\Theta JC}$	typ	45	°C/W
$R_{\Theta JA}$	typ	165	°C/W

Surface Mount Narrow Body (D); 150 mil Wide



REF: JEDEC MS-012

PRELIMINARY

Ordering Information

Part Number	Description
CS5171ED8	8L SO Narrow
CS5171EDR8	8L SO Narrow *(tape & reel)*
CS5172ED8	8L SO Narrow
CS5172EDR8	8L SO Narrow *(tape & reel)*
CS5173ED8	8L SO Narrow
CS5173EDR8	8L SO Narrow *(tape & reel)*
CS5174ED8	8L SO Narrow
CS5174EDR8	8L SO Narrow *(tape & reel)*

Preliminary

This product is in the preproduction stages of the design process. The data sheet contains preliminary data. Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.

