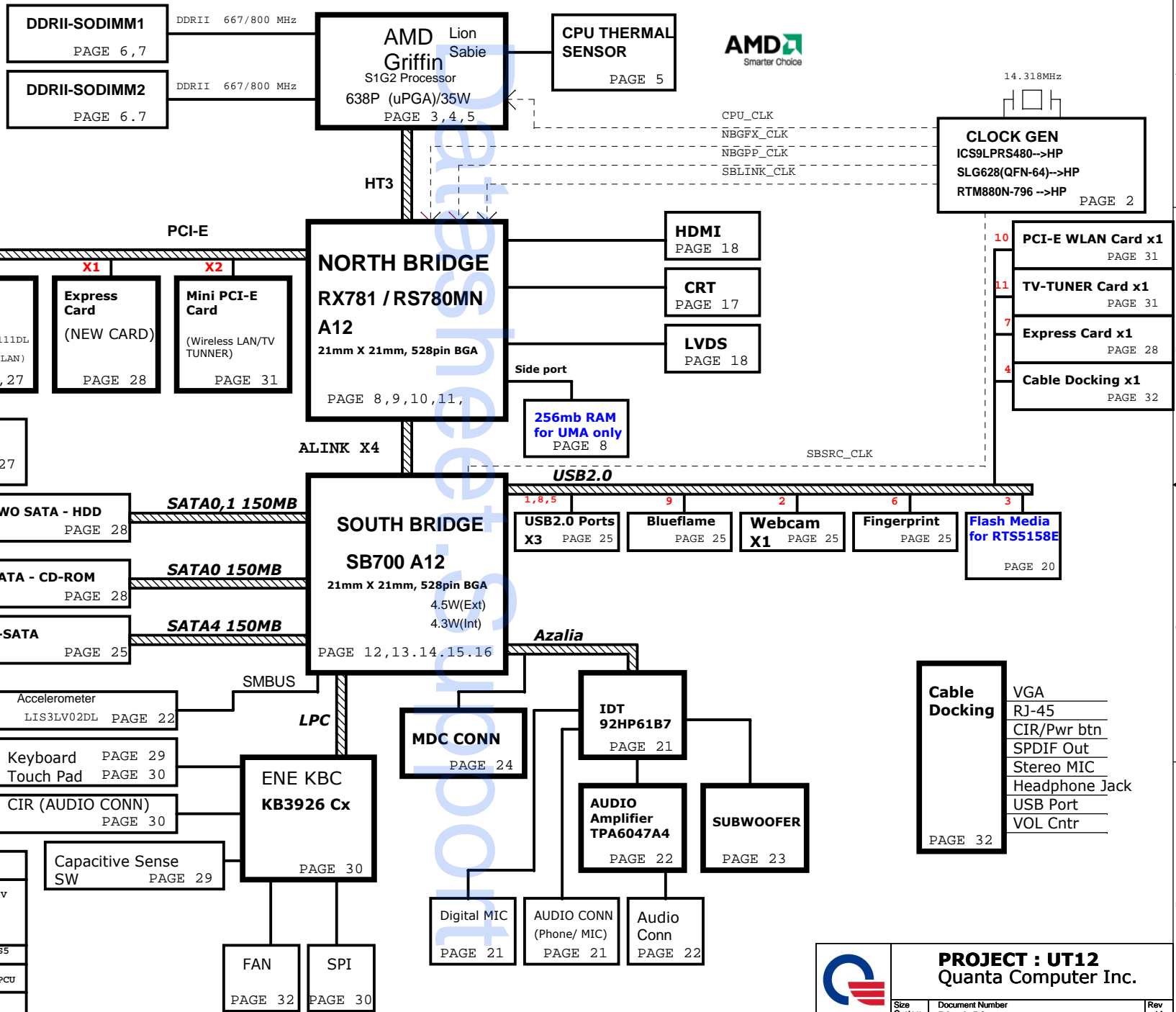


UT12(UMA) SYSTEM DIAGRAM

01

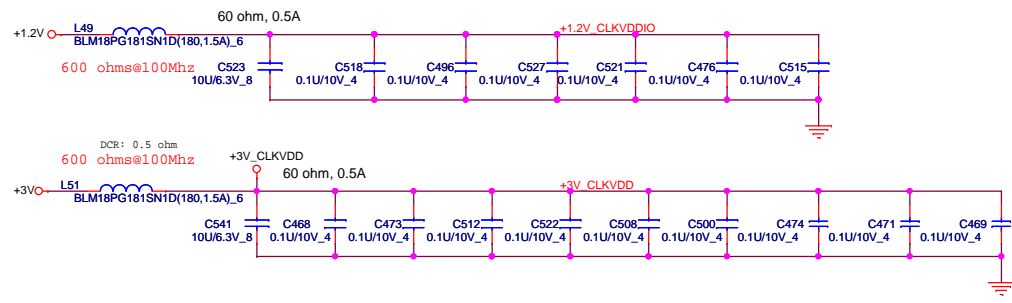
PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : IN1
- LAYER 3 : IN2
- LAYER 4 : VCC
- LAYER 5 : IN3
- LAYER 6 : BOT

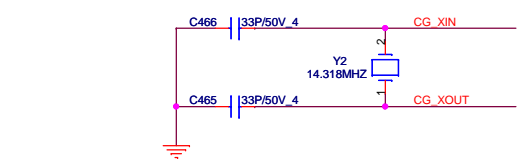
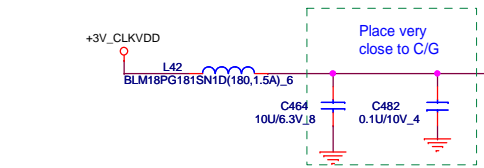


PROJECT : UT12
Quanta Computer Inc.

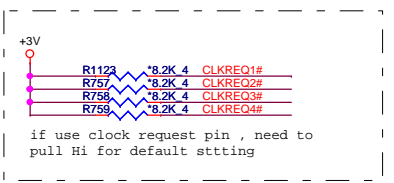
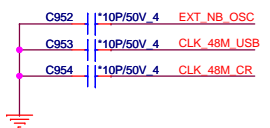
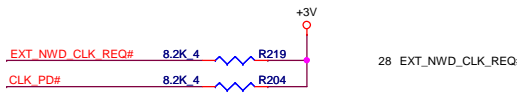
Size Custom	Document Number Block Diagram	Rev 1A
Date: Monday, November 10, 2008	Sheet 1 of 40	



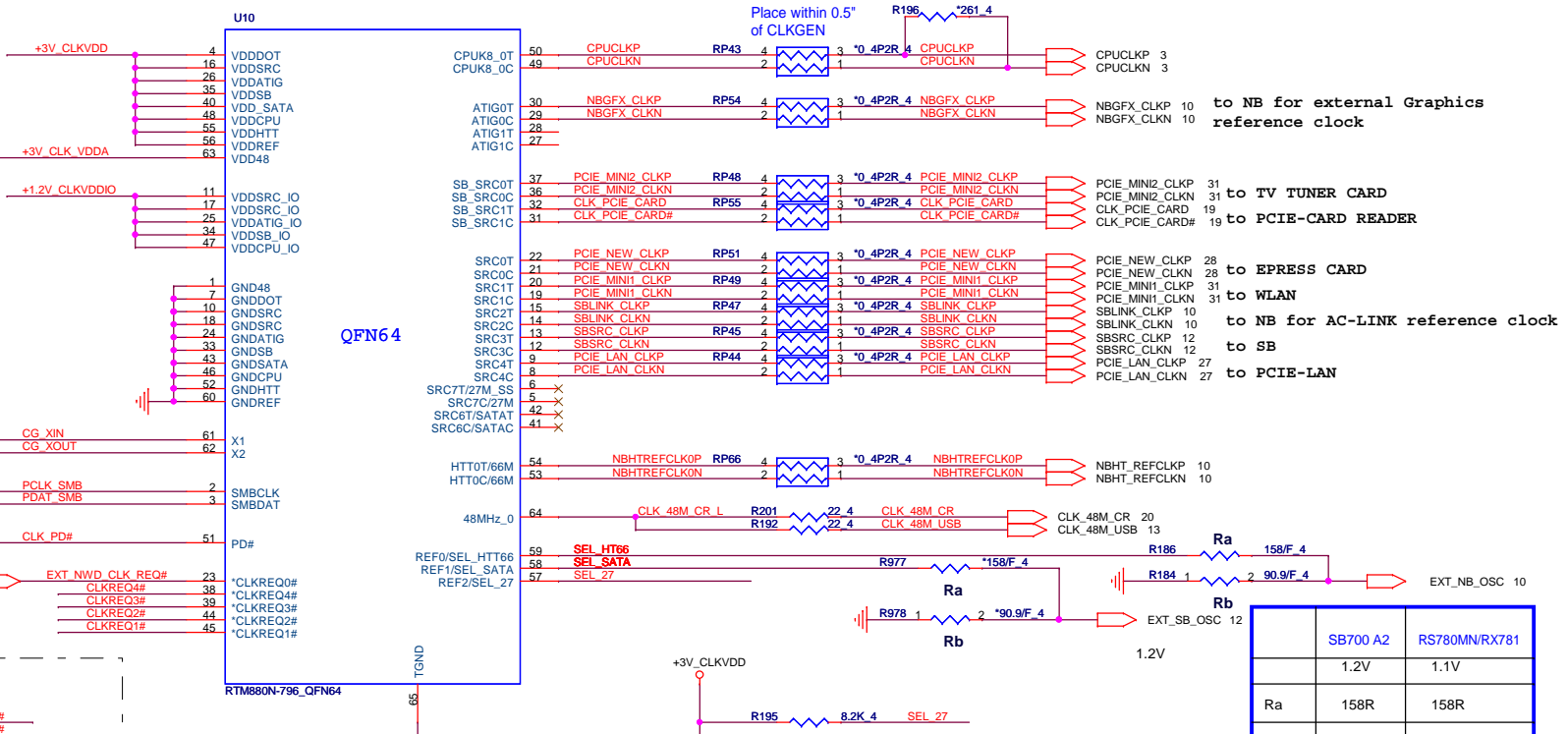
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



can remove MOSFET level shift SB/clock gen / DDR2 is 3.3V/S0 power level



if use clock request pin , need to pull Hi for default stting



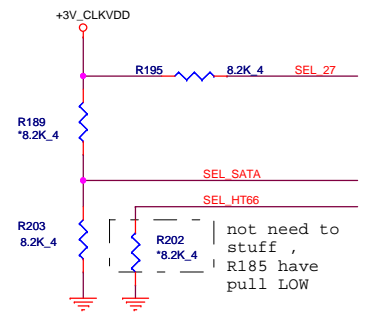
	SB700 A2	RS780M/RX781
	1.2V	1.1V
Ra	158R	158R
Rb	90.9R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS0902FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

ICS ICS9LPRS480
SLG SLG628(QFN-64)
RTL RTM880N-796-- AL000880001

* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock



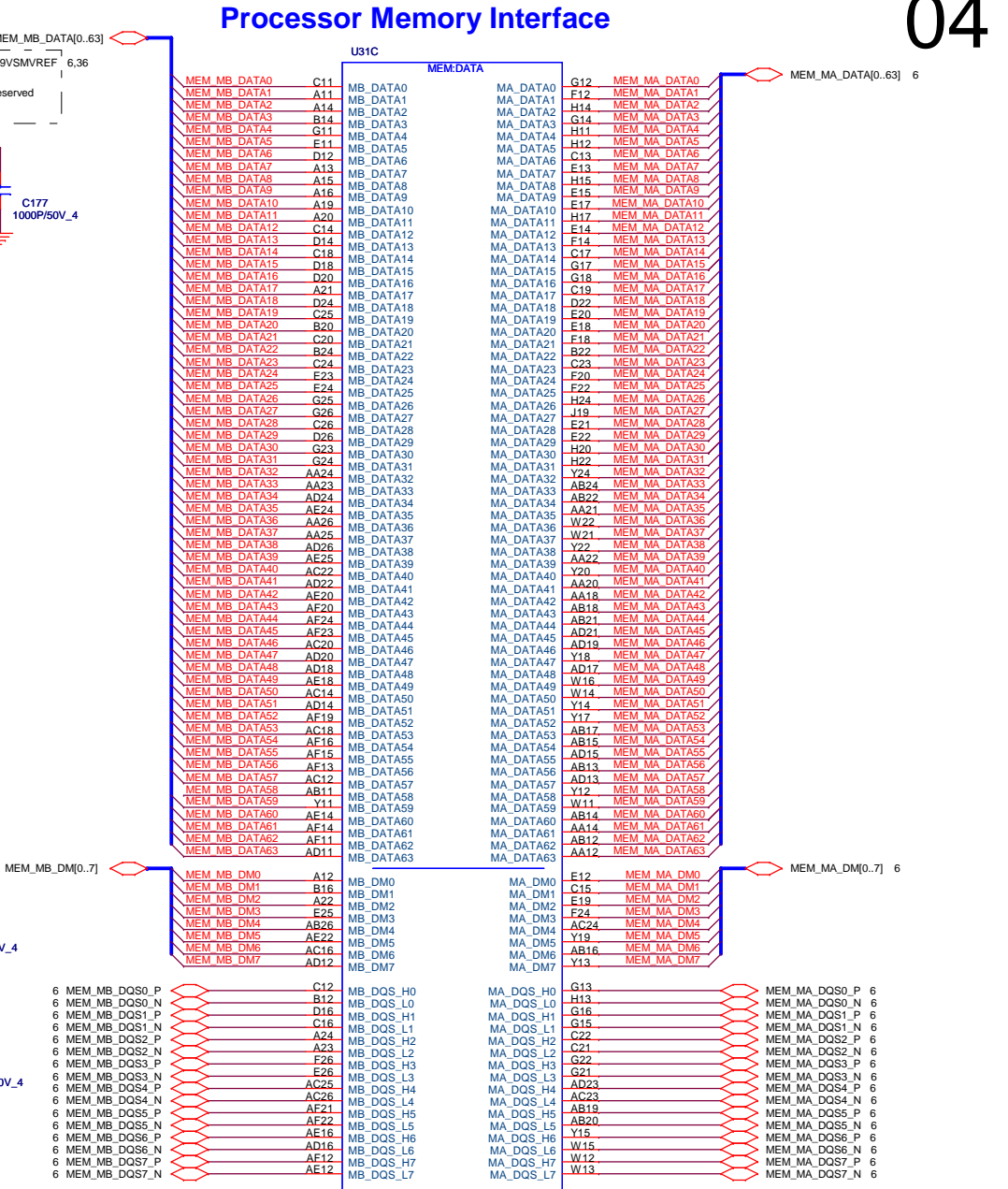
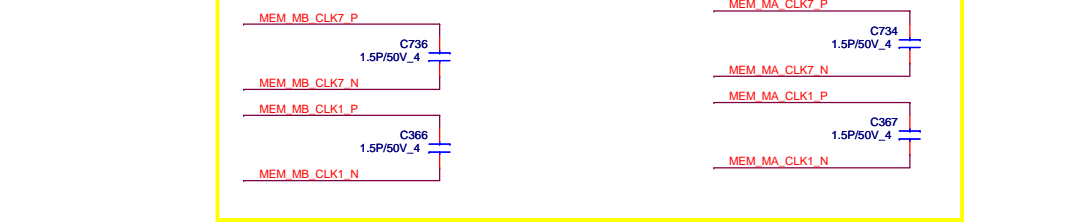
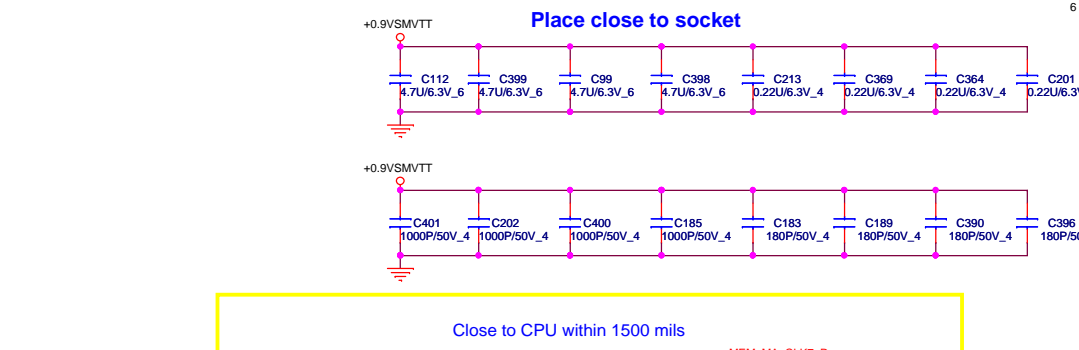
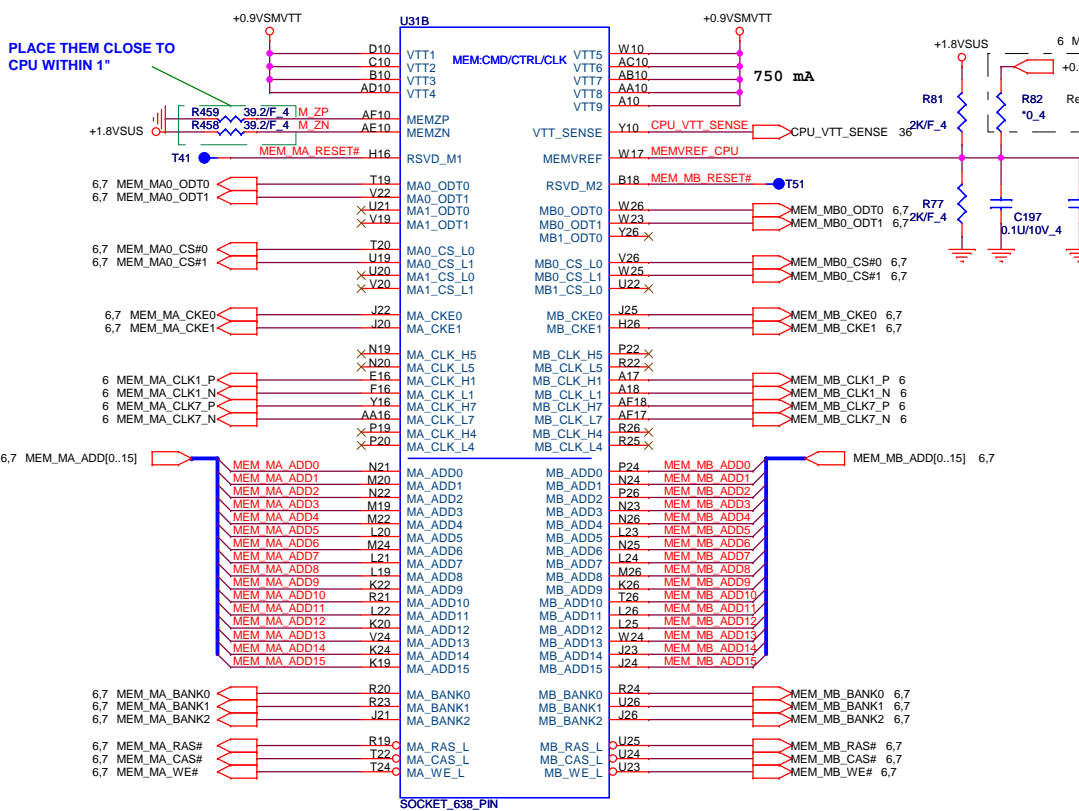
not need to stuff , R185 have pull LOW



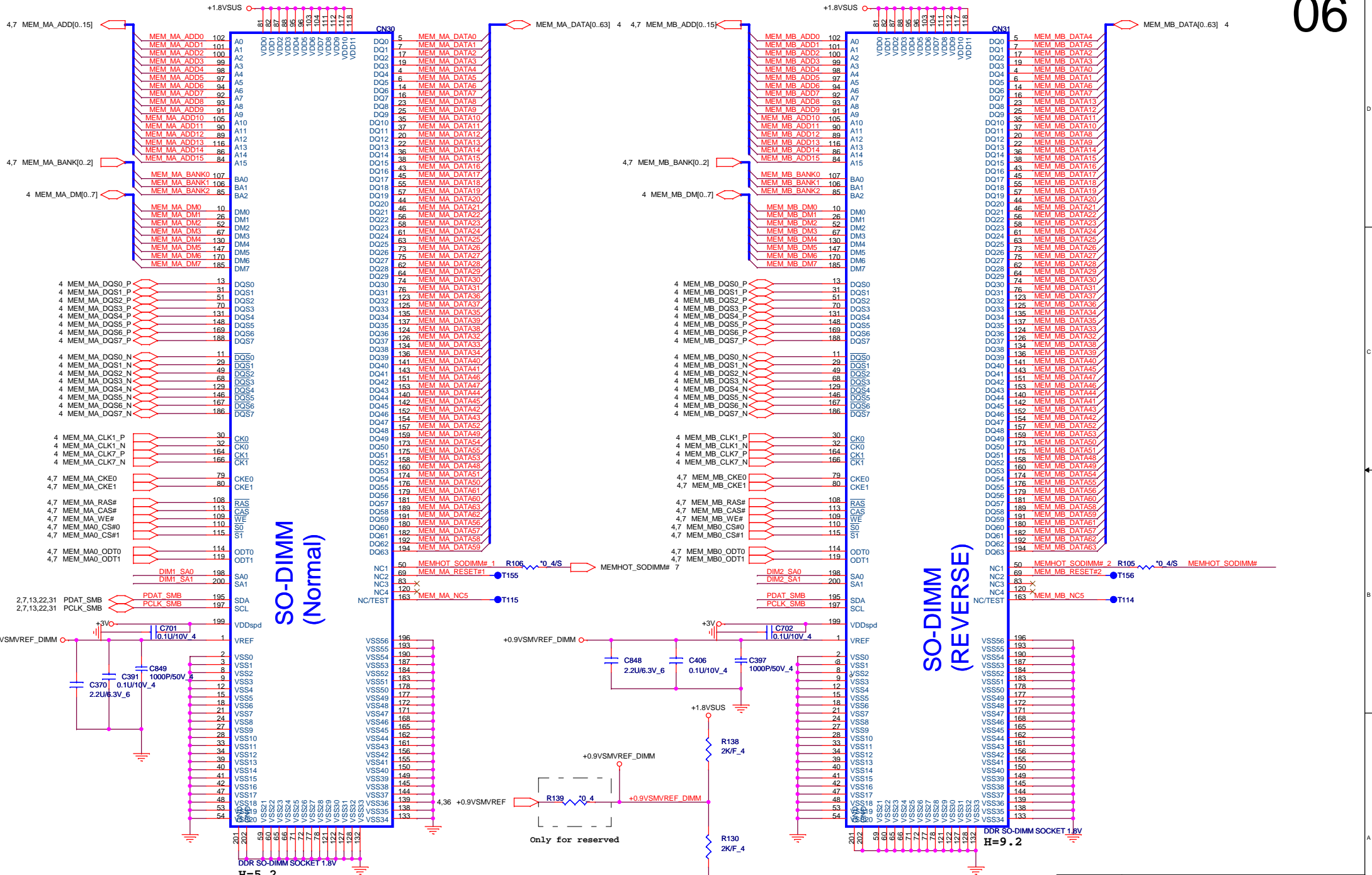
PROJECT : UT12
Quanta Computer Inc.

Processor Memory Interface

PLACE THEM CLOSE TO CPU WITHIN 1"



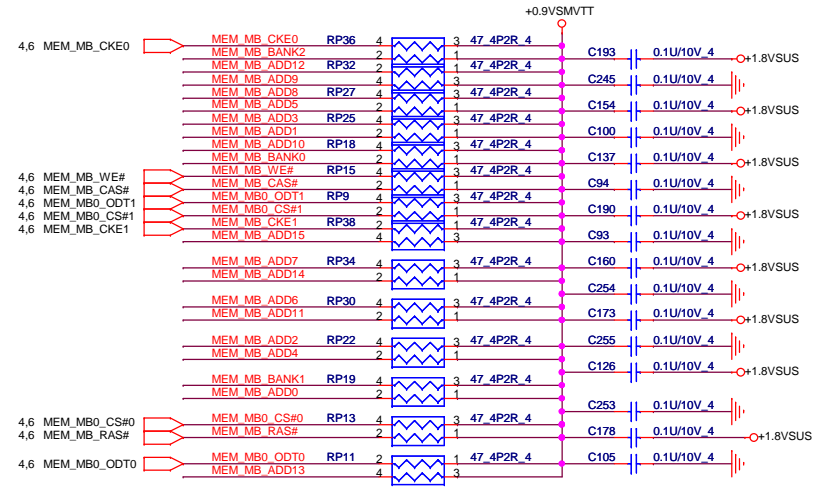
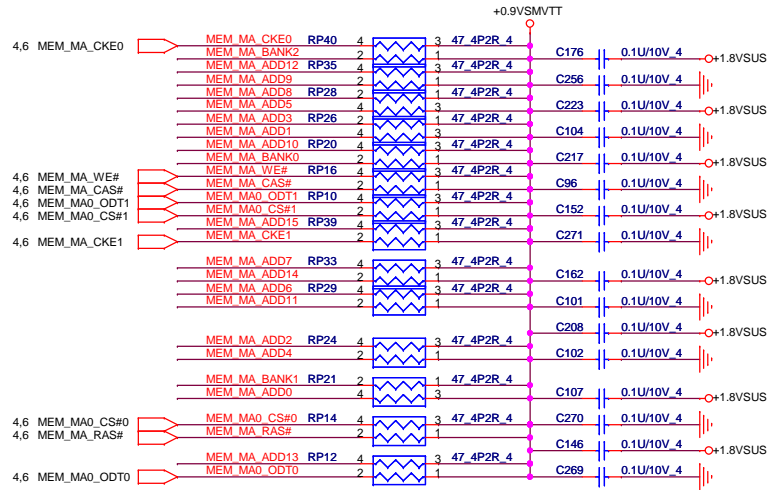
PROJECT : UT12
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PROJECT : UT12
Quanta Computer Inc.

4,6 MEM_MA_ADD[0..15] MEM_MA_ADD[0..15]
 4,6 MEM_MA_BANK[0..2] MEM_MA_BANK[0..2]

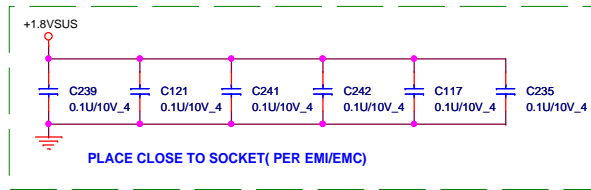
4,6 MEM_MB_ADD[0..15] MEM_MB_ADD[0..15]
 4,6 MEM_MB_BANK[0..2] MEM_MB_BANK[0..2]



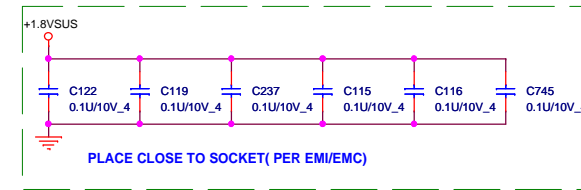
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



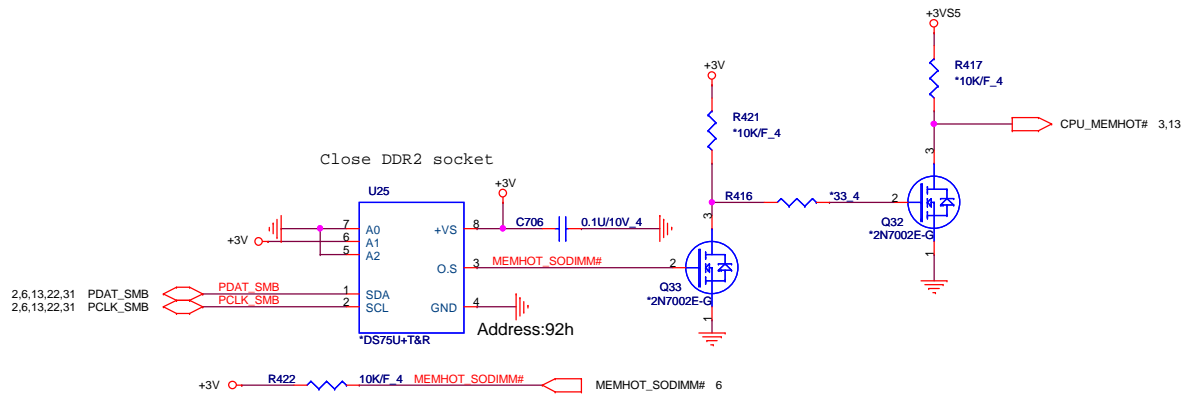
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



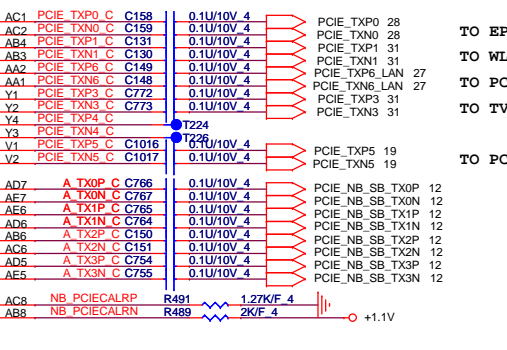
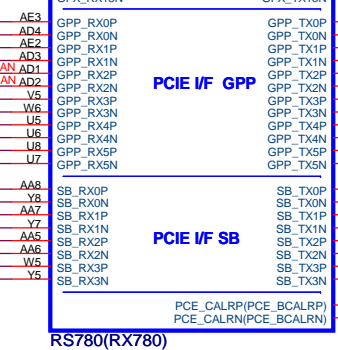
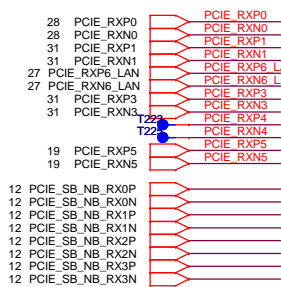
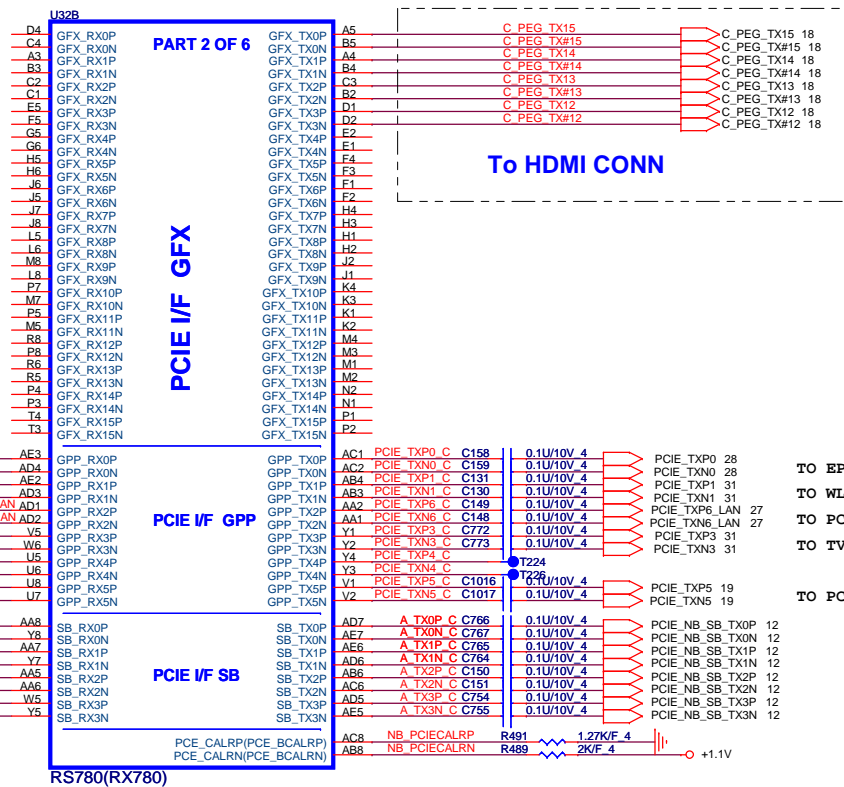
PLACE CLOSE TO SOCKET (PER EMI/EMC)



PLACE CLOSE TO SOCKET (PER EMI/EMC)



	PROJECT : UT12 Quantia Computer Inc.	
	Size Custom	Document Number DDR2 SODIMMS TERMINATIONS
Date: Monday, November 10, 2008		Sheet 7 of 40



- TO EPRESS CARD
- TO WLAN
- TO PCIE-LAN
- TO TV TUNNER
- TO PCIE CARD READER

RX780/RS740/RS780 difference table (PCIE LINK)

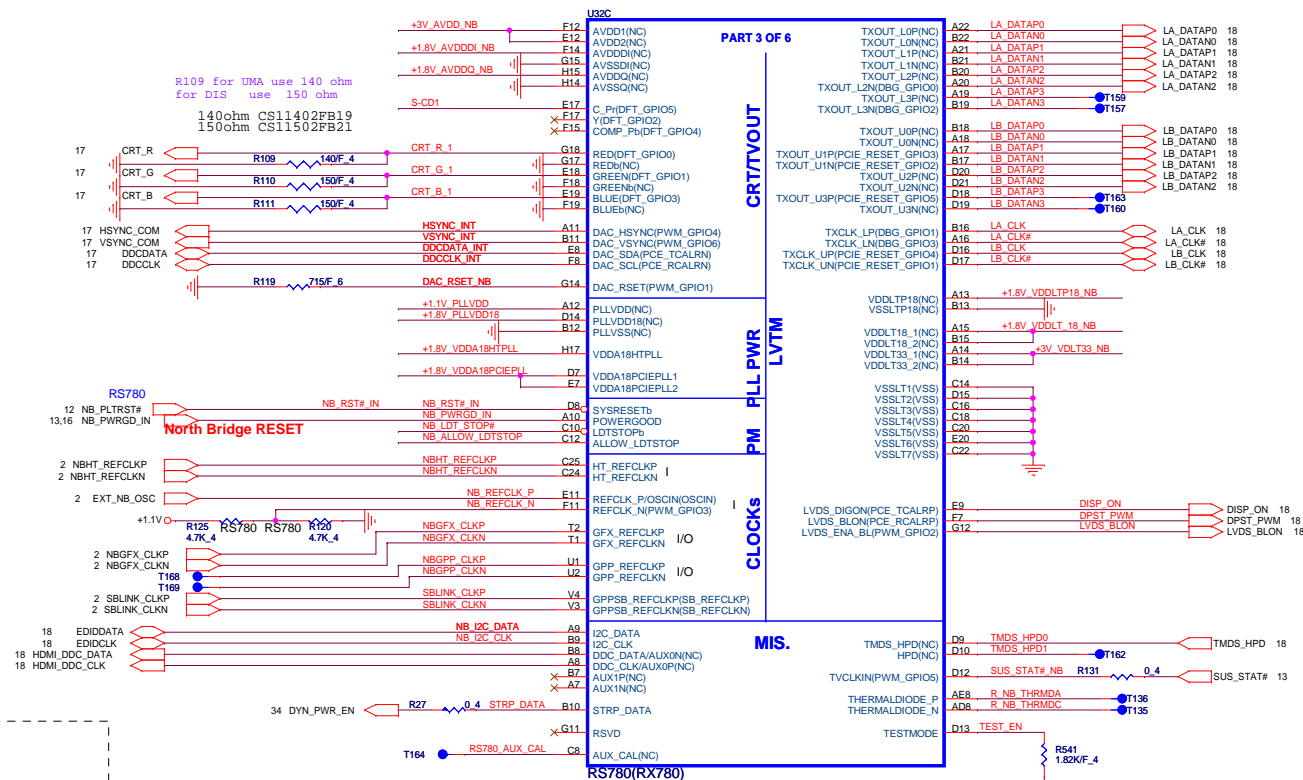
	RS740	RX780/RS780
NB_PCIEALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

PROJECT : UT12
Quanta Computer Inc.

Size Custom	Document Number RS740/RS780-PCIE I/F 2/5	Rev 1A
Date: Monday, November 10, 2008 Sheet 9 of 40		



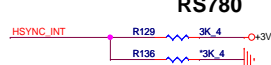
selects Loading of straps from EPROM
 1 : use default vaule , default
 0 : I2C Master can load strap values from EEPROM
 if connected, or use default values if not connected
 RX780 --RS780_AUX_CAL
 RS780 -- SUS_ATAT



Enables Debug Bus access through memory T/O pads and GPIO.
 0 : Enable RS780 , Default
 1 : Disable RS780
 (RS780 use VSYNC#)



Indicates if memory Side port is available or not
 0 : available RS780 , Default
 1 : Not available RS780
 (RS780 use VSYNC#)



For extrnal EEPROM Debug only

RS780/RX780

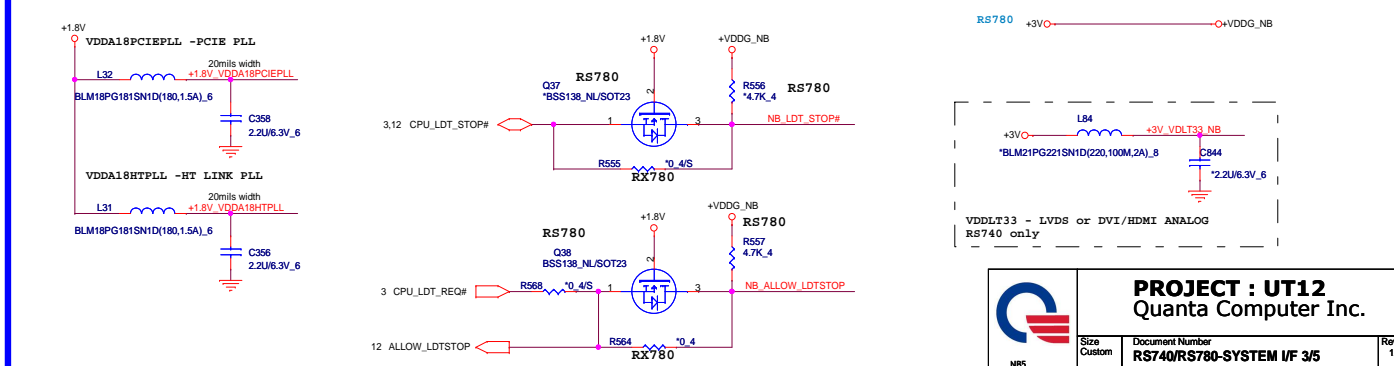
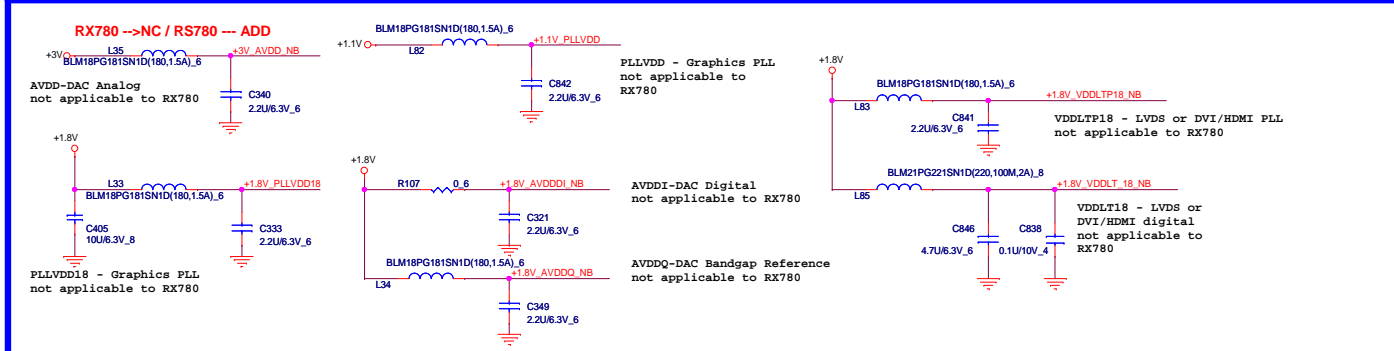


Enables Debug Bus access through memory T/O pads and GPIO.
 1 : Enable RX780 , Default
 0 : Disable RX780

RX780

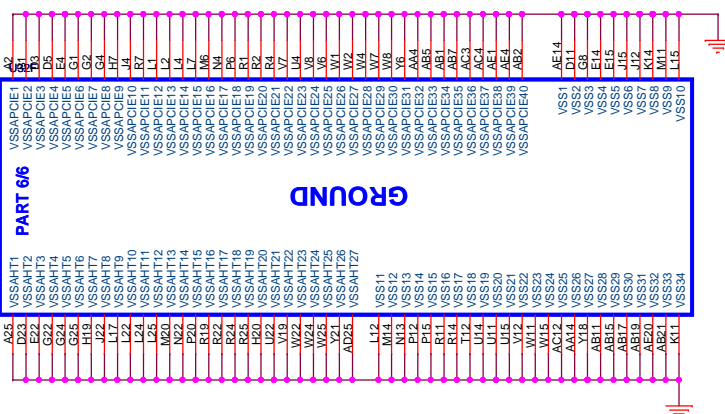


Reserved only



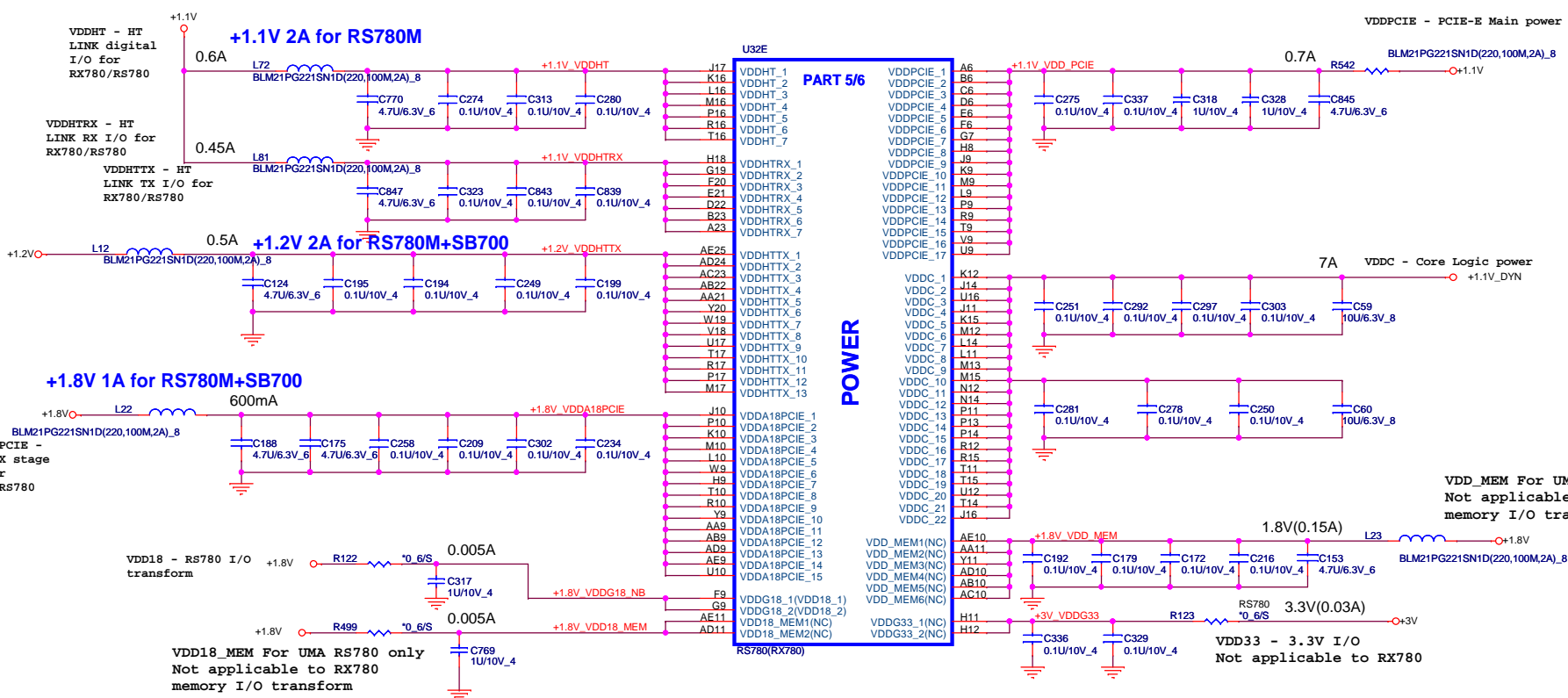
PROJECT : UT12
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	RS740/RS780-SYSTEM I/F 3/5	
Date: Monday, November 10, 2008	Sheet 10 of 40	



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDL33	NC	NC

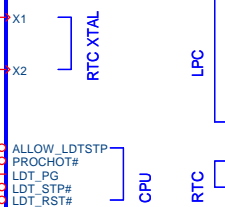
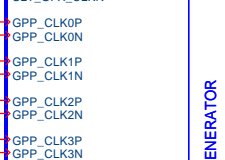
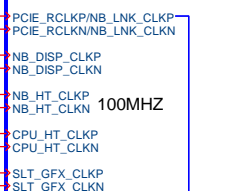
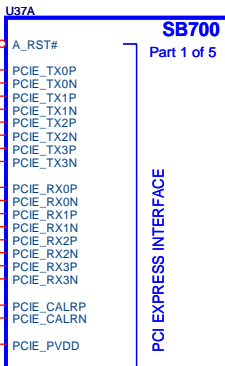
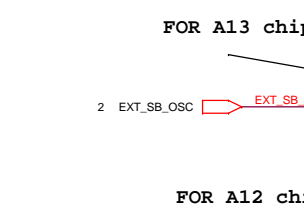
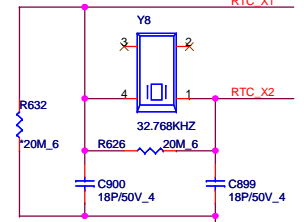
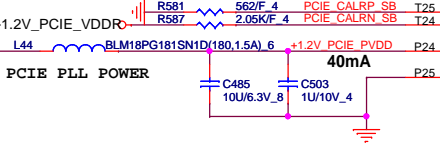
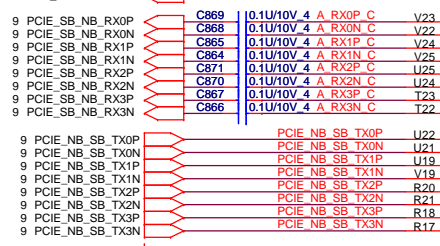
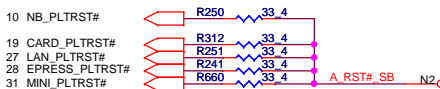


PROJECT : UT12
Quanta Computer Inc.

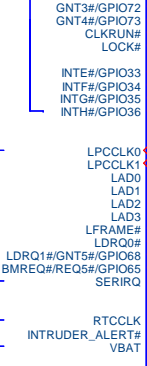
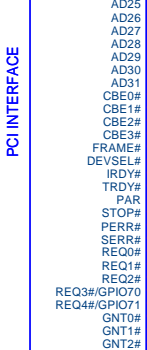
Size Custom	Document Number RS740/RS780-POWER5/5	Rev 1A
Date: Monday, November 10, 2008 Sheet 11 of 40		

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

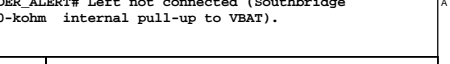
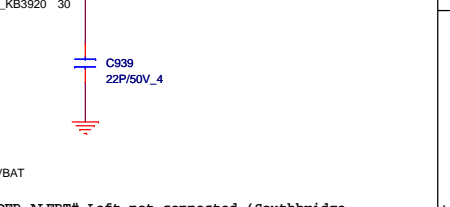
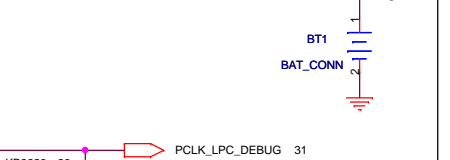
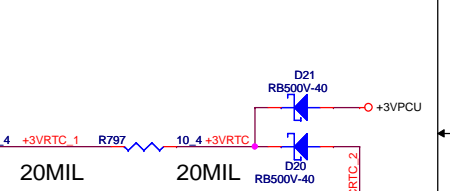
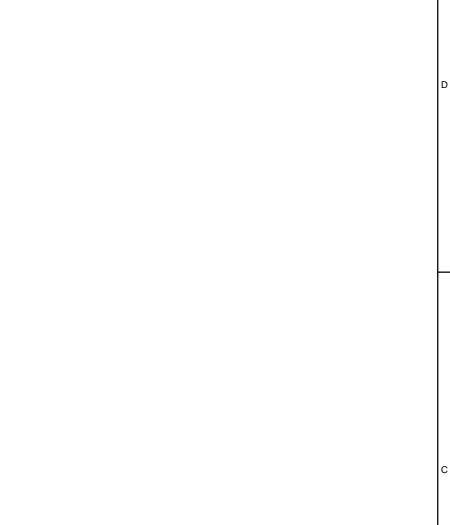
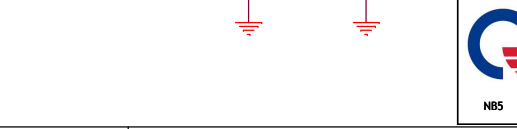
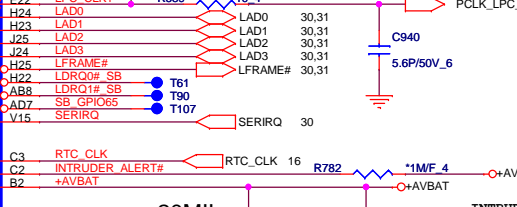
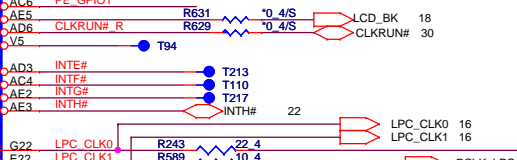
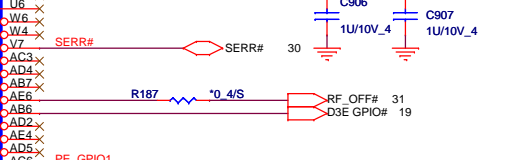
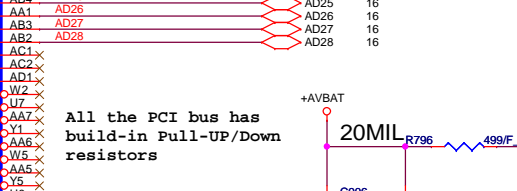
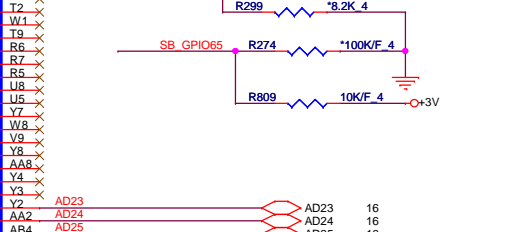
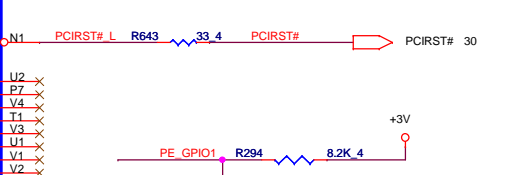
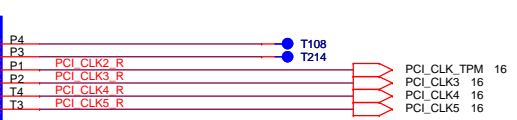
To RS780



SB700
 IC CTRL(528P) SB700 All(218S7EAL11FG)
 P/N : AJALAL10T00



SB700
 IC CTRL(528P) SB700 All(218S7EAL11FG)
 P/N : AJALAL10T00



PROJECT : UT12
 Quantal Computer Inc.

Size Custom	Document Number SB700-PCIE/PCU/CPU/LPC 1/4	Rev 1A
Date: Monday, November 10, 2008	Sheet 12 of 40	

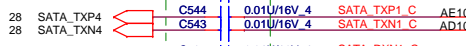
SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB700

SATA1



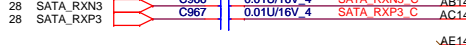
SATA ODD



E-SATA

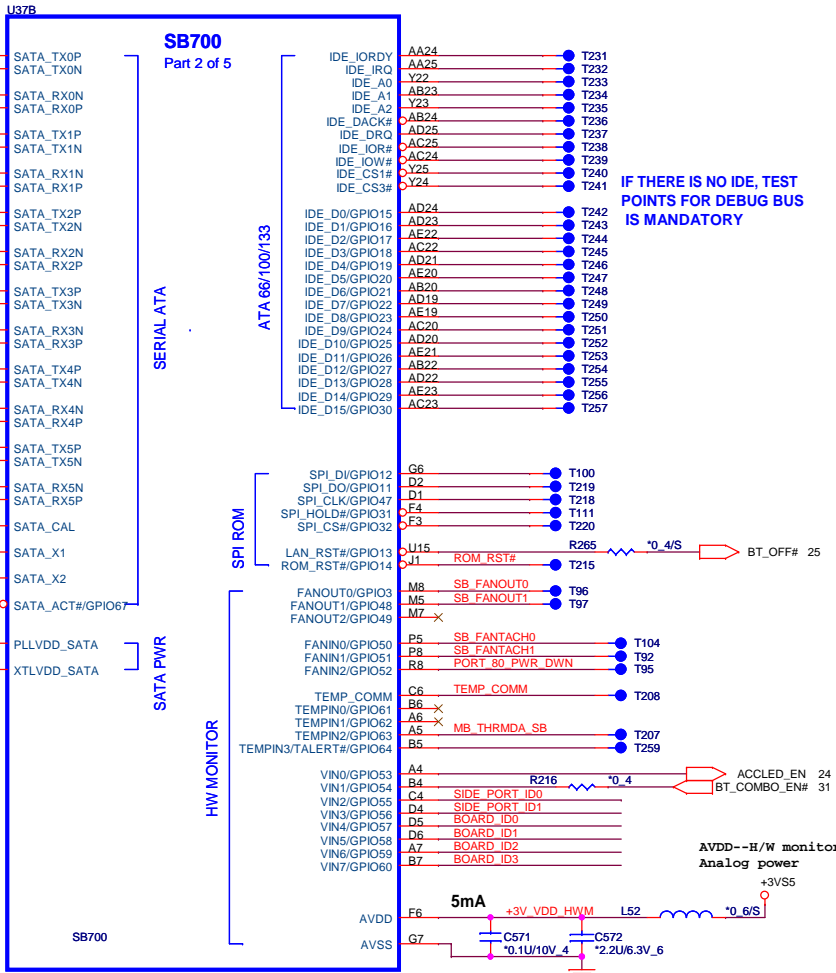
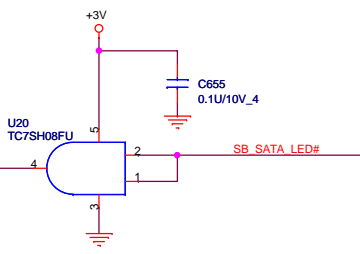
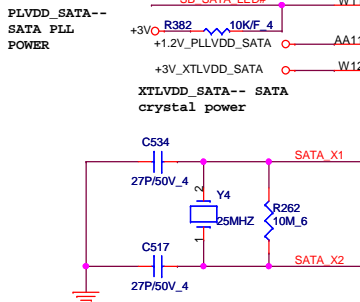


SATA HDD2



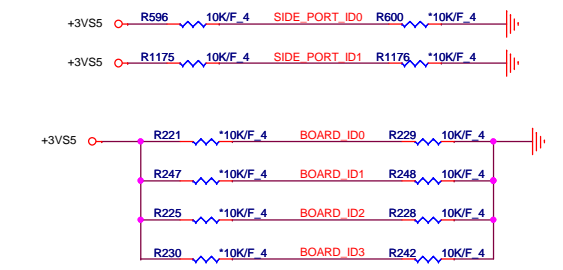
SATA PORT 4,5
are only
support IDE
mode

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

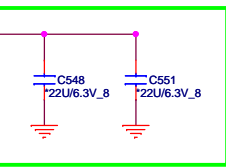


IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	Samsung
0	1	Qimonda
1	0	Hynix
1	1	no support side port



ID3	ID2	ID1	ID0	
0	0	0	0	UT1 UMA
0	0	0	1	UT2 UMA
0	0	1	0	UT1 M92
0	0	1	1	UT2 M92
0	1	0	0	UT1 M96
0	1	0	1	UT2 M96
0	1	1	0	
0	1	1	1	

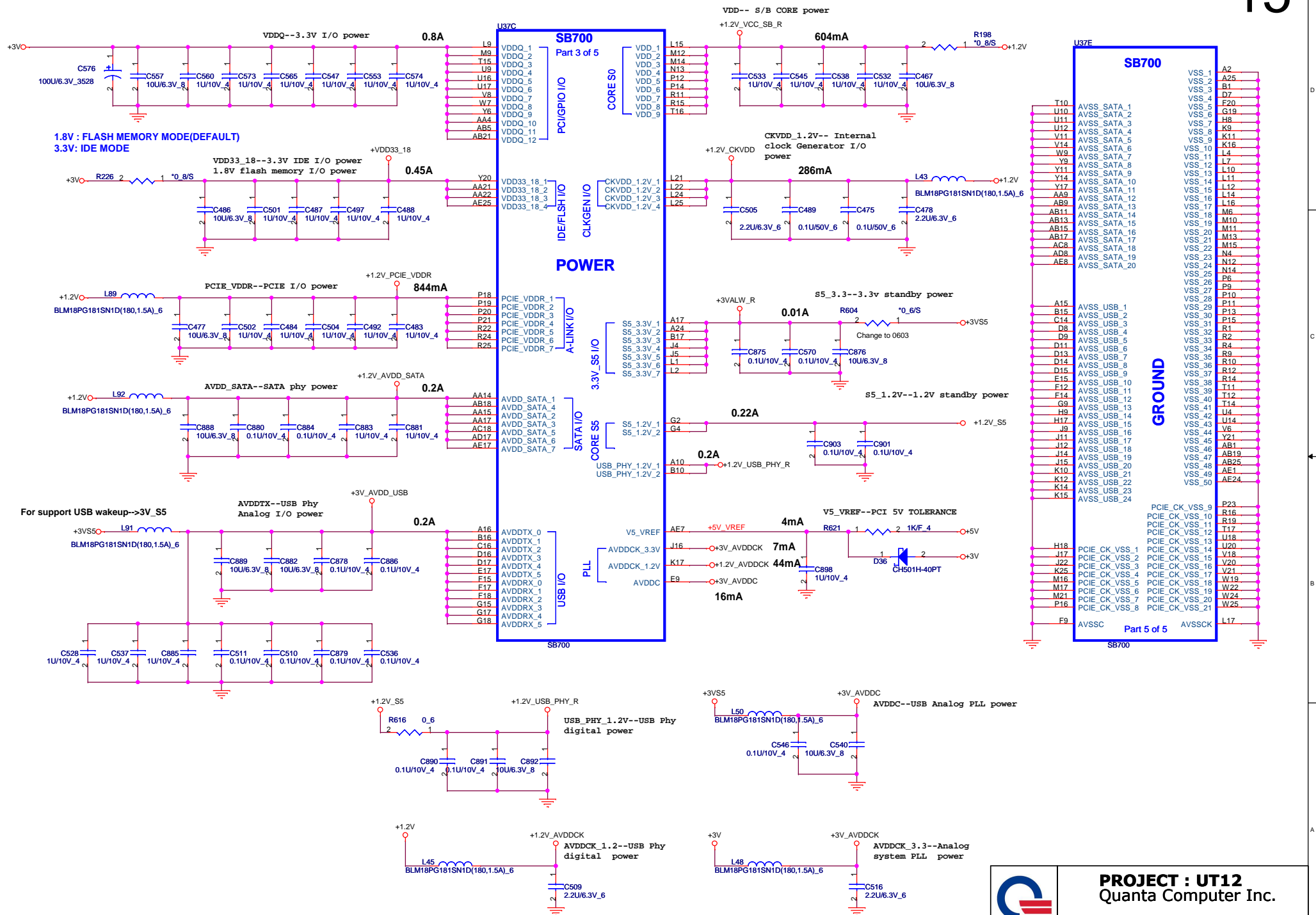


SI stage remove C548 , C551



PROJECT : UT12
Quantal Computer Inc.

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



PROJECT : UT12
Quanta Computer Inc.

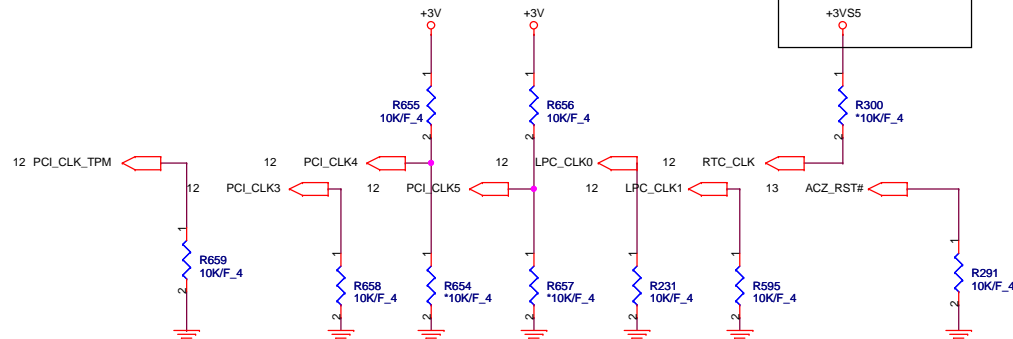
Size Custom	Document Number SB700-PWR/DECOUPLING 4/4	Rev 1A
Date: Monday, November 10, 2008		Sheet 15 of 40



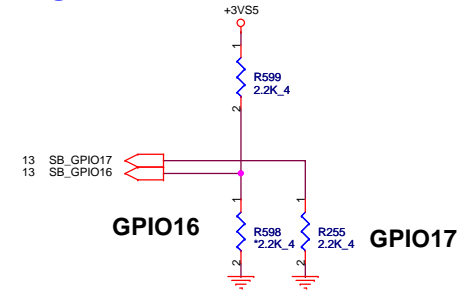
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

It must ready before RSMRST#



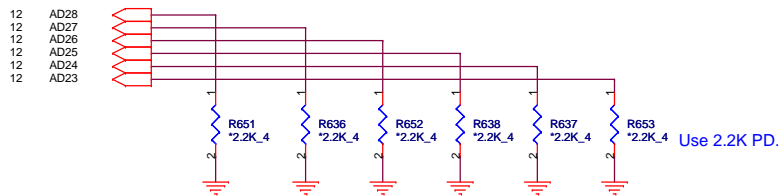
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

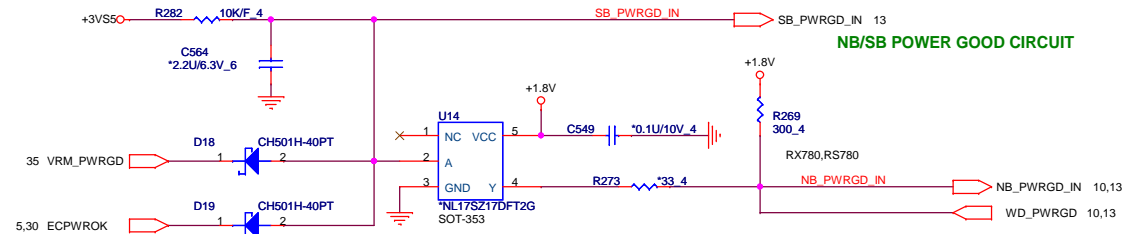
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

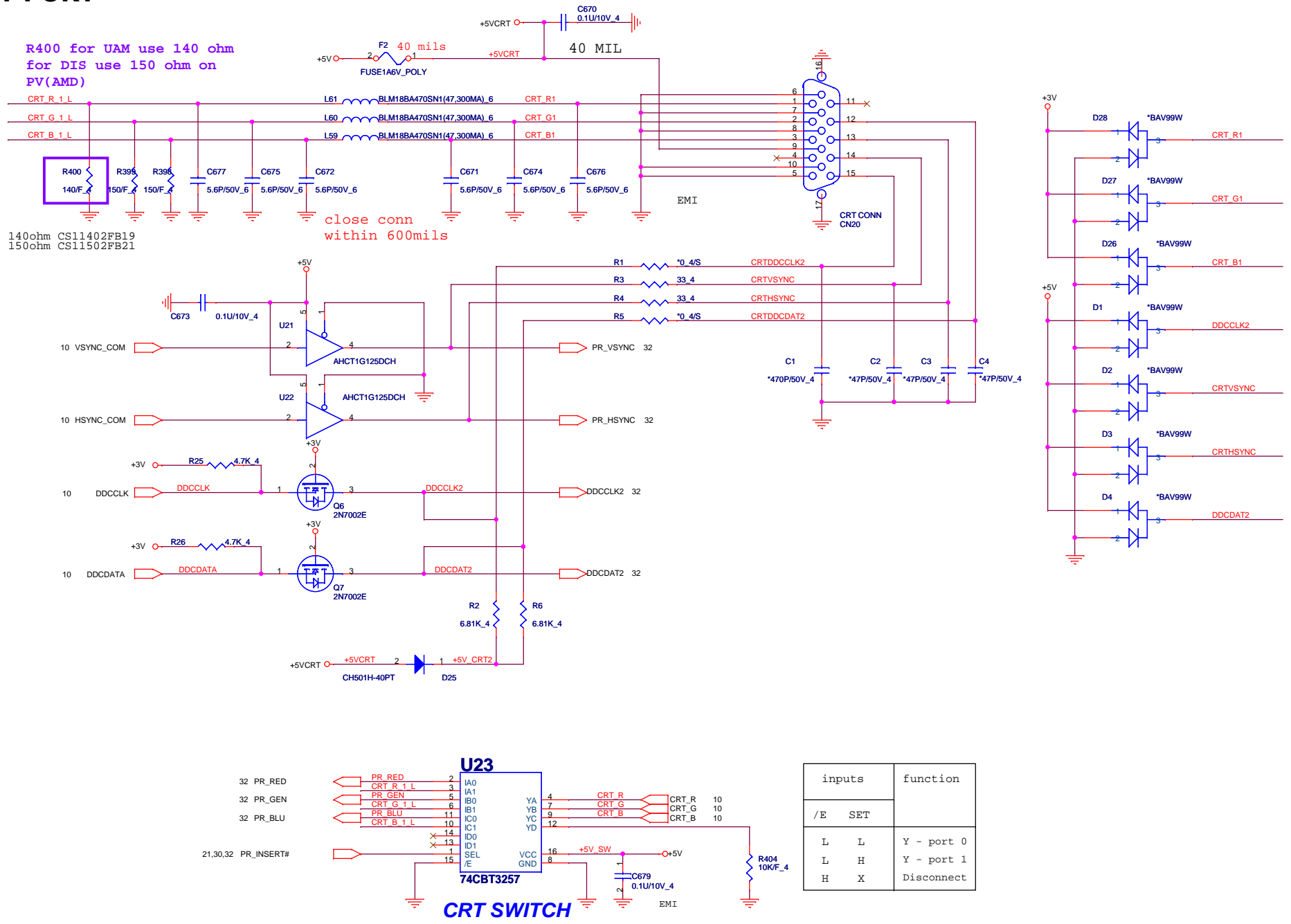
NB_PWRGD_IN: RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

PROJECT : UT12
Quanta Computer Inc.

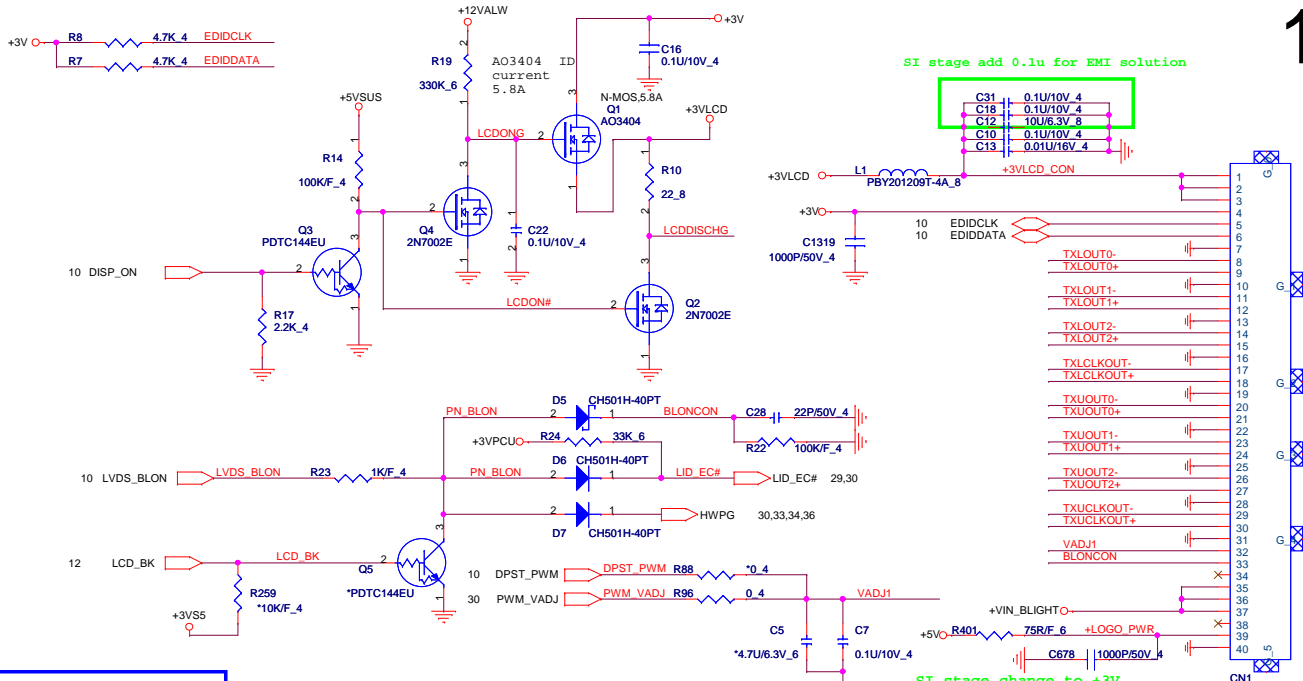
Size Custom Document Number **SB700-STRAPS** Rev 1A
Date: Monday, November 10, 2008 Sheet 16 of 40



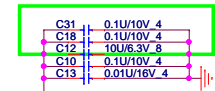
PROJECT : UT12
Quanta Computer Inc.

OPTION SIGNAL FROM NB to LVDS for UMA

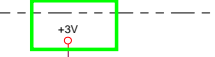
10	LA_CLK	LA_CLK	TXLCLKOUT+
10	LA_CLK#	LA_CLK#	TXLCLKOUT-
10	LA_DATAP0	LA_DATAP0	TXLOUT0+
10	LA_DATAN0	LA_DATAN0	TXLOUT0-
10	LA_DATAP1	LA_DATAP1	TXLOUT1+
10	LA_DATAN1	LA_DATAN1	TXLOUT1-
10	LA_DATAP2	LA_DATAP2	TXLOUT2+
10	LA_DATAN2	LA_DATAN2	TXLOUT2-
10	LB_CLK	LB_CLK	TXUCLKOUT+
10	LB_CLK#	LB_CLK#	TXUCLKOUT-
10	LB_DATAP0	LB_DATAP0	TXUOUT0+
10	LB_DATAN0	LB_DATAN0	TXUOUT0-
10	LB_DATAP1	LB_DATAP1	TXUOUT1+
10	LB_DATAN1	LB_DATAN1	TXUOUT1-
10	LB_DATAP2	LB_DATAP2	TXUOUT2+
10	LB_DATAN2	LB_DATAN2	TXUOUT2-



SI stage add 0.1u for EMI solution

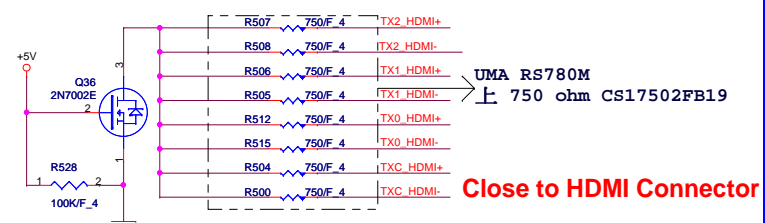


SI stage change to +3V



From RS780M

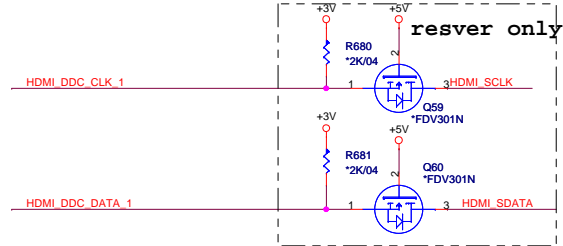
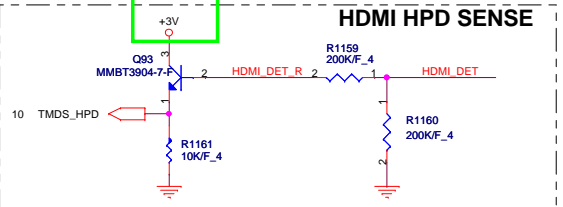
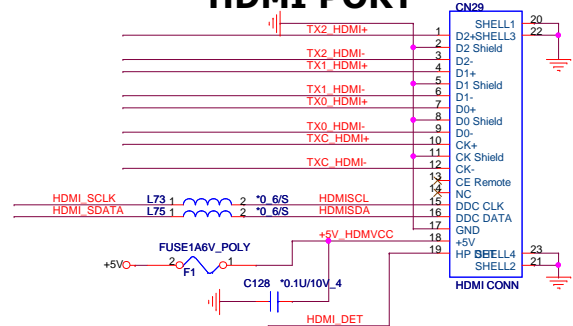
9	C_PEG_TX#15	C_PEG_TX#15	C386	0.1U/10V_4	TX2_HDMI-L	TX2_HDMI-
9	C_PEG_TX15	C_PEG_TX15	C387	0.1U/10V_4	TX2_HDMI+L	TX2_HDMI+
9	C_PEG_TX#14	C_PEG_TX#14	C388	0.1U/10V_4	TX1_HDMI-L	TX1_HDMI-
9	C_PEG_TX14	C_PEG_TX14	C389	0.1U/10V_4	TX1_HDMI+L	TX1_HDMI+
9	C_PEG_TX#13	C_PEG_TX#13	C355	0.1U/10V_4	TX0_HDMI-L	TX0_HDMI-
9	C_PEG_TX13	C_PEG_TX13	C344	0.1U/10V_4	TX0_HDMI+L	TX0_HDMI+
9	C_PEG_TX#12	C_PEG_TX#12	C827	0.1U/10V_4	TXC_HDMI-L	TXC_HDMI-
9	C_PEG_TX12	C_PEG_TX12	C828	0.1U/10V_4	TXC_HDMI+L	TXC_HDMI+

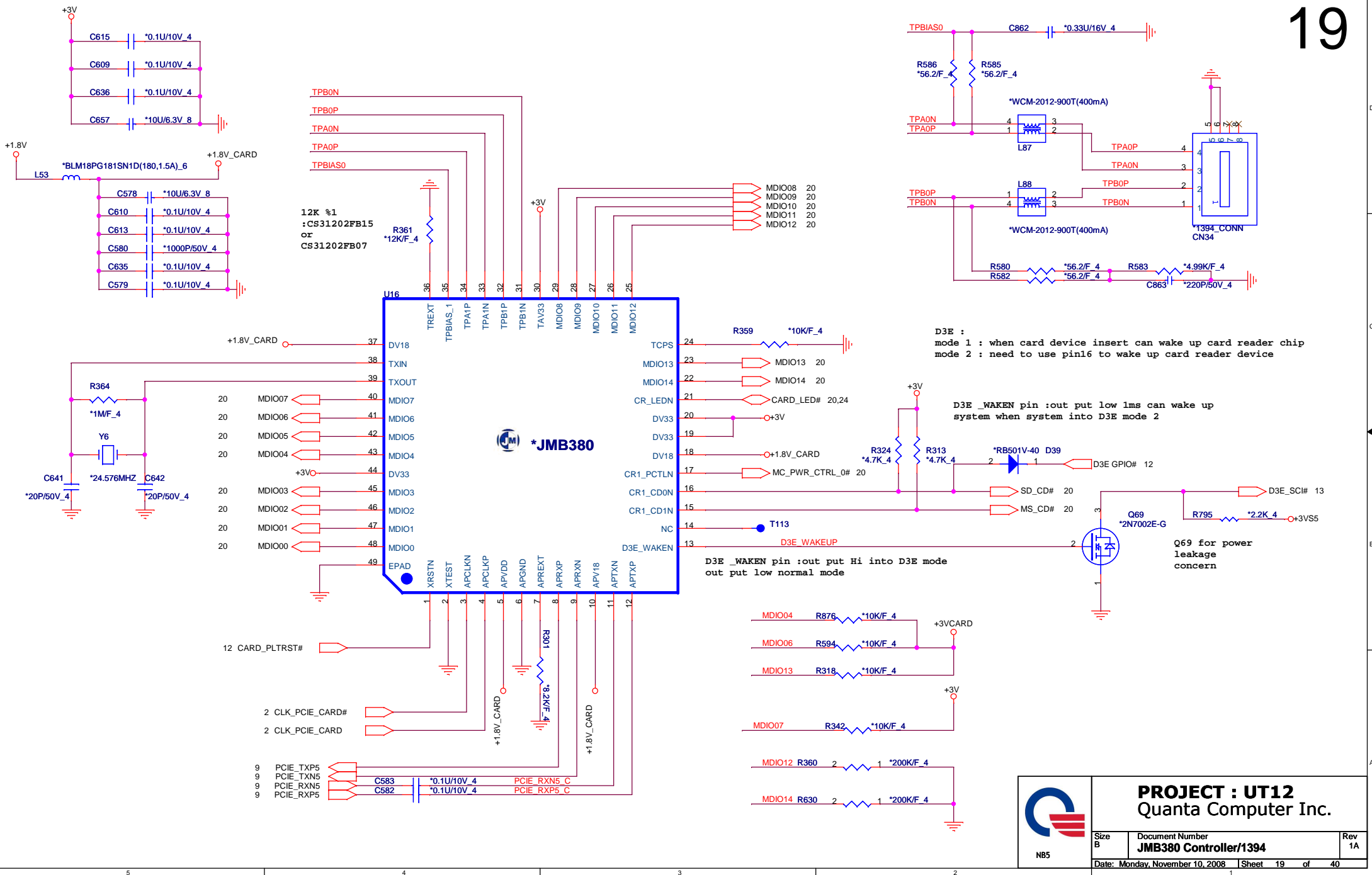


UMA RS780M
750 ohm CS17502FB19

Close to HDMI Connector

HDMI PORT






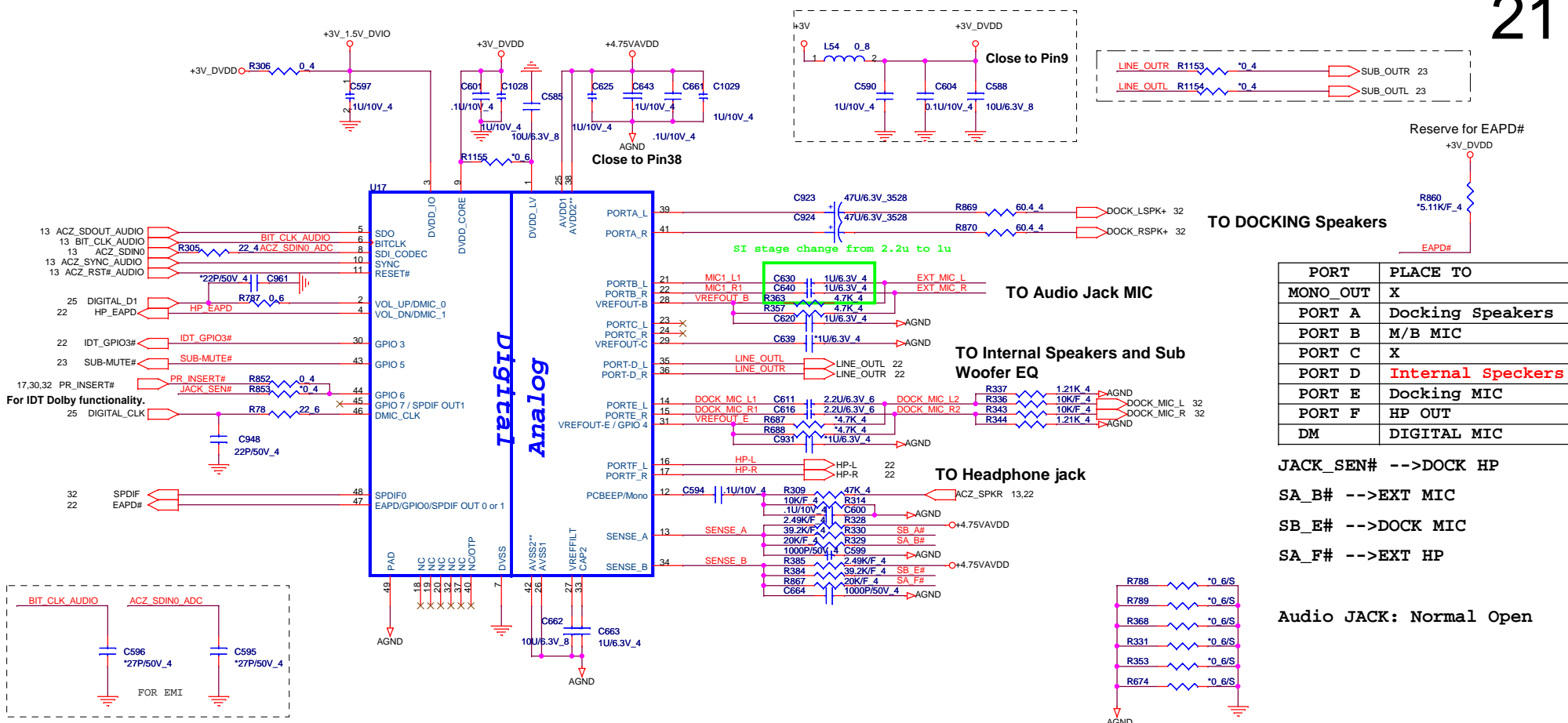
D3E :
 mode 1 : when card device insert can wake up card reader chip
 mode 2 : need to use pin16 to wake up card reader device

D3E_WAKEN pin : out put low lms can wake up system when system into D3E mode 2

D3E_WAKEN pin : out put Hi into D3E mode
 out put low normal mode

Q69 for power leakage concern

		PROJECT : UT12	
		Quanta Computer Inc.	
Size B	Document Number	Rev 1A	
JMB380 Controller/1394			
Date: Monday, November 10, 2008	Sheet 19	of 40	

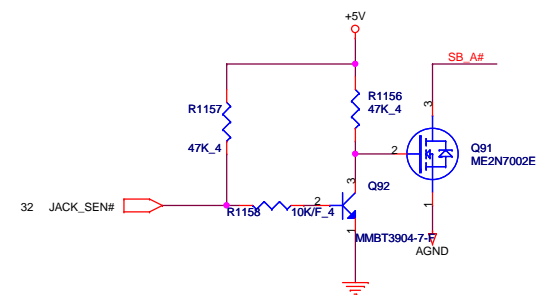
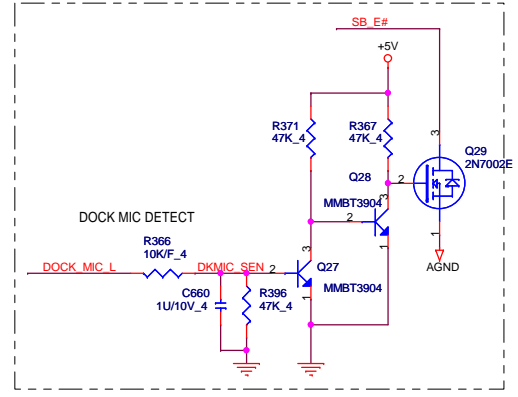
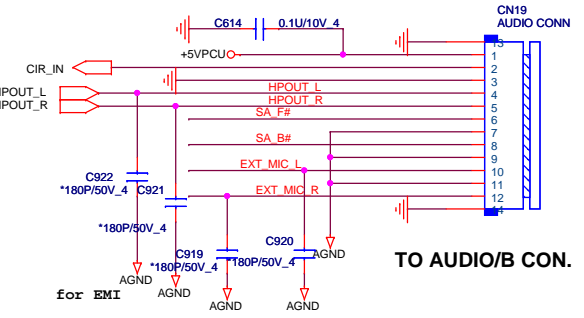
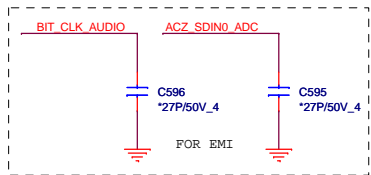


TO DOCKING Speakers

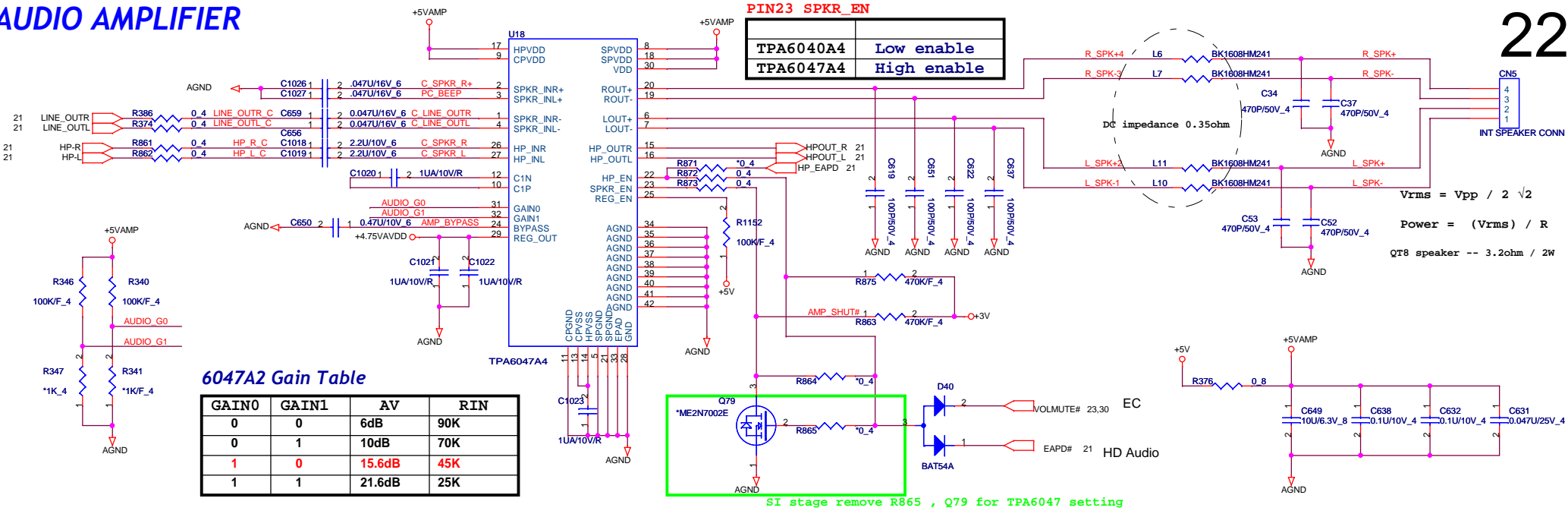
PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC

JACK_SEN# -->DOCK HP
 SA_B# -->EXT MIC
 SB_E# -->DOCK MIC
 SA_F# -->EXT HP

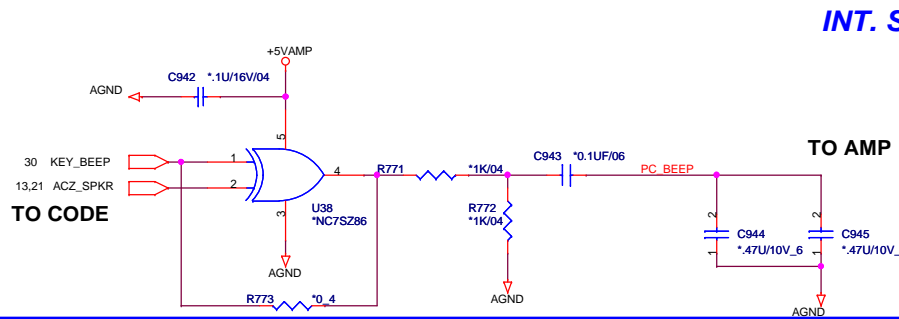
Audio JACK: Normal Open



AUDIO AMPLIFIER



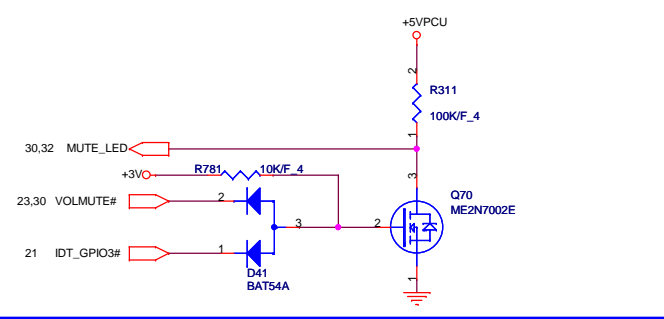
PC-BEEP



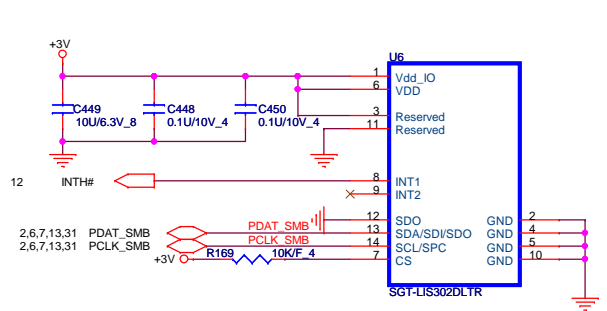
INT. SPEAKER

MUTE_LED

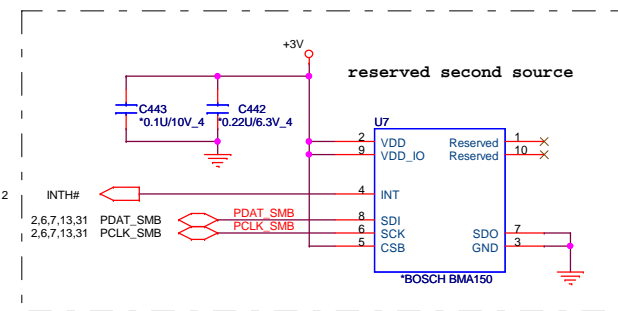
Low --> un-MUTE
High --> Mute



Acceleration sensor



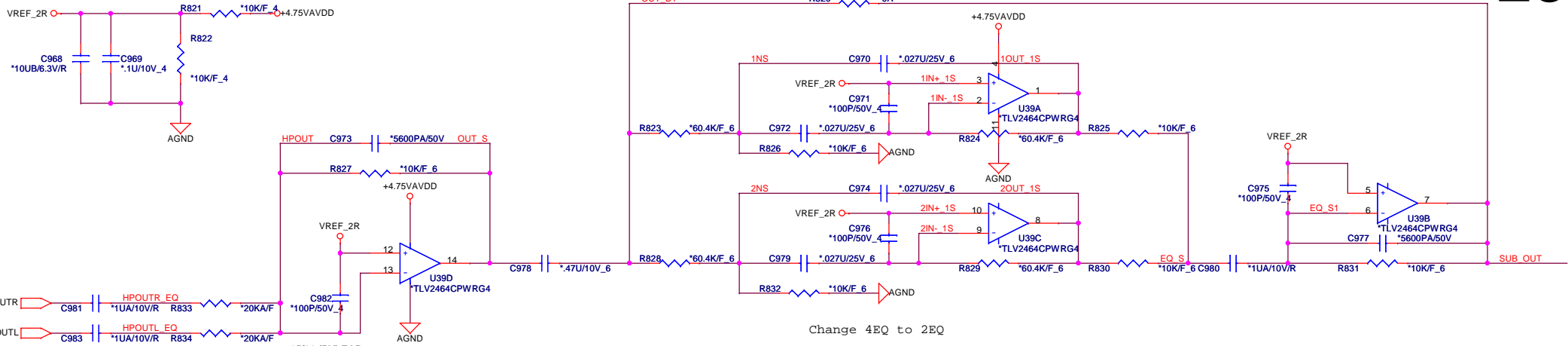
SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



PROJECT : UT12
Quanta Computer Inc.

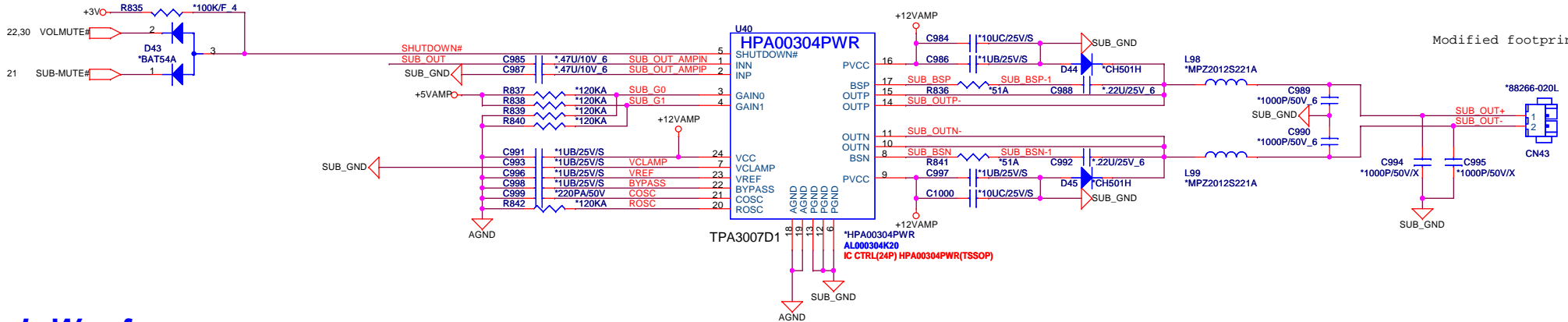
Size Custom	Document Number AMP_TPA6017/INT SPK	Rev 1A
Date: Monday, November 10, 2008	Sheet 22	of 40

EQ FOR SUBWOOFER

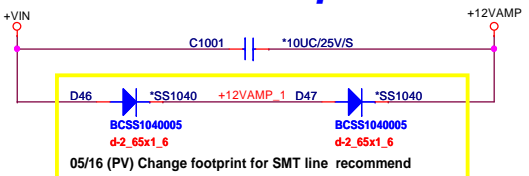


MODEL	UT1	UT2
R823	60.4K/F_6	40.2K/F_6
R824	60.4K/F_6	40.2K/F_6
R828	60.4K/F_6	80.6K/F_6
R829	60.4K/F_6	80.6K/F_6
C970	0.027U/25V_6	0.022U/50V_6
C972	0.027U/25V_6	0.022U/50V_6
C974	0.027U/25V_6	0.039U/16V_6
C976	0.027U/25V_6	0.039U/16V_6

05/26 (PV) FOR BOM update.



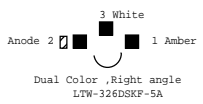
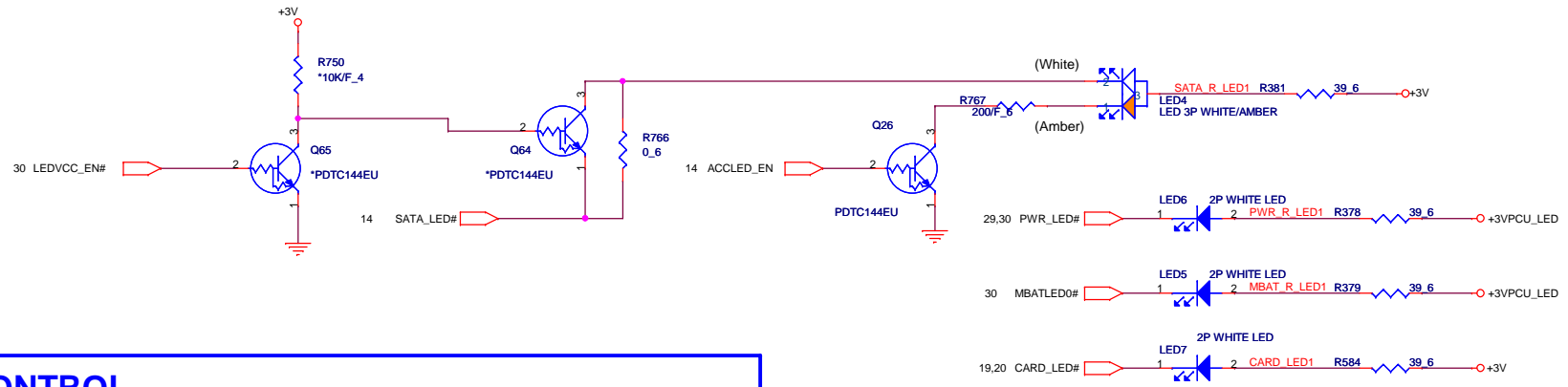
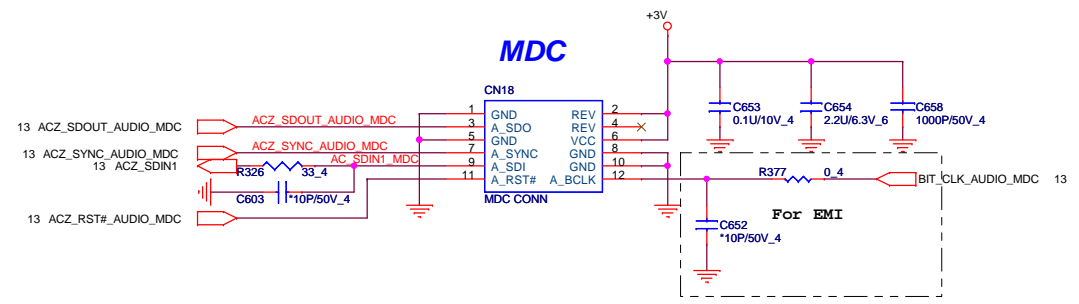
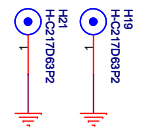
Sub-Woofler power



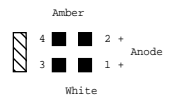
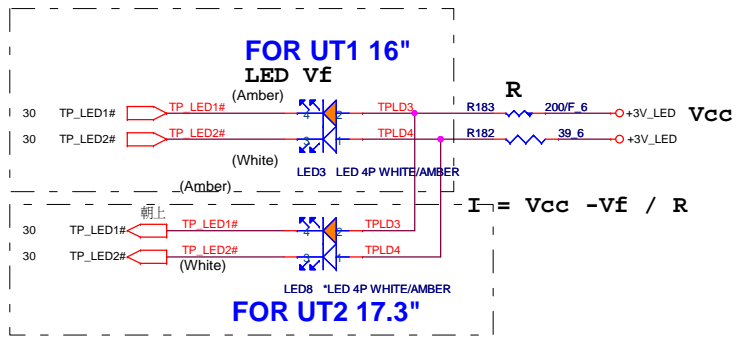
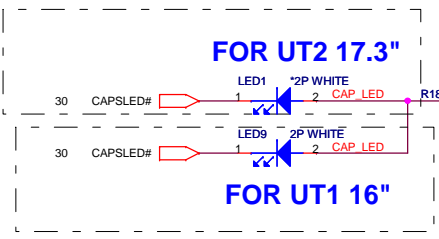
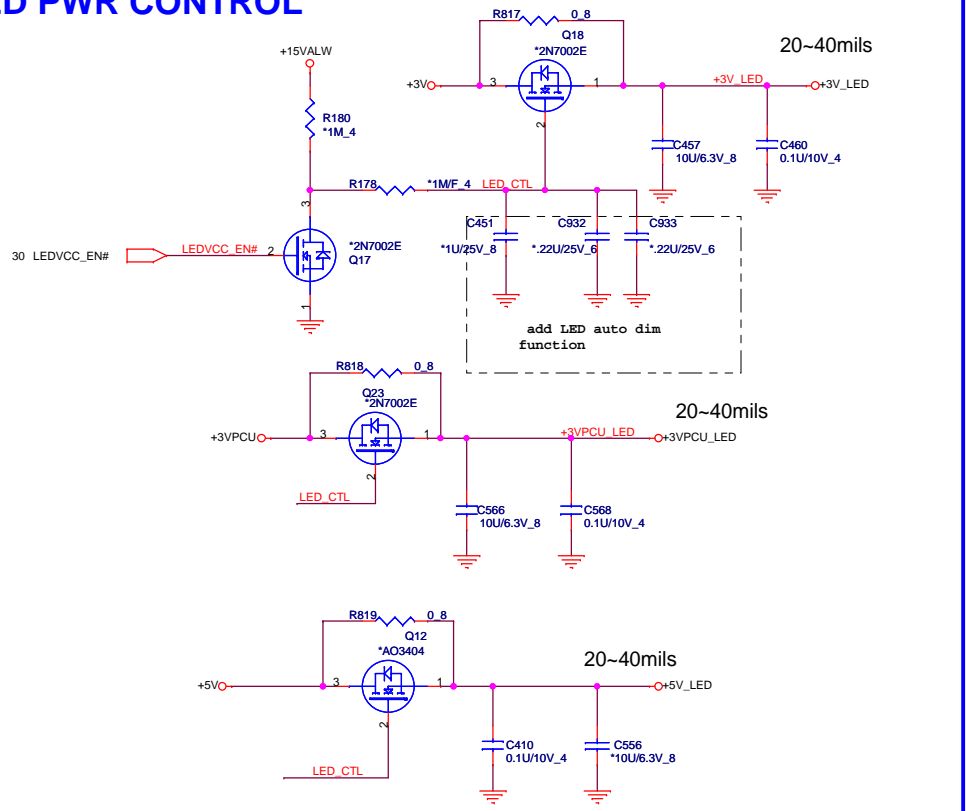
PROJECT : UT12
Quanta Computer Inc.

Size Custom	Document Number SUBWOOFER(EQ & AMP.)	Rev 1A
Date: Monday, November 10, 2008 Sheet 23 of 40		

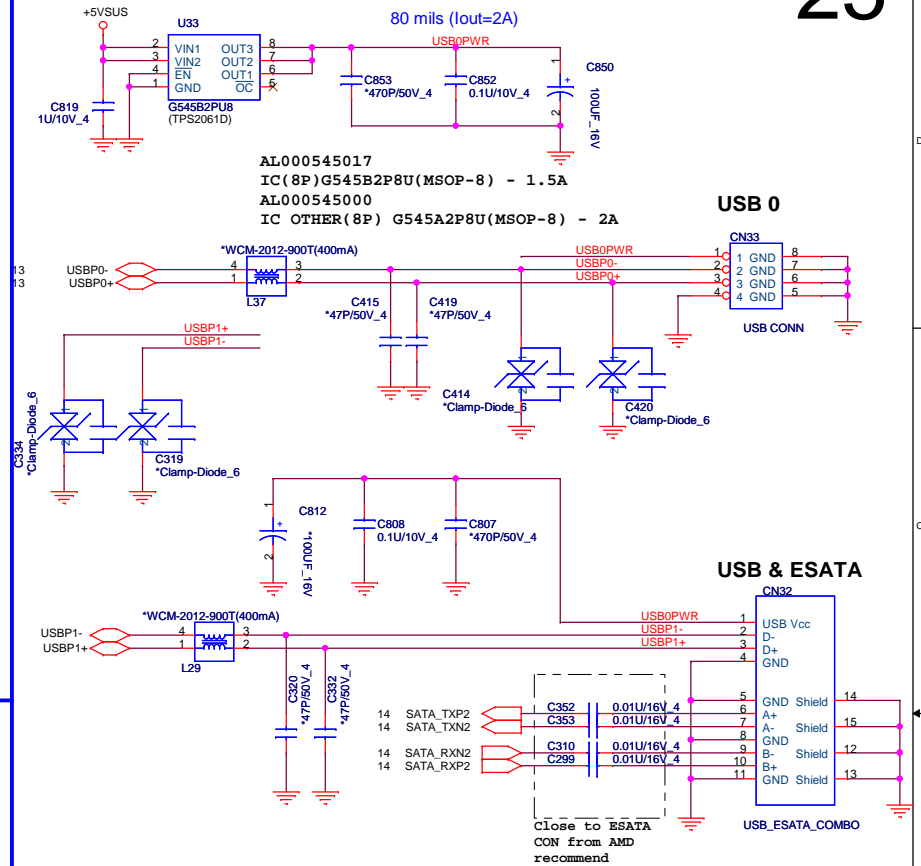
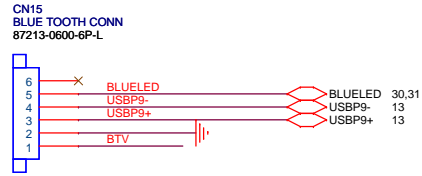
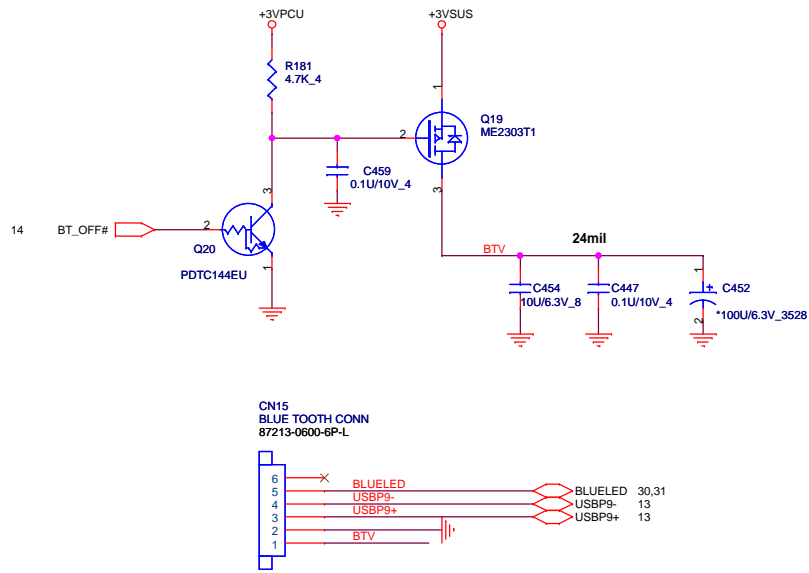
Modem CONN



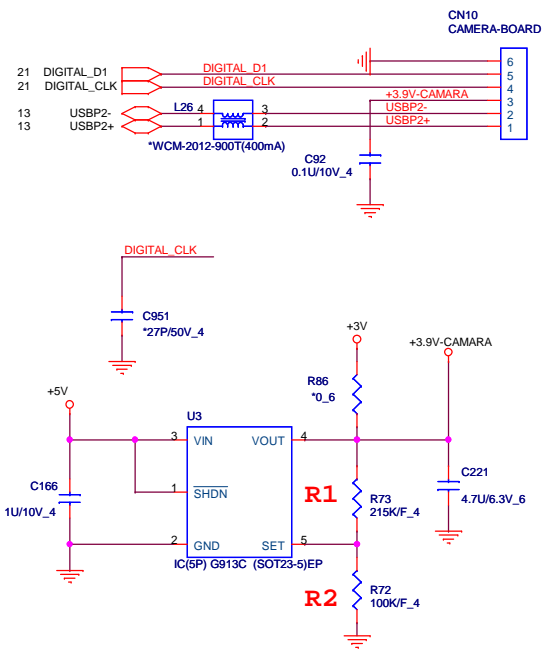
LED PWR CONTROL



	PROJECT : UT12		
	Quanta Computer Inc.		
	Size Custom	Document Number MDC1.5 Con Accelerometer/LED	Rev 1A
Date: Monday, November 10, 2008			Sheet 24 of 40



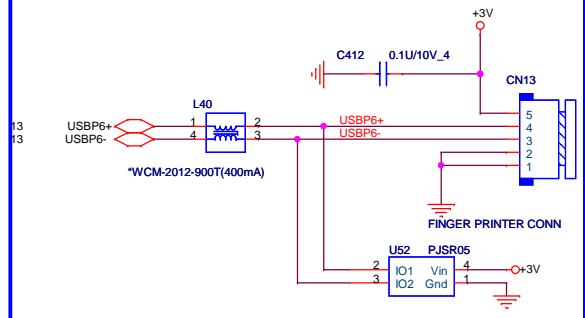
USB CAMERA CONNECT



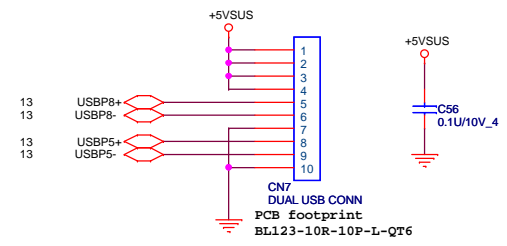
$V_{out} = 1.25(1 + R1/R2)$

USB Fingerprint CON

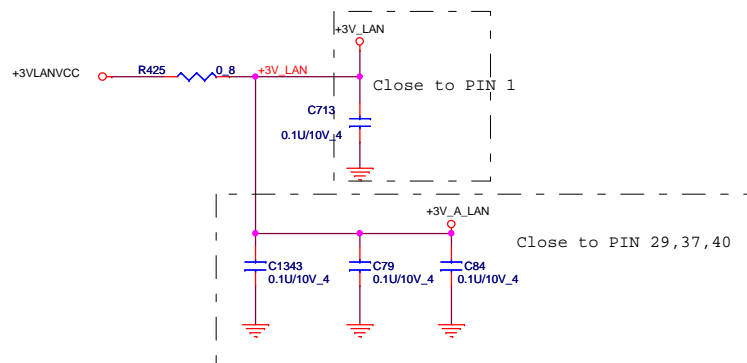
1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)



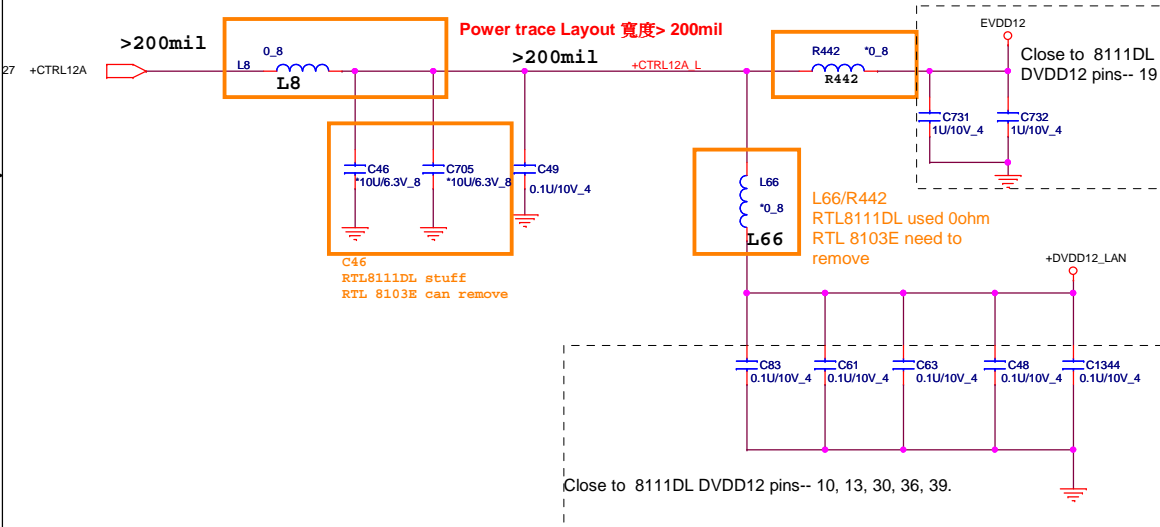
RIGHT SIDE USBX2



	<p>PROJECT : UT12 Quanta Computer Inc.</p>	
	<p>Size Custom</p>	<p>Document Number BT/WEBCAM/FT/USBX4/ESATA</p>
<p>Date: Monday, November 10, 2008</p>	<p>Sheet 25 of 40</p>	<p>Rev 1A</p>

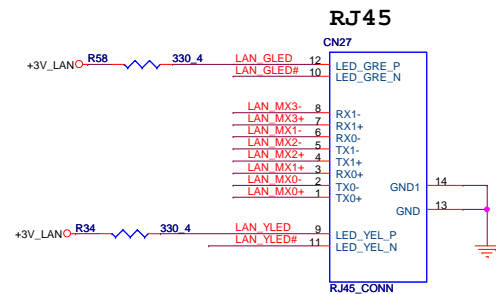
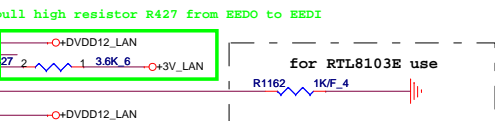
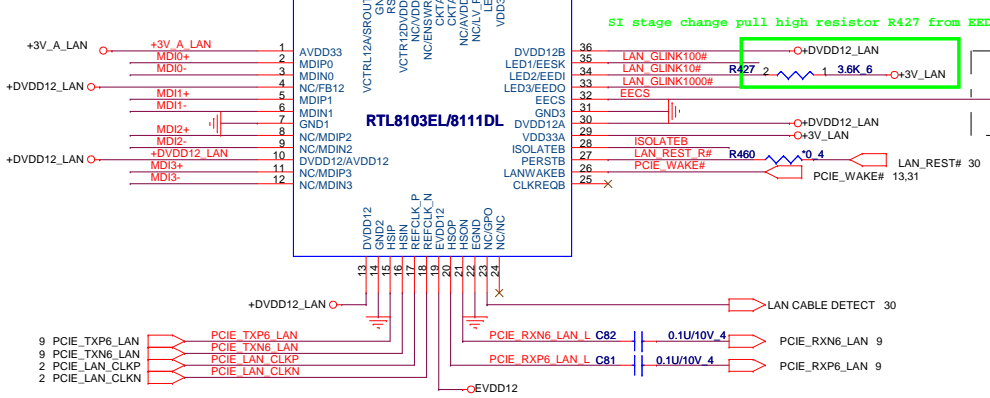
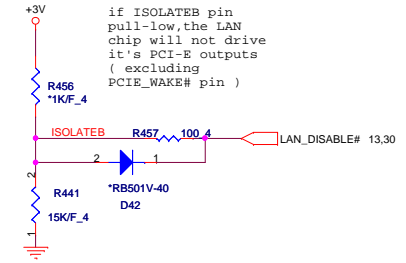
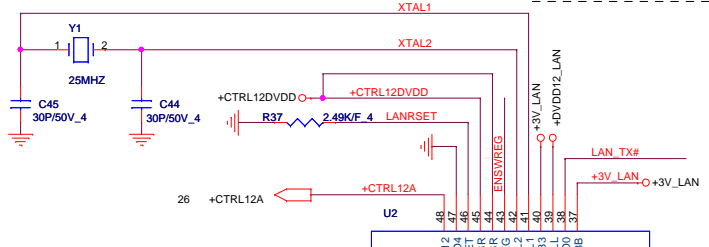
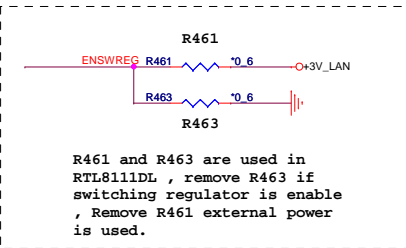
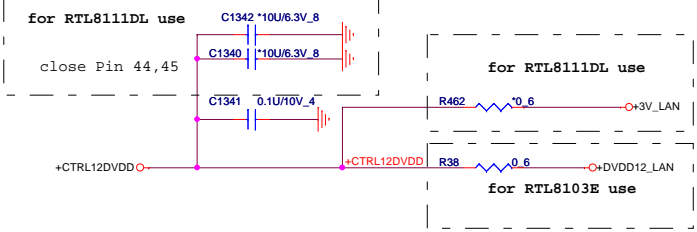


L8
RTL8111DL (Gaga lan) use 4.7uH
power choke A>600mA tolerance
±15%
RTL8103E stuff 0ohm



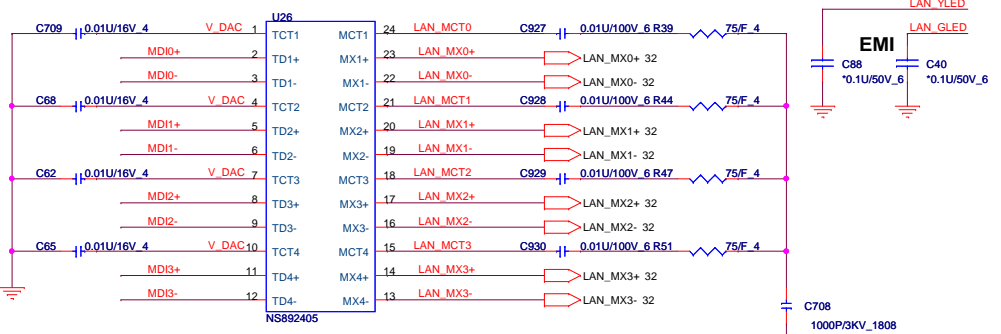
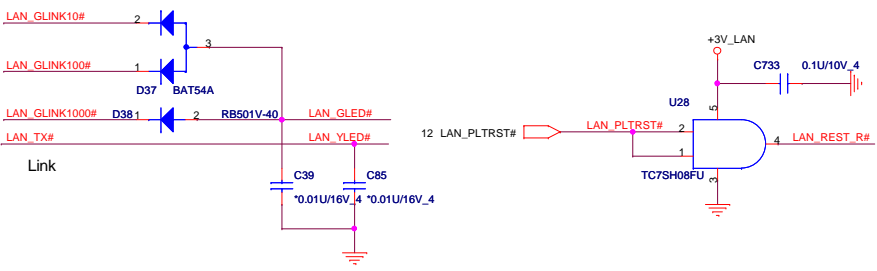
C46
RTL8111DL stuff
RTL 8103E can remove

L66/R442
RTL8111DL used 0ohm
RTL 8103E need to
remove



AL08111DB00 RTL8111DL-GR

AL08103EB00 RTL8103EL-GR

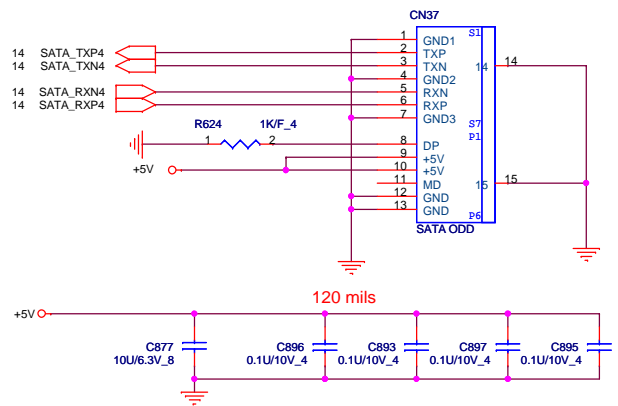


NS892402:GIGABIT DB0AT9LAN05

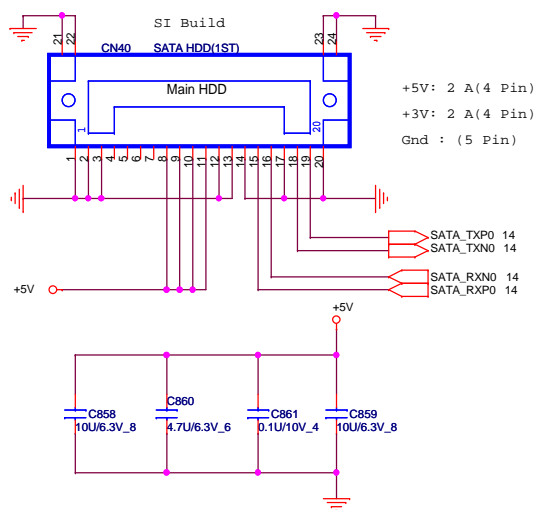
NS892405:10/100 DB0ZB1LAN04

SATA CD-ROM

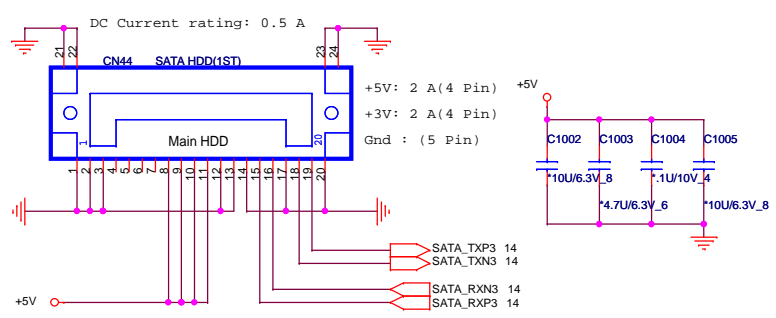
17.3 ODD P/N : DFHS13FR030 or DFHS13FR040
 16.3 ODD P/N : DFHD13MR006 , DFHD13MR009 , DFHD13MR008



SATA_1 HDD CONNECTOR

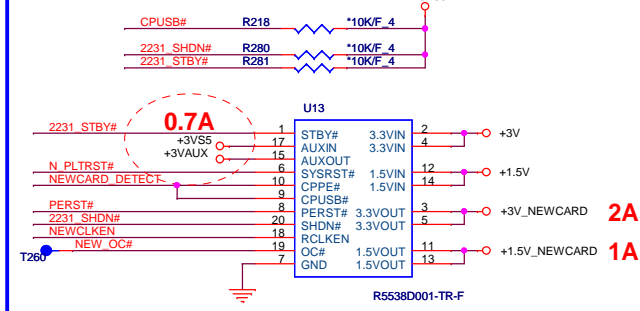
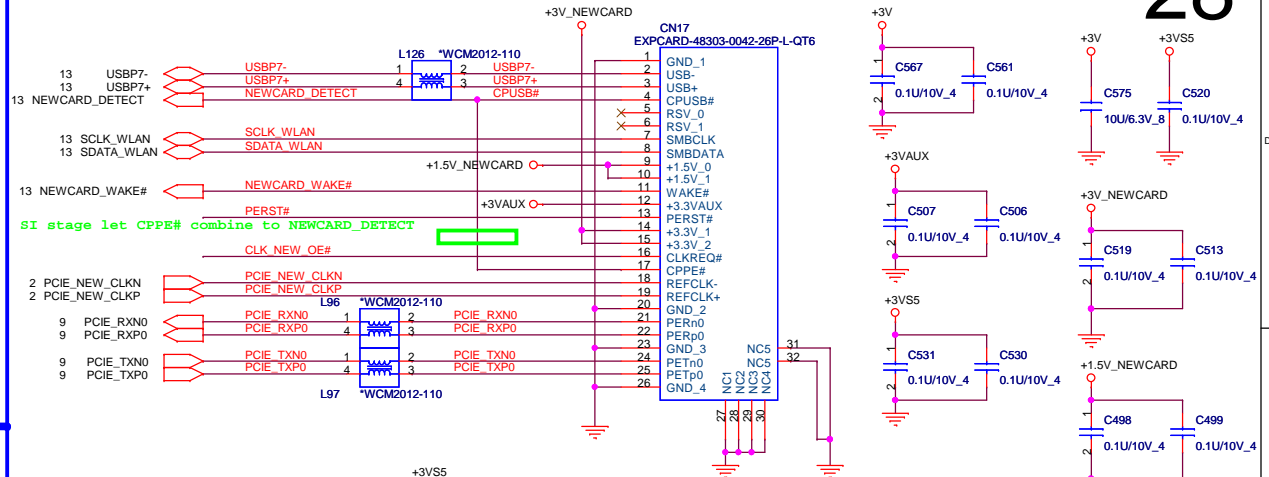


SATA_2 CONNECTOR

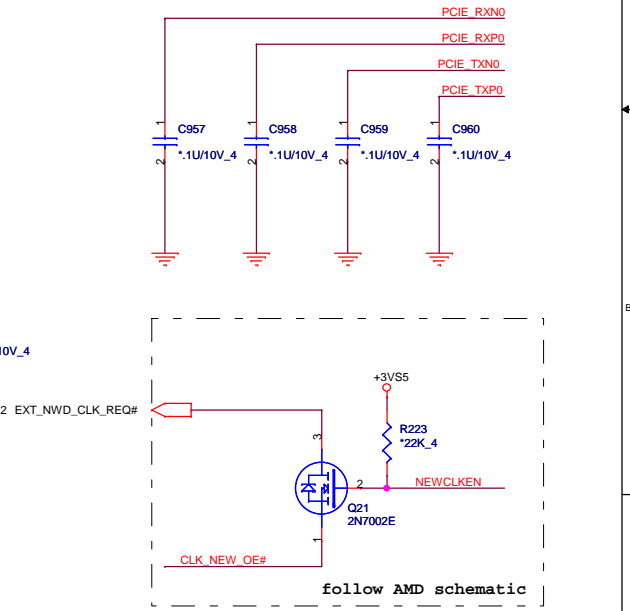
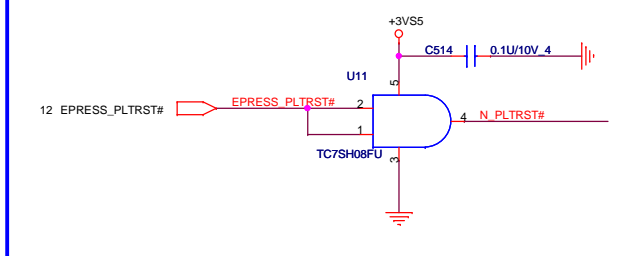


NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)



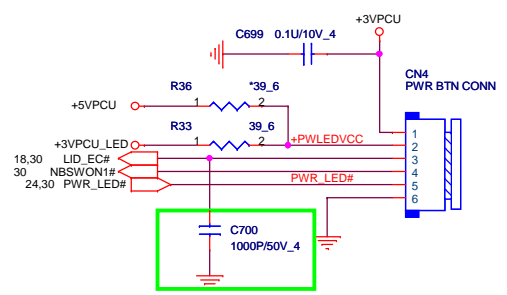
R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYRSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN



PROJECT : UT12
Quanta Computer Inc.

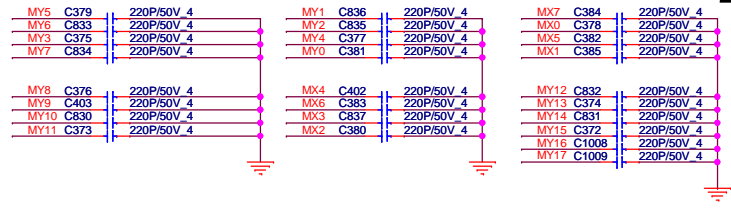
Size Custom	Document Number NEW CARD/SATA ODD/SATA HDD	Rev 1A
Date: Monday, November 10, 2008	Sheet 28 of 40	

POWER BUTTON CONNECT

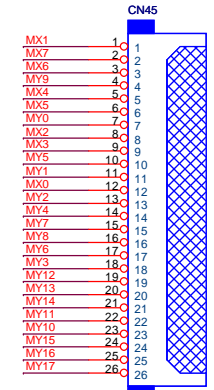
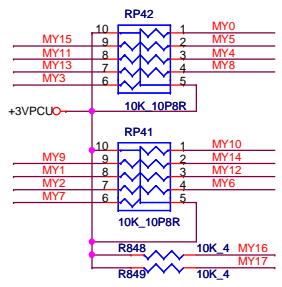


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

SI stage add 1000P for EMI solution



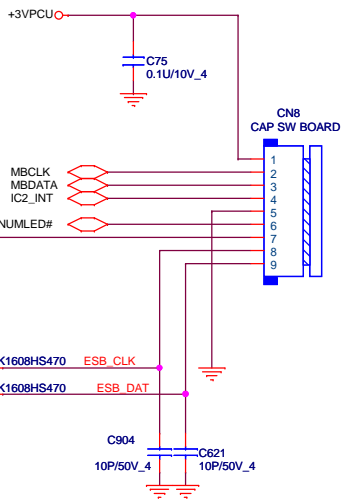
KEYBOARD PULL-UP



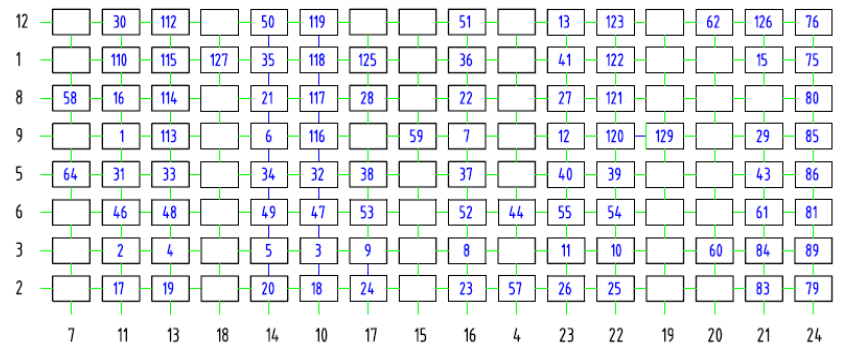
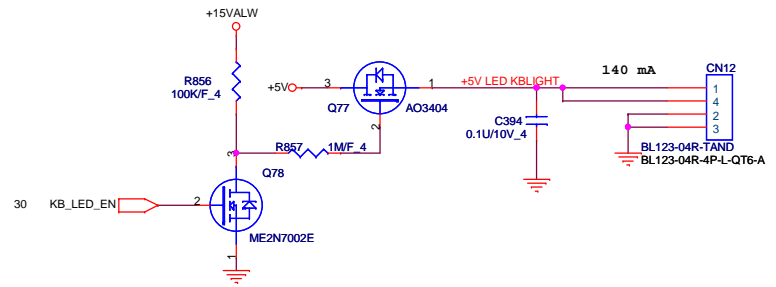
GB1RF260-1253-8F

Footprint: "gb1rf260-1253-7f-26p-1"

CAP SW CONNECT

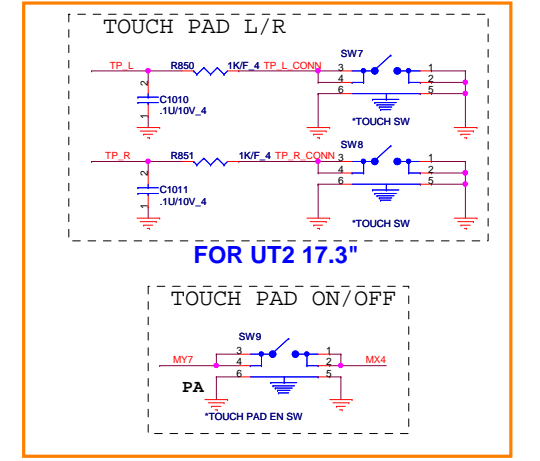
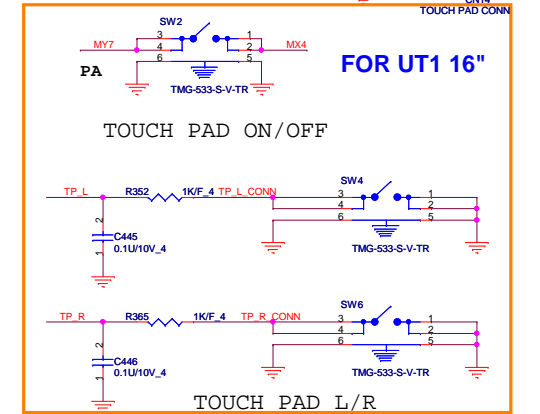
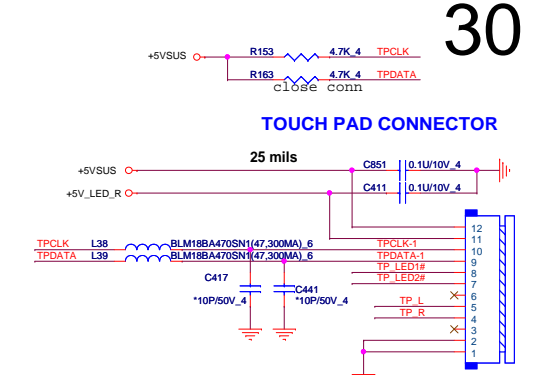
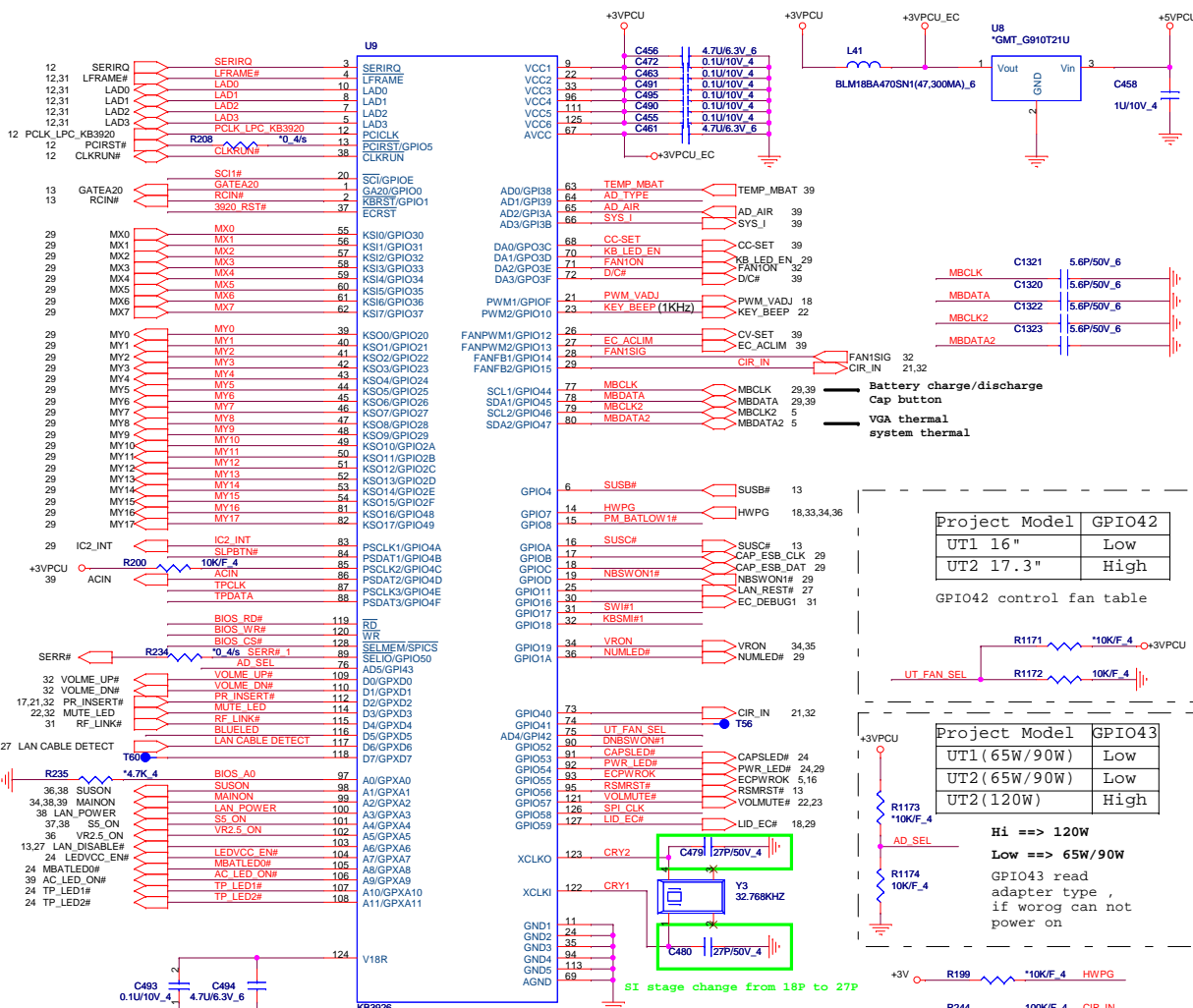


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT



PROJECT : UT12
Quanta Computer Inc.

Size Custom	Document Number LED/KEYBOARD/SW	Rev 1A
Date: Monday, November 10, 2008	Sheet 29	of 40



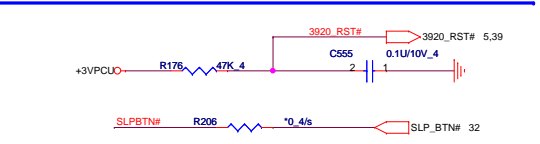
GPIO42 control fan table

Project Model	GPIO42
UT1 16"	Low
UT2 17.3"	High

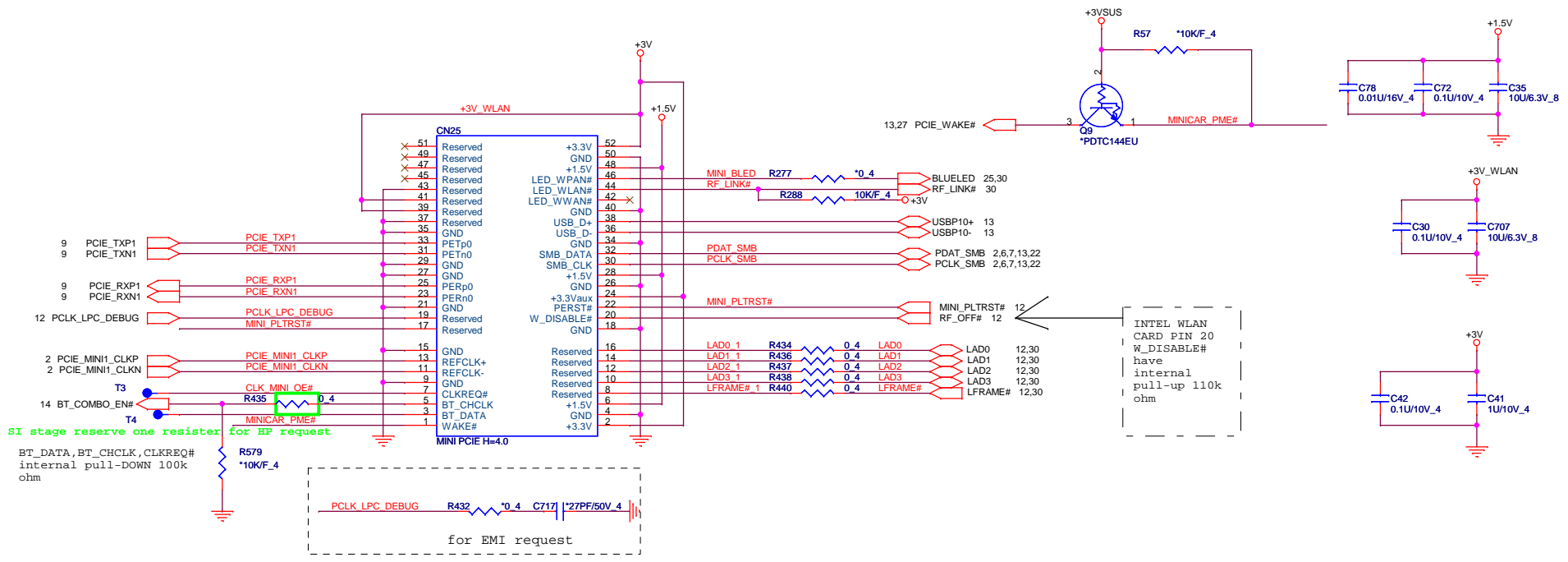
GPIO43 control fan table

Project Model	GPIO43
UT1 (65W/90W)	Low
UT2 (65W/90W)	Low
UT2 (120W)	High

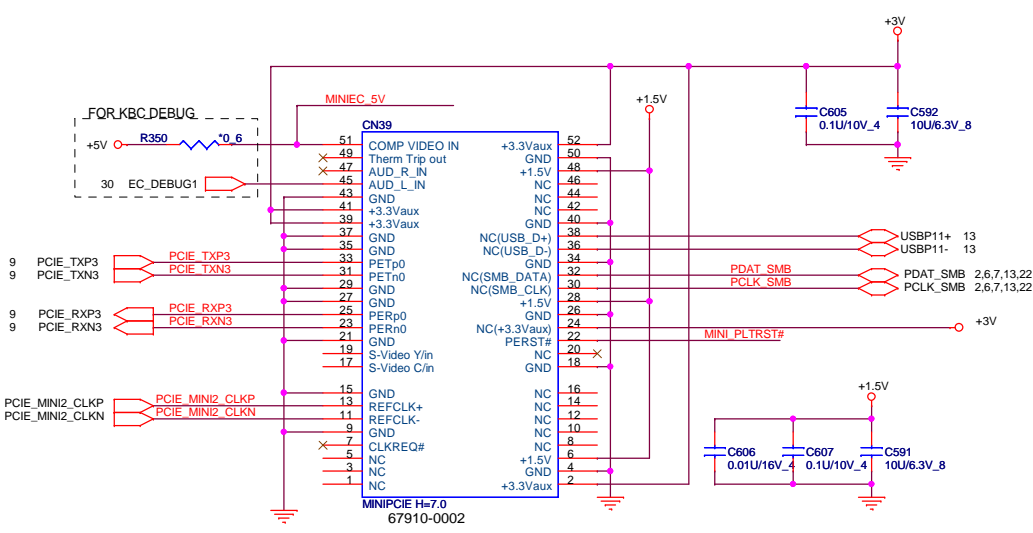
Hi ==> 120W
 Low ==> 65W/90W
 GPIO43 read adapter type, if wrong can not power on




Mini PCI-E Card 1 WLAN



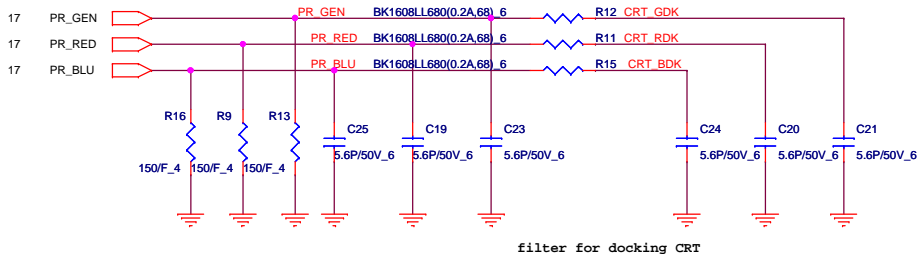
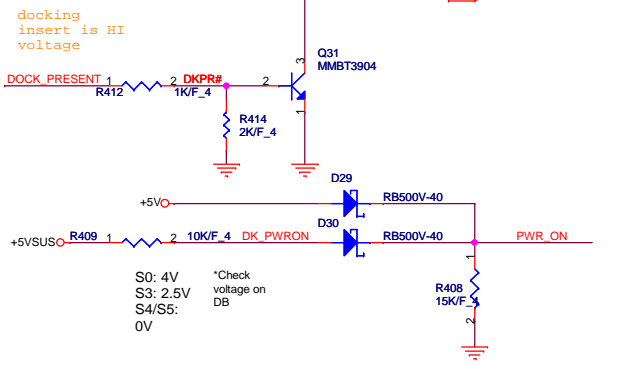
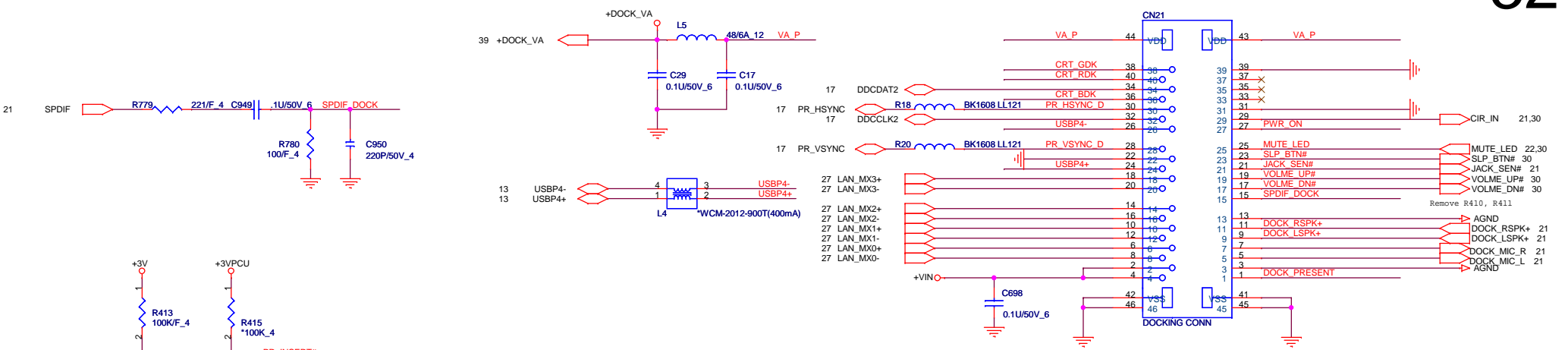
Mini PCI-E Card 2 TV tuner card



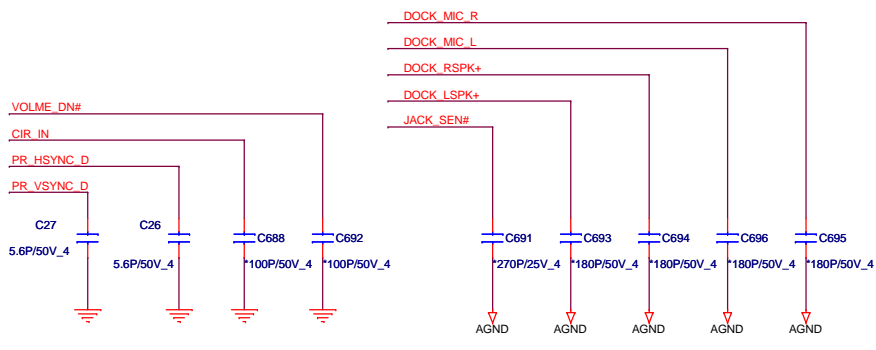
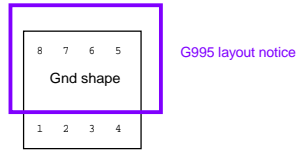
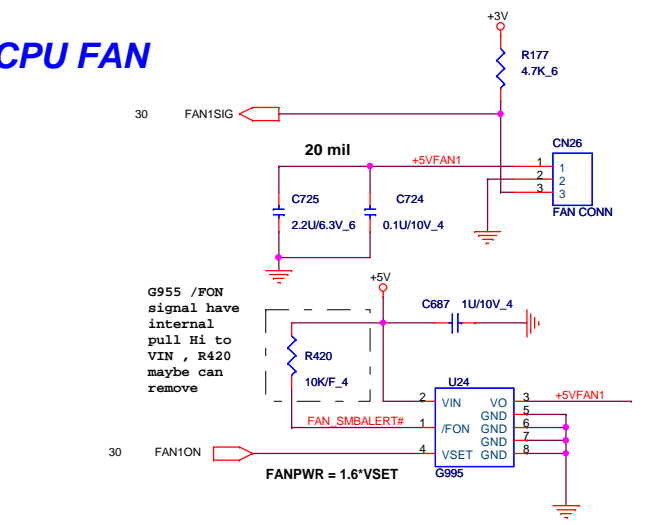
 NBS	PROJECT : UT12 Quanta Computer Inc.	
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support 6A 200mils
CX000480005

CABLE DOCK



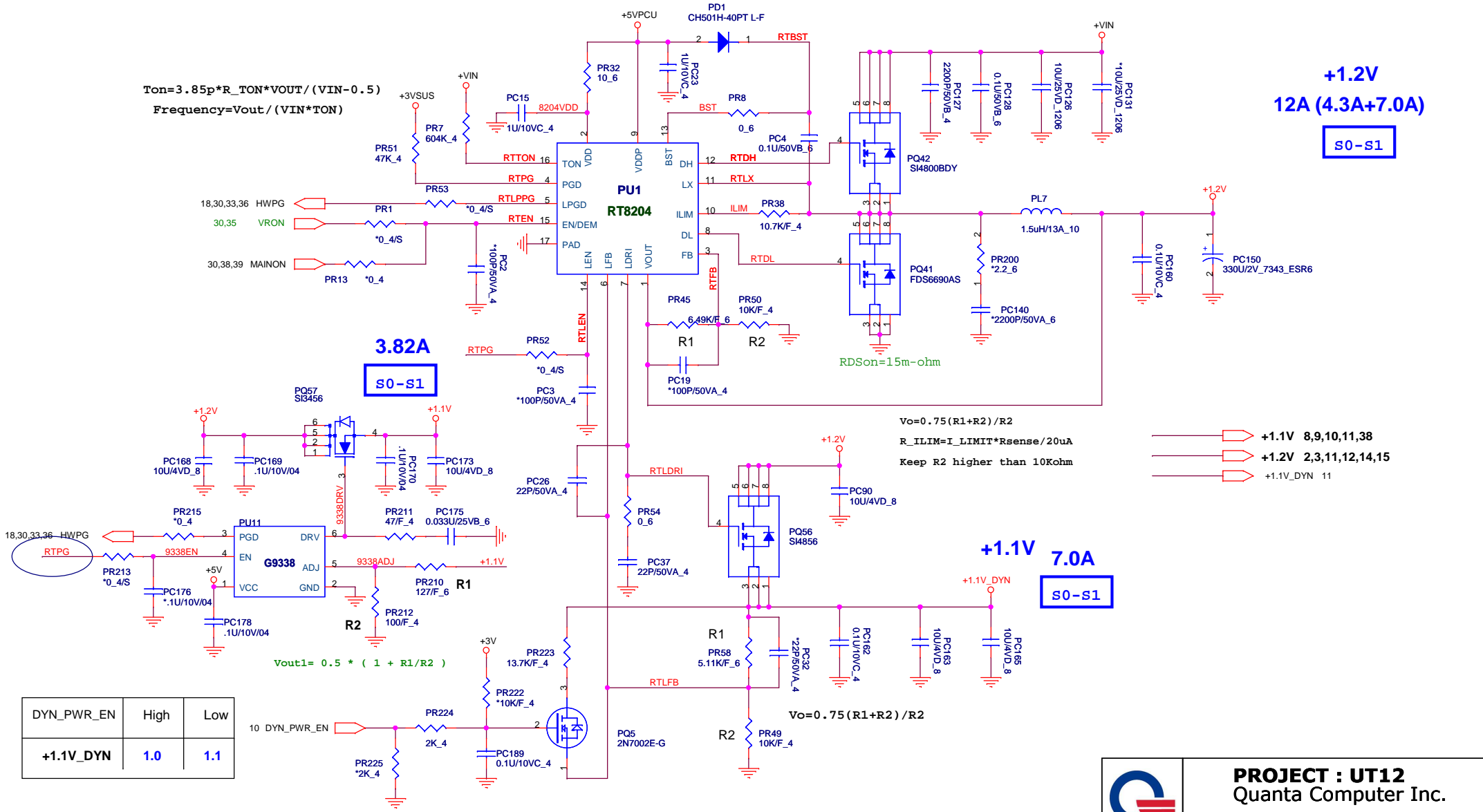
CPU FAN



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$$T_{on} = 3.85p * R_{TON} * V_{OUT} / (V_{IN} - 0.5)$$

$$Frequency = V_{out} / (V_{IN} * T_{ON})$$



- +1.1V 8,9,10,11,38
- +1.2V 2,3,11,12,14,15
- +1.1V_DYN 11

DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1



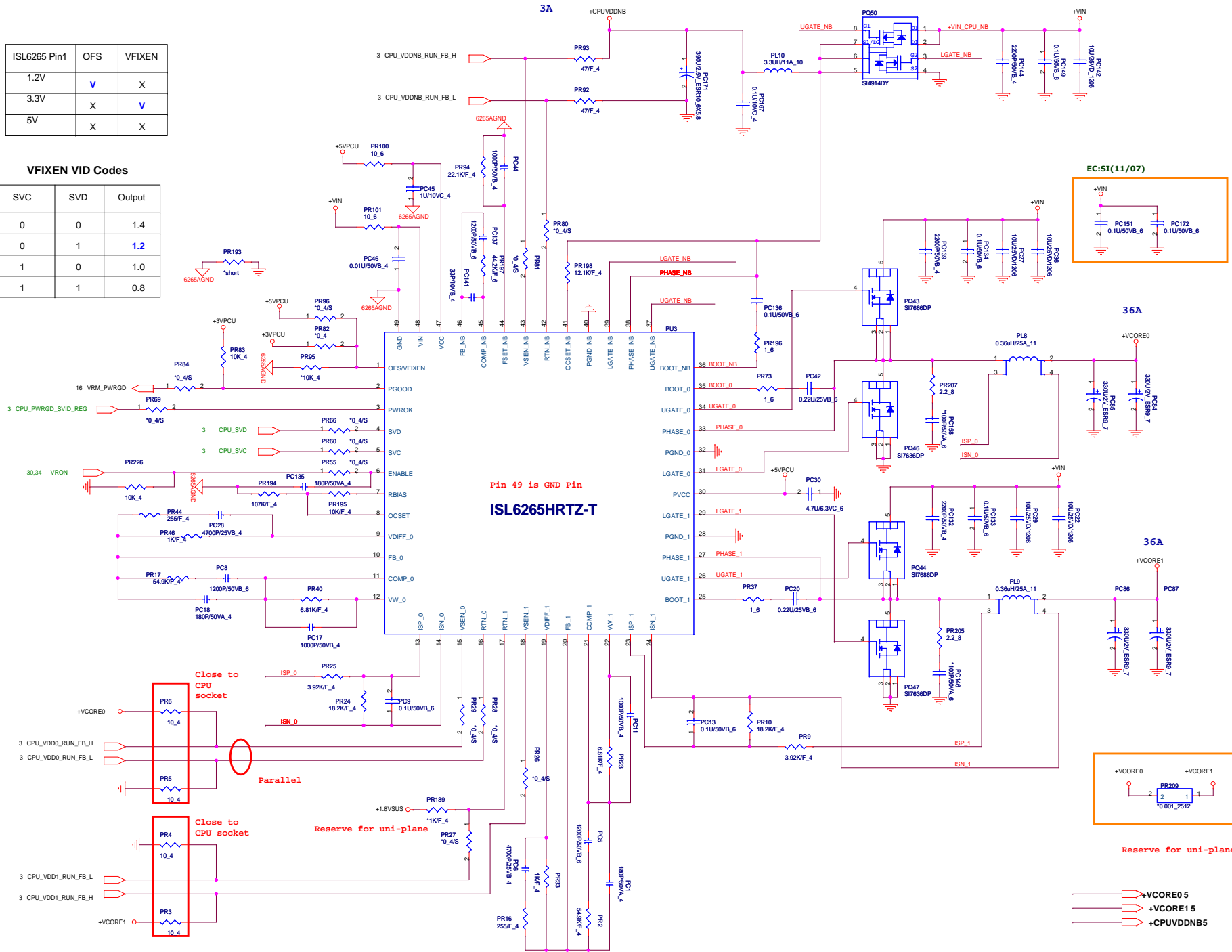
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Quanta Computer Inc.

Size B	Document Number +1.2V & +1.1V(RT8204)	Rev 1A
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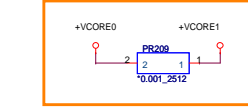
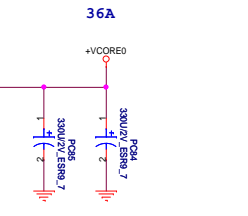
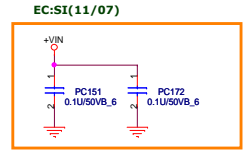
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

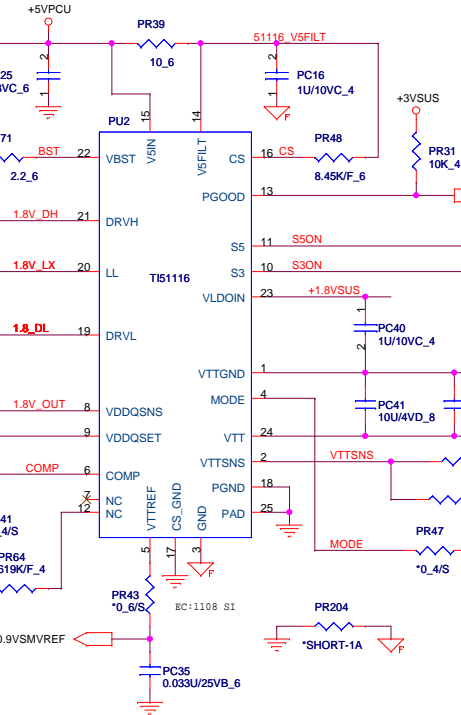
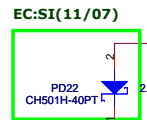
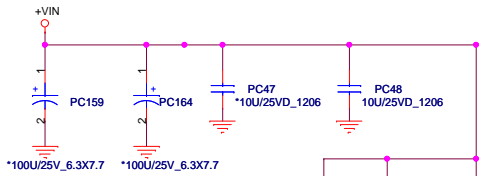
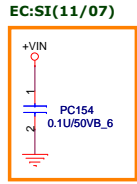


Pin 49 is GND Pin
ISL6265HRTZ-T



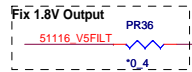
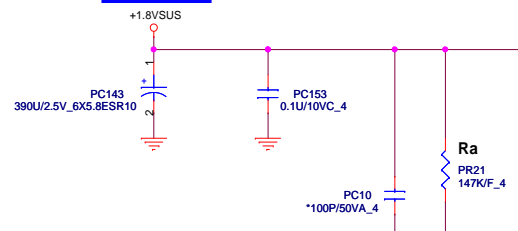
- +VREG0 5
- +VREG1 5
- +CPUVDDNB 5

→ +2.5V 3
→ +1.8VSUS 3,4,5,6,7,35,37

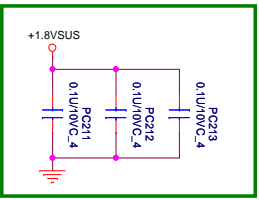


$I_{lim(Valley)} = 10\mu A * R_{ILIM} / R_{DS_ON}$
For OCP set.

23.65A
S0-S3



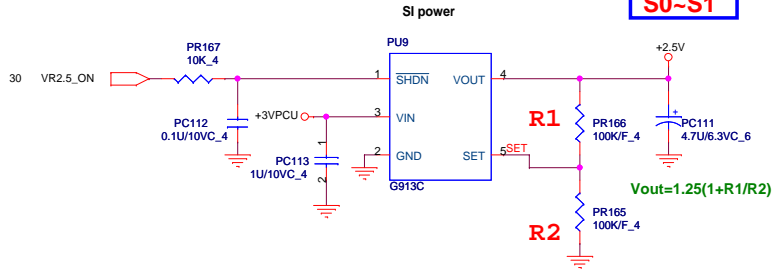
Add 0.1u CAP PC211, PC212, PC213 for EMI



$R_a = (V_{out} - 0.75) / 0.75 * R_b$
Rb value from 100K to 300K ohm

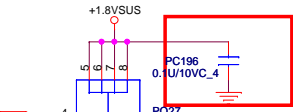
+2.5V
0.25A
S0-S1

Close to CPU



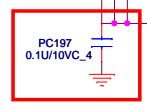
$V_{out} = 1.25 * (1 + R1/R2)$

For EMI-SI



+1.8V
10.4A
S0-S1

For EMI-SI



Discrete:SI4856
UMA:SI4800

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$V_{TRIP}(mV) = R_{TRIP}(Kohm) * 10 (uA)$

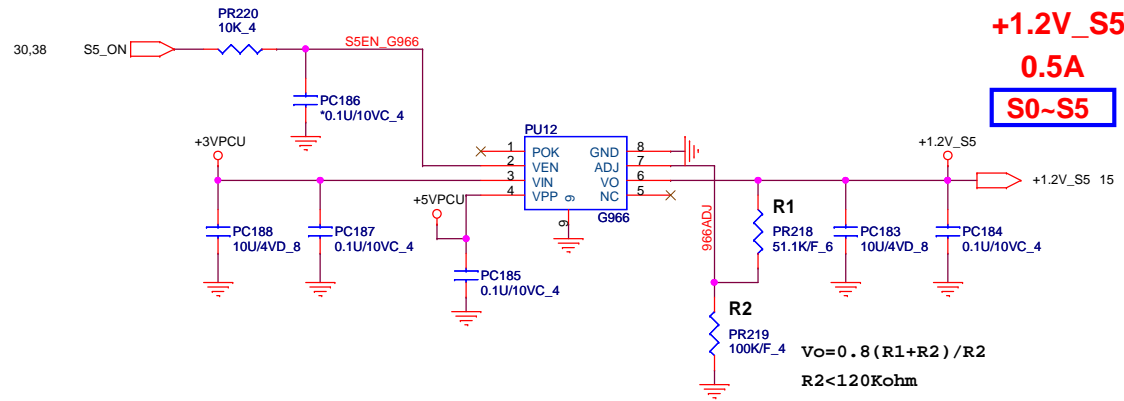
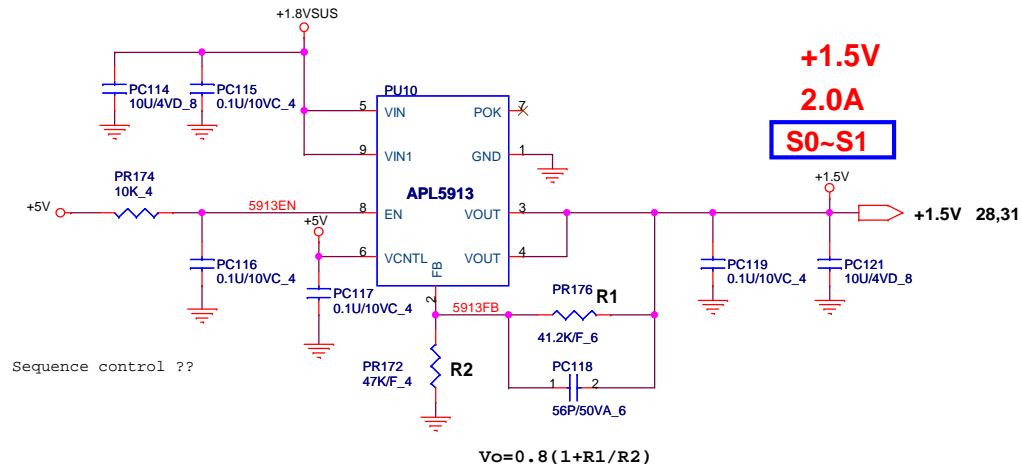
$I_{OCP} = V_{trip} / R_{ds_on} + I_{Ripple} / 2$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V_{_vddqsns} / 2$	DDR
V5IN	1.8	$V_{_vddqsns} / 2$	DDR2
FB	adjustable	$V_{_VDDQSNS} / 2$	$1.5V < VDDQ < 3V$



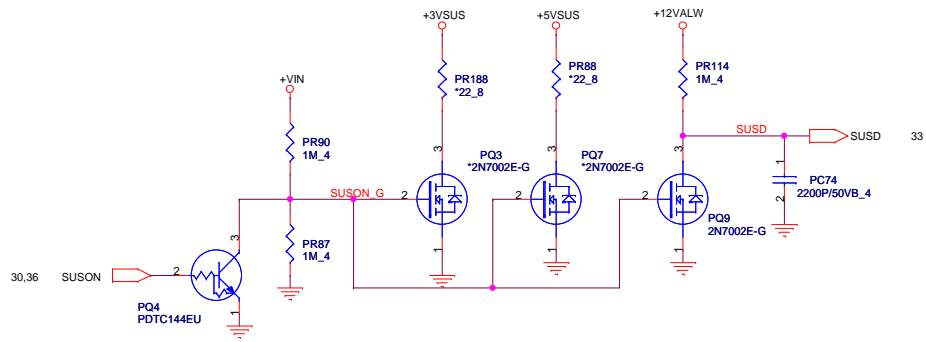
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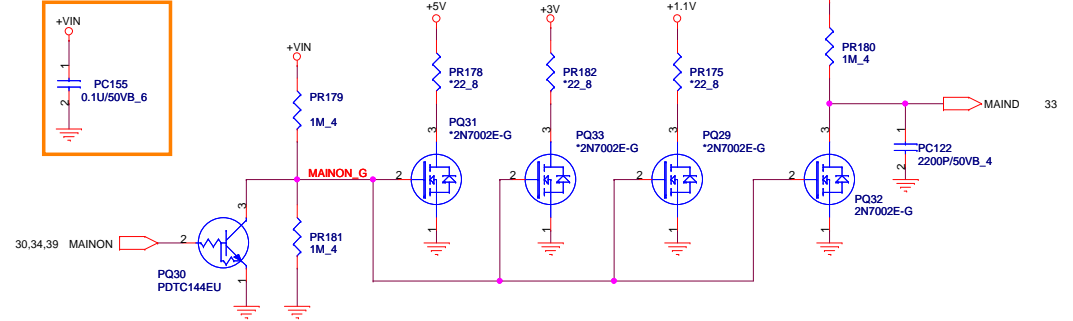


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EC:SI(11/07)



EC:SI(11/07)

