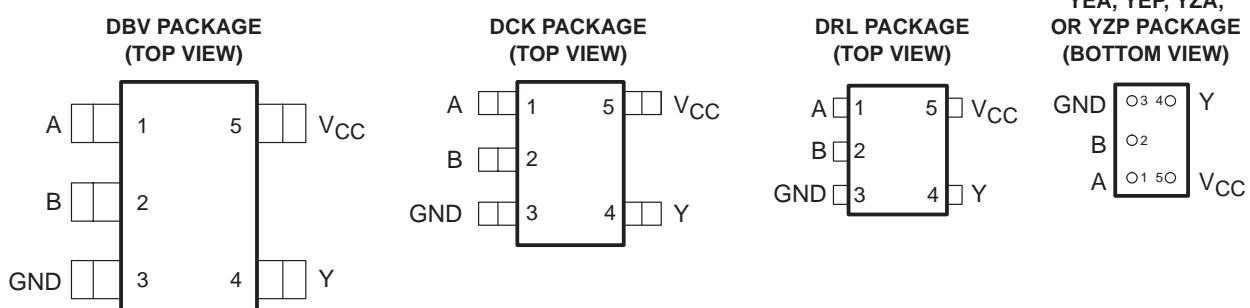


- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

description/ordering information

This single 2-input exclusive-OR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G86 performs the Boolean function Y = A ⊕ B or Y = $\overline{A}B + A\overline{B}$ in positive logic.

ORDERING INFORMATION

T _A	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA	Reel of 3000	---CH_
	NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free)		
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP		
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G86DBVR
		Reel of 250	SN74LVC1G86DBVT
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G86DCKR
		Reel of 250	SN74LVC1G86DCKT
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1G86DRLR
			CH_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site.

YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date.
Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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SN74LVC1G86

SINGLE 2-INPUT EXCLUSIVE-OR GATE

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description/ordering information (continued)

A common application is as a true/complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

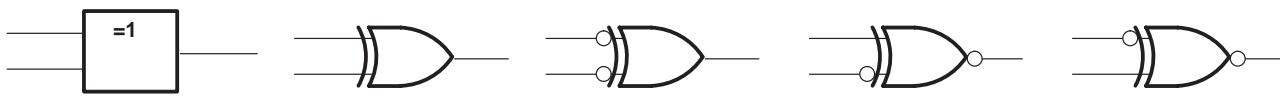
FUNCTION TABLE

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE OR



These are five equivalent exclusive-OR symbols valid for an SN74LVC1G86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



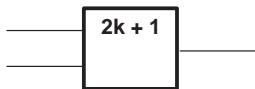
The output is active (low) if all inputs stand at the same logic level (i.e., $A = B$).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	-0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3): DBV package	206°C/W
DCK package	252°C/W
DRL package	142°C/W
YEA/YZA package	154°C/W
YEP/YZP package	132°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC1G86

SINGLE 2-INPUT EXCLUSIVE-OR GATE

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.8		
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}		
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	-4		mA
		V _{CC} = 2.3 V	-8		
		V _{CC} = 3 V	-16		
			-24		
I _{OL}	Low-level output current	V _{CC} = 4.5 V	-32		mA
		V _{CC} = 1.65 V	4		
		V _{CC} = 2.3 V	8		
		V _{CC} = 3 V	16		
			24		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 4.5 V	32		ns/V
		V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20		
		V _{CC} = 3.3 V ± 0.3 V	10		
T _A	Operating free-air temperature	V _{CC} = 5 V ± 0.5 V	5		°C
			-40	85	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	1.65 V to 5.5 V	V _{CC} -0.1			V
	I _{OH} = -4 mA	1.65 V	1.2			
	I _{OH} = -8 mA	2.3 V	1.9			
	I _{OH} = -16 mA	3 V	2.4			
	I _{OH} = -24 mA		2.3			
	I _{OH} = -32 mA	4.5 V	3.8			
V _{OL}	I _{OL} = 100 µA	1.65 V to 5.5 V		0.1		V
	I _{OL} = 4 mA	1.65 V		0.45		
	I _{OL} = 8 mA	2.3 V		0.3		
	I _{OL} = 16 mA	3 V		0.4		
	I _{OL} = 24 mA			0.55		
	I _{OL} = 32 mA	4.5 V		0.55		
I _I	A or B input	V _I = 5.5 V or GND	0 to 5.5 V		±5	µA
I _{off}		V _I or V _O = 5.5 V	0		±10	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0		1.65 V to 5.5 V		10	µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		3 V to 5.5 V		500	µA
C _i	V _I = V _{CC} or GND		3.3 V		6	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 5 V ± 0.5 V	UNIT				
			MIN	MAX	MIN	MAX					
t _{pd}	A or B	Y	2.1	9.1	1	4.5	0.6	4	0.8	3.3	ns

switching characteristics over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 5 V ± 0.5 V	UNIT				
			MIN	MAX	MIN	MAX					
t _{pd}	A or B	Y	3.5	9.9	1.8	5.5	1.3	5	1	4	ns

operating characteristics, T_A = 25°C

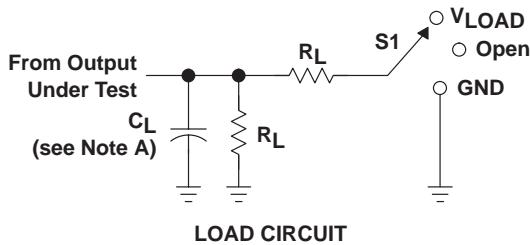
PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT	
		MIN	MAX	MIN	MAX		
C _{pd}	Power dissipation capacitance	f = 10 MHz	22	22	22	24	pF

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SINGLE 2-INPUT EXCLUSIVE-OR GATE

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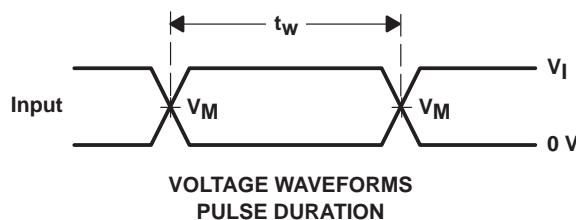
PARAMETER MEASUREMENT INFORMATION



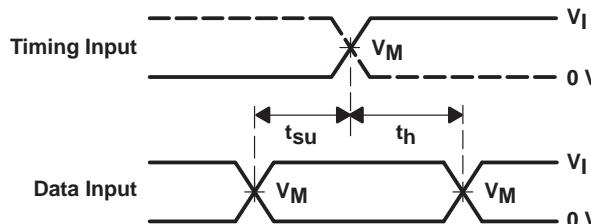
TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	V _{LOAD}
tPHZ/tPZH	GND

LOAD CIRCUIT

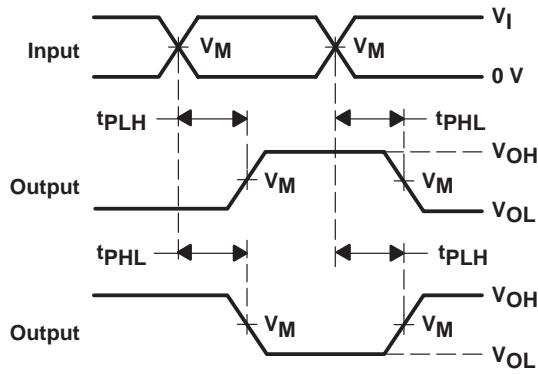
V _{CC}	INPUTS		V _M	V _{LOAD}	C _L	R _L	V _Δ
	V _I	t _r /t _f					
1.8 V ± 0.15 V	V _{CC}	≤ 2 ns	V _{CC} /2	2 × V _{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V _{CC}	≤ 2 ns	V _{CC} /2	2 × V _{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V _{CC}	≤ 2.5 ns	V _{CC} /2	2 × V _{CC}	15 pF	1 MΩ	0.3 V



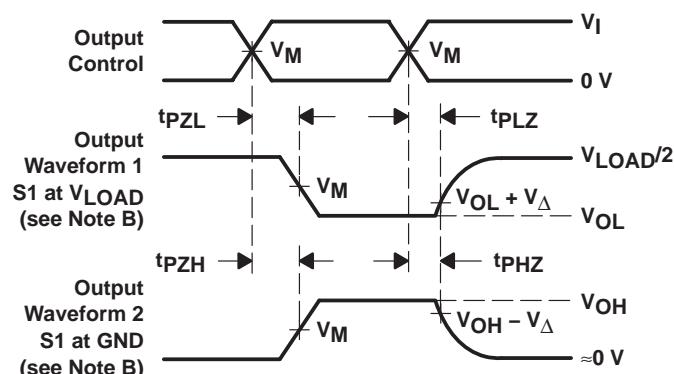
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

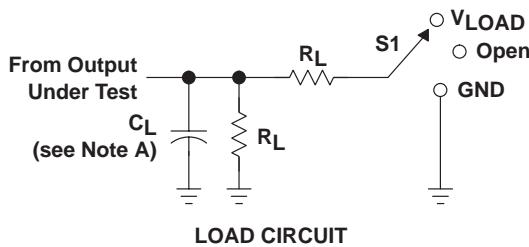
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

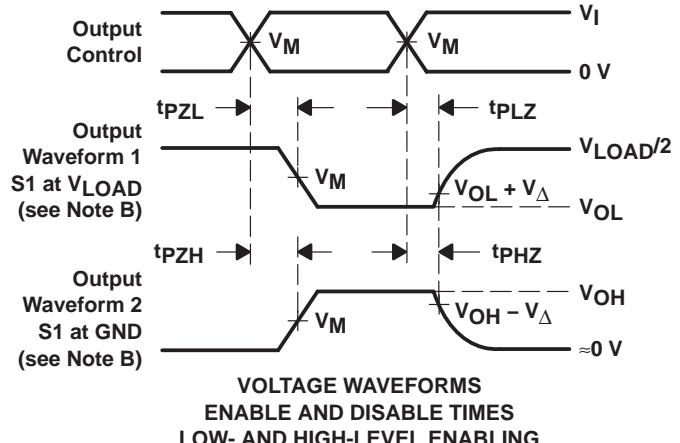
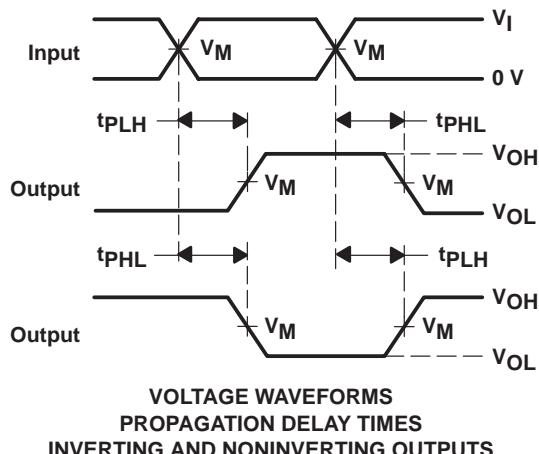
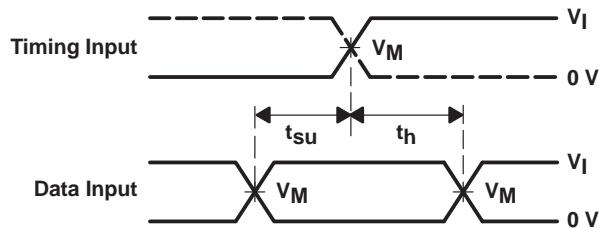
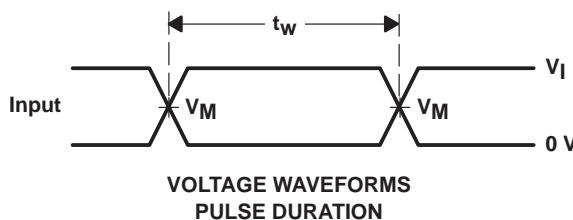


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8 V \pm 0.15 V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 V \pm 0.2 V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3 V \pm 0.3 V$	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5 V \pm 0.5 V$	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC1G86DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G86DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G86DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G86DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G86DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G86DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G86DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G86DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G86DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G86DRLR	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G86DRLRG4	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G86YEAR	ACTIVE	WCSP	YEA	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G86YEPR	ACTIVE	WCSP	YEP	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G86YZAR	ACTIVE	WCSP	YZA	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM
SN74LVC1G86YZPR	ACTIVE	WCSP	YZP	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

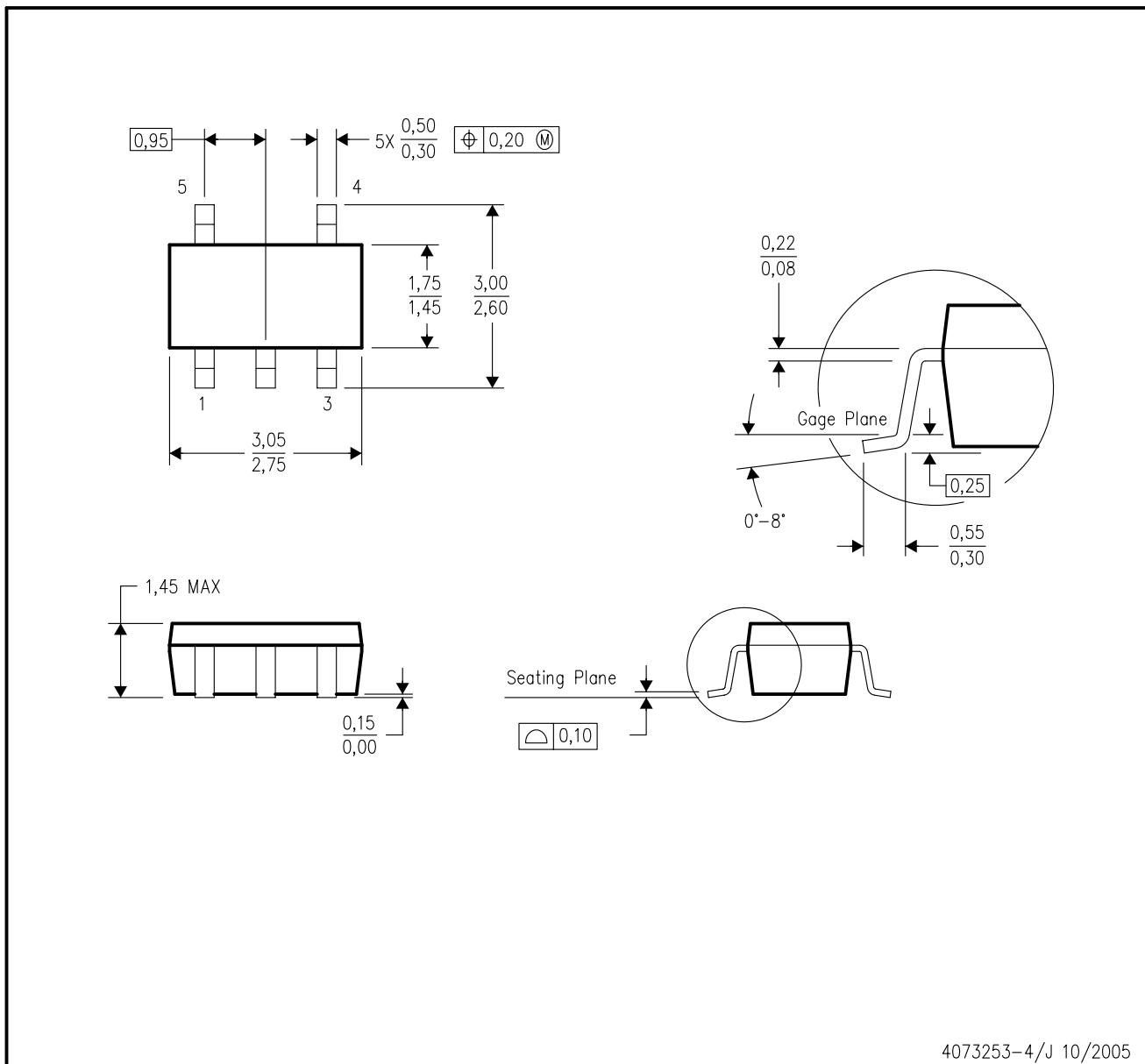
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DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

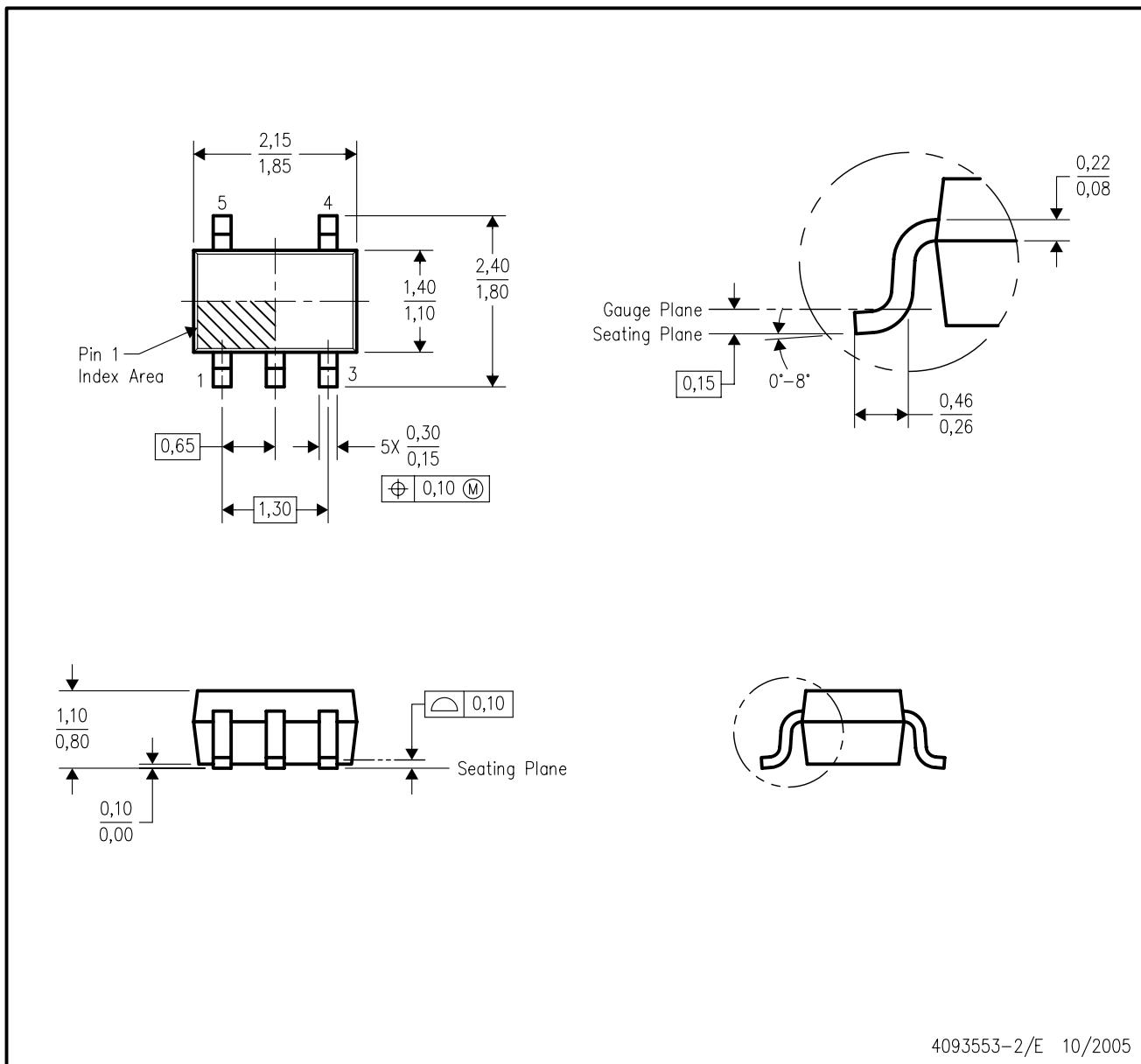


4073253-4/J 10/2005

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0,15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

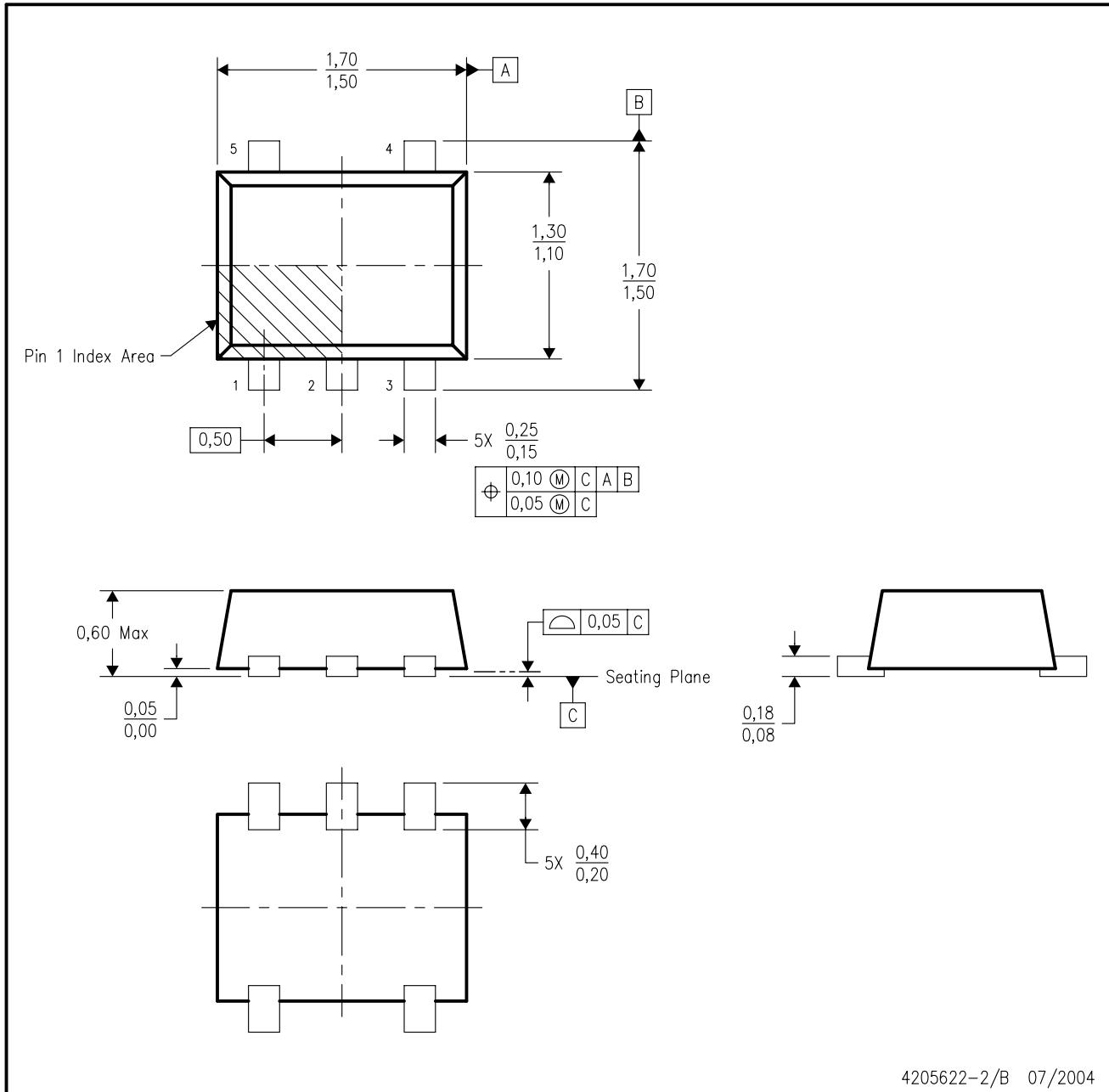


4093553-2/E 10/2005

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

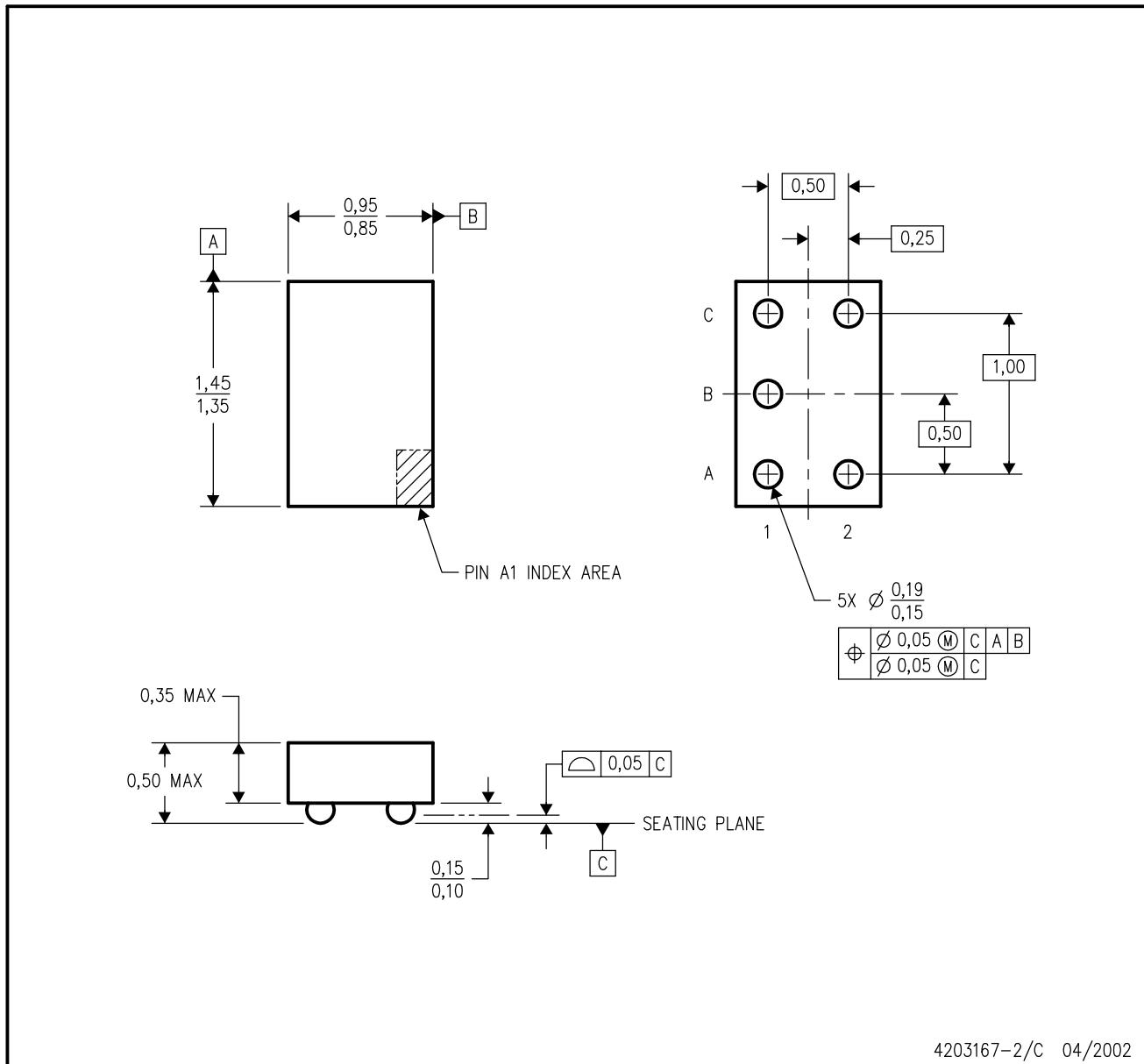


4205622-2/B 07/2004

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - JEDEC package registration is pending.

YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



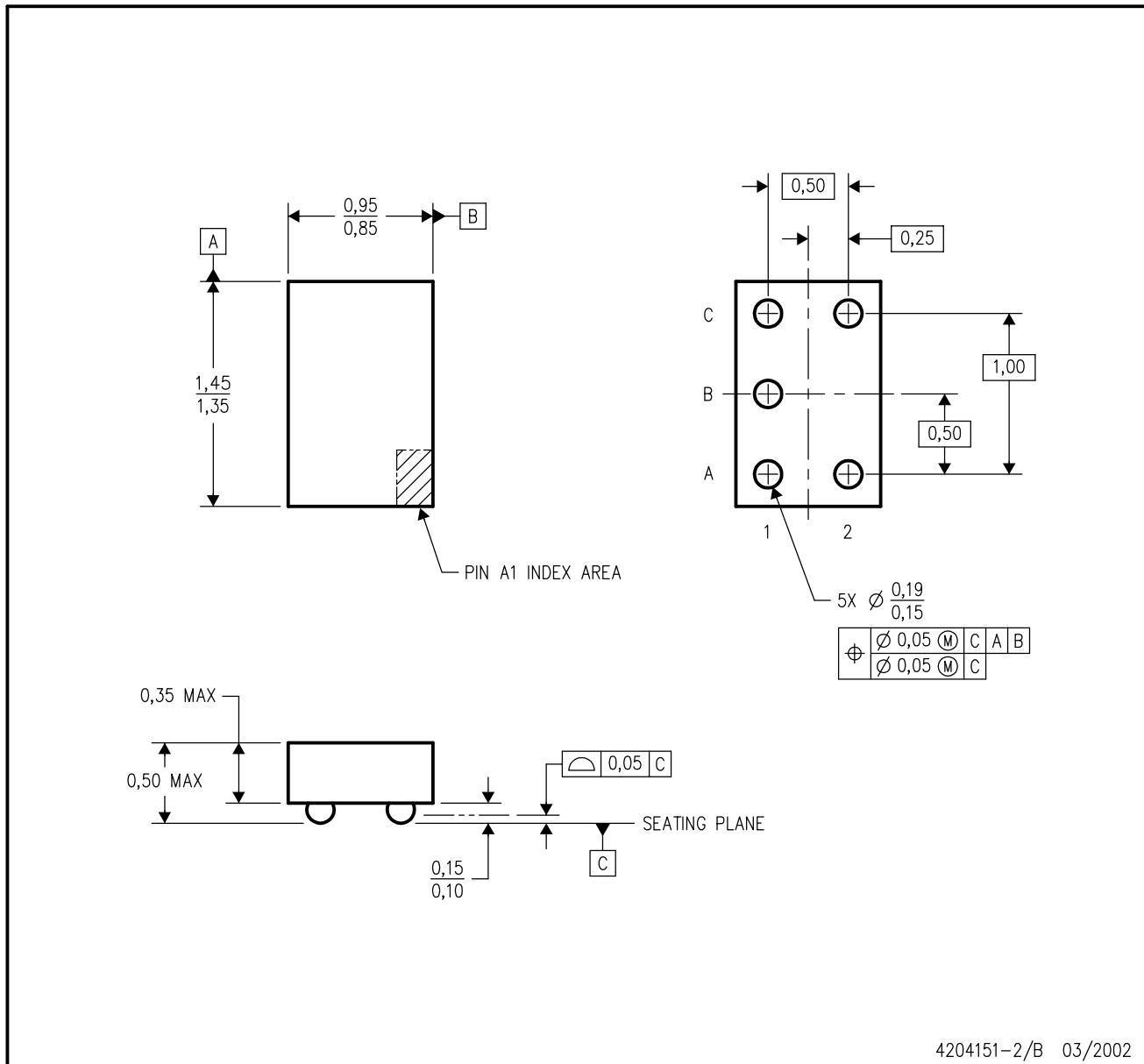
4203167-2/C 04/2002

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - NanoStar™ package configuration.
 - Package complies to JEDEC MO-211 variation EA.
 - This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.

YZA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



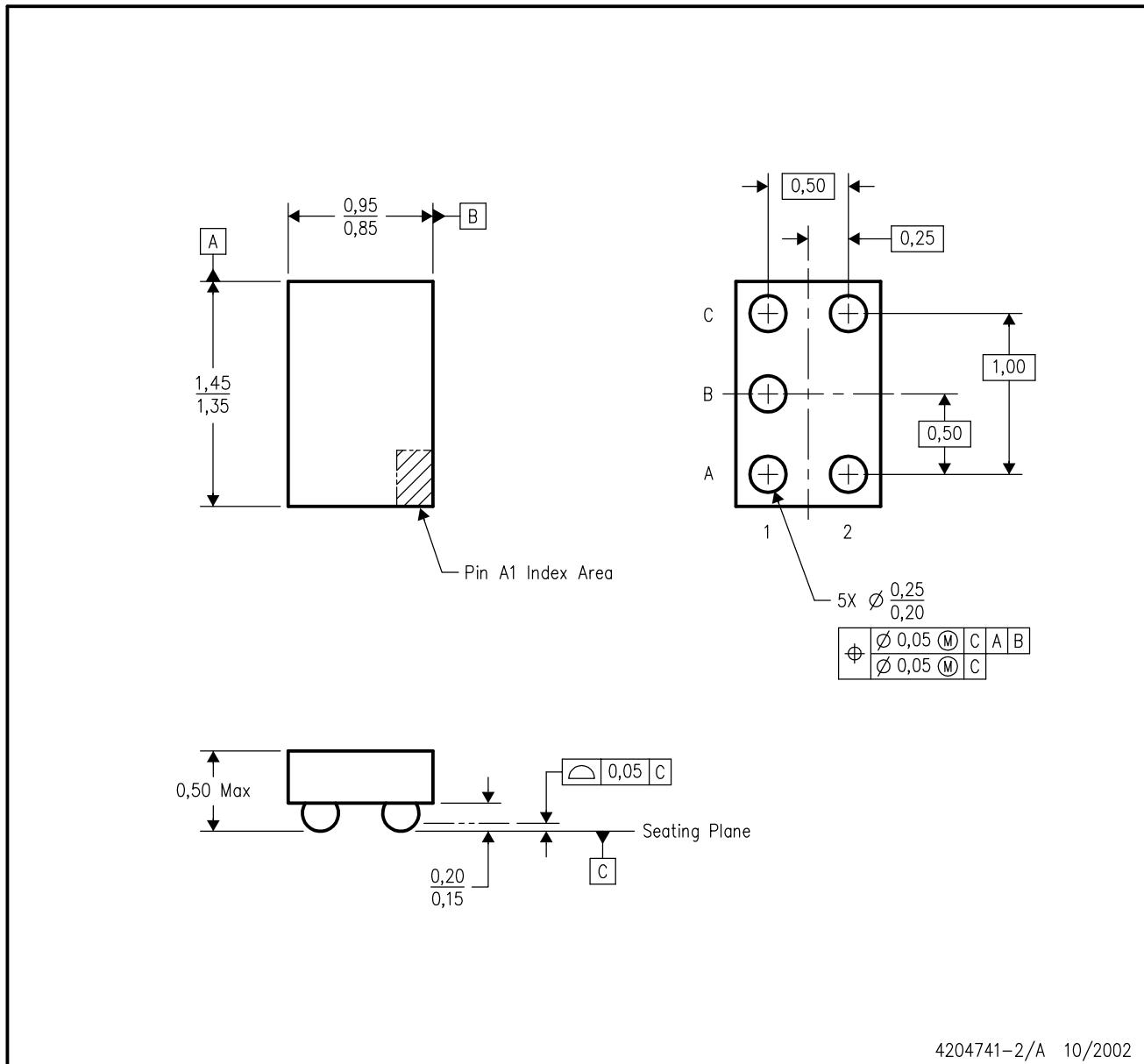
4204151-2/B 03/2002

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - NanoFree™ package configuration.
 - Package complies to JEDEC MO-211 variation EA.
 - This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



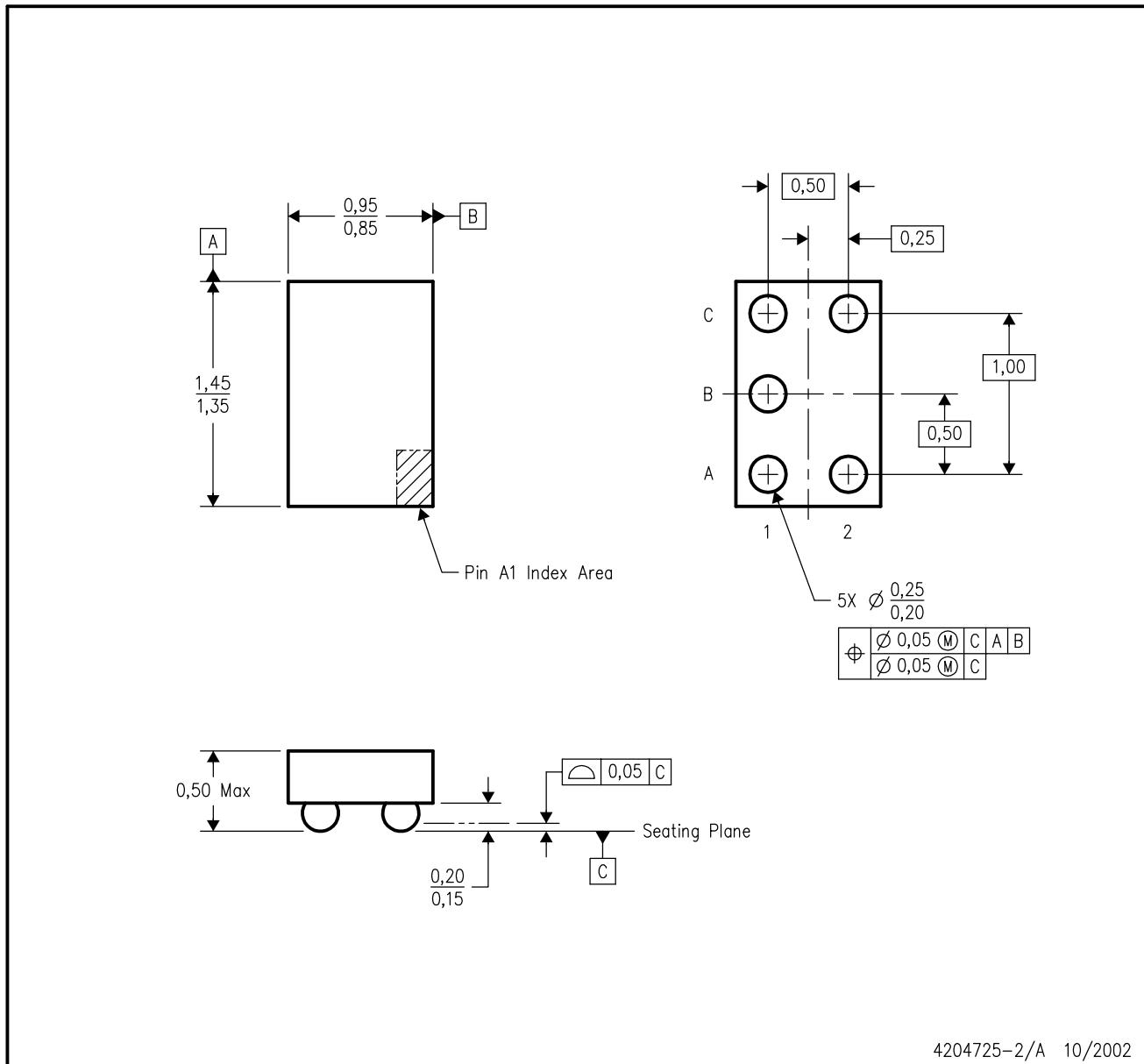
4204741-2/A 10/2002

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - NanoFree™ package configuration.
 - This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204725-2/A 10/2002

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - NanoStar™ package configuration.
 - This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

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NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price (\$US) QTY	Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74LVC1G86DBVR	ACTIVE	-40 to 85	0.12 1KU	SOT-23 (DBV) 5	View	3000	<input type="checkbox"/>	Request Free Samples
SN74LVC1G86DBVRG4	ACTIVE	-40 to 85	0.14 1KU	SOT-23 (DBV) 5	View	3000	<input type="checkbox"/>	Purchase Samples
SN74LVC1G86DBVT	ACTIVE	-40 to 85	0.47 1KU	SOT-23 (DBV) 5	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC1G86DBVTE4	ACTIVE	-40 to 85	0.47 1KU	SOT-23 (DBV) 5	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC1G86DCKR	ACTIVE	-40 to 85	0.13 1KU	SC70 (DCK) 5	View	3000	<input type="checkbox"/>	Request Free Samples
SN74LVC1G86DCKRE4	ACTIVE	-40 to 85	0.13 1KU	SC70 (DCK) 5	View	3000	<input type="checkbox"/>	Request Free Samples
SN74LVC1G86DCKRG4	ACTIVE	-40 to 85	0.15 1KU	SC70 (DCK) 5	View	3000	<input type="checkbox"/>	Purchase Samples
SN74LVC1G86DCKT	ACTIVE	-40 to 85	0.46 1KU	SC70 (DCK) 5	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC1G86DCKTE4	ACTIVE	-40 to 85	0.46 1KU	SC70 (DCK) 5	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC1G86DRLR	ACTIVE	-40 to 85	0.15 1KU	SOP (DRL) 5		4000	<input type="checkbox"/>	Request Free Samples
SN74LVC1G86DRLRG4	ACTIVE	-40 to 85	0.15 1KU	SOP (DRL) 5		4000	<input type="checkbox"/>	Request Free Samples
SN74LVC1G86YEAR	ACTIVE	-40 to 85	0.23 1KU	WCSP (YEA) 5		3000	<input type="checkbox"/>	Request Free Samples
SN74LVC1G86YEPR	ACTIVE	-40 to 85	0.23 1KU	WCSP (YEP) 5		3000	<input type="checkbox"/>	Request Free Samples
SN74LVC1G86YZAR	ACTIVE	-40 to 85	0.23 1KU	WCSP (YZA) 5		3000	<input type="checkbox"/>	Request Free Samples
SN74LVC1G86YZPR	ACTIVE	-40 to 85	0.23 1KU	WCSP (YZP) 5		3000	<input type="checkbox"/>	Request Free Samples

Inventory

		TI Inventory Status			Reported Distributor Inventory			
SN74LVC1G86DBVR		As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
	0*	1 12 Dec	6 Weeks	Americas	DigiKey	>1k	<input type="checkbox"/>	
		>10k 9 Jan		Asia	P&S	>1k	<input type="checkbox"/>	
SN74LVC1G86DBVRG4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005				
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
	0*	>10k 9 Jan	6 Weeks	None Reported		<input type="checkbox"/>	<input type="checkbox"/>	
View Distributors								
SN74LVC1G86DBVT	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005				
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	

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	0*	>10k 31 Jan	9 Weeks	Europe	Abacus Polar	250	
					Avnet-SILICA	250	
SN74LVC1G86DBVTE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 31 Jan	9 Weeks	None Reported View Distributors			
SN74LVC1G86DCKR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 23 Jan	8 Weeks	Americas	DigiKey	984	
SN74LVC1G86DCKRE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 23 Jan	8 Weeks	None Reported View Distributors			
SN74LVC1G86DCKRG4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 23 Jan	8 Weeks	None Reported View Distributors			
SN74LVC1G86DCKT	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 12 Dec	6 Weeks	Asia	P&S	144	
				Europe	Avnet-SILICA	730	
SN74LVC1G86DCKTE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 12 Dec	6 Weeks	None Reported View Distributors			
SN74LVC1G86DRLR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	8000 12 Dec	4 Weeks	Americas	DigiKey	>1k	
		>10k 4 Jan					
SN74LVC1G86DRLRG4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	8000 12 Dec	4 Weeks	None Reported View Distributors			
		>10k 4 Jan					
SN74LVC1G86YEAR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 15 Feb	10 Weeks	Americas	DigiKey	>1k	
SN74LVC1G86YEPR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 16 Feb	10 Weeks	Americas	DigiKey	>1k	
SN74LVC1G86YZAR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	>10k*	>10k 12 Dec	6 Weeks	Americas	DigiKey	>1k	

SN74LVC1G86YZPR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 13 Jan	7 Weeks	Americas	DigiKey	>1k	

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Quality & Lead (Pb)-Free Data

<input type="checkbox"/>	Product Content				MTBF/FIT Rate	
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details	
SN74LVC1G86DBVR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86DBVRG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86DBVT	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86DBVTE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86DCKR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86DCKRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86DCKRG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86DCKT	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86DCKTE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86DRLR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86DRLRG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86YEAR	TBD	SNPB	Level-1-260C-UNLIM	View	View	
SN74LVC1G86YEPR	TBD	SNPB	Level-1-260C-UNLIM	View	View	
SN74LVC1G86YZAR	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM	View	View	
SN74LVC1G86YZPR	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM	View	View	

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

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Technical Documents

<input type="checkbox"/>	Datasheets	Keep track of what's new
SN74LVC1G86 (Rev. M) (sn74lvc1g86.pdf, 490 KB)		
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Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB)		
08 Jul 2004 Abstract		
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22 Jun 2004 Abstract		
Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB)		
24 May 2004 Abstract		
Use of the CMOS Unbuffered Inverter in Oscillator Circuits (szza043.htm, 9 KB)		
06 Nov 2003 Abstract		
Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB)		
28 May 2003 Abstract		
Texas Instruments Little Logic Application Report (scea029.htm, 9 KB)		
01 Nov 2002 Abstract		
TI IBIS File Creation, Validation, and Distribution Processes (szza034.htm, 9 KB)		
29 Aug 2002 Abstract		
16-Bit Widebus Logic Families in 56-Ball, 0.65-mm Pitch Very Thin Fine-Pitch BGA (Rev. B) (szza029b.htm, 9 KB)		
22 May 2002 Abstract		
Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (szza033.htm, 9 KB)		
10 May 2002 Abstract		
Selecting the Right Texas Instruments Signal Switch (szza030.htm, 9 KB)		
07 Sep 2001 Abstract		
Implications of Slow or Floating CMOS Inputs (Rev. C) (scba004c.htm, 9 KB)		
01 Feb 1998 Abstract		

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