National Semiconductor

LM78L05IBP MICRO SMD QUALIFICATION PACKAGE

Winter 1999

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1.0 INTRODUCTION

1.1 General Product Description

The LM78L05IBP is a three terminal positive regulator with a fixed 5.0V output in the micro SMD (surface mount device) package. When used as a zener diode/resistor combination replacement, the LM78L05 is usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. The device can provide local on card regulation, eliminating the distribution problems associated with single point regulation.

Since the die is the package, the micro SMD is the smallest package possible, making it ideal for applications that can take advantage of a surface mount package that is smaller than SOT-23 and SC-70. The LM78L05 is also available in standard SO-8 and TO-92 packages. Please refer to the datasheet included in this booklet or visit National Semiconductor's website (http://www.national.com) for more information on those packages.

1.2 Technical Product Description

As with previous versions of the LM78L05, the LM78L05IBP is manufactured using National's single-layer metal bipolar process. National's name for the wafer-level chi-scale package used for the LM78L05 is micro SMD. Since assembly of the die is done at wafer level, there are additional wafer processing steps that are used instead of the usual assembly of a molded plastic surface mount package. These additional steps are covered under the Packaging Information section of this booklet.

The micro SMD version of the LM78L05 is assembled with 8 eutectic solder bumps (functioning as pins) on the active side of the die. The non-active side of the die is coated with epoxy and laser marked with a part number identification code, a die lot/date code, and a bump one identifier. The LM78L05 in micro SMD is shipped in standard 250 and 3,000 unit tape and reel. The devices are mounted on printed circuit boards bump side down using the same methods as other small surface mount packages.

For more information concerning application and use of the micro SMD package, please refer to Application Note AN-1112 included in this booklet

1.3 Reliability/Qualification Overview

The LM78L05 underwent a re-layout to provide the necessary spacing between the bond pads that enables proper surface mounting of the die. To qualify this new die, one lot of the micro SMD device was fabricated and mounted on conversion boards and went through operating life testing. Additional units were used to for human body model and machine model electrostatic discharge testing. The 8-bump micro SMD package was qualified by extension to the successful LMC6035 8-bump qualification.

1.4 Technical Assistance

Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

Europe
Fax: +49 (0) 1 80 5 30 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80 5 30 85 85
English Tel: +49 (0) 1 80 5 32 78 32

Japan
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

Asia Pacific
Fax: 65-2504466
Email: sea.support@nsc.com
Tel: 65-2544466
(IDD telephone charge to be paid by caller)

See us on the Worldwide Web @ http://www.national.com

2.0 DEVICE INFORMATION

2.1 Datasheet

National Semiconductor

September 1999

LM78LXX Series
3-Terminal Positive Regulators

General Description

The LM78LXX series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a zener diode/resistor combination replacement, the LM78LXX usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM78LXX to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment.

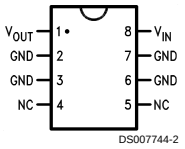
The LM78LXX is available in the plastic TO-92 (Z) package, the plastic SO-8 (M) package and a chip sized package (8-Bump micro SMD) using National's micro SMD package technology. With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistors is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Features

- LM78L05 in micro SMD package
- Output voltage tolerances of ±5% over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and plastic SO-8 low profile packages
- No external components
- Output voltages of 5.0V, 6.2V, 8.2V, 9.0V, 12V, 15V

Connection Diagrams

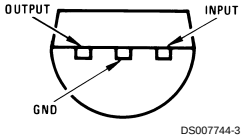
SO-8 Plastic (M)
(Narrow Body)



DS007744-2

Top View
Order Number LM78L05ACM,
LM78L12ACM or LM78L15ACM
See NS Package Number M08A

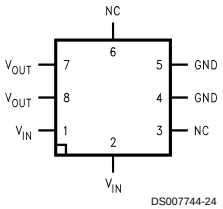
(TO-92)
Plastic Package (Z)



DS007744-3

Bottom View
Order Number
LM78L05ACZ, LM78L09ACZ,
LM78L12ACZ, LM78L15ACZ, LM78L62ACZ or
LM78L82ACZ
See NS Package Number Z03A

8-Bump micro SMD



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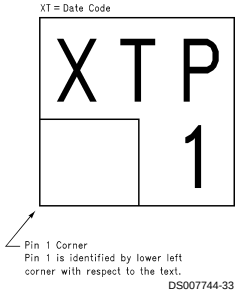
Bottom View
Order Number LM78L05IBP
or LM78L05IBPX
See NS Package Number BPA08AAA

micro SMD Marking Orientation



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Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation (Note 5)	Internally Limited
Input Voltage	35V
Storage Temperature	−65˚C to +150˚C
Operating Junction Temperature	
SO-8	0˚C to 125˚C
micro SMD	−40˚C to 85˚C
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C (lead time)
ESD Susceptibility (Note 2)	1kV

LM78LXX Electrical Characteristics

Limits in standard typeface are for T_J = 25˚C, **Bold typeface applies over 0˚C to 125˚C for SO-8 package and −40˚C to 85˚C for micro SMD package.** Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF.

LM78L05

Unless otherwise specified, V_{IN} = 10V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		4.8	5	5.2	V
		7V ≤ V_{IN} ≤ 20V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**4.75**		**5.25**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**4.75**		**5.25**	
ΔV_O	Line Regulation	7V ≤ V_{IN} ≤ 20V		18	75	mV
		8V ≤ V_{IN} ≤ 20V		10	54	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		20	60	
		1 mA ≤ I_O ≤ 40 mA		5	30	
I_Q	Quiescent Current			3	5	mA
ΔI_Q	Quiescent Current Change	8V ≤ V_{IN} ≤ 20V			**1.0**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage	f = 10 Hz to 100 kHz (Note 4)		40		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 8V ≤ V_{IN} ≤ 16V	47	62		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−0.65		mV/˚C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			6.7	7	V
θ_{JA}	Thermal Resistance (8-Bump micro SMD)			230.9		˚C/W

LM78L62AC

Unless otherwise specified, V_{IN} = 12V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		5.95	6.2	6.45	V
		8.5V ≤ V_{IN} ≤ 20V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**5.9**		**6.5**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**5.9**		**6.5**	
ΔV_O	Line Regulation	8.5V ≤ V_{IN} ≤ 20V		65	175	mV
		9V ≤ V_{IN} ≤ 20V		55	125	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		13	80	
		1 mA ≤ I_O ≤ 40 mA		6	40	

LM78L62AC (Continued)

Unless otherwise specified, V_{IN} = 12V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_Q	Quiescent Current			2	5.5	mA
ΔI_Q	Quiescent Current Change	8V ≤ V_{IN} ≤ 20V			**1.5**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage	f = 10 Hz to 100 kHz (Note 4)		50		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 10V ≤ V_{IN} ≤ 20V	40	46		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−0.75		mV/°C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			7.9		V

LM78L82AC

Unless otherwise specified, V_{IN} = 14V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		7.87	8.2	8.53	V
		11V ≤ V_{IN} ≤ 23V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**7.8**		**8.6**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**7.8**		**8.6**	
ΔV_O	Line Regulation	11V ≤ V_{IN} ≤ 23V		80	175	mV
		12V ≤ V_{IN} ≤ 23V		70	125	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		15	80	
		1 mA ≤ I_O ≤ 40 mA		8	40	
I_Q	Quiescent Current			2	5.5	mA
ΔI_Q	Quiescent Current Change	12V ≤ V_{IN} ≤ 23V			**1.5**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage	f = 10 Hz to 100 kHz (Note 4)		60		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 12V ≤ V_{IN} ≤ 22V	39	45		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−0.8		mV/°C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			9.9		V

LM78L09AC

Unless otherwise specified, V_{IN} = 15V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		8.64	9.0	9.36	V
		11.5V ≤ V_{IN} ≤ 24V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**8.55**		**9.45**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**8.55**		**9.45**	

LM78L09AC (Continued)

Unless otherwise specified, V_{IN} = 15V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ΔV_O	Line Regulation	11.5V ≤ V_{IN} ≤ 24V		100	200	mV
		13V ≤ V_{IN} ≤ 24V		90	150	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		20	90	
		1 mA ≤ I_O ≤ 40 mA		10	45	
I_Q	Quiescent Current			2	5.5	mA
ΔI_Q	Quiescent Current Change	11.5V ≤ V_{IN} ≤ 24V			**1.5**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage			70		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 15V ≤ V_{IN} ≤ 25V	38	44		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−0.9		mV/°C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			10.7		V

LM78L12AC

Unless otherwise specified, V_{IN} = 19V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		11.5	12	12.5	V
		14.5V ≤ V_{IN} ≤ 27V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**11.4**		**12.6**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**11.4**		**12.6**	
ΔV_O	Line Regulation	14.5V ≤ V_{IN} ≤ 27V		30	180	mV
		16V ≤ V_{IN} ≤ 27V		20	110	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		30	100	
		1 mA ≤ I_O ≤ 40 mA		10	50	
I_Q	Quiescent Current			3	5	mA
ΔI_Q	Quiescent Current Change	16V ≤ V_{IN} ≤ 27V			**1**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage			80		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 15V ≤ V_{IN} ≤ 25	40	54		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−1.0		mV/°C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			13.7	14.5	V

LM78L15AC

Unless otherwise specified, V_{IN} = 23V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		14.4	15.0	15.6	V
		17.5V ≤ V_{IN} ≤ 30V 1 mA ≤ I_O ≤ 40 mA (Note 3)	**14.25**		**15.75**	
		1 mA ≤ I_O ≤ 70 mA (Note 3)	**14.25**		**15.75**	
ΔV_O	Line Regulation	17.5V ≤ V_{IN} ≤ 30V		37	250	mV
		20V ≤ V_{IN} ≤ 30V		25	140	
ΔV_O	Load Regulation	1 mA ≤ I_O ≤ 100 mA		35	150	
		1 mA ≤ I_O ≤ 40 mA		12	75	
I_Q	Quiescent Current			3	5	mA
ΔI_Q	Quiescent Current Change	20V ≤ V_{IN} ≤ 30V			**1**	
		1 mA ≤ I_O ≤ 40 mA			**0.1**	
V_n	Output Noise Voltage			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 18.5V ≤ V_{IN} ≤ 28.5V	37	51		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5 mA		−1.3		mV/°C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			16.7	17.5	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device outside of its stated operating conditions.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Power dissipation ≤ 0.75W.

Note 4: Recommended minimum load capacitance of 0.01 µF to limit high frequency noise.

Note 5: Typical thermal resistance values for the packages are:

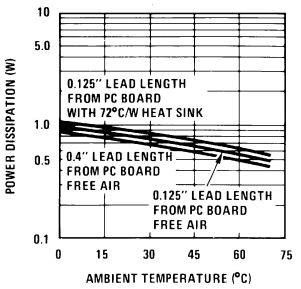
Z Package: θ_{JC} = 60 °C/W, = θ_{JA} = 230 °C/W

M Package: θ_{JA} = 180 °C/W

micro SMD Package: θ_{JA} = 230.9°C/W

Typical Performance Characteristics

Maximum Average Power Dissipation (Z Package)



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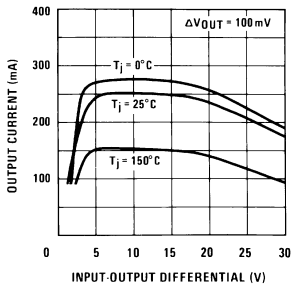
Peak Output Current



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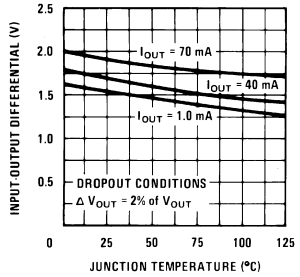
Dropout Voltage



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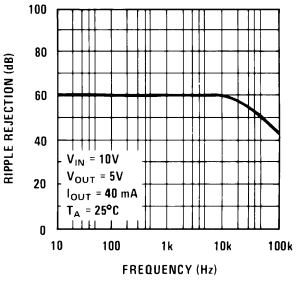
Ripple Rejection



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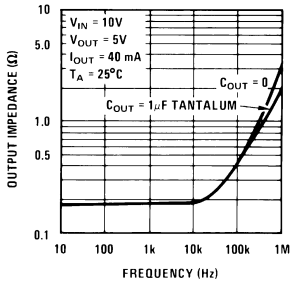
Output Impedance



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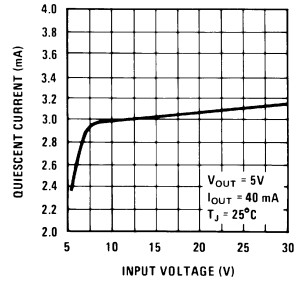
Quiescent Current



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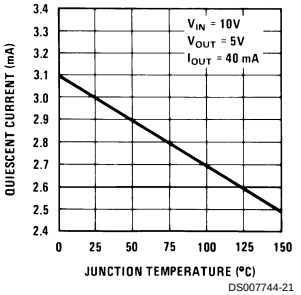
Quiescent Current



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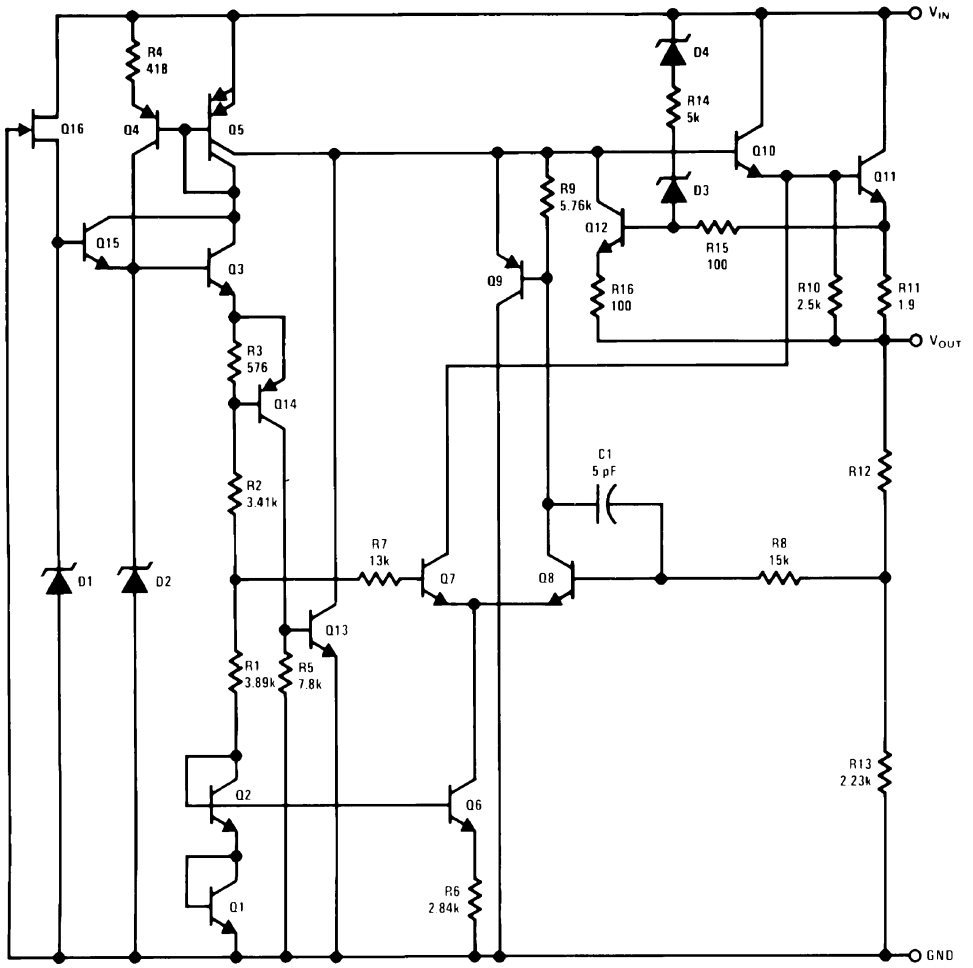
Equivalent Circuit

LM78LXX



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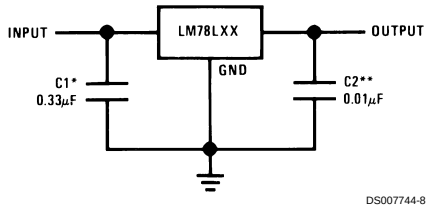
Typical Applications

Fixed Output Regulator

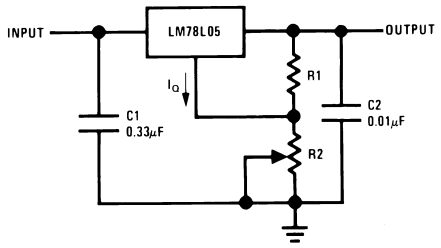


DS007744-8

*Required if the regulator is located more than 3" from the power supply filter.
**See (Note 4) in the electrical characteristics table.

Typical Applications (Continued)

Adjustable Output Regulator



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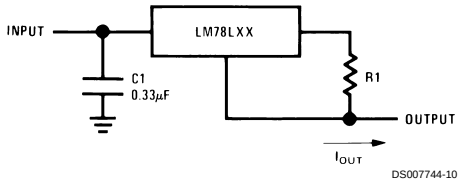
V_{OUT} = 5V + (5V/R1 + I_Q) R2
5V/R1 > 3 I_Q, load regulation (L_r) ≈ [(R1 + R2)/R1] (L_r of LM78L05)

Current Regulator



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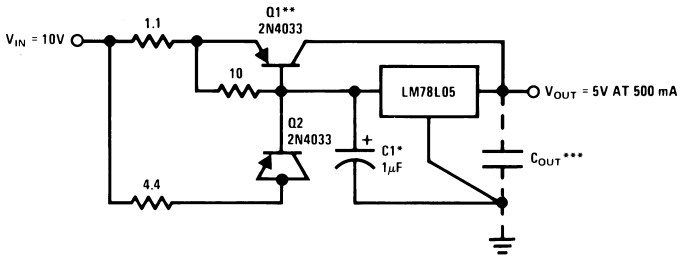
I_{OUT} = (V_{OUT}/R1) + I_Q
>I_Q = 1.5 mA over line and load changes

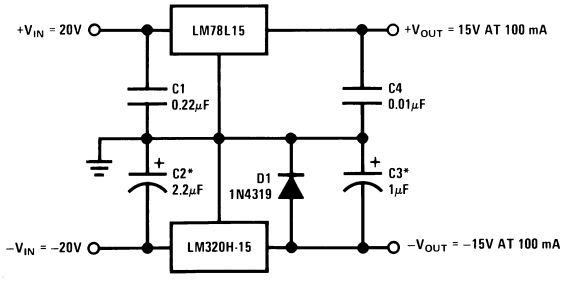
5V, 500 mA Regulator with Short Circuit Protection



DS007744-11

*Solid tantalum.
**Heat sink Q1.
***Optional: Improves ripple rejection and transient response.
Load Regulation: 0.6% 0 ≤ I_L ≤ 250 mA pulsed with t_{ON} = 50 ms.

±15V, 100 mA Dual Power Supply



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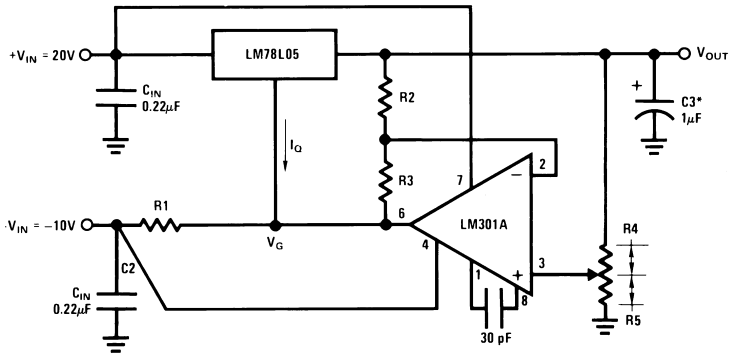
*Solid tantalum.

Typical Applications (Continued)

Variable Output Regulator 0.5V-18V



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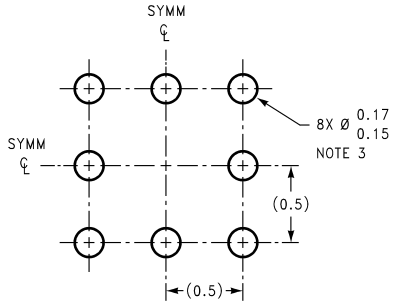
*Solid tantalum.

$V_{OUT} = V_G + 5V$, $R1 = (-V_{IN}/I_{Q\ LM78L05})$

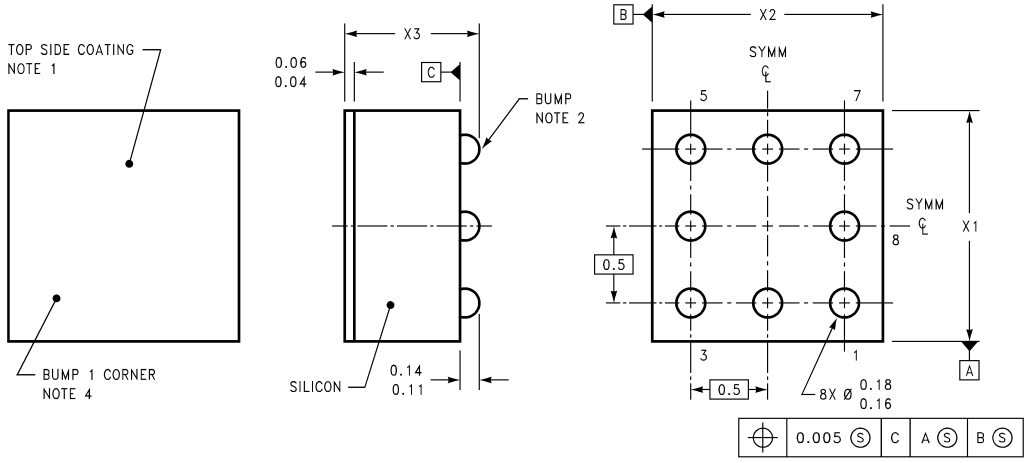
$V_{OUT} = 5V\ (R2/R4)$ for $(R2 + R3) = (R4 + R5)$

A 0.5V output will correspond to $(R2/R4) = 0.1\ (R3/R4) = 0.9$

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



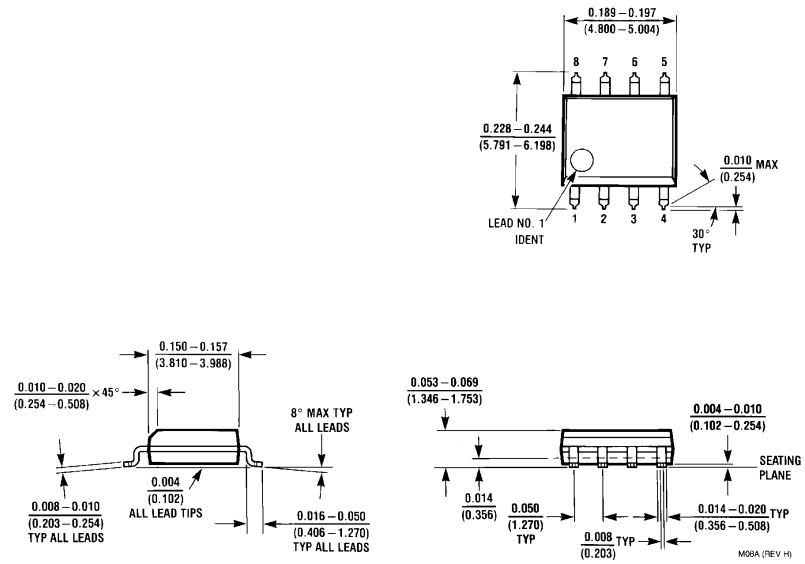
DIMENSIONS ARE IN MILLIMETERS BPA08XXX (REV A)

NOTES: UNLESS OTHERWISE SPECIFIED

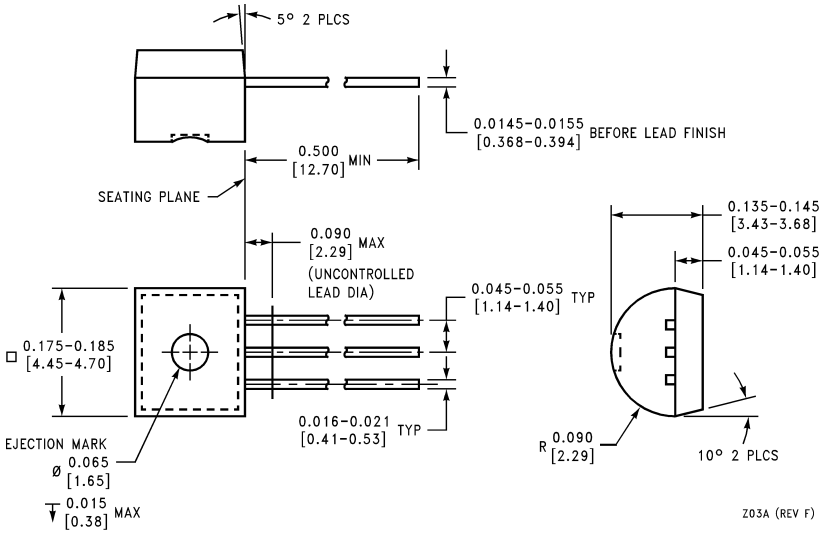
1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTERCLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X_1 IS PACKAGE WIDTH, X_2 IS PACKAGE LENGTH AND X_3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

8-Bump micro SMD
Order Number LM78L05IBP or LM78L05IBPX
NS Package Number BPA08AAA
X_1 = 1.285 X_2 = 1.285 X_3 = 0.7

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



S.O. Package (M)
Order Number LM78L05ACM, LM78L12ACM or LM78L15ACM
NS Package Number M08A



Molded Offset TO-92 (Z)
Order Number LM78L05ACZ, LM78L09ACZ, LM78L62ACZ,
LM78L82ACZ, LM78L12ACZ or LM78L15ACZ
NS Package Number Z03A

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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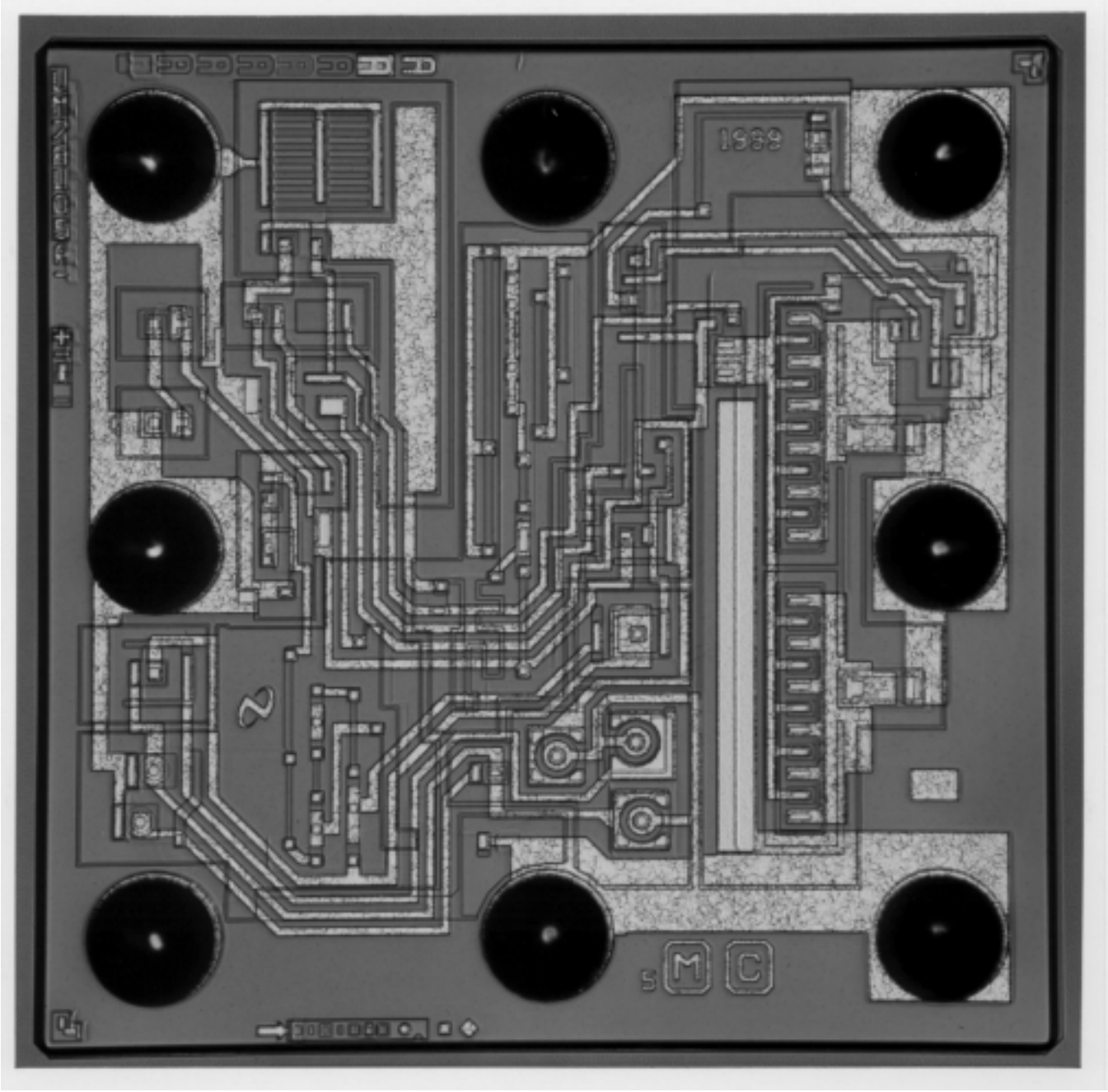
2.2 Die Photo



3.0 PROCESS INFORMATION

3.1 Process Details

Fabrication Site	Greenock, Scotland
Process Technology	Bipolar SLM
Wafer Diameter	4 inches
Number of Masks	9
Starting Material Substrate	P-type <111>
Metalization	0.5% CuAl
Passivation	10KA VOM 10KA Plasma Nitride

3.2 Masking Sequence

Mask #	Name
10	Collector
20	Isolation
30	Base
40	Emitter
41	Resistor Implant
42	Capacitor
50	Contact
60	Metal
70	Pad

3.3 Process Flow

1. Initial Oxidation
2. Mask 10
3. SB implant
4. SB drive
5. Epitaxial growth
6. Epitaxial re-oxidation
7. Mask 20
8. Iso Predeposition
9. Iso drive
10. FTA implant
11. Mask 30
12. Pre base oxidation
13. Base implant
14. Base diffusion
15. Mask 40
16. Emitter diffusion
17. Mask 41
18. Ion implant
19. VOE
20. Getter
21. Mask 42
22. Mosox
23. Mask 50
24. 0.5% CuAl sputter
25. Mask 60
26. VOM
27. Plasma Nitride
28. Mask 70
29. EOL Anneal
30. Wafer test

3.4 Micro SMD Assembly Flow

1: Receive into Bump Assembly Processing	[wafer level]
2: 2nd Passivation	[wafer level]
3: Passivation Mask	[wafer level]
4: Passivation Etch	[wafer level]
5: UBM (under bump metal) Application	[wafer level]
6: UBM Etch	[wafer level]
7: Solder Bump Application	[wafer level]
8: Solder Bump Reflow	[wafer level]
9: Epoxy Back Side	[wafer level]
10: Laser Mark Back Side	[wafer level]
11: Electric Test	[wafer level]
12: Saw Scribe Singulation	[wafer level]
13: Pack in Tape/Reel	[individual part level]

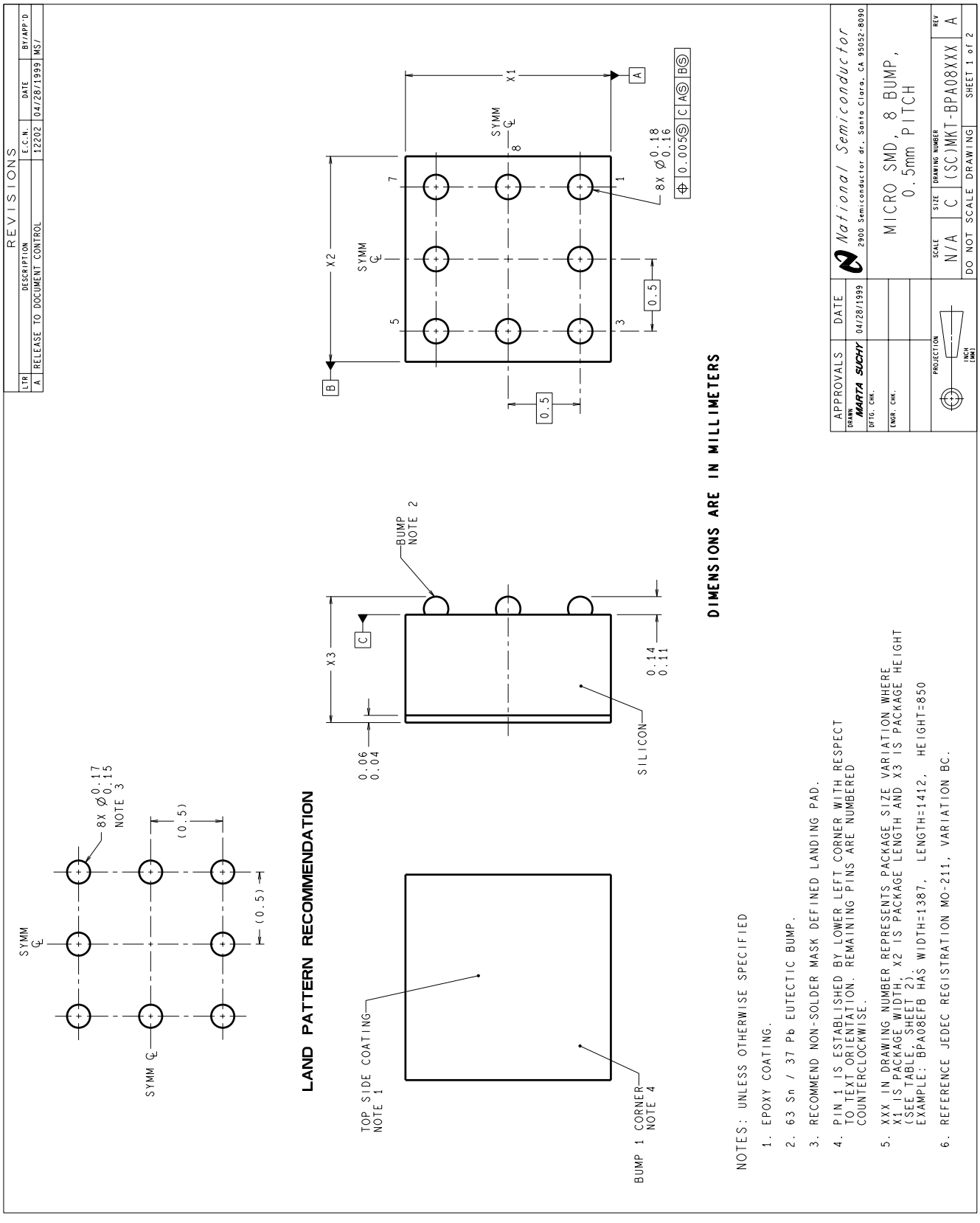
4.0 PACKAGING INFORMATION

4.1 Package Material

Generic Package Type	**8-Bump Micro SMD**
NS Package Number	BPA08AAA
Bump Material	Eutectic Solder
Bump Mechanical: Stress Buffer Material (Active side of die)	2nd Passivation
Back Side Coating Material (Non-active side of die)	Epoxy
Package Thermal	230°C/W

4.2 Package Dimensions

For LM78L05IBP use dimensions for X1 = A, X2 = A, And X3 = A.



REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
	SEE SHEET 1			

8 BUMP NOMINAL PACKAGE DIMENSIONS					
X1 DESIGNATOR	X1 PACKAGE WIDTH (±30μm)	X2 DESIGNATOR	X2 PACKAGE LENGTH (±30μm)	X3 DESIGNATOR	X3 PACKAGE HEIGHT (±50μm)
A	1285	A	1285	A	700
B	1311	B	1311	B	850
C	1336	C	1336	C	900
D	1361	D	1361		
E	1387	E	1387		
F	1412	F	1412		
G	1438	G	1438		
H	1463	H	1463		
J	1488	J	1488		
K	1514	K	1514		
L	1539	L	1539		
M	1565	M	1565		
N	1590	N	1590		
P	1615	P	1615		
Q	1641	Q	1641		
R	1666	R	1666		
S	1692	S	1692		
T	1717	T	1717		
U	1742	U	1742		
V	1768	V	1768		
W	1793	W	1793		
X	1819	X	1819		
Y	1844	Y	1844		
2	1869	2	1869		
3	1895	3	1895		
4	1920	4	1920		
5	1946	5	1946		
6	1971	6	1971		

APPROVALS	DATE
DRAWN MARTA SUCHY	04/28/1999
DFTG. CHK.	
ENGR. CHK.	

PROJECTION

INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

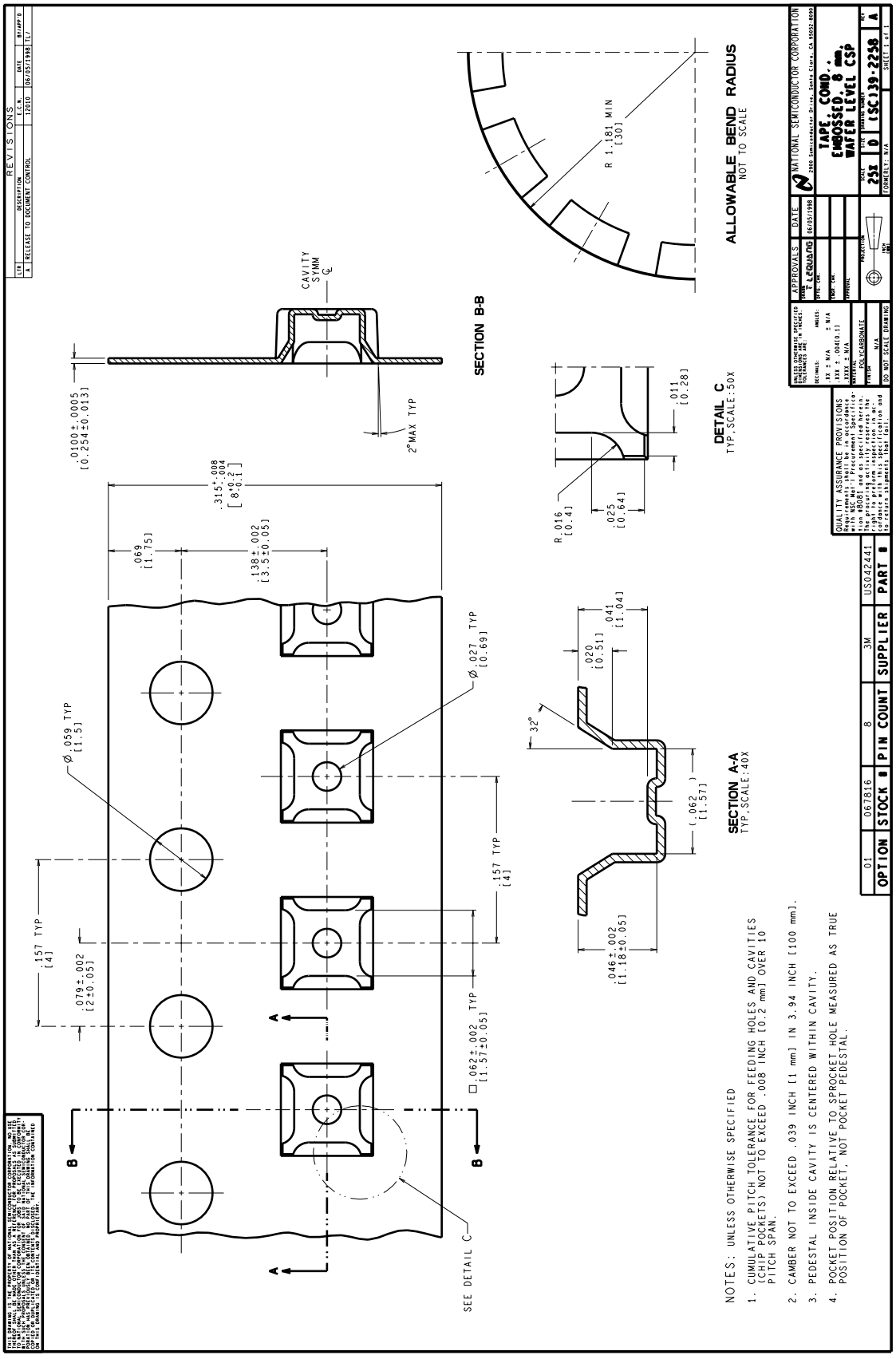
MICRO SMD, 8 BUMP, 0.5mm PITCH

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-BPA08XXX	A

DO NOT SCALE DRAWING | SHEET 2 of 2

4.3 Tape & Reel Dimensions

For LM78L05IBP see dimensions for Option #01 (Stock #067816).



5.0 RELIABILITY DATA

5.1 Reliability Report

Reliability Test Report

File Number: FSC19990252
Originator: Alex Ruiz
Date: July 14, 1999

Purpose

Qualification of the redesigned LM78L05IBP in the 8-bump micro SMD package.

Approvals

Reliability Engineer	Date
Reliability Engineering Manager	Date
Product Line Engineer	Date
Product Line Engineering Manager	Date
Product Line General Manger	Date
Product Line V.P.	Date
Corporate Reliability Director	Date
QA&R V.P.	Date

Reference File Numbers

RSC199901849
RSC199901908
Q19990190

Distribution List

Standard Analog Product Group:
CK Tai, Sharon Ignaut

QA&R:
MN Bhatt, Richard Rosales, Gil Alcaraz, Violetta Luis, Alex Ruiz

Abstract

The Micro Surface Mount Device (micro SMD) is a version of a wafer level chip scale package where the package-size is the same as that of the die. Electrical connection to the outside world is made through solder bump construction on the Aluminum bond pad, where the die is flipped to solder on to the printed circuit board. The passivation and the BCB, along with the solder bumps form a protective barrier for the active area of the die from outside world contaminants. An Epoxy back coat done to the backside of the die is used for marking.

The LM78L05IBP is re-laid out so as to provide necessary spacing between the bond pads that enables proper surface mounting of this die. To qualify this new die, one lot of the micro SMD device was fabricated and mounted on conversion boards and tested through OPL. Additional units was also ESD tested.

The 8-bump micro SMD package was qualified by extension to the successful LMC6035 8-bump qualification (Q19980548, FSC19980255).

1) The LM78L05IBP has passed 500 hours OPL with no failure.
2) After completion of all ESD testing, it was found that the device only has 1500V HBM ESD rating. This data shows that the ESD rating is better than previous control unit ESD rating. Based on the HBM ESD comparison, the redesigned die has no impact on HBM ESD capability.
3) The datasheet for the LM78L05 states 2000V HBM ESD rating – a rating higher that the current ESD data. The LM78L05 datasheet information will be change by the product line to reflect the 1000V HBM ESD capability (see FSC19990221 action item).
4) There have been zero PQAs in the last two years for ESD related failures for the LM78L05 device.

Therefore, the LM78L05IBP is being released to production with a waiver for HBM ESD performance with no corrective action required.

5.0 RELIABILITY DATA

Description

Test Request	Device Name	Sbgp	Wafer Die Run	Fab Loc	Tech Code	Pkg Code	# Leads	Assy Loc	Date Cd	Mold Cmpnd
RSC199901849	LM78L05IBP	A	HL09A23G	UK	LF	C\SSWA	8	EM	9918	N/A
RSC199901908	LM78L05IBP	A	HL09A23G	UK	LF	C\SSWA	8	EM	9918	N/A

Tests Performed

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	High Temp
RSC199901849	LM78L05IBP	A	150

Timepoints:	Test Request	TP	Duration
	RSC199901849	1	168
	RSC199901849	2	500

Test: Electrostatic Discharge – Human Body Model (ESDH)

Test Request	Device	Method
RSC199901849	LM78L05IBP	ATE
(Tst# 1)	Sublot	Voltage
	1	500
	2	1000
	3	1500
	4	2000
	5	2500

Test: Electrostatic Discharge – Machine Model (ESDM)

Test Request	Device	Method
RSC199901908	LM78L05IBP	ATE
(Tst# 1)	Sublot	Voltage
	1	50
	2	100
	3	150
	4	200
	5	250

Results/Discussion

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199901849	LM78L05IBP	A	1	168	100	0
RSC199901849	LM78L05IBP	A	2	500	100	0

Test: Electrostatic Discharge – Human Body Model (ESDH)

Test Request	Device	Sbgrp	Sublot	Voltage	SS	#Failures	#ETRejects
RSC199901849	LM78L05IBP	A	1	500	5	0	0
RSC199901849	LM78L05IBP	A	2	1000	5	0	0
RSC199901849	LM78L05IBP	A	3	1500	5	0	0
RSC199901849	LM78L05IBP	A	4	2000	5	5	5
RSC199901849	LM78L05IBP	A	5	2500	5	0	5

Test: Electrostatic Discharge – Machine Model (ESDM)

Test Request	Device	Sbgrp	Sublot	Voltage	SS	#Failures	#ETRejects
RSC199901908	LM78L05IBP	A	1	50	5	0	0
RSC199901908	LM78L05IBP	A	2	100	5	0	0
RSC199901908	LM78L05IBP	A	3	150	5	0	0
RSC199901908	LM78L05IBP	A	4	200	5	0	0
RSC199901908	LM78L05IBP	A	5	250	5	0	0

Conclusion

The LM78L05IBP micro SMD qualification has successfully satisfied all reliability requirements as per qualification plan Q19990190 with the exception of Human Body Model (HBM) ESD testing. The LM78L05IBP device is being released to production with a waiver for HBM ESD performance with no requirement for corrective action.

The LM78L05IBP device, fabbed on the NSUK BIP Linear process and packaged in the 8-bump micro SMD package, is now fully qualified and approved for production release.

6.0 APPLICATIONS DATA

6.1 Application Note

Micro SMD Wafer Level Chip Scale Package

National Semiconductor
Application Note 1112
September 1999

CONTENTS

Introduction to Micro SMD

Micro SMD is a wafer level chip scale/size package (CSP). A CSP is designed to have external package dimensions substantially equal to that of the silicon IC. Typical CSP configurations are broadly classified as one with an interposer between the silicon IC and the printed circuit board which acts as an intermediate level interconnect and another without any such interposer. Micro SMD belongs to the latter category. It is manufactured in wafer form and hence further categorized as a wafer level CSP. It extends the flip chip packaging technology to standard surface mount technology and has the following advantages:

- No need for underfill material
- Smallest footprint per I/O that results in significant real estate savings on PCB
- Leverage standard surface mount assembly technology
- Cost effective manufacturing and assembly
- Matrix interconnect layout at 0.5 mm pitch

PACKAGE CONSTRUCTION

Construction of micro SMD illustrated in *Figure 1* and *Figure 2*. It has solder bumps located in matrix layout on the active side of silicon IC. Backside of silicon is protected with proprietary protective encapsulation. The micro SMD manufacturing process steps include wafer fabrication process, wafer repassivation, deposition of eutectic solder bumps, laser based inspection of bump characteristics, application of protective encapsulation coating, wafer sort testing, laser marking, singulation and shipping in tape and reel. The package is assembled on PCB using standard surface mount assembly techniques (SMT).

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FIGURE 1. Micro SMD 4 I/O

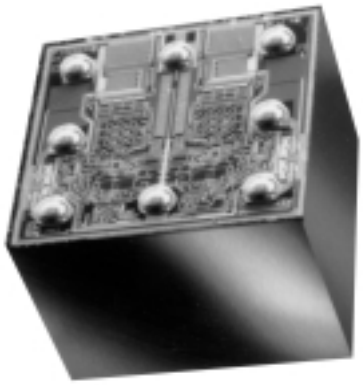

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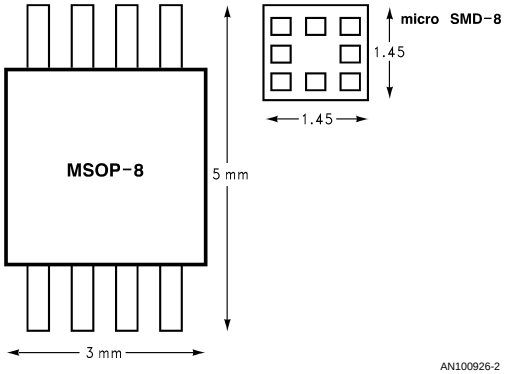
FIGURE 2. Micro SMD 8 I/O

KEY ATTRIBUTES FOR MICRO SMD 4 and 8 I/O PACKAGES

I/O Count	4	8
Pitch	0.5 mm	0.5 mm
Outline	2 x 2	3 x 3 peripheral
Weight	0.001 - 0.004 gm	0.003 - 0.007 gm
Bump Diameter	0.16 - 0.18 mm	0.16 - 0.18mm
Bump Height	0.11 - 0.14 mm	0.11 - 0.14 mm
Bump Coplanarity	±0.015 mm	±0.015 mm
Shipping Media	Tape & Reel	Tape & Reel
Desiccant Pack	Level 1	Level 1

SMALLEST FOOTPRINT

The micro SMD offers significant advantage in terms of footprints available in conventional packages. *Figure 3* compares a 8-lead MSOP - the smallest conventional surface mount 8 I/O package and the micro SMD 8 I/O. Replacing 8-lead MSOP with micro SMD 8 I/O results in 85% savings in real estate. The micro SMD footprint is at 0.5 mm matrix pitch and follows JEDEC Registered Outline M0-211 [1].



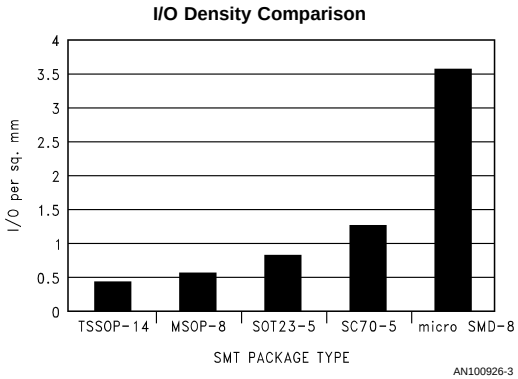


FIGURE 3. Footprint Comparison

MICRO SMD HANDLING

The micro SMD is shipped in standard polycarbonate conductive carrier tape with pressure sensitive adhesive (PSA) cover tape. The micro SMD can be ordered in quantities of 250 (7" reel) and 3000 (7" reel). *Figure 4* shows details of tape cavity design for micro SMD 8 I/O.

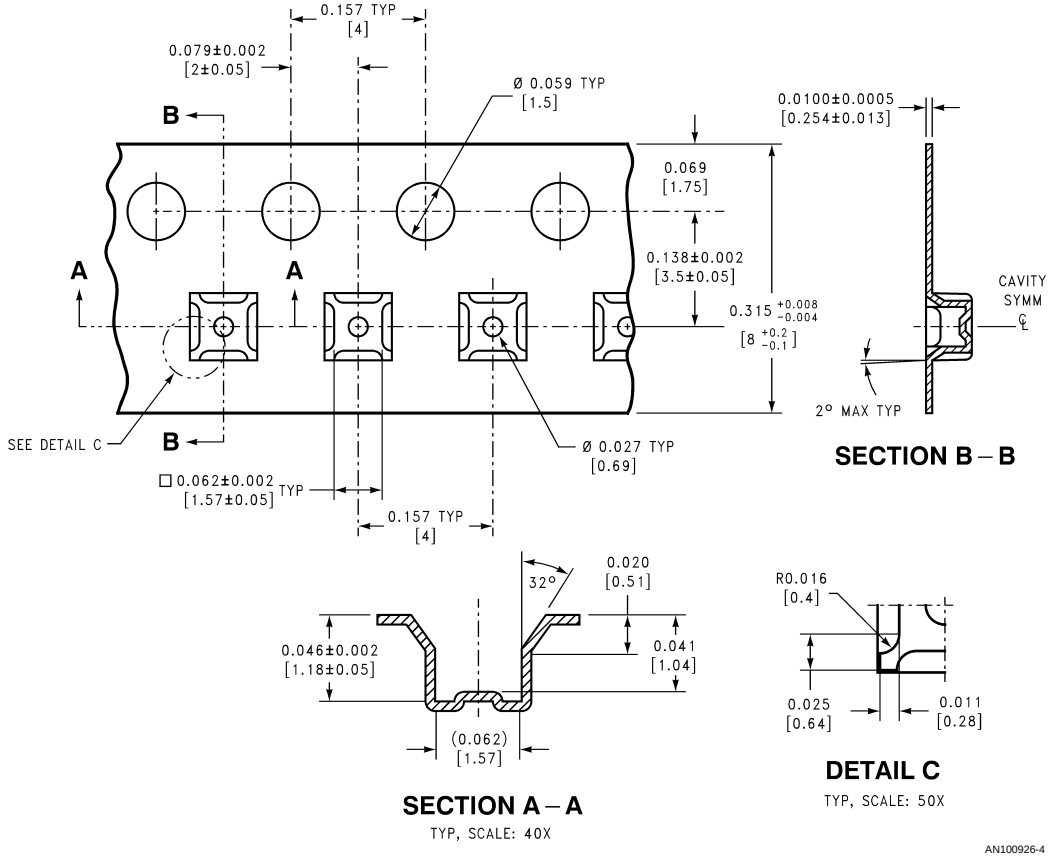


FIGURE 4. Micro SMD Tape & Reel Design

SURFACE MOUNT TECHNOLOGY (SMT) ASSEMBLY CONSIDERATIONS

The micro SMD surface mount assembly operations include printing solder paste on PCB, component placement, solder reflow and cleaning (depending on flux type). The most significant advantage of micro SMD is the ease of surface mount assembly. Contradictory to the conventional flip chip package, it can be placed on board using standard SMT pick and place equipment. Standard tape and reel shipping media facilitates package handling during assembly. Handling damage is minimal due to robust package and interconnects design. Following sections outline specific details of each SMT process step.

PRINTED CIRCUIT BOARD LAYOUT

Two types of land patterns are used for surface mount packages: (1) Solder mask defined (SMD) pads have solder mask opening smaller than metal pad; (2) Non-solder mask defined (NSMD) pads have metal pad smaller than the solder mask opening. *Figure 5* illustrates the two different types of pad geometry.

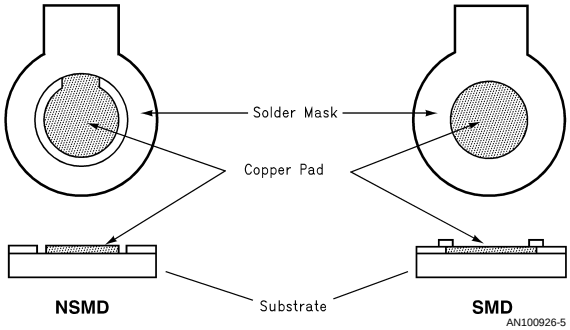


FIGURE 5. NSMD and SMD Pad Definition

NSMD definition is preferred due to tighter control on copper etch process compared to solder mask etch process. Moreover, SMD pad definition introduces stress concentration point near solder mask on the PCB side that may result in solder joint cracking under extreme fatigue conditions. Further a smaller size of copper pad in the case of NSMD definition facilitates escape routing on PCB, if necessary.

SMD pad size on package side is 0.150mm (6 mil). It is recommended to have 0.160 ±0.010 mm pad size on the PCB for optimum reliability. PCB layout assumes 0.100mm (4mil) wide trace and 0.5oz copper layer thickness. A copper pad smaller than 0.150mm may result in a reduced copper to FR4 substrate adhesion causing delamination. *Table 1* summarizes key feature dimensions.

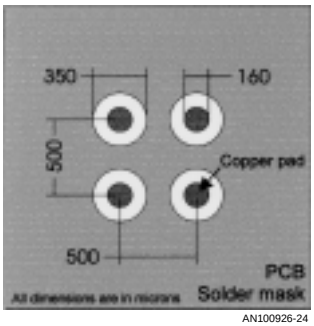
TABLE 1. SMD Pad Dimensions on PCB

Pad Definition	Copper Pad	Solder Mask Opening
NSMD	0.160 ±0.010 mm	0.350 ±0.025 mm
SMD	0.350 ±0.025 mm	0.160 ±0.010 mm

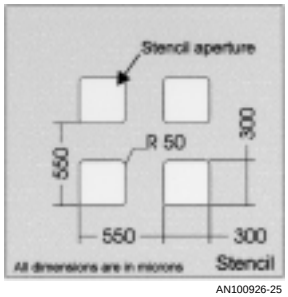
Majority of board level characterization was performed using PCB with organic solderability preservative coating (OSP) finish. A uniform coating thickness is key for high assembly yield. For an electroplated nickel-immersion gold finish, the gold thickness must be less than 0.5 micron to avoid solder joint embrittlement.

STENCIL PRINTING SOLDER PASTE

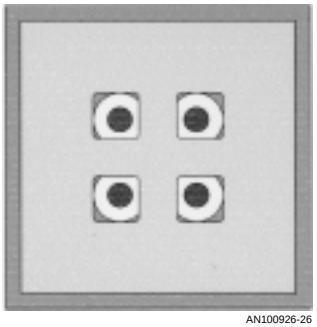
Solder paste deposition using stencil-printing process involves transferring solder paste through pre-defined apertures via application of pressure. Three typical stencil fabrication methods include chem-etch, laser cut and metal additive processes. Laser cut process followed by electro-polish process ensures tapering aperture walls that facilitate paste release. Apertures 0.275 mm X 0.275 mm or 0.300 mm X 0.300 mm square on a 0.125 mm thick laser cut stencil have consistently yielded acceptable results. *Figure 6* and *Figure 7* show sample stencil layouts for micro SMD 4 & 8 bump packages. It is recommended to offset stencil apertures from copper pad locations. This is to maximize separation between solder paste deposits in order to avoid solder bridging. A type 3 or finer solder paste is recommended. Depending on the type of solder paste used subsequent cleaning of flux may be needed. With recommended stencil parameters a vertical stand-off of 0.140 mm in the final assembly can be achieved.



Package Footprint

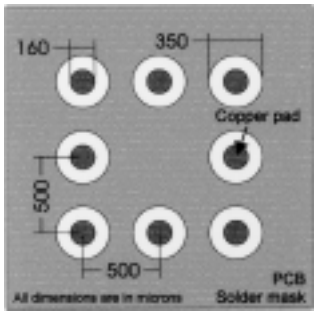


Stencil Layout



Stencil laid over PCB

FIGURE 6. Micro SMD 4 I/O PCB & Stencil Layout



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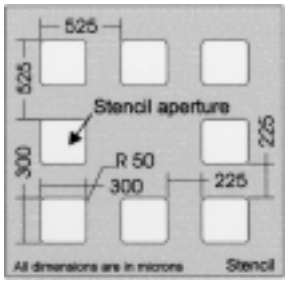
Package Footprint



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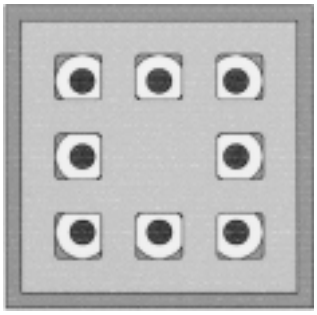
Stencil Layout



AN100926-23

Stencil laid over PCB

FIGURE 7. Micro SMD 8 I/O PCB & Stencil Layout

COMPONENT PLACEMENT

The micro SMD can be placed using standard pick and place equipment. The pick and place systems comprise of a vision system to recognize and position the component and a mechanical system to perform the pick and place operation. Two commonly used types of vision systems for bumped packages are (1) a vision system that locates package silhouette and (2) a vision system that locates individual bumps on the interconnect pattern. Latter type renders more accurate placement but tends to be more expensive and time consuming. Both methods are acceptable for micro SMD because during solder reflow the component aligns due to self-centering feature of the micro SMD solder joint. *Figure 8* illustrates the phenomenon of self-alignment when parts are intentionally placed off the actual location. Results indicate that for the prescribed stencil design (which overprints solder paste on the pad), the micro SMD is forgiving to off placements up to ±0.225 mm in X and Y directions. In the absence of solder paste on PCB (flip chip assembly), it may be off placed to an extent such that the solder bump is in contact with edge of copper pad on the PCB. In the figure it is referred to as process window for the flip chip attachment process. Published results are based on placement using *Amistar PlacePro 5800*.

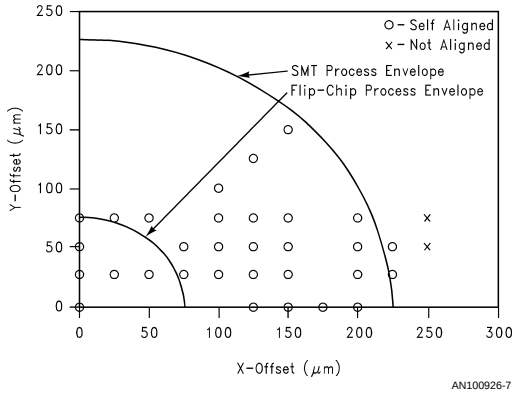


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FIGURE 8. Micro SMD Self Alignment Characteristics

SOLDER PASTE REFLOW AND CLEANING

The micro SMD may be assembled using standard SMT reflow process. Similar to any other package, thermal profile at specific board locations must be determined. Nitrogen purge is recommended during solder reflow operation. *Figure 9* illustrates a typical reflow profile. The micro SMD is qualified for up to three reflow cycles (235˚ C peak) per J-STD-020[2]. During reflow, eutectic solder bumps and the eutectic solder paste on PCB melt in presence of flux to form a cohesive shiny solder joint (*Figures 10, 11*). Depending on type of flux used the assembly may be cleaned.

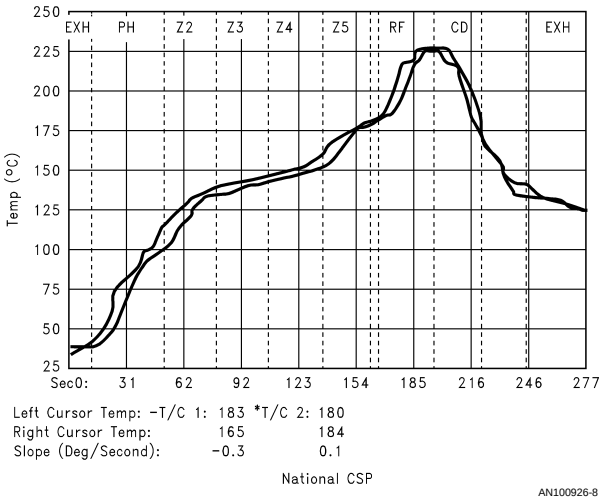

FIGURE 9. Micro SMD Reflow Profile

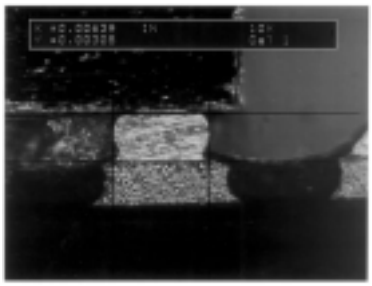

FIGURE 10. Micro SMD Solder Joint on SMD Pad

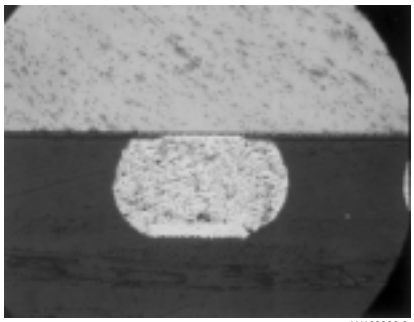

FIGURE 11. Micro SMD Solder Joint on NSMD Pad

MICRO SMD REWORK

Reworking the micro SMD part involves following the same process for reworking a typical BGA or CSP part. In order to maintain component and PC board integrity, and to obtain reliable solder connections, the rework process should duplicate the original reflow profile. For the micro SMD part, a rework system should include a localized convection heating oven with profiling capability, a bottom-side preheater, and a part placer with image overlay for alignment. The following rework process was developed using OK International's BGA-3000 Rework System [3] and can be used as a guide for developing a specific rework process.

The rework process beigns with removing the part. After establishing a rework reflow profile similar to the original reflow profile, the part can easily be removed by heating it with a convection nozzle and bottom-side preheater. Once the sol-

der has reached the liquidus point, it can be lifted off using tweezers. After the part is removed, the site is prepared by tinning the pads with a temperature controlled soldering iron. A gel flux is then applied to the pads using a small paint brush or swab. The replacement part can be picked with a vacuum needle pick-up tip. Using a prism for image overlay, the part is then aligned over the rework site and the component is placed onto the pasted site. Finally, using the convection nozzle and bottom-side preheater, reflow the part using a profile which matches the original reflow profile. For National's process, a three stage hot air convection profile at 8 litres per minute flow rate was used.

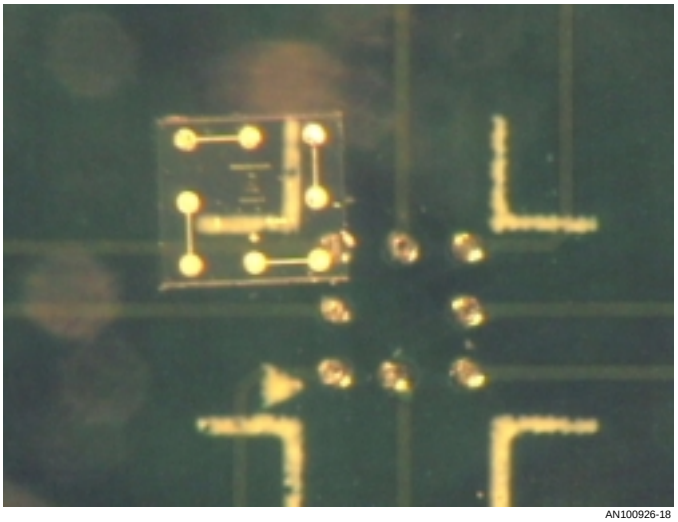

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FIGURE 12. Image overlay of 8 I/O micro SMD part

SOLDER JOINT INSPECTION

After surface mount assembly transmission X-ray can be used for sample monitoring of solder attachment process to identify defects such as bridging, shorts, opens and voids. *Figure 13* shows a typical X-ray photograph after assembly.

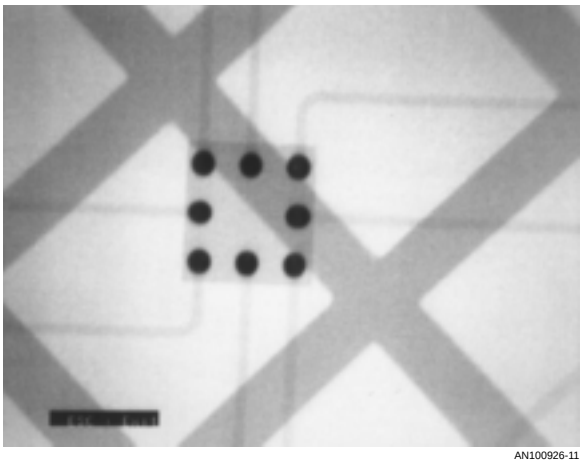

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FIGURE 13. X-Ray Inspection of micro SMD Solder Joints

MICRO SMD PACKAGE QUALIFICATION

The micro SMD package qualification plan included industry standard reliability test such as temperature cycle test (TMCL), temperature humidity bias test (THBT), biased operational life test (SOPL), and preconditioning stress (Precon). *Table 2* summarizes the qualification results.

PRECONDITIONING STRESS

Preconditioning is performed to simulate product shipping, storage and surface mount assembly operations. Micro SMD packages are subjected to the following preconditioning sequence per J-STD-020 “Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices”. [2]

1. temperature cycle – 5 cycles at −40˚C to 60˚C,
2. bake – 16 hours at 125˚C,
3. level 1 moisture soak – at 85˚C/85%RH for 168 hours,
4. 3 IR reflow passes (235˚C peak),
5. flux immersion and clean.

Packaging are subjected to preconditioning prior to THBT and TMCL testing.

TEMPERATURE HUMIDITY BIAS TEST (THBT)

THBT is designed to precipitate reliability failures of non-hermetic parts under humid environments. Typical failure mechanisms include galvanic corrosion of metal layers and threshold shifts due to moisture and contamination.

STATIC OPERATING LIFE TEST (SOPL)

SOPL accelerates oxide breakdown failures. Test is conducted at 150˚C under electrical bias.

TEMPERATURE CYCLING TEST (TMCL)

TMCL is designed to test package integrity and overall ruggedness. It tests mechanical integrity of a package when subjected to temperature cycling under conditions of −65˚C to 150˚C.

TABLE 2. Package Reliability Results

Reliability Test	Test Conditions	Test Point	Test Results		
			Lot A	Lot B	Lot C
THBT	85˚C/85% RH	1000 hours	0/77	0/77	0/77
SOPL	150˚C	500 hours	0/77	0/77	0/77
TMCL	−65˚C to 150˚C	500 cycles	0/80	0/80	0/80

SOLDER JOINT RELIABILITY

The micro SMD extends flip chip technology to cost-effective surface mount assembly. With the absence of compliant leads and underfill, it is necessary to assess solder joint reliability. Following IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments [4], daisy chain micro SMD 8 I/O parts mounted onto 4-layer FR4 PCB (0.062” thick) were subjected to temperature cycling at 0˚C to 100˚C, 1 cycle/hr. For more demanding applications such as automotive and telecom equipment further testing was conducted at −40˚C to 125˚C, 1 cycle/hr. The actual temperature profiles measured at several PCB locations are shown in *Figures 14, 15. Table 3* outlines reliability data for the two test conditions. To assess reliability of a reworked part, units with flip chip assembly process (without solder paste printing) were tested. Following optimum assembly conditions described here, micro SMD 8 I/O can pass 2300 cycles under 0˚C to 100˚C, 1 cycle/hr and 800 cycles under −40˚C to 125˚C, 1 cycle/hr without any failure (*Figure 16*).

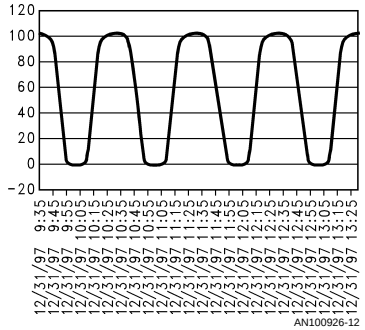

FIGURE 14. 0˚C to 100˚C, 1 cycle/hr Temperature Cycling Profile

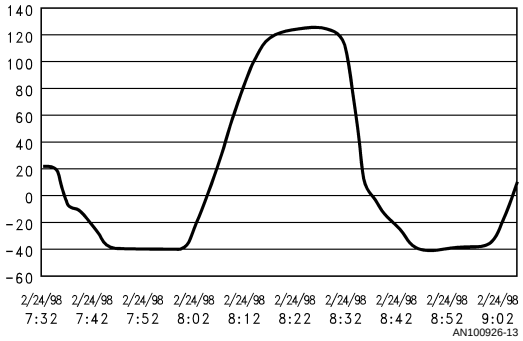

FIGURE 15. −40˚C to 125˚C, 1 cycle/hr Temperature Cycling Profile

TABLE 3. Micro SMD Solder Joint Reliability Test Matrix

Micro-SMD Assembly	Test Condition	0 cycles	500 cycles	800 cycles	1000 cycles	2300 cycles
8 I/O SMT	0˚C to 100˚C	0/62	0/62	0/62	0/62	0/62
8 I/O Flip Chip	0˚C to 100˚C	0/64	0/64	0/64	0/64	0/64
8 I/O SMT	−40˚C to 125˚C	0/61	0/61	0/61	6/61	N/A
8 I/O Flip Chip	−40˚C to 125˚C	0/32	0/32	0/32	10/32	N/A

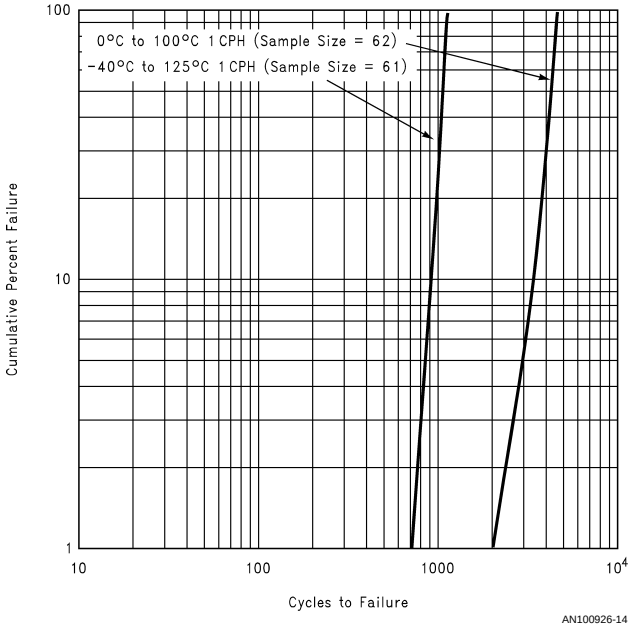

FIGURE 16. Micro SMD Solder Joint Failure Distribution

DROP TEST

Drop Test was performed on micro SMD 8 I/O package following the PC Card Environmental Test standard. Micro SMD 8 I/O assemblies (mounted on PCB) were dropped two (2) times in three (3) mutually exclusive axes from a height of 750 mm onto a noncushioning, vinyl tile surface. 20/20 samples passed the test.

THREE-POINT BEND TEST

The setup for three-point bend test of micro SMD package assemblies included a test board with a span of 100 mm. A deflection was applied at the center of the board at a rate of 9.45mm/min. *Figure 17* shows the time-deflection and time-resistance curves of the test board with the micro SMD 8 I/O. No solder joint failure was observed even with the deflection

greater than 25 mm. For this size of board, this magnitude of deflection is beyond most manufacturing, shipping, handling and operating conditions. Four boards with one unit per board were tested.

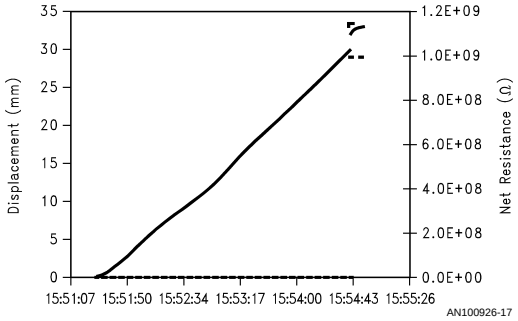

FIGURE 17. Board Deflection and Net Resistance

VIBRATION TEST

Sample size for vibration testing was 16 micro SMD 8 I/O parts mounted on PCB. Both random and sinusoidal excitations were used. Natural frequencies of sample boards were determined using the vibration shaker to sweep at very small magnitudes for a wide range of frequencies. The natural frequencies were found to range from 270 Hz to 320 Hz. The excitation of the shaker was set to perform a sinusoidal excitation with a frequency sweep between 260 Hz to 320 Hz to obtain 20G to 40G responses at the board. micro SMD 8 I/O survived 1 hour of sinusoidal vibration at 20G followed by 3 hours of sinusoidal vibration at 40G without any failure. Additionally micro SMD 8 I/O also passed 3 hours of 2G RMS random vibration with frequencies ranging from 20 Hz to 2000 Hz.

THERMAL CHARACTERIZATION

Thermal performance of micro SMD 4 and 8 I/O packages was assessed using a low effective thermal conductivity test board fabricated per EIA/JESD51-3. *Table 4* summarises θ_{JA} for each package at zero air flow without any thermal enhancement. Enhancement guidelines for improved thermal performance are listed in specific product data sheet.

TABLE 4. θ_{JA} for micro SMD PACKAGES

Micro SMD Package Type	θ_{JA} (°C/W)
4 I/O	340 ± 20
8 I/O	220 ± 20

FREQUENTLY ASKED QUESTIONS

Q1:	Nominal bump/ball diameter	A1:	0.170 mm
Q2:	Pin 1 location	A2:	Laser marked on top side
Q3:	Solder pad dimension & definition	A3:	NSMD 0.160 mm ± 0.01 mm round
Q4:	Solder mask opening	A4:	0.350 mm round
Q5:	Stencil specifications	A5:	0.125 mm thick, laser cut + eletropolished, 0.275 mm square or 0.300 mm square aperture
Q6:	Solder paste specification	A6:	Type 3 paste
Q7:	Flux specification	A7:	Water soluble or no-clean
Q8:	Compatibility with 3 IR reflows	A8:	Can withstand two 235°C peak reflow followed by one 260°C peak reflow (30 sec max. dwell at peak)
Q9:	Shipping media	A9:	Tape & Reel
Q10:	Moisture sensitivity level	A10:	Level 1

REFERENCES

1. JEDEC Registered Outline M0-211-FXBGA - Die Sized Ball Grid Array
2. J-STD-020, “Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices”, October 1996.
3. “A Successful Rework Process for Chip-Scale Packages”, Paul Wood, OK International, Chip Scale Review, Vol. 2, No. 4, 1998, pp. 41–45.
4. IPC-5M-785, “Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments”, November 1992.

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